



## 1. Description

### 1.1. Project

Project Name	Multi- Function_Device_Main_GD103_V1p 00
Board Name	custom
Generated with:	STM32CubeMX 6.3.0
Date	05/27/2022

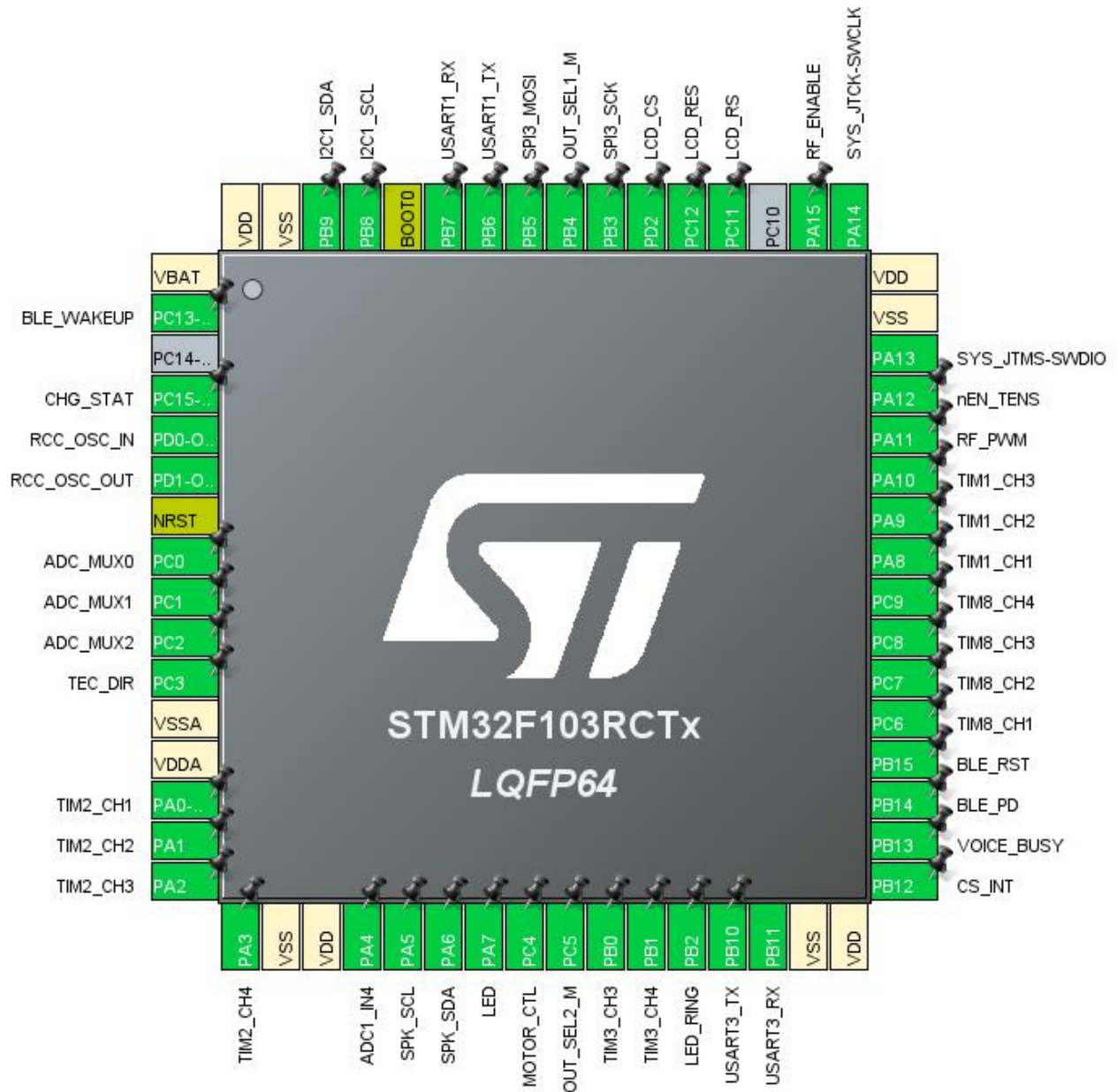
### 1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103RCTx
MCU Package	LQFP64
MCU Pin number	64

### 1.3. Core(s) information

Core(s)	Arm Cortex-M3
---------	---------------

## 2. Pinout Configuration



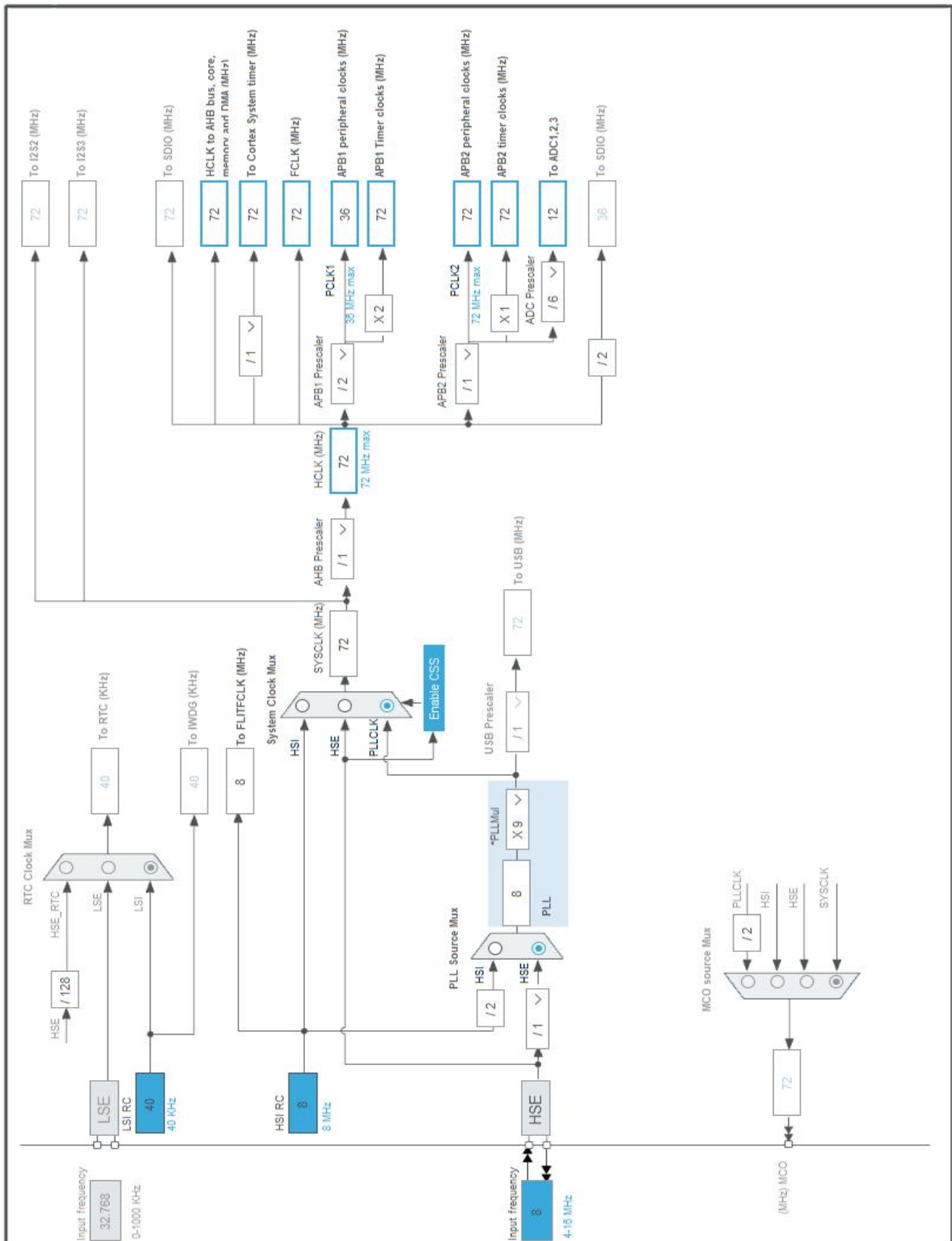
### 3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-TAMPER-RTC *	I/O	GPIO_Output	BLE_WAKEUP
4	PC15-OSC32_OUT	I/O	GPIO_EXTI15	CHG_STAT
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Output	ADC_MUX0
9	PC1 *	I/O	GPIO_Output	ADC_MUX1
10	PC2 *	I/O	GPIO_Output	ADC_MUX2
11	PC3 *	I/O	GPIO_Output	TEC_DIR
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	TIM2_CH1	
15	PA1	I/O	TIM2_CH2	
16	PA2	I/O	TIM2_CH3	
17	PA3	I/O	TIM2_CH4	
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	ADC1_IN4	
21	PA5 *	I/O	GPIO_Output	SPK_SCL
22	PA6 *	I/O	GPIO_Output	SPK_SDA
23	PA7 *	I/O	GPIO_Output	LED
24	PC4 *	I/O	GPIO_Output	MOTOR_CTL
25	PC5 *	I/O	GPIO_Output	OUT_SEL2_M
26	PB0	I/O	TIM3_CH3	
27	PB1	I/O	TIM3_CH4	
28	PB2 *	I/O	GPIO_Output	LED_RING
29	PB10	I/O	USART3_TX	
30	PB11	I/O	USART3_RX	
31	VSS	Power		
32	VDD	Power		
33	PB12	I/O	GPIO_EXTI12	CS_INT
34	PB13 *	I/O	GPIO_Input	VOICE_BUSY
35	PB14 *	I/O	GPIO_Output	BLE_PD
36	PB15 *	I/O	GPIO_Output	BLE_RST
37	PC6	I/O	TIM8_CH1	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
38	PC7	I/O	TIM8_CH2	
39	PC8	I/O	TIM8_CH3	
40	PC9	I/O	TIM8_CH4	
41	PA8	I/O	TIM1_CH1	
42	PA9	I/O	TIM1_CH2	
43	PA10	I/O	TIM1_CH3	
44	PA11	I/O	TIM1_CH4	RF_PWM
45	PA12 *	I/O	GPIO_Output	nEN_TENS
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
50	PA15 *	I/O	GPIO_Output	RF_ENABLE
52	PC11 *	I/O	GPIO_Output	LCD_RS
53	PC12 *	I/O	GPIO_Output	LCD_RES
54	PD2 *	I/O	GPIO_Output	LCD_CS
55	PB3	I/O	SPI3_SCK	
56	PB4 *	I/O	GPIO_Output	OUT_SEL1_M
57	PB5	I/O	SPI3_MOSI	
58	PB6	I/O	USART1_TX	
59	PB7	I/O	USART1_RX	
60	BOOT0	Boot		
61	PB8	I/O	I2C1_SCL	
62	PB9	I/O	I2C1_SDA	
63	VSS	Power		
64	VDD	Power		

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 5. Software Project

### 5.1. Project Settings

Name	Value
Project Name	Multi-Function_Device_Main_GD103_V1p00
Project Folder	C:\Users\Administrator\Downloads\Multi-
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.4
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_ADC1_Init	ADC1
4	MX_I2C1_Init	I2C1
5	MX_TIM1_Init	TIM1
6	MX_TIM2_Init	TIM2
7	MX_TIM6_Init	TIM6
8	MX_TIM8_Init	TIM8
9	MX_USART1_UART_Init	USART1
10	MX_USART3_UART_Init	USART3
11	MX_TIM3_Init	TIM3

Rank	Function Name	Peripheral Instance Name
12	MX_SPI3_Init	SPI3



## 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103RCTx
Datasheet	DS5792_Rev12

### 6.2. Parameter Selection

Temperature	25
Vdd	3.3

### 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

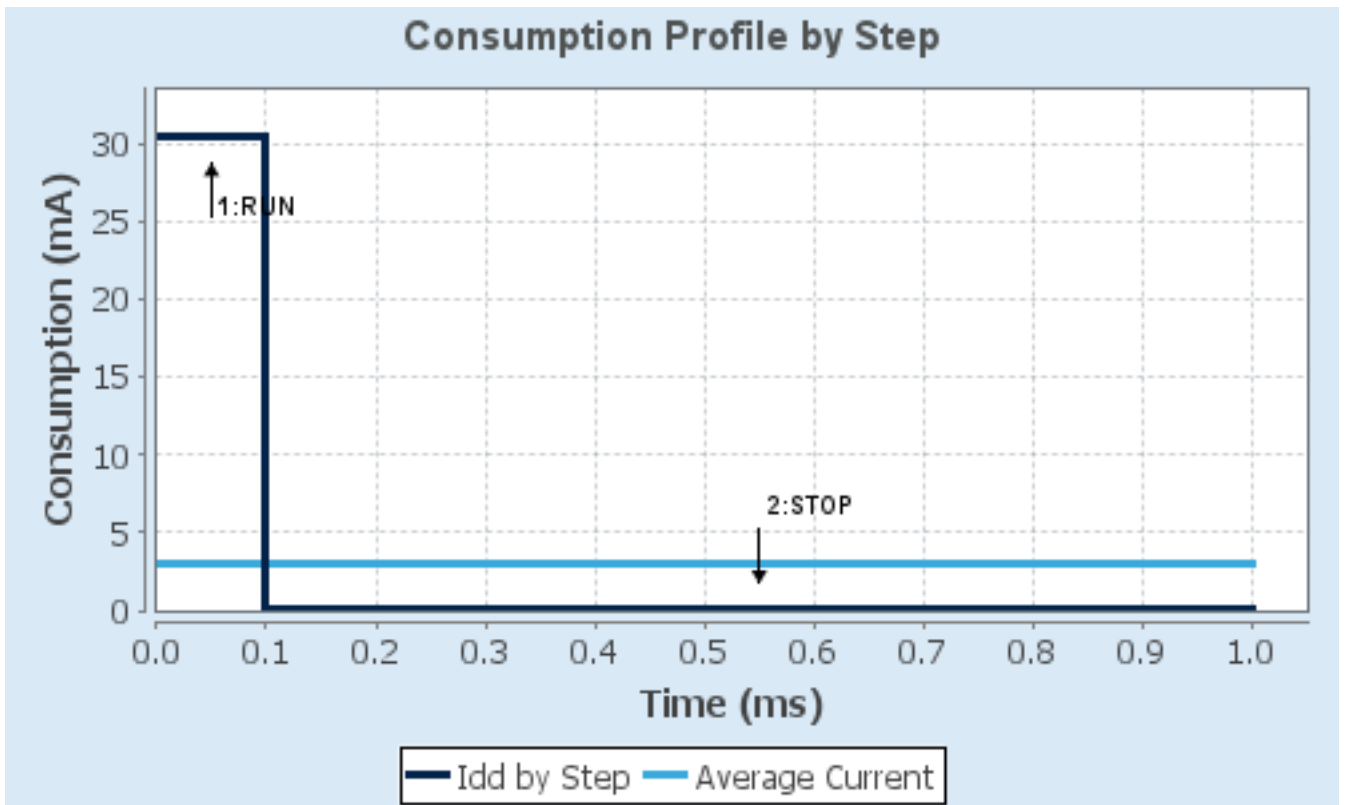
## 6.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.3	3.3
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	No Scale	No Scale
<b>Fetch Type</b>	FLASH	n/a
<b>CPU Frequency</b>	72 MHz	0 Hz
<b>Clock Configuration</b>	HSE PLL	Regulator LP
<b>Clock Source Frequency</b>	8 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	30.5 mA	25 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	90.0	0.0
<b>Ta Max</b>	100.47	105
<b>Category</b>	In DS Table	In DS Table

## 6.5. Results

Sequence Time	1 ms	Average Current	3.07 mA
Battery Life	1 month, 15 days, 15 hours	Average DMIPS	61.0 DMIPS

## 6.6. Chart



## 7. Peripherals and Middlewares Configuration

### 7.1. ADC1

**mode: IN4**

#### 7.1.1. Parameter Settings:

##### **ADCs\_Common\_Settings:**

Mode Independent mode

##### **ADC\_Settings:**

Data Alignment Right alignment

Scan Conversion Mode Disabled

Continuous Conversion Mode **Enabled \***

Discontinuous Conversion Mode Disabled

##### **ADC\_Regular\_ConversionMode:**

Enable Regular Conversions Enable

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

Rank 1

Channel Channel 4

Sampling Time 1.5 Cycles

##### **ADC\_Injected\_ConversionMode:**

Enable Injected Conversions Disable

##### **WatchDog:**

Enable Analog WatchDog Mode false

### 7.2. I2C1

**I2C: I2C**

#### 7.2.1. Parameter Settings:

##### **Master Features:**

I2C Speed Mode Standard Mode

I2C Clock Speed (Hz) 100000

##### **Slave Features:**

Clock No Stretch Mode Disabled

Primary Address Length selection 7-bit

Dual Address Acknowledged Disabled

Primary slave address 0

General Call address detection Disabled

## 7.3. RCC

### High Speed Clock (HSE): Crystal/Ceramic Resonator

#### 7.3.1. Parameter Settings:

##### System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

##### RCC Parameters:

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

## 7.4. SPI3

### Mode: Transmit Only Master

#### 7.4.1. Parameter Settings:

##### Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

##### Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	<b>18.0 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

##### Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

## 7.5. SYS

### Debug: Serial Wire

### Timebase Source: SysTick

## 7.6. TIM1

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

**Channel3: PWM Generation CH3**

**Channel4: PWM Generation CH4**

### 7.6.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)	<b>1 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>2999 *</b>
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

#### **Break And Dead Time management - BRK Configuration:**

BRK State	Disable
BRK Polarity	High

#### **Break And Dead Time management - Output Configuration:**

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

#### **PWM Generation Channel 1:**

Mode	PWM mode 1
Pulse (16 bits value)	<b>300 *</b>
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

#### **PWM Generation Channel 2:**

Mode	PWM mode 1
Pulse (16 bits value)	<b>300 *</b>
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

CH Idle State	Reset
<b>PWM Generation Channel 3:</b>	
Mode	PWM mode 1
Pulse (16 bits value)	<b>300 *</b>
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset
<b>PWM Generation Channel 4:</b>	
Mode	PWM mode 1
Pulse (16 bits value)	<b>300 *</b>
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

## 7.7. TIM2

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

**Channel3: PWM Generation CH3**

**Channel4: PWM Generation CH4**

### 7.7.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)	<b>71 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>999 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

#### **PWM Generation Channel 1:**

Mode	PWM mode 1
Pulse (16 bits value)	<b>500 *</b>
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

### PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	<b>500 *</b>
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

### PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	<b>500 *</b>
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

### PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	<b>500 *</b>
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

## 7.8. TIM3

### Channel3: PWM Generation CH3

### Channel4: PWM Generation CH4

#### 7.8.1. Parameter Settings:

#### Counter Settings:

Prescaler (PSC - 16 bits value)	<b>1 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>899 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

#### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

### PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	<b>10 *</b>
Output compare preload	Enable
Fast Mode	Disable



CH Polarity	High
<b>PWM Generation Channel 4:</b>	
Mode	PWM mode 1
Pulse (16 bits value)	<b>10 *</b>
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

## 7.9. TIM6

**mode: Activated**

### 7.9.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)	<b>71 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>999 *</b>
auto-reload preload	Disable

#### **Trigger Output (TRGO) Parameters:**

Trigger Event Selection	Reset (UG bit from TIMx_EGR)
-------------------------	------------------------------

## 7.10. TIM8

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

**Channel3: PWM Generation CH3**

**Channel4: PWM Generation CH4**

### 7.10.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)	<b>71 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>999 *</b>
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
-----------------------------	--------------------------------------------

Trigger Event Selection                      Reset (UG bit from TIMx\_EGR)

### Break And Dead Time management - BRK Configuration:

BRK State                                      Disable  
BRK Polarity                                  High

### Break And Dead Time management - Output Configuration:

Automatic Output State                      Disable  
Off State Selection for Run Mode (OSSR)      Disable  
Off State Selection for Idle Mode (OSSI)      Disable  
Lock Configuration                          Off

### PWM Generation Channel 1:

Mode                                              PWM mode 1  
Pulse (16 bits value)                      **499 \***  
Output compare preload                      Enable  
Fast Mode                                      Disable  
CH Polarity                                      High  
CH Idle State                                      Reset

### PWM Generation Channel 2:

Mode                                              PWM mode 1  
Pulse (16 bits value)                      **499 \***  
Output compare preload                      Enable  
Fast Mode                                      Disable  
CH Polarity                                      **Low \***  
CH Idle State                                      Reset

### PWM Generation Channel 3:

Mode                                              PWM mode 1  
Pulse (16 bits value)                      **499 \***  
Output compare preload                      Enable  
Fast Mode                                      Disable  
CH Polarity                                      High  
CH Idle State                                      Reset

### PWM Generation Channel 4:

Mode                                              PWM mode 1  
Pulse (16 bits value)                      **500 \***  
Output compare preload                      Enable  
Fast Mode                                      Disable  
CH Polarity                                      High  
CH Idle State                                      Reset

## 7.11. USART1

**Mode: Asynchronous**

### 7.11.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate	<b>9600 *</b>
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

#### **Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples

## 7.12. USART3

**Mode: Asynchronous**

### 7.12.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

#### **Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples

**\* User modified value**

## 8. System Configuration

### 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA4	ADC1_IN4	Analog mode	n/a	n/a	
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	n/a	High *	
	PB9	I2C1_SDA	Alternate Function Open Drain	n/a	High *	
RCC	PD0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI3	PB3	SPI3_SCK	Alternate Function Push Pull	n/a	High *	
	PB5	SPI3_MOSI	Alternate Function Push Pull	n/a	High *	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	n/a	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	n/a	Low	
	PA10	TIM1_CH3	Alternate Function Push Pull	n/a	Low	
	PA11	TIM1_CH4	Alternate Function Push Pull	n/a	Low	RF_PWM
TIM2	PA0-WKUP	TIM2_CH1	Alternate Function Push Pull	n/a	Low	
	PA1	TIM2_CH2	Alternate Function Push Pull	n/a	Low	
	PA2	TIM2_CH3	Alternate Function Push Pull	n/a	Low	
	PA3	TIM2_CH4	Alternate Function Push Pull	n/a	Low	
TIM3	PB0	TIM3_CH3	Alternate Function Push Pull	n/a	Low	
	PB1	TIM3_CH4	Alternate Function Push Pull	n/a	Low	
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	n/a	Low	
	PC7	TIM8_CH2	Alternate Function Push Pull	n/a	Low	
	PC8	TIM8_CH3	Alternate Function Push Pull	n/a	Low	
	PC9	TIM8_CH4	Alternate Function Push Pull	n/a	Low	
USART1	PB6	USART1_TX	Alternate Function Push Pull	n/a	High *	
	PB7	USART1_RX	Input mode	No pull-up and no pull-down	n/a	
USART3	PB10	USART3_TX	Alternate Function Push Pull	n/a	High *	
	PB11	USART3_RX	Input mode	No pull-up and no pull-down	n/a	
GPIO	PC13-TAMPER-RTC	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BLE_WAKEUP
	PC15-	GPIO_EXTI15	External Interrupt Mode with	No pull-up and no pull-down	n/a	CHG_STAT

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	OSC32_OUT		Rising edge trigger detection			
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ADC_MUX0
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ADC_MUX1
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ADC_MUX2
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TEC_DIR
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPK_SCL
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPK_SDA
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_CTL
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUT_SEL2_M
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_RING
	PB12	GPIO_EXTI12	<b>External Interrupt Mode with Falling edge trigger detection</b>	No pull-up and no pull-down	n/a	CS_INT
	PB13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	VOICE_BUSY
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BLE_PD
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BLE_RST
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	nEN_TENS
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RF_ENABLE
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_RS
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_RES
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_CS
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUT_SEL1_M

## 8.2. DMA configuration

nothing configured in DMA service

## 8.3. NVIC configuration

### 8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
USART1 global interrupt	true	0	0
USART3 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	0	0
TIM6 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
TIM8 break interrupt	unused		
TIM8 update interrupt	unused		
TIM8 trigger and commutation interrupts	unused		
TIM8 capture compare interrupt	unused		
SPI3 global interrupt	unused		

### 8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
USART1 global interrupt	false	true	true
USART3 global interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true
TIM6 global interrupt	false	true	true

\* User modified value

## 9. System Views

### 9.1. Category view

#### 9.1.1. Current

Middleware					
------------	--	--	--	--	--

System Core	Analog	Timers	Connectivity	Multimedia	Computing
DMA	ADC1 ✓	TIM1 ✓	I2C1 ✓		
GPIO ✓		TIM2 ✓	SPI3 ✓		
NVIC ✓		TIM3 ✓	USART1 ✓		
RCC ✓		TIM6 ✓	USART3 ✓		
SYS ✓		TIM8 ✓			



## 10. Docs & Resources

Type	Link
Datasheet	<a href="http://www.st.com/resource/en/datasheet/CD00191185.pdf">http://www.st.com/resource/en/datasheet/CD00191185.pdf</a>
Reference manual	<a href="http://www.st.com/resource/en/reference_manual/CD00171190.pdf">http://www.st.com/resource/en/reference_manual/CD00171190.pdf</a>
Programming manual	<a href="http://www.st.com/resource/en/programming_manual/CD00228163.pdf">http://www.st.com/resource/en/programming_manual/CD00228163.pdf</a>
Programming manual	<a href="http://www.st.com/resource/en/programming_manual/CD00283419.pdf">http://www.st.com/resource/en/programming_manual/CD00283419.pdf</a>
Errata sheet	<a href="http://www.st.com/resource/en/errata_sheet/CD00197763.pdf">http://www.st.com/resource/en/errata_sheet/CD00197763.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00160362.pdf">http://www.st.com/resource/en/application_note/CD00160362.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00164185.pdf">http://www.st.com/resource/en/application_note/CD00164185.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00167594.pdf">http://www.st.com/resource/en/application_note/CD00167594.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00200423.pdf">http://www.st.com/resource/en/application_note/CD00200423.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00211314.pdf">http://www.st.com/resource/en/application_note/CD00211314.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00249778.pdf">http://www.st.com/resource/en/application_note/CD00249778.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00259245.pdf">http://www.st.com/resource/en/application_note/CD00259245.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264321.pdf">http://www.st.com/resource/en/application_note/CD00264321.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264342.pdf">http://www.st.com/resource/en/application_note/CD00264342.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264379.pdf">http://www.st.com/resource/en/application_note/CD00264379.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00024853.pdf">http://www.st.com/resource/en/application_note/DM00024853.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00032987.pdf">http://www.st.com/resource/en/application_note/DM00032987.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00033267.pdf">http://www.st.com/resource/en/application_note/DM00033267.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00033344.pdf">http://www.st.com/resource/en/application_note/DM00033344.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00042534.pdf">http://www.st.com/resource/en/application_note/DM00042534.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00052530.pdf">http://www.st.com/resource/en/application_note/DM00052530.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00073742.pdf">http://www.st.com/resource/en/application_note/DM00073742.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00080497.pdf">http://www.st.com/resource/en/application_note/DM00080497.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00129215.pdf">http://www.st.com/resource/en/application_note/DM00129215.pdf</a>

Application note [http://www.st.com/resource/en/application\\_note/DM00156964.pdf](http://www.st.com/resource/en/application_note/DM00156964.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00160482.pdf](http://www.st.com/resource/en/application_note/DM00160482.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00209695.pdf](http://www.st.com/resource/en/application_note/DM00209695.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00220769.pdf](http://www.st.com/resource/en/application_note/DM00220769.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00236305.pdf](http://www.st.com/resource/en/application_note/DM00236305.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00257177.pdf](http://www.st.com/resource/en/application_note/DM00257177.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00272912.pdf](http://www.st.com/resource/en/application_note/DM00272912.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00296349.pdf](http://www.st.com/resource/en/application_note/DM00296349.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00315319.pdf](http://www.st.com/resource/en/application_note/DM00315319.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00325582.pdf](http://www.st.com/resource/en/application_note/DM00325582.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00327191.pdf](http://www.st.com/resource/en/application_note/DM00327191.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00354244.pdf](http://www.st.com/resource/en/application_note/DM00354244.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00380469.pdf](http://www.st.com/resource/en/application_note/DM00380469.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00395696.pdf](http://www.st.com/resource/en/application_note/DM00395696.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00493651.pdf](http://www.st.com/resource/en/application_note/DM00493651.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00536349.pdf](http://www.st.com/resource/en/application_note/DM00536349.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00725181.pdf](http://www.st.com/resource/en/application_note/DM00725181.pdf)