



ARM Core  
Cortex™-M0 (AT510)  
**Errata Notice**

This document contains all errata known at the date of issue in supported releases up to and including revision r0p0 of Cortex-M0.

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General suggestion for additions and improvements are also welcome.

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## Introduction

### Scope

This document describes errata categorised by level of severity. Each description includes:

- a unique defect tracking identifier
- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

### Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1	Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.
Category 2	Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.
Category 3	Behavior that was not the originally intended behavior but should not cause any problems in applications.

## **Change Control**

### **26 Mar 2009: Changes in Document v1**

First revision of document with no errata listed

## Errata Summary Table

The errata associated with this product affect product versions as below.

A cell shown thus 

<b>X</b>
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 indicates that the defect affects the revision shown at the top of that column.

## **Errata - Category 1**

**There are no Errata in this Category**



## **Errata - Category 2**

**There are no Errata in this Category**

## **Errata - Category 3**

**There are no Errata in this Category**