TSMC 90nm CLN90G Process RVT 1.0-Volt Advantage^{TM} v1.0 Standard Cell Library Databook

ARM

May 2006, Revision 1.0

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Preface

Revision History

This document contains the release history for the TSMC 90nm CLN90G Process RVT 1.0-Volt Advantage^{TM} v1.0 Standard Cell Library Databook.

Part Number	Release Number	Date of Release	Updates
DB-Advantage-TSM055-1.0/90@1.0-1.0	1.0	May 2006	Initial Release

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Introduction

ARM's Artisan Physical IP Advantage[TM] standard cell library builds upon the SAGE architecture, producing the optimum combination of high-density with high-performance. The cell line-up is derived from extensive customer design, synthesis, and place-and-route benchmark analysis. Library optimization is achieved by carefully matching the library functions and drive strengths to leading synthesis and place-and-route tools, producing superior RTL-to-GDSII results.

How This Book Is Organized

This introduction is organized into three sections:

- *Global Parameters* provides an overview of parameters specific to your Advantage library.
- *Special Cells* details the types of special cells included in the library.
- *Reading the Datasheet* describes the components of each datasheet.

Datasheets for each cell in this library are provided after the introduction. The datasheets are included in alphabetical order.

Global Parameters

This section specifies global parameters for the TSMC 90nm CLN90G Process RVT Advantage v1.0 Standard Cell Library. Some of the following sections may be covered: physical specifications, electrical specifications, derating factors, propagation delay calculation, timing constraints, power calculation, and power-rail strapping.

Physical Specifications

Table 1 shows the physical design specifications of this library.

Table 1. Physical Specifications

Drawn Gate Length (um)	0.1
Layers of Metal	4, 5, 6, 7, 8 and 9
Layout Grid (um)	0.005
Vertical Pin Grid (um)	0.28
Horizontal Pin Grid (um)	0.28
Cell Power and Ground Rail Width (um)	0.42
Cell Height (um)	2.52

In the Advantage library, all pins are located on the vertical and horizontal pin grids. Most place-and-route tools work more efficiently with all pins on grids, and some tools even require it.

The Advantage library also supports designs with four, five, six, seven, eight or nine layers of metal. You may need to change the design rules in the technology file, because the top-level metal has a greater minimum width and greater minimum spacing requirement. See "TSMC 90nm CMOS Logic Design Rule (G/GT/LP)" design rule manual. You must define these rules correctly for the place-and-route tool.

Table 2 describes the electrical specifications for this library.

Table 2. Electrical Specifications

Parameter	Minimum	Typical	Maximum
DC Supply Voltage (Vdd)	0.9V	1.0V	1.1V
Junction Temperature	-40°C	25°C	125°C

Table 3 shows the derating factors for this library.

Table 3. Derating Factors

$K_{Process}$ (slow)	1.319
$K_{Process}$ (typical)	1.000 (by definition)
$K_{Process}$ (fast)	0.759
K_{Volt} (1.0V to 0.9V)	-1.837/V
K_{Volt} (1.0V to 1.1V)	-1.213/V
K_{Temp} (25°C to -40°C)	0.00089/°C
K_{Temp} (25°C to 125°C)	0.00098/°C

Propagation Delay and Transition Time

The propagation delay through a cell is the sum of the intrinsic delay, the load-dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing 50% of Vdd and the output crossing 50% of Vdd. Figure 1 illustrates the propagation delay.

Figure 1. Propagation Delay
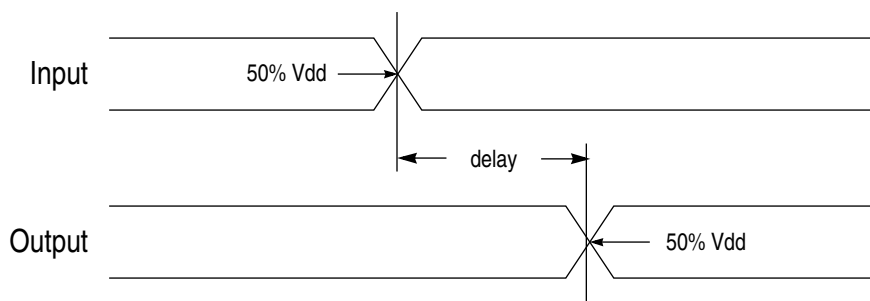
The transition times (slews) on input and output pins are defined as the time interval between the signal crossing 10% of Vdd and 90% of Vdd. Figure 2 illustrates transition time measurements for rising and falling signals.

Figure 2. Transition Time
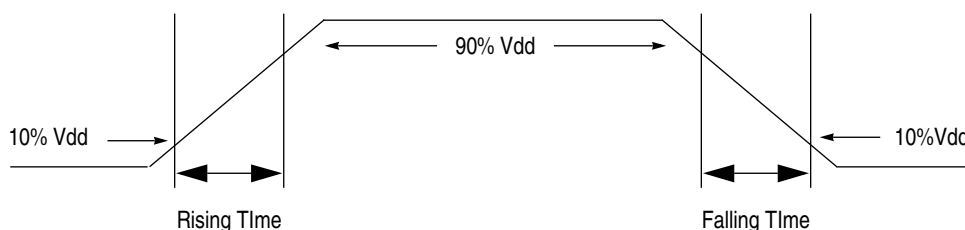
Factors that affect propagation delays and transition time include: temperature, supply voltage, process variations, fanout loading, interconnect loading, input-transition time, input-signal polarity, and timing constraints. The timing models provided with this library include the effects of input-transition time on propagation delays. Also, all timing models use a table lookup method to calculate accurate timing. To simplify calculations, the standard cell datasheets provide all timing numbers for an input slew of 0.018ns and a linearized load factor, K_{load}, which is not as accurate as the timing models. All cells have been characterized with a fully populated metal2 (0.28um horizontal pitch) and metal3 (0.28um vertical pitch) routing grid across the entire cell layout.

The Advantage library may contain negative propagation delays. Although most third-party verification tools can handle negative propagation delays, some tools will turn negative delays into a zero value.

Derating Factors

Derating factors are coefficients that the typical process characterization data is multiplied by to arrive at timing data that reflects appropriate operating conditions. The deratings table provides derating factors for variations in process case, temperature, and voltage.

Derating factors are derived by averaging the performance of many different cells in the library. A particular combination of cells may perform better or worse than indicated by these derating factors.

Delay Calculation

Using the delay data in the datasheets ($t_{intrinsic}$, K_{load}, and C_{load}) and the delay derating factors, the estimated total propagation delay is calculated as such:

$$t_{TPD} = (K_{Process}) * [1 + (K_{Volt} * \Delta Vdd)] * [1 + (K_{Temp} * \Delta T)] * t_{typical}$$

$$t_{typical} = t_{intrinsic} + (K_{load} * C_{load})$$

where:

t_{TPD} = total propagation delay (ns);

$t_{typical}$ = delay at typical corner-1.0V, 25°C, typical process (ns);

$t_{intrinsic}$ = delay through the cell when there is no output load (ns);

K_{load} = load delay multiplier (ns/pF);

C_{load} = total output load capacitance (pF);

$K_{Process}$ = process derating factor, where process is slow, typical, or fast;

K_{Volt} = voltage derating factor (/V);

ΔVdd = Vdd - 1.0V;

K_{Temp} = temperature derating factor (/°C);

ΔT = junction temperature - 25°C.

Timing Constraints

Timing constraints define minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing constraints include: setup time, hold time, recovery time, and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time and data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for 0.018ns data slew and 0.018ns clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process case variations. All cells have been characterized with a fully populated metal2 (0.28um horizontal pitch) and metal3 (0.28um vertical pitch) routing grid across the entire cell layout.

Timing constraints can affect propagation delays. The intrinsic delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, and pulse widths). The use of shorter timing constraint intervals may increase delay. Each cell is considered functional as long as the actual delay does not exceed the delay given in the datasheets by more than 10%.

Setup Time

The setup time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%. Setup-constraint values are measured as the interval between the data signal crossing 50% of Vdd for rising data (or 50% of Vdd for falling data) and the clock signal crossing 50% of Vdd for rising clocks (or 50% of Vdd for falling clocks). For the measurement of setup time, the data input signal is kept stable after the active clock edge for an infinite hold time. Figure 3 illustrates setup time for a positive-edge-triggered sequential cell.

Figure 3. Setup Time
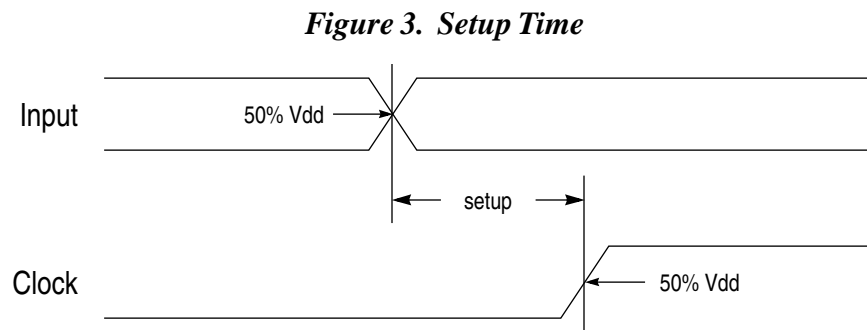
Hold Time

The hold time for a sequential cell is the minimum length of time the data-input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%. Hold-constraint values are measured as the interval between the data signal crossing 50% of Vdd for rising data (or 50% of Vdd for falling data) and the clock signal crossing 50% of Vdd for rising clocks (or 50% of Vdd for falling clocks). For the measurement of hold time, the data input signal is held stable before the active clock edge for an infinite setup time. Figure 4 illustrates hold time for a positive-edge-triggered sequential cell.

NOTE: ARM does not incorporate any hold time margins in the Synopsys, TLF, StarDC, or any other timing models. Chip designers should develop a timing methodology to account for chip-level timing inaccuracies inherent to extraction and timing analysis tools.

Figure 4. Hold Time
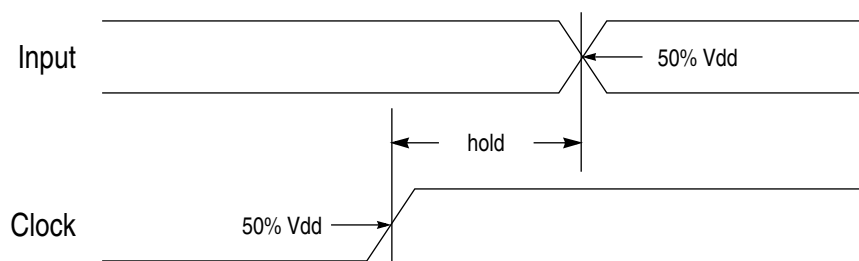
Recovery Time

Recovery time for sequential cells is the minimum length of time that the active-low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd for rising clocks (or 50% of Vdd for falling clocks). For the measurement of recovery time, the set or reset signal is held stable after the active clock edge for an infinite hold time. Figure 5 illustrates recovery time.

Figure 5. Recovery Time
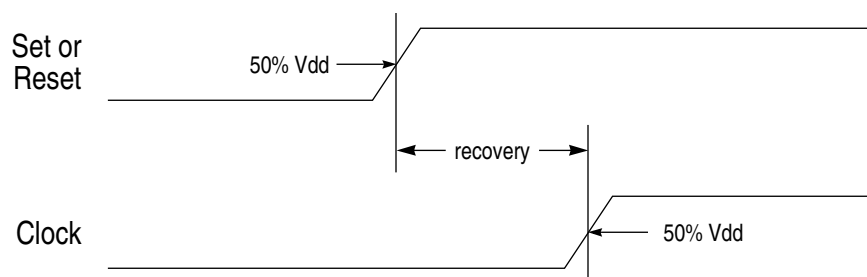
Removal Time

Removal time for sequential cells is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the active clock edge does not latch in a new data value from that programmed by the asynchronous set or reset signal. Removal constraint values are measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd for rising clocks (or 50% of Vdd for falling clocks). For the measurement of removal time, the set or reset signal is held stable before the active clock edge for an infinite setup time. Figure 6 illustrates removal time.

Figure 6. Removal Time
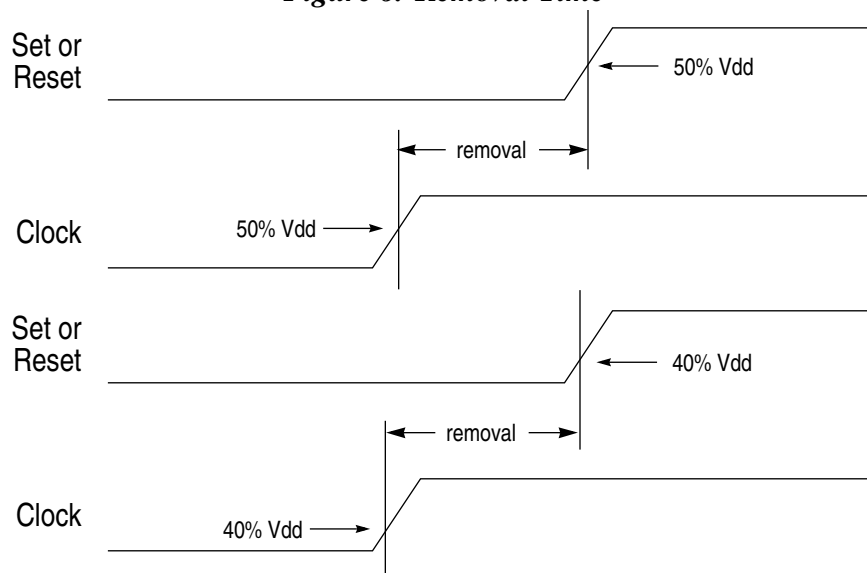
Minimum Pulse Width

Minimum pulse width is the minimum length of time between the leading and trailing edges of a pulse waveform. Minimum pulse width high (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of Vdd and the falling edge of the signal crossing 50% of Vdd. Minimum pulse width low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of Vdd and the rising edge of the signal crossing 50% of Vdd. Figure 7 illustrates minimum pulse width.

Figure 7. Minimum Pulse Width
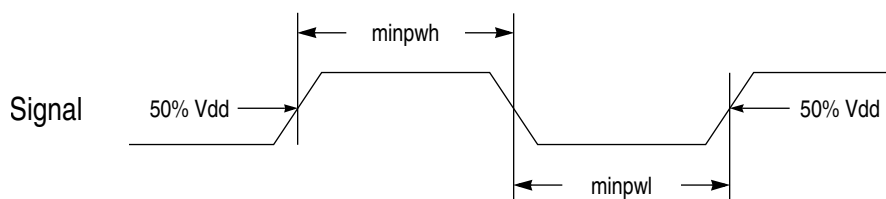
Minimum pulse width is defined as 0.83325ns for all set/reset pins (SN, RN) and 0.83325ns for all clock pins (G, GN, CK, CKN). These are the largest minimum pulse widths measured from all the cells in the library. An input pulse of shorter duration will produce unpredictable results.

Electromigration

min_period Property
All sequential cells in the .lib file have this clock pin property set:

min_period : 1.000000;

This property has the effect of limiting a design's clock frequency to 1.0GHz. Commonly used design flows may not be able to support the required accuracy for designs targeted for clock frequencies higher than this limit. Contact ARM technical support for designs targeting higher clock frequencies.

Electromigration Guideline Compliance
Artisan standard cell libraries are designed to meet foundry electromigration guidelines for normal chip design usage; however, it is the chip designer's responsibility to ensure that electromigration guidelines are met at the chip level with regard to foundry guidelines as well as ARM's guidelines for how the library will be used. The following three Electromigration guidelines must be met in order to ensure safe use of the standard cell library within the electromigration guidelines of the foundry.

1. The width of the Metal1 VDD and VSS power buses in the standard cells has been sized to provide adequate current to the cells. Vertical power straps must be placed with sufficient frequency to provide adequate current distribution to the standard cell power buses. For more details, see the section entitled Power-Rail Strapping in the standard cell user guide.

2. The output pin metal for each standard cell has been sized to accommodate multiple vias necessary (for worst case electromigration conditions) to meet via electromigration guidelines, although oversized Metal1 output pins do not necessarily require multiple vias. The number of vias required to meet electromigration guidelines is design dependent, and the chip designer must use an appropriate number of vias and wire width when routing from an output pin.

3. The internal layouts of the standard cells have been designed and verified to comply with the manufacturer's electromigration guidelines under normal usage. Normal usage is defined as follows:

• The current required by the cell does not exceed the maximum current that can be supplied by the Metal1 power buses.

- The output transition times (measured using 10% and 90% thresholds), for a cell outside the clock tree network, must be no greater than 20% of the total cycle time, or must be no greater than 10% of the cycle time for any of the output pins of that particular cell. Limiting the output transition time has the effect of limiting the load driven by the cell which will reduce the cell's current draw, making it comply with electromigration guidelines. Ratios larger than 20% are not appropriate for commonly used design flows and are unlikely to be encountered in normal designs.

- For a cell in the clock tree network, transition times must not exceed 10% of the total cycle time for that cell.

Power Dissipation

The Advantage library is designed to dissipate only AC power, except for the small reverse-bias leakage currents which are normally present in all CMOS circuits.

The power dissipation internal to a cell when a given input switches is primarily dependent upon the cell design itself. The power dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The Advantage library datasheets contain both an AC power table which documents the internal energy consumption of each cell and a pin capacitance table which gives input-pin capacitance data used to compute output loading. This information, coupled with design-specific information, can be used to estimate the total power dissipation of a cell within a design.

The AC power tables specify the amount of energy consumed within a cell (uW/MHz) when the corresponding pin changes state at 25°C, 1.0V, and typical process. The energy data in the tables were measured for an input slew of 0.018ns and no loading at the outputs.

For combinatorial cells, energy values are provided for only input pins. The energy value for each input pin is the average of energies associated with the input transitions which result in an output transition.

For sequential cells, the energy associated with each input pin is the average energy of those input transitions which *do not* result in an output transition. The energy associated with the output pin of a sequential cell is the average energy of all cases where an output transition is the result of a clock-input transition, minus the energy associated with the clock input pin. In the event that a sequential cell has multiple outputs, all output energy data will be associated with only one output pin.

Power Calculation

Power dissipation is dependent upon the power-supply voltage, frequency of operation, internal capacitance, and output load. The power dissipated by each cell is:

$$P_{avg} = \sum_{n=1}^{x}(E_{in} * f_{in}) + \sum_{n=1}^{y}(C_{on} * Vdd^2 * \frac{1}{2}f_{on}) + E_{os} * f_{01}$$

where:

P_{avg} = average power (uW);

x = number of input pins;

E_{in} = energy associated with the nth input pin (uW/MHz);

f_{in} = frequency at which the nth input pin changes state during the normal operation of the design (MHz);

y = number of output pins;

C_{on} = external capacitive loading on the nth output pin, including the capacitance of each input pin connected to the output driver, plus the route wire capacitance, actual or estimated (pF);

Vdd = operating voltage = 1.0V;

f_{on} = frequency at which the nth output pin changes state during the normal operation of the design (MHz);

E_{os} = energy associated with the output pin for sequential cells only (uW/MHz).

The switching frequency of inputs and outputs of a particular cell in a design can be obtained from a gate-level logic simulator (e.g. Verilog) by applying typical input stimuli and measuring the activity on each node of interest. The total average power for the design can be computed by adding the average power for each cell.

EXAMPLE: Calculating Power for a DFFXL Cell

For this exercise, assume that a DFFXL cell has clock switching at 133MHz (clock frequency = 66.5MHz), input and output pins switching at 20MHz, and an external capacitive loading on the output pin of 0.02pF. Using the AC Power table provided in the **sample** DFF datasheet at the end of the introduction, the power dissipated by the DFFXL can be calculated by using the following equation:

$$P_{avg} = \sum_{n=1}^{x}(E_{in} * f_{in}) + \sum_{n=1}^{y}(C_{on} * Vdd^2 * \frac{1}{2}f_{on}) + E_{os} * f_{01}$$

Given:

$x = 2$;

$E_{i1} = 0.0056$ <uW/MHz;

$E_{i2} = 0.0063$ uW/MHz;

$f_{i1} = 20$ MHz;

$f_{i2} = 133$ MHz;

$y = 2$;

$C_{o1} = 0.02$ pF;

$C_{o2} = 0.02$ pF;

$Vdd = 1.0$V;

$f_{o1} = 20$ MHz;

$f_{o2} = 20$ MHz;

$E_{os} = 0.0060$ uW/MHz,

we have:

$$P_{avg} = \sum_{n=1}^{2}(E_{in} * f_{in}) + \sum_{n=1}^{2}(C_{on} * Vdd^2 * \frac{1}{2}f_{on}) + E_{os} * f_{01}$$

$$P_{avg} = (E_{i1} * f_{i1}) + (E_{i2} * f_{i2}) + (C_{o1} * VDD^2 * \frac{1}{2}f_{o1})$$
$$+ (C_{o2} * VDD^2 * \frac{1}{2}f_{o2}) + (E_{os} * f_{01})$$

$$P_{avg} = (0.0056 * 20) + (0.0063 * 133) + \left(0.02 * 1.0 * \frac{1}{2}(20)\right)$$

$$+ \left(0.02 * 1.0 * \frac{1}{2}(20)\right) + (0.0060 * 20)$$

$$P_{avg} = 1.46 \text{ uW}$$

Power-Rail Strapping

You must determine the required amount of vertical power-rail strapping to satisfy all requirements imposed by the design methodology for a given design. Power-rail strapping should be sized small enough to optimize standard cell height and maximize router efficiency, yet it must be large enough to provide sufficient power to the cells.

The guidelines below provide a rough estimate with many simplifying assumptions. For a given module design, you can estimate the amount of vertical power-rail strapping that is required to fulfill electromigration requirements.

Given:

I_{avg} = total average current for the module, calculated from previous section (mA);

w_{m1} = VSS/VDD metal1 wire width (um), see Physical Specifications;

r = number of rows in module;

d_{m1} = maximum metal1 current density allowed for the process (mA/um);

d_{m2} = maximum metal2 current density allowed for the process (mA/um);

I_{m1} = maximum current that can be supported by all horizontal metal1 wires (mA);

I_{strap} = total current that must be supported by the vertical metal2 strapping (mA);

w_{m2} = metal2 wire width required for vertical strapping (um);

c = minimum number of metal2 straps;

we have:

$$I_{m1} = w_{m1} * r * 2 * d_{m1},$$

where multiplying by 2 assumes metal1 wires are supplied from both ends;

$$I_{strap} = \frac{(I_{avg} - I_{m1})}{2},$$

where dividing by 2 assumes the metal2 vertical strap wires are supplied from both ends;

$$w_{m2} = \frac{I_{strap}}{d_{m2}},$$

It is recommended that the metal2 wire width, w_{m2}, be divided into c equal portions which are spaced equidistant across the module, where

$$c = \frac{I_{avg}}{I_{m1}}, \text{ rounded up to the next integer.}$$

The same consideration must be given to the number of vias used to connect the metal1 and metal2 straps.

Adding Routing Channels

In the Advantage library, each cell is designed with a uniform cell height of 2.52um (i.e., 9 tracks tall with 0.28um per track). The cell layouts allow neighboring rows of cells to share common power or ground rails when cells abut each other at the top and bottom edges of the cell bounding box. The sea-of-cells layout with no channels between rows will usually yield the minimum area. In case of extremely congested areas, you may want to separate some rows of cells to increase the number of routing channels within a particular layout region. Because geometries must overlap cell boundaries, a particular spacing between the rows may result in DRC violations for layer spacing. It is recommended that you do not use spacings that cause DRC violations. If these spacings must be used, the DRC violations must be fixed manually by filling the void between the rows with the appropriate layer(s).

Table 4 indicates which DRC violations to expect and how to correct them for a separation between rows of cells.

Table 4. Correcting DRC Violations

Row Separation in Number of Grids	Expected DRC Violations	Action to Correct DRC Violations
0 (Rows Abut)	None	None
1	NP/PP space < 0.24um	Draw NP/PP layer between rows to merge implant regions above and below row separation
2	NWELL space < 0.62 depending on the well bias up to 1.2um M1 space < 0.12 depending on the width of Metal up to 1.5um	Draw NWELL layer between rows to merge NWELL regions above and below row separation Draw Metal1 layer between rows to merge Metal1 regions above and below row separation
3	NWELL space < 0.62 depending on the well bias up to 1.2um	Draw NWELL layer between rows to merge NWELL regions above and below row separation
4	None	None
5 or more	None	None

Special Cells

This section discusses special cells in the Advantage library.

Antenna-Fix Cell

The library contains an antenna-fix cell which must be inserted manually. However, most place and route tools will indicate which nets require the antenna-fix cell. The TSMC antenna effect prevention guideline, "TSMC 90nm CMOS Logic Design Rule", specifies a maximum wire length. During place and route, the router may connect wires to the input gates of cells that are longer than the maximum length allowable by the guideline. The antenna cell can be used in this case to add an optional diode on the net close to the input gates which do not meet the guideline. Pin A on the antenna cell connects to a diode, reverse biased to ground. A diode can be added to either P or N.

Delay Cells

The library contains delay cells that have the same width. These delay cells allow you to adjust a given delay path with a simple cell substitution after place and route.

FILL Cells

The library contains several FILL cells: FILL1, FILL2, FILL4, FILL8, FILL16, FILL32, FILL64. The number appended to FILL in the cell name denotes the width of the cell in tracks.

During place and route, the FILL cells are used to connect power and ground rails across an area containing no cells. The FILL cells are also used to ensure gaps do not occur between well or implant layers which could cause design rule violations. Using wider cells where appropriate reduces the size of the layout database.

FILLCAP Cells

FILLCAPs function as FILL cells. Inside the FILLCAP, PMOS and NMOS devices form decoupling capacitors between the VDD and VSS rails, reducing ground bounce in the power grids. Figure 8 illustrates the FILLCAP functional schematic.

Figure 8. FILLCAP Functional Schematic
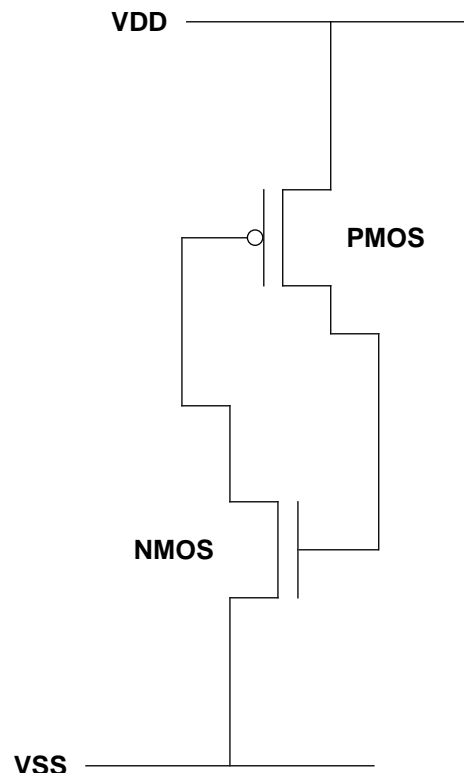
Low-Power (XL) Cells

The library contains a wide variety of cells, denoted by an "XL" suffix in the cell name, that are designed specifically for low-power applications. Input capacitance for the XL cells is much lower than that for corresponding X1 (1x drive strength) cells. Because XL cells have been designed for the sole purpose of reducing power consumption, output rise and fall times for these cells may not be equal, and due to the low-drive capability of the XL cells, these cells are not intended for use in critical timing paths, or to drive heavily loaded nets.

NWELL and Substrate Tie Cell

The library does not have well or substrate ties inside the cells. You are required to tie the NWELLS to Vdd and the substrate to Vss before place-and-route using the FILLTIE cell. Before place-and-route, pre-place the FILLTIE cell periodically in every placement row. You must place the FILLTIE cell as frequently as the design requires.

For example, if the design rules require a well or substrate connection every 20um, then the FILLTIE cell must be pre-placed every 20um. See Figure 9.

Figure 9. Sample Placement of FILLTIE Cells for 20um NWELL and Substrate Tie Design Rule
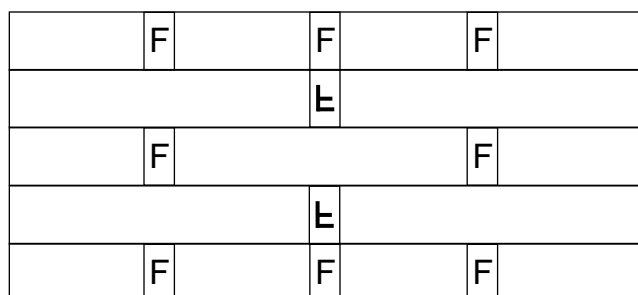
Note: The letter "F" indicates a FILLTIE cell placed in normal orientation, and the letter "F" flipped upside down indicates a FILLTIE cell placed in MY orientation.

In all rows except for the top and bottom rows, the NWELL and substrate are shared by two adjacent placement rows. This allows you to place the FILLTIE cell only half as frequently as the design rules require. But don't forget to stagger the placement in the adjacent rows by an amount equal to the design row.

Assuming that the rule is every 20um, you will need to place FILLTIE cells every 20um in the top and bottom rows. If you stagger the placement by 20um between adjacent rows, you can place FILLTIE cells every 40um for all rows between the top and bottom rows. This method will allow every row to have well and substrate ties every 20um.

Register File Cells

Register file cells (RF*) are provided to support creating very small memories from standard cells. The register file bit cells (RF1R1W, RF2R1W) have tri-state outputs. Users must tie these tri-state outputs together on a bit line and have this bit line drive function as an output buffer. The library contains a number of inverting and non-inverting buffers (INV*, BUF*, TRI*) that can buffer the bit lines.

It is possible to make a memory that has a non-power-of-two word depth. If this is employed, it is possible to input an address to the memory such that none of the bit cells are addressed and nothing is driving the bit line. A floating bit line can cause the logic following it to go into a high power state, therefore, users must take special care when designing a memory with a non-power-of-two word depth. Users must guarantee that the bit line is never allowed to float by ensuring that at least one bit cell is always driving the bit line, or that a floating bit line does not cause subsequent logic to go into a high power state. One way to achieve the latter is to use an output buffer with an enable. NAND or AND gates or tri-state output buffers (NAND*, AND*, TRI*) can be used for this purpose. Whichever is used, be sure to generate an enable signal that only enables the output buffer when the bit line is not floating.

Figure 10 shows a sample circuit for generating an enable signal when the bit line is not floating in a register file of up to 64 words.

Figure 10. Enable Signal Circuit Example
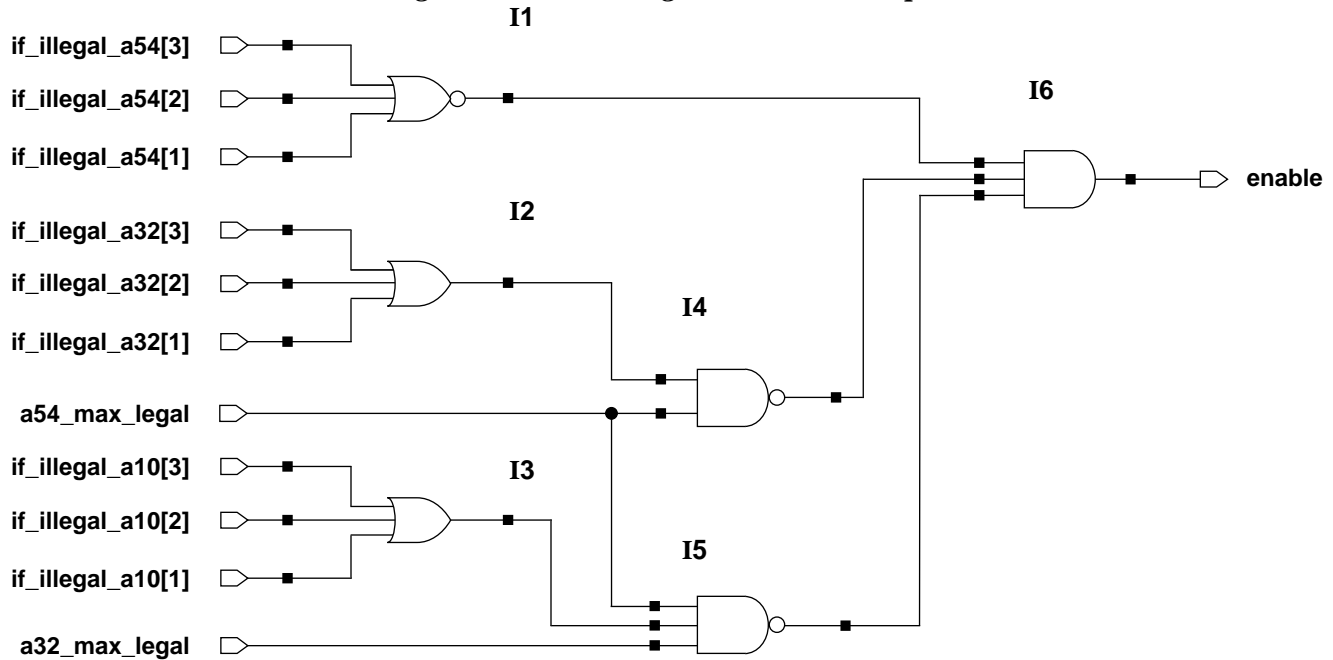
The circuit in Figure 10 assumes the address lines are pre-decoded in pairs. The circuit is a comparator. Program it with the number of words in the memory. The circuit compares the address input of the memory to the pre-programmed number of words. When the address is less than or equal to the size of the memory, it generates an enable signal for the output buffers. When the address input is higher than the number of words in the memory, the output of the comparator is false and the outputs are disabled, which prevents them from going into a high power state.

To program the example comparator, connect predecoded address lines to gates I1, I2 and I3 if the address should be larger than the size of the memory when those signals are active, and more significant address bits have not resolved the comparison. If, when those signals are active, the address should not be larger than the size of the memory, either ground that pin or reduce the number of inputs to the gate. To enable the comparison of lower address bits, connect to gates I4 and I5 signals that signify that the higher address bits have not been able to resolve the comparison. To I4, connect the signal that is true when the most significant two address bits are exactly equal to what they are in the highest address that exists in the memory. To I5, connect the signals that are true when the most significant for bits are exactly equal to what they are in the highest address that exists in the memory.

Figure 11 shows an example for a memory that has 21 words.

Figure 11. 21-Word Memory Example
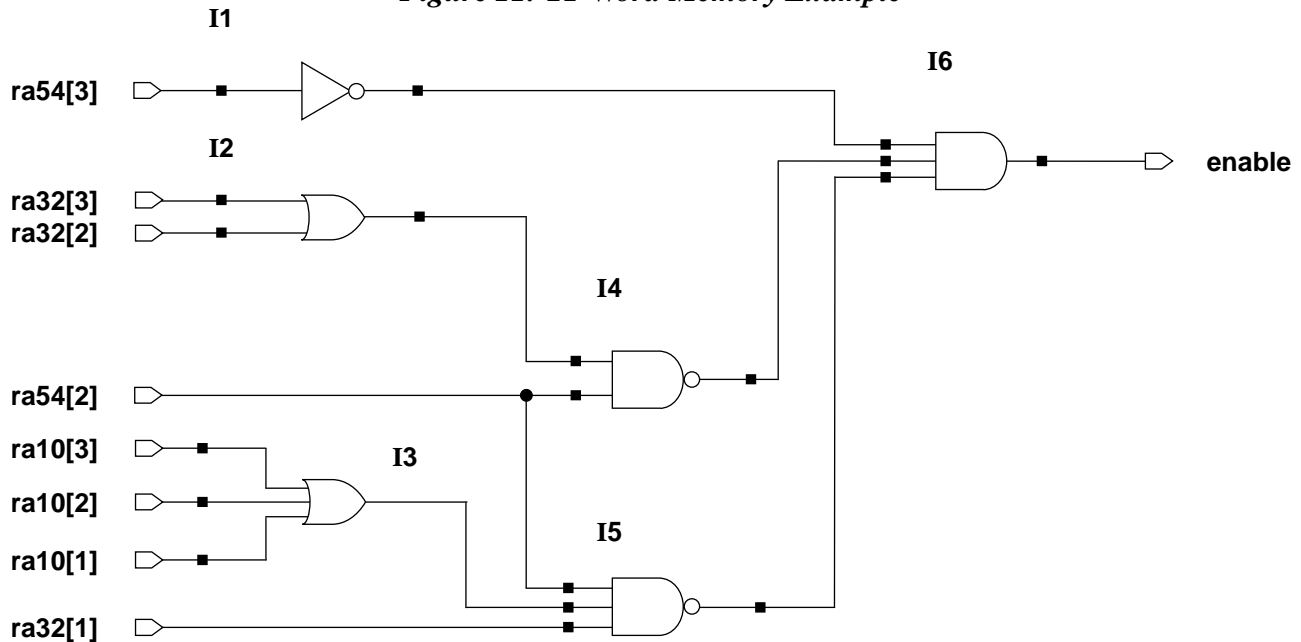
In binary mode, the highest address that exists in the memory is 100100. The read address RA[5:0] is pre-decoded into RA54[3:0] which are the four possible combinations of the two most significant address bits. RA32[3:0] is the four possible combinations of address bits 3 and 2. RA10[3:0] is the four possible combinations of address bits 1 and 0. If RA54[3] is true, we are accessing address 11XXXX in the memory. This address does not exist, so the comparison does not need to continue to the remaining address bits. Gate I1 needs only RA54[3] as an input because this is the only combination of these 2 address bits which is never in the memory. We connect RA54[2] to gate I4 because if this signal is true we don't know if the address exists and we have to continue the comparison to the next pair of addresses. To gate I2 we connect RA32[3] and RA32[2] because if RA54[2] is true and either of RA32[3] or RA32[2] are true, the address doesn't exist and we are done. If RA54[2] and RA32[1] are true, we are addressing word 1001XX which might be in the memory so we connect these two signals to I5 and check RA10. We connect RA10[3], RA10[2] and RA10[1] to I3 because of the memory addresses 1001XX, only 100100 exists in the memory. I6 generates the enable signal based on the results of all of the comparisons.

TIEHI/LO Cells

The library contains a TIEHI cell and a TIELO cell. The outputs of the TIEHI and TIELO cells are driven through diffusion to provide isolation from the power and ground rails for better ESD protection. The standard cell abstract methodology assumes that the TIEHI and TIELO cells are used to tie off any inputs to power and ground. If these cells are not used and the router is allowed to drop vias on the power rail, DRC errors or shorts may result.

Advantage Naming Convention

Reading the Datasheet

Please refer to the **sample** datasheet for DFF at the end of the introduction for the arrangement of each of the following datasheet sections. Datasheet titles reference standard Artisan cell names. Cell names for your specific library are reflected in the cell size table on each datasheet.

NOTE: This datasheet contains **sample** characterization values.

1. Base Cell Name

The cell name field contains the cell name. The datasheets are presented alphabetically by cell name. The cell name presented here is the base cell name. The Cell Size table displays cell names for your specific library.

2. Cell Description

The cell description gives the function of the cell. When applicable, the equation(s) for the output pins are provided.

3. Functions

The function table gives all possible combinations of input and output signals for the cell. Table 5 defines the symbols used in datasheet function tables.

Table 5. Functions Key

Symbol	Description
0	Logic Low
1	Logic High
⌐_	High to Low Transition
_⌐	Low to High Transition
X	Don't Care
IL	Illegal/Undefined
Z	High Impedance

4. Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

5. Cell Size

This cell size table gives the height and width (μm) for each drive strength of the cell.

6. Functional Schematic

The functional schematic provides a functional representation of the cell.

7. Drive Strength

The drive strength of each cell is indicated by an "X" followed by the unit strength.

8. AC Power

The AC power table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state. The energy data for each drive strength of the cell in the **sample** DFF datasheet are calculated at 25°C, 1.0V, typical process, input slew of 0.018ns, and no external load at the output pins.

9. Delay

The delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF). The delays and load multiplier for each drive strength of the cell in the sample DFF datasheet are calculated at 25°C, 1.0V, typical process, and input slew of 0.018ns.

10. Timing Constraints

The timing constraints table in the **sample** DFF datasheet shows the timing conditions (ns) required at 25°C, 1.0V, and typical process to maintain proper functionality. Setup constraint values are measured for 0.018ns data slew and 0.018ns clock slew. Hold constraint values are measured for 0.018ns data slew and 0.018ns clock slew. Minimum pulse width is defined to be 0.83325ns for all set/reset pins and 0.83325ns for all clock pins. These are the largest minimum pulse widths measured from all the cells in the library.

11. Pin Capacitance

The pin capacitance table shows the typical loading at the input pins of the cell (pF) for each drive strength of the cell.

▼ *This datasheet contains sample characterization values.* ▼

Process Technology:
CustomerName & Code

(1)

DFF

Cell Description

The DFF cell is a positive-edge triggered, static D-type flip-flop.

(2)

Logic Symbol

(4)

D — Q
CK — QN

Function Table

(3)

D	CK	Q[n+1]	QN[n+1]
0	⌐	0	1
1	⌐	1	0
x	⌐	Q[n]	QN[n]

Cell Size

(5)
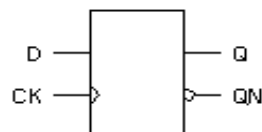
Drive Strength	Height (μm)	Width (μm)
DFFXL	1.000	1.000
DFFX1	2.000	2.000
DFFX2	3.000	3.000
DFFX4	4.000	4.000
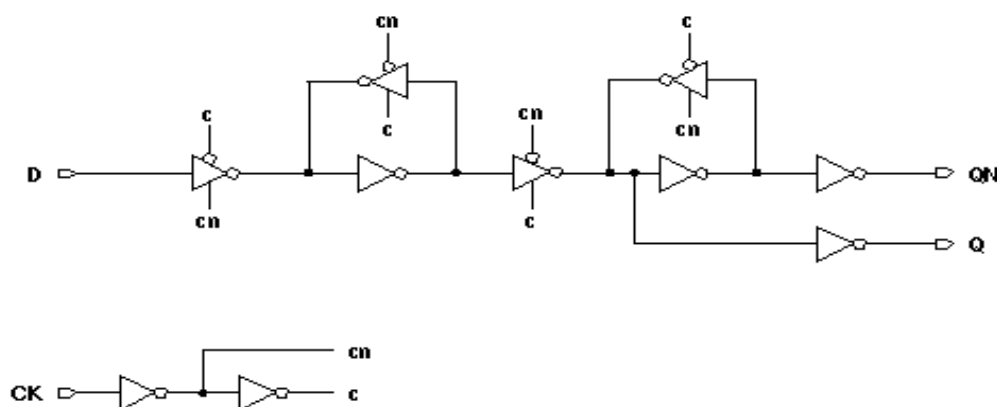
(7)

(6)

Functional Schematic

D — QN
Q
CK

▼ *This datasheet contains sample characterization values.* ▼

Process Technology:
CustomerName & Code

DFF

⑧

AC Power

⑦

Pin	Power (μW/MHz)			
	XL	X1	X2	X4
D	1.000	1.000	1.000	1.000
CK	2.000	2.000	2.000	2.000
Q	3.000	3.000	3.000	3.000

⑪

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	1.000	1.000	1.000	1.000
CK	2.000	2.000	2.000	2.000

Delays at TypTemp°C, TypVoltV, Typical Process

⑨

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	1.000	1.000	1.000	1.000	1.000	1.000	1.000	1.000
CK → Q↓	2.000	2.000	2.000	2.000	2.000	2.000	2.000	2.000
CK → QN↑	3.000	3.000	3.000	3.000	3.000	3.000	3.000	3.000
CK → QN↓	4.000	4.000	4.000	4.000	4.000	4.000	4.000	4.000

Timing Constraints at TypTemp°C, TypVoltV, Typical Process

⑩

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	1.000	1.000	1.000	1.000
	setup↓ → CK	2.000	2.000	2.000	2.000
	hold↑ → CK	3.000	3.000	3.000	3.000
	hold↓ → CK	4.000	4.000	4.000	4.000
CK	minpwh	5.000	5.000	5.000	5.000
	minpwh	6.000	6.000	6.000	6.000

Cell Description

The ACCSHCIN cell provides a carry-select addercarry generation function with active-low carry inputs. The function produces the carryouts (CO0,CO1) of the operands (A,B) with active-low carry-ins (CI0N,CI1N).The outputs (CO0,CO1) are represented by the logic equations:

$$CO0 = (A{\bullet}B) + (A{\bullet}\overline{CI0N}) + (B{\bullet}CI0N)$$

$$CO1 = (A{\bullet}B) + (A{\bullet}\overline{CI1N}) + (B{\bullet}\overline{CI1N})$$

Logic Symbol
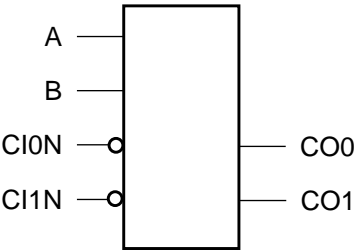
Function Table

A	B	CI0N	CI1N	CO0	CO1
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	1	1
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	0
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
ACCSHCINX2AD	2.52	9.52
ACCSHCINX4AD	2.52	9.52

Functional Schematic
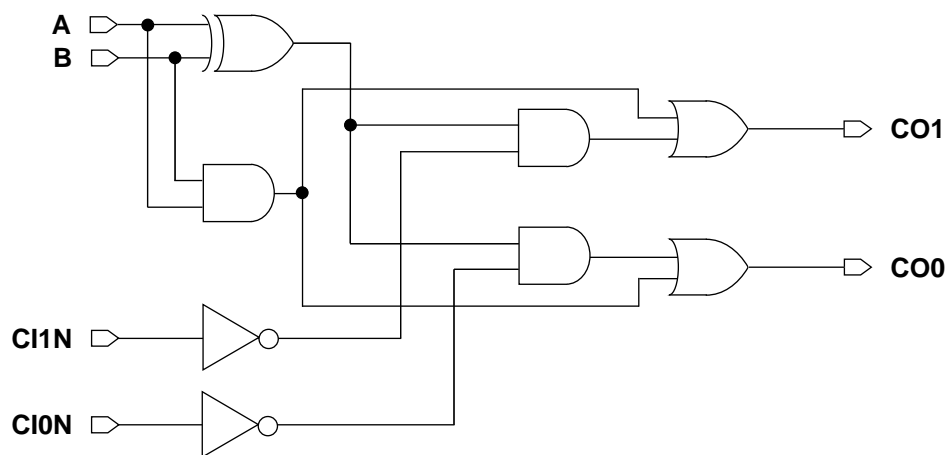
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
A	0.0256	0.0248
B	0.0211	0.0204
CI0N	0.0057	0.0055
CI1N	0.0069	0.0067

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
A	0.0026	0.0026
B	0.0061	0.0059
CI0N	0.0025	0.0026
CI1N	0.0026	0.0026

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
A	→	CO0	↑	0.0869	0.0911	3.6849	3.6437
A	→	CO0	↓	0.1058	0.1079	2.3553	2.3232
B	→	CO0	↑	0.0670	0.0675	3.5463	3.6034
B	→	CO0	↓	0.0734	0.0752	2.3148	2.3149
CI0N	→	CO0	↑	0.0258	0.0254	3.5162	3.5768
CI0N	→	CO0	↓	0.0176	0.0176	2.1170	2.1564
A	→	CO1	↑	0.0959	0.0983	3.5792	3.5777
A	→	CO1	↓	0.1114	0.1130	2.2461	2.2324
B	→	CO1	↑	0.0567	0.0597	3.5308	3.5604
B	→	CO1	↓	0.0704	0.0731	2.2281	2.2283
CI1N	→	CO1	↑	0.0312	0.0307	3.4730	3.5480
CI1N	→	CO1	↓	0.0214	0.0213	2.1531	2.1969

Cell Description

The ACCSHCON cell provides a carry-select addercarry generation function that produces active-low carryouts (CO0N,CO1N) of the operands (A,B) with carry-ins (CI0,CI1).The outputs (CO0N,CO1N) are represented by the logic equations:

$$CO0N = \overline{(A \bullet B) + (A \bullet CI0) + (B \bullet CI0)}$$

$$CO1N = \overline{(A \bullet B) + (A \bullet CI1) + (B \bullet CI1)}$$

Logic Symbol
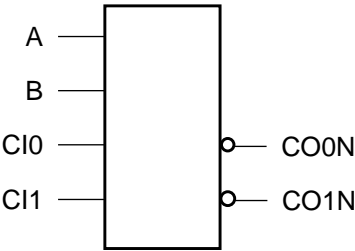
Function Table

A	B	CI0	CI1	CO0N	CO1N
0	0	0	0	1	1
0	0	0	1	1	1
0	0	1	0	1	1
0	0	1	1	1	1
0	1	0	0	1	1
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	0
1	1	0	0	0	0
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
ACCSHCONX2AD	2.52	8.68
ACCSHCONX4AD	2.52	10.36

Functional Schematic
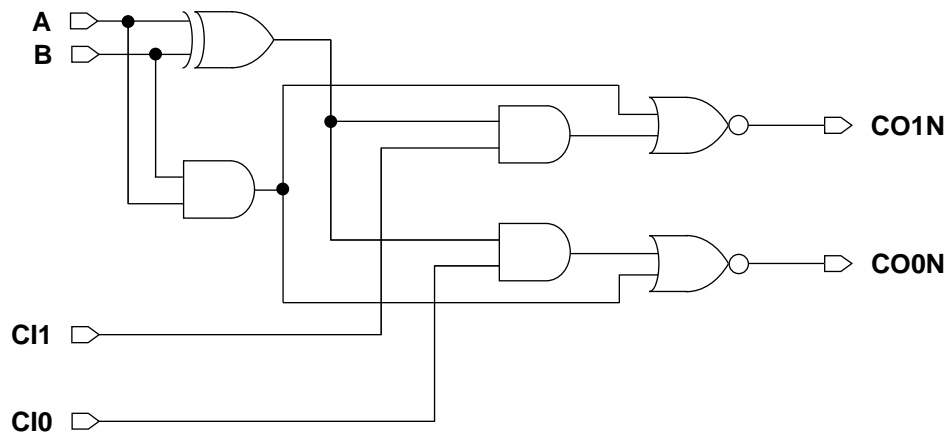
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
A	0.0238	0.0279
B	0.0225	0.0263
CI0	0.0060	0.0103
CI1	0.0070	0.0110

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
A	0.0054	0.0055
B	0.0079	0.0078
CI0	0.0028	0.0054
CI1	0.0028	0.0054

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
A	→	CO0N	↑	0.1041	0.1240	3.0770	3.0841
A	→	CO0N	↓	0.1013	0.1253	2.1918	2.0847
B	→	CO0N	↑	0.0817	0.1025	3.1345	3.0876
B	→	CO0N	↓	0.0808	0.1040	2.1952	2.0875
CI0	→	CO0N	↑	0.0255	0.0232	3.1922	1.5971
CI0	→	CO0N	↓	0.0172	0.0162	1.9279	0.9879
A	→	CO1N	↑	0.1049	0.1238	3.0777	3.0331
A	→	CO1N	↓	0.1010	0.1231	2.0916	2.0199
B	→	CO1N	↑	0.0835	0.1023	3.0501	3.0325
B	→	CO1N	↓	0.0798	0.1014	2.0915	2.0181
CI1	→	CO1N	↑	0.0309	0.0251	3.2016	1.6498
CI1	→	CO1N	↓	0.0210	0.0173	2.0071	1.0335

Cell Description

The ACCSIHCON cell provides a carry-select addercarry generation function for the first stage of a carry-select adder block (i.e., there are no carry-inputs). The function produces active-low carryouts (CO0N,CO1N) of the operands (A,B).The outputs (CO0N,CO1N) are represented by the logic equations:

$$CO0N = \overline{A \bullet B}$$

$$CO1N = \overline{A + B}$$

Logic Symbol
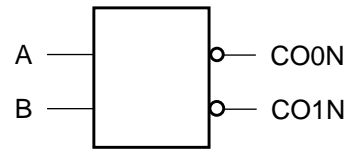
Function Table

A	B	CO0N	CO1N
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
ACCSIHCONX2AD	2.52	1.96
ACCSIHCONX4AD	2.52	3.36

Functional Schematic
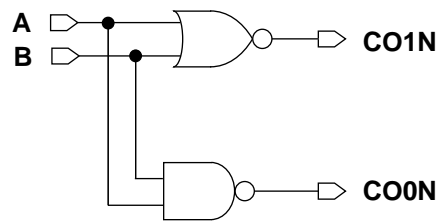
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
A	0.0046	0.0091
B	0.0055	0.0109

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
A	0.0044	0.0088
B	0.0051	0.0098

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)		K_{load} (ns/pF)	
			X2	**X4**	**X2**	**X4**
A	→	CO0N ↑	0.0161	0.0159	2.4300	1.2174
A	→	CO0N ↓	0.0136	0.0134	2.1881	1.0745
B	→	CO0N ↑	0.0135	0.0130	2.3673	1.2430
B	→	CO0N ↓	0.0126	0.0116	2.1891	1.0734
A	→	CO1N ↑	0.0201	0.0193	4.6923	2.4020
A	→	CO1N ↓	0.0092	0.0087	1.2520	0.6188
B	→	CO1N ↑	0.0240	0.0247	4.6856	2.4016
B	→	CO1N ↓	0.0100	0.0101	1.2338	0.6178

Cell Description

The ACHCIN cell is a full adder carry-generator that provides the arithmetic carryout (CO) of two operands (A,B) with active low carry-in (CIN). The output (CO) is represented by the logic equation:

$$CO = (A \bullet B) + (A \bullet \overline{CIN}) + (B \bullet \overline{CIN})$$

Logic Symbol
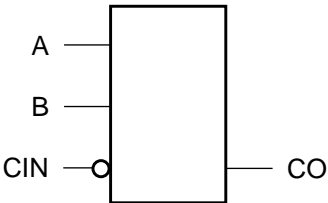
Function Table

A	B	CIN	CO
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
ACHCINX2AD	2.52	5.88
ACHCINX4AD	2.52	7.28

Functional Schematic
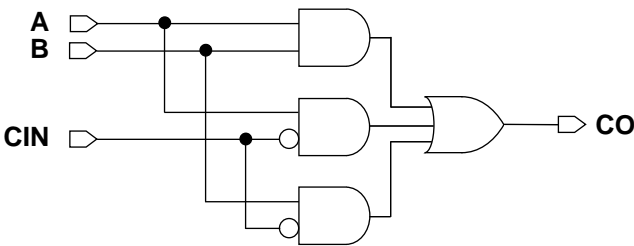
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
A	0.0165	0.0207
B	0.0180	0.0212
CIN	0.0062	0.0101

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
A	0.0028	0.0028
B	0.0062	0.0068
CIN	0.0028	0.0054

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
A	$\rightarrow$	CO	↑	0.0710	0.0828	3.2741	3.2066
A	$\rightarrow$	CO	↓	0.0780	0.0933	2.0211	1.9436
B	$\rightarrow$	CO	↑	0.0577	0.0653	3.1672	3.1676
B	$\rightarrow$	CO	↓	0.0655	0.0721	1.9716	1.9347
CIN	$\rightarrow$	CO	↑	0.0264	0.0222	3.0539	1.5608
CIN	$\rightarrow$	CO	↓	0.0193	0.0168	1.9508	0.9932

Cell Description

The ACHCON cell is a full adder carry-generator that provides the arithmetic activelow carry-out (CON) of two operands (A,B) with carryin (CI). The output (CON) is represented by the logic equation:

$$CON = \overline{(A \bullet B) + (A \bullet CI) + (B \bullet CI)}$$

Logic Symbol

A

B
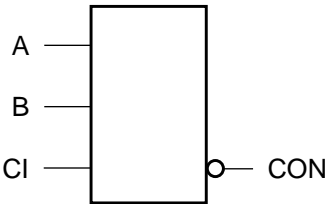
CI — CON

Function Table

A	B	CI	CON
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
ACHCONX2AD	2.52	5.88
ACHCONX4AD	2.52	7.28

Functional Schematic

A
B

CI

CON
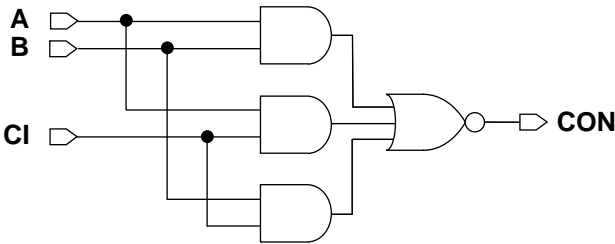
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
A	0.0183	0.0225
B	0.0178	0.0206
CI	0.0060	0.0099

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
A	0.0028	0.0028
B	0.0085	0.0087
CI	0.0028	0.0054

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
A	→	CON	↑	0.0922	0.1016	2.9962	3.0961
A	→	CON	↓	0.0880	0.0961	1.9193	1.8771
B	→	CON	↑	0.0607	0.0651	3.0827	3.1401
B	→	CON	↓	0.0525	0.0602	1.9582	1.9104
CI	→	CON	↑	0.0263	0.0221	3.0541	1.5610
CI	→	CON	↓	0.0193	0.0169	1.9509	0.9938

Cell Description

The ADDF cell provides the arithmetic sum (S) and carry out (CO) of two operands (A,B) with carry in (CI). The two outputs (S,CO) are represented by the logic equations:

$S = (A \oplus B \oplus CI)$

$CO = (A \oplus B) \bullet CI + (A \bullet B)$

Logic Symbol

A —
B —
CI —
— S
— CO
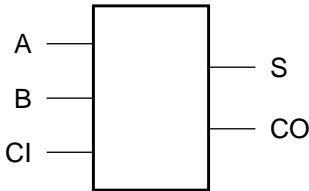
Function Table

CI	A	B	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
ADDFXLAD	2.52	7.00
ADDFX1AD	2.52	7.00
ADDFX2AD	2.52	7.00
ADDFX4AD	2.52	7.84

Functional Schematic
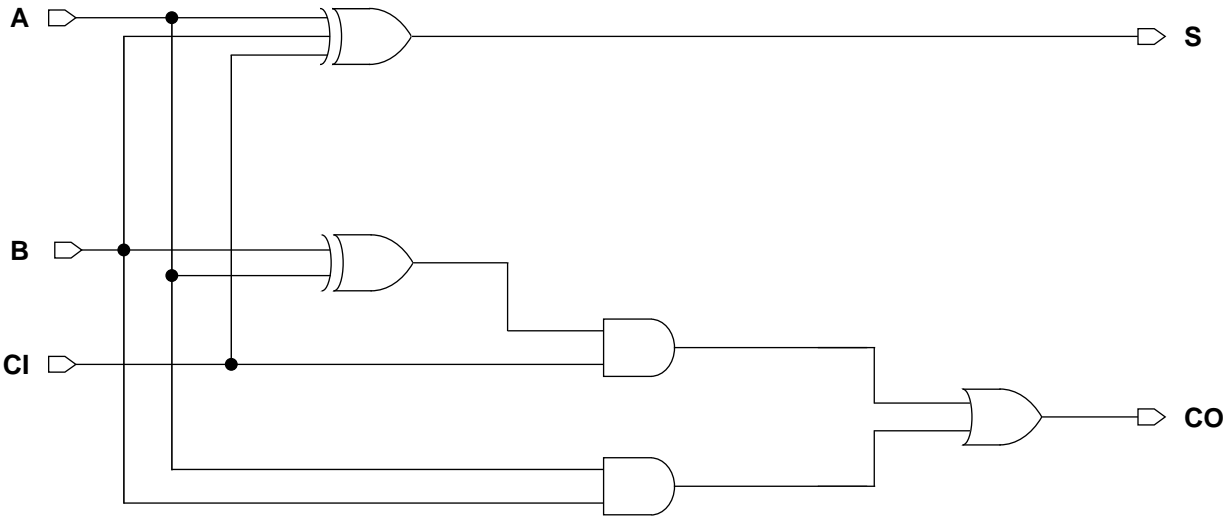
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A	0.0157	0.0167	0.0203	0.0289
B	0.0191	0.0204	0.0254	0.0342
CI	0.0088	0.0099	0.0134	0.0228

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A	0.0026	0.0026	0.0029	0.0029
B	0.0026	0.0026	0.0029	0.0028
CI	0.0028	0.0028	0.0030	0.0030

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A	→	S	↑	0.1087	0.1109	0.1117	0.1303	5.8192	3.9351	2.4221	1.2631
A	→	S	↓	0.1440	0.1508	0.1443	0.1665	5.3573	3.5559	1.6019	0.8551
B	→	S	↑	0.1280	0.1302	0.1295	0.1447	5.8237	3.9358	2.4269	1.2704
B	→	S	↓	0.1617	0.1684	0.1621	0.1835	5.3596	3.5572	1.6024	0.8555
CI	→	S	↑	0.0836	0.0869	0.0896	0.1132	5.7551	3.9072	2.4174	1.2682
CI	→	S	↓	0.0722	0.0785	0.0776	0.0984	5.3400	3.5643	1.6142	0.8737
A	→	CO	↑	0.1370	0.1412	0.1410	0.1664	5.6723	3.6599	2.3796	1.2338
A	→	CO	↓	0.1290	0.1359	0.1335	0.1564	4.8817	3.3301	1.5020	0.8066
B	→	CO	↑	0.1546	0.1588	0.1586	0.1833	5.6726	3.6600	2.3795	1.2338
B	→	CO	↓	0.1482	0.1548	0.1513	0.1731	4.7228	3.2151	1.4218	0.7550
CI	→	CO	↑	0.0702	0.0742	0.0816	0.1046	5.7935	3.7254	2.4216	1.2583
CI	→	CO	↓	0.0851	0.0925	0.0923	0.1132	5.0882	3.4156	1.5334	0.8347

Cell Description

The ADDFH cell is a high-speed cell providing the arithmetic sum (S) and carry out (CO) of two operands (A,B) with carry in (CI). The two outputs (S,CO) are represented by the logic equations:

$S = (A \oplus B \oplus CI)$

$CO = (A \oplus B) \bullet CI + (A \bullet B)$

Logic Symbol
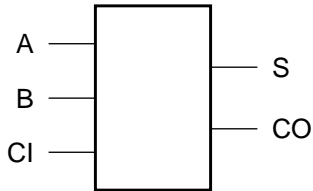
Function Table

CI	A	B	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
ADDFHXLAD	2.52	7.56
ADDFHX1AD	2.52	8.12
ADDFHX2AD	2.52	10.92
ADDFHX4AD	2.52	17.64

Functional Schematic
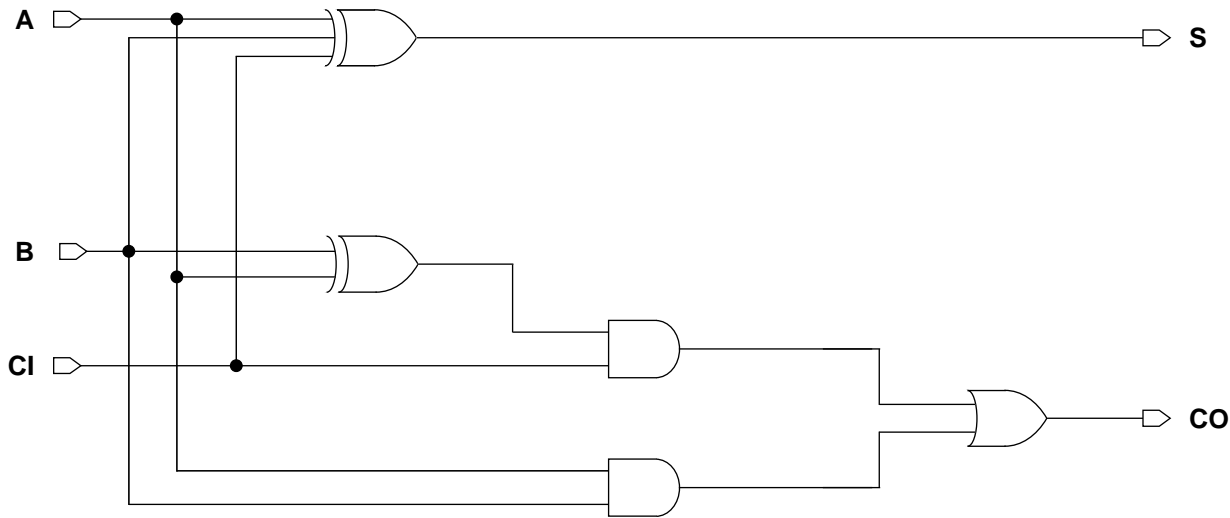
AC Power

Pin	Power (uW/MHz)			
	XL	X1	X2	X4
A	0.0173	0.0213	0.0356	0.0625
B	0.0150	0.0190	0.0301	0.0554
CI	0.0094	0.0114	0.0175	0.0347

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A	0.0026	0.0031	0.0051	0.0096
B	0.0045	0.0062	0.0098	0.0176
CI	0.0017	0.0020	0.0028	0.0053

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	X1	X2	X4	XL	X1	X2	X4
A	→	S	↑	0.1310	0.1124	0.1064	0.0966	5.7388	3.7718	2.3602	1.2133
A	→	S	↓	0.1353	0.1223	0.1145	0.1038	5.0258	3.2274	1.3672	0.6716
B	→	S	↑	0.0991	0.0841	0.0776	0.0781	5.7805	3.7662	2.3656	1.2161
B	→	S	↓	0.1168	0.1001	0.0892	0.0842	5.0320	3.2286	1.3766	0.6754
CI	→	S	↑	0.1061	0.0897	0.0817	0.0825	5.7712	3.7824	2.3663	1.2162
CI	→	S	↓	0.1125	0.0946	0.0813	0.0794	5.0784	3.2452	1.3837	0.6792
A	→	CO	↑	0.1316	0.1127	0.1085	0.0966	5.7199	3.6483	2.4086	1.2205
A	→	CO	↓	0.1361	0.1233	0.1146	0.1049	4.6623	3.1690	1.3926	0.6796
B	→	CO	↑	0.0888	0.0757	0.0702	0.0644	5.7318	3.6538	2.4076	1.2214
B	→	CO	↓	0.1109	0.0973	0.0876	0.0843	4.6668	3.1507	1.3622	0.6665
CI	→	CO	↑	0.0595	0.0506	0.0474	0.0453	5.7679	3.6675	2.4178	1.2245
CI	→	CO	↓	0.0802	0.0733	0.0665	0.0642	5.1100	3.3089	1.4421	0.7078

Cell Description

The ADDH cell provides the arithmetic sum (S) and carry out (CO) of two operands (A,B). The two outputs (S,CO) are represented by the logic equations:

$S = (\overline{A} \bullet B) + (A \bullet \overline{B})$

$CO = A \bullet B$

Logic Symbol
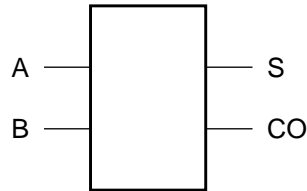
Function Table

A	B	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Cell Size

Drive Strength	Height (um)	Width (um)
ADDHXLAD	2.52	4.20
ADDHX1AD	2.52	4.20
ADDHX2AD	2.52	4.48
ADDHX4AD	2.52	6.44

Functional Schematic
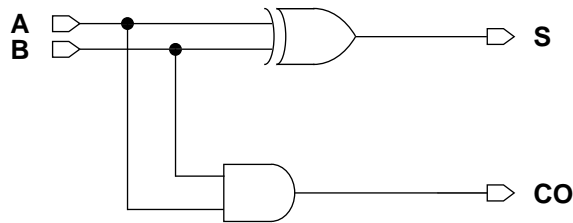
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A	0.0076	0.0097	0.0159	0.0292
B	0.0053	0.0062	0.0092	0.0169

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A	0.0020	0.0029	0.0049	0.0090
B	0.0025	0.0026	0.0030	0.0050

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A	→ S	↑	0.0587	0.0437	0.0397	0.0361	8.2875	5.9218	3.1220	1.6145
A	→ S	↓	0.0693	0.0608	0.0451	0.0401	6.4560	4.7887	2.0006	1.0026
B	→ S	↑	0.0277	0.0257	0.0248	0.0242	8.3511	5.8995	3.1338	1.6168
B	→ S	↓	0.0315	0.0333	0.0358	0.0337	6.1078	4.5966	1.9011	0.9589
A	→ CO	↑	0.0375	0.0426	0.0373	0.0366	5.4699	3.6088	2.3732	1.1819
A	→ CO	↓	0.0501	0.0591	0.0478	0.0448	4.5946	3.1095	1.3138	0.6615
B	→ CO	↑	0.0375	0.0416	0.0367	0.0359	5.4858	3.6102	2.3732	1.1818
B	→ CO	↓	0.0463	0.0538	0.0434	0.0402	4.5853	3.0958	1.3068	0.6567

Cell Description

The AFCSHCIN cell provides a carry-select adder function that produces the arithmetic sum (S) and carryouts (CO0,CO1) of the operands (A,B) with active-low carry-ins (CI0N,CI1N).The three outputs (S,CO0,CO1) are represented by the logic equations:

$$S = CS \bullet (A \oplus B \oplus \overline{CI1N}) + \overline{CS} \bullet (A \oplus B \oplus \overline{CI0N})$$

$$CO0 = (A \bullet B) + (A \bullet \overline{CI0N}) + (B \bullet \overline{CI0N})$$

$$CO1 = (A \bullet B) + (A \bullet \overline{CI1N}) + (B \bullet \overline{CI1N})$$

Logic Symbol
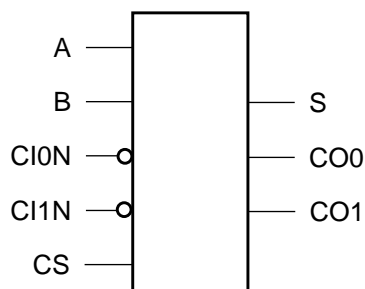
Cell Size

Drive Strength	Height (um)	Width (um)
AFCSHCINX2AD	2.52	15.96
AFCSHCINX4AD	2.52	16.52

Function Table

A	B	CI0N	CI1N	CS	S	CO0	CO1
0	0	0	0	0	1	0	0
0	0	0	0	1	1	0	0
0	0	0	1	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	0	0	0
0	0	1	0	1	1	0	0
0	0	1	1	0	0	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	0	1	1
0	1	0	0	1	0	1	1
0	1	0	1	0	0	1	0
0	1	0	1	1	1	1	0
0	1	1	0	0	1	0	1
0	1	1	0	1	0	0	1
0	1	1	1	0	1	0	0
0	1	1	1	1	1	0	0

Function Table (Cont'd.)

A	B	CI0N	CI1N	CS	S	CO0	CO1
1	0	0	0	0	0	1	1
1	0	0	0	1	0	1	1
1	0	0	1	0	0	1	0
1	0	0	1	1	1	1	0
1	0	1	0	0	1	0	1
1	0	1	0	1	0	0	1
1	0	1	1	0	1	0	0
1	0	1	1	1	1	0	0
1	1	0	0	0	1	1	1
1	1	0	0	1	1	1	1
1	1	0	1	0	1	1	1
1	1	0	1	1	0	1	1
1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	1
1	1	1	1	0	0	1	1
1	1	1	1	1	0	1	1

Functional Schematic
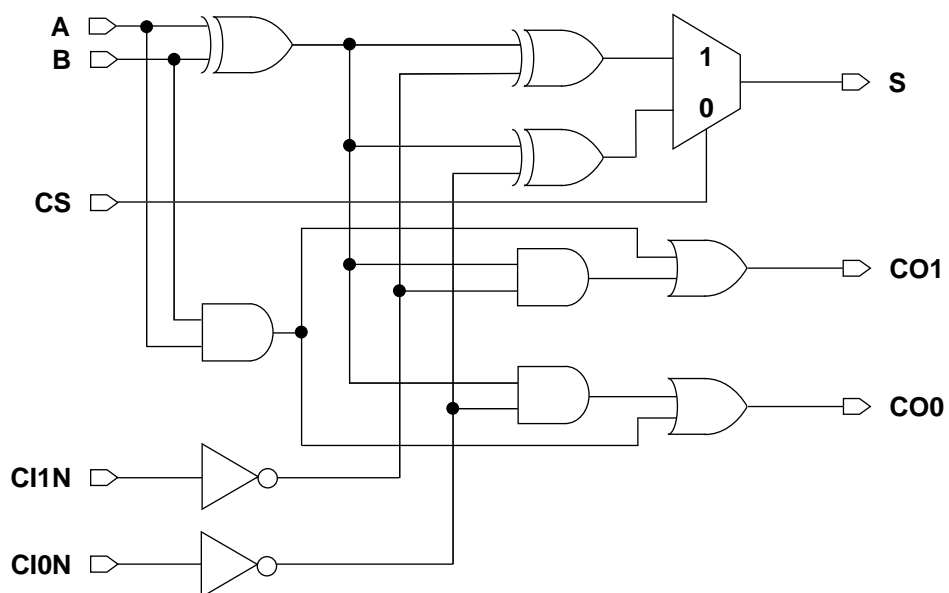
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
CS	0.0102	0.0103
A	0.0427	0.0431
B	0.0383	0.0385
CI0N	0.0202	0.0228
CI1N	0.0210	0.0226

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
CS	0.0019	0.0019
A	0.0029	0.0029
B	0.0061	0.0061
CI0N	0.0048	0.0077
CI1N	0.0052	0.0070

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
CS	→	S	↑	0.0854	0.0859	2.3430	2.3160
CS	→	S	↓	0.0783	0.0818	1.3896	1.3149
A	→	S	↑	0.2243	0.2268	2.3470	2.3171
A	→	S	↓	0.2196	0.2209	1.3981	1.3156
B	→	S	↑	0.1870	0.1888	2.3469	2.3171
B	→	S	↓	0.1874	0.1892	1.3983	1.3157
CI0N	→	S	↑	0.1412	0.1400	2.3471	2.3173
CI0N	→	S	↓	0.1410	0.1364	1.3978	1.3155
CI1N	→	S	↑	0.1179	0.1190	2.3318	2.3115
CI1N	→	S	↓	0.1190	0.1235	1.3895	1.3149
A	→	CO0	↑	0.1021	0.1062	3.5675	3.4651
A	→	CO0	↓	0.1223	0.1275	2.4040	2.2991
B	→	CO0	↑	0.0794	0.0837	3.4953	3.4306
B	→	CO0	↓	0.0866	0.0905	2.3759	2.2922
CI0N	→	CO0	↑	0.0290	0.0234	3.1579	2.2844
CI0N	→	CO0	↓	0.0193	0.0176	1.8740	1.5127
A	→	CO1	↑	0.0994	0.1048	3.6272	3.5137
A	→	CO1	↓	0.1283	0.1328	2.4449	2.3482
B	→	CO1	↑	0.0680	0.0716	3.5735	3.4958
B	→	CO1	↓	0.0870	0.0911	2.4313	2.3428
CI1N	→	CO1	↑	0.0282	0.0229	3.1809	2.3947
CI1N	→	CO1	↓	0.0191	0.0147	1.9345	1.4635

Cell Description

The AFCSHCON cell provides a carry-select adder function that produces the arithmetic sum (S) and active-low carryouts (CO0N,CO1N) of two operands (A,B) with carry-ins (CI0,CI1). The three outputs (S,CO0N,CO1N) are represented by the logic equations:

$$S = CS \bullet (A \oplus B \oplus CI1) + \overline{CS} \bullet (A \oplus B \oplus CI0)$$

$$CO0N = \overline{(A \bullet B) + (A \bullet CI0) + (B \bullet CI0)}$$

$$CO1N = \overline{(A \bullet B) + (A \bullet CI1) + (B \bullet CI1)}$$

Logic Symbol
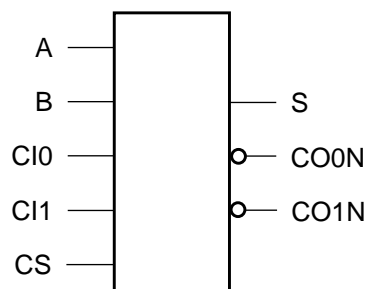
Cell Size

Drive Strength	Height (um)	Width (um)
AFCSHCONX2AD	2.52	15.12
AFCSHCONX4AD	2.52	16.24

Function Table

A	B	CI0	CI1	CS	S	CO0N	CO1N
0	0	0	0	0	0	1	1
0	0	0	0	1	0	1	1
0	0	0	1	0	0	1	1
0	0	0	1	1	1	1	1
0	0	1	0	0	1	1	1
0	0	1	0	1	0	1	1
0	0	1	1	0	1	1	1
0	0	1	1	1	1	1	1
0	1	0	0	0	1	1	1
0	1	0	0	1	1	1	1
0	1	0	1	0	1	1	0
0	1	0	1	1	0	1	0
0	1	1	0	0	0	0	1
0	1	1	0	1	1	0	1
0	1	1	1	0	0	0	0
0	1	1	1	1	0	0	0

Function Table (Cont'd.)

A	B	CI0	CI1	CS	S	CO0N	CO1N
1	0	0	0	0	1	1	1
1	0	0	0	1	1	1	1
1	0	0	1	0	1	1	0
1	0	0	1	1	0	1	0
1	0	1	0	0	0	0	1
1	0	1	0	1	1	0	1
1	0	1	1	0	0	0	0
1	0	1	1	1	0	0	0
1	1	0	0	0	0	0	0
1	1	0	0	1	0	0	0
1	1	0	1	0	0	0	0
1	1	0	1	1	1	0	0
1	1	1	0	0	1	0	0
1	1	1	0	1	0	0	0
1	1	1	1	0	1	0	0
1	1	1	1	1	1	0	0

Functional Schematic
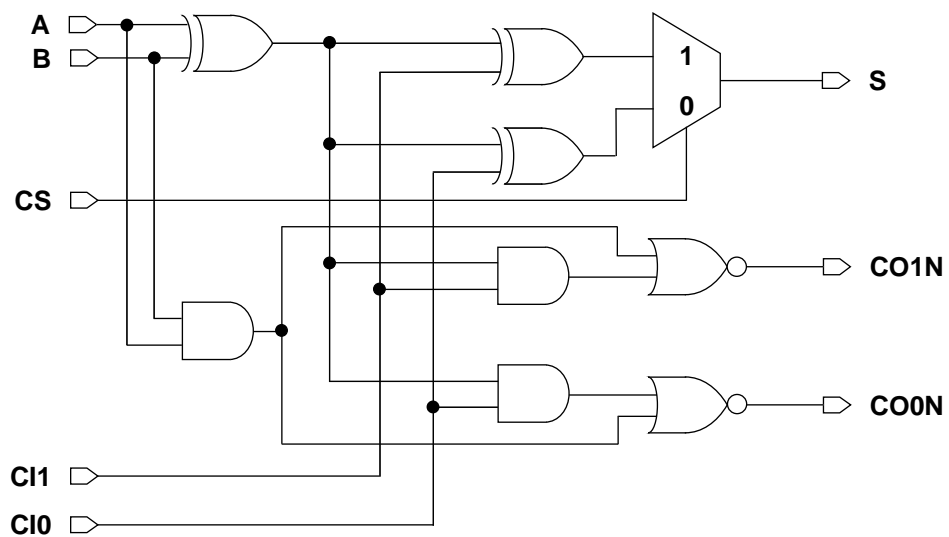
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
CS	0.0101	0.0105
A	0.0402	0.0415
B	0.0400	0.0413
CI0	0.0182	0.0240
CI1	0.0192	0.0227

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
CS	0.0040	0.0039
A	0.0052	0.0052
B	0.0066	0.0066
CI0	0.0048	0.0106
CI1	0.0055	0.0094

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
CS	→	S	↑	0.0823	0.0815	2.3398	2.3166
CS	→	S	↓	0.0797	0.0825	1.3929	1.3153
A	→	S	↑	0.2525	0.2571	2.3432	2.3178
A	→	S	↓	0.2403	0.2447	1.4028	1.3177
B	→	S	↑	0.2399	0.2444	2.3436	2.3177
B	→	S	↓	0.2279	0.2321	1.4028	1.3177
CI0	→	S	↑	0.1369	0.1353	2.3435	2.3181
CI0	→	S	↓	0.1375	0.1302	1.4012	1.3167
CI1	→	S	↑	0.1161	0.1136	2.3326	2.3141
CI1	→	S	↓	0.1202	0.1177	1.3930	1.3153
A	→	CO0N	↑	0.1061	0.1106	3.1739	2.9343
A	→	CO0N	↓	0.1356	0.1436	2.1610	1.9994
B	→	CO0N	↑	0.0981	0.0991	3.5831	2.9286
B	→	CO0N	↓	0.1229	0.1308	2.1594	1.9986
CI0	→	CO0N	↑	0.0266	0.0188	3.6054	2.6694
CI0	→	CO0N	↓	0.0195	0.0173	2.1792	1.7381
A	→	CO1N	↑	0.1197	0.1259	3.7483	3.0819
A	→	CO1N	↓	0.1389	0.1467	2.1118	1.9548
B	→	CO1N	↑	0.0928	0.0986	3.3079	2.9564
B	→	CO1N	↓	0.1262	0.1339	2.1095	1.9534
CI1	→	CO1N	↑	0.0259	0.0217	3.6559	3.0457
CI1	→	CO1N	↓	0.0196	0.0168	2.3472	1.9635

Cell Description

The AFCSIHCON cell provides a carry-select adder function for the initial stage of carry-select adder block. The function produces the arithmetic sum (S) and activelow carryouts (CO0N,CO1N) of two operands (A,B).The three outputs (S,CO0N,CO1N) are represented by the logic equations:

$S = A \oplus B \oplus CS$

$CO0N = \overline{A \bullet B}$

$CO1N = \overline{A + B}$

Logic Symbol
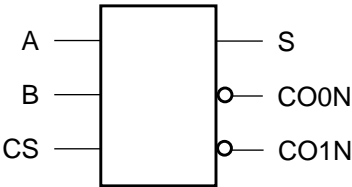
Function Table

A	B	CS	S	CO0N	CO1N
0	0	0	0	1	1
0	0	1	1	1	1
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	0	0	0
1	1	1	1	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
AFCSIHCONX2AD	2.52	6.16
AFCSIHCONX4AD	2.52	7.56

Functional Schematic
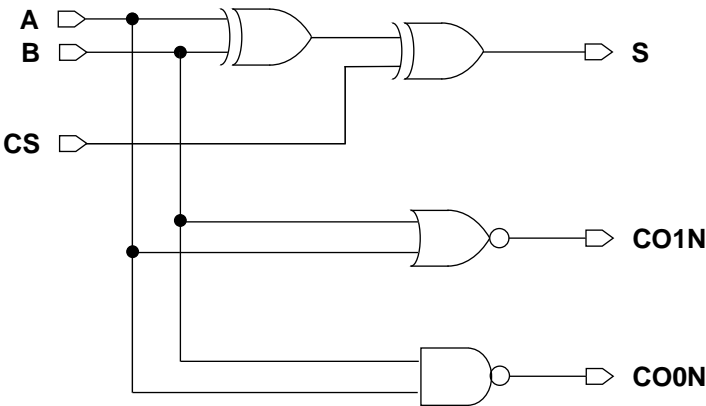
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
A	0.0188	0.0230
B	0.0186	0.0234
CS	0.0091	0.0094

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
A	0.0065	0.0107
B	0.0081	0.0123
CS	0.0040	0.0039

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
A	$\rightarrow$	S	$\uparrow$	0.1339	0.1356	2.3414	2.3176
A	$\rightarrow$	S	$\downarrow$	0.1468	0.1565	1.6762	1.4740
B	$\rightarrow$	S	$\uparrow$	0.1245	0.1263	2.4169	2.3473
B	$\rightarrow$	S	$\downarrow$	0.1442	0.1464	1.4149	1.3716
CS	$\rightarrow$	S	$\uparrow$	0.0754	0.0760	2.3357	2.3159
CS	$\rightarrow$	S	$\downarrow$	0.0656	0.0739	1.6414	1.4583
A	$\rightarrow$	CO0N	$\uparrow$	0.0154	0.0143	3.1323	1.5846
A	$\rightarrow$	CO0N	$\downarrow$	0.0129	0.0113	2.4264	1.1604
B	$\rightarrow$	CO0N	$\uparrow$	0.0190	0.0175	3.2209	1.5729
B	$\rightarrow$	CO0N	$\downarrow$	0.0139	0.0126	2.4251	1.1603
A	$\rightarrow$	CO1N	$\uparrow$	0.0195	0.0200	4.8953	2.3665
A	$\rightarrow$	CO1N	$\downarrow$	0.0102	0.0115	1.6107	0.7781
B	$\rightarrow$	CO1N	$\uparrow$	0.0249	0.0234	4.8949	2.3641
B	$\rightarrow$	CO1N	$\downarrow$	0.0120	0.0114	1.6080	0.7856

Cell Description

The AFHCIN cell is a full adder that provides the arithmetic sum (S) and carry-out (CO) of two operands (A,B) with active-low carry-in (CIN). The outputs (S,CO) are represented by the logic equations:

$$S = A \oplus B \oplus \overline{CIN}$$

$$CO = (A \bullet B) + (A \bullet \overline{CIN}) + (B \bullet \overline{CIN})$$

Logic Symbol
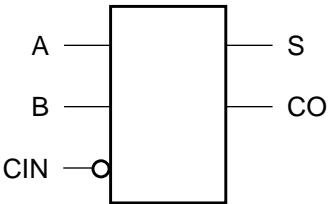
Function Table

A	B	CIN	S	CO
0	0	0	1	0
0	0	1	0	0
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

Cell Size

Drive Strength	Height (um)	Width (um)
AFHCINX2AD	2.52	8.96
AFHCINX4AD	2.52	11.48

Functional Schematic
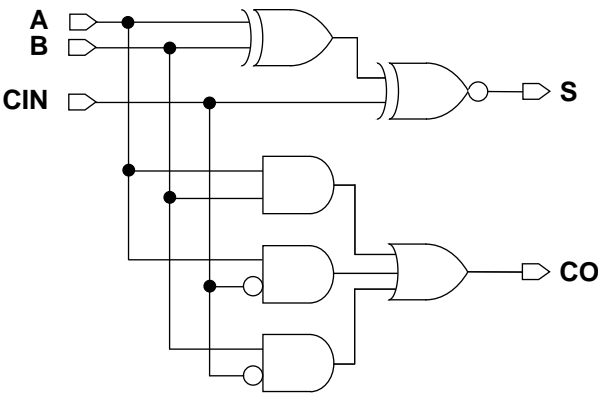
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
A	0.0252	0.0331
B	0.0260	0.0365
CIN	0.0177	0.0273

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
A	0.0028	0.0028
B	0.0068	0.0071
CIN	0.0053	0.0104

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
A	→	S	↑	0.1234	0.1509	2.4852	2.5184
A	→	S	↓	0.1344	0.1592	1.4496	1.3383
B	→	S	↑	0.0977	0.1299	2.4904	2.5212
B	→	S	↓	0.1065	0.1218	1.4504	1.3359
CIN	→	S	↑	0.0679	0.0677	2.4789	2.5149
CIN	→	S	↓	0.0744	0.0801	1.4528	1.3402
A	→	CO	↑	0.0761	0.0879	3.3926	2.5526
A	→	CO	↓	0.0931	0.1094	2.1475	1.5223
B	→	CO	↑	0.0622	0.0720	3.2532	2.5060
B	→	CO	↓	0.0783	0.0910	2.1064	1.4865
CIN	→	CO	↑	0.0264	0.0245	2.9965	1.5609
CIN	→	CO	↓	0.0209	0.0194	1.9644	0.9502

Cell Description

The AFHCON cell is a full adder that provides
the arithmetic sum (S) and active-low carry-out
(CON) of two operands (A,B) with carry-in (CI).
The outputs (S,CON) are represented by the
logic equations:

$S = A \oplus B \oplus CI$

$CON = \overline{(A \bullet B) + (A \bullet CI) + (B \bullet CI)}$

Logic Symbol
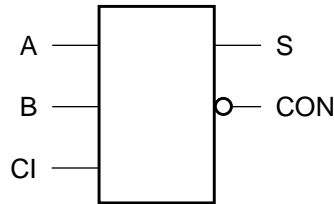
Function Table

A	B	CI	S	CON
0	0	0	0	1
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
AFHCONX2AD	2.52	8.96
AFHCONX4AD	2.52	9.52

Functional Schematic
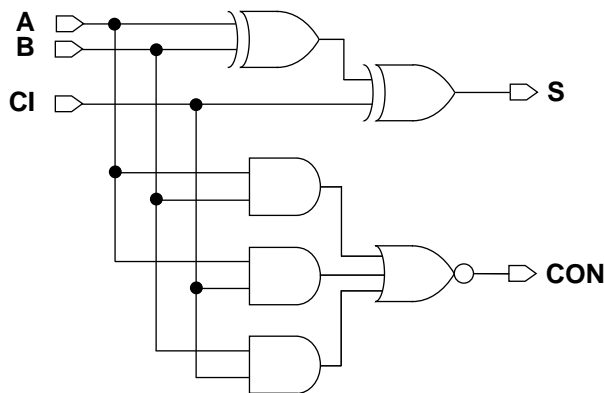
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
A	0.0252	0.0276
B	0.0236	0.0254
CI	0.0175	0.0214

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
A	0.0028	0.0028
B	0.0082	0.0082
CI	0.0052	0.0077

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
A	→	S	↑	0.1143	0.1199	2.4767	2.5004
A	→	S	↓	0.1289	0.1364	1.4393	1.3512
B	→	S	↑	0.0842	0.0888	2.4781	2.5011
B	→	S	↓	0.0981	0.1052	1.4395	1.3496
CI	→	S	↑	0.0660	0.0684	2.4695	2.4959
CI	→	S	↓	0.0744	0.0780	1.4424	1.3514
A	→	CON	↑	0.1018	0.1107	3.1498	3.2007
A	→	CON	↓	0.0889	0.1011	2.0319	2.0226
B	→	CON	↑	0.0731	0.0823	3.2075	3.2312
B	→	CON	↓	0.0588	0.0701	2.0674	2.0471
CI	→	CON	↑	0.0285	0.0233	3.1658	1.6292
CI	→	CON	↓	0.0211	0.0176	2.0701	1.0041

Cell Description

The AHCSHCIN cell provides a carry-select halfadder function that produces the arithmetic sum (S) and carryout (CO) of a single operand (A) with activelow carry-in (CIN). The outputs (S,CO) are represented by the following equations:

$$S = CS \bullet (A \oplus \overline{CIN}) + (\overline{CS} \bullet (A)$$

$$CO = A \bullet \overline{CIN}$$

Logic Symbol
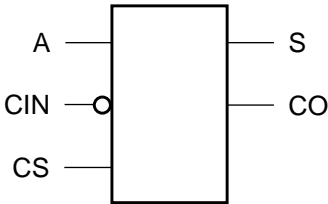
Function Table

A	CIN	CS	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	1	0
1	1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
AHCSHCINX2AD	2.52	5.32
AHCSHCINX4AD	2.52	6.16

Functional Schematic
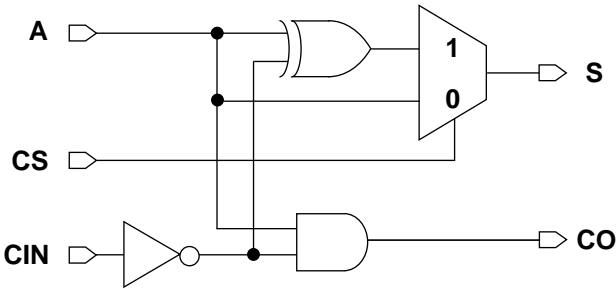
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
CS	0.0091	0.0095
A	0.0177	0.0211
CIN	0.0164	0.0192

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
CS	0.0039	0.0039
A	0.0029	0.0029
CIN	0.0073	0.0095

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
CS	→	S	↑	0.0592	0.0611	2.3290	2.2994
CS	→	S	↓	0.0633	0.0697	1.5527	1.3871
A	→	S	↑	0.1052	0.1160	2.3672	2.3135
A	→	S	↓	0.1282	0.1383	1.5728	1.3957
CIN	→	S	↑	0.0976	0.0989	2.3662	2.3128
CIN	→	S	↓	0.0955	0.1016	1.5718	1.3953
A	→	CO	↑	0.0470	0.0508	4.7435	2.4135
A	→	CO	↓	0.0640	0.0717	1.7134	0.8732
CIN	→	CO	↑	0.0188	0.0177	4.7483	2.4116
CIN	→	CO	↓	0.0102	0.0096	1.5874	0.7827

Cell Description

The AHCSHCON cell provides a carry-select halfadder function that produces the arithmetic sum (S) and active-low carryout (CON) of a single operand (A) with carry-in (CI). The outputs (S,CON) are represented by the following equations:

$$S = CS \bullet (A \oplus CI) + \overline{CS} \bullet (A)$$

$$CON = \overline{A \bullet CI}$$

Logic Symbol
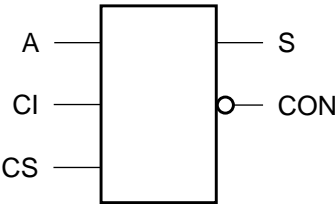
Function Table

A	CI	CS	S	CON
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	0
1	1	1	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
AHCSHCONX2AD	2.52	5.32
AHCSHCONX4AD	2.52	6.16

Functional Schematic
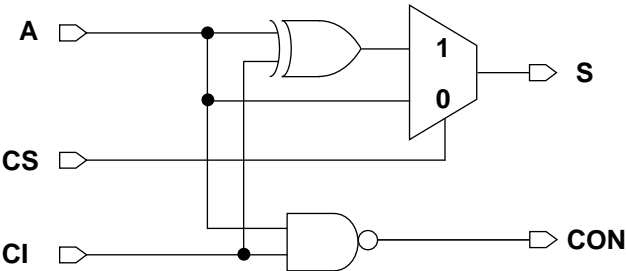
AC Power

Pin	Power (uW/MHz)	
	X2	X4
CS	0.0088	0.0089
A	0.0173	0.0208
CI	0.0130	0.0147

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
CS	0.0040	0.0039
A	0.0048	0.0075
CI	0.0061	0.0074

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)		K_{load} (ns/pF)	
			X2	X4	X2	X4
CS	→	S	↑	0.0593	0.0600	2.3269	2.3229
CS	→	S	↓	0.0637	0.0692	1.5677	1.3989
A	→	S	↑	0.0947	0.0969	2.3670	2.3376
A	→	S	↓	0.1286	0.1348	1.5883	1.4083
CI	→	S	↑	0.0778	0.0791	2.3540	2.3322
CI	→	S	↓	0.1238	0.1298	1.5880	1.4082
A	→	CON	↑	0.0190	0.0185	3.2460	1.6097
A	→	CON	↓	0.0126	0.0125	2.0815	1.0775
CI	→	CON	↑	0.0152	0.0146	3.1436	1.6470
CI	→	CON	↓	0.0112	0.0107	2.0797	1.0767

Cell Description

The AHHCIN cell is a half adder that provides the arithmetic sum (S) and carry-out (CO) of the input operand (A) with an active-low carry-in (CIN). The outputs (S,CO) are represented by the logic equations:

$S = A \oplus \overline{CIN}$

$CO = A \bullet \overline{CIN}$

Logic Symbol
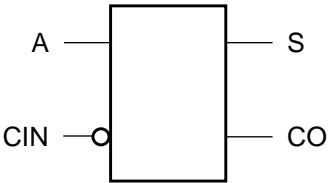
Function Table

A	CIN	S	CO
0	0	1	0
0	1	0	0
1	0	0	1
1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
AHHCINX2AD	2.52	4.20
AHHCINX4AD	2.52	5.04

Functional Schematic
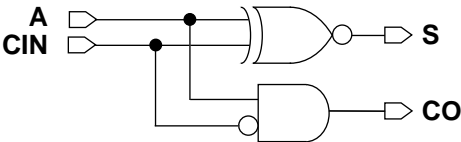
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
A	0.0134	0.0167
CIN	0.0119	0.0159

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
A	0.0040	0.0050
CIN	0.0069	0.0091

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
A	→	S	↑	0.0423	0.0419	3.1028	3.1697
A	→	S	↓	0.0457	0.0464	1.8556	1.8478
CIN	→	S	↑	0.0278	0.0272	3.1190	3.1770
CIN	→	S	↓	0.0395	0.0385	1.7044	1.7435
A	→	CO	↑	0.0356	0.0331	4.5661	2.3632
A	→	CO	↓	0.0392	0.0348	1.3007	0.6406
CIN	→	CO	↑	0.0244	0.0245	4.5601	2.3619
CIN	→	CO	↓	0.0101	0.0100	1.2518	0.6303

Cell Description

The AHHCON cell is a half adder that provides the arithmetic sum (S) and active-low carry-out (CON) of the input operand (A) with carry-in (CI). The outputs (S,CON) are represented by the logic equations:

$S = A \oplus CI$

$CON = \overline{A \cdot CI}$

Logic Symbol
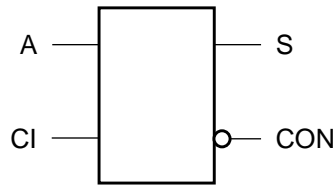
Function Table

A	CI	S	CON
0	0	0	1
0	1	1	1
1	0	1	1
1	1	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
AHHCONX2AD	2.52	3.64
AHHCONX4AD	2.52	6.16

Functional Schematic
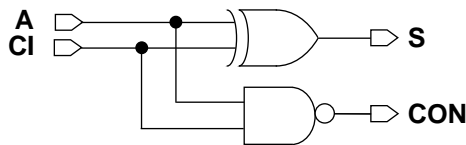
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
A	0.0134	0.0263
CI	0.0083	0.0156

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
A	0.0051	0.0107
CI	0.0071	0.0134

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
A	→	S	↑	0.0386	0.0381	3.2182	1.6287
A	→	S	↓	0.0465	0.0441	1.9975	1.0149
CI	→	S	↑	0.0267	0.0259	3.1247	1.6316
CI	→	S	↓	0.0379	0.0356	1.8962	0.9696
A	→	CON	↑	0.0164	0.0167	2.4630	1.2388
A	→	CON	↓	0.0138	0.0141	2.1839	1.1040
CI	→	CON	↑	0.0136	0.0140	2.3883	1.2184
CI	→	CON	↓	0.0127	0.0129	2.1836	1.1046

Cell Description

The AND2 cell provides the logical AND of two inputs (A,B). The output (Y) is represented by the logic equation:

$Y = (A \bullet B)$

Logic Symbol
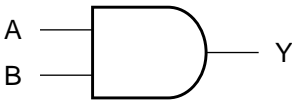
Function Table

A	B	Y
0	x	0
x	0	0
1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
AND2XLAD	2.52	1.40
AND2X1AD	2.52	1.40
AND2X2AD	2.52	1.40
AND2X4AD	2.52	2.24
AND2X6AD	2.52	2.80
AND2X8AD	2.52	3.92

Functional Schematic
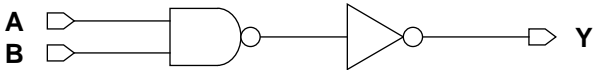
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0025	0.0030	0.0045	0.0081	0.0120	0.0161
B	0.0029	0.0034	0.0052	0.0093	0.0139	0.0185

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0011	0.0011	0.0015	0.0028	0.0038	0.0054
B	0.0012	0.0012	0.0016	0.0029	0.0042	0.0053

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)					
				XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	$\rightarrow$	Y	$\uparrow$	0.0385	0.0410	0.0363	0.0343	0.0321	0.0337
A	$\rightarrow$	Y	$\downarrow$	0.0453	0.0518	0.0434	0.0403	0.0409	0.0401
B	$\rightarrow$	Y	$\uparrow$	0.0410	0.0434	0.0384	0.0359	0.0342	0.0353
B	$\rightarrow$	Y	$\downarrow$	0.0516	0.0583	0.0494	0.0447	0.0453	0.0459

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)					
				XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	$\rightarrow$	Y	$\uparrow$	5.5692	3.5431	2.3392	1.1785	0.8130	0.6063
A	$\rightarrow$	Y	$\downarrow$	4.0904	3.0837	1.3115	0.6491	0.4338	0.3225
B	$\rightarrow$	Y	$\uparrow$	5.5705	3.5432	2.3391	1.1784	0.8131	0.6064
B	$\rightarrow$	Y	$\downarrow$	4.1269	3.1015	1.3208	0.6523	0.4354	0.3254

Cell Description

The AND3 cell provides the logical AND of three inputs (A,B,C). The output (Y) is represented by the logic equation:

$Y = (A \bullet B \bullet C)$

Logic Symbol
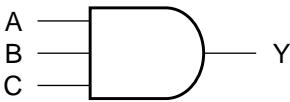
Function Table

A	B	C	Y
0	x	x	0
x	0	x	0
x	x	0	0
1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
AND3XLAD	2.52	1.68
AND3X1AD	2.52	1.68
AND3X2AD	2.52	1.68
AND3X4AD	2.52	3.08
AND3X6AD	2.52	3.64
AND3X8AD	2.52	5.04

Functional Schematic
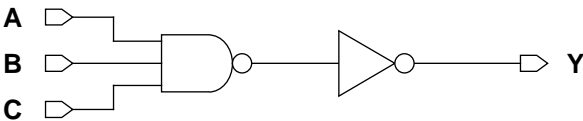
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0028	0.0034	0.0051	0.0091	0.0131	0.0180
B	0.0032	0.0038	0.0058	0.0106	0.0154	0.0209
C	0.0036	0.0043	0.0066	0.0122	0.0179	0.0239

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0010	0.0011	0.0016	0.0029	0.0041	0.0064
B	0.0011	0.0012	0.0016	0.0031	0.0044	0.0060
C	0.0012	0.0013	0.0017	0.0037	0.0048	0.0060

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	0.0553	0.0511	0.0445	0.0407	0.0378	0.0390
A	→ Y	↓	0.0558	0.0620	0.0495	0.0462	0.0449	0.0445
B	→ Y	↑	0.0588	0.0545	0.0479	0.0442	0.0416	0.0422
B	→ Y	↓	0.0586	0.0678	0.0568	0.0517	0.0511	0.0507
C	→ Y	↑	0.0619	0.0575	0.0503	0.0470	0.0439	0.0440
C	→ Y	↓	0.0641	0.0744	0.0627	0.0565	0.0563	0.0561

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	5.7379	3.5973	2.3571	1.2143	0.8231	0.6163
A	→ Y	↓	4.2338	3.1332	1.3282	0.6571	0.4324	0.3252
B	→ Y	↑	5.7379	3.5974	2.3567	1.2147	0.8231	0.6161
B	→ Y	↓	4.2429	3.1525	1.3443	0.6616	0.4353	0.3283
C	→ Y	↑	5.7392	3.5976	2.3569	1.2146	0.8228	0.6160
C	→ Y	↓	4.2789	3.1712	1.3544	0.6639	0.4380	0.3315

Cell Description

The AND4 cell provides the logical AND of four inputs (A,B,C,D). The output (Y) is represented by the logic equation:

$Y = (A \bullet B \bullet C \bullet D)$

Logic Symbol
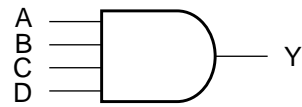
Function Table

A	B	C	D	Y
0	x	x	x	0
x	0	x	x	0
x	x	0	x	0
x	x	x	0	0
1	1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
AND4XLAD	2.52	2.24
AND4X1AD	2.52	2.24
AND4X2AD	2.52	2.24
AND4X4AD	2.52	3.64
AND4X6AD	2.52	5.04
AND4X8AD	2.52	6.44

Functional Schematic
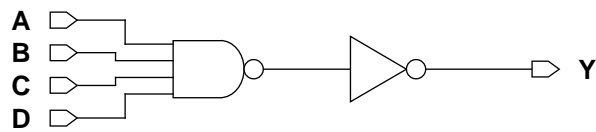
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0030	0.0036	0.0054	0.0094	0.0149	0.0195
B	0.0034	0.0042	0.0064	0.0113	0.0174	0.0228
C	0.0038	0.0048	0.0074	0.0130	0.0200	0.0264
D	0.0042	0.0053	0.0083	0.0149	0.0229	0.0303

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0010	0.0011	0.0017	0.0031	0.0056	0.0068
B	0.0011	0.0012	0.0017	0.0035	0.0054	0.0069
C	0.0010	0.0012	0.0017	0.0035	0.0052	0.0072
D	0.0013	0.0014	0.0019	0.0039	0.0057	0.0079

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	0.0677	0.0559	0.0495	0.0439	0.0474	0.0468
A	→ Y	↓	0.0550	0.0629	0.0528	0.0468	0.0515	0.0498
B	→ Y	↑	0.0729	0.0612	0.0546	0.0498	0.0525	0.0520
B	→ Y	↓	0.0596	0.0698	0.0613	0.0556	0.0571	0.0551
C	→ Y	↑	0.0760	0.0644	0.0579	0.0530	0.0560	0.0556
C	→ Y	↓	0.0636	0.0759	0.0676	0.0617	0.0647	0.0631
D	→ Y	↑	0.0821	0.0694	0.0615	0.0557	0.0589	0.0586
D	→ Y	↓	0.0718	0.0863	0.0739	0.0680	0.0706	0.0688

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)					
				XL	X1	X2	X4	X6	X8
A	→	Y	↑	6.0336	3.7468	2.3770	1.2254	0.8311	0.6287
A	→	Y	↓	4.2179	3.1227	1.3356	0.6567	0.4461	0.3313
B	→	Y	↑	6.0338	3.7466	2.3768	1.2254	0.8309	0.6287
B	→	Y	↓	4.2529	3.1447	1.3540	0.6651	0.4483	0.3329
C	→	Y	↑	6.0332	3.7461	2.3764	1.2255	0.8309	0.6286
C	→	Y	↓	4.2921	3.1695	1.3680	0.6721	0.4544	0.3376
D	→	Y	↑	6.0351	3.7467	2.3760	1.2256	0.8310	0.6288
D	→	Y	↓	4.3471	3.2024	1.3786	0.6790	0.4582	0.3404

Cell Description

The AO21 cell provides the logical OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = (A0 \bullet A1) + \overline{B0}$$

Logic Symbol
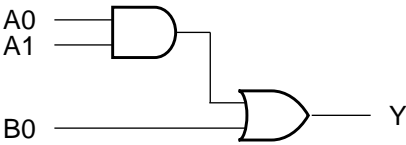
Function Table

A0	A1	B0	Y
0	x	0	0
x	0	0	0
x	x	1	1
1	1	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
AO21XLAD	2.52	1.96
AO21X1AD	2.52	1.96
AO21X2AD	2.52	1.96
AO21X4AD	2.52	2.52

Functional Schematic
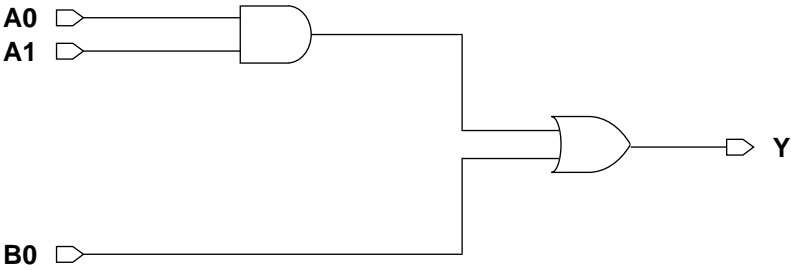
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0031	0.0037	0.0056	0.0106
A1	0.0034	0.0040	0.0062	0.0117
B0	0.0031	0.0037	0.0057	0.0104

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0010	0.0011	0.0016	0.0027
A1	0.0009	0.0010	0.0015	0.0026
B0	0.0011	0.0012	0.0016	0.0026

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0438	0.0483	0.0431	0.0422	5.5962	3.6085	2.3198	1.1862
A0	→	Y	↓	0.0930	0.0886	0.0717	0.0662	4.9181	3.2536	1.3976	0.6804
A1	→	Y	↑	0.0449	0.0494	0.0445	0.0436	5.5979	3.6090	2.3200	1.1864
A1	→	Y	↓	0.0991	0.0930	0.0766	0.0715	4.9467	3.2620	1.4029	0.6843
B0	→	Y	↑	0.0291	0.0301	0.0329	0.0308	5.4545	3.5237	2.2978	1.1758
B0	→	Y	↓	0.0871	0.0816	0.0674	0.0626	4.9484	3.2624	1.4031	0.6842

Cell Description

The AO22 cell provides the logical OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = (A0 \bullet A1) + (B0 \bullet B1)$$

Logic Symbol
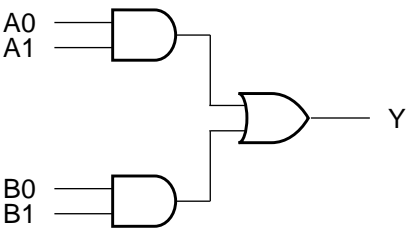
Function Table

A0	A1	B0	B1	Y
0	x	0	x	0
0	x	x	0	0
x	0	0	x	0
x	0	x	0	0
x	x	1	1	1
1	1	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
AO22XLAD	2.52	2.24
AO22X1AD	2.52	2.24
AO22X2AD	2.52	2.52
AO22X4AD	2.52	2.80

Functional Schematic
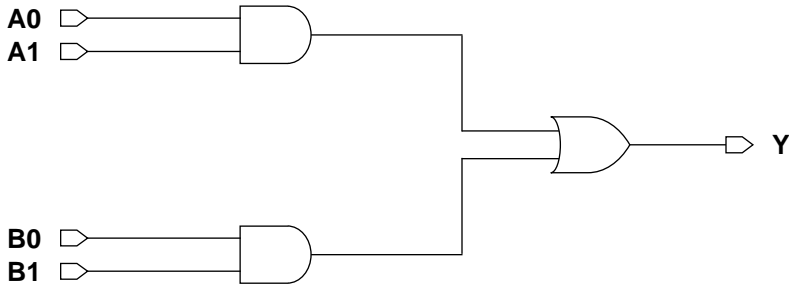
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0035	0.0040	0.0063	0.0112
A1	0.0039	0.0045	0.0070	0.0124
B0	0.0040	0.0044	0.0073	0.0129
B1	0.0043	0.0048	0.0079	0.0140

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0011	0.0011	0.0017	0.0028
A1	0.0012	0.0011	0.0017	0.0028
B0	0.0010	0.0011	0.0017	0.0027
B1	0.0009	0.0009	0.0015	0.0026

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0442	0.0446	0.0410	0.0403	5.6054	3.5536	2.3125	1.1807
A0	→	Y	↓	0.0980	0.1029	0.0774	0.0670	5.1417	3.4369	1.4479	0.6984
A1	→	Y	↑	0.0467	0.0469	0.0432	0.0420	5.6063	3.5539	2.3117	1.1806
A1	→	Y	↓	0.1084	0.1121	0.0847	0.0730	5.1899	3.4541	1.4572	0.7027
B0	→	Y	↑	0.0507	0.0531	0.0485	0.0483	5.6948	3.6080	2.3282	1.1884
B0	→	Y	↓	0.1150	0.1263	0.0928	0.0805	5.1503	3.4449	1.4510	0.6995
B1	→	Y	↑	0.0519	0.0541	0.0502	0.0499	5.6958	3.6084	2.3284	1.1884
B1	→	Y	↓	0.1212	0.1307	0.0977	0.0852	5.1915	3.4553	1.4572	0.7025

Cell Description

The AO2B2 cell provides the logical OR of
two AND groups consisting of two inputs
each: (A0,A1N) and (B0,B1). The output (Y) is
represented by the logic equation:

$Y = (A0 \bullet \overline{A1N}) + (B0 \bullet B1)$

Logic Symbol
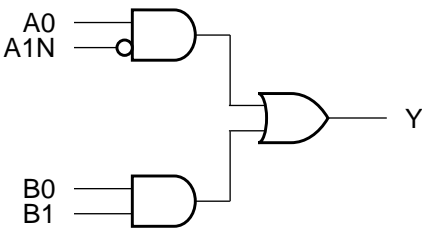
Function Table

A0	A1N	B0	B1	Y
1	0	x	x	1
x	x	1	1	1
0	x	0	x	0
x	1	0	x	0
0	x	x	0	0
x	1	x	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
AO2B2XLAD	2.52	2.80
AO2B2X1AD	2.52	2.80
AO2B2X2AD	2.52	2.80
AO2B2X4AD	2.52	3.08

Functional Schematic
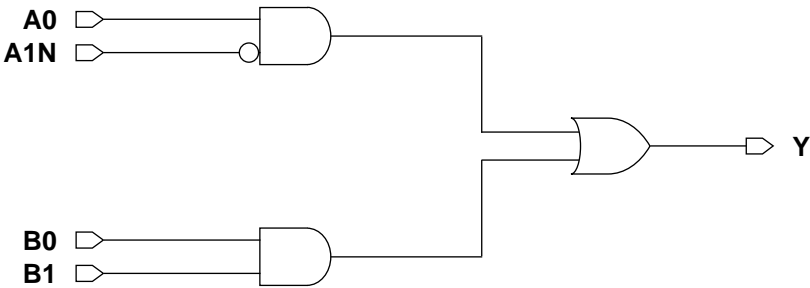
AC Power

Pin	Power (uW/MHz)			
	XL	X1	X2	X4
A0	0.0035	0.0043	0.0063	0.0113
A1N	0.0041	0.0048	0.0072	0.0128
B0	0.0041	0.0048	0.0073	0.0133
B1	0.0044	0.0052	0.0078	0.0144

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0008	0.0007	0.0011	0.0018
A1N	0.0009	0.0009	0.0012	0.0014
B0	0.0010	0.0010	0.0016	0.0028
B1	0.0009	0.0009	0.0015	0.0026

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	X1	X2	X4	XL	X1	X2	X4
A0	→	Y	↑	0.0466	0.0484	0.0436	0.0426	5.7152	3.6390	2.3326	1.1949
A0	→	Y	↓	0.0989	0.1122	0.0772	0.0692	5.2846	3.5529	1.4664	0.7110
A1N	→	Y	↑	0.0774	0.0795	0.0744	0.0770	5.7191	3.6405	2.3330	1.1952
A1N	→	Y	↓	0.1193	0.1328	0.0959	0.0925	5.3279	3.5721	1.4748	0.7149
B0	→	Y	↑	0.0543	0.0575	0.0522	0.0506	5.8194	3.6987	2.3515	1.2018
B0	→	Y	↓	0.1245	0.1383	0.0945	0.0843	5.3073	3.5667	1.4720	0.7121
B1	→	Y	↑	0.0554	0.0586	0.0536	0.0521	5.8195	3.6988	2.3519	1.2017
B1	→	Y	↓	0.1287	0.1422	0.0984	0.0886	5.3257	3.5725	1.4748	0.7150

Cell Description

The AO2B2B cell provides the logical OR of two AND groups consisting of two inputs each: (A0,A1N) and (B0,B1N). The output (Y) is represented by the logic equation:

$$Y = (A0 \bullet \overline{A1N}) + (B0 \bullet \overline{B1N})$$

Logic Symbol
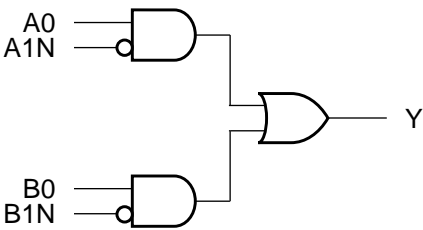
Function Table

A0	A1N	B0	B1N	Y
0	x	0	x	0
0	x	x	1	0
x	1	0	x	0
x	1	x	1	0
x	x	1	0	1
1	0	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
AO2B2BXLAD	2.52	3.36
AO2B2BX1AD	2.52	3.36
AO2B2BX2AD	2.52	3.36
AO2B2BX4AD	2.52	3.92

Functional Schematic
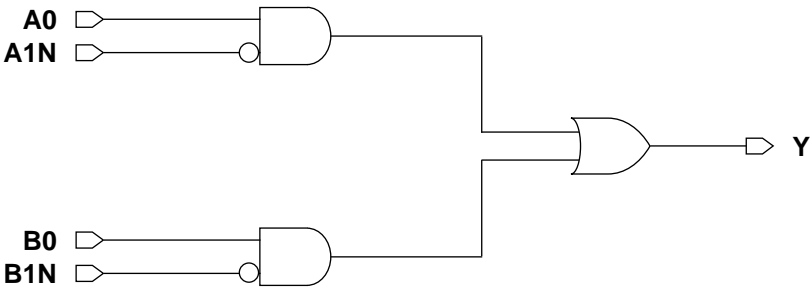
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0035	0.0043	0.0064	0.0113
A1N	0.0040	0.0048	0.0073	0.0128
B0	0.0041	0.0049	0.0074	0.0132
B1N	0.0046	0.0051	0.0079	0.0144

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0012	0.0012	0.0017	0.0028
A1N	0.0009	0.0009	0.0012	0.0014
B0	0.0010	0.0011	0.0016	0.0027
B1N	0.0011	0.0011	0.0014	0.0014

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0462	0.0495	0.0449	0.0427	5.7121	3.6468	2.3300	1.1989
A0	→	Y	↓	0.0978	0.1122	0.0780	0.0693	5.2752	3.5489	1.4682	0.7105
A1N	→	Y	↑	0.0770	0.0804	0.0754	0.0764	5.7164	3.6487	2.3303	1.1995
A1N	→	Y	↓	0.1182	0.1321	0.0962	0.0923	5.3132	3.5669	1.4753	0.7153
B0	→	Y	↑	0.0531	0.0562	0.0519	0.0501	5.8102	3.6928	2.3460	1.2055
B0	→	Y	↓	0.1234	0.1367	0.0947	0.0847	5.2869	3.5582	1.4710	0.7127
B1N	→	Y	↑	0.0833	0.0866	0.0812	0.0815	5.8084	3.6927	2.3457	1.2053
B1N	→	Y	↓	0.1405	0.1535	0.1105	0.1059	5.3115	3.5656	1.4750	0.7152

Cell Description

The AOI21 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + B0}$$

Logic Symbol
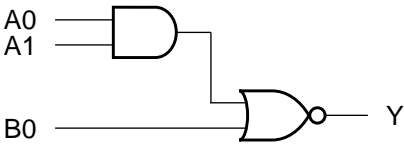
Function Table

A0	A1	B0	Y
0	x	0	1
x	0	0	1
x	x	1	0
1	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI21XLAD	2.52	1.40
AOI21X1AD	2.52	1.40
AOI21X2AD	2.52	1.68
AOI21X3AD	2.52	2.52
AOI21X4AD	2.52	2.52
AOI21X6AD	2.52	3.64
AOI21X8AD	2.52	4.76

Functional Schematic
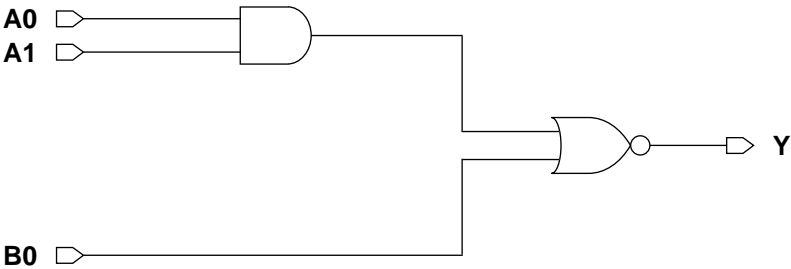
AC Power

Pin	Power (uW/MHz)						
	XL	X1	X2	X3	X4	X6	X8
A0	0.0021	0.0029	0.0048	0.0076	0.0097	0.0143	0.0186
A1	0.0024	0.0033	0.0058	0.0090	0.0116	0.0173	0.0227
B0	0.0019	0.0025	0.0045	0.0070	0.0091	0.0134	0.0175

Pin Capacitance

Pin	Capacitance (pF)						
	XL	X1	X2	X3	X4	X6	X8
A0	0.0013	0.0017	0.0028	0.0045	0.0057	0.0082	0.0107
A1	0.0012	0.0016	0.0026	0.0039	0.0051	0.0079	0.0108
B0	0.0014	0.0018	0.0029	0.0042	0.0054	0.0080	0.0106

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)						
			XL	X1	X2	X3	X4	X6	X8
A0	→ Y	↑	0.0327	0.0280	0.0299	0.0313	0.0302	0.0302	0.0298
A0	→ Y	↓	0.0246	0.0234	0.0168	0.0171	0.0167	0.0163	0.0158
A1	→ Y	↑	0.0355	0.0316	0.0348	0.0369	0.0357	0.0362	0.0356
A1	→ Y	↓	0.0257	0.0249	0.0183	0.0181	0.0179	0.0177	0.0173
B0	→ Y	↑	0.0247	0.0232	0.0263	0.0278	0.0267	0.0271	0.0263
B0	→ Y	↓	0.0121	0.0118	0.0094	0.0096	0.0094	0.0092	0.0090

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)						
			XL	X1	X2	X3	X4	X6	X8
A0	→ Y	↑	11.1263	7.1799	4.6694	3.1927	2.3786	1.6267	1.2442
A0	→ Y	↓	7.5210	5.2208	2.1937	1.4543	1.1001	0.7254	0.5407
A1	→ Y	↑	10.8644	7.2361	4.6068	3.2411	2.4092	1.6306	1.2298
A1	→ Y	↓	7.5198	5.2199	2.1940	1.4536	1.1000	0.7257	0.5407
B0	→ Y	↑	10.9815	7.2592	4.6199	3.2498	2.4157	1.6341	1.2329
B0	→ Y	↓	4.2469	2.9573	1.2333	0.8275	0.6287	0.4106	0.3088

Cell Description

The AOI211 cell provides the logical inverted OR of one AND group and two additional inputs. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + B0 + C0}$$

Logic Symbol
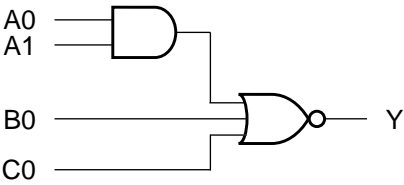
Function Table

A0	A1	B0	C0	Y
0	x	0	0	1
x	0	0	0	1
x	x	x	1	0
x	x	1	x	0
1	1	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI211XLAD	2.52	1.68
AOI211X1AD	2.52	1.68
AOI211X2AD	2.52	1.68
AOI211X4AD	2.52	3.08

Functional Schematic
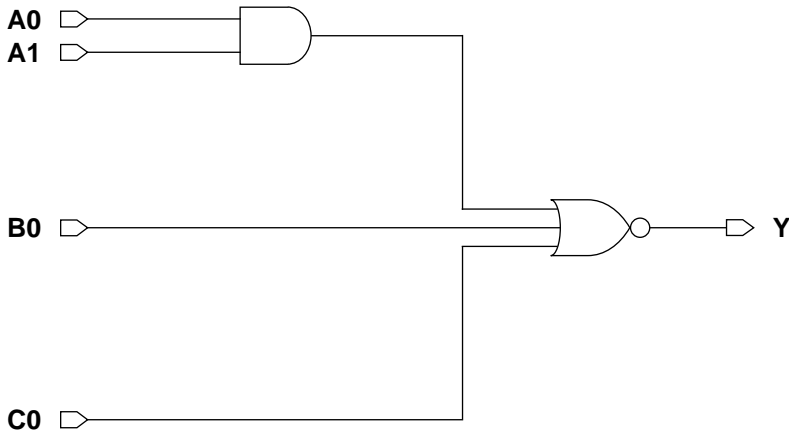
AC Power

Pin	Power (uW/MHz)			
	XL	X1	X2	X4
A0	0.0031	0.0042	0.0065	0.0131
A1	0.0034	0.0045	0.0074	0.0150
B0	0.0024	0.0031	0.0053	0.0106
C0	0.0028	0.0037	0.0062	0.0126

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0015	0.0018	0.0028	0.0057
A1	0.0013	0.0016	0.0026	0.0050
B0	0.0014	0.0018	0.0028	0.0053
C0	0.0014	0.0018	0.0028	0.0056

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	X1	X2	X4	XL	X1	X2	X4
A0	$\rightarrow$	Y	$\uparrow$	0.0590	0.0512	0.0524	0.0531	16.9944	10.9478	7.0691	3.6022
A0	$\rightarrow$	Y	$\downarrow$	0.0273	0.0290	0.0194	0.0191	6.9768	5.2699	2.2168	1.1106
A1	$\rightarrow$	Y	$\uparrow$	0.0637	0.0553	0.0597	0.0612	16.7753	10.8096	6.9850	3.6323
A1	$\rightarrow$	Y	$\downarrow$	0.0283	0.0302	0.0208	0.0202	6.9772	5.2678	2.2169	1.1103
B0	$\rightarrow$	Y	$\uparrow$	0.0458	0.0372	0.0421	0.0413	16.8713	10.8451	7.0059	3.6410
B0	$\rightarrow$	Y	$\downarrow$	0.0147	0.0135	0.0106	0.0101	4.2229	2.9449	1.2547	0.6120
C0	$\rightarrow$	Y	$\uparrow$	0.0561	0.0474	0.0528	0.0539	16.8159	10.8342	6.9995	3.6397
C0	$\rightarrow$	Y	$\downarrow$	0.0163	0.0154	0.0118	0.0116	4.1679	2.9055	1.2381	0.6195

Cell Description

The AOI21B cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + \overline{B0N}}$$

Logic Symbol
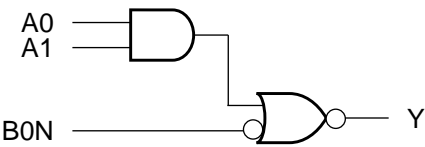
Function Table

A0	A1	B0N	Y
x	x	0	0
x	0	1	1
0	x	1	1
1	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI21BXLAD	2.52	2.24
AOI21BX1AD	2.52	2.24
AOI21BX2AD	2.52	2.24
AOI21BX4AD	2.52	2.52

Functional Schematic
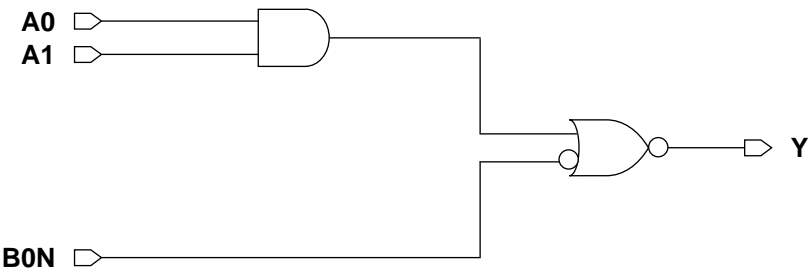
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0041	0.0045	0.0063	0.0101
A1	0.0038	0.0042	0.0059	0.0096
B0N	0.0024	0.0029	0.0045	0.0082

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0011	0.0011	0.0013	0.0014
A1	0.0011	0.0011	0.0014	0.0014
B0N	0.0010	0.0011	0.0015	0.0024

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0825	0.0847	0.0764	0.0790	5.7390	3.6257	2.3488	1.2113
A0	→	Y	↓	0.0791	0.0835	0.0698	0.0707	4.6533	3.1920	1.3552	0.6613
A1	→	Y	↑	0.0761	0.0782	0.0704	0.0732	5.7370	3.6250	2.3491	1.2115
A1	→	Y	↓	0.0778	0.0822	0.0685	0.0697	4.6543	3.1923	1.3550	0.6612
B0N	→	Y	↑	0.0396	0.0416	0.0393	0.0391	5.7316	3.6231	2.3487	1.2117
B0N	→	Y	↓	0.0538	0.0574	0.0478	0.0440	4.6732	3.1993	1.3583	0.6610

Cell Description

The AOI22 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + (B0 \bullet B1)}$$

Logic Symbol
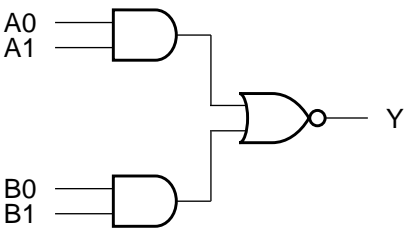
Function Table

A0	A1	B0	B1	Y
0	x	0	x	1
0	x	x	0	1
x	0	0	x	1
x	0	x	0	1
x	x	1	1	0
1	1	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI22XLAD	2.52	1.68
AOI22X1AD	2.52	1.96
AOI22X2AD	2.52	1.96
AOI22X4AD	2.52	3.36

Functional Schematic

TSMC CLN90G
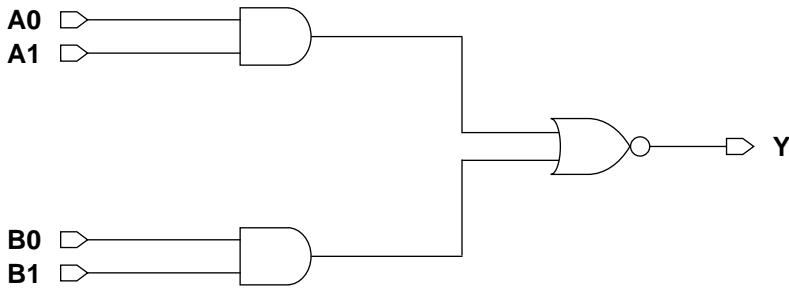
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0021	0.0029	0.0049	0.0097
A1	0.0025	0.0034	0.0059	0.0118
B0	0.0028	0.0041	0.0066	0.0130
B1	0.0031	0.0045	0.0075	0.0151

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0018	0.0028	0.0054
A1	0.0014	0.0019	0.0029	0.0057
B0	0.0013	0.0017	0.0027	0.0053
B1	0.0012	0.0016	0.0026	0.0055

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0272	0.0263	0.0293	0.0298	11.1903	7.3190	4.7210	2.4224
A0	→	Y	↓	0.0200	0.0200	0.0145	0.0142	7.4150	5.1712	2.1957	1.0821
A1	→	Y	↑	0.0317	0.0302	0.0346	0.0355	11.0075	7.2376	4.6679	2.3965
A1	→	Y	↓	0.0223	0.0224	0.0165	0.0160	7.4227	5.1740	2.1964	1.0823
B0	→	Y	↑	0.0458	0.0403	0.0425	0.0426	11.1856	7.3171	4.7301	2.4281
B0	→	Y	↓	0.0340	0.0326	0.0217	0.0211	7.4898	5.1882	2.1930	1.0835
B1	→	Y	↑	0.0481	0.0428	0.0468	0.0480	10.8696	7.1858	4.6433	2.3915
B1	→	Y	↓	0.0354	0.0341	0.0233	0.0228	7.4905	5.1885	2.1923	1.0840

Cell Description

The AOI221 cell provides the logical inverted OR of two AND groups and a third input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + (B0 \bullet B1) + C0}$$

Logic Symbol
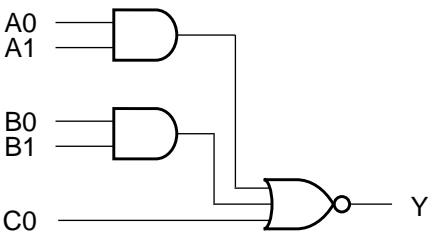
Function Table

A0	A1	B0	B1	C0	Y
0	x	0	x	0	1
0	x	x	0	0	1
x	0	0	x	0	1
x	0	x	0	0	1
x	x	x	x	1	0
x	x	1	1	x	0
1	1	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI221XLAD	2.52	2.24
AOI221X1AD	2.52	2.52
AOI221X2AD	2.52	2.52
AOI221X4AD	2.52	4.48

Functional Schematic
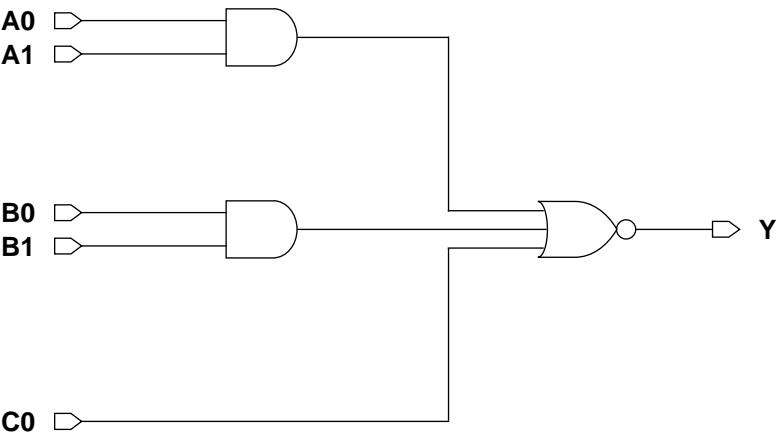
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0030	0.0042	0.0070	0.0130
A1	0.0032	0.0046	0.0079	0.0151
B0	0.0037	0.0053	0.0085	0.0160
B1	0.0040	0.0057	0.0095	0.0181
C0	0.0027	0.0037	0.0068	0.0126

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0014	0.0017	0.0027	0.0051
A1	0.0013	0.0017	0.0027	0.0052
B0	0.0013	0.0017	0.0026	0.0051
B1	0.0012	0.0016	0.0026	0.0054
C0	0.0015	0.0018	0.0029	0.0054

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0618	0.0557	0.0613	0.0578	16.0378	10.6465	6.8794	3.5894
A0	→	Y	↓	0.0292	0.0283	0.0200	0.0181	7.3567	5.1072	2.1702	1.0731
A1	→	Y	↑	0.0681	0.0618	0.0699	0.0655	16.2762	10.7286	6.9288	3.5455
A1	→	Y	↓	0.0304	0.0300	0.0214	0.0195	7.3554	5.1069	2.1701	1.0732
B0	→	Y	↑	0.0738	0.0672	0.0716	0.0688	16.2973	10.7517	6.9419	3.5954
B0	→	Y	↓	0.0339	0.0343	0.0222	0.0203	7.7062	5.2994	2.2356	1.1111
B1	→	Y	↑	0.0793	0.0719	0.0796	0.0767	16.2673	10.7266	6.9287	3.5351
B1	→	Y	↓	0.0352	0.0354	0.0237	0.0220	7.7092	5.2992	2.2358	1.1113
C0	→	Y	↑	0.0448	0.0411	0.0509	0.0468	16.3506	10.7574	6.9454	3.5515
C0	→	Y	↓	0.0143	0.0138	0.0111	0.0102	4.2477	2.9411	1.2561	0.6196

Cell Description

The AOI222 cell provides the logical inverted OR of three AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + (B0 \bullet B1) + (C0 \bullet C1)}$$

Logic Symbol
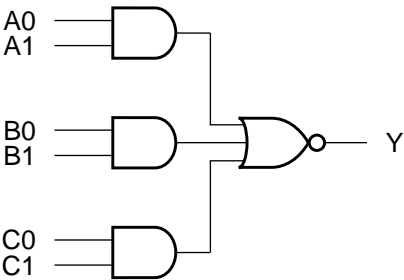
Function Table

A0	A1	B0	B1	C0	C1	Y
0	x	0	x	0	x	1
0	x	0	x	x	0	1
0	x	x	0	0	x	1
0	x	x	0	x	0	1
x	0	0	x	0	x	1
x	0	0	x	x	0	1
x	0	x	0	0	x	1
x	0	x	0	x	0	1
x	x	x	x	1	1	0
x	x	1	1	x	x	0
1	1	x	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI222XLAD	2.52	2.52
AOI222X1AD	2.52	2.80
AOI222X2AD	2.52	2.80
AOI222X4AD	2.52	5.04

Functional Schematic
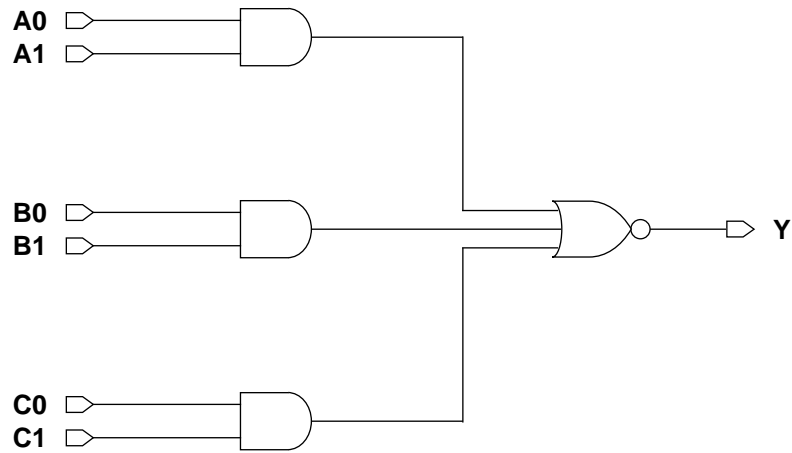
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0030	0.0041	0.0072	0.0137
A1	0.0034	0.0046	0.0081	0.0157
B0	0.0037	0.0052	0.0087	0.0167
B1	0.0040	0.0057	0.0096	0.0188
C0	0.0045	0.0064	0.0103	0.0198
C1	0.0048	0.0068	0.0112	0.0218

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0018	0.0028	0.0053
A1	0.0014	0.0018	0.0028	0.0057
B0	0.0013	0.0017	0.0028	0.0053
B1	0.0013	0.0018	0.0026	0.0055
C0	0.0013	0.0017	0.0027	0.0052
C1	0.0013	0.0017	0.0027	0.0055

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0468	0.0446	0.0531	0.0524	16.3026	10.7263	6.9614	3.5936
A0	→	Y	↓	0.0246	0.0242	0.0171	0.0164	7.3999	5.1599	2.1825	1.0846
A1	→	Y	↑	0.0539	0.0501	0.0610	0.0610	16.0661	10.6454	6.9067	3.5605
A1	→	Y	↓	0.0273	0.0264	0.0190	0.0182	7.4088	5.1619	2.1830	1.0847
B0	→	Y	↑	0.0840	0.0739	0.0802	0.0782	16.3114	10.7604	6.9986	3.5963
B0	→	Y	↓	0.0392	0.0372	0.0245	0.0234	7.3363	5.0958	2.1520	1.0729
B1	→	Y	↑	0.0878	0.0780	0.0868	0.0861	15.9723	10.5898	6.8937	3.5607
B1	→	Y	↓	0.0406	0.0386	0.0258	0.0249	7.3350	5.0954	2.1519	1.0729
C0	→	Y	↑	0.0943	0.0834	0.0891	0.0894	16.0862	10.6839	6.9150	3.6070
C0	→	Y	↓	0.0477	0.0459	0.0289	0.0274	7.6339	5.2745	2.2229	1.1044
C1	→	Y	↑	0.0998	0.0884	0.0972	0.0969	16.0773	10.6406	6.9047	3.5486
C1	→	Y	↓	0.0491	0.0475	0.0304	0.0292	7.6366	5.2740	2.2228	1.1045

Cell Description

The AOI2B1 cell provides the logical inverted
OR of one AND group and an additional input.
The output (Y) is represented by the logic
equation:

$$Y = \overline{(A0 \bullet \overline{A1N}) + B0}$$

Logic Symbol
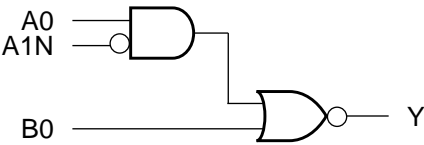
Function Table

A0	A1N	B0	Y
0	x	0	1
x	1	0	1
x	x	1	0
1	0	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI2B1XLAD	2.52	1.96
AOI2B1X1AD	2.52	1.96
AOI2B1X2AD	2.52	2.24
AOI2B1X4AD	2.52	3.36

Functional Schematic
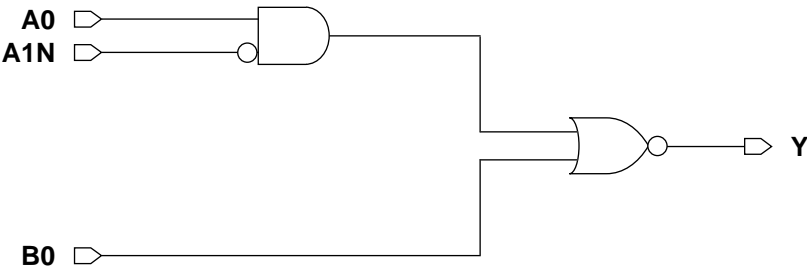
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0022	0.0030	0.0047	0.0095
A1N	0.0027	0.0033	0.0057	0.0119
B0	0.0019	0.0025	0.0045	0.0092

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0017	0.0028	0.0056
A1N	0.0011	0.0011	0.0014	0.0023
B0	0.0014	0.0018	0.0029	0.0054

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0317	0.0282	0.0298	0.0304	11.1242	7.1688	4.6700	2.3797
A0	→	Y	↓	0.0235	0.0232	0.0165	0.0166	7.3574	5.1431	2.1734	1.1014
A1N	→	Y	↑	0.0481	0.0468	0.0522	0.0542	10.9068	7.1698	4.6061	2.4163
A1N	→	Y	↓	0.0565	0.0597	0.0488	0.0475	7.3752	5.1567	2.1817	1.1050
B0	→	Y	↑	0.0258	0.0230	0.0260	0.0266	10.9859	7.1972	4.6226	2.4239
B0	→	Y	↓	0.0122	0.0117	0.0095	0.0093	4.2112	2.9402	1.2561	0.6285

Cell Description

The AOI2BB1 cell provides the logical inverted OR of one AND group of two inverted inputs (A0N,A1N) and an additional non-inverted input (B0). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} \bullet \overline{A1N}) + B0}$$

Logic Symbol
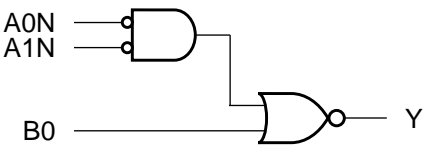
Function Table

A0N	A1N	B0	Y
1	x	0	1
x	1	0	1
x	x	1	0
0	0	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI2BB1XLAD	2.52	1.68
AOI2BB1X1AD	2.52	1.68
AOI2BB1X2AD	2.52	1.68
AOI2BB1X4AD	2.52	2.52

Functional Schematic
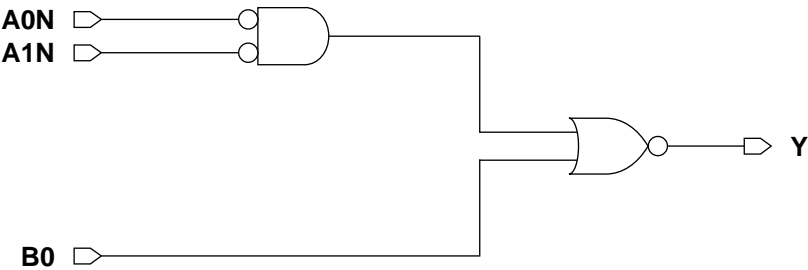
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0N	0.0029	0.0035	0.0051	0.0091
A1N	0.0033	0.0038	0.0055	0.0100
B0	0.0018	0.0025	0.0041	0.0085

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0N	0.0012	0.0012	0.0015	0.0026
A1N	0.0013	0.0013	0.0015	0.0025
B0	0.0012	0.0016	0.0027	0.0056

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0N	→ Y	↑	0.0396	0.0387	0.0407	0.0380	11.3306	7.2055	4.6340	2.3900
A0N	→ Y	↓	0.0601	0.0673	0.0643	0.0586	4.6658	3.2091	1.3881	0.6793
A1N	→ Y	↑	0.0412	0.0405	0.0424	0.0398	11.3410	7.2058	4.6359	2.3895
A1N	→ Y	↓	0.0650	0.0724	0.0690	0.0633	4.6652	3.2088	1.3880	0.6794
B0	→ Y	↑	0.0259	0.0238	0.0255	0.0259	11.2924	7.1856	4.6275	2.3865
B0	→ Y	↓	0.0128	0.0129	0.0103	0.0101	4.1554	2.9334	1.2543	0.6215

Cell Description

The AOI2BB2 cell provides the logical inverted OR of one AND group of two inverted inputs (A0N,A1N) and one AND group of two non-inverted inputs (B0,B1). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} \bullet \overline{A1N}) + (B0 \bullet B1)}$$

Logic Symbol
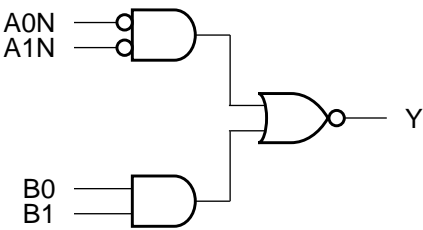
Function Table

A0N	A1N	B0	B1	Y
1	x	0	x	1
1	x	x	0	1
x	1	0	x	1
x	1	x	0	1
x	x	1	1	0
0	0	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI2BB2XLAD	2.52	2.24
AOI2BB2X1AD	2.52	2.24
AOI2BB2X2AD	2.52	2.24
AOI2BB2X4AD	2.52	3.64

Functional Schematic
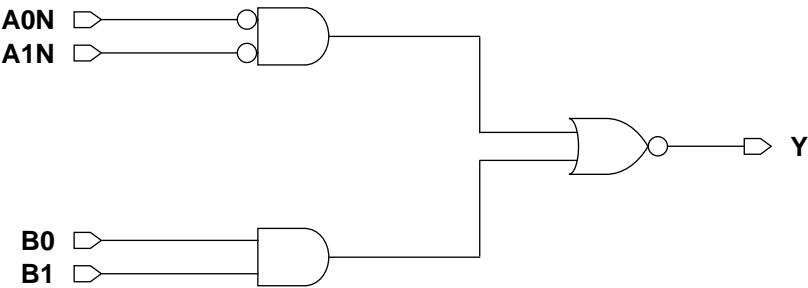
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0N	0.0031	0.0035	0.0051	0.0090
A1N	0.0033	0.0038	0.0055	0.0099
B0	0.0022	0.0030	0.0047	0.0093
B1	0.0025	0.0034	0.0057	0.0115

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0N	0.0014	0.0014	0.0017	0.0026
A1N	0.0011	0.0011	0.0014	0.0026
B0	0.0014	0.0017	0.0027	0.0053
B1	0.0013	0.0016	0.0027	0.0054

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0N	→	Y	↑	0.0445	0.0426	0.0460	0.0433	11.0512	7.1439	4.6437	2.3875
A0N	→	Y	↓	0.0617	0.0677	0.0645	0.0569	4.6162	3.1572	1.3812	0.6622
A1N	→	Y	↑	0.0463	0.0445	0.0483	0.0450	11.0623	7.1495	4.6463	2.3880
A1N	→	Y	↓	0.0641	0.0702	0.0675	0.0619	4.6148	3.1563	1.3808	0.6622
B0	→	Y	↑	0.0333	0.0301	0.0312	0.0307	11.2129	7.2202	4.7007	2.4172
B0	→	Y	↓	0.0239	0.0235	0.0165	0.0158	7.3955	5.1415	2.1860	1.0813
B1	→	Y	↑	0.0360	0.0326	0.0360	0.0362	10.9860	7.0729	4.6142	2.3776
B1	→	Y	↓	0.0248	0.0245	0.0178	0.0174	7.3935	5.1415	2.1854	1.0818

Cell Description

The AOI31 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1 \bullet A2) + B0}$$

Logic Symbol

A0
A1
A2

B0 ───────── Y
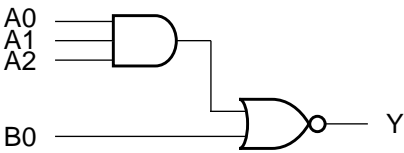
Function Table

A0	A1	A2	B0	Y
0	x	x	0	1
x	0	x	0	1
x	x	0	0	1
x	x	x	1	0
1	1	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI31XLAD	2.52	1.68
AOI31X1AD	2.52	1.68
AOI31X2AD	2.52	1.96
AOI31X4AD	2.52	3.36

Functional Schematic

A0

A1

A2

Y

B0
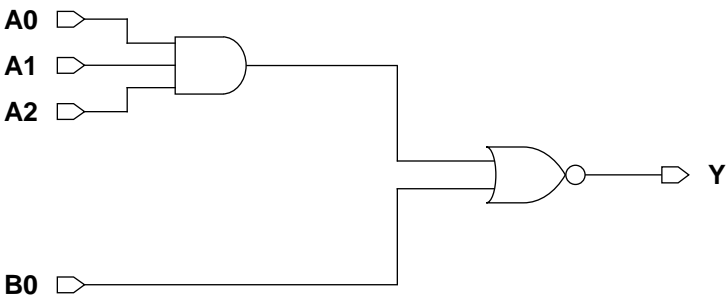
AC Power

Pin	Power (uW/MHz)			
	XL	X1	X2	X4
A0	0.0023	0.0032	0.0051	0.0105
A1	0.0026	0.0036	0.0061	0.0125
A2	0.0030	0.0041	0.0072	0.0144
B0	0.0022	0.0030	0.0056	0.0114

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0013	0.0017	0.0028	0.0058
A1	0.0013	0.0017	0.0027	0.0055
A2	0.0012	0.0016	0.0026	0.0050
B0	0.0013	0.0018	0.0029	0.0054

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	X1	X2	X4	XL	X1	X2	X4
A0	→ Y	↑	0.0333	0.0303	0.0327	0.0333	11.2155	7.2256	4.7093	2.3919
A0	→ Y	↓	0.0329	0.0330	0.0226	0.0229	10.2520	7.1556	2.9746	1.5042
A1	→ Y	↑	0.0375	0.0348	0.0383	0.0398	11.2228	7.3768	4.7156	2.4248
A1	→ Y	↓	0.0364	0.0365	0.0258	0.0261	10.2551	7.1570	2.9753	1.5047
A2	→ Y	↑	0.0398	0.0371	0.0427	0.0449	10.9545	7.1927	4.6247	2.4467
A2	→ Y	↓	0.0377	0.0380	0.0275	0.0273	10.2560	7.1566	2.9756	1.5047
B0	→ Y	↑	0.0286	0.0256	0.0316	0.0328	11.1275	7.3310	4.6735	2.4531
B0	→ Y	↓	0.0119	0.0116	0.0096	0.0093	4.2440	2.9539	1.2577	0.6185

Cell Description

The AOI32 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1 \bullet A2) + (B0 \bullet B1)}$$

Logic Symbol
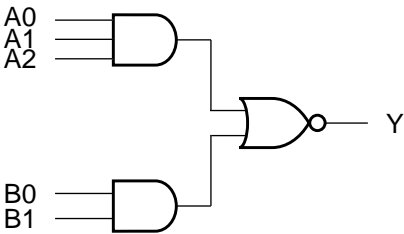
## Function Table

A0	A1	A2	B0	B1	Y
0	x	x	0	x	1
0	x	x	x	0	1
x	0	x	0	x	1
x	0	x	x	0	1
x	x	0	0	x	1
x	x	0	x	0	1
x	x	x	1	1	0
1	1	1	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI32XLAD	2.52	1.96
AOI32X1AD	2.52	2.24
AOI32X2AD	2.52	2.24
AOI32X4AD	2.52	4.20

Functional Schematic
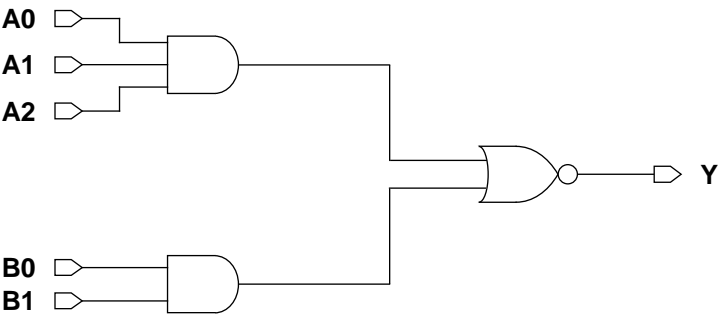
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0029	0.0042	0.0068	0.0136
A1	0.0032	0.0046	0.0078	0.0158
A2	0.0035	0.0051	0.0088	0.0179
B0	0.0025	0.0034	0.0061	0.0122
B1	0.0028	0.0038	0.0070	0.0142

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0017	0.0027	0.0051
A1	0.0013	0.0017	0.0026	0.0056
A2	0.0012	0.0016	0.0026	0.0056
B0	0.0013	0.0018	0.0028	0.0054
B1	0.0014	0.0019	0.0028	0.0057

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0475	0.0421	0.0445	0.0458	11.2648	7.4313	4.7771	2.4635
A0	→	Y	↓	0.0476	0.0454	0.0292	0.0288	10.2182	7.0750	2.9969	1.4793
A1	→	Y	↑	0.0508	0.0456	0.0502	0.0522	11.2031	7.4189	4.7598	2.4430
A1	→	Y	↓	0.0505	0.0488	0.0327	0.0327	10.2133	7.0724	2.9962	1.4793
A2	→	Y	↑	0.0529	0.0479	0.0543	0.0569	10.9477	7.2640	4.6643	2.4160
A2	→	Y	↓	0.0521	0.0504	0.0343	0.0345	10.2159	7.0739	2.9970	1.4792
B0	→	Y	↑	0.0317	0.0299	0.0348	0.0365	11.2428	7.4403	4.7728	2.4517
B0	→	Y	↓	0.0199	0.0199	0.0145	0.0143	7.4257	5.1813	2.1970	1.0810
B1	→	Y	↑	0.0362	0.0335	0.0403	0.0421	10.9872	7.2858	4.7066	2.4172
B1	→	Y	↓	0.0226	0.0222	0.0164	0.0161	7.4361	5.1841	2.1976	1.0812

Cell Description

The AOI33 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1 \bullet A2) + (B0 \bullet B1 \bullet B2)}$$

Logic Symbol
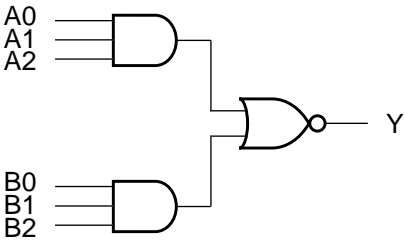
Function Table

A0	A1	A2	B0	B1	B2	Y
0	x	x	0	x	x	1
0	x	x	x	0	x	1
0	x	x	x	x	0	1
x	0	x	0	x	x	1
x	0	x	x	0	x	1
x	0	x	x	x	0	1
x	x	0	0	x	x	1
x	x	0	x	0	x	1
x	x	0	x	x	0	1
x	x	x	1	1	1	0
1	1	1	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI33XLAD	2.52	2.52
AOI33X1AD	2.52	2.52
AOI33X2AD	2.52	2.52
AOI33X4AD	2.52	4.76

Functional Schematic
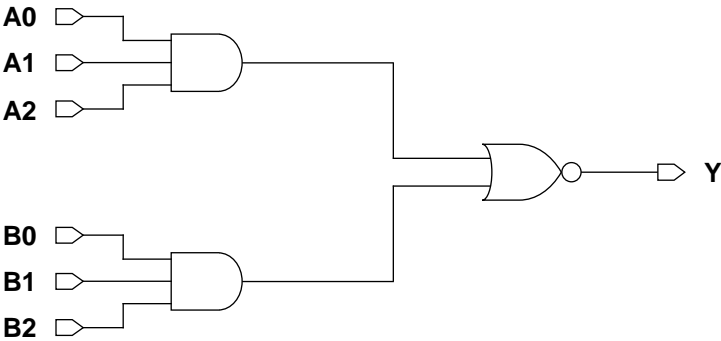
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0028	0.0038	0.0066	0.0131
A1	0.0031	0.0042	0.0076	0.0152
A2	0.0035	0.0047	0.0086	0.0173
B0	0.0039	0.0053	0.0087	0.0173
B1	0.0041	0.0057	0.0096	0.0193
B2	0.0045	0.0061	0.0106	0.0215

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0014	0.0018	0.0029	0.0052
A1	0.0014	0.0018	0.0028	0.0057
A2	0.0014	0.0018	0.0029	0.0059
B0	0.0013	0.0017	0.0027	0.0051
B1	0.0013	0.0017	0.0027	0.0055
B2	0.0012	0.0016	0.0026	0.0056

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→ Y	↑	0.0393	0.0346	0.0400	0.0393	11.5081	7.4431	4.8051	2.4506
A0	→ Y	↓	0.0309	0.0299	0.0211	0.0197	9.8970	6.9194	3.0032	1.4867
A1	→ Y	↑	0.0441	0.0388	0.0459	0.0462	11.4592	7.4214	4.7841	2.4427
A1	→ Y	↓	0.0352	0.0339	0.0248	0.0236	9.9002	6.9201	3.0032	1.4870
A2	→ Y	↑	0.0484	0.0422	0.0509	0.0518	11.2859	7.3097	4.7102	2.4196
A2	→ Y	↓	0.0380	0.0364	0.0269	0.0256	9.9075	6.9226	3.0038	1.4873
B0	→ Y	↑	0.0597	0.0533	0.0571	0.0581	11.5268	7.4573	4.8118	2.4613
B0	→ Y	↓	0.0572	0.0569	0.0364	0.0356	10.1111	7.0654	2.9885	1.4802
B1	→ Y	↑	0.0633	0.0569	0.0628	0.0645	11.4588	7.4166	4.7845	2.4470
B1	→ Y	↓	0.0605	0.0604	0.0399	0.0394	10.1094	7.0685	2.9882	1.4802
B2	→ Y	↑	0.0657	0.0589	0.0666	0.0693	11.2192	7.2521	4.6892	2.4160
B2	→ Y	↓	0.0621	0.0620	0.0416	0.0413	10.1112	7.0652	2.9883	1.4801

Cell Description

The booth encoder block, BENC, cell performs a 2bit multiplier recoding per a modified Booth's algorithm. Each BENC cell examines 3 bits of the multiplier (M0,M1,M2) and generates the appropriate control signals to adjust the multiplicand for subsequent partial product reduction. The outputs (S,A,X2) are represented by the logic equations:

$A = M2 + (\overline{M0} \bullet \overline{M1})$

$S = \overline{M2} + (M0 \bullet M1)$

$X2 = \overline{M1 \oplus M0}$

Logic Symbol
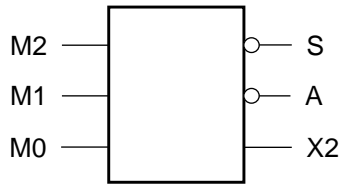
Function Table

M2	M1	M0	X2	A	S
0	0	0	1	1	1
0	0	1	0	0	1
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
BENCX1AD	2.52	11.20
BENCX2AD	2.52	14.00
BENCX4AD	2.52	21.84

Functional Schematic
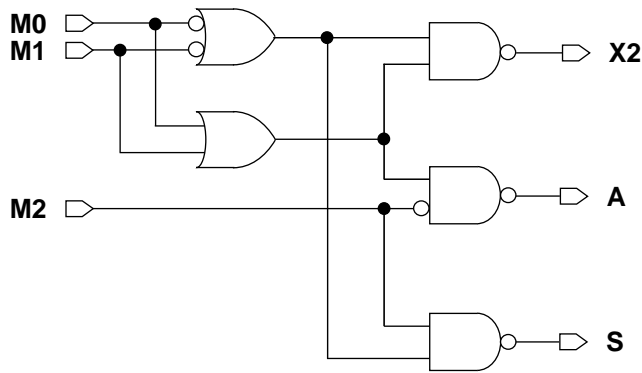
AC Power

Pin	Power (uW/MHz)		
	X1	**X2**	**X4**
M2	0.0196	0.0359	0.0690
M1	0.0206	0.0397	0.0751
M0	0.0214	0.0419	0.0782

Pin Capacitance

Pin	Capacitance (pF)		
	X1	**X2**	**X4**
M2	0.0033	0.0041	0.0059
M1	0.0044	0.0064	0.0109
M0	0.0040	0.0064	0.0094

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)			K_{load} (ns/pF)		
			X1	**X2**	**X4**	**X1**	**X2**	**X4**
M2	→	A ↑	0.1071	0.1050	0.1021	1.4040	0.6322	0.3235
M2	→	A ↓	0.1121	0.1041	0.1170	0.9323	0.3965	0.1998
M1	→	A ↑	0.1043	0.0965	0.0894	1.4029	0.6310	0.3232
M1	→	A ↓	0.0936	0.0801	0.0872	0.9329	0.3966	0.1999
M0	→	A ↑	0.1023	0.0935	0.0844	1.4021	0.6309	0.3230
M0	→	A ↓	0.0900	0.0759	0.0821	0.9307	0.3955	0.1995
M2	→	S ↑	0.0977	0.0887	0.0816	1.3993	0.6338	0.3232
M2	→	S ↓	0.0873	0.0714	0.0748	0.9327	0.3986	0.1988
M1	→	S ↑	0.1368	0.1217	0.1130	1.3985	0.6329	0.3231
M1	→	S ↓	0.1471	0.1260	0.1174	0.9361	0.4000	0.1994
M0	→	S ↑	0.1289	0.1064	0.0994	1.3977	0.6326	0.3230
M0	→	S ↓	0.1287	0.0999	0.1074	0.9329	0.3984	0.1993
M1	→	X2 ↑	0.0936	0.0865	0.0878	1.4005	0.6458	0.3301
M1	→	X2 ↓	0.1066	0.1006	0.0913	0.9271	0.3982	0.2057
M0	→	X2 ↑	0.1182	0.1039	0.0997	1.4002	0.6457	0.3301
M0	→	X2 ↓	0.1187	0.1059	0.1090	0.9268	0.3985	0.2062

Cell Description

The BMX cell performs the shifting and 2's complement inversion of the multiplicand bits (M1,M0) based on the recode control signals (X2,A,S) from the booth encoder block cell. The partial product output (PP) is represented by the logic equation:

$$PP = X2\bullet((M0\bullet\overline{A}) + (\overline{M0}\bullet\overline{S})) + \overline{X2}\bullet((M1\bullet\overline{A}) + (\overline{M1}\bullet\overline{S}))$$

Logic Symbol

Function Table

X2	A	S	M0	M1	PP
0	0	0	x	x	x
0	0	1	x	0	0
0	0	1	x	1	1
0	1	0	x	0	1
0	1	0	x	1	0
0	1	1	x	x	0
1	0	0	x	x	x
1	0	1	0	x	0
1	0	1	1	x	1
1	1	0	0	x	1
1	1	0	1	x	0
1	1	1	x	x	0
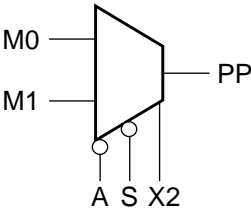
Cell Size

Drive Strength	Height (um)	Width (um)
BMXX2AD	2.52	7.56
BMXX4AD	2.52	9.80

Functional Schematic
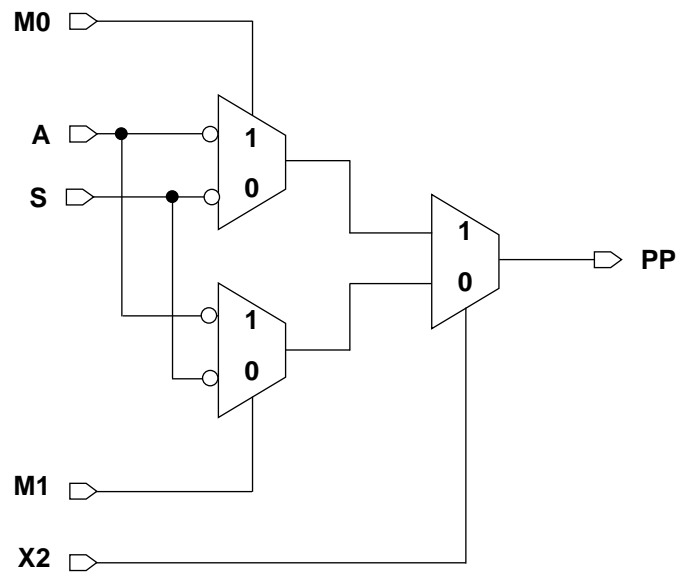
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
X2	0.0091	0.0173
M0	0.0139	0.0239
A	0.0185	0.0328
S	0.0167	0.0297
M1	0.0118	0.0214

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
X2	0.0023	0.0037
M0	0.0034	0.0037
A	0.0024	0.0048
S	0.0025	0.0047
M1	0.0028	0.0038

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
X2	$\rightarrow$	PP	$\uparrow$	0.0612	0.0593	2.3169	1.1911
X2	$\rightarrow$	PP	$\downarrow$	0.0534	0.0510	1.4079	0.6977
M0	$\rightarrow$	PP	$\uparrow$	0.0925	0.0866	2.3225	1.1921
M0	$\rightarrow$	PP	$\downarrow$	0.1102	0.1080	1.4110	0.6988
A	$\rightarrow$	PP	$\uparrow$	0.1116	0.0998	2.3241	1.1930
A	$\rightarrow$	PP	$\downarrow$	0.1000	0.0901	1.4121	0.6994
S	$\rightarrow$	PP	$\uparrow$	0.1065	0.0969	2.3242	1.1931
S	$\rightarrow$	PP	$\downarrow$	0.1009	0.0910	1.4126	0.6994
M1	$\rightarrow$	PP	$\uparrow$	0.0867	0.0866	2.3202	1.1927
M1	$\rightarrow$	PP	$\downarrow$	0.1026	0.1035	1.4117	0.6969

Cell Description

The BMXI cell performs the shifting and 2's complement inversion of the multiplicand bits (M1,M0) based on the recode control signals (X2,A,S) from the booth encoder block cell. The inverted partial product output (PPN) is represented by the logic equation:

$$PPN = \overline{X2\bullet((M0\bullet\overline{A}) + (\overline{M0}\bullet\overline{S})) + \overline{X2}\bullet((M1\bullet\overline{A}) + (\overline{M1}\bullet\overline{S}))}$$

Logic Symbol
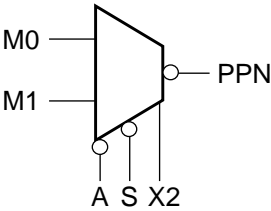
Function Table

X2	A	S	M0	M1	PPN
0	0	0	x	x	x
0	0	1	x	0	1
0	0	1	x	1	0
0	1	0	x	0	0
0	1	0	x	1	1
0	1	1	x	x	1
1	0	0	x	x	x
1	0	1	0	x	1
1	0	1	1	x	0
1	1	0	0	x	0
1	1	0	1	x	1
1	1	1	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
BMXIX2AD	2.52	6.72
BMXIX4AD	2.52	10.08

Functional Schematic
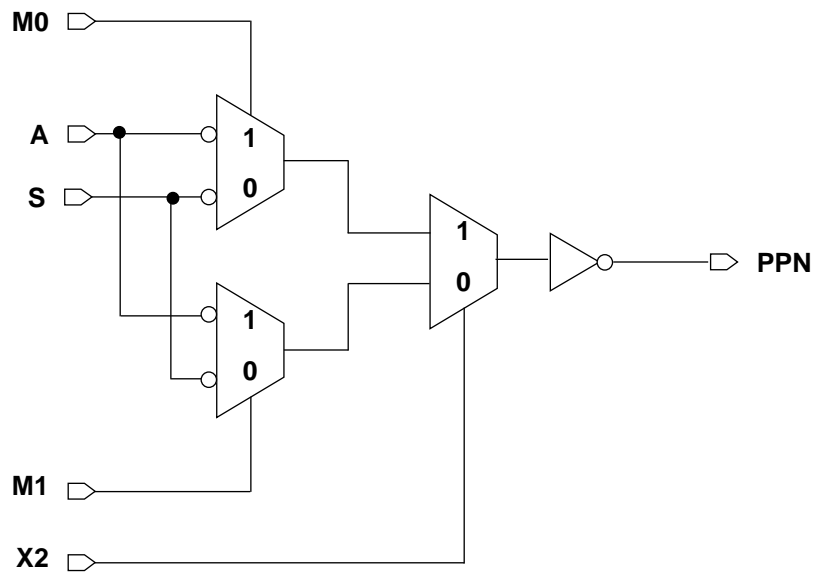
AC Power

Pin	Power (uW/MHz)	
	X2	X4
X2	0.0080	0.0150
M0	0.0111	0.0205
A	0.0169	0.0308
S	0.0146	0.0266
M1	0.0097	0.0182

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
X2	0.0032	0.0054
M0	0.0039	0.0062
A	0.0026	0.0052
S	0.0028	0.0052
M1	0.0033	0.0056

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	X4	X2	X4
X2	→	PPN	↑	0.0669	0.0682	2.3470	1.2054
X2	→	PPN	↓	0.0621	0.0648	1.5513	0.7698
M0	→	PPN	↑	0.0850	0.0846	2.3509	1.2069
M0	→	PPN	↓	0.0865	0.0840	1.5443	0.7719
A	→	PPN	↑	0.0731	0.0697	2.3514	1.2075
A	→	PPN	↓	0.1026	0.0947	1.5955	0.7836
S	→	PPN	↑	0.0757	0.0718	2.3527	1.2078
S	→	PPN	↓	0.0964	0.0889	1.5721	0.7840
M1	→	PPN	↑	0.0832	0.0837	2.3497	1.2067
M1	→	PPN	↓	0.0796	0.0772	1.5508	0.7740

Cell Description

The BUF cell provides the logical buffer of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Logic Symbol

A ───▷─── Y

Function Table

A	Y
0	0
1	1
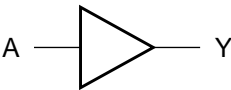
Cell Size

Drive Strength	Height (um)	Width (um)
BUFX2AD	2.52	1.12
BUFX3AD	2.52	1.40
BUFX4AD	2.52	1.68
BUFX5AD	2.52	1.96
BUFX6AD	2.52	2.24
BUFX8AD	2.52	2.52
BUFX10AD	2.52	3.08
BUFX12AD	2.52	3.64
BUFX14AD	2.52	4.20
BUFX16AD	2.52	4.48
BUFX18AD	2.52	5.04
BUFX20AD	2.52	5.60

Functional Schematic

A ▷──────▷o──────▷o──────▷ Y

AC Power

Pin	Power (uW/MHz)							
	X2	**X3**	**X4**	**X5**	**X6**	**X8**	**X10**	**X12**
A	0.0041	0.0059	0.0076	0.0099	0.0114	0.0147	0.0182	0.0221

AC Power (Cont'd.)

Pin	Power (uW/MHz)			
	X14	**X16**	**X18**	**X20**
A	0.0257	0.0290	0.0329	0.0362

Pin Capacitance

Pin	Capacitance (pF)							
	X2	**X3**	**X4**	**X5**	**X6**	**X8**	**X10**	**X12**
A	0.0014	0.0019	0.0024	0.0029	0.0037	0.0046	0.0055	0.0067

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)			
	X14	**X16**	**X18**	**X20**
A	0.0077	0.0083	0.0099	0.0108

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X2	**X3**	**X4**	**X5**	**X6**	**X8**	**X10**	**X12**
A → Y ↑	0.0291	0.0280	0.0273	0.0286	0.0268	0.0263	0.0261	0.0266
A → Y ↓	0.0405	0.0385	0.0376	0.0387	0.0370	0.0366	0.0363	0.0372

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)			
	X14	**X16**	**X18**	**X20**
A → Y ↑	0.0267	0.0270	0.0264	0.0260
A → Y ↓	0.0368	0.0384	0.0366	0.0368

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X2	**X3**	**X4**	**X5**	**X6**	**X8**	**X10**	**X12**
A → Y ↑	2.3102	1.5956	1.1931	0.9787	0.8068	0.6107	0.4961	0.4129
A → Y ↓	1.3198	0.8570	0.6412	0.5167	0.4296	0.3206	0.2559	0.2132

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)			
	X14	**X16**	**X18**	**X20**
A → Y ↑	0.3591	0.3150	0.2810	0.2534
A → Y ↓	0.1828	0.1600	0.1419	0.1275

Cell Description

The CLKAND2 cell provides the logical AND of two inputs (A,B). The output (Y) is represented by the logic equation:

$Y = A \bullet B$

Logic Symbol
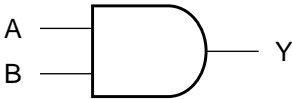
Function Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
CLKAND2X2AD	2.52	1.40
CLKAND2X3AD	2.52	1.68
CLKAND2X4AD	2.52	1.96
CLKAND2X6AD	2.52	2.24
CLKAND2X8AD	2.52	3.36
CLKAND2X12AD	2.52	4.20

Functional Schematic
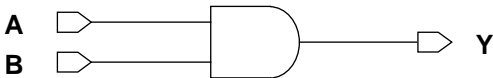
AC Power

Pin	Power (uW/MHz)					
	X2	**X3**	**X4**	**X6**	**X8**	**X12**
A	0.0036	0.0051	0.0064	0.0094	0.0123	0.0177
B	0.0040	0.0056	0.0070	0.0102	0.0134	0.0194

Pin Capacitance

Pin	Capacitance (pF)					
	X2	**X3**	**X4**	**X6**	**X8**	**X12**
A	0.0013	0.0017	0.0020	0.0027	0.0039	0.0052
B	0.0014	0.0018	0.0021	0.0028	0.0041	0.0054

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)					
				X2	**X3**	**X4**	**X6**	**X8**	**X12**
A	→	Y	↑	0.0465	0.0479	0.0455	0.0441	0.0472	0.0422
A	→	Y	↓	0.0430	0.0423	0.0399	0.0438	0.0407	0.0439
B	→	Y	↑	0.0475	0.0498	0.0475	0.0458	0.0489	0.0439
B	→	Y	↓	0.0464	0.0466	0.0433	0.0478	0.0422	0.0461

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)					
				X2	**X3**	**X4**	**X6**	**X8**	**X12**
A	→	Y	↑	2.3398	1.6106	1.2130	0.8230	0.6260	0.4194
A	→	Y	↓	2.6349	1.7968	1.2940	0.8612	0.6423	0.4276
B	→	Y	↑	2.3401	1.6109	1.2134	0.8229	0.6262	0.4193
B	→	Y	↓	2.6396	1.8004	1.2959	0.8632	0.6422	0.4278

Cell Description

The CLKBUF cell provides the logical buffer of a single input (A), with balanced delays for clock signals. The output (Y) is represented by the logic equation:

$Y = A$

Logic Symbol

A ▷ Y

Function Table

A	Y
0	0
1	1
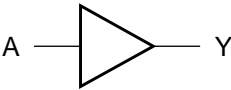
Cell Size

Drive Strength	Height (um)	Width (um)
CLKBUFX1AD	2.52	1.12
CLKBUFX2AD	2.52	1.12
CLKBUFX3AD	2.52	1.40
CLKBUFX4AD	2.52	1.40
CLKBUFX6AD	2.52	1.96
CLKBUFX8AD	2.52	2.52
CLKBUFX12AD	2.52	3.36
CLKBUFX16AD	2.52	3.92
CLKBUFX20AD	2.52	5.04
CLKBUFX24AD	2.52	5.60
CLKBUFX32AD	2.52	6.72
CLKBUFX40AD	2.52	8.12

Functional Schematic

A ▷ ▷o ▷o ▷ **Y**

AC Power

Pin	Power (uW/MHz)							
	X1	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**
A	0.0031	0.0038	0.0046	0.0056	0.0082	0.0106	0.0154	0.0202

AC Power (Cont'd.)

Pin	Power (uW/MHz)			
	X20	**X24**	**X32**	**X40**
A	0.0257	0.0307	0.0404	0.0506

Pin Capacitance

Pin	Capacitance (pF)							
	X1	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**
A	0.0017	0.0017	0.0016	0.0017	0.0022	0.0031	0.0042	0.0054

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)			
	X20	**X24**	**X32**	**X40**
A	0.0068	0.0081	0.0102	0.0128

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X1	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**
A → Y ↑	0.0301	0.0319	0.0376	0.0405	0.0403	0.0396	0.0386	0.0376
A → Y ↓	0.0308	0.0333	0.0381	0.0422	0.0410	0.0401	0.0394	0.0388

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)			
	X20	**X24**	**X32**	**X40**
A → Y ↑	0.0383	0.0377	0.0374	0.0376
A → Y ↓	0.0396	0.0396	0.0393	0.0394

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X1	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**
A → Y ↑	3.8755	2.3206	1.6003	1.1938	0.8119	0.6181	0.4147	0.3088
A → Y ↓	4.2374	2.6284	1.7107	1.3086	0.8812	0.6468	0.4362	0.3267

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)			
	X20	**X24**	**X32**	**X40**
A → Y ↑	0.2523	0.2035	0.1533	0.1230
A → Y ↓	0.2583	0.2167	0.1625	0.1294

Cell Description

The CLKINV cell provides the logical inversion of a single input (A), with balanced delays for clock signals. The output (Y) is represented by the logic equation:

$Y = \overline{A}$

Logic Symbol

A —▷o— Y

Function Table

A	Y
0	1
1	0
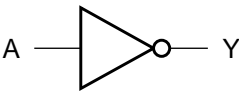
Cell Size

Drive Strength	Height (um)	Width (um)
CLKINVX1AD	2.52	0.84
CLKINVX2AD	2.52	0.84
CLKINVX3AD	2.52	1.12
CLKINVX4AD	2.52	1.12
CLKINVX6AD	2.52	1.68
CLKINVX8AD	2.52	1.96
CLKINVX12AD	2.52	2.52
CLKINVX16AD	2.52	3.36
CLKINVX20AD	2.52	3.64
CLKINVX24AD	2.52	4.48
CLKINVX32AD	2.52	5.60
CLKINVX40AD	2.52	7.00

Functional Schematic

A ▷———▷o———▷ Y
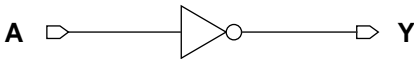
AC Power

Pin	Power (uW/MHz)							
	X1	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**
A	0.0015	0.0022	0.0031	0.0040	0.0059	0.0081	0.0118	0.0161

AC Power (Cont'd.)

Pin	Power (uW/MHz)			
	X20	**X24**	**X32**	**X40**
A	0.0200	0.0243	0.0322	0.0401

Pin Capacitance

Pin	Capacitance (pF)							
	X1	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**
A	0.0015	0.0023	0.0033	0.0043	0.0063	0.0085	0.0124	0.0169

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)			
	X20	**X24**	**X32**	**X40**
A	0.0207	0.0250	0.0330	0.0414

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X1	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**
A → Y ↑	0.0107	0.0102	0.0096	0.0095	0.0096	0.0097	0.0099	0.0100
A → Y ↓	0.0118	0.0115	0.0107	0.0103	0.0105	0.0105	0.0106	0.0106

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)			
	X20	**X24**	**X32**	**X40**
A → Y ↑	0.0100	0.0105	0.0110	0.0112
A → Y ↓	0.0106	0.0110	0.0116	0.0117

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X1	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**
A → Y ↑	3.7578	2.2808	1.5619	1.1681	0.7934	0.6007	0.4065	0.3075
A → Y ↓	4.2911	2.6591	1.7895	1.3010	0.8770	0.6555	0.4354	0.3257

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)			
	X20	**X24**	**X32**	**X40**
A → Y ↑	0.2420	0.2043	0.1531	0.1238
A → Y ↓	0.2573	0.2156	0.1610	0.1285

Cell Description

The CLKMX2 cell is a non-inverting 2 to 1 multiplexer with balanced delays for clock signals. The state of the select input (S0) determines which data input (A,B) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (S0 \bullet B) + (\overline{S0} \bullet A)$$

Logic Symbol

A — [MUX] — Y
B —
S0
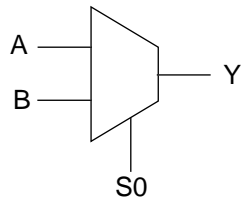
Function Table

S0	A	B	Y
0	0	x	0
0	1	x	1
1	x	0	0
1	x	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
CLKMX2X2AD	2.52	2.80
CLKMX2X3AD	2.52	3.36
CLKMX2X4AD	2.52	3.36
CLKMX2X6AD	2.52	3.92
CLKMX2X8AD	2.52	4.20
CLKMX2X12AD	2.52	5.04

Functional Schematic
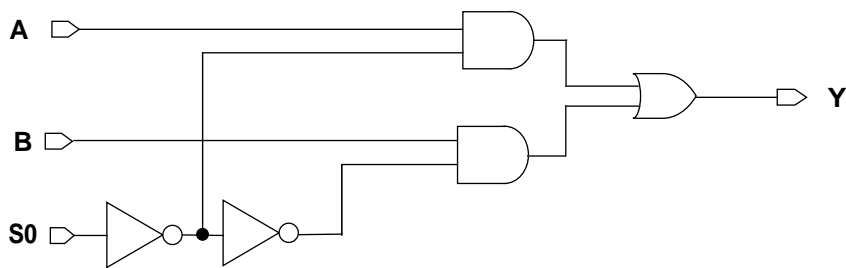
AC Power

Pin	Power (uW/MHz)					
	X2	**X3**	**X4**	**X6**	**X8**	**X12**
S0	0.0073	0.0094	0.0105	0.0131	0.0163	0.0233
B	0.0067	0.0084	0.0096	0.0124	0.0157	0.0232
A	0.0061	0.0075	0.0086	0.0115	0.0148	0.0223

Pin Capacitance

Pin	Capacitance (pF)					
	X2	**X3**	**X4**	**X6**	**X8**	**X12**
S0	0.0037	0.0042	0.0042	0.0042	0.0042	0.0041
B	0.0019	0.0022	0.0022	0.0022	0.0022	0.0022
A	0.0020	0.0023	0.0023	0.0023	0.0023	0.0023

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			X2	**X3**	**X4**	**X6**	**X8**	**X12**
S0	→ Y	↑	0.0557	0.0585	0.0614	0.0692	0.0768	0.0886
S0	→ Y	↓	0.0596	0.0628	0.0667	0.0752	0.0836	0.0995
B	→ Y	↑	0.0529	0.0544	0.0580	0.0666	0.0751	0.0886
B	→ Y	↓	0.0569	0.0601	0.0645	0.0742	0.0836	0.1003
A	→ Y	↑	0.0541	0.0555	0.0587	0.0674	0.0759	0.0891
A	→ Y	↓	0.0558	0.0580	0.0629	0.0730	0.0828	0.0999

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)					
			X2	**X3**	**X4**	**X6**	**X8**	**X12**
S0	→ Y	↑	2.3823	1.6546	1.2404	0.8454	0.6444	0.4428
S0	→ Y	↓	2.6667	1.8225	1.3765	0.9142	0.6859	0.4700
B	→ Y	↑	2.3840	1.6548	1.2410	0.8458	0.6447	0.4439
B	→ Y	↓	2.6666	1.8222	1.3764	0.9142	0.6859	0.4701
A	→ Y	↑	2.3814	1.6540	1.2405	0.8455	0.6447	0.4430
A	→ Y	↓	2.6642	1.8199	1.3758	0.9145	0.6864	0.4706

Cell Description

The CLKNAND2 cell provides the logical NAND of two inputs (A,B), with balanced delays for clock signals. The output (Y) is represented by the logic equation:

$Y = \overline{(A \bullet B)}$

Logic Symbol

A ───┐
     │ ╲
     │ ╲○── Y
B ───┘ ╱

Function Table

A	B	Y
0	x	1
x	0	1
1	1	0
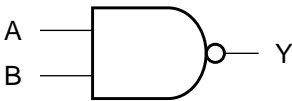
Cell Size

Drive Strength	Height (um)	Width (um)
CLKNAND2X2AD	2.52	1.12
CLKNAND2X4AD	2.52	1.96
CLKNAND2X8AD	2.52	3.36
CLKNAND2X12AD	2.52	4.76

Functional Schematic

A ▷───┐
          │ ╲
          │ ╲○───▷ **Y**
B ▷───┘ ╱

AC Power

Pin	Power (uW/MHz)			
	X2	**X4**	**X8**	**X12**
A	0.0027	0.0053	0.0108	0.0157
B	0.0034	0.0068	0.0136	0.0198

Pin Capacitance

Pin	Capacitance (pF)			
	X2	**X4**	**X8**	**X12**
A	0.0025	0.0047	0.0096	0.0141
B	0.0023	0.0050	0.0098	0.0143

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				X2	**X4**	**X8**	**X12**	**X2**	**X4**	**X8**	**X12**
A	→	Y	↑	0.0122	0.0125	0.0128	0.0126	2.3375	1.2223	0.6267	0.4220
A	→	Y	↓	0.0145	0.0148	0.0147	0.0146	3.0557	1.5708	0.7745	0.5258
B	→	Y	↑	0.0137	0.0142	0.0145	0.0144	2.3372	1.1815	0.6131	0.4150
B	→	Y	↓	0.0159	0.0166	0.0163	0.0163	3.0540	1.5717	0.7747	0.5260

Cell Description

The CLKXOR2 cell provides a logical
EXCLUSIVE OR of two inputs (A,B) with
balanced delays for clock signals. The output
(Y) is represented by the logic equation:

$$Y = (A \bullet \overline{B}) + (\overline{A} \bullet B)$$

Logic Symbol

Function Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0
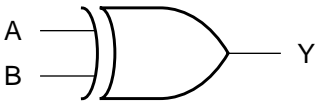
Cell Size

Drive Strength	Height (um)	Width (um)
CLKXOR2X1AD	2.52	2.80
CLKXOR2X2AD	2.52	2.80
CLKXOR2X4AD	2.52	4.20
CLKXOR2X8AD	2.52	6.72
CLKXOR2X12AD	2.52	10.08

Functional Schematic
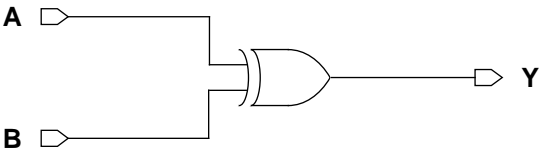
AC Power

Pin	Power (uW/MHz)				
	X1	**X2**	**X4**	**X8**	**X12**
A	0.0063	0.0069	0.0116	0.0220	0.0326
B	0.0068	0.0077	0.0145	0.0283	0.0433

Pin Capacitance

Pin	Capacitance (pF)				
	X1	**X2**	**X4**	**X8**	**X12**
A	0.0032	0.0032	0.0043	0.0072	0.0099
B	0.0017	0.0020	0.0037	0.0070	0.0106

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				
				X1	**X2**	**X4**	**X8**	**X12**
A	→	Y	↑	0.0565	0.0556	0.0568	0.0625	0.0652
A	→	Y	↓	0.0606	0.0642	0.0615	0.0684	0.0695
B	→	Y	↑	0.0802	0.0771	0.0739	0.0721	0.0726
B	→	Y	↓	0.0834	0.0837	0.0766	0.0784	0.0788

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)				
				X1	**X2**	**X4**	**X8**	**X12**
A	→	Y	↑	4.0050	2.3909	1.2134	0.6281	0.4148
A	→	Y	↓	4.3534	2.6924	1.3094	0.6573	0.4474
B	→	Y	↑	3.9852	2.3918	1.2148	0.6300	0.4162
B	→	Y	↓	4.3510	2.6915	1.3091	0.6572	0.4473

Cell Description

The CMPR42 cell takes in 4 bits of the partial product (A,B,C,D) and compresses them into 2-bits of partial product (S,CO). The cell requires an intermediate carry-in input (ICI) from the n-1 compressor and an intermediate carry-out output (CO) to the n+1 compressor. The CMPR42 cell also contains an internal sum IS. The internal sum IS, carry-in output (ICO), and the two outputs (S,CO) are represented by the logic equations:

$IS = A \oplus B \oplus C$

$ICO = (A \bullet B) + (A \bullet C) + (B \bullet C)$

$S = IS \oplus D \oplus ICI$

$CO = (IS \bullet D) + (IS \bullet ICI) + (D \bullet ICI)$

Logic Symbol
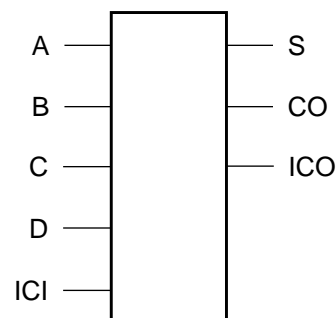
Cell Size

Drive Strength	Height (um)	Width (um)
CMPR42X1AD	2.52	12.88
CMPR42X2AD	2.52	12.88
CMPR42X4AD	2.52	18.48

Function Table

A	B	C	IS	ICO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Function Table (Cont'd.)

IS	D	ICI	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Functional Schematic
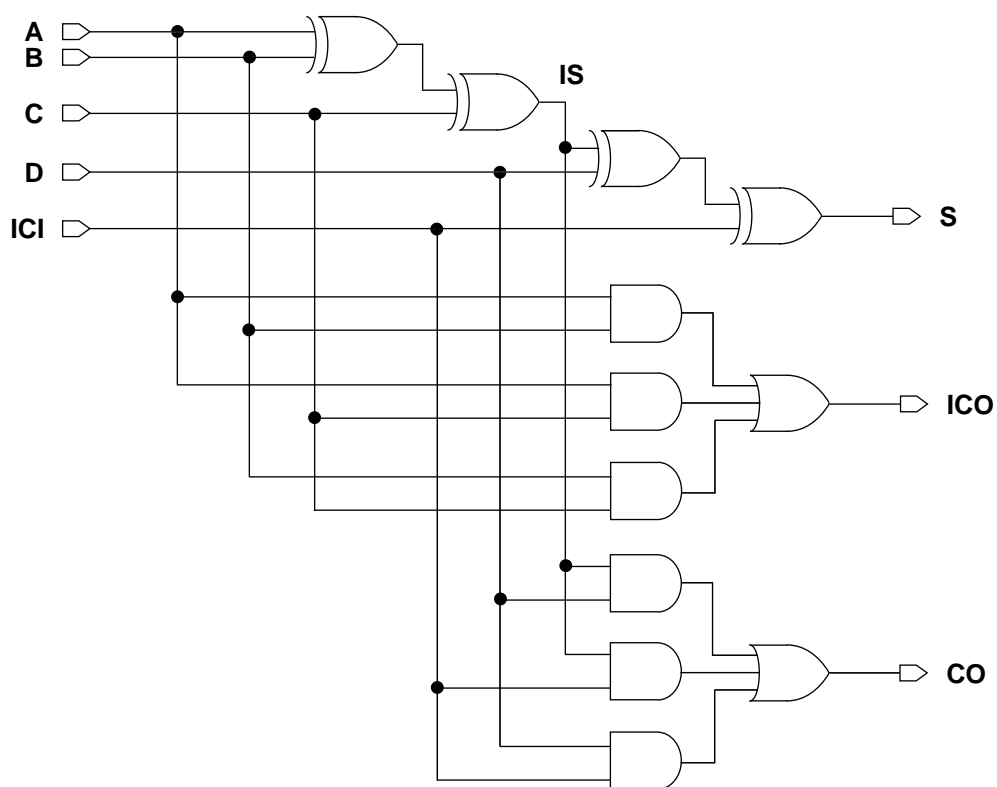
AC Power

Pin	Power (uW/MHz)		
	X1	**X2**	**X4**
A	0.0300	0.0409	0.0653
B	0.0294	0.0399	0.0638
C	0.0280	0.0376	0.0606
D	0.0229	0.0310	0.0544
ICI	0.0117	0.0163	0.0306

Pin Capacitance

Pin	Capacitance (pF)		
	X1	**X2**	**X4**
A	0.0047	0.0065	0.0102
B	0.0055	0.0073	0.0114
C	0.0044	0.0054	0.0066
D	0.0029	0.0036	0.0038
ICI	0.0018	0.0023	0.0026

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)			K_{load} (ns/pF)		
				X1	**X2**	**X4**	**X1**	**X2**	**X4**
A	→	S	↑	0.2504	0.2501	0.2866	3.7800	2.4353	1.2188
A	→	S	↓	0.3057	0.2894	0.3218	3.2953	1.4225	0.6973
B	→	S	↑	0.2131	0.1984	0.2313	3.7795	2.4341	1.2172
B	→	S	↓	0.2684	0.2376	0.2671	3.2954	1.4227	0.6974
C	→	S	↑	0.1871	0.1923	0.2132	3.7788	2.4345	1.2181
C	→	S	↓	0.2429	0.2324	0.2503	3.2955	1.4227	0.6974
D	→	S	↑	0.1712	0.1603	0.1889	3.7201	2.4213	1.2157
D	→	S	↓	0.2058	0.1848	0.2135	3.2954	1.4223	0.6957
ICI	→	S	↑	0.0891	0.0832	0.1057	3.7482	2.4240	1.2111
ICI	→	S	↓	0.1059	0.0964	0.1072	3.3016	1.4254	0.6986
A	→	ICO	↑	0.0471	0.0421	0.0417	3.6825	2.3651	1.2086
A	→	ICO	↓	0.0880	0.0718	0.0743	3.2162	1.3868	0.6913
B	→	ICO	↑	0.0481	0.0428	0.0426	3.6844	2.3662	1.2092
B	→	ICO	↓	0.0832	0.0689	0.0679	3.2177	1.3875	0.7143
C	→	ICO	↑	0.0400	0.0375	0.0370	3.6612	2.3614	1.2049
C	→	ICO	↓	0.0686	0.0586	0.0646	3.2280	1.3990	0.6965
A	→	CO	↑	0.2392	0.2380	0.2826	3.5720	2.4823	1.2363
A	→	CO	↓	0.2835	0.2760	0.3213	3.1666	1.9315	0.7360
B	→	CO	↑	0.2080	0.2088	0.2525	3.5722	2.4823	1.2363
B	→	CO	↓	0.2525	0.2469	0.2912	3.1669	1.9315	0.7360
C	→	CO	↑	0.1908	0.1831	0.2263	3.5711	2.4818	1.2362
C	→	CO	↓	0.2087	0.1983	0.2417	3.1674	1.9319	0.7359

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description				Intrinsic Delay (ns)			K_{load} (ns/pF)		
				X1	X2	X4	X1	X2	X4
D	$\rightarrow$	CO	$\uparrow$	0.1567	0.1378	0.1622	3.5457	2.4662	1.2207
D	$\rightarrow$	CO	$\downarrow$	0.1513	0.1416	0.1740	3.1517	1.9189	0.7317
ICI	$\rightarrow$	CO	$\uparrow$	0.0481	0.0521	0.0631	3.5804	2.4853	1.2345
ICI	$\rightarrow$	CO	$\downarrow$	0.0703	0.0640	0.0859	3.2549	1.9655	0.7793

Cell Description

The DFF cell is a positive-edge triggered, static D-type flipflop.

Logic Symbol

```
        ┌──────────┐
 D ─────┤          ├───── Q
        │          │
 CK ───▷│        ○─├───── QN
        └──────────┘
```
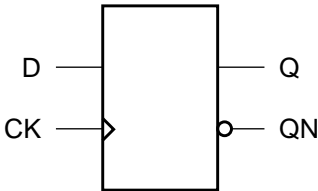
Function Table

D	CK	Q[n+1]	QN[n+1]
0	⎍	0	1
1	⎍	1	0
x	⎌	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFXLAD	2.52	6.16
DFFX1AD	2.52	6.16
DFFX2AD	2.52	6.16
DFFX4AD	2.52	7.84

Functional Schematic
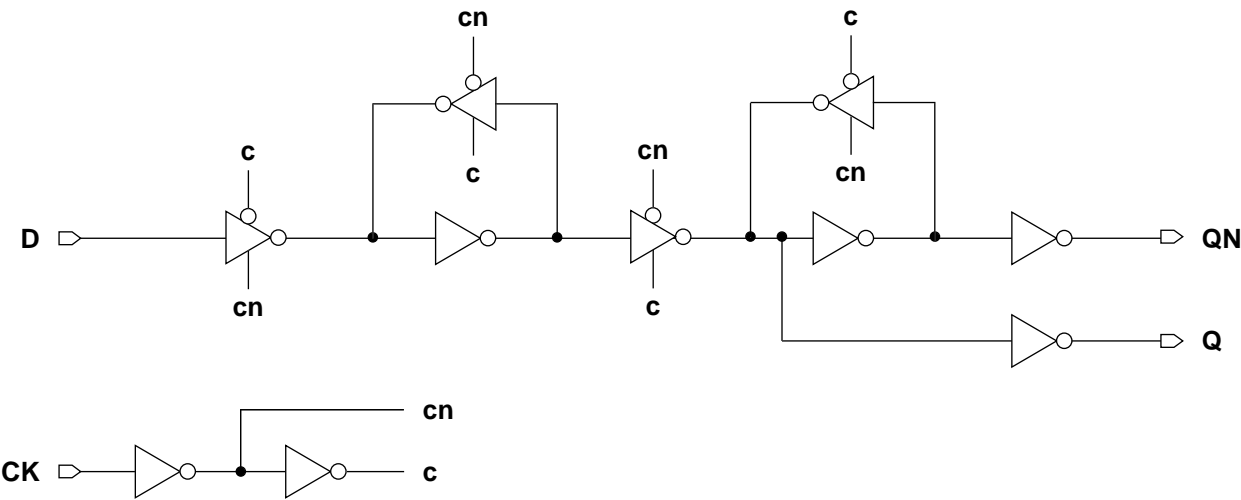
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0050	0.0051	0.0054	0.0067
CK	0.0103	0.0105	0.0110	0.0131
Q	0.0052	0.0062	0.0087	0.0154

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0011	0.0011	0.0011	0.0011
CK	0.0015	0.0015	0.0016	0.0018

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q ↑	0.1090	0.1060	0.1057	0.1042	5.8382	3.7181	2.3809	1.2240
CK	→	Q ↓	0.1205	0.1174	0.1052	0.1018	5.3376	3.4176	1.4590	0.7205
CK	→	QN ↑	0.1523	0.1488	0.1515	0.1501	5.6912	3.6608	2.3660	1.2114
CK	→	QN ↓	0.1498	0.1528	0.1603	0.1537	4.5376	3.1101	1.3818	0.6680

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	CK	0.0312	0.0352	0.0352	0.0391
	setup	↓	→	CK	0.0469	0.0469	0.0508	0.0625
	hold	↑	→	CK	-0.0195	-0.0234	-0.0195	-0.0234
	hold	↓	→	CK	-0.0078	-0.0078	-0.0078	-0.0117
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The DFFH cell is a positive-edge triggered,
static D-type flipflop and fast clock-to-Q-path.

Logic Symbol
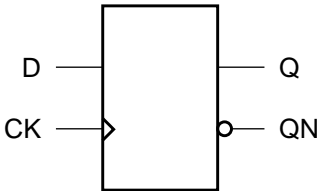
Function Table

D	CK	Q[n+1]	QN[n+1]
0	$\_\int$	0	1
1	$\_\int$	1	0
x	$\overline{}\_$	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFHX1AD	2.52	7.28
DFFHX2AD	2.52	7.56
DFFHX4AD	2.52	8.96
DFFHX8AD	2.52	14.28

Functional Schematic
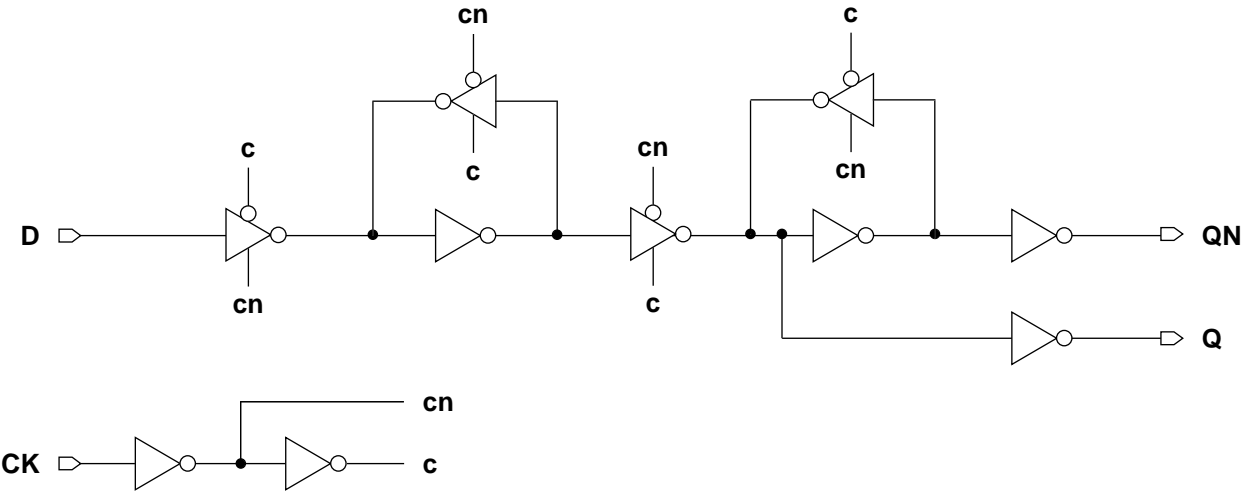
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
D	0.0071	0.0094	0.0131	0.0236
CK	0.0148	0.0190	0.0247	0.0466
Q	0.0052	0.0070	0.0095	0.0158

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
D	0.0012	0.0012	0.0016	0.0025
CK	0.0023	0.0025	0.0032	0.0054

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→ Q	↑	0.0742	0.0742	0.0669	0.0634	3.6477	2.3762	1.2041	0.6071
CK	→ Q	↓	0.0801	0.0796	0.0738	0.0665	3.1945	1.4176	0.7014	0.3285
CK	→ QN	↑	0.1056	0.1112	0.1101	0.1015	5.5881	5.5137	5.4381	5.4081
CK	→ QN	↓	0.1140	0.1168	0.1199	0.1186	4.3123	4.2316	4.2173	4.2091

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
D	setup	↑	→	CK	0.0469	0.0430	0.0391	0.0391
	setup	↓	→	CK	0.0508	0.0508	0.0508	0.0430
	hold	↑	→	CK	-0.0117	-0.0117	-0.0078	-0.0039
	hold	↓	→	CK	-0.0234	-0.0234	-0.0273	-0.0156
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The DFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop. The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol
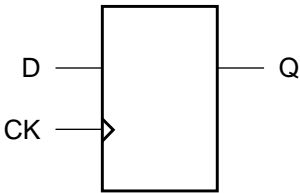
Function Table

D	CK	Q[n+1]
0	⌐⌐	0
1	⌐⌐	1
x	⌐⌐	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFHQX1AD	2.52	6.72
DFFHQX2AD	2.52	7.00
DFFHQX4AD	2.52	8.40
DFFHQX8AD	2.52	14.00

Functional Schematic
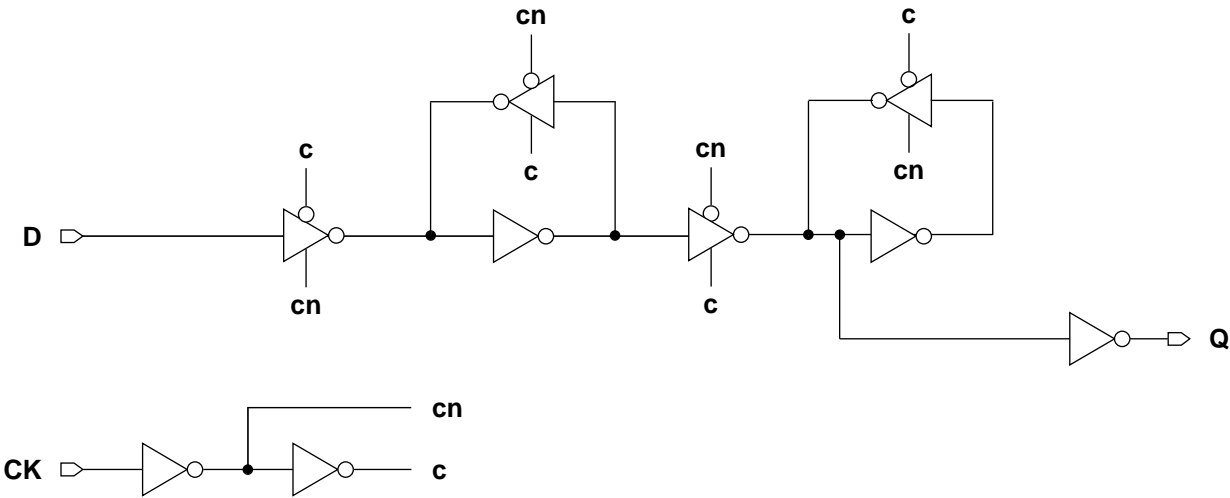
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
D	0.0070	0.0086	0.0135	0.0244
CK	0.0139	0.0173	0.0244	0.0465
Q	0.0038	0.0052	0.0084	0.0140

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
D	0.0016	0.0016	0.0021	0.0036
CK	0.0023	0.0024	0.0032	0.0054

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→ Q	↑	0.0764	0.0740	0.0671	0.0630	3.5531	2.3566	1.2056	0.6070
CK	→ Q	↓	0.0838	0.0774	0.0742	0.0662	3.2685	1.4310	0.7043	0.3292

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
D	setup	↑	→	CK	0.0547	0.0469	0.0430	0.0391
	setup	↓	→	CK	0.0391	0.0312	0.0352	0.0312
	hold	↑	→	CK	-0.0156	-0.0117	-0.0078	-0.0039
	hold	↓	→	CK	-0.0117	-0.0078	-0.0117	-0.0078
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The DFFNH cell is a negative-edge triggered, static D-type flip-flop and fast clock-to-Q-path.

Logic Symbol
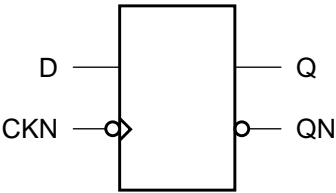
Function Table

D	CKN	Q[n+1]	QN[n+1]
0	⌐_	0	1
1	⌐_	1	0
x	_/	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFNHX1AD	2.52	7.00
DFFNHX2AD	2.52	7.00
DFFNHX4AD	2.52	9.24
DFFNHX8AD	2.52	13.72

Functional Schematic
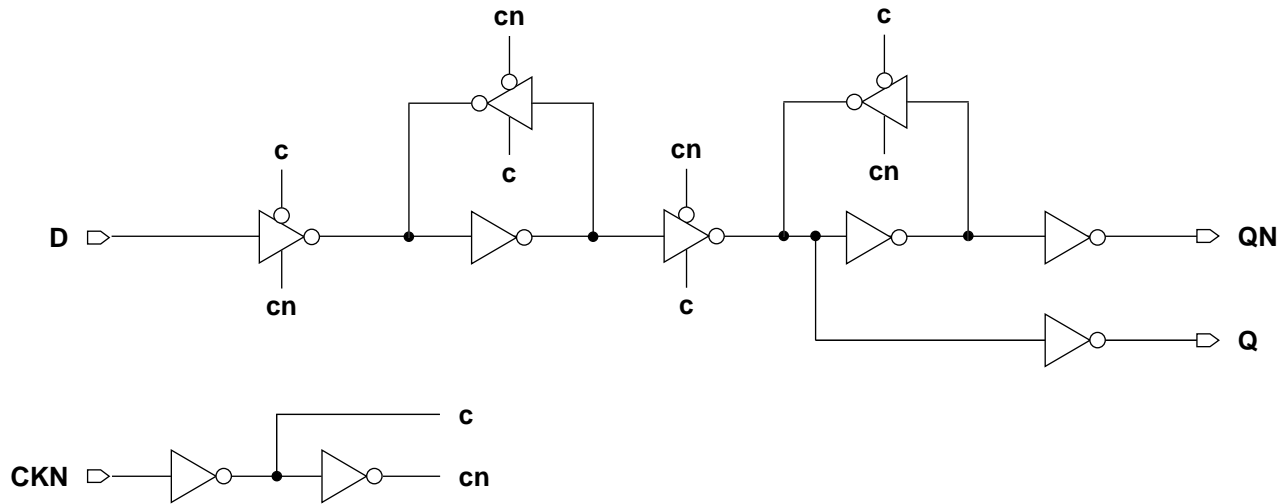
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
D	0.0069	0.0088	0.0135	0.0222
CKN	0.0113	0.0136	0.0200	0.0314
Q	0.0057	0.0072	0.0108	0.0183

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
D	0.0014	0.0018	0.0025	0.0046
CKN	0.0021	0.0022	0.0026	0.0042

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CKN	→	Q	↑	0.1476	0.1440	0.1437	0.1292	3.6408	2.3150	1.1842	0.6052
CKN	→	Q	↓	0.1290	0.1169	0.1126	0.0982	3.2760	1.3937	0.6737	0.3316
CKN	→	QN	↑	0.1574	0.1480	0.1487	0.1347	5.4432	5.4145	5.4506	5.4486
CKN	→	QN	↓	0.1895	0.1851	0.1978	0.1787	4.3450	4.2955	4.2183	4.2058

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
D	setup	↑	→	CKN	-0.0156	-0.0273	-0.0312	-0.0156
	setup	↓	→	CKN	0.0117	0.0039	0.0078	0.0195
	hold	↑	→	CKN	0.0469	0.0508	0.0508	0.0430
	hold	↓	→	CKN	0.0117	0.0156	0.0117	0.0078
CKN	minpwl				0.8332	0.8332	0.8332	0.8332
	minpwh				0.8332	0.8332	0.8332	0.8332

Cell Description

The DFFNSRH cell is a negative-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset, and fast clock-to-Q-path.

Logic Symbol
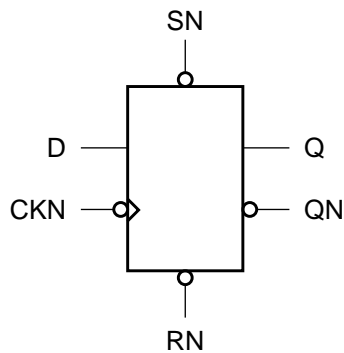
Function Table

RN	SN	D	CKN	Q[n+1]	QN[n+1]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0
1	1	0	⌐_	0	1
1	1	1	‾_	1	0
1	1	x	_/‾	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFNSRHX1AD	2.52	9.80
DFFNSRHX2AD	2.52	9.80
DFFNSRHX4AD	2.52	12.88
DFFNSRHX8AD	2.52	14.00

Functional Schematic
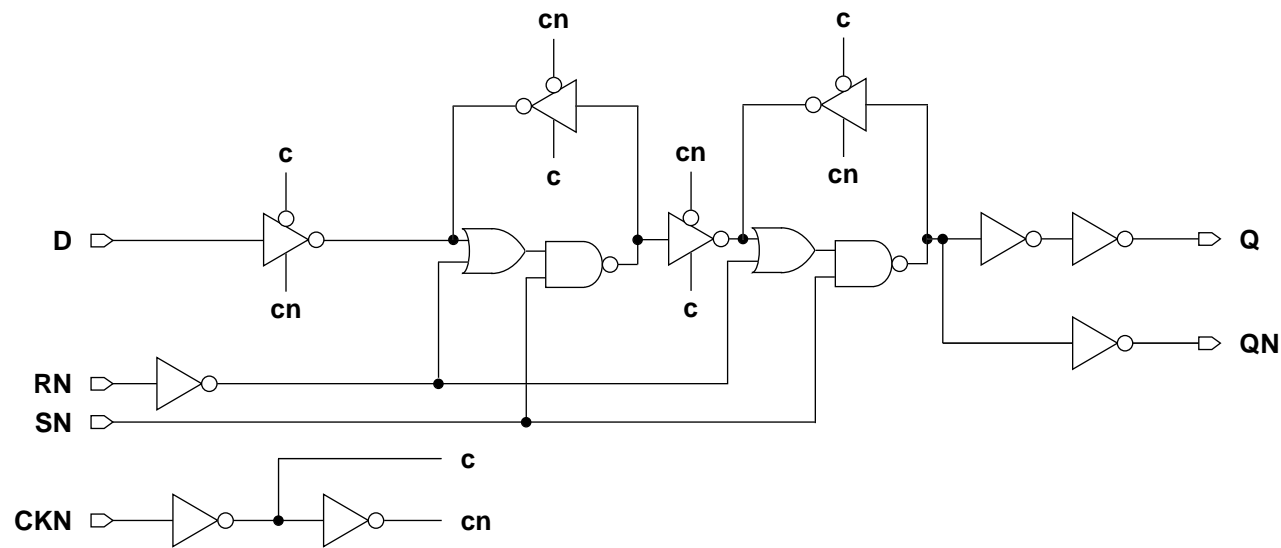
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
D	0.0079	0.0097	0.0158	0.0185
CKN	0.0122	0.0144	0.0223	0.0242
SN	0.0043	0.0046	0.0059	0.0071
RN	0.0015	0.0018	0.0029	0.0036
Q	0.0073	0.0088	0.0138	0.0205

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
D	0.0014	0.0017	0.0026	0.0045
CKN	0.0021	0.0023	0.0028	0.0041
SN	0.0022	0.0026	0.0035	0.0040
RN	0.0021	0.0024	0.0037	0.0040

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CKN	→	Q	↑	0.1678	0.1587	0.1618	0.1535	3.7533	2.4301	1.2057	0.6240
CKN	→	Q	↓	0.1410	0.1199	0.1174	0.1178	3.4125	1.4421	0.7012	0.3602
SN	→	Q	↑	0.1136	0.1349	0.1667	0.1177	3.6497	2.4261	1.2111	0.6181
SN	→	Q	↓	0.2046	0.1971	0.1723	0.1715	3.8908	1.7425	0.8487	0.4205
RN	→	Q	↓	0.1781	0.1656	0.1357	0.1425	3.9095	1.7441	0.8497	0.4206
CKN	→	QN	↑	0.1751	0.1577	0.1565	0.1623	5.4326	5.4346	5.4411	5.5887
CKN	→	QN	↓	0.2213	0.2118	0.2174	0.2129	4.4988	4.4194	4.3307	4.3821
SN	→	QN	↑	0.2439	0.2445	0.2197	0.2245	5.4630	5.4448	5.4438	5.5892
SN	→	QN	↓	0.1636	0.1877	0.2225	0.1761	4.4785	4.4133	4.3298	4.3817
RN	→	QN	↑	0.2178	0.2128	0.1829	0.1954	5.4632	5.4433	5.4430	5.5890

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
D	setup	↑	→	CKN	-0.0039	-0.0156	-0.0156	-0.0156
	setup	↓	→	CKN	0.0156	0.0117	0.0078	0.0195
	hold	↑	→	CKN	0.0508	0.0508	0.0508	0.0508
	hold	↓	→	CKN	0.0156	0.0156	0.0195	0.0117
CKN	minpwl				0.8332	0.8332	0.8332	0.8332
	minpwh				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0078	-0.0078	-0.0078	0.0039
	removal				0.0273	0.0273	0.0273	0.0156
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0898	-0.0859	-0.0898	-0.0742
	removal				0.1250	0.1328	0.1641	0.1406

Cell Description

The DFFQ cell is a positive-edge triggered, static D-type flip-flop. The cell has a single output (Q) .

Logic Symbol

D — | Q
CK —▷
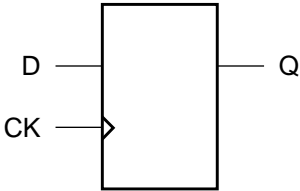
Function Table

D	CK	Q[n+1]
0	⌐	0
1	⌐	1
x	⌐	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFQXLAD	2.52	5.32
DFFQX1AD	2.52	5.60
DFFQX2AD	2.52	5.60
DFFQX4AD	2.52	7.00

Functional Schematic
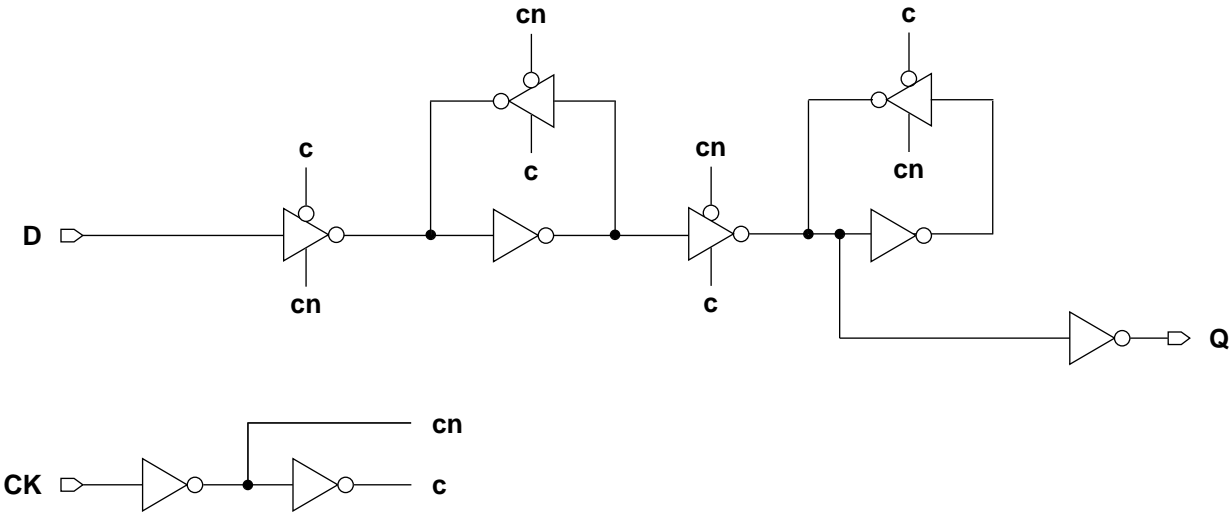
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0046	0.0047	0.0049	0.0063
CK	0.0098	0.0099	0.0101	0.0127
Q	0.0040	0.0046	0.0058	0.0097

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0011	0.0011	0.0011	0.0011
CK	0.0017	0.0017	0.0016	0.0017

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→ Q	↑	0.1039	0.1016	0.1014	0.1074	5.7059	3.6257	2.3146	1.1857
CK	→ Q	↓	0.1238	0.1210	0.1061	0.1027	5.3877	3.4654	1.4806	0.7205

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	CK	0.0312	0.0312	0.0312	0.0391
	setup	↓	→	CK	0.0469	0.0469	0.0469	0.0586
	hold	↑	→	CK	-0.0156	-0.0195	-0.0156	-0.0234
	hold	↓	→	CK	-0.0117	-0.0117	-0.0117	-0.0078
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The DFFR cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN).

Logic Symbol
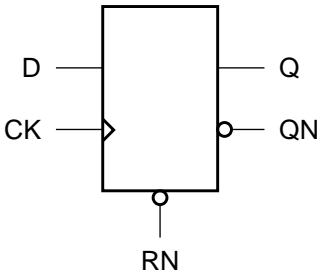
Function Table

RN	D	CK	Q[n+1]	QN[n+1]
0	x	x	0	1
1	0	⌐	0	1
1	1	⌐	1	0
1	x	⌐	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFRXLAD	2.52	6.72
DFFRX1AD	2.52	6.72
DFFRX2AD	2.52	7.00
DFFRX4AD	2.52	7.84

Functional Schematic
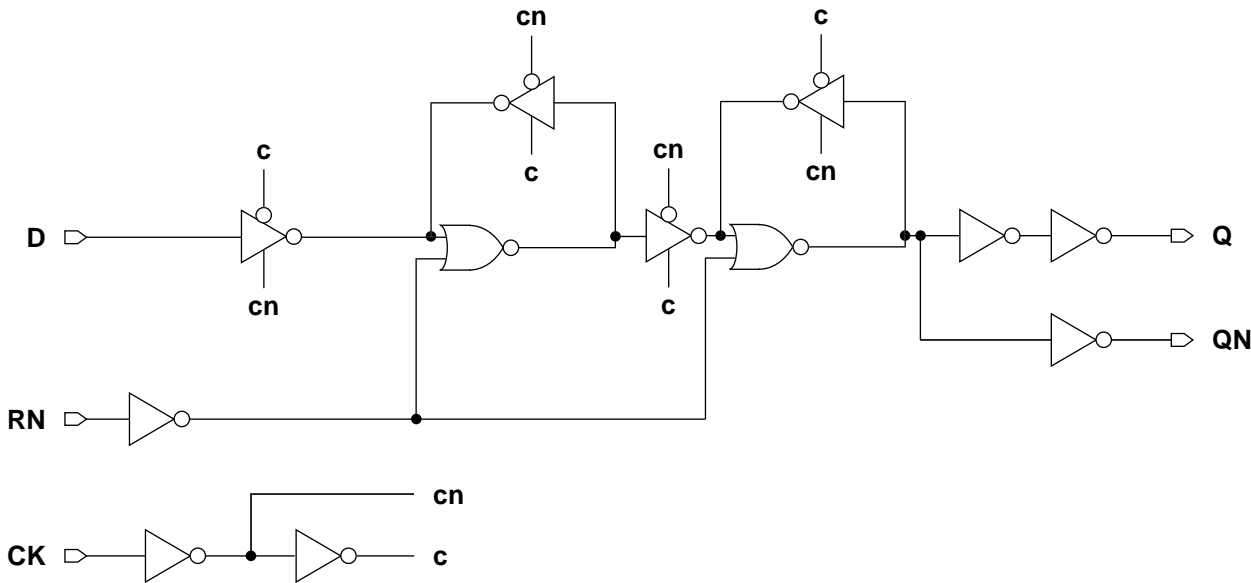
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0055	0.0056	0.0072	0.0080
CK	0.0109	0.0109	0.0127	0.0141
RN	0.0013	0.0013	0.0015	0.0019
Q	0.0049	0.0058	0.0087	0.0152

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0011	0.0011	0.0013	0.0014
CK	0.0017	0.0017	0.0018	0.0023
RN	0.0031	0.0031	0.0033	0.0040

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1334	0.1417	0.1312	0.1400	5.7554	3.8106	2.3833	1.2229
CK	→	Q	↓	0.1562	0.1670	0.1639	0.1650	4.4130	3.2251	1.4422	0.7166
RN	→	Q	↓	0.0725	0.0804	0.0900	0.0847	4.4854	3.2403	1.4621	0.7251
CK	→	QN	↑	0.0991	0.1001	0.0910	0.0879	5.7897	3.8348	2.3586	1.2464
CK	→	QN	↓	0.0891	0.0958	0.0799	0.0869	4.6783	3.3907	1.4024	0.7411
RN	→	QN	↑	0.1497	0.1510	0.1689	0.1947	5.7290	3.7924	2.4019	1.2845

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	CK	0.0820	0.0820	0.0742	0.0664
	setup	↓	→	CK	0.0352	0.0352	0.0234	0.0312
	hold	↑	→	CK	-0.0469	-0.0469	-0.0430	-0.0312
	hold	↓	→	CK	0.0078	0.0078	0.0117	0.0078
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.0820	0.0781	0.0742	0.0664
	removal				-0.0586	-0.0586	-0.0547	-0.0469

Cell Description

The DFFRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol
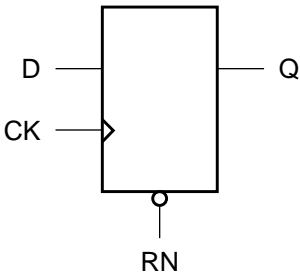
Function Table

RN	D	CK	Q[n+1]
0	x	x	0
1	0	⌐	0
1	1	⌐	1
1	x	⌐	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFRHQX1AD	2.52	7.56
DFFRHQX2AD	2.52	7.56
DFFRHQX4AD	2.52	9.24
DFFRHQX8AD	2.52	10.64

Functional Schematic
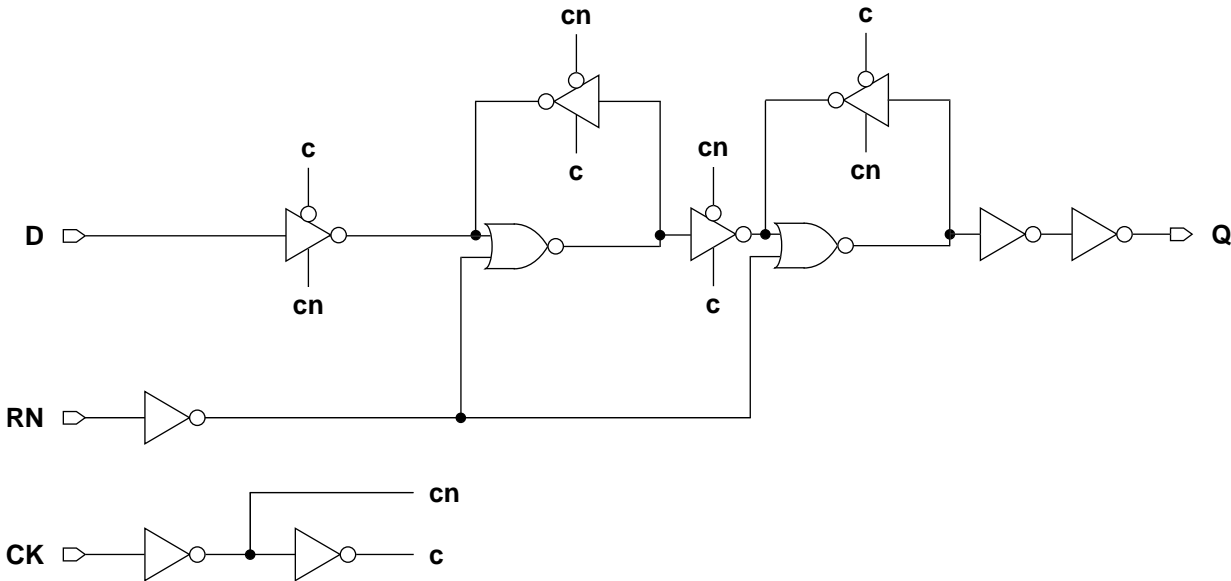
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
D	0.0076	0.0095	0.0145	0.0173
CK	0.0133	0.0165	0.0257	0.0309
RN	0.0014	0.0018	0.0028	0.0036
Q	0.0039	0.0054	0.0090	0.0160

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
D	0.0016	0.0016	0.0022	0.0038
CK	0.0021	0.0023	0.0031	0.0054
RN	0.0019	0.0024	0.0037	0.0042

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→	Q	↑	0.0820	0.0782	0.0743	0.0780	3.6882	2.3544	1.1954	0.6182
CK	→	Q	↓	0.0817	0.0746	0.0742	0.0784	3.2858	1.3905	0.6846	0.3554
RN	→	Q	↓	0.0852	0.0829	0.0699	0.0651	3.3869	1.4866	0.7175	0.3476

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
D	setup	↑	→	CK	0.0625	0.0547	0.0508	0.0469
	setup	↓	→	CK	0.0469	0.0391	0.0312	0.0312
	hold	↑	→	CK	-0.0156	-0.0117	-0.0117	-0.0039
	hold	↓	→	CK	-0.0117	-0.0117	-0.0078	-0.0039
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0117	-0.0156	-0.0195	-0.0117
	removal				0.0391	0.0469	0.0625	0.0547

Cell Description

The DFFRQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN). The cell has a single output (Q).

Logic Symbol
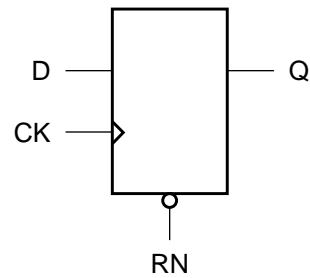
Function Table

RN	D	CK	Q[n+1]
0	x	x	0
1	0	⌐	0
1	1	⌐	1
1	x	⌐	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFRQXLAD	2.52	6.16
DFFRQX1AD	2.52	6.16
DFFRQX2AD	2.52	6.16
DFFRQX4AD	2.52	6.44

Functional Schematic
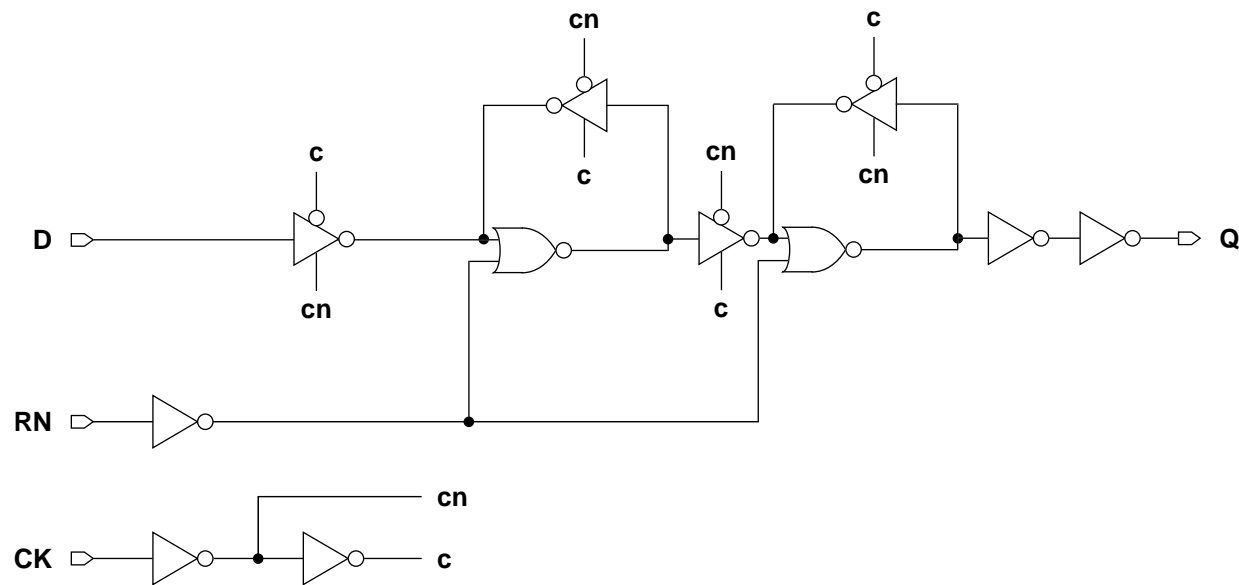
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0044	0.0044	0.0044	0.0046
CK	0.0084	0.0084	0.0084	0.0086
RN	0.0010	0.0010	0.0010	0.0013
Q	0.0037	0.0043	0.0059	0.0096

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0010	0.0010	0.0010	0.0010
CK	0.0013	0.0013	0.0013	0.0013
RN	0.0028	0.0028	0.0029	0.0034

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK → Q ↑	0.1253	0.1292	0.1310	0.1305	5.7701	3.6859	2.3519	1.2068
CK → Q ↓	0.1552	0.1630	0.1733	0.1722	4.7979	3.2730	1.4712	0.7220
RN → Q ↓	0.0683	0.0764	0.0874	0.0823	4.8397	3.2604	1.4480	0.7103

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		XL	**X1**	**X2**	**X4**
D	setup ↑ → CK	0.0742	0.0742	0.0742	0.0742
	setup ↓ → CK	0.0156	0.0156	0.0156	0.0156
	hold ↑ → CK	-0.0391	-0.0391	-0.0391	-0.0391
	hold ↓ → CK	0.0156	0.0117	0.0117	0.0156
CK	minpwh	0.8332	0.8332	0.8332	0.8332
	minpwl	0.8332	0.8332	0.8332	0.8332
RN	minpwl	0.8332	0.8332	0.8332	0.8332
	recovery	0.0742	0.0742	0.0742	0.0781
	removal	-0.0508	-0.0508	-0.0508	-0.0508

Cell Description

The DFFS cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low set (SN).

Logic Symbol
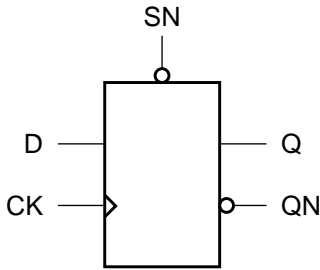
Function Table

SN	D	CK	Q[n+1]	QN[n+1]
0	x	x	1	0
1	0	⌐	0	1
1	1	⌐	1	0
1	x	⌐	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFSXLAD	2.52	6.16
DFFSX1AD	2.52	6.16
DFFSX2AD	2.52	6.16
DFFSX4AD	2.52	7.28

Functional Schematic
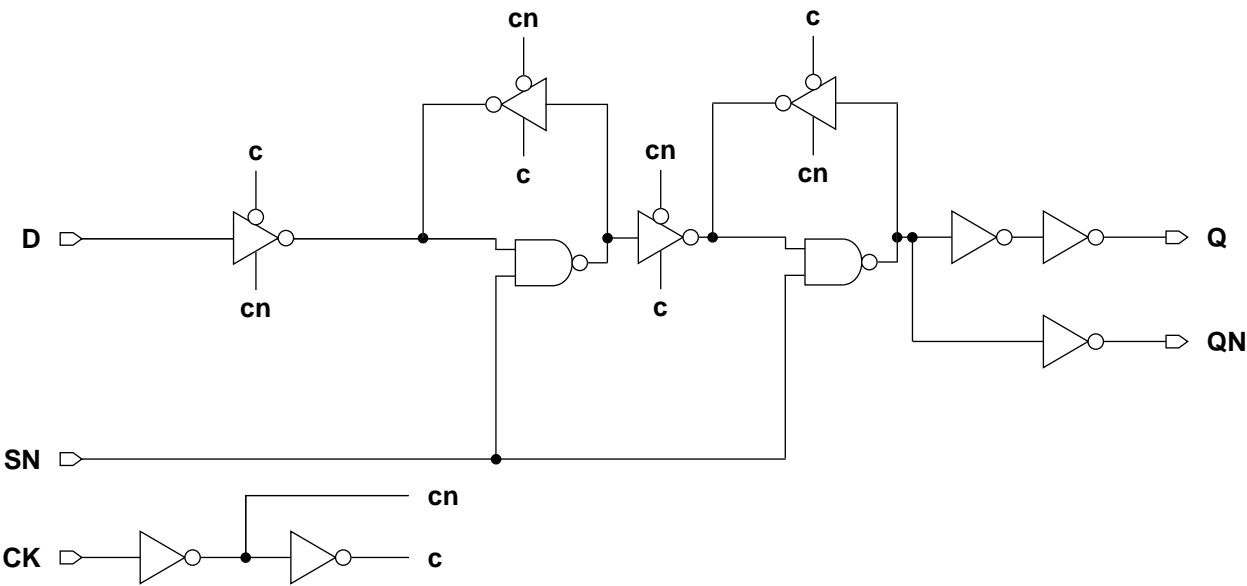
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0054	0.0054	0.0059	0.0078
CK	0.0108	0.0108	0.0114	0.0135
SN	0.0013	0.0013	0.0014	0.0019
Q	0.0054	0.0064	0.0091	0.0152

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0015	0.0015	0.0014	0.0016
CK	0.0019	0.0019	0.0020	0.0022
SN	0.0020	0.0020	0.0022	0.0029

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1427	0.1512	0.1574	0.1520	5.6768	3.7787	2.3670	1.2192
CK	→	Q	↓	0.1472	0.1553	0.1571	0.1576	4.5634	3.1224	1.3863	0.7023
SN	→	Q	↑	0.1274	0.1351	0.1666	0.2332	5.6411	3.7599	2.3629	1.2192
CK	→	QN	↑	0.1050	0.1066	0.0992	0.0880	5.9516	3.9199	2.4006	1.2438
CK	→	QN	↓	0.1076	0.1154	0.1030	0.0897	5.6937	3.7666	1.6185	0.7528
SN	→	QN	↓	0.0951	0.1018	0.1116	0.1532	4.9626	3.3303	1.5464	0.8339

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	CK	0.0625	0.0625	0.0547	0.0625
	setup	↓	→	CK	0.0156	0.0156	0.0156	0.0273
	hold	↑	→	CK	-0.0273	-0.0273	-0.0273	-0.0312
	hold	↓	→	CK	0.0117	0.0117	0.0117	0.0039
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0312	-0.0312	-0.0352	-0.0352
	removal				0.0508	0.0508	0.0547	0.0547

Cell Description

The DFFSHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low set (SN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol
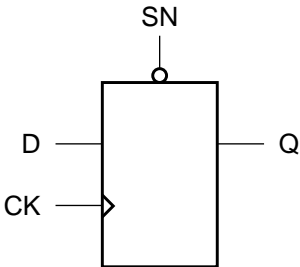
Function Table

SN	D	CK	Q[n+1]
0	x	x	1
1	0	⌐	0
1	1	⌐	1
1	x	⌐	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFSHQX1AD	2.52	7.84
DFFSHQX2AD	2.52	7.84
DFFSHQX4AD	2.52	9.24
DFFSHQX8AD	2.52	10.64

Functional Schematic
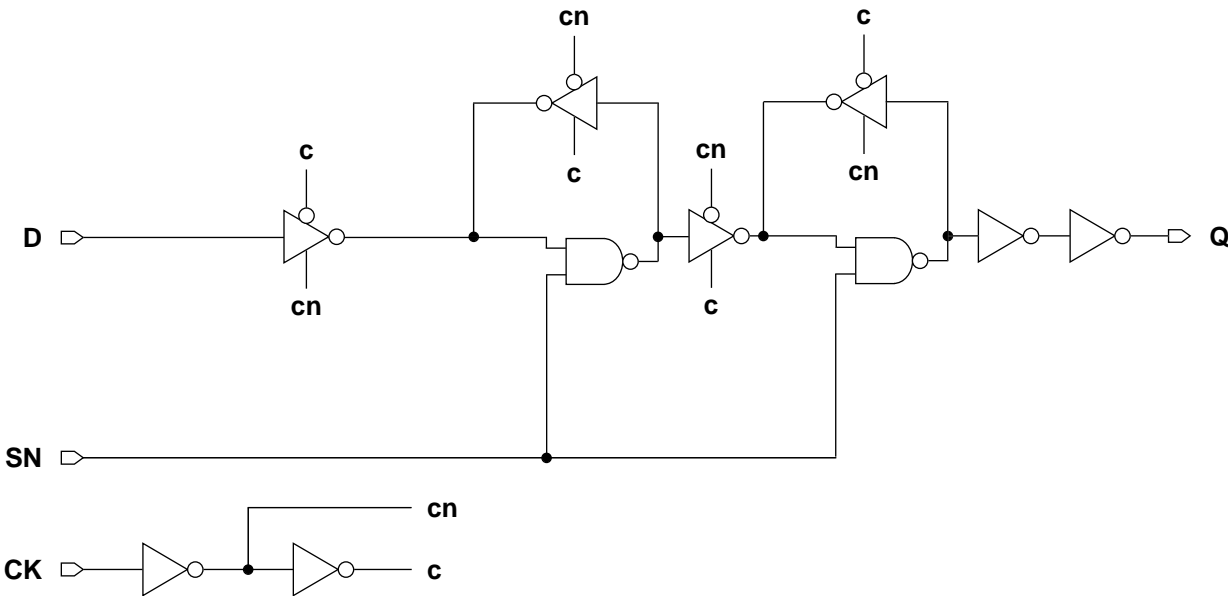
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
D	0.0070	0.0079	0.0114	0.0128
CK	0.0136	0.0157	0.0214	0.0237
SN	0.0037	0.0038	0.0047	0.0053
Q	0.0046	0.0058	0.0094	0.0159

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
D	0.0012	0.0012	0.0016	0.0025
CK	0.0021	0.0022	0.0032	0.0045
SN	0.0023	0.0027	0.0030	0.0030

Delays at 25°C,1.0V, Typical Process

Description					Intrinsic Delay (ns)				K_{load} (ns/pF)			
					X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→	Q	↑		0.0782	0.0749	0.0678	0.0708	3.6537	2.3367	1.1908	0.6170
CK	→	Q	↓		0.0853	0.0826	0.0725	0.0738	3.2358	1.4247	0.6910	0.3547
SN	→	Q	↑		0.1306	0.1442	0.1151	0.1169	3.9594	2.3832	1.1844	0.6103

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
D	setup	↑	→	CK	0.0625	0.0469	0.0508	0.0508
	setup	↓	→	CK	0.0547	0.0547	0.0547	0.0586
	hold	↑	→	CK	-0.0234	-0.0117	-0.0117	-0.0039
	hold	↓	→	CK	-0.0234	-0.0195	-0.0195	-0.0195
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.0273	0.0234	0.0312	0.0469
	removal				-0.0117	-0.0078	-0.0156	-0.0234

Cell Description

The DFFSQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low set (SN). The cell has a single output (Q).

Logic Symbol
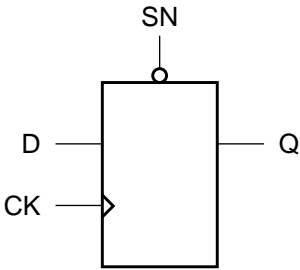
Function Table

SN	D	CK	Q[n+1]
0	x	x	1
1	0	⌐	0
1	1	⌐	1
1	x	⌐	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFSQXLAD	2.52	5.60
DFFSQX1AD	2.52	5.88
DFFSQX2AD	2.52	5.88
DFFSQX4AD	2.52	6.16

Functional Schematic
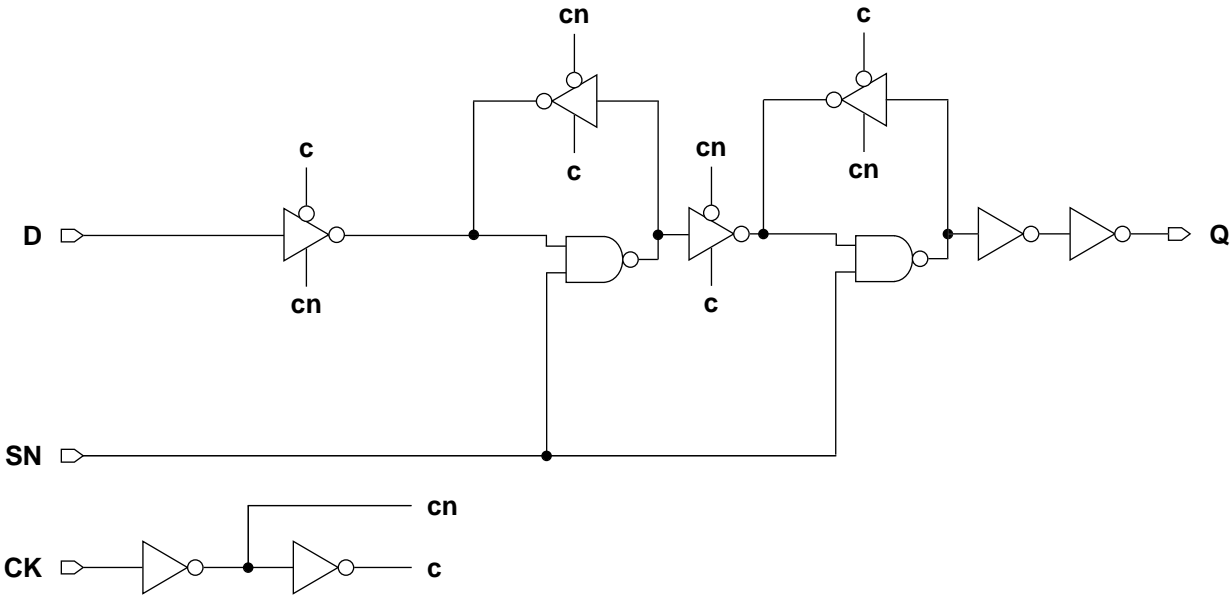
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0048	0.0048	0.0048	0.0050
CK	0.0102	0.0103	0.0103	0.0105
SN	0.0012	0.0012	0.0013	0.0015
Q	0.0040	0.0046	0.0059	0.0097

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0010	0.0010	0.0010	0.0010
CK	0.0020	0.0020	0.0020	0.0020
SN	0.0019	0.0020	0.0019	0.0020

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1186	0.1217	0.1304	0.1441	5.4954	3.6351	2.3485	1.1991
CK	→	Q	↓	0.1311	0.1385	0.1455	0.1579	4.5873	3.1763	1.4022	0.7115
SN	→	Q	↑	0.1086	0.1147	0.1206	0.1332	5.4762	3.6251	2.3446	1.1968

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	CK	0.0625	0.0625	0.0586	0.0547
	setup	↓	→	CK	0.0586	0.0586	0.0547	0.0547
	hold	↑	→	CK	-0.0195	-0.0195	-0.0195	-0.0195
	hold	↓	→	CK	-0.0078	-0.0117	-0.0078	-0.0117
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0234	-0.0234	-0.0234	-0.0273
	removal				0.0430	0.0391	0.0430	0.0430

Cell Description

The DFFSR cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset.

Logic Symbol
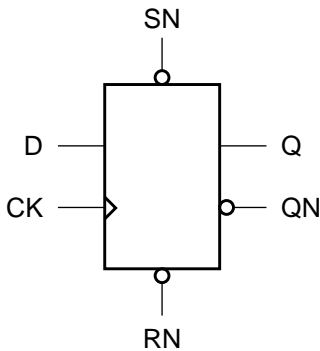
Function Table

RN	SN	D	CK	Q[n+1]	QN[n+1]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0
1	1	0	_/	0	1
1	1	1	_/	1	0
1	1	x	‾_	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFSRXLAD	2.52	7.84
DFFSRX1AD	2.52	8.12
DFFSRX2AD	2.52	8.40
DFFSRX4AD	2.52	10.36

Functional Schematic
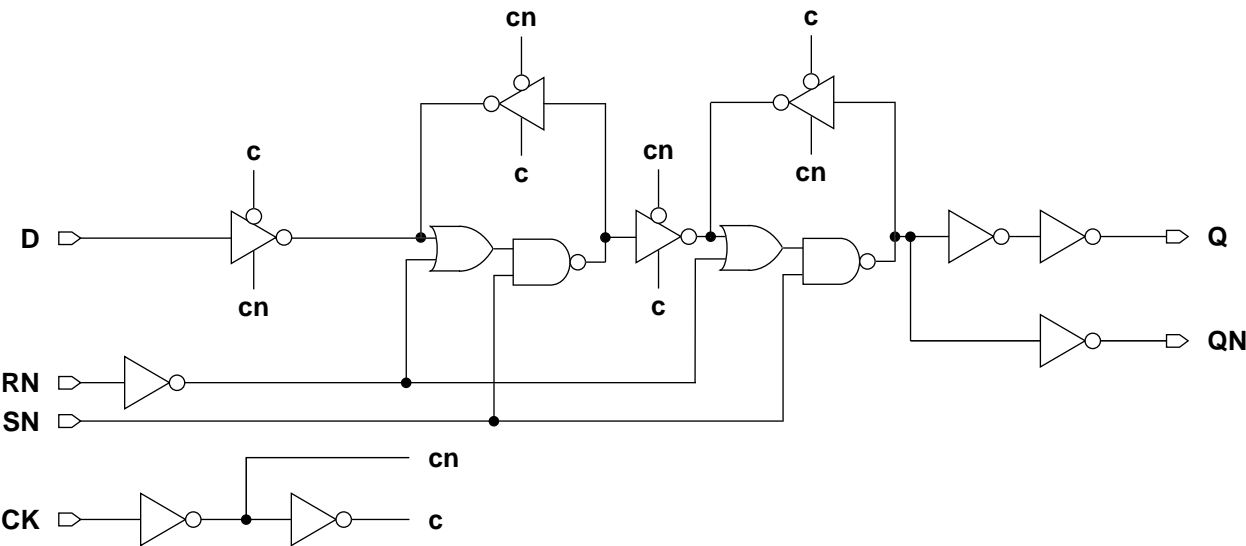
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0054	0.0054	0.0063	0.0097
CK	0.0110	0.0110	0.0123	0.0166
SN	0.0013	0.0014	0.0016	0.0020
RN	0.0026	0.0026	0.0029	0.0034
Q	0.0062	0.0074	0.0102	0.0152

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0010	0.0010	0.0010	0.0013
CK	0.0017	0.0017	0.0019	0.0022
SN	0.0021	0.0020	0.0023	0.0030
RN	0.0012	0.0012	0.0012	0.0012

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1528	0.1615	0.1663	0.1561	5.7268	3.6918	2.3773	1.2205
CK	→	Q	↓	0.1561	0.1658	0.1636	0.1677	4.2568	3.1347	1.3772	0.7019
SN	→	Q	↑	0.1436	0.1515	0.1834	0.2480	5.6730	3.6602	2.3708	1.2195
SN	→	Q	↓	0.1246	0.1334	0.1456	0.1669	4.2184	3.1175	1.3729	0.7024
RN	→	Q	↓	0.1474	0.1561	0.1744	0.2116	4.2300	3.1224	1.3743	0.7025
CK	→	QN	↑	0.1117	0.1122	0.1074	0.0984	6.1474	3.9298	2.4480	1.2504
CK	→	QN	↓	0.1151	0.1242	0.1131	0.0931	5.7408	4.0143	1.6811	0.7653
SN	→	QN	↑	0.0814	0.0816	0.0874	0.0897	5.9224	3.7989	2.4390	1.2711
SN	→	QN	↓	0.1095	0.1175	0.1298	0.1667	4.7902	3.4112	1.5704	0.8440
RN	→	QN	↑	0.1032	0.1035	0.1158	0.1373	5.9964	3.8320	2.4478	1.2782

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	X1	X2	X4
D	setup	↑	→	CK	0.0781	0.0781	0.0625	0.0625
	setup	↓	→	CK	0.0664	0.0664	0.0703	0.0664
	hold	↑	→	CK	-0.0195	-0.0195	-0.0234	-0.0234
	hold	↓	→	CK	-0.0156	-0.0156	-0.0195	-0.0156
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0234	-0.0234	-0.0312	-0.0391
	removal				0.0430	0.0391	0.0508	0.0625
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.0742	0.0703	0.0469	0.0508
	removal				-0.0234	-0.0234	-0.0156	-0.0117

Cell Description

The DFFSRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset. The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol
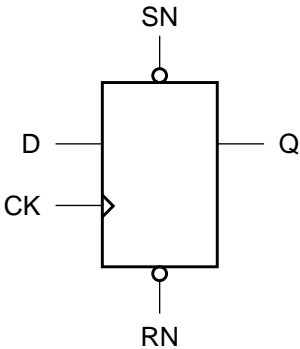
Function Table

RN	SN	D	CK	Q[n+1]
0	1	x	x	0
1	0	x	x	1
0	0	x	x	1
1	1	0	⌐	0
1	1	1	⌐	1
1	1	x	⌐	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFSRHQX1AD	2.52	9.24
DFFSRHQX2AD	2.52	9.24
DFFSRHQX4AD	2.52	11.76
DFFSRHQX8AD	2.52	13.16

Functional Schematic
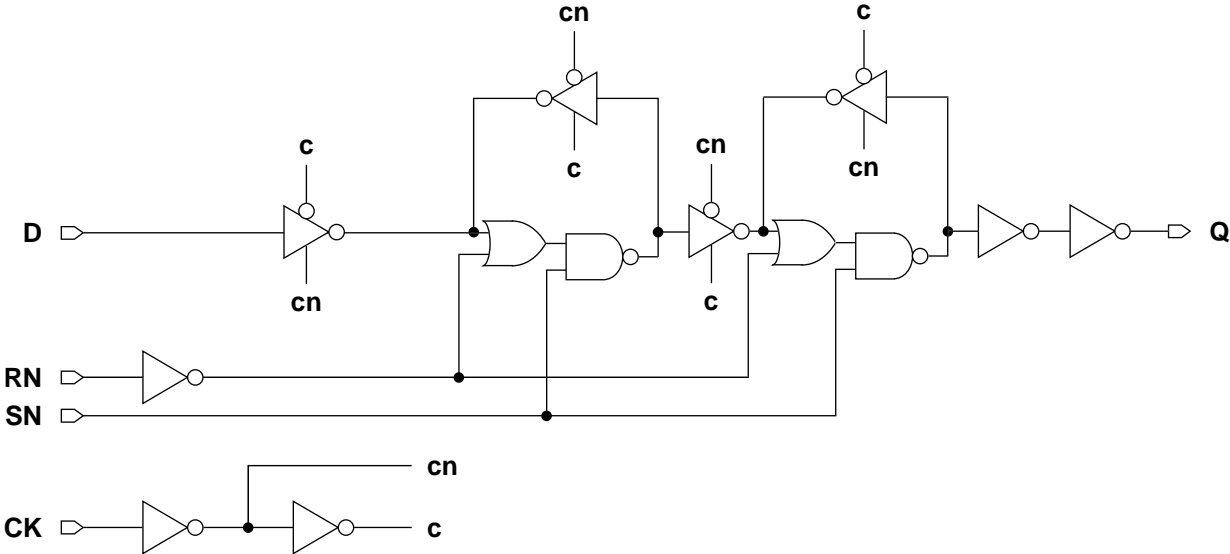
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
D	0.0076	0.0090	0.0137	0.0172
CK	0.0141	0.0162	0.0238	0.0301
SN	0.0044	0.0045	0.0058	0.0073
RN	0.0015	0.0017	0.0027	0.0037
Q	0.0052	0.0067	0.0102	0.0176

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
D	0.0012	0.0012	0.0015	0.0024
CK	0.0022	0.0021	0.0028	0.0041
SN	0.0023	0.0026	0.0033	0.0043
RN	0.0019	0.0023	0.0035	0.0041

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→ Q	↑	0.0931	0.0877	0.0824	0.0793	3.7892	2.3854	1.2077	0.6258
CK	→ Q	↓	0.0970	0.0877	0.0832	0.0766	3.4546	1.4714	0.7122	0.3614
SN	→ Q	↑	0.1085	0.1273	0.1676	0.1201	3.6597	2.3663	1.2011	0.6160
SN	→ Q	↓	0.2076	0.1893	0.1742	0.1746	3.7239	1.7158	0.8404	0.4235
RN	→ Q	↓	0.1834	0.1580	0.1352	0.1441	3.7350	1.7166	0.8419	0.4237

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
D	setup	↑	→	CK	0.0781	0.0625	0.0703	0.0586
	setup	↓	→	CK	0.0625	0.0508	0.0508	0.0547
	hold	↑	→	CK	-0.0234	-0.0195	-0.0195	-0.0078
	hold	↓	→	CK	-0.0234	-0.0195	-0.0156	-0.0156
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.0352	0.0234	0.0234	0.0312
	removal				-0.0156	-0.0117	-0.0078	-0.0156
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0117	-0.0156	-0.0156	-0.0078
	removal				0.0352	0.0430	0.0547	0.0469

Cell Description

The DFFTR cell is a positive-edge triggered, static D-type flip-flop with synchronous active-low reset (RN).

Logic Symbol
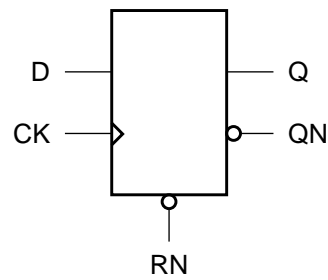
Function Table

RN	D	CK	Q[n+1]	QN[n+1]
0	x	⌐	0	1
x	x	⌐	Q[n]	QN[n]
1	0	⌐	0	1
1	1	⌐	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
DFFTRXLAD	2.52	5.88
DFFTRX1AD	2.52	6.16
DFFTRX2AD	2.52	6.16
DFFTRX4AD	2.52	8.12

Functional Schematic
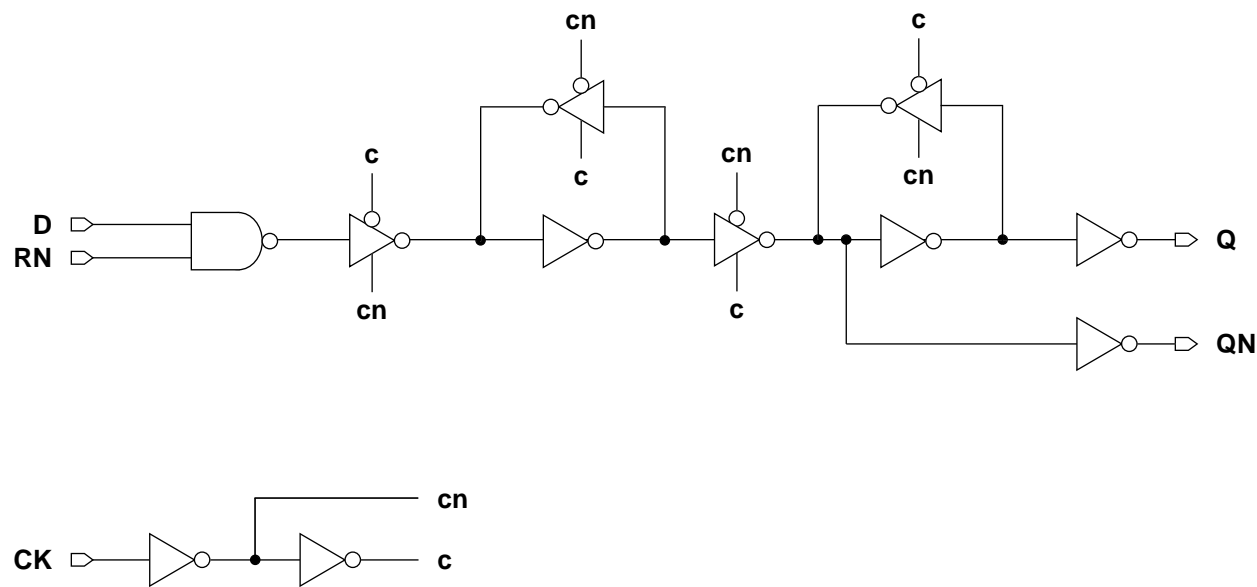
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0052	0.0058	0.0070	0.0112
CK	0.0107	0.0112	0.0131	0.0192
RN	0.0056	0.0061	0.0077	0.0129
Q	0.0053	0.0061	0.0085	0.0143

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0011	0.0011	0.0013	0.0020
CK	0.0016	0.0016	0.0017	0.0022
RN	0.0010	0.0010	0.0011	0.0016

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1225	0.1183	0.1218	0.1117	5.6563	3.6469	2.3622	1.2105
CK	→	Q	↓	0.1358	0.1399	0.1433	0.1353	4.1846	3.1102	1.3651	0.6642
CK	→	QN	↑	0.0958	0.0909	0.0913	0.0877	5.8263	3.6787	2.3567	1.2234
CK	→	QN	↓	0.0890	0.0870	0.0809	0.0728	4.6853	3.2762	1.3842	0.6696

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	CK	0.0703	0.0703	0.0547	0.0508
	setup	↓	→	CK	0.0977	0.1016	0.0820	0.0547
	hold	↑	→	CK	-0.0312	-0.0312	-0.0234	-0.0195
	hold	↓	→	CK	-0.0312	-0.0352	-0.0234	-0.0078
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
RN	setup	↑	→	CK	0.0703	0.0742	0.0586	0.0508
	setup	↓	→	CK	0.1016	0.1055	0.1211	0.1133
	hold	↑	→	CK	-0.0312	-0.0352	-0.0273	-0.0234
	hold	↓	→	CK	-0.0312	-0.0352	-0.0469	-0.0391

Cell Description

The DFFYQ cell is a positive-edge triggered, static D-type flip-flop to be used in synchronizing circuitry between asynchronous systems. The cell has a single output (Q) and overdriven feedback loops to increase MTBF due to metastability.

Logic Symbol

D — Q

CK —
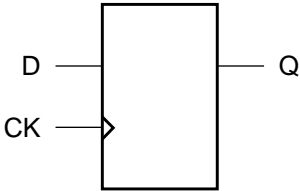
Function Table

D	CK	Q[n+1]
0	_/	0
1	_/	1
x	‾_	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFYQX2AD	2.52	6.16

Functional Schematic
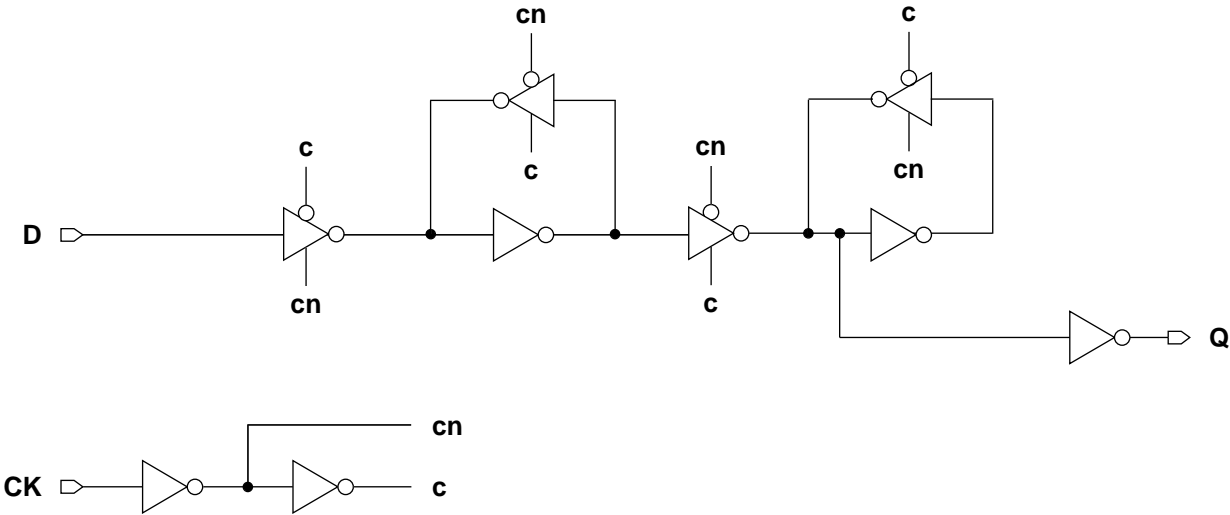
AC Power

Pin	Power (uW/MHz)
	X2
D	0.0094
CK	0.0167
Q	0.0059

Pin Capacitance

Pin	Capacitance (pF)
	X2
D	0.0023
CK	0.0026

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X2	**X2**
CK → Q ↑	0.0913	2.3195
CK → Q ↓	0.0984	1.4689

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)
		X2
D	setup ↑ → CK	0.0195
	setup ↓ → CK	0.0391
	hold ↑ → CK	-0.0117
	hold ↓ → CK	-0.0117
CK	minpwh	0.8332
	minpwl	0.8332

Cell Description

The DLY1 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

Y = A

Logic Symbol

A —[⊢——⊣]— Y

Function Table

A	Y
0	0
1	1
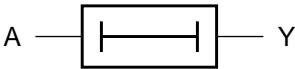
Cell Size

Drive Strength	Height (um)	Width (um)
DLY1X1AD	2.52	2.52
DLY1X4AD	2.52	3.08

Functional Schematic

A ▷———▷○———▷○———▷○———▷○———▷ Y

AC Power

Pin	Power (uW/MHz)	
	X1	**X4**
A	0.0057	0.0097

Pin Capacitance

Pin	Capacitance (pF)	
	X1	**X4**
A	0.0014	0.0020

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)		K_{load} (ns/pF)	
			X1	**X4**	**X1**	**X4**
A	→ Y	↑	0.0644	0.0601	3.7698	1.1966
A	→ Y	↓	0.0818	0.0773	3.0173	1.3534

Cell Description

The DLY2 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Logic Symbol

A ——▭—— Y

Function Table

A	Y
0	0
1	1
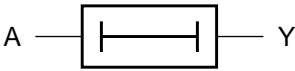
Cell Size

Drive Strength	Height (um)	Width (um)
DLY2X1AD	2.52	2.52
DLY2X4AD	2.52	3.08

Functional Schematic

A ▷——▷o——▷o——▷o——▷o——▷ Y
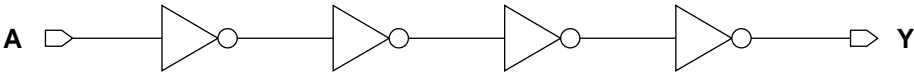
AC Power

Pin	Power (uW/MHz)	
	X1	**X4**
A	0.0067	0.0116

Pin Capacitance

Pin	Capacitance (pF)	
	X1	**X4**
A	0.0014	0.0020

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X1	**X4**	**X1**	**X4**
A → Y ↑	0.1108	0.1056	3.8088	1.2080
A → Y ↓	0.1266	0.1260	3.1711	1.3894

Cell Description

The DLY3 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Logic Symbol

A ——[|——|]—— Y

Function Table

A	Y
0	0
1	1
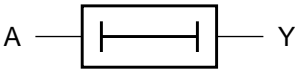
Cell Size

Drive Strength	Height (um)	Width (um)
DLY3X1AD	2.52	2.52
DLY3X4AD	2.52	3.08

Functional Schematic

A ▷——▷o——▷o——▷o——▷o——▷ Y
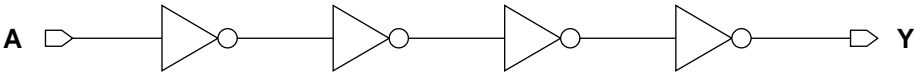
AC Power

Pin	Power (uW/MHz)	
	X1	**X4**
A	0.0079	0.0139

Pin Capacitance

Pin	Capacitance (pF)	
	X1	**X4**
A	0.0014	0.0020

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X1	**X4**	**X1**	**X4**
A → Y ↑	0.1681	0.1595	3.8707	1.2240
A → Y ↓	0.1754	0.1767	3.3620	1.4380

Cell Description

The DLY4 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Logic Symbol

A ⎯⎢ ⊢⎯⊣ ⎢⎯ Y

Function Table

A	Y
0	0
1	1
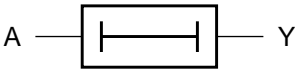
Cell Size

Drive Strength	Height (um)	Width (um)
DLY4X1AD	2.52	2.52
DLY4X4AD	2.52	3.08

Functional Schematic

A ▷⎯▷∘⎯▷∘⎯▷∘⎯▷∘⎯▷ Y

AC Power

Pin	Power (uW/MHz)	
	X1	**X4**
A	0.0092	0.0163

Pin Capacitance

Pin	Capacitance (pF)	
	X1	**X4**
A	0.0014	0.0020

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X1	**X4**	**X1**	**X4**
A → Y ↑	0.2390	0.2264	3.9675	1.2524
A → Y ↓	0.2325	0.2357	3.5815	1.4963

Cell Description

The EDFF cell is a positive-edge triggered, static D-type flip-flop with synchronous active-high enable (E).

Logic Symbol
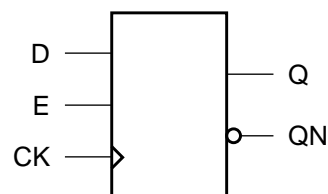
Function Table

E	D	CK	Q[n+1]	QN[n+1]
0	x	x	Q[n]	QN[n]
1	0	⌐	0	1
1	1	⌐	1	0
1	x	⌐	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
EDFFXLAD	2.52	7.56
EDFFX1AD	2.52	7.56
EDFFX2AD	2.52	7.56
EDFFX4AD	2.52	10.08

Functional Schematic
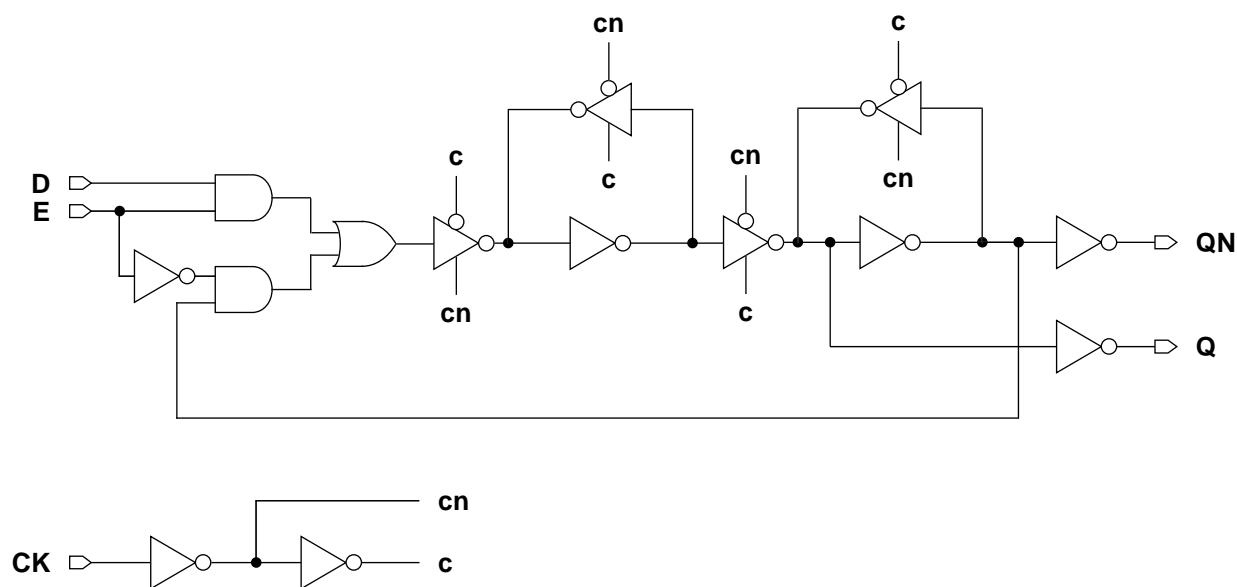
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0060	0.0061	0.0065	0.0077
CK	0.0104	0.0106	0.0110	0.0141
E	0.0087	0.0089	0.0093	0.0106
Q	0.0067	0.0076	0.0102	0.0176

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0015	0.0015	0.0015	0.0014
CK	0.0015	0.0015	0.0015	0.0018
E	0.0027	0.0027	0.0027	0.0027

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1053	0.1008	0.1027	0.1107	5.7264	3.5988	2.3783	1.2192
CK	→	Q	↓	0.1195	0.1143	0.1002	0.1011	5.3331	3.4119	1.4381	0.7224
CK	→	QN	↑	0.1708	0.1641	0.1510	0.1515	5.7518	3.6585	2.3446	1.2129
CK	→	QN	↓	0.1645	0.1669	0.1597	0.1626	4.8282	3.2533	1.3958	0.6748

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	CK	0.0859	0.0859	0.0898	0.0898
	setup	↓	→	CK	0.0820	0.0820	0.0898	0.1016
	hold	↑	→	CK	-0.0625	-0.0625	-0.0625	-0.0625
	hold	↓	→	CK	-0.0469	-0.0469	-0.0469	-0.0430
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
E	setup	↑	→	CK	0.1055	0.1055	0.1094	0.1211
	setup	↓	→	CK	0.1133	0.1133	0.1133	0.1133
	hold	↑	→	CK	-0.0703	-0.0703	-0.0703	-0.0703
	hold	↓	→	CK	-0.0430	-0.0430	-0.0391	-0.0352

Cell Description

The EDFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with a synchronous, active-high enable (E). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol
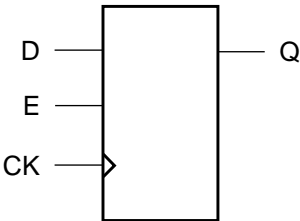
Function Table

E	D	CK	Q[n+1]
0	x	x	Q[n]
1	0	⌐	0
1	1	⌐	1
x	x	⌐	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
EDFFHQX1AD	2.52	8.68
EDFFHQX2AD	2.52	8.96
EDFFHQX4AD	2.52	11.76
EDFFHQX8AD	2.52	15.40

Functional Schematic
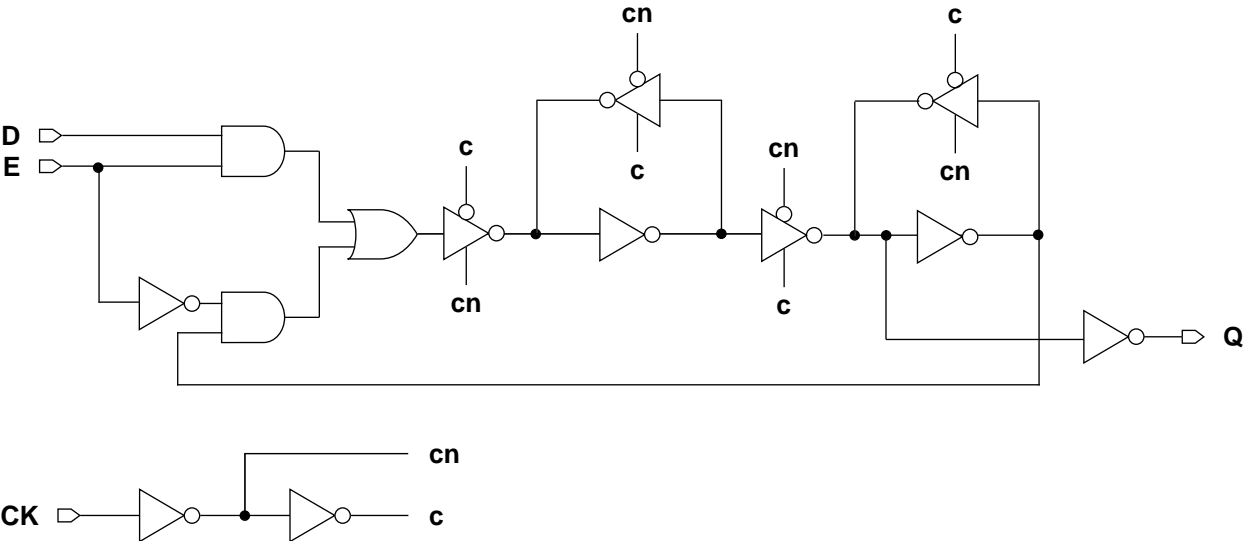
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
D	0.0094	0.0123	0.0184	0.0327
CK	0.0151	0.0182	0.0271	0.0408
E	0.0107	0.0124	0.0183	0.0295
Q	0.0047	0.0065	0.0097	0.0166

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
D	0.0018	0.0023	0.0038	0.0077
CK	0.0022	0.0025	0.0034	0.0044
E	0.0035	0.0036	0.0039	0.0060

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK → Q ↑	0.0800	0.0768	0.0679	0.0608	3.6438	2.3479	1.1902	0.6087
CK → Q ↓	0.0877	0.0816	0.0700	0.0639	3.2481	1.3981	0.6785	0.3319

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
D	setup	↑	→	CK	0.0664	0.0547	0.0508	0.0586
	setup	↓	→	CK	0.0625	0.0469	0.0469	0.0586
	hold	↑	→	CK	-0.0312	-0.0195	-0.0156	-0.0195
	hold	↓	→	CK	-0.0312	-0.0195	-0.0195	-0.0273
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
E	setup	↑	→	CK	0.0625	0.0508	0.0508	0.0664
	setup	↓	→	CK	0.0820	0.0859	0.0977	0.1016
	hold	↑	→	CK	-0.0430	-0.0312	-0.0234	-0.0312
	hold	↓	→	CK	-0.0625	-0.0703	-0.0703	-0.0625

Cell Description

The EDFFTR cell is a positive-edge triggered, static D-type flip-flop with synchronous active-high enable (E) and synchronous active-low reset (RN).

Logic Symbol
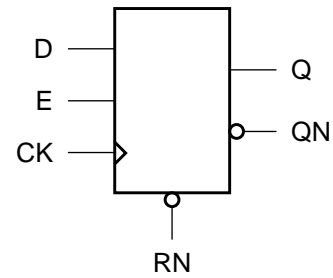
Function Table

RN	E	D	CK	Q[n+1]	QN[n+1]
0	x	x	⌐	0	1
x	x	x	⌐	Q[n]	QN[n]
1	0	x	⌐	Q[n]	QN[n]
1	1	0	⌐	0	1
1	1	1	⌐	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
EDFFTRXLAD	2.52	8.68
EDFFTRX1AD	2.52	8.68
EDFFTRX2AD	2.52	8.68
EDFFTRX4AD	2.52	10.08

Functional Schematic
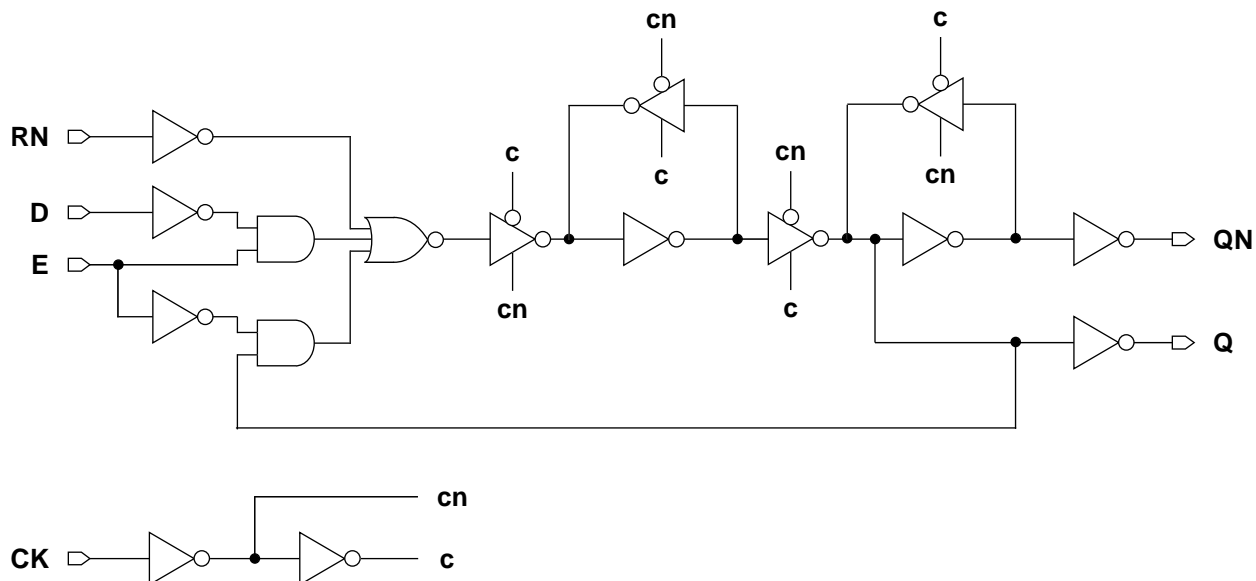
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0057	0.0058	0.0061	0.0074
CK	0.0111	0.0113	0.0117	0.0139
E	0.0084	0.0085	0.0088	0.0101
RN	0.0061	0.0063	0.0066	0.0079
Q	0.0060	0.0069	0.0096	0.0163

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0011	0.0011	0.0011	0.0011
CK	0.0016	0.0016	0.0016	0.0019
E	0.0030	0.0030	0.0030	0.0030
RN	0.0011	0.0010	0.0011	0.0011

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q ↑	0.1085	0.1049	0.1083	0.1017	5.7820	3.6990	2.3879	1.2259
CK	→	Q ↓	0.1173	0.1151	0.1036	0.0946	4.9382	3.3905	1.4362	0.7067
CK	→	QN ↑	0.1644	0.1596	0.1549	0.1443	5.7543	3.6922	2.3744	1.2136
CK	→	QN ↓	0.1642	0.1685	0.1704	0.1560	4.4379	3.2280	1.4092	0.6794

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	X1	X2	X4
D	setup	↑	→	CK	0.0781	0.0781	0.0820	0.0898
	setup	↓	→	CK	0.2070	0.2070	0.2109	0.2305
	hold	↑	→	CK	-0.0625	-0.0664	-0.0664	-0.0703
	hold	↓	→	CK	-0.1680	-0.1680	-0.1641	-0.1758
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
E	setup	↑	→	CK	0.2305	0.2305	0.2344	0.2539
	setup	↓	→	CK	0.1758	0.1758	0.1758	0.1875
	hold	↑	→	CK	-0.0625	-0.0625	-0.0625	-0.0703
	hold	↓	→	CK	-0.0977	-0.0977	-0.0977	-0.1055
RN	setup	↑	→	CK	0.0859	0.0898	0.0898	0.0977
	setup	↓	→	CK	0.1562	0.1562	0.1602	0.1758
	hold	↑	→	CK	-0.0742	-0.0742	-0.0742	-0.0781
	hold	↓	→	CK	-0.1094	-0.1094	-0.1055	-0.1172

Cell Description

The INV cell provides the logical inversion of a single input (A). The output (Y) is represented by the logic equation:

$Y = \overline{A}$

Logic Symbol

A ───▷o── Y

Function Table

A	Y
0	1
1	0
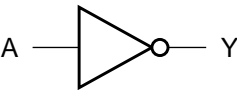
Cell Size

Drive Strength	Height (um)	Width (um)
INVXLAD	2.52	0.84
INVX1AD	2.52	0.84
INVX2AD	2.52	0.84
INVX3AD	2.52	1.12
INVX4AD	2.52	1.12
INVX5AD	2.52	1.40
INVX6AD	2.52	1.68
INVX8AD	2.52	1.96
INVX10AD	2.52	2.24
INVX12AD	2.52	2.52
INVX14AD	2.52	3.08
INVX16AD	2.52	3.36
INVX18AD	2.52	3.64
INVX20AD	2.52	4.20

Functional Schematic

A ▷─────▷o────▷ Y
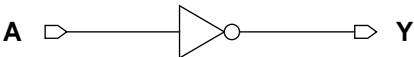
AC Power

Pin	Power (uW/MHz)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A	0.0012	0.0016	0.0027	0.0039	0.0049	0.0062	0.0076	0.0098

AC Power (Cont'd.)

Pin	Power (uW/MHz)					
	X10	**X12**	**X14**	**X16**	**X18**	**X20**
A	0.0126	0.0149	0.0177	0.0199	0.0226	0.0251

Pin Capacitance

Pin	Capacitance (pF)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A	0.0012	0.0017	0.0028	0.0043	0.0054	0.0066	0.0079	0.0106

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)					
	X10	**X12**	**X14**	**X16**	**X18**	**X20**
A	0.0133	0.0159	0.0186	0.0212	0.0239	0.0266

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A → Y ↑	0.0115	0.0108	0.0112	0.0111	0.0107	0.0109	0.0110	0.0109
A → Y ↓	0.0102	0.0101	0.0084	0.0080	0.0078	0.0080	0.0079	0.0079

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)					
	X10	**X12**	**X14**	**X16**	**X18**	**X20**
A → Y ↑	0.0111	0.0111	0.0114	0.0115	0.0116	0.0116
A → Y ↓	0.0080	0.0079	0.0081	0.0082	0.0082	0.0083

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A → Y ↑	5.4375	3.5081	2.2794	1.5668	1.1774	0.9404	0.7958	0.6022
A → Y ↓	4.3018	3.0042	1.2750	0.8256	0.6249	0.5088	0.4140	0.3088

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)					
	X10	**X12**	**X14**	**X16**	**X18**	**X20**
A → Y ↑	0.4860	0.4084	0.3513	0.3082	0.2751	0.2482
A → Y ↓	0.2494	0.2068	0.1766	0.1535	0.1367	0.1229

Cell Description

The MDFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with a 2-to-1data select control (S0) for the data inputs (D1,D0). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol
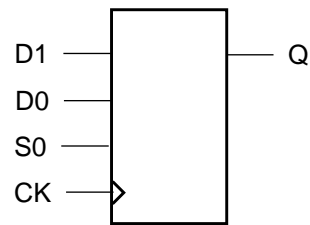
Function Table

S0	D1	D0	CK	Q[n+1]
0	x	0	⌐/	0
0	x	1	⌐/	1
1	0	x	⌐/	0
1	1	x	⌐/	1
x	x	x	⌐\	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
MDFFHQX1AD	2.52	8.12
MDFFHQX2AD	2.52	8.40
MDFFHQX4AD	2.52	11.48
MDFFHQX8AD	2.52	16.80

Functional Schematic
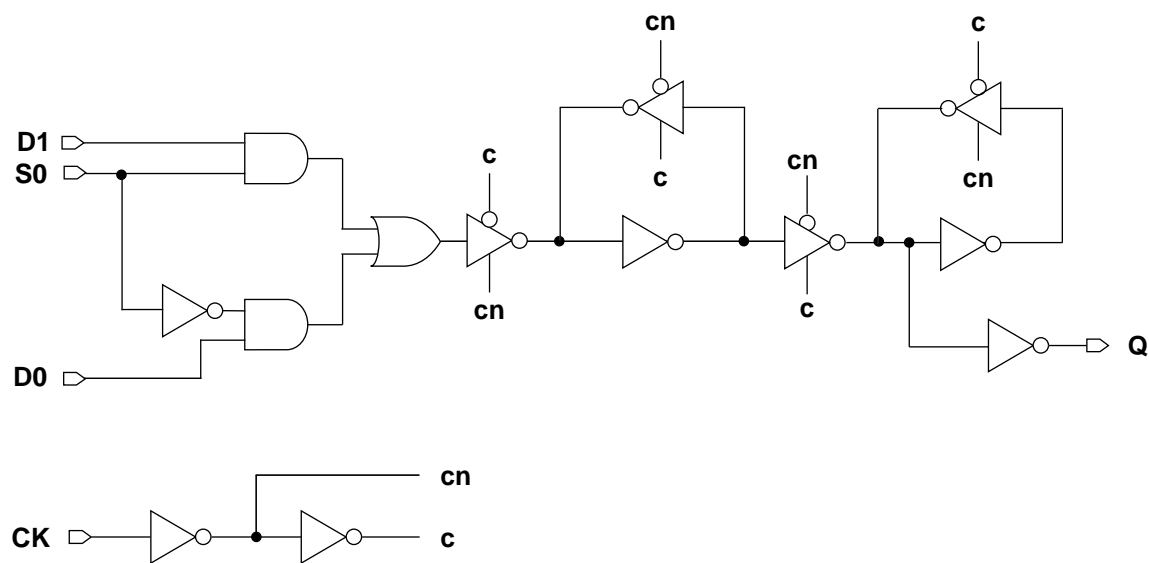
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
D0	0.0076	0.0103	0.0171	0.0293
D1	0.0081	0.0111	0.0187	0.0318
S0	0.0093	0.0122	0.0199	0.0343
CK	0.0136	0.0167	0.0269	0.0440
Q	0.0042	0.0057	0.0089	0.0144

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
D0	0.0012	0.0016	0.0026	0.0046
D1	0.0012	0.0016	0.0026	0.0047
S0	0.0022	0.0025	0.0030	0.0048
CK	0.0024	0.0024	0.0033	0.0053

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→ Q	↑	0.0777	0.0739	0.0683	0.0620	3.6227	2.3150	1.1810	0.6062
CK	→ Q	↓	0.0871	0.0818	0.0732	0.0647	3.2639	1.3886	0.6717	0.3268

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
D0	setup	↑	→	CK	0.0820	0.0664	0.0586	0.0547
	setup	↓	→	CK	0.0898	0.0742	0.0586	0.0742
	hold	↑	→	CK	-0.0430	-0.0352	-0.0234	-0.0195
	hold	↓	→	CK	-0.0586	-0.0430	-0.0312	-0.0391
D1	setup	↑	→	CK	0.0820	0.0625	0.0586	0.0508
	setup	↓	→	CK	0.0938	0.0742	0.0664	0.0781
	hold	↑	→	CK	-0.0430	-0.0312	-0.0234	-0.0156
	hold	↓	→	CK	-0.0625	-0.0469	-0.0352	-0.0430
S0	setup	↑	→	CK	0.0859	0.0703	0.0625	0.0781
	setup	↓	→	CK	0.0938	0.0859	0.0898	0.0859
	hold	↑	→	CK	-0.0352	-0.0234	-0.0156	-0.0117
	hold	↓	→	CK	-0.0508	-0.0391	-0.0312	-0.0391
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The MX2 cell is a 2-to-1 multiplexer. The state of the select input (S0) determines which data input (A,B) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (\overline{S0} \bullet A) + (S0 \bullet B)$$

Logic Symbol

A ───

B ───

Y

S0
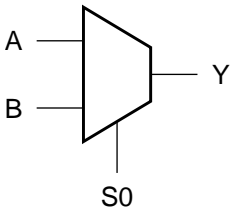
Function Table

S0	A	B	Y
0	0	x	0
0	1	x	1
1	x	0	0
1	x	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
MX2XLAD	2.52	2.52
MX2X1AD	2.52	2.52
MX2X2AD	2.52	3.08
MX2X3AD	2.52	3.36
MX2X4AD	2.52	3.36
MX2X6AD	2.52	3.92
MX2X8AD	2.52	4.20

Functional Schematic

A
s0n

B
s0

Y

s0n

S0

s0
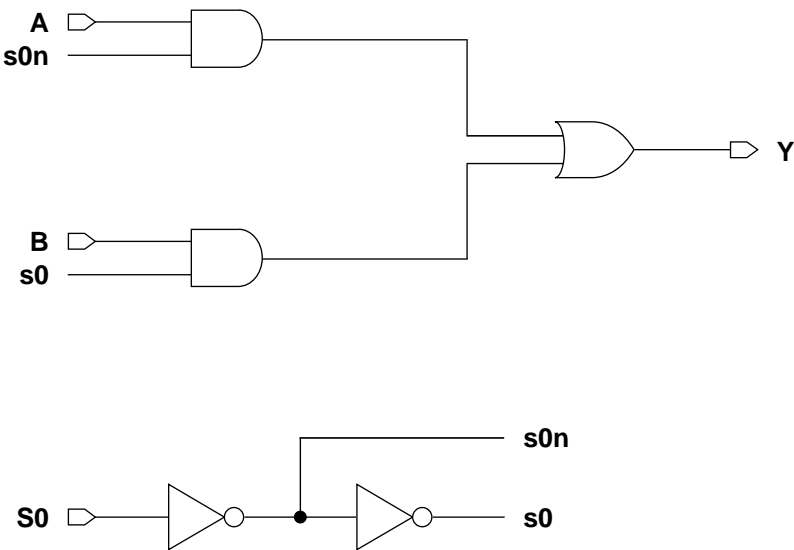
AC Power

Pin	Power (uW/MHz)						
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
S0	0.0046	0.0058	0.0098	0.0118	0.0129	0.0164	0.0210
A	0.0038	0.0047	0.0078	0.0102	0.0117	0.0160	0.0205
B	0.0042	0.0053	0.0085	0.0114	0.0128	0.0172	0.0218

Pin Capacitance

Pin	Capacitance (pF)						
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
S0	0.0026	0.0029	0.0042	0.0047	0.0047	0.0048	0.0048
A	0.0014	0.0017	0.0025	0.0029	0.0029	0.0029	0.0029
B	0.0013	0.0015	0.0022	0.0026	0.0026	0.0026	0.0026

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)						
				XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
S0	$\to$	Y	$\uparrow$	0.0604	0.0584	0.0675	0.0654	0.0668	0.0710	0.0759
S0	$\to$	Y	$\downarrow$	0.0620	0.0581	0.0559	0.0549	0.0593	0.0680	0.0778
A	$\to$	Y	$\uparrow$	0.0480	0.0425	0.0420	0.0430	0.0444	0.0507	0.0561
A	$\to$	Y	$\downarrow$	0.0688	0.0616	0.0546	0.0552	0.0589	0.0678	0.0759
B	$\to$	Y	$\uparrow$	0.0465	0.0409	0.0392	0.0400	0.0415	0.0478	0.0532
B	$\to$	Y	$\downarrow$	0.0700	0.0622	0.0554	0.0568	0.0599	0.0693	0.0774

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)						
				XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
S0	$\to$	Y	$\uparrow$	5.6796	3.6186	2.3757	1.6340	1.2174	0.8229	0.6237
S0	$\to$	Y	$\downarrow$	4.9082	3.0915	1.3752	0.9091	0.6984	0.4781	0.3709
A	$\to$	Y	$\uparrow$	5.6808	3.6175	2.3776	1.6352	1.2186	0.8240	0.6245
A	$\to$	Y	$\downarrow$	4.8852	3.0940	1.3816	0.9178	0.7044	0.4815	0.3727
B	$\to$	Y	$\uparrow$	5.6859	3.6193	2.3777	1.6360	1.2186	0.8244	0.6251
B	$\to$	Y	$\downarrow$	4.9115	3.0926	1.3747	0.9091	0.6953	0.4806	0.3721

Cell Description

The MX3 cell is a 3-to-1 multiplexer. The state of the select inputs (S1,S0) determines which data input (A,B,C) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (\overline{S0} \bullet \overline{S1} \bullet A) + (S0 \bullet \overline{S1} \bullet B) + (S1 \bullet C)$$

Logic Symbol
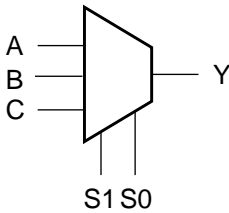
Function Table

S1	S0	A	B	C	Y
0	0	0	x	x	0
0	0	1	x	x	1
0	1	x	0	x	0
0	1	x	1	x	1
1	x	x	x	0	0
1	x	x	x	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
MX3XLAD	2.52	5.04
MX3X1AD	2.52	5.04
MX3X2AD	2.52	5.60
MX3X4AD	2.52	6.16

Functional Schematic
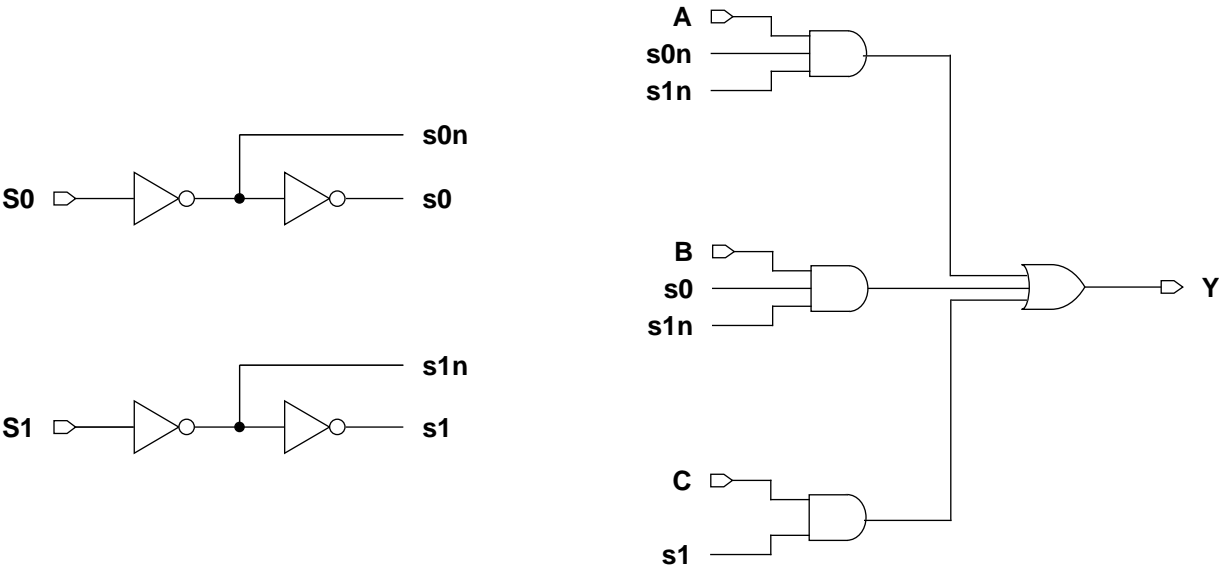
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
S0	0.0072	0.0092	0.0132	0.0170
S1	0.0056	0.0069	0.0093	0.0125
A	0.0065	0.0084	0.0120	0.0165
B	0.0071	0.0091	0.0133	0.0179
C	0.0052	0.0065	0.0104	0.0144

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
S0	0.0029	0.0034	0.0055	0.0055
S1	0.0029	0.0032	0.0041	0.0044
A	0.0015	0.0020	0.0028	0.0028
B	0.0015	0.0019	0.0027	0.0027
C	0.0011	0.0014	0.0024	0.0028

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
S0	→	Y	↑	0.0835	0.0824	0.0808	0.0888	5.7220	3.6259	2.3264	1.1995
S0	→	Y	↓	0.0921	0.0889	0.0807	0.0929	5.1167	3.5266	1.5578	0.7995
S1	→	Y	↑	0.0639	0.0627	0.0597	0.0669	5.7088	3.6234	2.3246	1.1997
S1	→	Y	↓	0.0629	0.0627	0.0522	0.0628	4.6078	3.2942	1.4407	0.7816
A	→	Y	↑	0.0707	0.0657	0.0625	0.0709	5.7253	3.6268	2.3274	1.2003
A	→	Y	↓	0.0933	0.0878	0.0789	0.0900	5.1203	3.5294	1.5608	0.8002
B	→	Y	↑	0.0695	0.0657	0.0612	0.0697	5.7233	3.6314	2.3282	1.2012
B	→	Y	↓	0.0962	0.0911	0.0831	0.0942	5.1410	3.5373	1.5647	0.8019
C	→	Y	↑	0.0539	0.0497	0.0451	0.0460	5.6009	3.5764	2.3076	1.1822
C	→	Y	↓	0.0786	0.0722	0.0626	0.0647	4.6270	3.2980	1.4242	0.7060

Cell Description

The MX4 cell is a 4-to-1 multiplexer. The state of the select inputs (S1,S0) determines which data input (A,B,C,D) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (\overline{S0} \bullet \overline{S1} \bullet A) + (S0 \bullet \overline{S1} \bullet B) + (\overline{S0} \bullet S1 \bullet C) + (S0 \bullet S1 \bullet D)$$

Logic Symbol
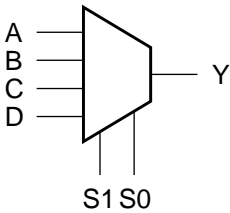
Function Table

S1	S0	A	B	C	D	Y
0	0	0	x	x	x	0
0	0	1	x	x	x	1
0	1	x	0	x	x	0
0	1	x	1	x	x	1
1	0	x	x	0	x	0
1	0	x	x	1	x	1
1	1	x	x	x	0	0
1	1	x	x	x	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
MX4XLAD	2.52	6.72
MX4X1AD	2.52	7.00
MX4X2AD	2.52	7.28
MX4X4AD	2.52	7.84

Functional Schematic
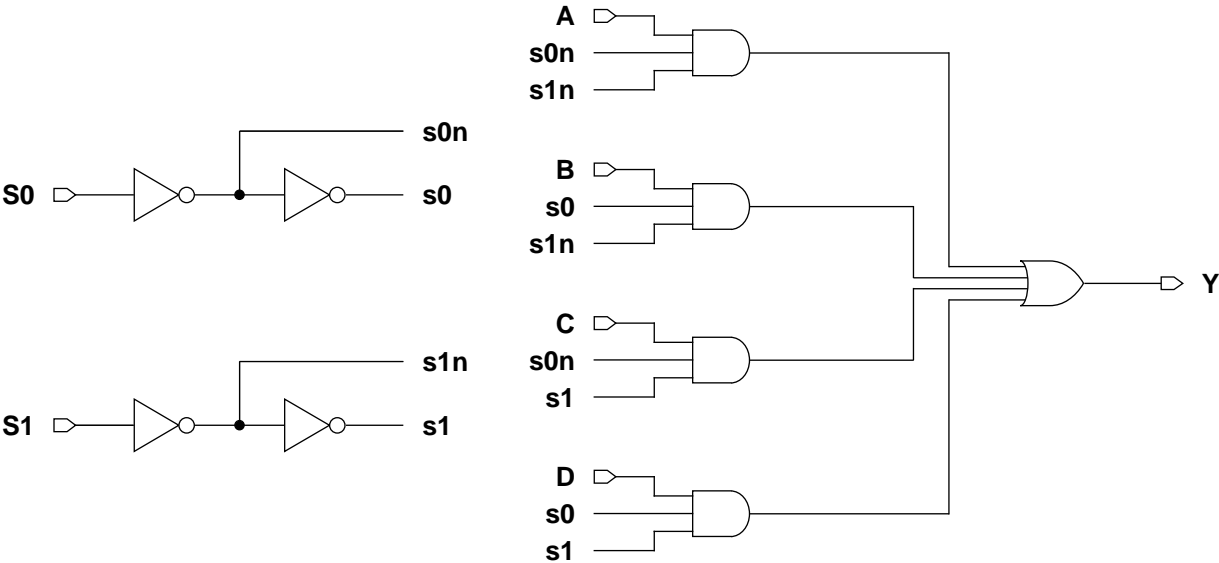
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
S0	0.0130	0.0154	0.0220	0.0268
S1	0.0057	0.0069	0.0101	0.0130
A	0.0067	0.0082	0.0124	0.0170
B	0.0072	0.0090	0.0136	0.0182
C	0.0083	0.0099	0.0147	0.0194
D	0.0086	0.0103	0.0155	0.0203

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
S0	0.0066	0.0075	0.0103	0.0103
S1	0.0033	0.0034	0.0045	0.0045
A	0.0015	0.0019	0.0027	0.0027
B	0.0015	0.0018	0.0026	0.0026
C	0.0015	0.0019	0.0028	0.0028
D	0.0014	0.0019	0.0027	0.0027

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
S0	→ Y	↑	0.0979	0.0839	0.0786	0.0870	5.7390	4.0171	2.3607	1.2013
S0	→ Y	↓	0.1176	0.1003	0.0922	0.1046	5.6968	3.5695	1.5737	0.8049
S1	→ Y	↑	0.0601	0.0627	0.0594	0.0669	5.6618	4.0443	2.3565	1.2010
S1	→ Y	↓	0.0553	0.0580	0.0548	0.0658	5.5292	3.5649	1.5588	0.8034
A	→ Y	↑	0.0683	0.0627	0.0610	0.0697	5.6730	4.0041	2.3571	1.2012
A	→ Y	↓	0.0931	0.0894	0.0798	0.0913	5.5417	3.5853	1.5641	0.8000
B	→ Y	↑	0.0683	0.0727	0.0613	0.0701	5.6733	4.0516	2.3588	1.2025
B	→ Y	↓	0.0959	0.0876	0.0821	0.0936	5.5428	3.5238	1.5642	0.7997
C	→ Y	↑	0.0742	0.0647	0.0622	0.0706	5.7334	4.0153	2.3608	1.2031
C	→ Y	↓	0.1046	0.0914	0.0862	0.0978	5.7089	3.5747	1.5760	0.8056
D	→ Y	↑	0.0713	0.0658	0.0616	0.0702	5.7167	4.0311	2.3624	1.2045
D	→ Y	↓	0.1052	0.0993	0.0888	0.1007	5.7065	3.6168	1.5817	0.8085

Cell Description

The MXI2 cell is a 2-to-1 multiplexer with inverted output. The state of the select input (S0) determines which data input (A,B) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{S0}\bullet A) + (S0 \bullet B)}$$

Logic Symbol
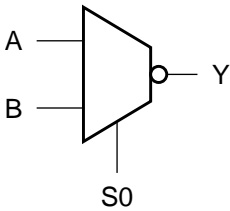
Function Table

S0	A	B	Y
0	0	x	1
0	1	x	0
1	x	0	1
1	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
MXI2XLAD	2.52	2.24
MXI2X1AD	2.52	2.24
MXI2X2AD	2.52	3.08
MXI2X3AD	2.52	4.48
MXI2X4AD	2.52	4.48
MXI2X6AD	2.52	6.16
MXI2X8AD	2.52	8.68

Functional Schematic
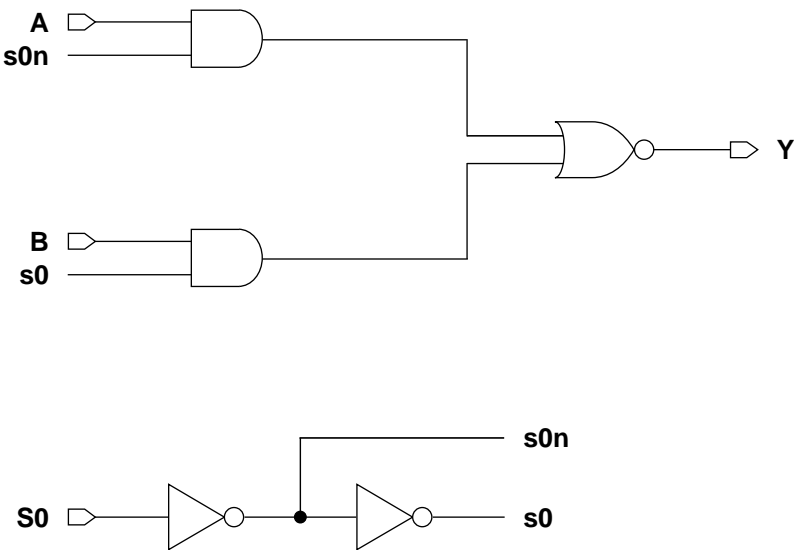
AC Power

Pin	Power (uW/MHz)						
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
S0	0.0037	0.0047	0.0072	0.0111	0.0139	0.0179	0.0254
A	0.0026	0.0034	0.0061	0.0094	0.0111	0.0162	0.0222
B	0.0031	0.0041	0.0072	0.0106	0.0127	0.0191	0.0273

Pin Capacitance

Pin	Capacitance (pF)						
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
S0	0.0027	0.0032	0.0045	0.0070	0.0080	0.0114	0.0160
A	0.0013	0.0017	0.0027	0.0044	0.0053	0.0077	0.0103
B	0.0014	0.0018	0.0027	0.0041	0.0051	0.0078	0.0104

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)						
				XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
S0	→	Y	↑	0.0268	0.0261	0.0275	0.0283	0.0288	0.0231	0.0239
S0	→	Y	↓	0.0346	0.0360	0.0361	0.0376	0.0418	0.0313	0.0323
A	→	Y	↑	0.0282	0.0245	0.0266	0.0279	0.0262	0.0256	0.0262
A	→	Y	↓	0.0252	0.0240	0.0200	0.0218	0.0209	0.0195	0.0198
B	→	Y	↑	0.0298	0.0269	0.0293	0.0291	0.0270	0.0280	0.0292
B	→	Y	↓	0.0245	0.0229	0.0183	0.0182	0.0171	0.0167	0.0176

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)						
				XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
S0	→	Y	↑	7.6837	5.0565	2.9484	1.9751	1.5738	1.0581	0.7750
S0	→	Y	↓	5.4897	3.8021	1.7019	1.1637	0.9050	0.6125	0.4398
A	→	Y	↑	7.6358	5.0264	2.9563	1.9801	1.5699	1.0642	0.7817
A	→	Y	↓	5.8943	4.0670	1.7858	1.2241	0.9513	0.6359	0.4591
B	→	Y	↑	7.5558	5.0664	2.9383	2.0071	1.5368	1.0756	0.7751
B	→	Y	↓	5.9001	4.0801	1.7761	1.2166	0.9402	0.6199	0.4504

Cell Description

The MXI2D cell is a 2-to-1 multiplexer with inverted output. The state of the select input (S0) determines which data input (A, B) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{S0} \bullet A) + (S0 \bullet B)}$$

Note: The MXI2D cell architecture uses transmission gate inputs for the data input pins and a double-buffered select signal to minimize the risk associated with transmission gate inputs. Do not drive MXI2D inputs from MXI2, ACCSHCIN, ACCSHCON, ACHCIN, ACHCON, ADDH, AFHCIN, AFHCON, AHHCIN, and AHHCON cells. Furthermore, special care should be taken in designs that use multiple voltage domains for standard cell regions. Do not allow high voltage signals to be coupled into the input pins, A and B, when the cell is used in a low voltage domain; otherwise, it may be possible for the cell to latch. If your design methodology does not permit cells with transmission gate inputs, the MXI2 cell may be used as an alternative.

Logic Symbol
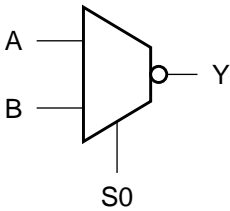
Function Table

S0	A	B	Y
0	0	x	1
0	1	x	0
1	x	0	1
1	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
MXI2DXLAD	2.52	2.80
MXI2DX1AD	2.52	2.80
MXI2DX2AD	2.52	2.80
MXI2DX4AD	2.52	4.20

Functional Schematic
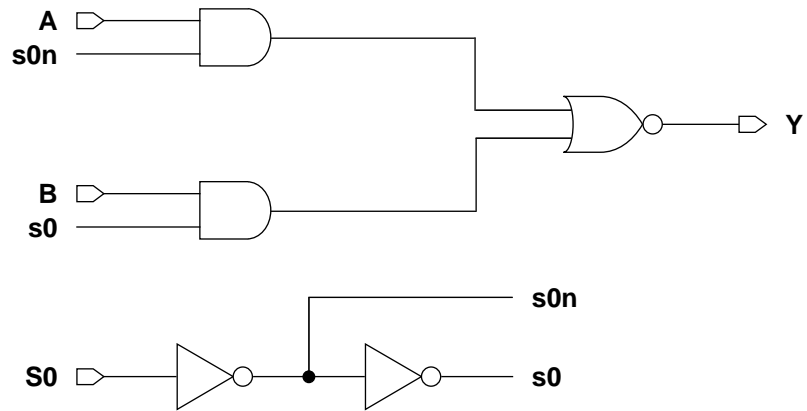
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
S0	0.0054	0.0063	0.0088	0.0157
A	0.0023	0.0030	0.0047	0.0089
B	0.0023	0.0031	0.0048	0.0092

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
S0	0.0012	0.0013	0.0016	0.0026
A	0.0035	0.0046	0.0071	0.0138
B	0.0041	0.0051	0.0076	0.0145

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
S0	→ Y	↑	0.0852	0.0871	0.0780	0.0688	5.4683	3.5578	2.2885	1.1681
S0	→ Y	↓	0.0996	0.0898	0.0774	0.0683	4.5761	3.0995	1.3165	0.6445
A	→ Y	↑	0.0265	0.0236	0.0220	0.0215	5.4680	3.5576	2.2897	1.1684
A	→ Y	↓	0.0275	0.0256	0.0211	0.0203	4.5776	3.0999	1.3155	0.6441
B	→ Y	↑	0.0280	0.0250	0.0235	0.0224	5.4698	3.5587	2.2903	1.1686
B	→ Y	↓	0.0282	0.0257	0.0209	0.0194	4.5798	3.1031	1.3214	0.6449

Cell Description

The MXI3 cell is a 3-to-1 multiplexer with inverted output. The state of the select inputs (S1,S0) determines which data input (A,B,C) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (S0 \bullet S1 \bullet \overline{A}) + (\overline{S0} \bullet S1 \bullet \overline{B}) + (\overline{S1} \bullet \overline{C})$$

Logic Symbol

A
B
C
Y
S1 S0
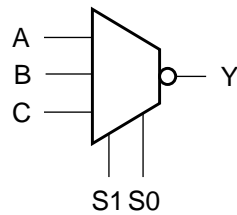
Function Table

S1	S0	A	B	C	Y
0	0	0	x	x	1
0	0	1	x	x	0
0	1	x	0	x	1
0	1	x	1	x	0
1	0	x	x	0	1
1	0	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
MXI3XLAD	2.52	5.32
MXI3X1AD	2.52	5.32
MXI3X2AD	2.52	5.60
MXI3X4AD	2.52	6.44

Functional Schematic
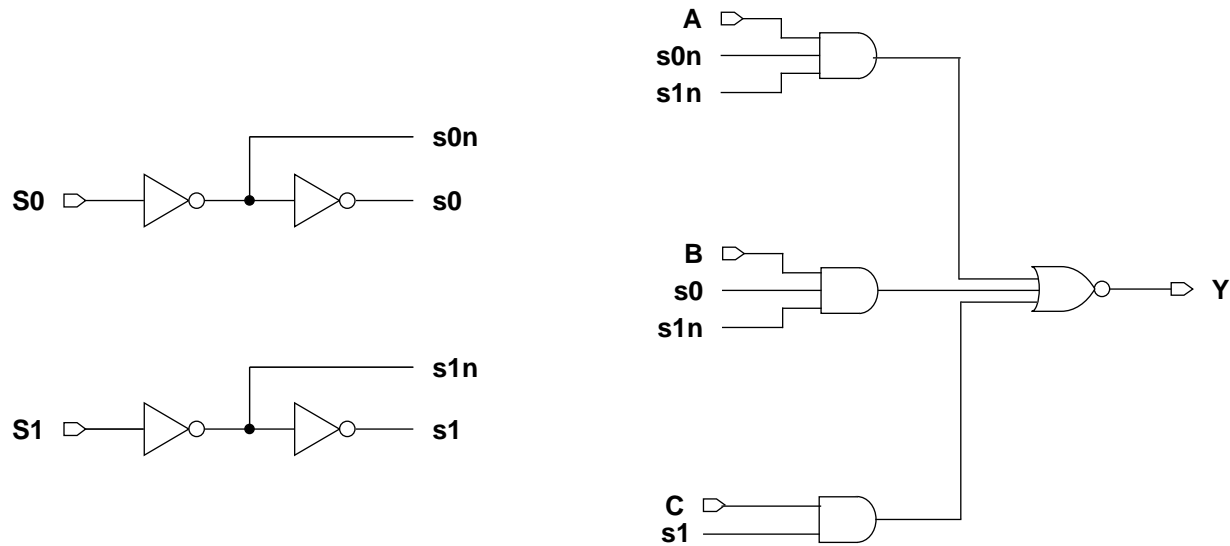
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
S0	0.0078	0.0091	0.0131	0.0190
S1	0.0050	0.0061	0.0090	0.0121
A	0.0066	0.0080	0.0118	0.0165
B	0.0067	0.0082	0.0123	0.0180
C	0.0047	0.0060	0.0090	0.0132

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
S0	0.0025	0.0026	0.0032	0.0039
S1	0.0019	0.0021	0.0025	0.0025
A	0.0013	0.0015	0.0021	0.0023
B	0.0012	0.0014	0.0020	0.0022
C	0.0013	0.0013	0.0013	0.0015

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
S0	→	Y	↑	0.1129	0.1064	0.0941	0.1069	5.7095	3.6059	2.3544	1.1845
S0	→	Y	↓	0.1261	0.1178	0.1064	0.1193	5.0584	3.2621	1.4310	0.7139
S1	→	Y	↑	0.0615	0.0603	0.0634	0.0624	5.6852	3.5946	2.3511	1.1822
S1	→	Y	↓	0.0651	0.0596	0.0532	0.0599	5.0240	3.2481	1.4260	0.7275
A	→	Y	↑	0.1251	0.1151	0.0979	0.1029	5.6997	3.6013	2.3528	1.1843
A	→	Y	↓	0.1184	0.1074	0.0878	0.0958	5.0463	3.2564	1.4293	0.7140
B	→	Y	↑	0.1201	0.1129	0.0981	0.1086	5.7077	3.6055	2.3542	1.1844
B	→	Y	↓	0.1129	0.1038	0.0851	0.0939	5.0564	3.2608	1.4305	0.7138
C	→	Y	↑	0.0783	0.0749	0.0772	0.0767	5.6745	3.5907	2.3503	1.1802
C	→	Y	↓	0.0898	0.0823	0.0743	0.0845	5.0396	3.2458	1.4259	0.7279

Cell Description

The MXI4 cell is a 4-to-1 multiplexer with inverted output. The state of the select inputs (S1,S0) determines which data input (A,B,C,D) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{S0}\bullet\overline{S1}\bullet A) + (S0\bullet\overline{S1}\bullet B) + (\overline{S0}\bullet S1\bullet C) + (S0\bullet S1\bullet D)}$$

Logic Symbol
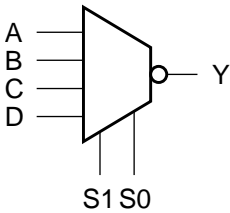
Function Table

S1	S0	A	B	C	D	Y
0	0	0	x	x	x	1
0	0	1	x	x	x	0
0	1	x	0	x	x	1
0	1	x	1	x	x	0
1	0	x	x	0	x	1
1	0	x	x	1	x	0
1	1	x	x	x	0	1
1	1	x	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
MXI4XLAD	2.52	7.00
MXI4X1AD	2.52	7.00
MXI4X2AD	2.52	7.00
MXI4X4AD	2.52	7.56

Functional Schematic
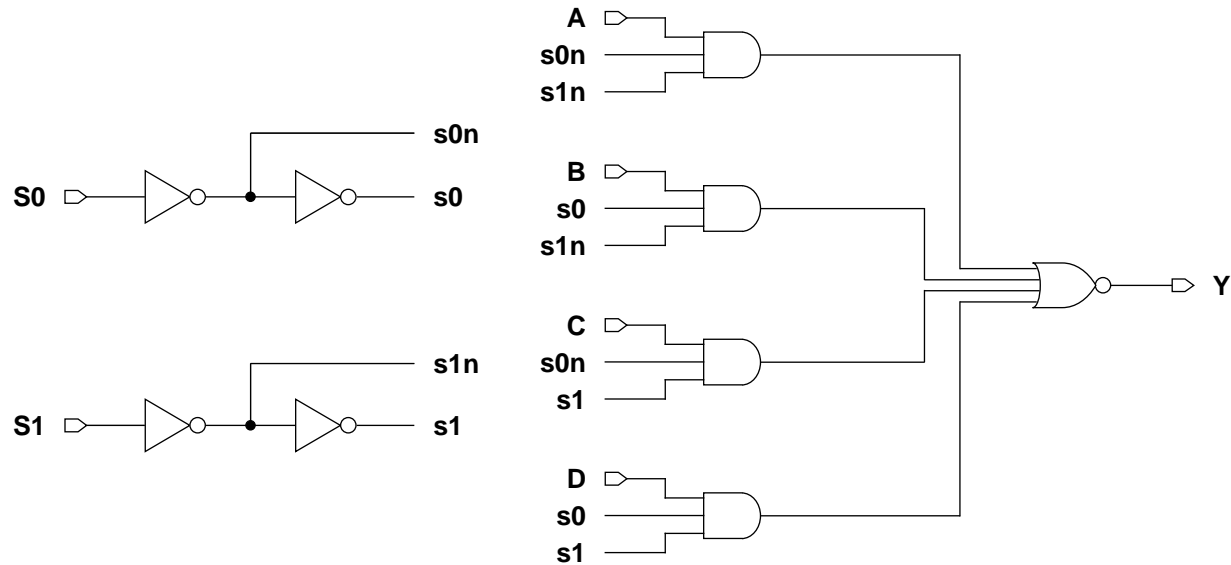
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
S0	0.0124	0.0146	0.0211	0.0275
S1	0.0053	0.0064	0.0097	0.0124
A	0.0068	0.0081	0.0121	0.0171
B	0.0073	0.0086	0.0129	0.0179
C	0.0060	0.0073	0.0111	0.0154
D	0.0064	0.0077	0.0117	0.0154

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
S0	0.0041	0.0043	0.0059	0.0069
S1	0.0020	0.0021	0.0024	0.0024
A	0.0012	0.0013	0.0020	0.0022
B	0.0012	0.0013	0.0019	0.0020
C	0.0013	0.0015	0.0021	0.0024
D	0.0012	0.0013	0.0019	0.0020

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
S0	→	Y	↑	0.1233	0.1163	0.0987	0.1083	5.6350	3.5813	2.3043	1.2109
S0	→	Y	↓	0.1436	0.1388	0.1161	0.1133	5.1866	3.3613	1.4510	0.7233
S1	→	Y	↑	0.0637	0.0621	0.0667	0.0628	5.6035	3.5694	2.3003	1.2090
S1	→	Y	↓	0.0674	0.0638	0.0561	0.0607	5.1994	3.3506	1.4270	0.7230
A	→	Y	↑	0.1205	0.1129	0.0974	0.1074	5.6367	3.5825	2.3044	1.2106
A	→	Y	↓	0.1181	0.1110	0.0950	0.0956	5.1855	3.3598	1.4498	0.7090
B	→	Y	↑	0.1256	0.1176	0.1002	0.1122	5.6390	3.5833	2.3042	1.2109
B	→	Y	↓	0.1176	0.1102	0.0936	0.0963	5.1858	3.3596	1.4497	0.7091
C	→	Y	↑	0.1135	0.1063	0.0925	0.0903	5.6278	3.5774	2.3002	1.2078
C	→	Y	↓	0.1136	0.1059	0.0882	0.0950	5.2055	3.3537	1.4284	0.7239
D	→	Y	↑	0.1138	0.1059	0.0915	0.0951	5.6281	3.5772	2.2996	1.2077
D	→	Y	↓	0.1127	0.1049	0.0881	0.0974	5.2060	3.3542	1.4284	0.7240

TSMC CLN90G

Cell Description

The NAND2 cell provides the logical NAND of two inputs (A,B). The output (Y) is represented by the logic equation:

$Y = \overline{(A \bullet B)}$

Logic Symbol

Function Table

A	B	Y
0	x	1
x	0	1
1	1	0
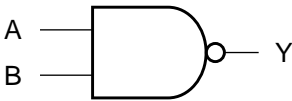
Cell Size

Drive Strength	Height (um)	Width (um)
NAND2XLAD	2.52	1.12
NAND2X1AD	2.52	1.12
NAND2X2AD	2.52	1.12
NAND2X3AD	2.52	1.96
NAND2X4AD	2.52	1.96
NAND2X5AD	2.52	2.52
NAND2X6AD	2.52	2.52
NAND2X8AD	2.52	3.36

Functional Schematic

AC Power

Pin	Power (uW/MHz)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A	0.0015	0.0020	0.0032	0.0048	0.0059	0.0077	0.0088	0.0117
B	0.0017	0.0024	0.0041	0.0064	0.0080	0.0102	0.0117	0.0157

Pin Capacitance

Pin	Capacitance (pF)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A	0.0014	0.0018	0.0029	0.0045	0.0055	0.0073	0.0084	0.0108
B	0.0012	0.0016	0.0027	0.0047	0.0057	0.0070	0.0080	0.0109

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A → Y ↑	0.0148	0.0135	0.0137	0.0140	0.0132	0.0136	0.0133	0.0135
A → Y ↓	0.0176	0.0177	0.0130	0.0122	0.0116	0.0119	0.0121	0.0119
B → Y ↑	0.0156	0.0145	0.0158	0.0167	0.0160	0.0164	0.0159	0.0161
B → Y ↓	0.0177	0.0182	0.0141	0.0142	0.0136	0.0135	0.0134	0.0135

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A → Y ↑	5.5852	3.6091	2.3407	1.6322	1.2239	0.9729	0.8147	0.6303
A → Y ↓	7.1685	5.2670	2.2261	1.3769	1.0390	0.8223	0.7264	0.5403
B → Y ↑	5.5675	3.6035	2.3379	1.5800	1.1908	0.9723	0.8138	0.6156
B → Y ↓	7.1527	5.2621	2.2246	1.3767	1.0390	0.8224	0.7261	0.5402

Cell Description

The NAND2B cell provides the logical NAND of one inverted input (AN) and one non-inverted input (B). The output (Y) is represented by the logic equation:

$Y = \overline{(\overline{AN} \bullet B)}$

Logic Symbol
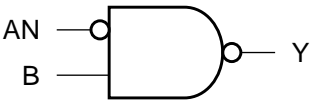
Function Table

AN	B	Y
1	x	1
x	0	1
0	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND2BXLAD	2.52	1.40
NAND2BX1AD	2.52	1.40
NAND2BX2AD	2.52	1.40
NAND2BX4AD	2.52	2.24
NAND2BX8AD	2.52	3.92

Functional Schematic
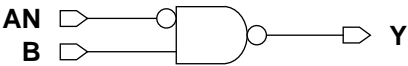
AC Power

Pin	Power (uW/MHz)				
	XL	**X1**	**X2**	**X4**	**X8**
AN	0.0026	0.0031	0.0045	0.0086	0.0163
B	0.0014	0.0019	0.0031	0.0063	0.0124

Pin Capacitance

Pin	Capacitance (pF)				
	XL	**X1**	**X2**	**X4**	**X8**
AN	0.0011	0.0011	0.0014	0.0025	0.0045
B	0.0013	0.0017	0.0027	0.0057	0.0109

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				
				XL	**X1**	**X2**	**X4**	**X8**
AN	→	Y	↑	0.0291	0.0294	0.0314	0.0304	0.0290
AN	→	Y	↓	0.0537	0.0571	0.0448	0.0424	0.0401
B	→	Y	↑	0.0151	0.0140	0.0152	0.0156	0.0158
B	→	Y	↓	0.0178	0.0183	0.0149	0.0147	0.0147

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)				
				XL	**X1**	**X2**	**X4**	**X8**
AN	→	Y	↑	5.6181	3.6270	2.3509	1.2333	0.6319
AN	→	Y	↓	7.1939	5.0253	2.1864	1.0428	0.5291
B	→	Y	↑	5.5833	3.5808	2.3673	1.2070	0.6223
B	→	Y	↓	7.1171	4.9971	2.1753	1.0381	0.5274

Cell Description

The NAND3 cell provides the logical NAND of three inputs (A,B,C). The output (Y) is represented by the logic equation:

$Y = \overline{(A \bullet B \bullet C)}$

Logic Symbol
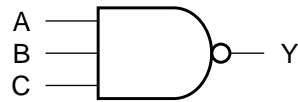
Function Table

A	B	C	Y
0	x	x	1
x	0	x	1
x	x	0	1
1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND3XLAD	2.52	1.40
NAND3X1AD	2.52	1.40
NAND3X2AD	2.52	1.68
NAND3X3AD	2.52	2.52
NAND3X4AD	2.52	2.52
NAND3X6AD	2.52	3.64
NAND3X8AD	2.52	4.76

Functional Schematic
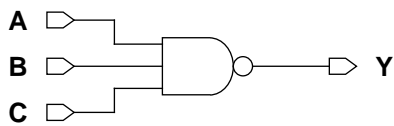
AC Power

Pin	Power (uW/MHz)						
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A	0.0017	0.0023	0.0036	0.0052	0.0065	0.0101	0.0133
B	0.0019	0.0027	0.0046	0.0069	0.0086	0.0130	0.0174
C	0.0023	0.0031	0.0055	0.0087	0.0108	0.0163	0.0219

Pin Capacitance

Pin	Capacitance (pF)						
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A	0.0014	0.0019	0.0029	0.0043	0.0053	0.0085	0.0109
B	0.0013	0.0017	0.0028	0.0046	0.0056	0.0082	0.0110
C	0.0012	0.0016	0.0026	0.0048	0.0057	0.0081	0.0114

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)						
			XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A	→ Y	↑	0.0170	0.0158	0.0158	0.0154	0.0148	0.0153	0.0153
A	→ Y	↓	0.0264	0.0261	0.0179	0.0163	0.0155	0.0163	0.0159
B	→ Y	↑	0.0187	0.0175	0.0189	0.0185	0.0178	0.0183	0.0183
B	→ Y	↓	0.0286	0.0288	0.0212	0.0201	0.0192	0.0195	0.0193
C	→ Y	↑	0.0198	0.0185	0.0206	0.0206	0.0199	0.0209	0.0211
C	→ Y	↓	0.0304	0.0306	0.0225	0.0221	0.0211	0.0215	0.0216

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)						
			XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A	→ Y	↑	5.6185	3.6316	2.3565	1.6364	1.2457	0.8240	0.6300
A	→ Y	↓	10.0089	7.0072	2.9606	1.9230	1.4497	0.9684	0.7208
B	→ Y	↑	5.7400	3.7128	2.4103	1.6212	1.2340	0.8301	0.6267
B	→ Y	↓	9.9918	7.0006	2.9599	1.9240	1.4499	0.9679	0.7208
C	→ Y	↑	5.5609	3.6052	2.3628	1.5738	1.1981	0.8278	0.6205
C	→ Y	↓	9.9976	7.0031	2.9605	1.9246	1.4502	0.9684	0.7211

Cell Description

The NAND3B cell provides the logical NAND of one inverted input (AN) and two non-inverted inputs (B,C). The output (Y) is represented by the logic equation:

$Y = \overline{(\overline{AN} \bullet B \bullet C)}$

Logic Symbol
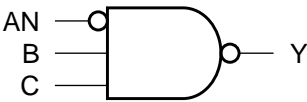
Function Table

AN	B	C	Y
1	x	x	1
x	0	x	1
x	x	0	1
0	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND3BXLAD	2.52	1.68
NAND3BX1AD	2.52	1.68
NAND3BX2AD	2.52	1.96
NAND3BX4AD	2.52	3.08

Functional Schematic
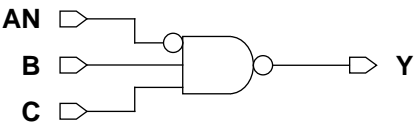
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
AN	0.0029	0.0036	0.0053	0.0092
B	0.0017	0.0023	0.0036	0.0071
C	0.0019	0.0026	0.0045	0.0093

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
AN	0.0012	0.0012	0.0014	0.0024
B	0.0013	0.0018	0.0027	0.0055
C	0.0013	0.0017	0.0026	0.0059

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
AN	→	Y	↑	0.0318	0.0329	0.0347	0.0321	5.5789	3.6013	2.3655	1.2526
AN	→	Y	↓	0.0635	0.0677	0.0517	0.0459	9.9428	6.9973	2.9544	1.4464
B	→	Y	↑	0.0181	0.0168	0.0182	0.0178	5.7048	3.6787	2.4254	1.2437
B	→	Y	↓	0.0285	0.0291	0.0221	0.0206	9.9028	6.9856	2.9506	1.4460
C	→	Y	↑	0.0194	0.0180	0.0205	0.0204	5.6108	3.5955	2.3940	1.2169
C	→	Y	↓	0.0307	0.0315	0.0239	0.0231	9.9064	6.9840	2.9500	1.4464

Cell Description

The NAND4 cell provides a logical NAND of four
inputs (A,B,C,D). The output (Y) is represented
by the logic equation:

$Y = \overline{(A \bullet B \bullet C \bullet D)}$

Logic Symbol
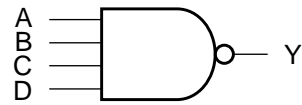
Function Table

A	B	C	D	Y
0	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
1	1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND4XLAD	2.52	1.68
NAND4X1AD	2.52	1.68
NAND4X2AD	2.52	1.96
NAND4X4AD	2.52	3.36
NAND4X6AD	2.52	5.04
NAND4X8AD	2.52	6.72

Functional Schematic
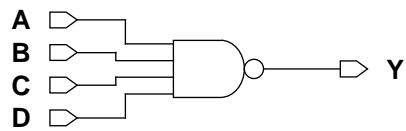
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0019	0.0026	0.0039	0.0074	0.0114	0.0151
B	0.0021	0.0030	0.0049	0.0096	0.0145	0.0193
C	0.0025	0.0035	0.0060	0.0117	0.0178	0.0237
D	0.0028	0.0039	0.0070	0.0140	0.0213	0.0284

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0014	0.0018	0.0029	0.0051	0.0087	0.0111
B	0.0013	0.0017	0.0027	0.0055	0.0085	0.0113
C	0.0013	0.0017	0.0027	0.0055	0.0085	0.0115
D	0.0012	0.0016	0.0026	0.0061	0.0088	0.0123

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	0.0181	0.0168	0.0173	0.0170	0.0176	0.0177
A	→ Y	↓	0.0352	0.0349	0.0232	0.0208	0.0216	0.0212
B	→ Y	↑	0.0202	0.0189	0.0205	0.0204	0.0208	0.0209
B	→ Y	↓	0.0390	0.0393	0.0280	0.0266	0.0267	0.0266
C	→ Y	↑	0.0221	0.0207	0.0232	0.0228	0.0238	0.0238
C	→ Y	↓	0.0430	0.0432	0.0316	0.0300	0.0305	0.0303
D	→ Y	↑	0.0221	0.0208	0.0244	0.0248	0.0266	0.0266
D	→ Y	↓	0.0441	0.0445	0.0333	0.0329	0.0333	0.0334

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)					
				XL	X1	X2	X4	X6	X8
A	$\rightarrow$	Y	$\uparrow$	5.4899	3.5599	2.3685	1.2647	0.8468	0.6504
A	$\rightarrow$	Y	$\downarrow$	12.8129	8.9885	3.7933	1.8554	1.2401	0.9249
B	$\rightarrow$	Y	$\uparrow$	5.7160	3.7087	2.4351	1.2494	0.8508	0.6436
B	$\rightarrow$	Y	$\downarrow$	12.8004	8.9844	3.7904	1.8551	1.2402	0.9246
C	$\rightarrow$	Y	$\uparrow$	5.7377	3.7189	2.4429	1.2401	0.8531	0.6417
C	$\rightarrow$	Y	$\downarrow$	12.8033	8.9855	3.7913	1.8555	1.2403	0.9248
D	$\rightarrow$	Y	$\uparrow$	5.5382	3.5864	2.3786	1.2026	0.8536	0.6370
D	$\rightarrow$	Y	$\downarrow$	12.7922	8.9798	3.7915	1.8565	1.2407	0.9251

Cell Description

The NAND4B cell provides a logical NAND of one inverted input (AN) and three non-inverted inputs (B,C,D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} \bullet B \bullet C \bullet D)}$$

Logic Symbol
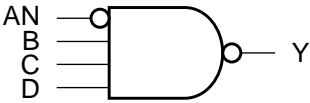
Function Table

AN	B	C	D	Y
1	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
0	1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND4BXLAD	2.52	2.24
NAND4BX1AD	2.52	2.24
NAND4BX2AD	2.52	2.24
NAND4BX4AD	2.52	3.92

Functional Schematic
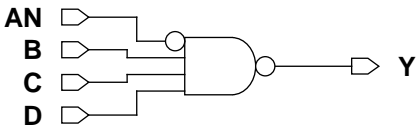
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
AN	0.0032	0.0040	0.0057	0.0103
B	0.0018	0.0025	0.0039	0.0080
C	0.0021	0.0029	0.0049	0.0099
D	0.0025	0.0034	0.0059	0.0123

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
AN	0.0012	0.0012	0.0015	0.0024
B	0.0013	0.0017	0.0027	0.0053
C	0.0013	0.0017	0.0027	0.0056
D	0.0013	0.0017	0.0026	0.0063

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
AN	→	Y	↑	0.0350	0.0360	0.0362	0.0343	5.6588	3.6589	2.3730	1.2802
AN	→	Y	↓	0.0754	0.0779	0.0568	0.0513	12.6868	8.9174	3.7928	1.8573
B	→	Y	↑	0.0207	0.0191	0.0196	0.0202	5.8278	3.7661	2.4431	1.2668
B	→	Y	↓	0.0404	0.0407	0.0286	0.0278	12.6591	8.9072	3.7907	1.8577
C	→	Y	↑	0.0227	0.0210	0.0226	0.0231	5.8595	3.7814	2.4522	1.2583
C	→	Y	↓	0.0444	0.0449	0.0325	0.0318	12.6600	8.9079	3.7913	1.8577
D	→	Y	↑	0.0234	0.0216	0.0242	0.0261	5.7895	3.7174	2.4130	1.2584
D	→	Y	↓	0.0454	0.0460	0.0341	0.0349	12.6623	8.9087	3.7903	1.8578

Cell Description

The NAND4BB cell provides a logical NAND of two inverted inputs (AN,BN) and two non-inverted inputs (C,D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} \bullet \overline{BN} \bullet C \bullet D)}$$

Logic Symbol
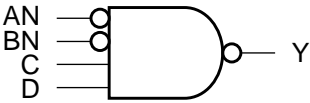
Function Table

AN	BN	C	D	Y
1	x	x	x	1
x	1	x	x	1
x	x	0	x	1
x	x	x	0	1
0	0	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND4BBXLAD	2.52	2.80
NAND4BBX1AD	2.52	2.80
NAND4BBX2AD	2.52	2.80
NAND4BBX4AD	2.52	4.48

Functional Schematic
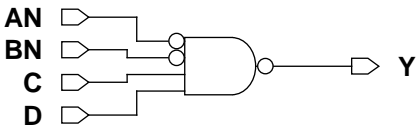
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
AN	0.0034	0.0043	0.0060	0.0109
BN	0.0033	0.0042	0.0063	0.0120
C	0.0018	0.0025	0.0042	0.0084
D	0.0021	0.0029	0.0051	0.0105

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
AN	0.0011	0.0011	0.0014	0.0023
BN	0.0010	0.0010	0.0014	0.0023
C	0.0013	0.0017	0.0027	0.0056
D	0.0013	0.0017	0.0027	0.0063

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
AN	→	Y	↑	0.0365	0.0379	0.0380	0.0355	5.6551	3.6466	2.3722	1.2786
AN	→	Y	↓	0.0777	0.0825	0.0584	0.0517	12.8833	9.0186	3.8036	1.8635
BN	→	Y	↑	0.0355	0.0369	0.0387	0.0380	5.8113	3.7491	2.4382	1.2650
BN	→	Y	↓	0.0747	0.0804	0.0602	0.0573	12.8847	9.0299	3.8104	1.8674
C	→	Y	↑	0.0219	0.0206	0.0222	0.0226	5.8317	3.7586	2.4434	1.2545
C	→	Y	↓	0.0444	0.0461	0.0336	0.0327	12.8569	9.0075	3.8040	1.8648
D	→	Y	↑	0.0227	0.0214	0.0239	0.0253	5.6821	3.6764	2.3885	1.2279
D	→	Y	↓	0.0465	0.0482	0.0357	0.0362	12.8549	9.0105	3.8044	1.8662

Cell Description

The NOR2 cell provides a logical NOR of two inputs (A,B). The output (Y) is represented by the logic equation:

$Y = \overline{(A + B)}$

Logic Symbol

A ——⊃o— Y
B
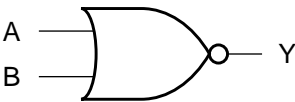
Function Table

A	B	Y
0	0	1
x	1	0
1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR2XLAD	2.52	1.12
NOR2X1AD	2.52	1.12
NOR2X2AD	2.52	1.12
NOR2X3AD	2.52	1.96
NOR2X4AD	2.52	1.96
NOR2X5AD	2.52	2.52
NOR2X6AD	2.52	2.52
NOR2X8AD	2.52	3.36

Functional Schematic

A
B ———⊃o——⊳ Y
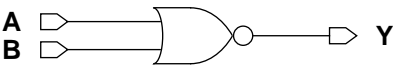
AC Power

Pin	Power (uW/MHz)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A	0.0015	0.0020	0.0034	0.0050	0.0065	0.0085	0.0098	0.0130
B	0.0019	0.0026	0.0042	0.0064	0.0083	0.0106	0.0123	0.0166

Pin Capacitance

Pin	Capacitance (pF)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A	0.0014	0.0018	0.0029	0.0042	0.0054	0.0072	0.0084	0.0108
B	0.0013	0.0017	0.0026	0.0045	0.0055	0.0069	0.0078	0.0110

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A $\rightarrow$ Y $\uparrow$	0.0220	0.0193	0.0204	0.0197	0.0194	0.0208	0.0201	0.0199
A $\rightarrow$ Y $\downarrow$	0.0121	0.0116	0.0095	0.0088	0.0089	0.0092	0.0090	0.0089
B $\rightarrow$ Y $\uparrow$	0.0255	0.0230	0.0242	0.0251	0.0242	0.0255	0.0246	0.0250
B $\rightarrow$ Y $\downarrow$	0.0135	0.0133	0.0104	0.0104	0.0102	0.0103	0.0102	0.0102

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A $\rightarrow$ Y $\uparrow$	10.9023	7.0359	4.5274	3.1285	2.3411	1.9287	1.5941	1.2067
A $\rightarrow$ Y $\downarrow$	4.2448	2.9610	1.2601	0.8116	0.6229	0.4982	0.4139	0.3092
B $\rightarrow$ Y $\uparrow$	10.8713	7.0197	4.5209	3.1271	2.3412	1.9262	1.5924	1.2060
B $\rightarrow$ Y $\downarrow$	4.2560	2.9695	1.2542	0.8239	0.6224	0.4990	0.4145	0.3106

Cell Description

The NOR2B cell provides a logical NOR of one inverted input (AN) and one non-inverted input (B). The output (Y) is represented by the logic equation:

$Y = \overline{(\overline{AN} + B)}$

Logic Symbol
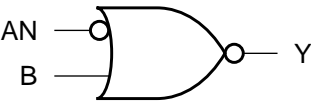
Function Table

AN	B	Y
1	0	1
x	1	0
0	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR2BXLAD	2.52	1.40
NOR2BX1AD	2.52	1.40
NOR2BX2AD	2.52	1.68
NOR2BX4AD	2.52	2.24
NOR2BX8AD	2.52	4.20

Functional Schematic
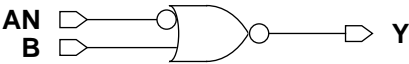
AC Power

Pin	Power (uW/MHz)				
	XL	**X1**	**X2**	**X4**	**X8**
AN	0.0022	0.0028	0.0044	0.0079	0.0155
B	0.0018	0.0025	0.0042	0.0084	0.0168

Pin Capacitance

Pin	Capacitance (pF)				
	XL	**X1**	**X2**	**X4**	**X8**
AN	0.0011	0.0011	0.0014	0.0024	0.0045
B	0.0013	0.0017	0.0027	0.0057	0.0109

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				
			XL	**X1**	**X2**	**X4**	**X8**
AN	$\rightarrow$ Y	$\uparrow$	0.0335	0.0345	0.0381	0.0359	0.0355
AN	$\rightarrow$ Y	$\downarrow$	0.0461	0.0510	0.0428	0.0395	0.0384
B	$\rightarrow$ Y	$\uparrow$	0.0251	0.0236	0.0257	0.0259	0.0265
B	$\rightarrow$ Y	$\downarrow$	0.0127	0.0129	0.0102	0.0101	0.0100

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)				
			XL	**X1**	**X2**	**X4**	**X8**
AN	$\rightarrow$ Y	$\uparrow$	11.0116	7.0964	4.5990	2.3641	1.2229
AN	$\rightarrow$ Y	$\downarrow$	4.4161	3.0569	1.3049	0.6425	0.3188
B	$\rightarrow$ Y	$\uparrow$	10.9982	7.0827	4.5939	2.3633	1.2224
B	$\rightarrow$ Y	$\downarrow$	4.1890	2.9363	1.2438	0.6182	0.3094

Cell Description

The NOR3 cell provides a logical NOR of three inputs (A,B,C). The output (Y) is represented by the logic equation:

$Y = \overline{(A + B + C)}$

Logic Symbol
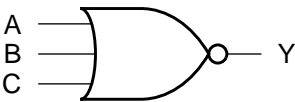
Function Table

A	B	C	Y
0	0	0	1
x	x	1	0
x	1	x	0
1	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR3XLAD	2.52	1.40
NOR3X1AD	2.52	1.40
NOR3X2AD	2.52	1.68
NOR3X4AD	2.52	2.52
NOR3X6AD	2.52	3.92
NOR3X8AD	2.52	5.32

Functional Schematic
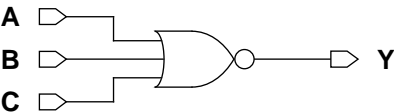
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0019	0.0025	0.0042	0.0082	0.0121	0.0162
B	0.0022	0.0030	0.0050	0.0100	0.0145	0.0195
C	0.0027	0.0036	0.0059	0.0118	0.0171	0.0232

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0014	0.0018	0.0029	0.0052	0.0087	0.0110
B	0.0013	0.0017	0.0027	0.0055	0.0081	0.0109
C	0.0012	0.0016	0.0026	0.0057	0.0080	0.0113

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	0.0342	0.0291	0.0315	0.0298	0.0309	0.0306
A	→ Y	↓	0.0135	0.0128	0.0103	0.0097	0.0099	0.0097
B	→ Y	↑	0.0440	0.0387	0.0415	0.0421	0.0414	0.0420
B	→ Y	↓	0.0150	0.0147	0.0114	0.0112	0.0110	0.0110
C	→ Y	↑	0.0486	0.0430	0.0454	0.0471	0.0463	0.0478
C	→ Y	↓	0.0160	0.0158	0.0119	0.0118	0.0116	0.0116

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	16.7581	10.6999	6.9045	3.5685	2.4342	1.8488
A	→ Y	↓	4.2327	2.9479	1.2497	0.6090	0.4143	0.3084
B	→ Y	↑	16.7140	10.6803	6.8959	3.5669	2.4307	1.8467
B	→ Y	↓	4.1857	2.9113	1.2379	0.6139	0.4137	0.3101
C	→ Y	↑	16.7124	10.6783	6.8948	3.5669	2.4313	1.8476
C	→ Y	↓	4.3212	2.9926	1.2613	0.6314	0.4244	0.3172

Cell Description

The NOR3B cell provides a logical NOR of one inverted input (AN) and two non-inverted inputs (B,C). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + B + C)}$$

Logic Symbol

AN ○
B
C — Y
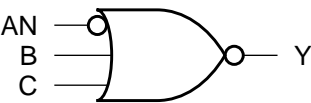
Function Table

AN	B	C	Y
1	0	0	1
x	x	1	0
x	1	x	0
0	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR3BXLAD	2.52	1.68
NOR3BX1AD	2.52	1.68
NOR3BX2AD	2.52	1.96
NOR3BX4AD	2.52	3.08

Functional Schematic

AN
B — **Y**
C
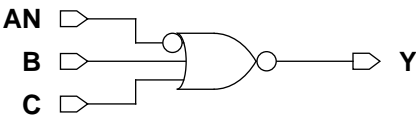
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
AN	0.0029	0.0033	0.0045	0.0083
B	0.0022	0.0029	0.0051	0.0100
C	0.0025	0.0035	0.0059	0.0118

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
AN	0.0011	0.0011	0.0014	0.0024
B	0.0012	0.0016	0.0026	0.0054
C	0.0012	0.0016	0.0026	0.0058

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
AN	→	Y	↑	0.0499	0.0465	0.0494	0.0473	16.7955	10.7773	6.9894	3.6235
AN	→	Y	↓	0.0526	0.0578	0.0440	0.0412	4.4073	3.0516	1.2931	0.6295
B	→	Y	↑	0.0430	0.0387	0.0434	0.0430	16.7409	10.7555	6.9804	3.6202
B	→	Y	↓	0.0143	0.0141	0.0114	0.0109	4.1599	2.9026	1.2365	0.6128
C	→	Y	↑	0.0475	0.0430	0.0476	0.0485	16.7328	10.7521	6.9784	3.6220
C	→	Y	↓	0.0151	0.0152	0.0118	0.0117	4.2343	2.9608	1.2510	0.6258

Cell Description

The NOR4 cell provides a logical NOR of four inputs (A,B,C,D). The output (Y) is represented by the logic equation:

$Y = \overline{(A + B + C + D)}$

Logic Symbol
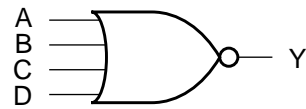
Function Table

A	B	C	D	Y
0	0	0	0	1
x	x	x	1	0
x	x	1	x	0
x	1	x	x	0
1	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR4XLAD	2.52	1.68
NOR4X1AD	2.52	1.68
NOR4X2AD	2.52	2.80
NOR4X4AD	2.52	5.60
NOR4X6AD	2.52	8.68
NOR4X8AD	2.52	11.48

Functional Schematic
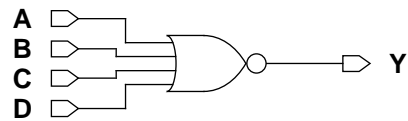
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0023	0.0029	0.0061	0.0126	0.0211	0.0290
B	0.0027	0.0034	0.0078	0.0161	0.0279	0.0384
C	0.0031	0.0040	0.0096	0.0196	0.0341	0.0470
D	0.0035	0.0045	0.0114	0.0229	0.0402	0.0556

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0014	0.0018	0.0040	0.0086	0.0134	0.0184
B	0.0014	0.0017	0.0043	0.0088	0.0129	0.0178
C	0.0014	0.0017	0.0047	0.0094	0.0128	0.0177
D	0.0013	0.0017	0.0048	0.0094	0.0127	0.0176

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	0.0432	0.0386	0.0243	0.0267	0.0240	0.0237
A	→ Y	↓	0.0150	0.0138	0.0127	0.0131	0.0136	0.0136
B	→ Y	↑	0.0612	0.0563	0.0421	0.0453	0.0450	0.0450
B	→ Y	↓	0.0171	0.0159	0.0157	0.0161	0.0175	0.0176
C	→ Y	↑	0.0707	0.0658	0.0534	0.0579	0.0570	0.0570
C	→ Y	↓	0.0180	0.0169	0.0175	0.0181	0.0193	0.0194
D	→ Y	↑	0.0749	0.0698	0.0583	0.0625	0.0617	0.0618
D	→ Y	↓	0.0184	0.0174	0.0181	0.0185	0.0194	0.0195

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)					
				XL	X1	X2	X4	X6	X8
A	→	Y	↑	20.4708	14.5708	4.8154	2.5057	1.4819	1.0785
A	→	Y	↓	4.2535	2.9661	1.2614	0.6252	0.4109	0.3001
B	→	Y	↑	20.4265	14.5550	4.8082	2.5014	1.4787	1.0762
B	→	Y	↓	4.1483	2.8952	1.2393	0.6187	0.4105	0.3005
C	→	Y	↑	20.4083	14.5448	4.8078	2.5051	1.4796	1.0760
C	→	Y	↓	4.2244	2.9333	1.2629	0.6309	0.4203	0.3081
D	→	Y	↑	20.4045	14.5433	4.8105	2.5044	1.4793	1.0767
D	→	Y	↓	4.4501	3.0674	1.3166	0.6580	0.4365	0.3197

Cell Description

The NOR4B cell provides a logical NOR of one inverted input (AN) and three non-inverted inputs (B,C,D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + B + C + D)}$$

Logic Symbol
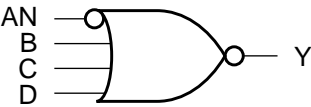
Function Table

AN	B	C	D	Y
1	0	0	0	1
x	x	x	1	0
x	x	1	x	0
x	1	x	x	0
0	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR4BXLAD	2.52	2.24
NOR4BX1AD	2.52	2.24
NOR4BX2AD	2.52	3.36
NOR4BX4AD	2.52	3.36

Functional Schematic
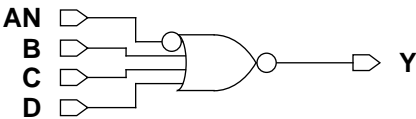
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
AN	0.0027	0.0031	0.0064	0.0081
B	0.0026	0.0034	0.0079	0.0098
C	0.0030	0.0039	0.0095	0.0114
D	0.0034	0.0045	0.0115	0.0133

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
AN	0.0011	0.0012	0.0021	0.0028
B	0.0013	0.0017	0.0042	0.0052
C	0.0013	0.0016	0.0044	0.0048
D	0.0013	0.0016	0.0049	0.0053

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
AN	→	Y	↑	0.0583	0.0546	0.0397	0.0485	20.7112	14.6615	4.8812	4.8851
AN	→	Y	↓	0.0549	0.0493	0.0429	0.0377	4.4012	3.0034	1.2828	0.7936
B	→	Y	↑	0.0593	0.0550	0.0433	0.0534	20.6522	14.6368	4.8726	4.8833
B	→	Y	↓	0.0163	0.0153	0.0155	0.0111	4.1508	2.8891	1.2400	0.6369
C	→	Y	↑	0.0706	0.0657	0.0542	0.0631	20.6442	14.6301	4.8744	4.8778
C	→	Y	↓	0.0174	0.0164	0.0172	0.0165	4.2131	2.9204	1.2622	1.0017
D	→	Y	↑	0.0747	0.0697	0.0605	0.0696	20.6365	14.6285	4.8806	4.8812
D	→	Y	↓	0.0172	0.0166	0.0183	0.0174	4.3030	2.9996	1.3163	1.0311

Cell Description

The NOR4BB cell provides a logical NOR of two inverted inputs (AN,BN) and two non-inverted inputs (C,D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + \overline{BN} + C + D)}$$

Logic Symbol
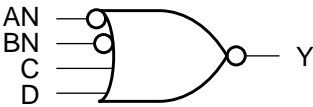
Function Table

AN	BN	C	D	Y
1	1	0	0	1
x	x	x	1	0
x	x	1	x	0
x	0	x	x	0
0	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR4BBXLAD	2.52	2.80
NOR4BBX1AD	2.52	2.80
NOR4BBX2AD	2.52	3.92
NOR4BBX4AD	2.52	3.92

Functional Schematic
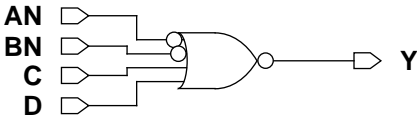
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
AN	0.0029	0.0035	0.0067	0.0077
BN	0.0029	0.0035	0.0082	0.0094
C	0.0030	0.0039	0.0098	0.0111
D	0.0034	0.0044	0.0117	0.0130

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
AN	0.0011	0.0012	0.0021	0.0023
BN	0.0011	0.0012	0.0020	0.0023
C	0.0013	0.0017	0.0044	0.0047
D	0.0013	0.0017	0.0049	0.0052

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
AN	→	Y	↑	0.0586	0.0571	0.0411	0.0554	20.3263	14.6133	4.8758	4.9140
AN	→	Y	↓	0.0595	0.0537	0.0431	0.0359	4.4364	3.0111	1.2791	0.8232
BN	→	Y	↑	0.0726	0.0714	0.0600	0.0651	20.2554	14.5802	4.8708	4.9031
BN	→	Y	↓	0.0566	0.0515	0.0498	0.0540	4.3082	2.9484	1.2624	1.1907
C	→	Y	↑	0.0689	0.0659	0.0563	0.0634	20.2554	14.5776	4.8706	4.9052
C	→	Y	↓	0.0173	0.0164	0.0174	0.0162	4.2476	2.9365	1.2620	1.0057
D	→	Y	↑	0.0730	0.0700	0.0628	0.0697	20.2491	14.5744	4.8756	4.9068
D	→	Y	↓	0.0176	0.0169	0.0186	0.0169	4.4410	3.0566	1.3153	1.0213

Cell Description

The OA21 cell provides the logical AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = (A0 + A1) \bullet B0$$

Logic Symbol
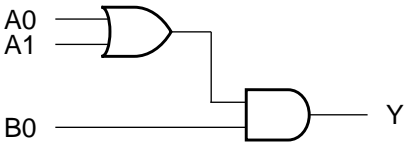
Function Table

A0	A1	B0	Y
x	x	0	0
0	0	x	0
x	1	1	1
1	x	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
OA21XLAD	2.52	1.68
OA21X1AD	2.52	1.68
OA21X2AD	2.52	2.24
OA21X4AD	2.52	2.52

Functional Schematic
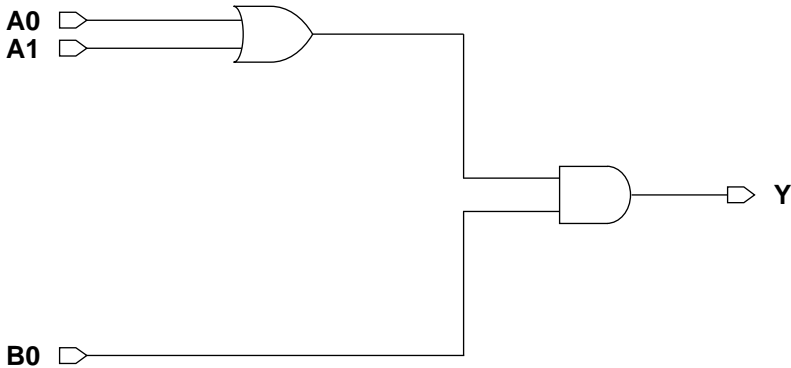
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0036	0.0043	0.0064	0.0116
A1	0.0038	0.0045	0.0068	0.0123
B0	0.0027	0.0032	0.0050	0.0090

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0010	0.0010	0.0015	0.0025
A1	0.0009	0.0009	0.0014	0.0024
B0	0.0012	0.0012	0.0016	0.0027

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→ Y	↑	0.0437	0.0462	0.0397	0.0387	5.5546	3.5395	2.3300	1.2078
A0	→ Y	↓	0.1072	0.1163	0.0913	0.0822	5.2254	3.4976	1.4863	0.7197
A1	→ Y	↑	0.0464	0.0492	0.0426	0.0419	5.5762	3.5512	2.3353	1.2102
A1	→ Y	↓	0.1113	0.1204	0.0958	0.0868	5.2251	3.4977	1.4865	0.7198
B0	→ Y	↑	0.0426	0.0454	0.0394	0.0386	5.5758	3.5507	2.3352	1.2102
B0	→ Y	↓	0.0552	0.0604	0.0488	0.0439	4.7291	3.2265	1.3810	0.6702

Cell Description

The OA22 cell provides the logical AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = (A0 + A1) \bullet (B0 + B1)$$

Logic Symbol
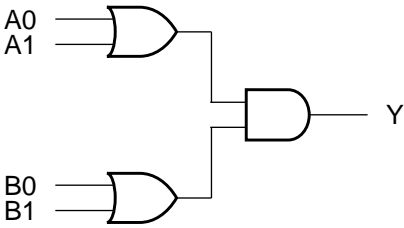
Function Table

A0	A1	B0	B1	Y
x	x	0	0	0
0	0	x	x	0
x	1	x	1	1
x	1	1	x	1
1	x	x	1	1
1	x	1	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
OA22XLAD	2.52	2.24
OA22X1AD	2.52	2.24
OA22X2AD	2.52	2.52
OA22X4AD	2.52	3.08

Functional Schematic
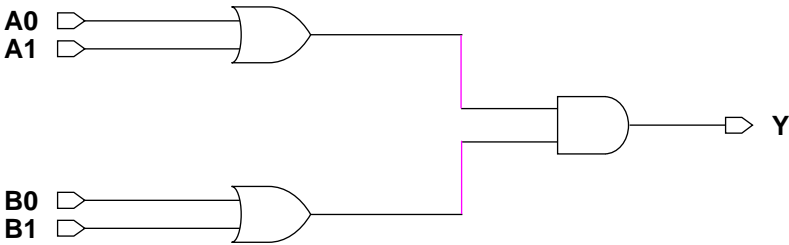
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0032	0.0039	0.0062	0.0111
A1	0.0034	0.0042	0.0067	0.0120
B0	0.0044	0.0051	0.0080	0.0142
B1	0.0046	0.0054	0.0085	0.0151

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0011	0.0012	0.0017	0.0028
A1	0.0010	0.0011	0.0016	0.0027
B0	0.0012	0.0013	0.0017	0.0028
B1	0.0011	0.0011	0.0017	0.0027

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0433	0.0479	0.0443	0.0431	5.6772	3.6453	2.3673	1.2252
A0	→	Y	↓	0.0940	0.0915	0.0749	0.0674	5.3263	3.4675	1.4938	0.7255
A1	→	Y	↑	0.0455	0.0509	0.0476	0.0464	5.6941	3.6562	2.3713	1.2275
A1	→	Y	↓	0.0981	0.0957	0.0795	0.0719	5.3261	3.4677	1.4937	0.7255
B0	→	Y	↑	0.0508	0.0557	0.0507	0.0488	5.6832	3.6498	2.3690	1.2258
B0	→	Y	↓	0.1269	0.1175	0.0962	0.0854	5.5339	3.5622	1.5369	0.7450
B1	→	Y	↑	0.0526	0.0578	0.0538	0.0520	5.6868	3.6533	2.3714	1.2272
B1	→	Y	↓	0.1310	0.1218	0.1019	0.0908	5.5321	3.5608	1.5368	0.7450

Cell Description

The OAI21 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet B0}$$

Logic Symbol
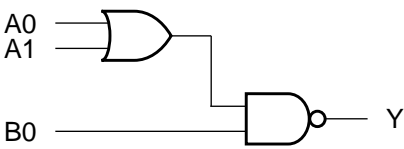
Function Table

A0	A1	B0	Y
0	0	x	1
x	x	0	1
x	1	1	0
1	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI21XLAD	2.52	1.40
OAI21X1AD	2.52	1.40
OAI21X2AD	2.52	1.68
OAI21X3AD	2.52	2.52
OAI21X4AD	2.52	2.52
OAI21X6AD	2.52	3.64
OAI21X8AD	2.52	4.76

Functional Schematic
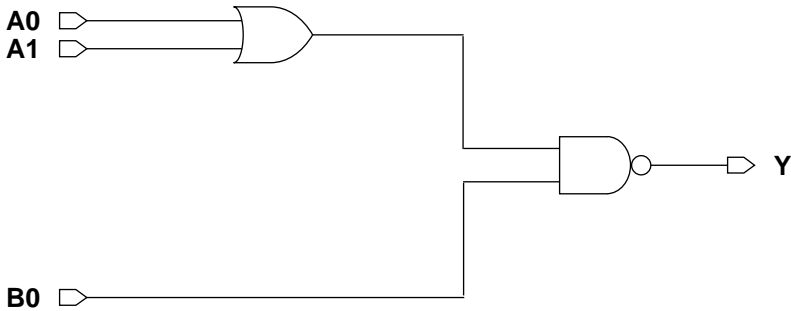
AC Power

Pin	Power (uW/MHz)						
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A0	0.0021	0.0028	0.0050	0.0076	0.0095	0.0144	0.0189
A1	0.0025	0.0034	0.0059	0.0091	0.0114	0.0170	0.0225
B0	0.0018	0.0025	0.0039	0.0058	0.0073	0.0114	0.0146

Pin Capacitance

Pin	Capacitance (pF)						
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A0	0.0013	0.0017	0.0027	0.0042	0.0052	0.0081	0.0106
A1	0.0012	0.0016	0.0026	0.0043	0.0054	0.0079	0.0106
B0	0.0014	0.0018	0.0029	0.0043	0.0053	0.0078	0.0104

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)						
			XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A0	→ Y	↑	0.0309	0.0273	0.0314	0.0328	0.0305	0.0319	0.0310
A0	→ Y	↓	0.0209	0.0203	0.0157	0.0159	0.0151	0.0156	0.0150
A1	→ Y	↑	0.0357	0.0318	0.0361	0.0379	0.0357	0.0369	0.0362
A1	→ Y	↓	0.0251	0.0248	0.0186	0.0185	0.0178	0.0180	0.0176
B0	→ Y	↑	0.0147	0.0137	0.0139	0.0140	0.0133	0.0139	0.0135
B0	→ Y	↓	0.0216	0.0217	0.0151	0.0147	0.0142	0.0147	0.0142

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)						
			XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A0	→ Y	↑	11.2214	7.1778	4.7042	3.2212	2.3946	1.6291	1.2294
A0	→ Y	↓	7.0819	4.9557	2.0843	1.3794	1.0459	0.6991	0.5214
A1	→ Y	↑	11.2064	7.1692	4.7038	3.2193	2.3932	1.6278	1.2285
A1	→ Y	↓	7.1984	5.0403	2.1248	1.3822	1.0465	0.6968	0.5221
B0	→ Y	↑	5.6250	3.6543	2.3992	1.6280	1.2176	0.8228	0.6248
B0	→ Y	↓	7.2223	5.0493	2.1274	1.3839	1.0471	0.6974	0.5225

Cell Description

The OAI211 cell provides the logical inverted OR of one OR group and two additional inputs. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet B0 \bullet C0}$$

Logic Symbol
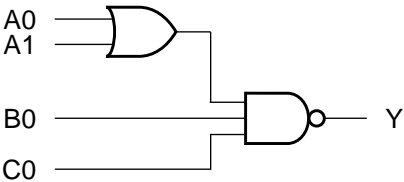
Function Table

A0	A1	B0	C0	Y
0	0	x	x	1
x	x	0	x	1
x	x	x	0	1
x	1	1	1	0
1	x	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI211XLAD	2.52	1.68
OAI211X1AD	2.52	1.68
OAI211X2AD	2.52	1.96
OAI211X4AD	2.52	3.36

Functional Schematic
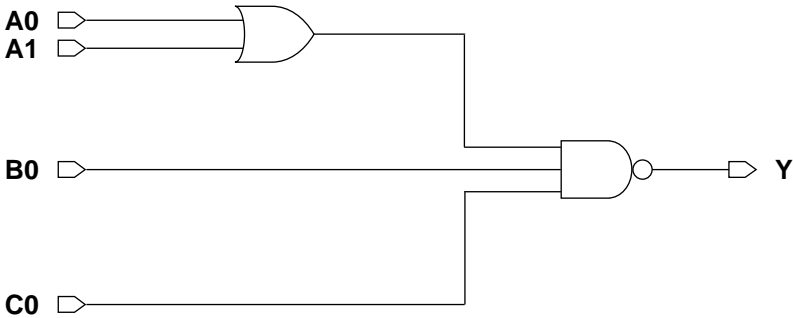
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0027	0.0037	0.0065	0.0126
A1	0.0031	0.0042	0.0074	0.0144
B0	0.0021	0.0029	0.0044	0.0084
C0	0.0023	0.0032	0.0054	0.0106

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0018	0.0028	0.0056
A1	0.0012	0.0016	0.0026	0.0050
B0	0.0015	0.0020	0.0029	0.0053
C0	0.0013	0.0017	0.0027	0.0057

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0399	0.0355	0.0413	0.0418	11.2691	7.2375	4.6910	2.4226
A0	→	Y	↓	0.0347	0.0338	0.0250	0.0246	10.1873	7.1428	2.9220	1.4587
A1	→	Y	↑	0.0442	0.0396	0.0458	0.0463	11.2596	7.2327	4.6889	2.4217
A1	→	Y	↓	0.0408	0.0403	0.0291	0.0283	10.3100	7.2356	2.9667	1.4657
B0	→	Y	↑	0.0176	0.0166	0.0162	0.0161	5.6168	3.7660	2.3772	1.2440
B0	→	Y	↓	0.0348	0.0346	0.0225	0.0212	10.3493	7.2499	2.9714	1.4677
C0	→	Y	↑	0.0191	0.0182	0.0194	0.0193	5.7639	3.8680	2.4480	1.2235
C0	→	Y	↓	0.0364	0.0367	0.0256	0.0253	10.3328	7.2471	2.9711	1.4681

Cell Description

The OAI21B cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet \overline{B0N}}$$

Logic Symbol
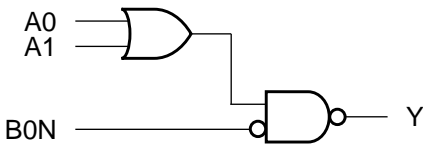
Function Table

A0	A1	B0N	Y
0	0	x	1
x	x	1	1
x	1	0	0
1	x	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI21BXLAD	2.52	1.96
OAI21BX1AD	2.52	1.96
OAI21BX2AD	2.52	2.24
OAI21BX4AD	2.52	3.36

Functional Schematic
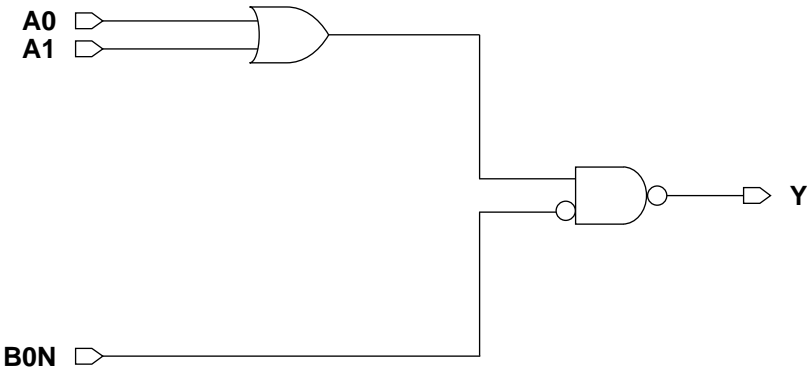
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0020	0.0026	0.0039	0.0075
A1	0.0024	0.0031	0.0048	0.0093
B0N	0.0027	0.0034	0.0050	0.0093

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0017	0.0027	0.0052
A1	0.0011	0.0015	0.0026	0.0053
B0N	0.0012	0.0012	0.0014	0.0025

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0350	0.0297	0.0309	0.0303	11.3763	7.2278	4.6960	2.4022
A0	→	Y	↓	0.0249	0.0242	0.0179	0.0174	7.2390	5.0508	2.1097	1.0524
A1	→	Y	↑	0.0389	0.0335	0.0354	0.0354	11.3551	7.2181	4.6885	2.4009
A1	→	Y	↓	0.0291	0.0287	0.0209	0.0202	7.3448	5.1215	2.1473	1.0517
B0N	→	Y	↑	0.0313	0.0322	0.0325	0.0300	5.8117	3.7382	2.4120	1.2370
B0N	→	Y	↓	0.0604	0.0648	0.0482	0.0442	7.3853	5.1401	2.1531	1.0540

Cell Description

The OAI22 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet (B0 + B1)}$$

Logic Symbol
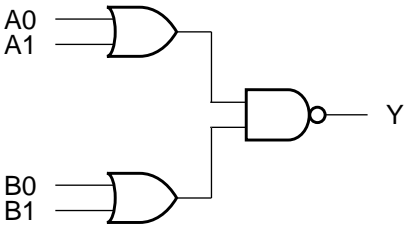
Function Table

A0	A1	B0	B1	Y
0	0	x	x	1
x	x	0	0	1
x	1	x	1	0
x	1	1	x	0
1	x	x	1	0
1	x	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI22XLAD	2.52	1.68
OAI22X1AD	2.52	1.68
OAI22X2AD	2.52	1.96
OAI22X4AD	2.52	3.36

Functional Schematic
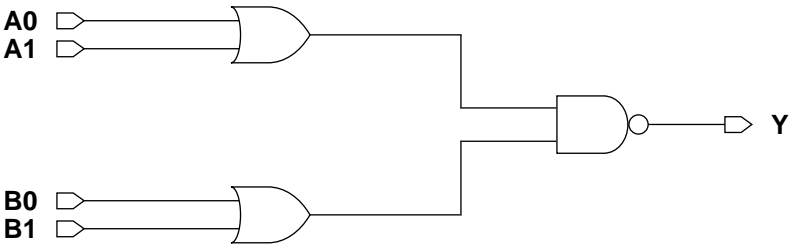
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0023	0.0030	0.0046	0.0090
A1	0.0027	0.0036	0.0055	0.0109
B0	0.0034	0.0043	0.0070	0.0136
B1	0.0038	0.0049	0.0079	0.0155

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0014	0.0018	0.0027	0.0053
A1	0.0013	0.0017	0.0026	0.0057
B0	0.0014	0.0018	0.0029	0.0053
B1	0.0013	0.0017	0.0027	0.0055

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0293	0.0249	0.0251	0.0253	11.3428	7.2812	4.7329	2.4343
A0	→	Y	↓	0.0241	0.0231	0.0161	0.0159	7.1288	4.9856	2.1139	1.0456
A1	→	Y	↑	0.0342	0.0295	0.0298	0.0309	11.3268	7.2742	4.7289	2.4337
A1	→	Y	↓	0.0289	0.0280	0.0189	0.0188	7.2642	5.0768	2.1370	1.0405
B0	→	Y	↑	0.0449	0.0372	0.0402	0.0399	11.3776	7.3327	4.7406	2.4237
B0	→	Y	↓	0.0329	0.0304	0.0215	0.0206	7.1791	4.9998	2.1190	1.0413
B1	→	Y	↑	0.0490	0.0416	0.0448	0.0452	11.3599	7.3258	4.7363	2.4225
B1	→	Y	↓	0.0371	0.0351	0.0244	0.0235	7.2673	5.0765	2.1379	1.0406

Cell Description

The OAI221 cell provides the logical inverted AND of two OR groups and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1)\bullet(B0 + B1)\bullet C0}$$

Logic Symbol

A0
A1

B0
B1

C0

Y
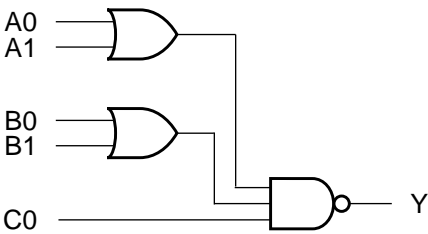
Function Table

A0	A1	B0	B1	C0	Y
0	0	x	x	x	1
x	x	0	0	x	1
x	x	x	x	0	1
x	1	x	1	1	0
x	1	1	x	1	0
1	x	x	1	1	0
1	x	1	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI221XLAD	2.52	2.52
OAI221X1AD	2.52	2.52
OAI221X2AD	2.52	2.52
OAI221X4AD	2.52	4.48

Functional Schematic

A0
A1

B0
B1

C0

Y
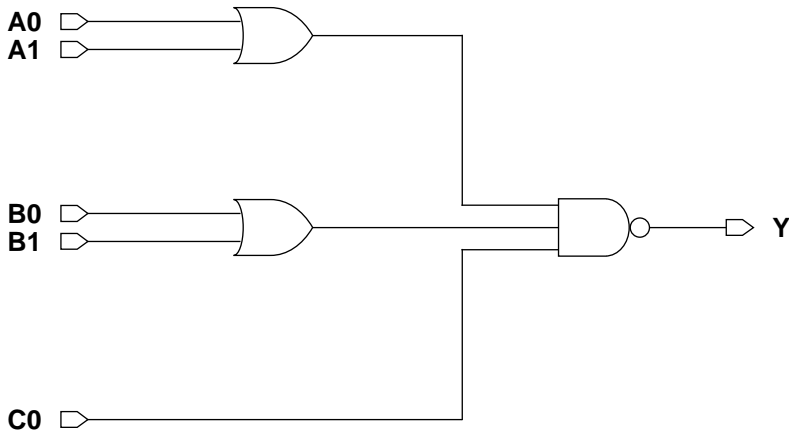
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0030	0.0039	0.0063	0.0124
A1	0.0034	0.0045	0.0073	0.0140
B0	0.0039	0.0051	0.0084	0.0168
B1	0.0043	0.0057	0.0093	0.0185
C0	0.0025	0.0034	0.0053	0.0102

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0017	0.0028	0.0057
A1	0.0013	0.0017	0.0027	0.0049
B0	0.0013	0.0016	0.0027	0.0055
B1	0.0012	0.0016	0.0026	0.0050
C0	0.0013	0.0018	0.0029	0.0053

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0447	0.0383	0.0403	0.0401	11.7695	7.5553	4.8626	2.4912
A0	→	Y	↓	0.0460	0.0441	0.0303	0.0290	10.2049	7.1478	3.0407	1.4925
A1	→	Y	↑	0.0498	0.0434	0.0453	0.0443	11.7622	7.5525	4.8607	2.4893
A1	→	Y	↓	0.0521	0.0506	0.0341	0.0327	10.1389	7.1020	3.0020	1.4997
B0	→	Y	↑	0.0533	0.0451	0.0497	0.0511	11.5741	7.3742	4.7479	2.4496
B0	→	Y	↓	0.0517	0.0489	0.0342	0.0337	10.1350	7.0915	3.0099	1.5033
B1	→	Y	↑	0.0575	0.0494	0.0542	0.0555	11.5687	7.3719	4.7462	2.4487
B1	→	Y	↓	0.0575	0.0555	0.0381	0.0375	10.1381	7.1008	3.0039	1.5000
C0	→	Y	↑	0.0192	0.0174	0.0174	0.0169	5.6755	3.7011	2.3981	1.2314
C0	→	Y	↓	0.0421	0.0420	0.0277	0.0266	10.1581	7.1129	3.0065	1.5019

Cell Description

The OAI222 cell provides the logical inverted AND of three OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1)\bullet(B0 + B1)\bullet(C0 + C1)}$$

Logic Symbol
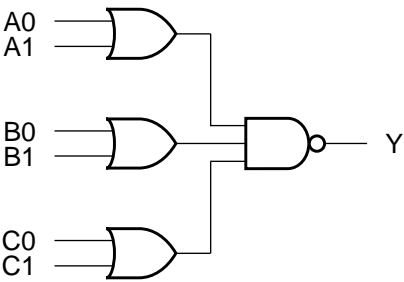
Function Table

A0	A1	B0	B1	C0	C1	Y
0	0	x	x	x	x	1
x	x	0	0	x	x	1
x	x	x	x	0	0	1
x	1	x	1	1	x	0
x	1	x	1	x	1	0
x	1	1	x	1	x	0
x	1	1	x	x	1	0
1	x	x	1	1	x	0
1	x	x	1	x	1	0
1	x	1	x	1	x	0
1	x	1	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI222XLAD	2.52	2.80
OAI222X1AD	2.52	2.80
OAI222X2AD	2.52	3.08
OAI222X4AD	2.52	5.04

Functional Schematic
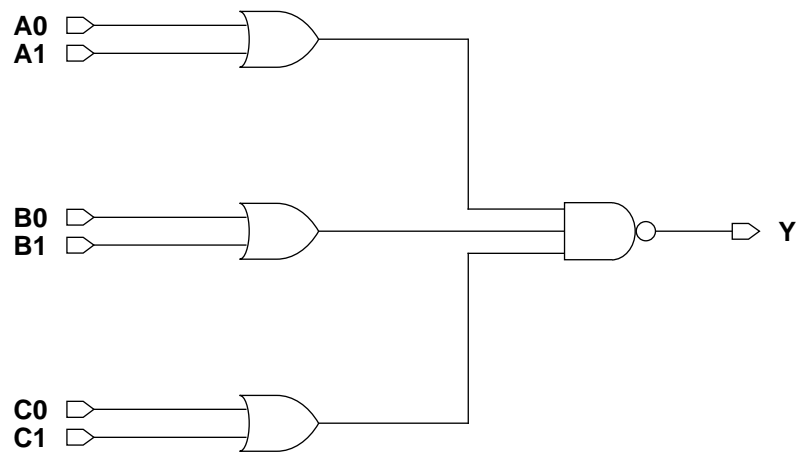
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0043	0.0054	0.0084	0.0163
A1	0.0046	0.0060	0.0093	0.0181
B0	0.0051	0.0064	0.0105	0.0208
B1	0.0055	0.0071	0.0114	0.0225
C0	0.0028	0.0038	0.0060	0.0119
C1	0.0032	0.0044	0.0068	0.0136

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0014	0.0018	0.0028	0.0056
A1	0.0013	0.0017	0.0027	0.0050
B0	0.0012	0.0017	0.0027	0.0056
B1	0.0012	0.0016	0.0026	0.0051
C0	0.0014	0.0018	0.0028	0.0058
C1	0.0013	0.0017	0.0027	0.0051

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→ Y	↑	0.0582	0.0477	0.0500	0.0489	11.9108	7.6383	4.9388	2.5129
A0	→ Y	↓	0.0619	0.0580	0.0387	0.0372	10.1701	7.1027	3.0109	1.4960
A1	→ Y	↑	0.0627	0.0522	0.0552	0.0537	11.9026	7.6345	4.9370	2.5118
A1	→ Y	↓	0.0671	0.0637	0.0423	0.0412	10.0633	7.0309	2.9726	1.4982
B0	→ Y	↑	0.0660	0.0540	0.0599	0.0612	11.5933	7.4213	4.7708	2.4642
B0	→ Y	↓	0.0667	0.0622	0.0426	0.0422	10.0960	7.0466	2.9804	1.5023
B1	→ Y	↑	0.0704	0.0584	0.0643	0.0656	11.5889	7.4192	4.7689	2.4634
B1	→ Y	↓	0.0727	0.0686	0.0464	0.0459	10.0529	7.0298	2.9709	1.4975
C0	→ Y	↑	0.0373	0.0325	0.0333	0.0336	11.6482	7.4256	4.8027	2.4679
C0	→ Y	↓	0.0435	0.0437	0.0294	0.0290	10.1297	7.0771	3.0165	1.4978
C1	→ Y	↑	0.0415	0.0368	0.0378	0.0378	11.6286	7.4181	4.7992	2.4655
C1	→ Y	↓	0.0486	0.0494	0.0327	0.0326	10.0619	7.0314	2.9683	1.4980

TSMC CLN90G

Cell Description

The OAI2B1 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + \overline{A1N}) \bullet B0}$$

Logic Symbol
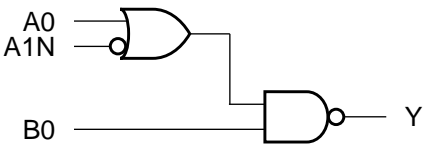
Function Table

A0	A1N	B0	Y
0	1	x	1
x	x	0	1
x	0	1	0
1	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI2B1XLAD	2.52	1.96
OAI2B1X1AD	2.52	1.96
OAI2B1X2AD	2.52	2.24
OAI2B1X4AD	2.52	3.36

Functional Schematic

TSMC CLN90G
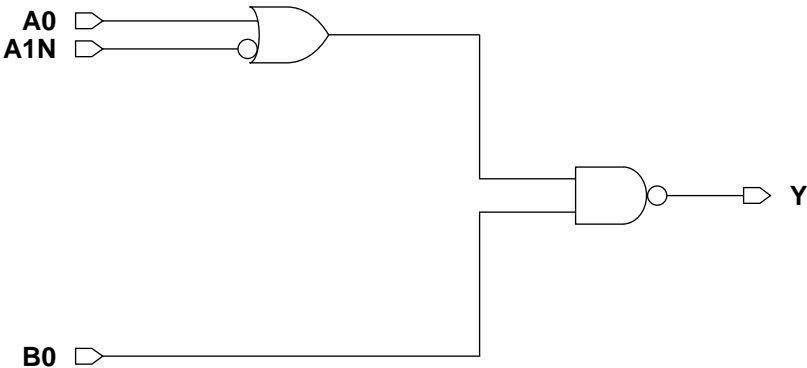
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0022	0.0029	0.0050	0.0096
A1N	0.0026	0.0035	0.0060	0.0116
B0	0.0018	0.0025	0.0038	0.0071

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0018	0.0028	0.0052
A1N	0.0012	0.0012	0.0014	0.0024
B0	0.0014	0.0018	0.0029	0.0053

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→ Y	↑	0.0323	0.0287	0.0314	0.0311	11.1863	7.2600	4.7114	2.4398
A0	→ Y	↓	0.0219	0.0211	0.0157	0.0153	7.0767	4.9469	2.0860	1.0489
A1N	→ Y	↑	0.0509	0.0491	0.0541	0.0542	11.1524	7.2473	4.7082	2.4371
A1N	→ Y	↓	0.0615	0.0656	0.0516	0.0498	7.2379	5.0591	2.1381	1.0555
B0	→ Y	↑	0.0151	0.0140	0.0138	0.0133	5.6433	3.6619	2.4040	1.2175
B0	→ Y	↓	0.0220	0.0221	0.0150	0.0142	7.2259	5.0493	2.1298	1.0512

Cell Description

The OAI2B11 cell provides the logical inverted OR of one OR group and two additional inputs. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + \overline{A1N}) \bullet B0 \bullet C0}$$

Logic Symbol
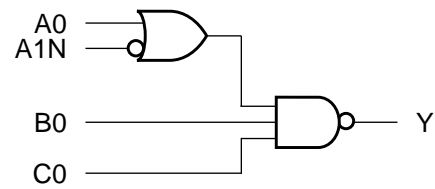
Function Table

A0	A1N	B0	C0	Y
0	1	x	x	1
x	x	0	x	1
x	x	x	0	1
x	0	1	1	0
1	x	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI2B11XLAD	2.52	2.24
OAI2B11X1AD	2.52	2.24
OAI2B11X2AD	2.52	2.24
OAI2B11X4AD	2.52	3.92

Functional Schematic
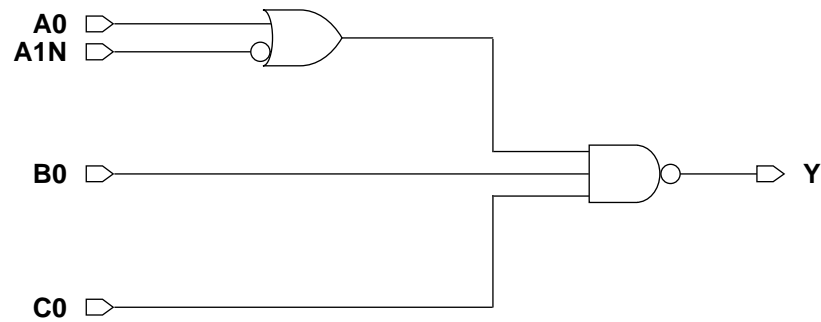
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0028	0.0037	0.0065	0.0128
A1N	0.0032	0.0042	0.0073	0.0146
B0	0.0019	0.0026	0.0043	0.0080
C0	0.0022	0.0031	0.0053	0.0103

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0017	0.0028	0.0056
A1N	0.0011	0.0012	0.0014	0.0023
B0	0.0013	0.0017	0.0029	0.0052
C0	0.0013	0.0017	0.0028	0.0057

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→ Y	↑	0.0412	0.0364	0.0416	0.0421	11.3480	7.3727	4.7447	2.4232
A0	→ Y	↓	0.0357	0.0344	0.0255	0.0247	10.2612	7.1719	3.0129	1.4594
A1N	→ Y	↑	0.0606	0.0577	0.0639	0.0641	11.3387	7.3691	4.7426	2.4226
A1N	→ Y	↓	0.0778	0.0799	0.0604	0.0572	10.3948	7.2588	3.0793	1.4690
B0	→ Y	↑	0.0170	0.0157	0.0164	0.0162	5.6790	3.6675	2.3789	1.2439
B0	→ Y	↓	0.0335	0.0337	0.0235	0.0213	10.4086	7.2630	3.0804	1.4682
C0	→ Y	↑	0.0193	0.0179	0.0195	0.0194	5.8550	3.7793	2.4495	1.2235
C0	→ Y	↓	0.0367	0.0370	0.0266	0.0254	10.4065	7.2643	3.0800	1.4687

Cell Description

The OAI2B2 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + \overline{A1N}) \bullet (B0 + B1)}$$

Logic Symbol
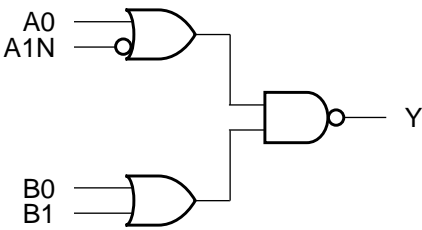
## Function Table

A0	A1N	B0	B1	Y
0	1	x	x	1
x	x	0	0	1
x	0	x	1	0
x	0	1	x	0
1	x	x	1	0
1	x	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI2B2XLAD	2.52	2.24
OAI2B2X1AD	2.52	2.24
OAI2B2X2AD	2.52	2.52
OAI2B2X4AD	2.52	3.92

Functional Schematic
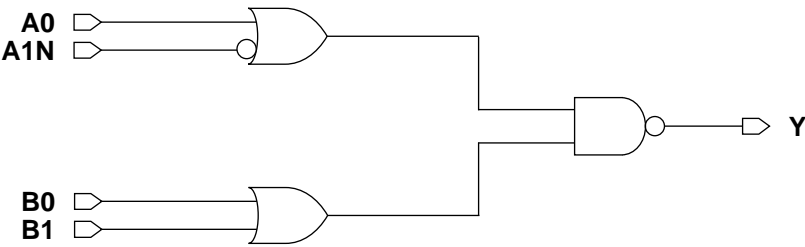
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0022	0.0028	0.0045	0.0089
A1N	0.0030	0.0036	0.0055	0.0107
B0	0.0030	0.0037	0.0061	0.0118
B1	0.0034	0.0043	0.0070	0.0137

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0016	0.0018	0.0029	0.0052
A1N	0.0011	0.0011	0.0015	0.0024
B0	0.0014	0.0017	0.0028	0.0053
B1	0.0012	0.0015	0.0026	0.0055

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0299	0.0246	0.0249	0.0248	11.6129	7.4150	4.7660	2.4664
A0	→	Y	↓	0.0244	0.0228	0.0159	0.0156	7.1854	5.0030	2.0991	1.0510
A1N	→	Y	↑	0.0488	0.0460	0.0480	0.0478	11.5772	7.4054	4.7630	2.4654
A1N	→	Y	↓	0.0668	0.0701	0.0528	0.0501	7.3518	5.1162	2.1505	1.0492
B0	→	Y	↑	0.0444	0.0358	0.0393	0.0390	11.4068	7.2850	4.7025	2.4205
B0	→	Y	↓	0.0339	0.0319	0.0235	0.0226	7.2272	5.0348	2.1251	1.0520
B1	→	Y	↑	0.0487	0.0400	0.0441	0.0444	11.3931	7.2784	4.6993	2.4195
B1	→	Y	↓	0.0386	0.0367	0.0266	0.0256	7.3437	5.1120	2.1487	1.0485

Cell Description

The OAI2BB1 cell provides the logical inverted AND of one OR group of two inverted inputs (A0N,A1N) and an additional non-inverted input (B0). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} + \overline{A1N}) \bullet B0}$$

Logic Symbol
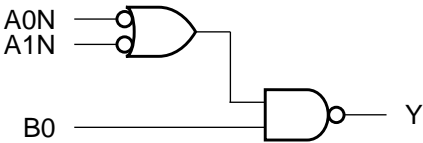
Function Table

A0N	A1N	B0	Y
1	1	x	1
x	x	0	1
x	0	1	0
0	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI2BB1XLAD	2.52	1.68
OAI2BB1X1AD	2.52	1.68
OAI2BB1X2AD	2.52	1.96
OAI2BB1X4AD	2.52	2.52

Functional Schematic
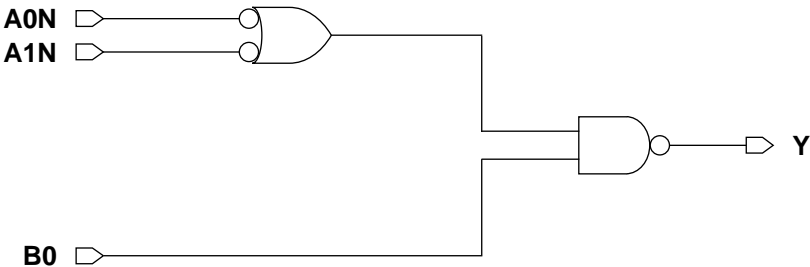
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0N	0.0031	0.0036	0.0056	0.0101
A1N	0.0028	0.0033	0.0051	0.0091
B0	0.0014	0.0019	0.0031	0.0063

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0N	0.0009	0.0009	0.0012	0.0020
A1N	0.0007	0.0007	0.0010	0.0016
B0	0.0011	0.0014	0.0022	0.0045

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0N	→ Y	↑	0.0441	0.0454	0.0411	0.0394	5.7043	3.6831	2.3702	1.2531
A0N	→ Y	↓	0.0625	0.0666	0.0553	0.0489	7.5248	5.2570	2.2086	1.0409
A1N	→ Y	↑	0.0432	0.0444	0.0396	0.0378	5.7033	3.6841	2.3707	1.2531
A1N	→ Y	↓	0.0571	0.0608	0.0500	0.0438	7.4951	5.2430	2.2024	1.0374
B0	→ Y	↑	0.0152	0.0141	0.0154	0.0158	5.5680	3.5922	2.3782	1.2095
B0	→ Y	↓	0.0181	0.0186	0.0147	0.0145	7.4085	5.2072	2.1848	1.0321

Cell Description

The OAI2BB2 cell provides the logical inverted AND of one OR group of two inverted inputs (A0N,A1N) and one OR group of two non-inverted inputs (B0,B1). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} + \overline{A1N}) \bullet (B0 + B1)}$$

Logic Symbol
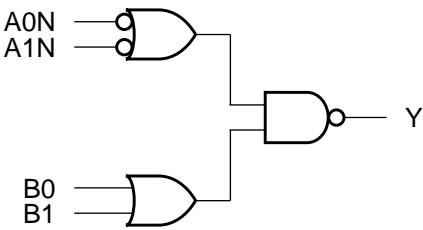
Function Table

A0N	A1N	B0	B1	Y
1	1	x	x	1
x	x	0	0	1
x	0	x	1	0
x	0	1	x	0
0	x	x	1	0
0	x	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI2BB2XLAD	2.52	2.24
OAI2BB2X1AD	2.52	2.24
OAI2BB2X2AD	2.52	2.24
OAI2BB2X4AD	2.52	3.64

Functional Schematic
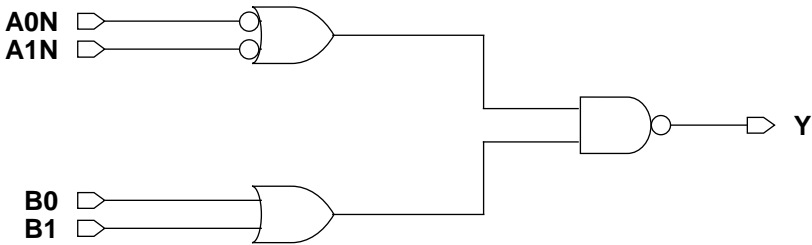
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0N	0.0033	0.0039	0.0062	0.0114
A1N	0.0030	0.0037	0.0057	0.0104
B0	0.0019	0.0024	0.0040	0.0074
B1	0.0023	0.0030	0.0048	0.0094

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0N	0.0010	0.0010	0.0014	0.0024
A1N	0.0011	0.0011	0.0016	0.0027
B0	0.0013	0.0017	0.0027	0.0052
B1	0.0012	0.0016	0.0026	0.0054

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0N	→	Y	↑	0.0446	0.0474	0.0437	0.0420	5.7333	3.7172	2.4069	1.2295
A0N	→	Y	↓	0.0649	0.0709	0.0575	0.0534	7.3449	5.1091	2.1692	1.0593
A1N	→	Y	↑	0.0437	0.0465	0.0425	0.0407	5.7334	3.7171	2.4066	1.2294
A1N	→	Y	↓	0.0633	0.0696	0.0557	0.0508	7.3419	5.1098	2.1690	1.0586
B0	→	Y	↑	0.0321	0.0281	0.0311	0.0311	11.3557	7.2670	4.7156	2.4487
B0	→	Y	↓	0.0223	0.0221	0.0175	0.0174	7.1654	5.0065	2.1051	1.0545
B1	→	Y	↑	0.0364	0.0322	0.0358	0.0363	11.3407	7.2597	4.7133	2.4489
B1	→	Y	↓	0.0268	0.0270	0.0209	0.0202	7.2760	5.0790	2.1564	1.0536

Cell Description

The OAI31 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1 + A2) \cdot B0}$$

Logic Symbol
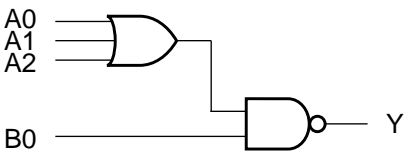
Function Table

A0	A1	A2	B0	Y
0	0	0	x	1
x	x	x	0	1
x	x	1	1	0
x	1	x	1	0
1	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI31XLAD	2.52	1.68
OAI31X1AD	2.52	1.68
OAI31X2AD	2.52	1.96
OAI31X4AD	2.52	3.36

Functional Schematic
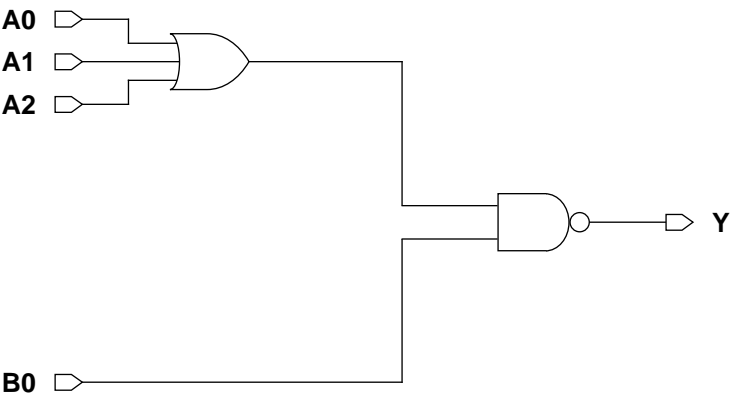
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0023	0.0030	0.0054	0.0108
A1	0.0027	0.0036	0.0063	0.0127
A2	0.0030	0.0042	0.0072	0.0145
B0	0.0021	0.0030	0.0048	0.0091

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0017	0.0028	0.0052
A1	0.0012	0.0016	0.0026	0.0054
A2	0.0012	0.0015	0.0026	0.0056
B0	0.0014	0.0018	0.0029	0.0053

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0452	0.0392	0.0462	0.0469	16.9479	10.9000	7.0479	3.6274
A0	→	Y	↓	0.0218	0.0210	0.0165	0.0164	7.0405	4.9223	2.0769	1.0492
A1	→	Y	↑	0.0560	0.0496	0.0566	0.0586	16.9368	10.8898	7.0425	3.6263
A1	→	Y	↓	0.0260	0.0255	0.0192	0.0192	7.1027	4.9686	2.0981	1.0433
A2	→	Y	↑	0.0601	0.0537	0.0607	0.0635	16.9216	10.8862	7.0418	3.6267
A2	→	Y	↓	0.0286	0.0286	0.0207	0.0206	7.3146	5.0930	2.1407	1.0557
B0	→	Y	↑	0.0146	0.0136	0.0138	0.0134	5.6775	3.6672	2.3790	1.2177
B0	→	Y	↓	0.0241	0.0247	0.0167	0.0158	7.3429	5.1071	2.1436	1.0570

Cell Description

The OAI32 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1 + A2) \bullet (B0 + B1)}$$

Logic Symbol
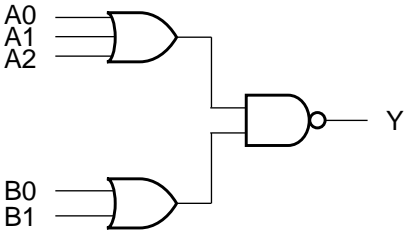
## Function Table

A0	A1	A2	B0	B1	Y
0	0	0	x	x	1
x	x	x	0	0	1
x	x	1	x	1	0
x	x	1	1	x	0
x	1	x	1	x	0
x	1	x	x	1	0
1	x	x	1	x	0
1	x	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI32XLAD	2.52	1.96
OAI32X1AD	2.52	2.24
OAI32X2AD	2.52	2.24
OAI32X4AD	2.52	4.20

Functional Schematic
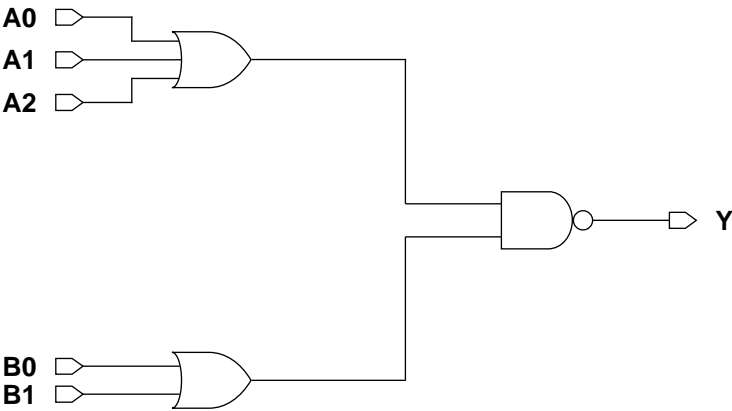
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0036	0.0043	0.0074	0.0149
A1	0.0039	0.0049	0.0083	0.0167
A2	0.0043	0.0055	0.0091	0.0185
B0	0.0025	0.0035	0.0053	0.0108
B1	0.0029	0.0040	0.0062	0.0126

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0018	0.0028	0.0052
A1	0.0012	0.0016	0.0026	0.0055
A2	0.0011	0.0016	0.0026	0.0056
B0	0.0013	0.0018	0.0028	0.0052
B1	0.0014	0.0017	0.0027	0.0055

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0656	0.0515	0.0594	0.0610	17.3039	11.0637	7.1203	3.6547
A0	→	Y	↓	0.0325	0.0297	0.0217	0.0218	7.1592	4.9491	2.0927	1.0483
A1	→	Y	↑	0.0769	0.0616	0.0699	0.0730	17.2831	11.0523	7.1148	3.6529
A1	→	Y	↓	0.0370	0.0342	0.0246	0.0248	7.1835	4.9637	2.0995	1.0417
A2	→	Y	↑	0.0813	0.0659	0.0741	0.0778	17.2823	11.0519	7.1146	3.6525
A2	→	Y	↓	0.0405	0.0377	0.0265	0.0264	7.3748	5.0585	2.1407	1.0499
B0	→	Y	↑	0.0270	0.0246	0.0244	0.0253	11.4191	7.3373	4.7327	2.4314
B0	→	Y	↓	0.0254	0.0262	0.0174	0.0176	7.2512	4.9974	2.1134	1.0609
B1	→	Y	↑	0.0331	0.0291	0.0291	0.0307	11.4199	7.3289	4.7287	2.4307
B1	→	Y	↓	0.0316	0.0313	0.0206	0.0205	7.3882	5.0583	2.1412	1.0502

Cell Description

The OAI33 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1 + A2) \bullet (B0 + B1 + B2)}$$

Logic Symbol
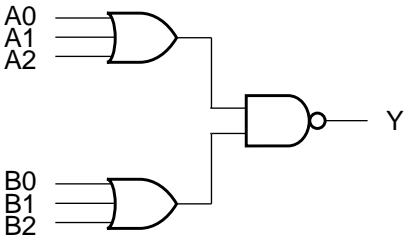
Function Table

A0	A1	A2	B0	B1	B2	Y
0	0	0	x	x	x	1
x	x	x	0	0	0	1
x	x	1	x	x	1	0
x	x	1	x	1	x	0
x	x	1	1	x	x	0
x	1	x	x	x	1	0
x	1	x	x	1	x	0
x	1	x	1	x	x	0
1	x	x	x	x	1	0
1	x	x	x	1	x	0
1	x	x	1	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI33XLAD	2.52	2.52
OAI33X1AD	2.52	2.52
OAI33X2AD	2.52	2.52
OAI33X4AD	2.52	4.76

Functional Schematic
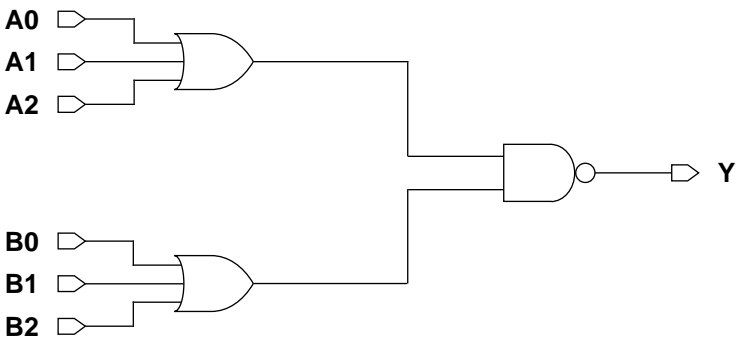
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0030	0.0041	0.0063	0.0124
A1	0.0034	0.0046	0.0071	0.0141
A2	0.0038	0.0052	0.0080	0.0159
B0	0.0041	0.0055	0.0093	0.0186
B1	0.0045	0.0061	0.0103	0.0204
B2	0.0049	0.0066	0.0111	0.0222

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0018	0.0028	0.0052
A1	0.0013	0.0017	0.0027	0.0055
A2	0.0013	0.0017	0.0027	0.0058
B0	0.0013	0.0017	0.0027	0.0051
B1	0.0013	0.0017	0.0027	0.0054
B2	0.0012	0.0016	0.0026	0.0056

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→ Y	↑	0.0451	0.0389	0.0388	0.0389	17.3600	11.2024	7.1904	3.6950
A0	→ Y	↓	0.0290	0.0289	0.0190	0.0186	7.1514	5.0099	2.1030	1.0491
A1	→ Y	↑	0.0569	0.0500	0.0499	0.0511	17.3402	11.1917	7.1849	3.6936
A1	→ Y	↓	0.0341	0.0341	0.0223	0.0220	7.1715	5.0140	2.1184	1.0503
A2	→ Y	↑	0.0631	0.0556	0.0549	0.0565	17.3515	11.1945	7.1866	3.6947
A2	→ Y	↓	0.0387	0.0386	0.0247	0.0242	7.3211	5.0991	2.1570	1.0578
B0	→ Y	↑	0.0724	0.0619	0.0722	0.0734	17.3550	11.1460	7.1526	3.6724
B0	→ Y	↓	0.0369	0.0359	0.0257	0.0257	7.1469	4.9565	2.1133	1.0625
B1	→ Y	↑	0.0836	0.0730	0.0833	0.0851	17.3368	11.1378	7.1481	3.6706
B1	→ Y	↓	0.0418	0.0416	0.0290	0.0288	7.1653	5.0230	2.1196	1.0536
B2	→ Y	↑	0.0885	0.0772	0.0876	0.0904	17.3365	11.1365	7.1478	3.6708
B2	→ Y	↓	0.0459	0.0455	0.0313	0.0307	7.3205	5.0969	2.1574	1.0580

Cell Description

The OR2 cell provides the logical OR of two inputs (A,B). The output (Y) is represented by the logic equation:

$Y = (A + B)$

Logic Symbol

A ⎯⎯
B ⎯⎯ ⟩ ⎯⎯ Y
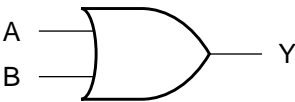
Function Table

A	B	Y
0	0	0
x	1	1
1	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
OR2XLAD	2.52	1.40
OR2X1AD	2.52	1.40
OR2X2AD	2.52	1.40
OR2X4AD	2.52	2.52
OR2X6AD	2.52	2.80
OR2X8AD	2.52	3.64

Functional Schematic

A
B

Y
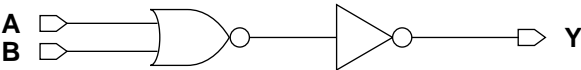
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0027	0.0032	0.0049	0.0091	0.0136	0.0184
B	0.0030	0.0037	0.0056	0.0105	0.0155	0.0210

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0011	0.0012	0.0018	0.0033	0.0045	0.0066
B	0.0011	0.0013	0.0018	0.0035	0.0048	0.0065

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	0.0273	0.0299	0.0326	0.0300	0.0298	0.0302
A	→ Y	↓	0.0696	0.0611	0.0493	0.0460	0.0467	0.0465
B	→ Y	↑	0.0288	0.0322	0.0359	0.0336	0.0331	0.0335
B	→ Y	↓	0.0759	0.0669	0.0548	0.0516	0.0523	0.0517

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	5.5749	3.5922	2.3385	1.2024	0.8188	0.6168
A	→ Y	↓	4.7791	3.1756	1.3596	0.6671	0.4447	0.3314
B	→ Y	↑	5.5822	3.5978	2.3407	1.2033	0.8197	0.6175
B	→ Y	↓	4.7791	3.1756	1.3596	0.6670	0.4447	0.3314

Cell Description

The OR3 cell provides the logical OR of three inputs (A,B,C). The output (Y) is represented by the logic equation:

$Y = (A + B + C)$

Logic Symbol
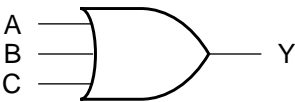
Function Table

A	B	C	Y
0	0	0	0
x	x	1	1
x	1	x	1
1	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
OR3XLAD	2.52	1.68
OR3X1AD	2.52	1.68
OR3X2AD	2.52	1.68
OR3X4AD	2.52	2.80
OR3X6AD	2.52	4.20
OR3X8AD	2.52	5.60

Functional Schematic
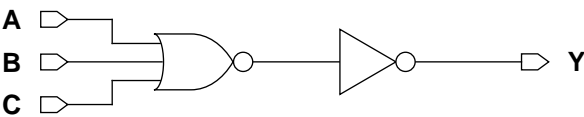
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0034	0.0041	0.0060	0.0110	0.0168	0.0220
B	0.0037	0.0045	0.0068	0.0128	0.0196	0.0253
C	0.0041	0.0050	0.0077	0.0147	0.0222	0.0291

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0013	0.0015	0.0022	0.0039	0.0061	0.0083
B	0.0013	0.0015	0.0022	0.0041	0.0064	0.0082
C	0.0013	0.0015	0.0021	0.0043	0.0062	0.0086

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	0.0310	0.0340	0.0367	0.0339	0.0344	0.0337
A	→ Y	↓	0.0804	0.0704	0.0562	0.0519	0.0533	0.0522
B	→ Y	↑	0.0332	0.0376	0.0417	0.0392	0.0394	0.0387
B	→ Y	↓	0.0916	0.0816	0.0671	0.0634	0.0655	0.0632
C	→ Y	↑	0.0345	0.0400	0.0452	0.0427	0.0429	0.0425
C	→ Y	↓	0.0963	0.0862	0.0716	0.0682	0.0702	0.0688

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	5.6404	3.6393	2.3732	1.2182	0.8229	0.6213
A	→ Y	↓	5.0676	3.3064	1.4198	0.6921	0.4655	0.3432
B	→ Y	↑	5.6541	3.6492	2.3788	1.2208	0.8248	0.6226
B	→ Y	↓	5.0662	3.3058	1.4196	0.6920	0.4655	0.3432
C	→ Y	↑	5.6826	3.6665	2.3864	1.2248	0.8279	0.6250
C	→ Y	↓	5.0663	3.3054	1.4194	0.6920	0.4655	0.3432

Cell Description

The OR4 cell provides the logical OR of four inputs (A,B,C,D). The output (Y) is represented by the logic equation:

$Y = (A + B + C + D)$

Logic Symbol
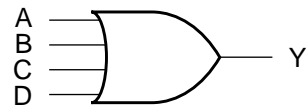
Function Table

A	B	C	D	Y
0	0	0	0	0
x	x	x	1	1
x	x	1	x	1
x	1	x	x	1
1	x	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
OR4XLAD	2.52	2.24
OR4X1AD	2.52	2.24
OR4X2AD	2.52	2.24
OR4X4AD	2.52	3.64
OR4X6AD	2.52	5.32
OR4X8AD	2.52	7.00

Functional Schematic
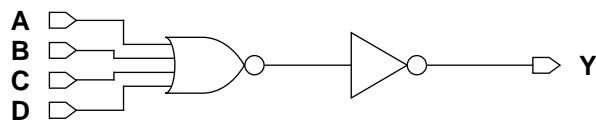
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0038	0.0045	0.0067	0.0122	0.0193	0.0246
B	0.0041	0.0049	0.0074	0.0139	0.0215	0.0277
C	0.0044	0.0053	0.0081	0.0153	0.0237	0.0307
D	0.0047	0.0058	0.0090	0.0170	0.0263	0.0342

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0012	0.0014	0.0021	0.0036	0.0063	0.0079
B	0.0011	0.0013	0.0019	0.0038	0.0060	0.0078
C	0.0011	0.0013	0.0019	0.0040	0.0060	0.0082
D	0.0012	0.0014	0.0020	0.0044	0.0063	0.0093

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	0.0313	0.0340	0.0372	0.0343	0.0353	0.0343
A	→ Y	↓	0.1181	0.0991	0.0754	0.0694	0.0724	0.0696
B	→ Y	↑	0.0328	0.0366	0.0413	0.0388	0.0398	0.0388
B	→ Y	↓	0.1354	0.1166	0.0922	0.0879	0.0907	0.0879
C	→ Y	↑	0.0340	0.0387	0.0446	0.0418	0.0432	0.0423
C	→ Y	↓	0.1475	0.1277	0.1029	0.0981	0.1019	0.0993
D	→ Y	↑	0.0347	0.0399	0.0466	0.0439	0.0453	0.0449
D	→ Y	↓	0.1552	0.1344	0.1086	0.1047	0.1084	0.1061

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)					
				XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→	Y	↑	5.6552	3.6411	2.3699	1.2130	0.8242	0.6195
A	→	Y	↓	5.7872	3.6121	1.5488	0.7552	0.5110	0.3756
B	→	Y	↑	5.6675	3.6488	2.3751	1.2154	0.8260	0.6209
B	→	Y	↓	5.7871	3.6102	1.5486	0.7553	0.5110	0.3757
C	→	Y	↑	5.6952	3.6661	2.3842	1.2202	0.8293	0.6234
C	→	Y	↓	5.7871	3.6109	1.5486	0.7550	0.5110	0.3756
D	→	Y	↑	5.7324	3.6910	2.3970	1.2267	0.8340	0.6272
D	→	Y	↓	5.7893	3.6101	1.5485	0.7553	0.5109	0.3756

Cell Description

The RF1R1W register file cell is an active-high D-type transparent latch with an active-high tristate output. The output (RB) is inverted.

Logic Symbol
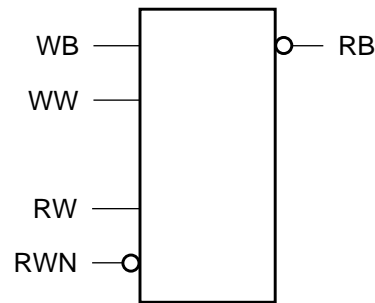
Cell Size

Drive Strength	Height (um)	Width (um)
RF1R1WX1AD	2.52	3.36

Function Table

WW	WB	q[n+1]
0	x	q[n]
1	0	0
1	1	1

- Functions for Write Operations

Function Table (Cont'd.)

RW	RWN	q	RB
0	0	0	1
0	0	1	Hi-Z
0	1	0	Hi-Z
0	1	1	Hi-Z
1	0	0	1
1	0	1	0
1	1	0	Hi-Z
1	1	1	0

- Functions for Read Operations
- Shaded areas represent operations that are legal only during RW/RWN transitions.

Functional Schematic
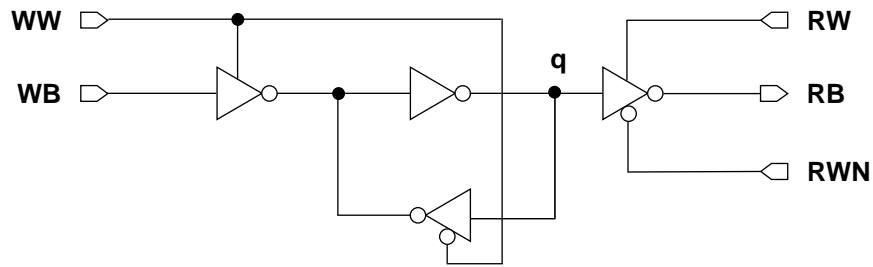
AC Power

Pin	Power (uW/MHz)
	X1
WW	0.0043
WB	0.0046
RW	0.0003
RB	0.0014

Pin Capacitance

Pin	Capacitance (pF)
	X1
WW	0.0023
WB	0.0012
RW	0.0007
RWN	0.0003
RB	0.3064

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)	K_{load} (ns/pF)
				X1	**X1**
WW	→	RB	↑	0.1270	12.7388
WW	→	RB	↓	0.0733	6.2495
WB	→	RB	↑	0.1101	12.7393
WB	→	RB	↓	0.0838	6.2504
RW	→	RB	↑	0.0162	12.7289
RW	→	RB	↓	0.0099	6.2289

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)
					X1
WW	minpwh				0.8332
WB	setup	↑	→	WW	0.0508
	setup	↓	→	WW	0.0508
	hold	↑	→	WW	-0.0430
	hold	↓	→	WW	-0.0430

Cell Description

The RF2R1W register file cell is an active-high D-type transparent latch with two independently controlled, active-high tri-state outputs. The cell has two read ports and one write port. The outputs (R1B,R2B) are inverted.

Logic Symbol
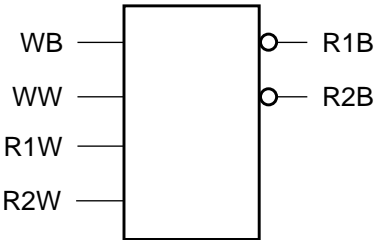
Cell Size

Drive Strength	Height (um)	Width (um)
RF2R1WX1AD	2.52	5.32

Function Table

WW	WB	q[n+1]
0	0	q[n]
0	1	q[n]
1	0	0
1	1	1

- Functions for Write Operations

Function Table (Cont'd.)

R1W/R2W	q	R1B/R2B
0	0	Hi-Z
0	1	Hi-Z
1	0	1
1	1	0

- Functions for Read Operations

Functional Schematic
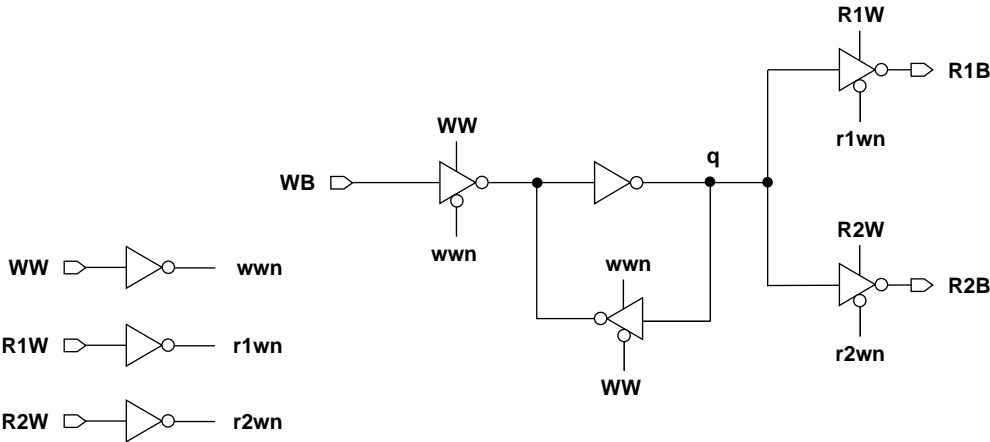
AC Power

Pin	Power (uW/MHz)
	X1
WB	0.0052
WW	0.0029
R1W	0.0015
R2W	0.0015
R1B	0.0075

Pin Capacitance

Pin	Capacitance (pF)
	X1
WB	0.0010
WW	0.0019
R1W	0.0014
R2W	0.0016
R1B	0.0009
R2B	0.0009

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)	K_{load} (ns/pF)
			X1	**X1**
WB	→	R1B ↑	0.1380	12.7239
WB	→	R1B ↓	0.1000	6.2574
WW	→	R1B ↑	0.1574	12.7240
WW	→	R1B ↓	0.0914	6.2571
R1W	→	R1B ↑	0.0343	12.6970
R1W	→	R1B ↓	0.0089	6.2014
WB	→	R2B ↑	0.1355	12.6430
WB	→	R2B ↓	0.0992	6.2942
WW	→	R2B ↑	0.1550	12.6444
WW	→	R2B ↓	0.0906	6.2941
R2W	→	R2B ↑	0.0325	12.6237
R2W	→	R2B ↓	0.0085	6.2349

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)
					X1
WB	setup	↑	→	WW	0.0547
	setup	↓	→	WW	0.0703
	hold	↑	→	WW	-0.0430
	hold	↓	→	WW	-0.0586
WW	minpwh				0.8332

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Cell Description

The SDFF cell is a positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE).

Logic Symbol

Function Table

D	SI	SE	CK	Q[n+1]	QN[n+1]
1	x	0	⌐	1	0
0	x	0	⌐	0	1
x	x	x	⌐	Q[n]	QN[n]
x	1	1	⌐	1	0
x	0	1	⌐	0	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFXLAD	2.52	7.56
SDFFX1AD	2.52	7.56
SDFFX2AD	2.52	7.56
SDFFX4AD	2.52	9.52

Functional Schematic

AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
SI	0.0069	0.0071	0.0072	0.0084
SE	0.0083	0.0086	0.0086	0.0098
D	0.0060	0.0062	0.0063	0.0075
CK	0.0113	0.0115	0.0117	0.0135
Q	0.0054	0.0064	0.0085	0.0150

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
SI	0.0010	0.0010	0.0010	0.0010
SE	0.0030	0.0031	0.0030	0.0031
D	0.0014	0.0014	0.0014	0.0014
CK	0.0017	0.0017	0.0016	0.0019

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→ Q	↑	0.1114	0.1077	0.1022	0.0990	5.8650	3.7328	2.3802	1.2169
CK	→ Q	↓	0.1303	0.1254	0.1030	0.0970	5.5121	3.4921	1.4335	0.7148
CK	→ QN	↑	0.1579	0.1535	0.1461	0.1428	5.7134	3.6694	2.3633	1.2098
CK	→ QN	↓	0.1499	0.1528	0.1534	0.1475	4.6460	3.1619	1.3591	0.6655

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	X1	X2	X4
SI	setup	↑	→	CK	0.0820	0.0859	0.0820	0.0938
	setup	↓	→	CK	0.1992	0.1992	0.2070	0.2227
	hold	↑	→	CK	-0.0664	-0.0664	-0.0664	-0.0664
	hold	↓	→	CK	-0.1641	-0.1641	-0.1641	-0.1758
SE	setup	↑	→	CK	0.1992	0.1992	0.2070	0.2227
	setup	↓	→	CK	0.0977	0.0977	0.0938	0.1016
	hold	↑	→	CK	-0.0625	-0.0625	-0.0625	-0.0664
	hold	↓	→	CK	-0.0391	-0.0391	-0.0430	-0.0469
D	setup	↑	→	CK	0.0703	0.0742	0.0703	0.0781
	setup	↓	→	CK	0.0742	0.0781	0.0820	0.0977
	hold	↑	→	CK	-0.0547	-0.0586	-0.0547	-0.0586
	hold	↓	→	CK	-0.0391	-0.0391	-0.0391	-0.0469
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The SDFFH cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and fast clock-to-Q-path.

Logic Symbol
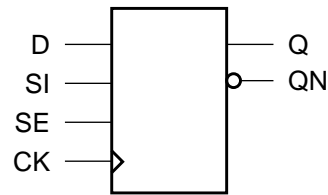
Function Table

D	SI	SE	CK	Q[n+1]	QN[n+1]
1	x	0	⌐⌐	1	0
0	x	0	⌐⌐	0	1
x	x	x	⌐⌐	Q[n]	QN[n]
x	1	1	⌐⌐	1	0
x	0	1	⌐⌐	0	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFHX1AD	2.52	8.40
SDFFHX2AD	2.52	9.24
SDFFHX4AD	2.52	10.64
SDFFHX8AD	2.52	18.20

Functional Schematic
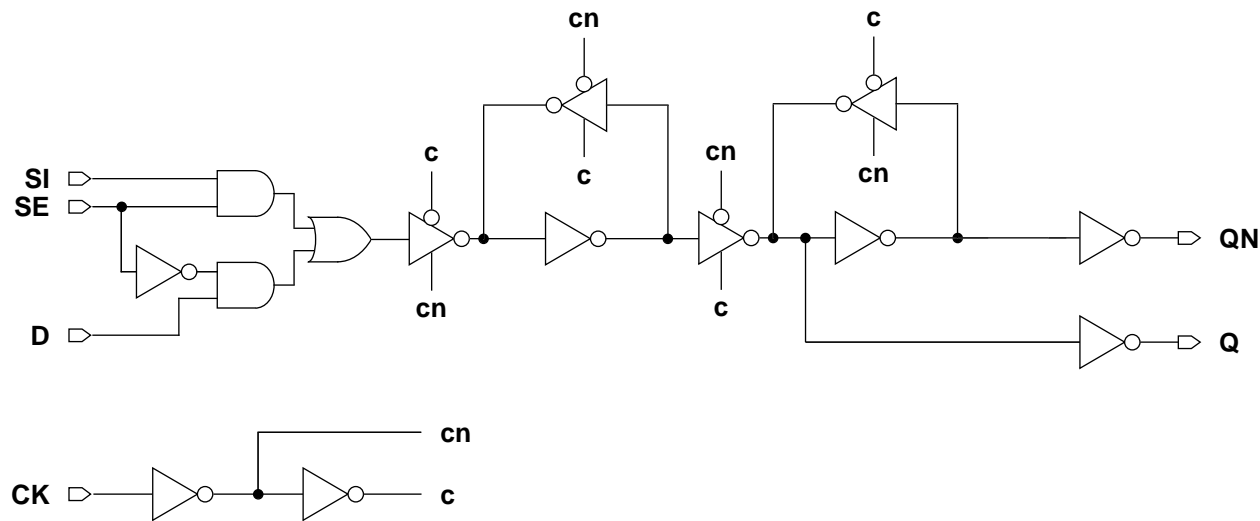
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
SI	0.0077	0.0100	0.0144	0.0273
SE	0.0107	0.0131	0.0169	0.0340
D	0.0087	0.0113	0.0161	0.0315
CK	0.0152	0.0190	0.0255	0.0484
Q	0.0054	0.0068	0.0095	0.0159

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
SI	0.0014	0.0014	0.0018	0.0027
SE	0.0032	0.0035	0.0033	0.0063
D	0.0013	0.0017	0.0021	0.0051
CK	0.0023	0.0022	0.0032	0.0054

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→	Q ↑	0.0808	0.0778	0.0682	0.0651	3.6032	2.3747	1.2027	0.6067
CK	→	Q ↓	0.0842	0.0808	0.0754	0.0685	3.2702	1.4088	0.7009	0.3287
CK	→	QN ↑	0.1161	0.1138	0.1112	0.1040	5.5271	5.4454	5.4605	5.4097
CK	→	QN ↓	0.1397	0.1360	0.1283	0.1288	4.3796	4.2536	4.2213	4.2096

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
SI	setup	↑	→	CK	0.0742	0.0703	0.0586	0.0586
	setup	↓	→	CK	0.1094	0.1094	0.1016	0.0977
	hold	↑	→	CK	-0.0312	-0.0312	-0.0273	-0.0234
	hold	↓	→	CK	-0.0742	-0.0781	-0.0703	-0.0625
SE	setup	↑	→	CK	0.1367	0.1406	0.1289	0.1406
	setup	↓	→	CK	0.1016	0.0820	0.0781	0.0938
	hold	↑	→	CK	-0.0312	-0.0312	-0.0273	-0.0273
	hold	↓	→	CK	-0.0547	-0.0312	-0.0391	-0.0273
D	setup	↑	→	CK	0.0781	0.0625	0.0586	0.0508
	setup	↓	→	CK	0.0938	0.0703	0.0703	0.0586
	hold	↑	→	CK	-0.0391	-0.0234	-0.0234	-0.0195
	hold	↓	→	CK	-0.0625	-0.0391	-0.0430	-0.0273
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

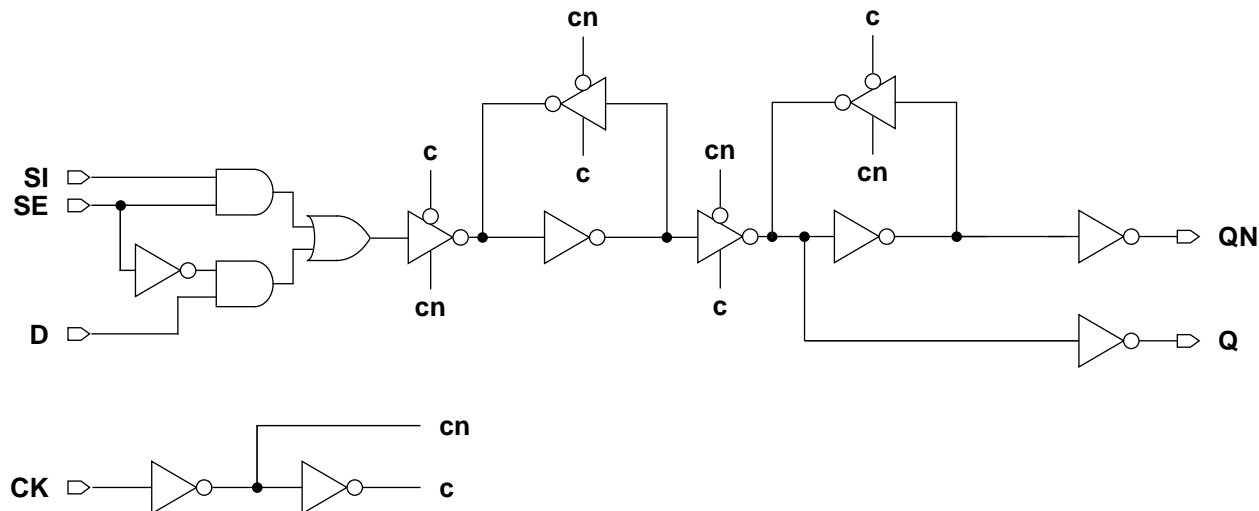The SDFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol
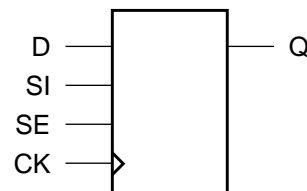
Function Table

D	SI	SE	CK	Q[n+1]
1	x	0	⌐	1
0	x	0	⌐	0
x	x	x	⌐	Q[n]
x	1	1	⌐	1
x	0	1	⌐	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFHQX1AD	2.52	8.12
SDFFHQX2AD	2.52	8.96
SDFFHQX4AD	2.52	10.08
SDFFHQX8AD	2.52	10.92

Functional Schematic
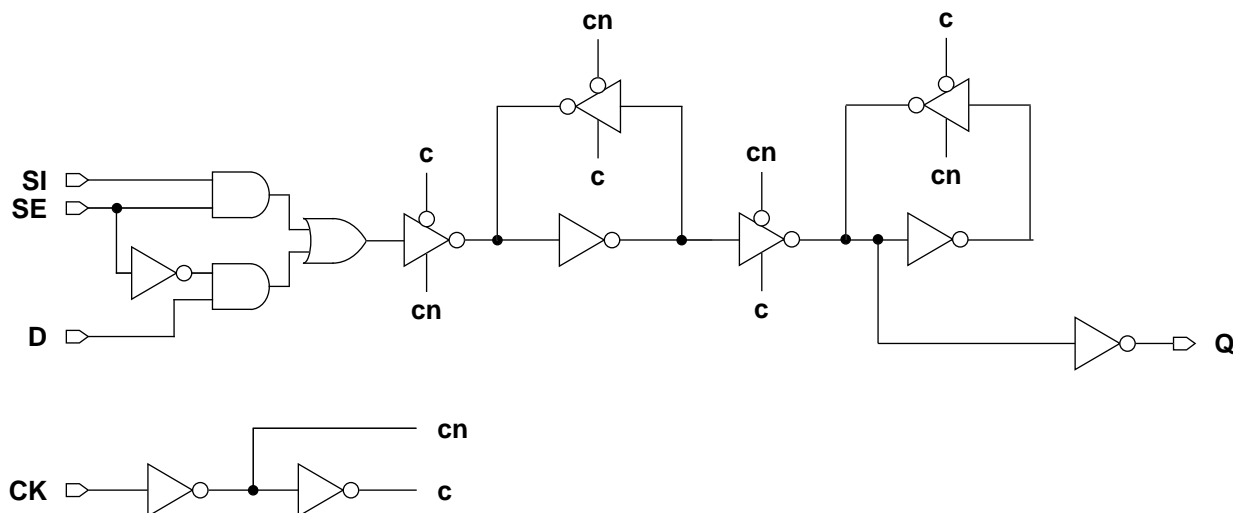
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
SI	0.0074	0.0096	0.0144	0.0148
SE	0.0103	0.0127	0.0167	0.0166
D	0.0086	0.0113	0.0160	0.0151
CK	0.0146	0.0183	0.0252	0.0245
Q	0.0037	0.0052	0.0084	0.0145

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
SI	0.0014	0.0014	0.0018	0.0014
SE	0.0032	0.0035	0.0033	0.0036
D	0.0016	0.0022	0.0021	0.0021
CK	0.0023	0.0022	0.0032	0.0032

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→ Q	↑	0.0836	0.0785	0.0684	0.0759	3.6211	2.3775	1.2057	0.6171
CK	→ Q	↓	0.0847	0.0816	0.0759	0.0808	3.2521	1.4072	0.7044	0.3431

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
SI	setup	↑	→	CK	0.0742	0.0703	0.0586	0.0781
	setup	↓	→	CK	0.1094	0.1094	0.1016	0.1367
	hold	↑	→	CK	-0.0312	-0.0312	-0.0273	-0.0352
	hold	↓	→	CK	-0.0742	-0.0781	-0.0703	-0.0977
SE	setup	↑	→	CK	0.1406	0.1406	0.1289	0.1562
	setup	↓	→	CK	0.1055	0.0859	0.0781	0.0859
	hold	↑	→	CK	-0.0273	-0.0312	-0.0273	-0.0273
	hold	↓	→	CK	-0.0469	-0.0234	-0.0391	-0.0312
D	setup	↑	→	CK	0.0859	0.0664	0.0586	0.0625
	setup	↓	→	CK	0.0820	0.0547	0.0703	0.0703
	hold	↑	→	CK	-0.0430	-0.0312	-0.0234	-0.0234
	hold	↓	→	CK	-0.0469	-0.0234	-0.0430	-0.0391
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The SDFFNH cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and fast clock-to-Q-path.

Logic Symbol
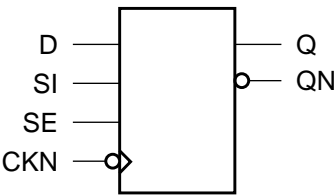
Function Table

D	SI	SE	CKN	Q[n+1]	QN[n+1]
1	x	0	⌐＿	1	0
0	x	0	⌐＿	0	1
x	x	x	＿/	Q[n]	QN[n]
x	1	1	⌐＿	1	0
x	0	1	⌐＿	0	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFNHX1AD	2.52	8.12
SDFFNHX2AD	2.52	8.40
SDFFNHX4AD	2.52	11.20
SDFFNHX8AD	2.52	15.12

Functional Schematic
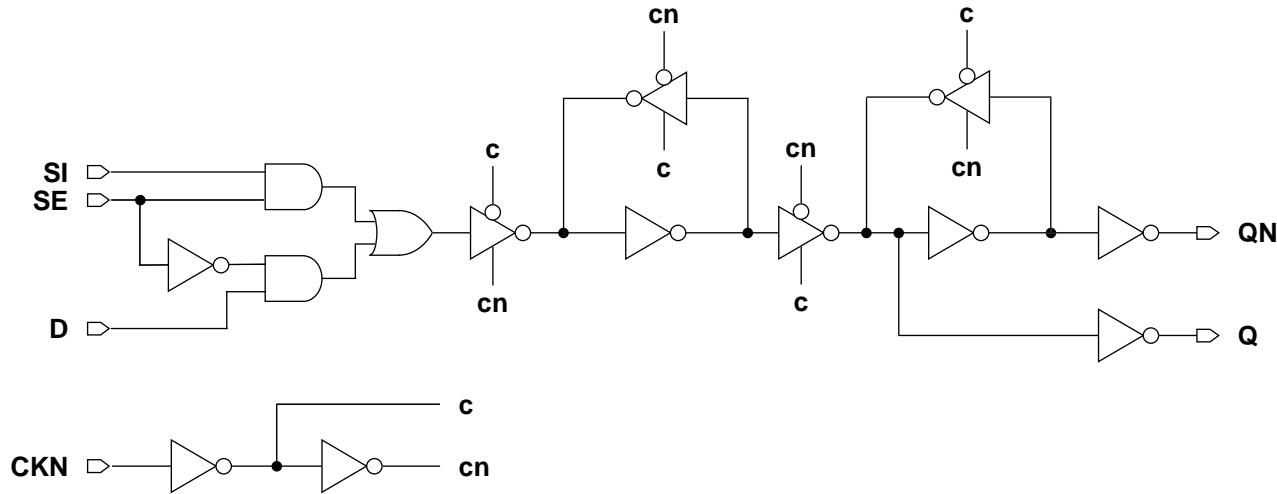
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
SI	0.0072	0.0089	0.0137	0.0210
SE	0.0098	0.0113	0.0165	0.0253
D	0.0083	0.0101	0.0157	0.0252
CKN	0.0119	0.0141	0.0205	0.0322
Q	0.0062	0.0072	0.0108	0.0187

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
SI	0.0013	0.0013	0.0017	0.0021
SE	0.0027	0.0028	0.0031	0.0038
D	0.0014	0.0017	0.0024	0.0046
CKN	0.0021	0.0022	0.0027	0.0042

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CKN	→	Q	↑	0.1562	0.1475	0.1436	0.1317	3.6205	2.3151	1.1832	0.6051
CKN	→	Q	↓	0.1345	0.1180	0.1115	0.0989	3.3219	1.3928	0.6736	0.3315
CKN	→	QN	↑	0.1668	0.1495	0.1475	0.1351	5.5010	5.4296	5.4507	5.4487
CKN	→	QN	↓	0.2016	0.1893	0.1979	0.1811	4.2843	4.2956	4.2183	4.2056

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
SI	setup	↑	→	CKN	0.0000	-0.0039	-0.0078	0.0117
	setup	↓	→	CKN	0.0625	0.0703	0.0625	0.0625
	hold	↑	→	CKN	0.0352	0.0312	0.0273	0.0195
	hold	↓	→	CKN	-0.0352	-0.0430	-0.0391	-0.0352
SE	setup	↑	→	CKN	0.0859	0.0938	0.0898	0.0938
	setup	↓	→	CKN	0.0430	0.0391	0.0469	0.0469
	hold	↑	→	CKN	0.0391	0.0352	0.0312	0.0195
	hold	↓	→	CKN	0.0117	0.0117	0.0039	-0.0078
D	setup	↑	→	CKN	0.0039	-0.0039	-0.0039	0.0117
	setup	↓	→	CKN	0.0469	0.0391	0.0430	0.0469
	hold	↑	→	CKN	0.0273	0.0273	0.0273	0.0195
	hold	↓	→	CKN	-0.0195	-0.0117	-0.0195	-0.0195
CKN	minpwl				0.8332	0.8332	0.8332	0.8332
	minpwh				0.8332	0.8332	0.8332	0.8332

Cell Description

The SDFFNSRH cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN). Set (SN) dominates reset (RN). This cell has a fast clock-to-Q path.

Logic Symbol
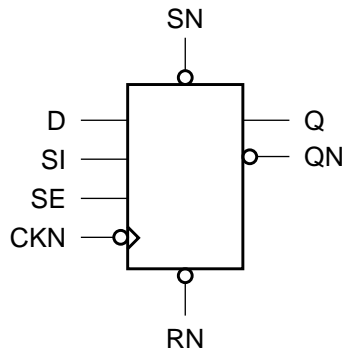
Function Table

RN	SN	D	SI	SE	CKN	Q[n+1]	QN[n+1]
1	1	1	x	0	⌐_	1	0
1	1	0	x	0	⌐_	0	1
1	1	x	x	x	_/‾	Q[n]	QN[n]
1	1	x	1	1	⌐_	1	0
1	1	x	0	1	⌐_	0	1
0	1	x	x	x	x	0	1
1	0	x	x	x	x	1	0
0	0	x	x	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFNSRHX1AD	2.52	11.76
SDFFNSRHX2AD	2.52	11.76
SDFFNSRHX4AD	2.52	14.84
SDFFNSRHX8AD	2.52	15.68

Functional Schematic
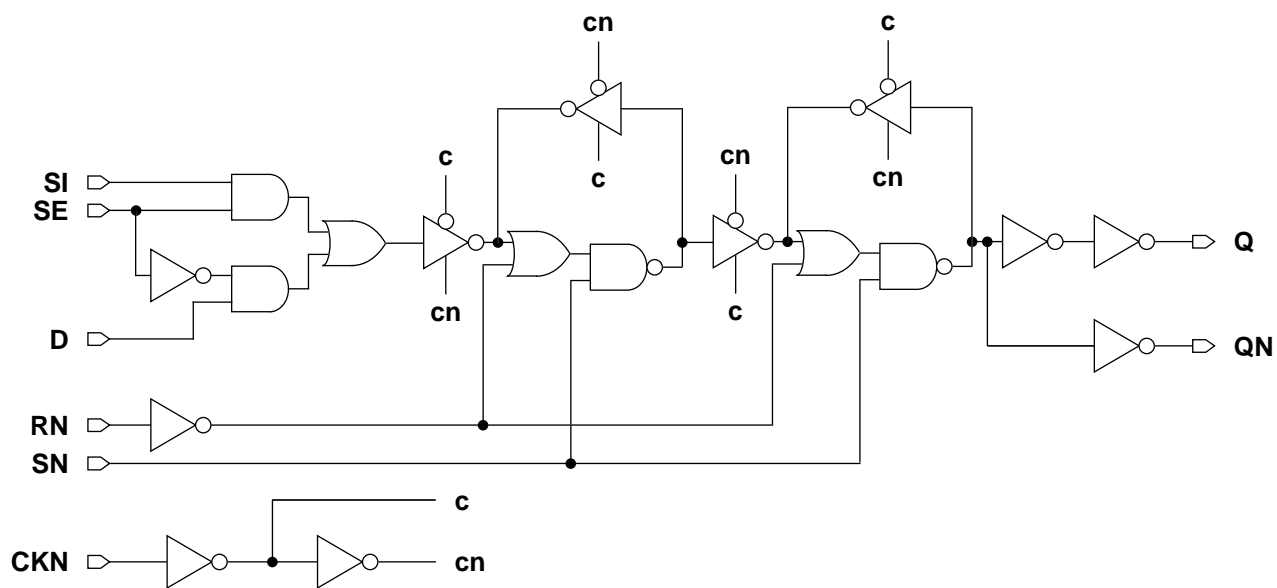
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
SI	0.0090	0.0107	0.0169	0.0189
SE	0.0103	0.0119	0.0180	0.0201
D	0.0099	0.0117	0.0184	0.0202
CKN	0.0128	0.0150	0.0228	0.0249
SN	0.0044	0.0047	0.0060	0.0069
RN	0.0016	0.0019	0.0030	0.0033
Q	0.0074	0.0091	0.0140	0.0205

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
SI	0.0013	0.0012	0.0015	0.0019
SE	0.0026	0.0026	0.0029	0.0033
D	0.0014	0.0017	0.0025	0.0025
CKN	0.0021	0.0023	0.0028	0.0041
SN	0.0022	0.0026	0.0035	0.0040
RN	0.0021	0.0025	0.0038	0.0039

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CKN	→	Q	↑	0.1742	0.1649	0.1658	0.1565	3.7559	2.4306	1.2056	0.6226
CKN	→	Q	↓	0.1441	0.1225	0.1187	0.1190	3.4085	1.4453	0.7008	0.3587
SN	→	Q	↑	0.1146	0.1369	0.1673	0.1384	3.6503	2.4257	1.2106	0.6132
SN	→	Q	↓	0.2049	0.1865	0.1722	0.1830	3.8914	1.7219	0.8482	0.4306
RN	→	Q	↓	0.1782	0.1549	0.1356	0.1550	3.9102	1.7235	0.8491	0.4308
CKN	→	QN	↑	0.1781	0.1604	0.1577	0.1634	5.4334	5.4350	5.4419	5.4401
CKN	→	QN	↓	0.2281	0.2183	0.2217	0.2177	4.4992	4.4201	4.3308	4.3232
SN	→	QN	↑	0.2442	0.2329	0.2196	0.2388	5.4639	5.4452	5.4437	5.4414
SN	→	QN	↓	0.1647	0.1896	0.2230	0.1979	4.4785	4.4132	4.3298	4.3224
RN	→	QN	↑	0.2179	0.2012	0.1828	0.2137	5.4640	5.4436	5.4433	5.4406

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
SI	setup	↑	→	CKN	0.0156	0.0156	0.0117	0.0039
	setup	↓	→	CKN	0.0742	0.0820	0.0859	0.1094
	hold	↑	→	CKN	0.0352	0.0273	0.0273	0.0352
	hold	↓	→	CKN	-0.0391	-0.0469	-0.0508	-0.0664
SE	setup	↑	→	CKN	0.1016	0.1094	0.1133	0.1406
	setup	↓	→	CKN	0.0547	0.0547	0.0547	0.0703
	hold	↑	→	CKN	0.0352	0.0273	0.0312	0.0352
	hold	↓	→	CKN	0.0117	0.0078	0.0078	0.0078
D	setup	↑	→	CKN	0.0234	0.0156	0.0117	0.0117
	setup	↓	→	CKN	0.0586	0.0508	0.0469	0.0586
	hold	↑	→	CKN	0.0273	0.0234	0.0273	0.0312
	hold	↓	→	CKN	-0.0234	-0.0156	-0.0117	-0.0195
CKN	minpwl				0.8332	0.8332	0.8332	0.8332
	minpwh				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0078	-0.0117	-0.0117	0.0000
	removal				0.0273	0.0273	0.0273	0.0195
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0977	-0.0898	-0.0938	-0.0781
	removal				0.1328	0.1406	0.1719	0.1445

Cell Description

The SDFFQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE). The cell has a single output (Q).

Logic Symbol
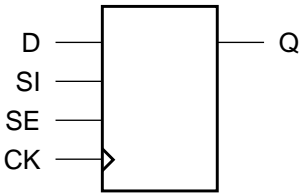
Function Table

D	SI	SE	CK	Q[n+1]
1	x	0	⌐	1
0	x	0	⌐	0
x	x	x	⌐	Q[n]
x	1	1	⌐	1
x	0	1	⌐	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFQXLAD	2.52	7.00
SDFFQX1AD	2.52	7.00
SDFFQX2AD	2.52	7.00
SDFFQX4AD	2.52	8.68

Functional Schematic
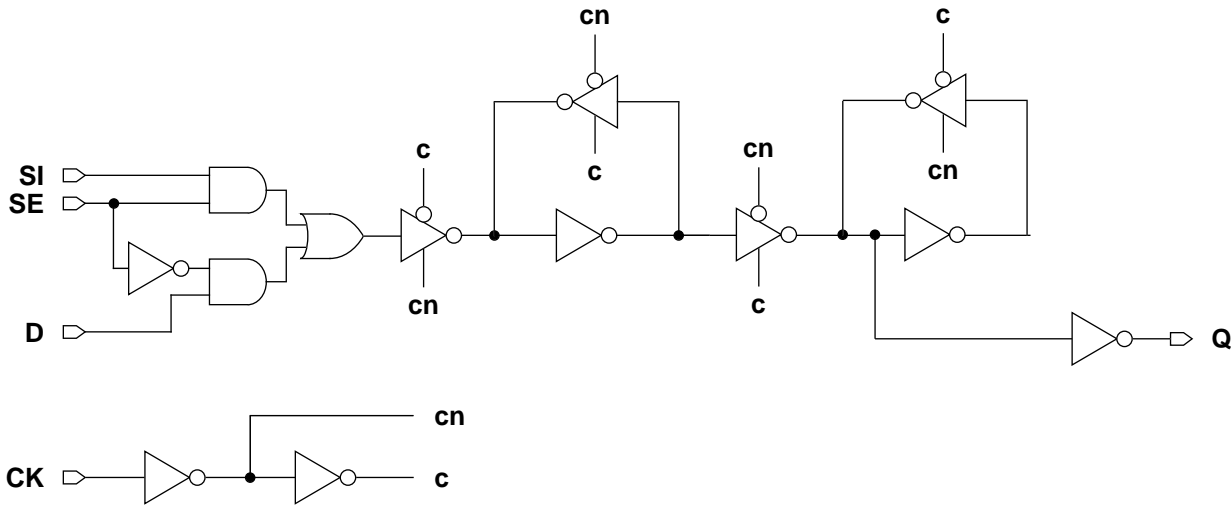
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
SI	0.0069	0.0070	0.0073	0.0081
SE	0.0083	0.0084	0.0087	0.0094
D	0.0060	0.0061	0.0064	0.0072
CK	0.0113	0.0114	0.0117	0.0133
Q	0.0041	0.0046	0.0060	0.0101

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
SI	0.0010	0.0010	0.0011	0.0010
SE	0.0030	0.0030	0.0030	0.0030
D	0.0014	0.0014	0.0016	0.0015
CK	0.0017	0.0017	0.0017	0.0018

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1083	0.1057	0.1041	0.1039	5.6900	3.6060	2.3127	1.1867
CK	→	Q	↓	0.1279	0.1235	0.1117	0.1051	5.4381	3.4675	1.5005	0.7227

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
SI	setup	↑	→	CK	0.0820	0.0820	0.0859	0.0938
	setup	↓	→	CK	0.1992	0.1992	0.2031	0.2188
	hold	↑	→	CK	-0.0664	-0.0664	-0.0664	-0.0703
	hold	↓	→	CK	-0.1641	-0.1641	-0.1641	-0.1680
SE	setup	↑	→	CK	0.1992	0.2031	0.2070	0.2148
	setup	↓	→	CK	0.0977	0.0977	0.0977	0.1055
	hold	↑	→	CK	-0.0625	-0.0625	-0.0625	-0.0664
	hold	↓	→	CK	-0.0391	-0.0391	-0.0391	-0.0430
D	setup	↑	→	CK	0.0703	0.0742	0.0742	0.0820
	setup	↓	→	CK	0.0742	0.0781	0.0820	0.0898
	hold	↑	→	CK	-0.0586	-0.0586	-0.0586	-0.0586
	hold	↓	→	CK	-0.0391	-0.0391	-0.0391	-0.0430
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The SDFFR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN).

Logic Symbol
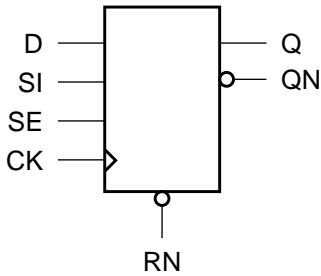
Function Table

RN	D	SI	SE	CK	Q[n+1]	QN[n+1]
1	1	x	0	⌐	1	0
1	0	x	0	⌐	0	1
1	x	x	x	⌐	Q[n]	QN[n]
1	x	1	1	⌐	1	0
1	x	0	1	⌐	0	1
0	x	x	x	x	0	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFRXLAD	2.52	8.40
SDFFRX1AD	2.52	8.40
SDFFRX2AD	2.52	8.40
SDFFRX4AD	2.52	8.96

Functional Schematic
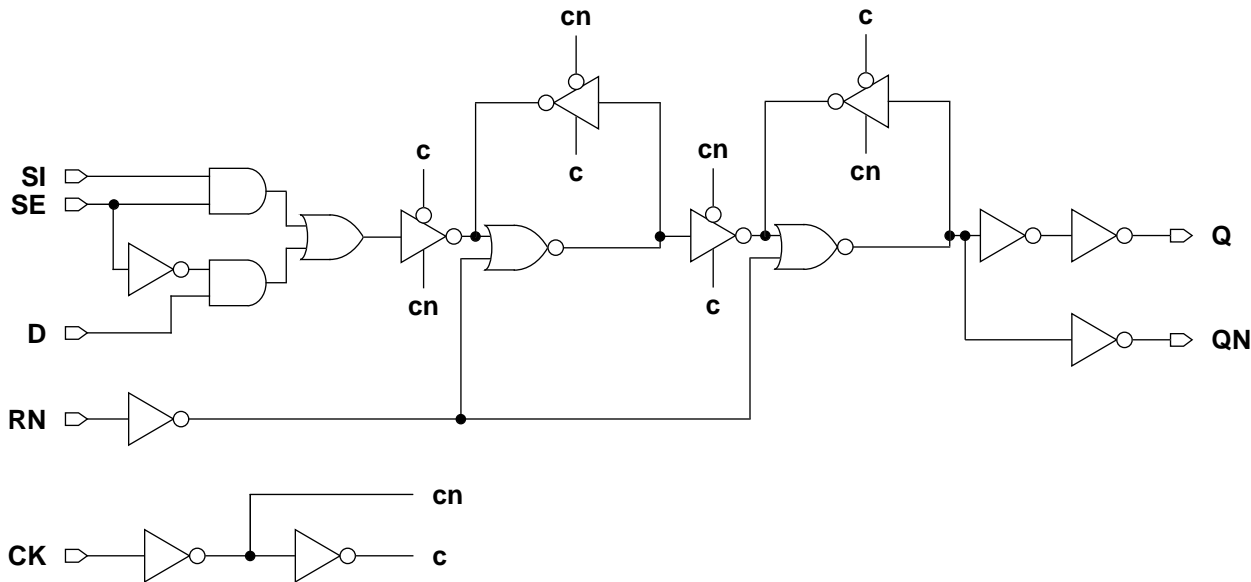
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
SI	0.0065	0.0067	0.0083	0.0094
SE	0.0074	0.0076	0.0090	0.0100
D	0.0063	0.0065	0.0080	0.0092
CK	0.0097	0.0099	0.0116	0.0130
RN	0.0013	0.0014	0.0016	0.0022
Q	0.0050	0.0061	0.0089	0.0155

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
SI	0.0009	0.0009	0.0008	0.0009
SE	0.0022	0.0022	0.0022	0.0026
D	0.0010	0.0010	0.0010	0.0014
CK	0.0017	0.0017	0.0018	0.0022
RN	0.0037	0.0037	0.0038	0.0046

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1360	0.1460	0.1324	0.1479	5.7951	3.7251	2.3869	1.2285
CK	→	Q	↓	0.1509	0.1555	0.1653	0.1677	4.7198	3.2088	1.4499	0.7159
RN	→	Q	↓	0.0709	0.0792	0.0907	0.0832	4.7896	3.2251	1.4656	0.7230
CK	→	QN	↑	0.0936	0.0904	0.0898	0.0902	5.8728	3.7207	2.3856	1.2620
CK	→	QN	↓	0.0892	0.0957	0.0806	0.0884	5.0279	3.3903	1.3960	0.7398
RN	→	QN	↑	0.1348	0.1315	0.1686	0.1900	5.7950	3.7189	2.4187	1.2954

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
SI	setup	↑	→	CK	0.0859	0.0859	0.0938	0.0859
	setup	↓	→	CK	0.1328	0.1289	0.1445	0.1445
	hold	↑	→	CK	-0.0469	-0.0508	-0.0547	-0.0391
	hold	↓	→	CK	-0.0703	-0.0703	-0.0742	-0.0703
SE	setup	↑	→	CK	0.1406	0.1328	0.1484	0.1523
	setup	↓	→	CK	0.0977	0.0977	0.1016	0.0938
	hold	↑	→	CK	-0.0391	-0.0430	-0.0430	-0.0312
	hold	↓	→	CK	-0.0312	-0.0312	-0.0352	-0.0156
D	setup	↑	→	CK	0.0742	0.0742	0.0820	0.0703
	setup	↓	→	CK	0.0977	0.0938	0.1094	0.0742
	hold	↑	→	CK	-0.0430	-0.0430	-0.0469	-0.0312
	hold	↓	→	CK	-0.0469	-0.0469	-0.0508	-0.0273
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.0820	0.0820	0.0898	0.0742
	removal				-0.0625	-0.0664	-0.0664	-0.0586

Cell Description

The SDFFRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol
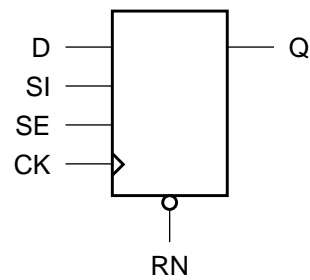
Function Table

RN	D	SI	SE	CK	Q[n+1]
1	1	x	0	⌐⌐	1
1	0	x	0	⌐⌐	0
1	x	x	x	⌐⌐	Q[n]
1	x	1	1	⌐⌐	1
1	x	0	1	⌐⌐	0
0	x	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFRHQX1AD	2.52	9.52
SDFFRHQX2AD	2.52	9.52
SDFFRHQX4AD	2.52	11.20
SDFFRHQX8AD	2.52	12.32

Functional Schematic
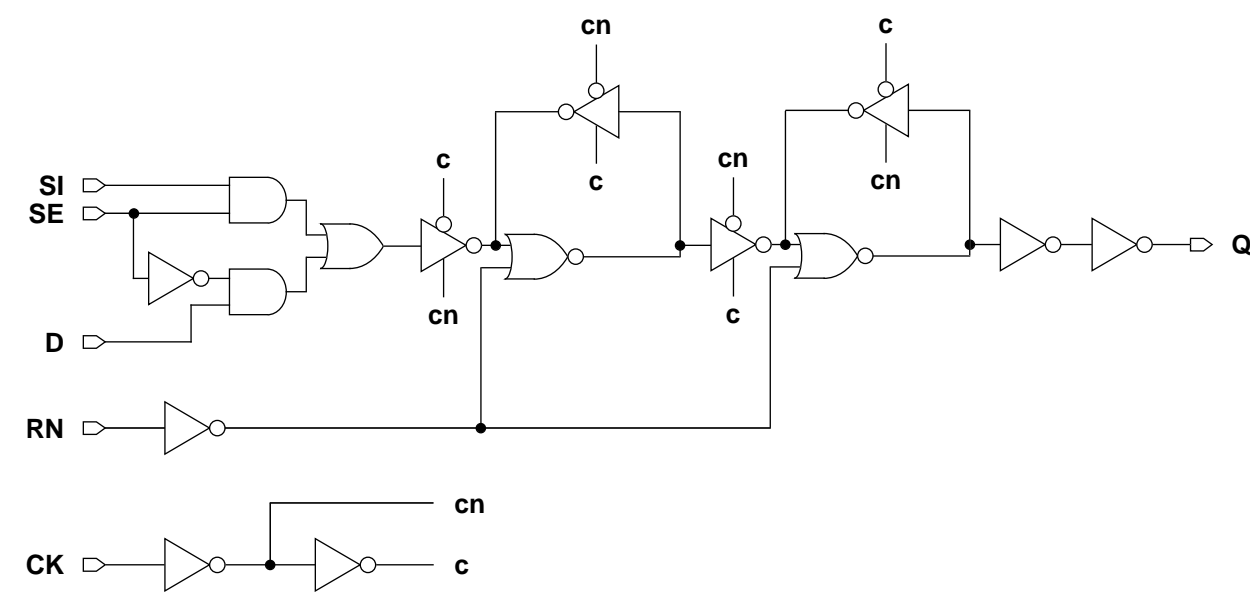
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
SI	0.0088	0.0107	0.0167	0.0184
SE	0.0100	0.0118	0.0181	0.0195
D	0.0093	0.0116	0.0172	0.0185
CK	0.0145	0.0175	0.0270	0.0315
RN	0.0016	0.0019	0.0030	0.0037
Q	0.0043	0.0055	0.0090	0.0160

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
SI	0.0012	0.0012	0.0017	0.0021
SE	0.0030	0.0032	0.0041	0.0044
D	0.0017	0.0023	0.0027	0.0027
CK	0.0021	0.0023	0.0031	0.0054
RN	0.0024	0.0029	0.0045	0.0051

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→	Q	↑	0.0874	0.0815	0.0772	0.0813	3.7027	2.3542	1.1954	0.6182
CK	→	Q	↓	0.0863	0.0782	0.0774	0.0811	3.2703	1.3907	0.6853	0.3552
RN	→	Q	↓	0.0926	0.0828	0.0699	0.0650	3.3291	1.4864	0.7176	0.3476

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
SI	setup	↑	→	CK	0.0820	0.0742	0.0781	0.0625
	setup	↓	→	CK	0.1172	0.1211	0.1172	0.1016
	hold	↑	→	CK	-0.0312	-0.0352	-0.0352	-0.0156
	hold	↓	→	CK	-0.0781	-0.0820	-0.0820	-0.0664
SE	setup	↑	→	CK	0.1289	0.1328	0.1406	0.1250
	setup	↓	→	CK	0.1016	0.0820	0.0859	0.0938
	hold	↑	→	CK	-0.0234	-0.0273	-0.0273	-0.0117
	hold	↓	→	CK	-0.0352	-0.0195	-0.0195	-0.0273
D	setup	↑	→	CK	0.0859	0.0625	0.0586	0.0625
	setup	↓	→	CK	0.0742	0.0508	0.0508	0.0586
	hold	↑	→	CK	-0.0391	-0.0234	-0.0195	-0.0195
	hold	↓	→	CK	-0.0352	-0.0195	-0.0234	-0.0273
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0156	-0.0195	-0.0234	-0.0156
	removal				0.0391	0.0469	0.0664	0.0586

Cell Description

The SDFFRQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN). The cell has a single output (Q).

Logic Symbol
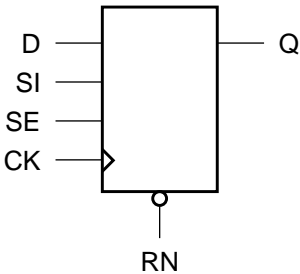
Function Table

RN	D	SI	SE	CK	Q[n+1]
1	1	x	0	⌐⌐	1
1	0	x	0	⌐⌐	0
1	x	x	x	⌐⌐	Q[n]
1	x	1	1	⌐⌐	1
1	x	0	1	⌐⌐	0
0	x	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFRQXLAD	2.52	7.84
SDFFRQX1AD	2.52	7.84
SDFFRQX2AD	2.52	7.84
SDFFRQX4AD	2.52	8.40

Functional Schematic
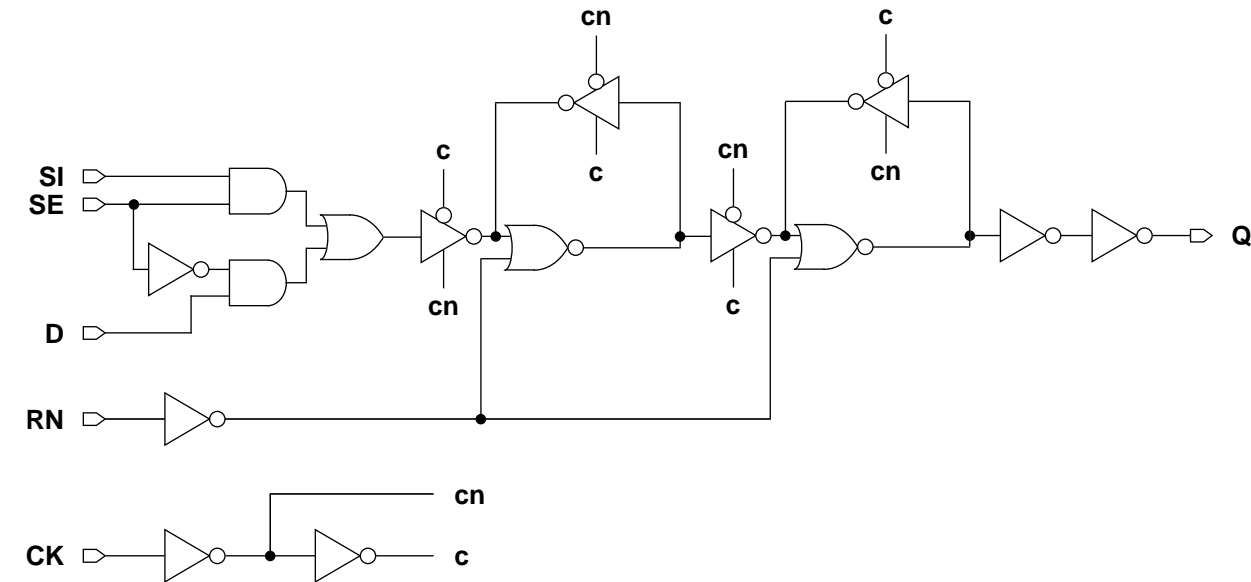
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
SI	0.0065	0.0065	0.0065	0.0067
SE	0.0074	0.0074	0.0074	0.0076
D	0.0063	0.0063	0.0063	0.0065
CK	0.0096	0.0096	0.0097	0.0097
RN	0.0014	0.0014	0.0013	0.0017
Q	0.0038	0.0042	0.0057	0.0094

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
SI	0.0009	0.0009	0.0008	0.0008
SE	0.0022	0.0022	0.0022	0.0022
D	0.0010	0.0010	0.0010	0.0010
CK	0.0017	0.0017	0.0018	0.0017
RN	0.0038	0.0038	0.0037	0.0044

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1191	0.1220	0.1172	0.1202	5.7405	3.6613	2.3361	1.1993
CK	→	Q	↓	0.1426	0.1505	0.1575	0.1561	4.4545	3.2727	1.4780	0.7230
RN	→	Q	↓	0.0700	0.0785	0.0870	0.0810	4.5277	3.2722	1.4584	0.7120

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
SI	setup	↑	→	CK	0.0898	0.0898	0.0898	0.0859
	setup	↓	→	CK	0.1328	0.1328	0.1289	0.1328
	hold	↑	→	CK	-0.0508	-0.0508	-0.0508	-0.0508
	hold	↓	→	CK	-0.0703	-0.0703	-0.0703	-0.0703
SE	setup	↑	→	CK	0.1406	0.1406	0.1367	0.1367
	setup	↓	→	CK	0.0977	0.0977	0.0977	0.0977
	hold	↑	→	CK	-0.0391	-0.0430	-0.0430	-0.0391
	hold	↓	→	CK	-0.0312	-0.0312	-0.0352	-0.0312
D	setup	↑	→	CK	0.0781	0.0781	0.0781	0.0742
	setup	↓	→	CK	0.0977	0.0977	0.0977	0.1016
	hold	↑	→	CK	-0.0430	-0.0430	-0.0430	-0.0430
	hold	↓	→	CK	-0.0469	-0.0469	-0.0508	-0.0469
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.0820	0.0820	0.0820	0.0820
	removal				-0.0625	-0.0625	-0.0625	-0.0625

Cell Description

The SDFFS cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN).

Logic Symbol
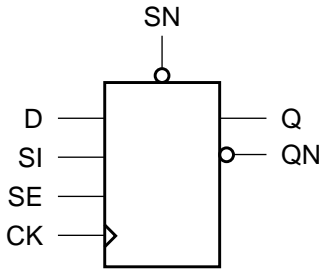
Function Table

SN	D	SI	SE	CK	Q[n+1]	QN[n+1]
1	1	x	0	⌐	1	0
1	0	x	0	⌐	0	1
1	x	x	x	⌐	Q[n]	QN[n]
1	x	1	1	⌐	1	0
1	x	0	1	⌐	0	1
0	x	x	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFSXLAD	2.52	7.56
SDFFSX1AD	2.52	7.56
SDFFSX2AD	2.52	7.56
SDFFSX4AD	2.52	8.68

Functional Schematic
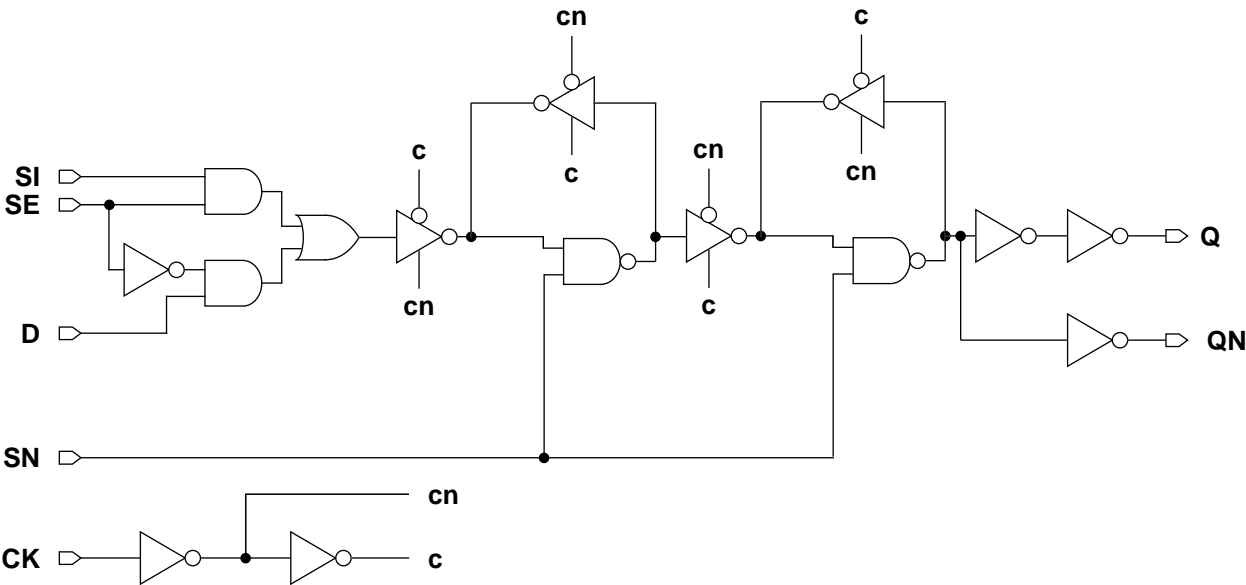
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
SI	0.0068	0.0068	0.0076	0.0108
SE	0.0077	0.0077	0.0082	0.0110
D	0.0063	0.0063	0.0070	0.0099
CK	0.0110	0.0110	0.0118	0.0149
SN	0.0013	0.0014	0.0015	0.0019
Q	0.0056	0.0065	0.0090	0.0153

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
SI	0.0015	0.0015	0.0015	0.0015
SE	0.0024	0.0024	0.0023	0.0023
D	0.0013	0.0013	0.0013	0.0013
CK	0.0019	0.0019	0.0020	0.0021
SN	0.0019	0.0019	0.0022	0.0029

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1433	0.1517	0.1548	0.1529	5.6726	3.7750	2.3658	1.2196
CK	→	Q	↓	0.1460	0.1553	0.1549	0.1585	4.2245	3.1250	1.3842	0.7025
SN	→	Q	↑	0.1283	0.1359	0.1648	0.2338	5.6378	3.7566	2.3622	1.2196
CK	→	QN	↑	0.1045	0.1058	0.0983	0.0889	5.9530	3.9208	2.4012	1.2491
CK	→	QN	↓	0.1065	0.1151	0.1027	0.0905	5.3564	3.7679	1.6149	0.7536
SN	→	QN	↓	0.0944	0.1019	0.1116	0.1537	4.6405	3.3314	1.5420	0.8343

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
SI	setup	↑	→	CK	0.0977	0.0938	0.0898	0.1016
	setup	↓	→	CK	0.1289	0.1289	0.1289	0.1562
	hold	↑	→	CK	-0.0508	-0.0508	-0.0547	-0.0625
	hold	↓	→	CK	-0.0703	-0.0703	-0.0742	-0.0898
SE	setup	↑	→	CK	0.1445	0.1406	0.1445	0.1680
	setup	↓	→	CK	0.1250	0.1211	0.1172	0.1250
	hold	↑	→	CK	-0.0391	-0.0391	-0.0430	-0.0508
	hold	↓	→	CK	-0.0312	-0.0312	-0.0312	-0.0469
D	setup	↑	→	CK	0.0977	0.0938	0.0898	0.0977
	setup	↓	→	CK	0.0977	0.0977	0.1016	0.1211
	hold	↑	→	CK	-0.0508	-0.0508	-0.0547	-0.0586
	hold	↓	→	CK	-0.0469	-0.0508	-0.0508	-0.0664
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0273	-0.0273	-0.0312	-0.0312
	removal				0.0469	0.0469	0.0508	0.0508

Cell Description

The SDFFSHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol
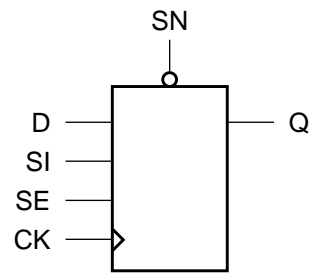
Function Table

SN	D	SI	SE	CK	Q[n+1]
1	1	x	0	⟋	1
1	0	x	0	⟋	0
1	x	x	x	⟍	Q[n]
1	x	1	1	⟋	1
1	x	0	1	⟋	0
0	x	x	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFSHQX1AD	2.52	9.52
SDFFSHQX2AD	2.52	9.52
SDFFSHQX4AD	2.52	11.48
SDFFSHQX8AD	2.52	12.32

Functional Schematic
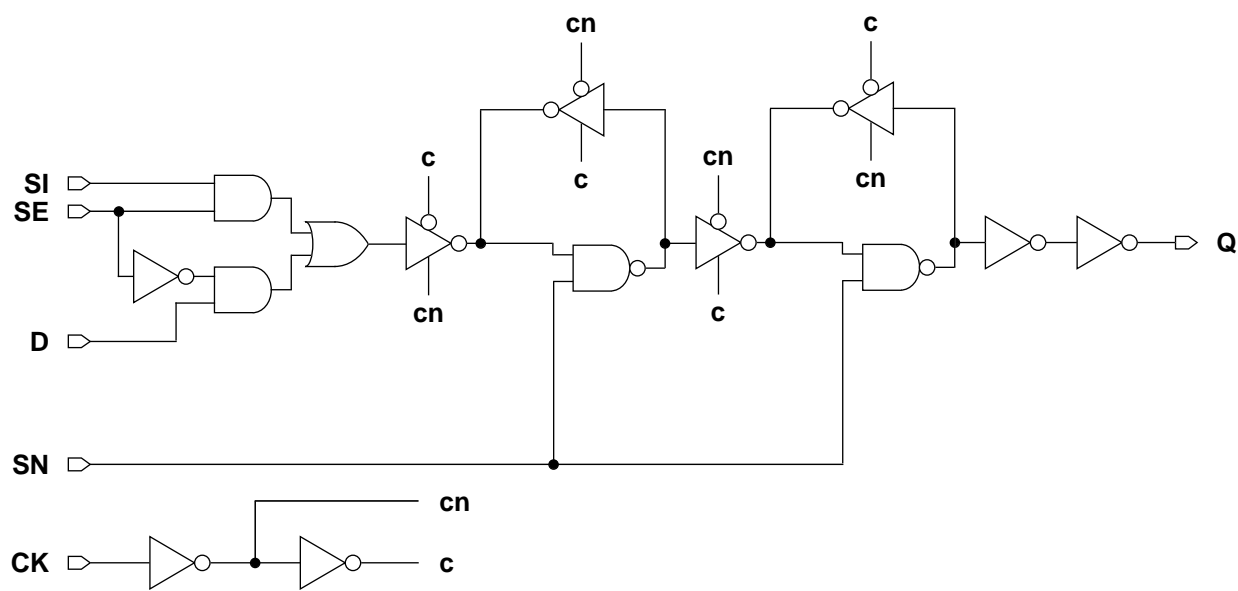
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
SI	0.0083	0.0098	0.0132	0.0146
SE	0.0097	0.0113	0.0150	0.0164
D	0.0083	0.0101	0.0141	0.0148
CK	0.0139	0.0163	0.0223	0.0239
SN	0.0037	0.0039	0.0048	0.0054
Q	0.0044	0.0058	0.0093	0.0160

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
SI	0.0012	0.0012	0.0014	0.0020
SE	0.0028	0.0031	0.0036	0.0040
D	0.0013	0.0017	0.0023	0.0023
CK	0.0021	0.0022	0.0031	0.0040
SN	0.0024	0.0027	0.0030	0.0031

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→	Q	↑	0.0805	0.0761	0.0703	0.0746	3.6529	2.3497	1.2020	0.6187
CK	→	Q	↓	0.0873	0.0840	0.0745	0.0808	3.2289	1.4193	0.6879	0.3551
SN	→	Q	↑	0.1317	0.1497	0.1154	0.1204	3.9621	2.3958	1.1956	0.6117

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
SI	setup	↑	→	CK	0.0859	0.0742	0.0859	0.0703
	setup	↓	→	CK	0.1133	0.1211	0.1367	0.1016
	hold	↑	→	CK	-0.0430	-0.0391	-0.0430	-0.0273
	hold	↓	→	CK	-0.0781	-0.0820	-0.0898	-0.0586
SE	setup	↑	→	CK	0.1289	0.1406	0.1602	0.1211
	setup	↓	→	CK	0.1016	0.0781	0.0820	0.0938
	hold	↑	→	CK	-0.0352	-0.0312	-0.0352	-0.0195
	hold	↓	→	CK	-0.0352	-0.0195	-0.0234	-0.0273
D	setup	↑	→	CK	0.0820	0.0586	0.0625	0.0664
	setup	↓	→	CK	0.0859	0.0664	0.0703	0.0742
	hold	↑	→	CK	-0.0430	-0.0273	-0.0195	-0.0234
	hold	↓	→	CK	-0.0508	-0.0312	-0.0312	-0.0352
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.0234	0.0195	0.0312	0.0352
	removal				-0.0117	-0.0078	-0.0156	-0.0195

Cell Description

The SDFFSQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN). The cell has a single output (Q).

Logic Symbol
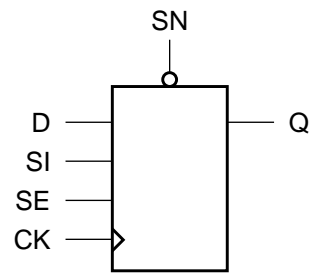
Function Table

| SN	D	SI	SE	CK	Q[n+1]
1	1	x	0	⌐_/	1
1	0	x	0	_/	0
1	x	x	x	‾_	Q[n]
1	x	1	1	_/	1
1	x	0	1	_/	0
0	x	x	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFSQXLAD	2.52	7.00
SDFFSQX1AD	2.52	7.28
SDFFSQX2AD	2.52	7.28
SDFFSQX4AD	2.52	7.56

Functional Schematic
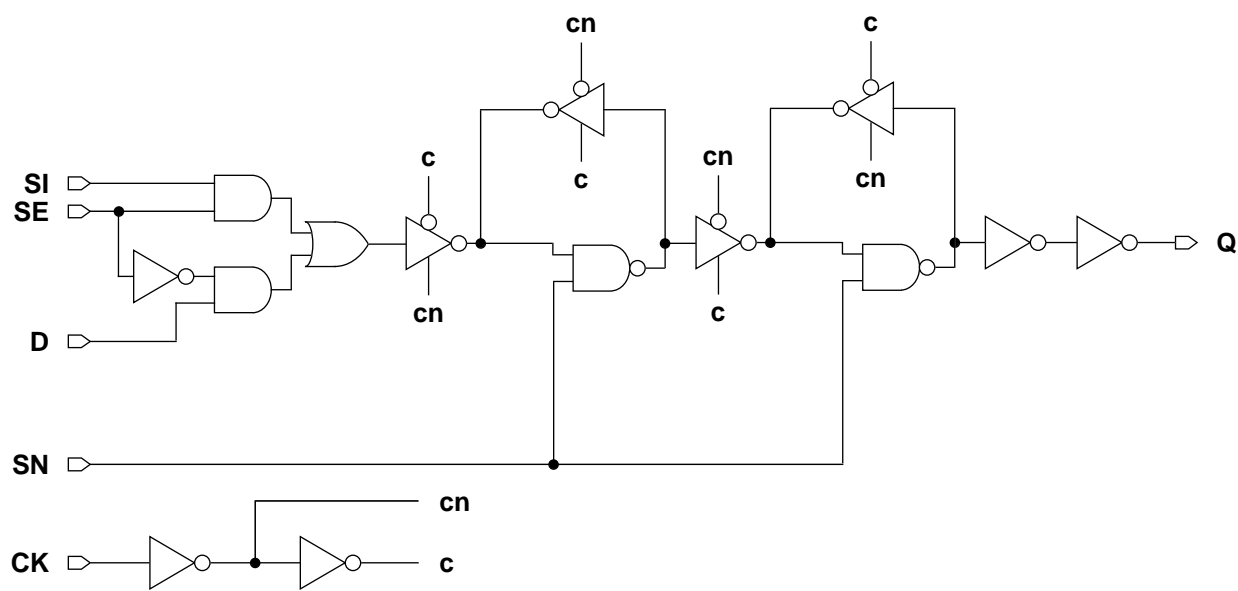
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
SI	0.0070	0.0070	0.0070	0.0072
SE	0.0076	0.0076	0.0077	0.0078
D	0.0064	0.0064	0.0065	0.0066
CK	0.0108	0.0108	0.0108	0.0110
SN	0.0012	0.0013	0.0014	0.0015
Q	0.0040	0.0046	0.0059	0.0097

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
SI	0.0015	0.0015	0.0015	0.0015
SE	0.0023	0.0023	0.0023	0.0023
D	0.0013	0.0013	0.0013	0.0013
CK	0.0020	0.0020	0.0020	0.0020
SN	0.0019	0.0020	0.0019	0.0020

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1185	0.1221	0.1305	0.1441	5.4738	3.6354	2.3520	1.2002
CK	→	Q	↓	0.1310	0.1392	0.1454	0.1588	4.5829	3.1774	1.4017	0.7120
SN	→	Q	↑	0.1084	0.1150	0.1214	0.1332	5.4546	3.6256	2.3479	1.1979

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	X1	X2	X4
SI	setup	↑	→	CK	0.1094	0.1094	0.1016	0.1016
	setup	↓	→	CK	0.1328	0.1367	0.1328	0.1328
	hold	↑	→	CK	-0.0547	-0.0547	-0.0547	-0.0547
	hold	↓	→	CK	-0.0703	-0.0742	-0.0703	-0.0742
SE	setup	↑	→	CK	0.1445	0.1484	0.1445	0.1445
	setup	↓	→	CK	0.1367	0.1367	0.1328	0.1289
	hold	↑	→	CK	-0.0430	-0.0430	-0.0430	-0.0430
	hold	↓	→	CK	-0.0312	-0.0312	-0.0312	-0.0352
D	setup	↑	→	CK	0.1094	0.1094	0.1055	0.1016
	setup	↓	→	CK	0.1016	0.1055	0.1016	0.1016
	hold	↑	→	CK	-0.0547	-0.0547	-0.0547	-0.0547
	hold	↓	→	CK	-0.0508	-0.0508	-0.0508	-0.0508
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0234	-0.0234	-0.0273	-0.0273
	removal				0.0430	0.0430	0.0430	0.0430

Cell Description

The SDFFSR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN). Set (SN) dominates reset (RN).

Logic Symbol
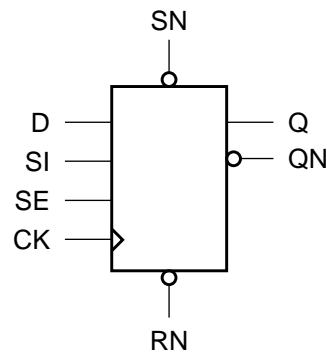
Function Table

RN	SN	D	SI	SE	CK	Q[n+1]	QN[n+1]
1	1	1	x	0	⌐	1	0
1	1	0	x	0	⌐	0	1
1	1	x	x	x	⌐	Q[n]	QN[n]
1	1	x	1	1	⌐	1	0
1	1	x	0	1	⌐	0	1
0	1	x	x	x	x	0	1
1	0	x	x	x	x	1	0
0	0	x	x	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFSRXLAD	2.52	9.24
SDFFSRX1AD	2.52	9.52
SDFFSRX2AD	2.52	9.80
SDFFSRX4AD	2.52	11.76

Functional Schematic
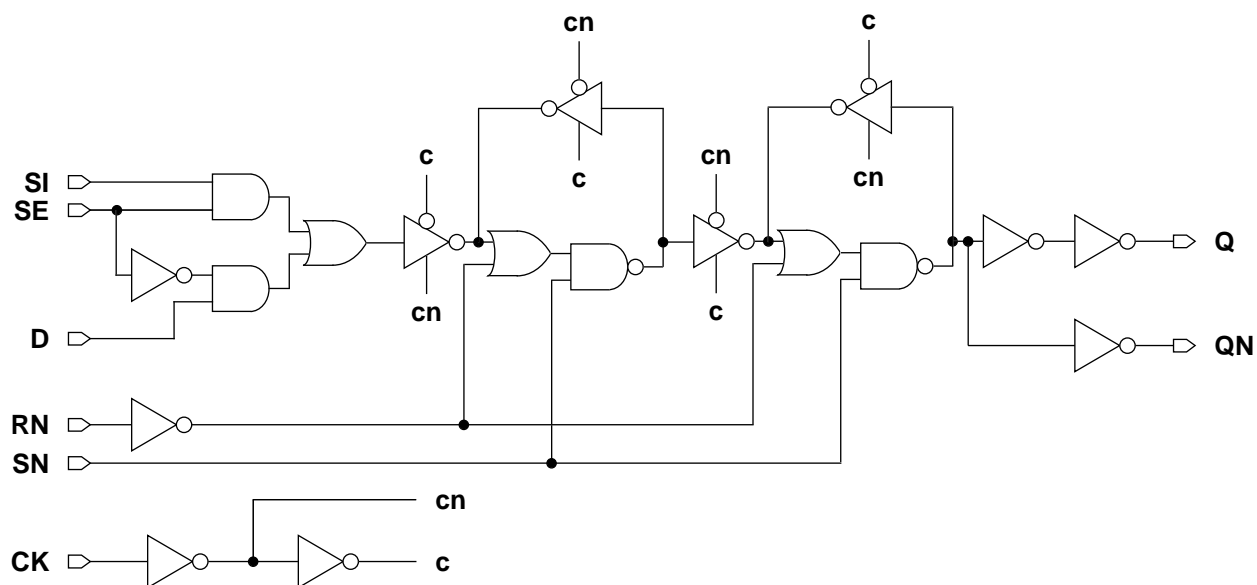
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
SI	0.0075	0.0075	0.0086	0.0132
SE	0.0086	0.0086	0.0095	0.0133
D	0.0070	0.0071	0.0081	0.0121
CK	0.0116	0.0117	0.0132	0.0188
SN	0.0014	0.0014	0.0016	0.0020
RN	0.0027	0.0027	0.0029	0.0035
Q	0.0061	0.0073	0.0102	0.0154

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
SI	0.0013	0.0013	0.0013	0.0013
SE	0.0024	0.0024	0.0024	0.0024
D	0.0013	0.0013	0.0013	0.0014
CK	0.0017	0.0017	0.0019	0.0022
SN	0.0021	0.0020	0.0023	0.0031
RN	0.0012	0.0012	0.0012	0.0012

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1525	0.1611	0.1662	0.1568	5.7263	3.6909	2.3772	1.2206
CK	→	Q	↓	0.1563	0.1660	0.1637	0.1681	4.2554	3.1336	1.3767	0.7023
SN	→	Q	↑	0.1432	0.1510	0.1833	0.2489	5.6721	3.6597	2.3708	1.2196
SN	→	Q	↓	0.1246	0.1333	0.1455	0.1672	4.2160	3.1168	1.3730	0.7024
RN	→	Q	↓	0.1470	0.1556	0.1743	0.2122	4.2284	3.1212	1.3739	0.7027
CK	→	QN	↑	0.1123	0.1126	0.1076	0.0988	6.1459	3.9296	2.4483	1.2506
CK	→	QN	↓	0.1153	0.1241	0.1131	0.0936	5.7254	4.0087	1.6808	0.7655
SN	→	QN	↑	0.0818	0.0817	0.0874	0.0901	5.9211	3.7985	2.4390	1.2712
SN	→	QN	↓	0.1095	0.1171	0.1297	0.1674	4.7769	3.4068	1.5702	0.8446
RN	→	QN	↑	0.1031	0.1031	0.1158	0.1377	6.0026	3.8351	2.4479	1.2781

Timing Constraints at 25°C,1.0V, Typical Process

| Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
SI	setup	↑	→	CK	0.1250	0.1211	0.1055	0.1250
	setup	↓	→	CK	0.1445	0.1406	0.1445	0.1758
	hold	↑	→	CK	-0.0547	-0.0547	-0.0586	-0.0703
	hold	↓	→	CK	-0.0781	-0.0781	-0.0820	-0.0977
SE	setup	↑	→	CK	0.1562	0.1562	0.1602	0.1953
	setup	↓	→	CK	0.1562	0.1523	0.1367	0.1328
	hold	↑	→	CK	-0.0430	-0.0430	-0.0469	-0.0586
	hold	↓	→	CK	-0.0352	-0.0391	-0.0391	-0.0469
D	setup	↑	→	CK	0.1250	0.1250	0.1094	0.1055
	setup	↓	→	CK	0.1133	0.1133	0.1133	0.1289
	hold	↑	→	CK	-0.0547	-0.0547	-0.0586	-0.0547
	hold	↓	→	CK	-0.0547	-0.0586	-0.0586	-0.0664
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0234	-0.0234	-0.0312	-0.0352
	removal				0.0430	0.0430	0.0508	0.0625
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.0781	0.0742	0.0508	0.0547
	removal				-0.0234	-0.0234	-0.0156	-0.0117

Cell Description

The SDFFSRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN), and set dominating reset. The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol
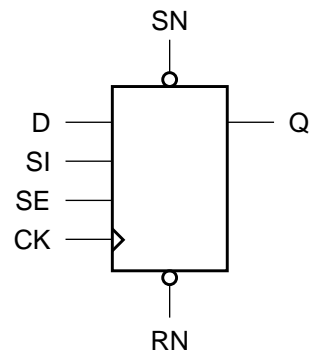
Function Table

RN	SN	D	SI	SE	CK	Q[n+1]
1	1	1	x	0	⌐⌐	1
1	1	0	x	0	⌐⌐	0
1	1	x	x	x	⌐⌐	Q[n]
1	1	x	1	1	⌐⌐	1
1	1	x	0	1	⌐⌐	0
0	1	x	x	x	x	0
1	0	x	x	x	x	1
0	0	x	x	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFSRHQX1AD	2.52	11.48
SDFFSRHQX2AD	2.52	11.48
SDFFSRHQX4AD	2.52	13.72
SDFFSRHQX8AD	2.52	14.56

Functional Schematic
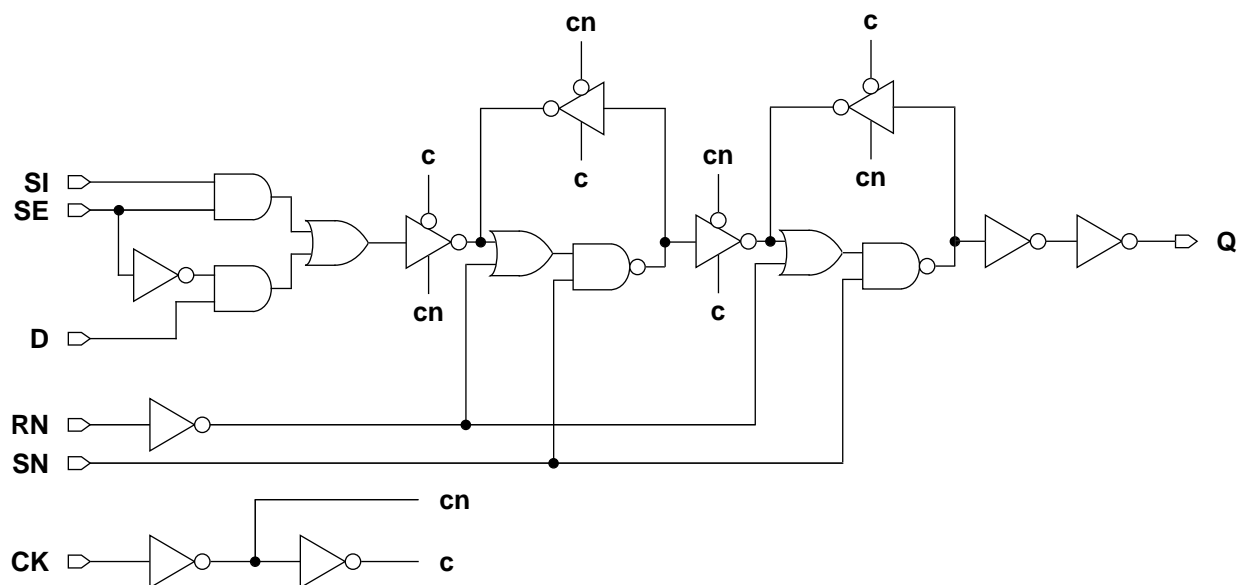
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
SI	0.0089	0.0104	0.0156	0.0178
SE	0.0101	0.0116	0.0165	0.0188
D	0.0089	0.0107	0.0162	0.0181
CK	0.0149	0.0172	0.0248	0.0288
SN	0.0045	0.0047	0.0061	0.0073
RN	0.0015	0.0018	0.0028	0.0036
Q	0.0052	0.0067	0.0101	0.0176

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
SI	0.0013	0.0013	0.0016	0.0021
SE	0.0030	0.0030	0.0034	0.0041
D	0.0012	0.0016	0.0024	0.0027
CK	0.0022	0.0021	0.0028	0.0041
SN	0.0023	0.0026	0.0033	0.0037
RN	0.0019	0.0023	0.0035	0.0040

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→ Q	↑	0.0983	0.0923	0.0855	0.0839	3.7899	2.3849	1.2074	0.6276
CK	→ Q	↓	0.1022	0.0918	0.0863	0.0806	3.4691	1.4659	0.7114	0.3658
SN	→ Q	↑	0.1090	0.1286	0.1682	0.1487	3.6654	2.3658	1.2009	0.6149
SN	→ Q	↓	0.2105	0.1883	0.1743	0.1926	3.7265	1.7091	0.8403	0.4311
RN	→ Q	↓	0.1837	0.1566	0.1353	0.1620	3.7366	1.7099	0.8418	0.4318

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
SI	setup	↑	→	CK	0.0938	0.0859	0.0938	0.0938
	setup	↓	→	CK	0.1211	0.1133	0.1055	0.1250
	hold	↑	→	CK	-0.0430	-0.0391	-0.0430	-0.0312
	hold	↓	→	CK	-0.0781	-0.0742	-0.0625	-0.0703
SE	setup	↑	→	CK	0.1406	0.1328	0.1250	0.1484
	setup	↓	→	CK	0.1211	0.1016	0.1172	0.1289
	hold	↑	→	CK	-0.0352	-0.0312	-0.0352	-0.0273
	hold	↓	→	CK	-0.0430	-0.0312	-0.0273	-0.0273
D	setup	↑	→	CK	0.0977	0.0781	0.0859	0.0977
	setup	↓	→	CK	0.0938	0.0703	0.0625	0.0742
	hold	↑	→	CK	-0.0430	-0.0312	-0.0352	-0.0312
	hold	↓	→	CK	-0.0547	-0.0352	-0.0234	-0.0273
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.0312	0.0195	0.0195	0.0391
	removal				-0.0156	-0.0078	-0.0078	-0.0156
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0156	-0.0234	-0.0195	-0.0039
	removal				0.0391	0.0469	0.0586	0.0391

Cell Description

The SDFFTR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-low reset (RN). Scan enable (SE) dominates reset (RN).

Logic Symbol
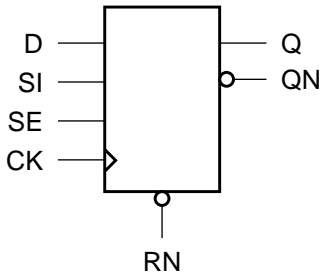
Function Table

RN	D	SI	SE	CK	Q[n+1]	QN[n+1]
x	x	0	1	⌐⌐	0	1
x	x	1	1	⌐⌐	1	0
0	x	x	0	⌐⌐	0	1
1	0	x	0	⌐⌐	0	1
1	1	x	0	⌐⌐	1	0
x	x	x	x	⌐⌐	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFTRXLAD	2.52	7.84
SDFFTRX1AD	2.52	8.12
SDFFTRX2AD	2.52	8.12
SDFFTRX4AD	2.52	10.08

Functional Schematic

TSMC CLN90G
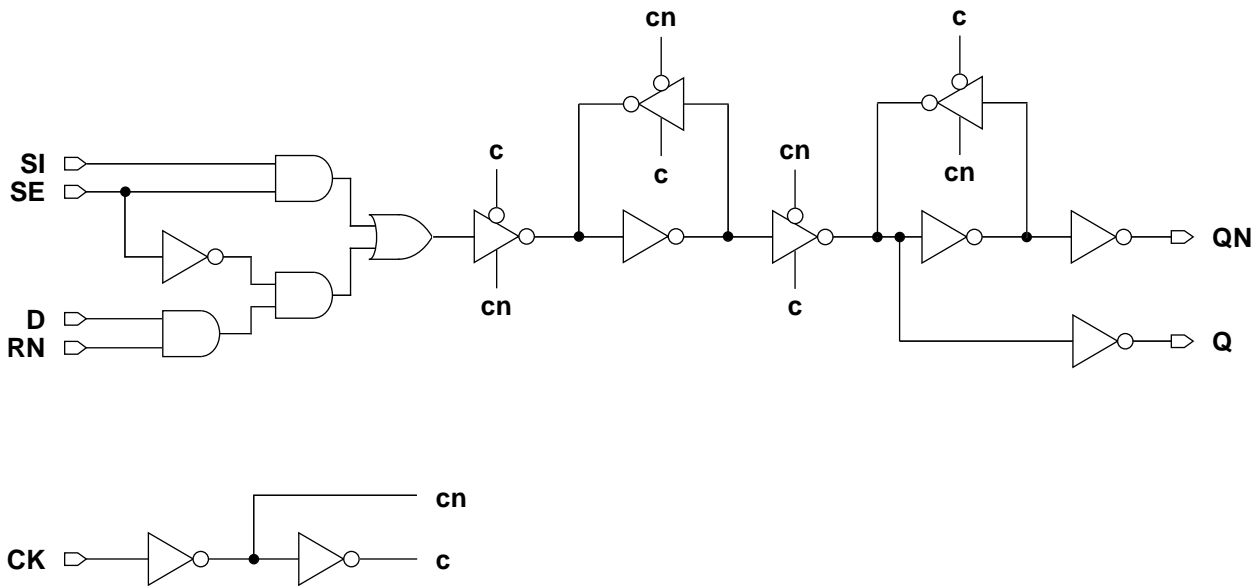
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
SI	0.0072	0.0080	0.0095	0.0163
SE	0.0087	0.0093	0.0107	0.0155
D	0.0069	0.0075	0.0088	0.0139
CK	0.0100	0.0106	0.0122	0.0192
RN	0.0077	0.0084	0.0101	0.0182
Q	0.0053	0.0061	0.0086	0.0142

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
SI	0.0012	0.0012	0.0012	0.0013
SE	0.0037	0.0037	0.0037	0.0041
D	0.0010	0.0010	0.0010	0.0013
CK	0.0018	0.0018	0.0018	0.0023
RN	0.0018	0.0018	0.0018	0.0022

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1196	0.1168	0.1209	0.1115	5.6609	3.6440	2.3621	1.2097
CK	→	Q	↓	0.1349	0.1380	0.1426	0.1326	4.2140	3.1077	1.3670	0.6634
CK	→	QN	↑	0.0935	0.0889	0.0903	0.0850	5.8476	3.6893	2.3583	1.2146
CK	→	QN	↓	0.0882	0.0858	0.0803	0.0722	5.0499	3.2728	1.3836	0.6715

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
SI	setup	↑	→	CK	0.0859	0.0859	0.0859	0.1055
	setup	↓	→	CK	0.1484	0.1523	0.1641	0.1992
	hold	↑	→	CK	-0.0469	-0.0508	-0.0508	-0.0586
	hold	↓	→	CK	-0.0820	-0.0859	-0.0938	-0.1094
SE	setup	↑	→	CK	0.1562	0.1602	0.1719	0.2109
	setup	↓	→	CK	0.1172	0.1172	0.1172	0.1133
	hold	↑	→	CK	-0.0391	-0.0430	-0.0430	-0.0508
	hold	↓	→	CK	-0.0430	-0.0469	-0.0547	-0.0391
D	setup	↑	→	CK	0.0938	0.0938	0.0938	0.0859
	setup	↓	→	CK	0.1133	0.1133	0.1250	0.1094
	hold	↑	→	CK	-0.0508	-0.0547	-0.0547	-0.0469
	hold	↓	→	CK	-0.0586	-0.0586	-0.0664	-0.0547
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
RN	setup	↑	→	CK	0.0977	0.0977	0.0977	0.0898
	setup	↓	→	CK	0.1602	0.1641	0.1758	0.2227
	hold	↑	→	CK	-0.0547	-0.0586	-0.0586	-0.0508
	hold	↓	→	CK	-0.0859	-0.0898	-0.0977	-0.1211

Cell Description

The SDFFYQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE). The cell has a single output (Q) and overdriven feedback loops to increase mean time between failure (MTBF) due to metastability.
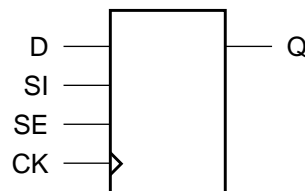
Logic Symbol

Function Table

D	SI	SE	CK	Q[n+1]
1	x	0	⌐/	1
0	x	0	⌐/	0
x	x	x	⌐\	Q[n]
x	1	1	⌐/	1
x	0	1	⌐/	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFYQX2AD	2.52	8.12

Functional Schematic
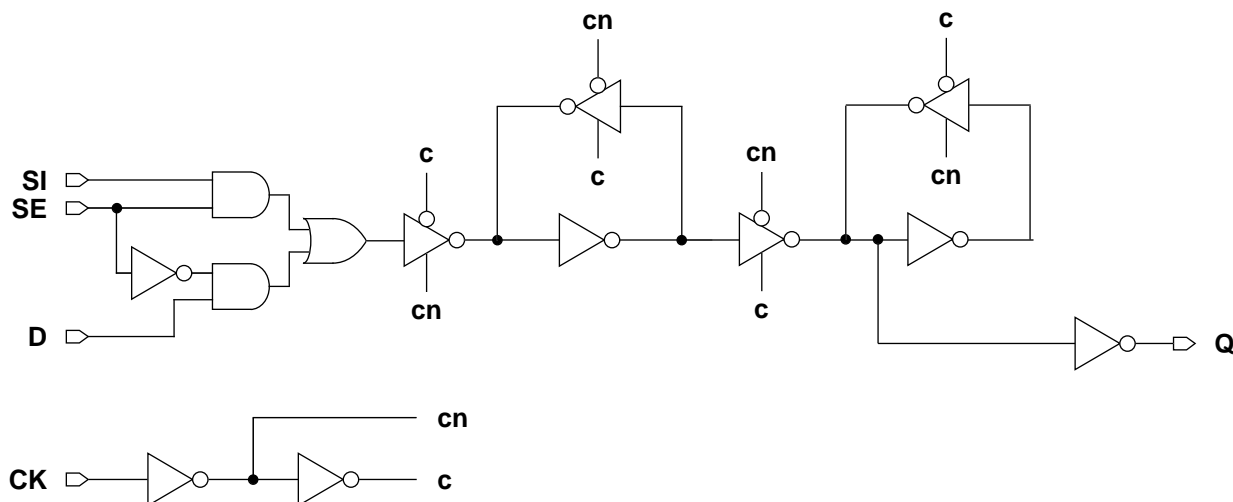
AC Power

Pin	Power (uW/MHz)
	X2
SI	0.0139
SE	0.0149
D	0.0106
CK	0.0198
Q	0.0059

Pin Capacitance

Pin	Capacitance (pF)
	X2
SI	0.0010
SE	0.0051
D	0.0024
CK	0.0024

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X2	**X2**
CK → Q ↑	0.0981	2.3301
CK → Q ↓	0.0990	1.4614

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)
					X2
SI	setup	↑	→	CK	0.1055
	setup	↓	→	CK	0.3125
	hold	↑	→	CK	-0.0938
	hold	↓	→	CK	-0.2852
SE	setup	↑	→	CK	0.3320
	setup	↓	→	CK	0.0859
	hold	↑	→	CK	-0.0898
	hold	↓	→	CK	-0.0391
D	setup	↑	→	CK	0.0312
	setup	↓	→	CK	0.0859
	hold	↑	→	CK	-0.0234
	hold	↓	→	CK	-0.0508
CK	minpwh				0.8332
	minpwl				0.8332

Cell Description

The SEDFF cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-high enable (E).

Logic Symbol
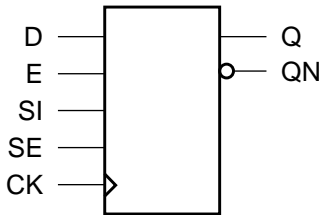
Function Table

D	E	SI	SE	CK	Q[n+1]	QN[n+1]
x	x	1	1	$\_\!\!/^-$	1	0
x	x	0	1	$\_\!\!/^-$	0	1
x	0	x	0	$\_\!\!/^-$	Q[n]	QN[n]
0	1	x	0	$\_\!\!/^-$	0	1
1	1	x	0	$\_\!\!/^-$	1	0
x	x	x	x	$^-\!\!\backslash\_$	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
SEDFFXLAD	2.52	8.68
SEDFFX1AD	2.52	8.96
SEDFFX2AD	2.52	9.24
SEDFFX4AD	2.52	11.48

Functional Schematic
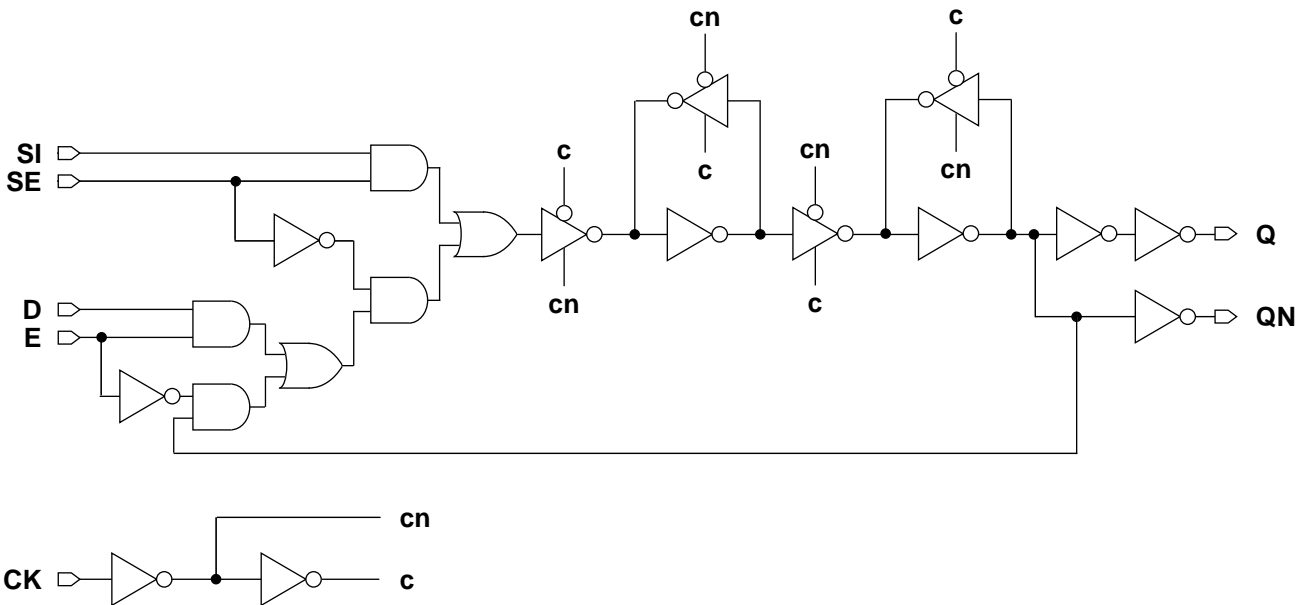
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
SI	0.0073	0.0074	0.0090	0.0103
SE	0.0093	0.0094	0.0107	0.0121
D	0.0063	0.0064	0.0070	0.0082
CK	0.0110	0.0112	0.0119	0.0150
E	0.0089	0.0090	0.0101	0.0114
Q	0.0066	0.0074	0.0104	0.0177

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
SI	0.0010	0.0010	0.0010	0.0010
SE	0.0023	0.0023	0.0027	0.0027
D	0.0010	0.0010	0.0015	0.0014
CK	0.0015	0.0015	0.0015	0.0017
E	0.0025	0.0025	0.0028	0.0028

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q ↑	0.1055	0.0992	0.1001	0.1107	5.8141	3.5994	2.3253	1.2193
CK	→	Q ↓	0.1197	0.1140	0.0994	0.1007	5.0051	3.4149	1.4372	0.7229
CK	→	QN ↑	0.1730	0.1620	0.1493	0.1506	5.7623	3.6489	2.3438	1.2126
CK	→	QN ↓	0.1616	0.1641	0.1561	0.1613	4.4363	3.2442	1.3918	0.6725

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	X1	X2	X4
SI	setup	↑	→	CK	0.0703	0.0742	0.1250	0.1289
	setup	↓	→	CK	0.2734	0.2734	0.2734	0.2969
	hold	↑	→	CK	-0.0625	-0.0625	-0.0898	-0.0898
	hold	↓	→	CK	-0.2188	-0.2188	-0.2227	-0.2305
SE	setup	↑	→	CK	0.2812	0.2812	0.2617	0.2852
	setup	↓	→	CK	0.3047	0.3047	0.1602	0.1680
	hold	↑	→	CK	-0.0508	-0.0508	-0.0938	-0.0938
	hold	↓	→	CK	-0.1055	-0.1055	-0.0898	-0.0820
D	setup	↑	→	CK	0.0820	0.0859	0.1289	0.1328
	setup	↓	→	CK	0.2812	0.2852	0.1133	0.1211
	hold	↑	→	CK	-0.0664	-0.0664	-0.0938	-0.0977
	hold	↓	→	CK	-0.2383	-0.2383	-0.0703	-0.0625
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
E	setup	↑	→	CK	0.3086	0.3086	0.1406	0.1523
	setup	↓	→	CK	0.2578	0.2578	0.1484	0.1562
	hold	↑	→	CK	-0.0664	-0.0664	-0.1016	-0.0977
	hold	↓	→	CK	-0.0977	-0.0977	-0.0664	-0.0586

Cell Description

The SEDFFHQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-high enable (E). The cell has a single output (Q) and fast clock-to-output path.

Logic Symbol
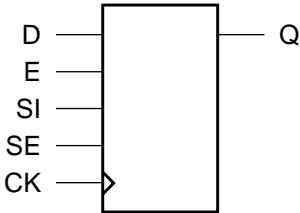
Function Table

D	E	SI	SE	CK	Q[n+1]
x	x	1	1	⟋	1
x	x	0	1	⟋	0
x	0	x	0	⟋	Q[n]
0	1	x	0	⟋	0
1	1	x	0	⟋	1
x	x	x	x	⟍	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
SEDFFHQX1AD	2.52	11.76
SEDFFHQX2AD	2.52	13.44
SEDFFHQX4AD	2.52	15.12
SEDFFHQX8AD	2.52	19.60

Functional Schematic
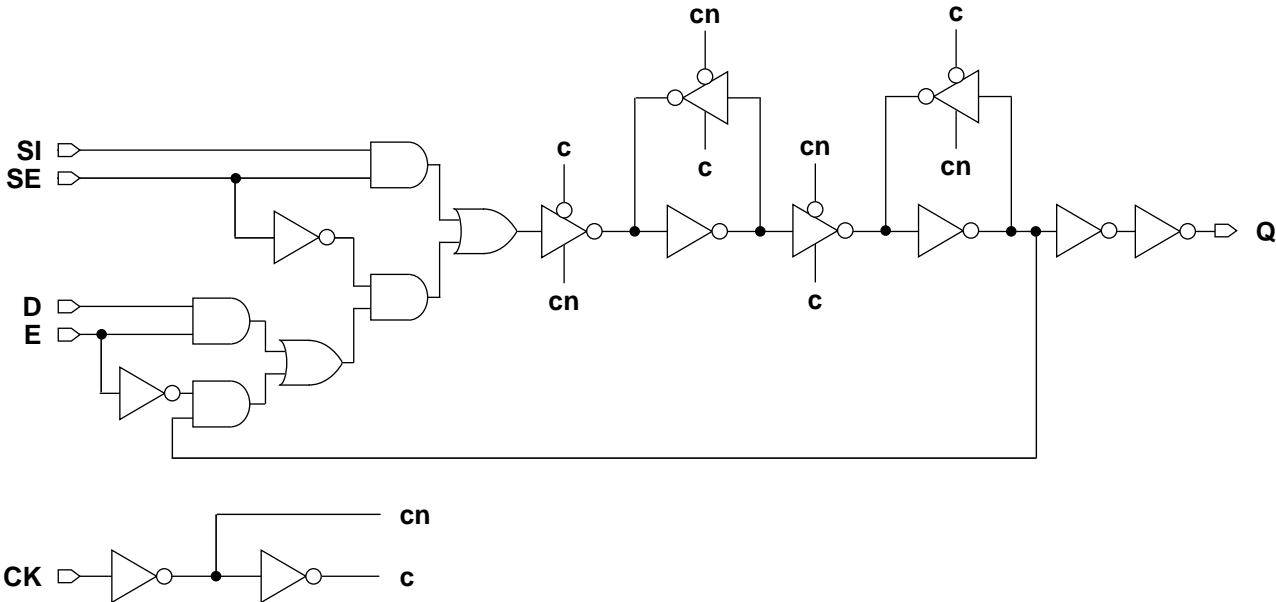
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
SI	0.0088	0.0120	0.0178	0.0274
SE	0.0143	0.0175	0.0228	0.0360
D	0.0091	0.0129	0.0183	0.0317
CK	0.0149	0.0202	0.0275	0.0412
E	0.0147	0.0180	0.0225	0.0333
Q	0.0054	0.0073	0.0097	0.0163

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
SI	0.0012	0.0012	0.0011	0.0014
SE	0.0034	0.0035	0.0036	0.0047
D	0.0017	0.0026	0.0039	0.0075
CK	0.0025	0.0026	0.0034	0.0045
E	0.0026	0.0026	0.0026	0.0027

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK → Q ↑	0.0745	0.0738	0.0683	0.0605	3.5885	2.3134	1.1903	0.6081
CK → Q ↓	0.0877	0.0835	0.0709	0.0633	3.3049	1.4191	0.6787	0.3316

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
SI	setup	↑	→	CK	0.0938	0.0938	0.1055	0.1172
	setup	↓	→	CK	0.1406	0.1641	0.1992	0.2031
	hold	↑	→	CK	-0.0586	-0.0586	-0.0664	-0.0742
	hold	↓	→	CK	-0.1094	-0.1250	-0.1562	-0.1523
SE	setup	↑	→	CK	0.1953	0.2227	0.2734	0.2930
	setup	↓	→	CK	0.1680	0.1523	0.1445	0.1602
	hold	↑	→	CK	-0.0742	-0.0781	-0.1016	-0.1211
	hold	↓	→	CK	-0.1172	-0.1055	-0.1016	-0.1055
D	setup	↑	→	CK	0.0859	0.0703	0.0547	0.0625
	setup	↓	→	CK	0.0742	0.0586	0.0508	0.0586
	hold	↑	→	CK	-0.0508	-0.0352	-0.0234	-0.0273
	hold	↓	→	CK	-0.0430	-0.0273	-0.0195	-0.0273
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
E	setup	↑	→	CK	0.1289	0.1133	0.1055	0.1211
	setup	↓	→	CK	0.1719	0.1914	0.1914	0.1875
	hold	↑	→	CK	-0.0977	-0.0859	-0.0781	-0.0859
	hold	↓	→	CK	-0.1016	-0.1055	-0.1016	-0.1016

Cell Description

The SEDFFTR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), synchronous active-high enable (E) and synchronous active low reset (RN). Scan enable (SE) dominates reset (RN) and enable (E).

Logic Symbol
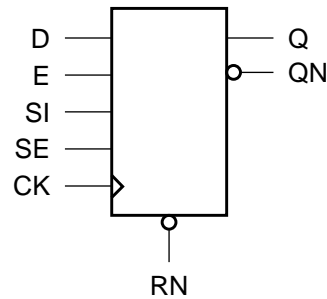
Function Table

RN	D	E	SI	SE	CK	Q[n+1]	QN[n+1]
x	x	x	0	1	⌐	0	1
x	x	x	1	1	⌐	1	0
1	x	0	x	0	⌐	Q[n]	QN[n]
0	x	x	x	0	⌐	0	1
1	1	1	x	0	⌐	1	0
1	0	1	x	0	⌐	0	1
x	x	x	x	x	⌐	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
SEDFFTRXLAD	2.52	12.60
SEDFFTRX1AD	2.52	12.60
SEDFFTRX2AD	2.52	12.60
SEDFFTRX4AD	2.52	14.56

Functional Schematic
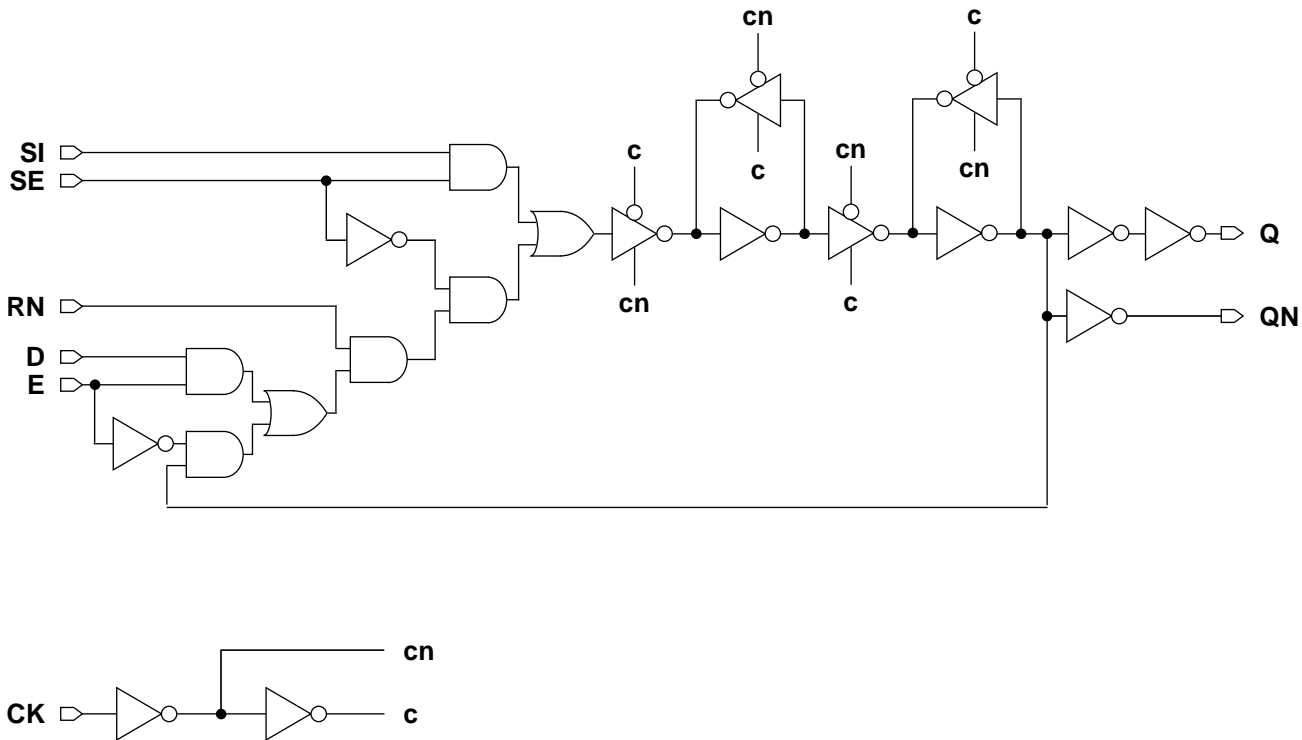
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
SI	0.0090	0.0094	0.0104	0.0138
SE	0.0119	0.0123	0.0133	0.0167
D	0.0111	0.0116	0.0125	0.0160
CK	0.0125	0.0130	0.0139	0.0184
E	0.0133	0.0137	0.0146	0.0178
RN	0.0087	0.0091	0.0099	0.0131
Q	0.0063	0.0073	0.0097	0.0164

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
SI	0.0011	0.0011	0.0011	0.0011
SE	0.0023	0.0023	0.0023	0.0023
D	0.0012	0.0012	0.0012	0.0012
CK	0.0015	0.0015	0.0016	0.0019
E	0.0013	0.0013	0.0013	0.0013
RN	0.0013	0.0013	0.0013	0.0013

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→ Q	↑	0.1464	0.1397	0.1324	0.1299	5.6967	3.6538	2.3596	1.2090
CK	→ Q	↓	0.1393	0.1387	0.1293	0.1332	4.2516	3.1130	1.3271	0.6613
CK	→ QN	↑	0.0959	0.0925	0.0899	0.0901	5.7394	3.6551	2.3508	1.2218
CK	→ QN	↓	0.1079	0.1065	0.0958	0.0900	4.8564	3.3465	1.4201	0.6974

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	X1	X2	X4
SI	setup	↑	→	CK	0.1055	0.1055	0.1172	0.1328
	setup	↓	→	CK	0.1367	0.1406	0.1445	0.1484
	hold	↑	→	CK	-0.0703	-0.0703	-0.0742	-0.0781
	hold	↓	→	CK	-0.1250	-0.1250	-0.1250	-0.1250
SE	setup	↑	→	CK	0.1523	0.1562	0.1602	0.1719
	setup	↓	→	CK	0.1719	0.1719	0.1797	0.1875
	hold	↑	→	CK	-0.1094	-0.1094	-0.1094	-0.1172
	hold	↓	→	CK	-0.1211	-0.1211	-0.1250	-0.1289
D	setup	↑	→	CK	0.1445	0.1445	0.1562	0.1719
	setup	↓	→	CK	0.1680	0.1680	0.1758	0.1797
	hold	↑	→	CK	-0.1055	-0.1055	-0.1094	-0.1133
	hold	↓	→	CK	-0.1523	-0.1523	-0.1523	-0.1562
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
E	setup	↑	→	CK	0.1875	0.1875	0.1953	0.2109
	setup	↓	→	CK	0.1758	0.1758	0.1719	0.1719
	hold	↑	→	CK	-0.1484	-0.1484	-0.1523	-0.1562
	hold	↓	→	CK	-0.0820	-0.0859	-0.1016	-0.1289
RN	setup	↑	→	CK	0.0898	0.0938	0.1016	0.1211
	setup	↓	→	CK	0.1094	0.1133	0.1172	0.1211
	hold	↑	→	CK	-0.0547	-0.0547	-0.0586	-0.0625
	hold	↓	→	CK	-0.0977	-0.0977	-0.0977	-0.0977

Cell Description

The SMDFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with a 2to1data select control (S0) for the data inputs (D1,D0), scan input (SI), and activehigh scan enable (SE). The cell has a single output (Q) and fast clocktoout path.

Logic Symbol

D1 ——
D0 —— ———— Q
S0 ——
SI ——
SE ——
CK ——▷
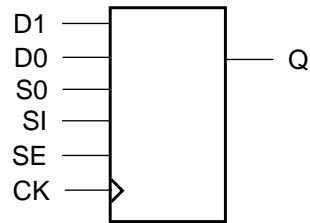
Function Table

SE	SI	S0	D1	D0	CK	Q[n+1]
0	x	0	x	0	⌐⌐	0
0	x	0	x	1	⌐⌐	1
0	x	1	0	x	⌐⌐	0
0	x	1	1	x	⌐⌐	1
1	0	x	x	x	⌐⌐	0
1	1	x	x	x	⌐⌐	1
x	x	x	x	x	⌐⌐	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
SMDFFHQX1AD	2.52	11.20
SMDFFHQX2AD	2.52	12.04
SMDFFHQX4AD	2.52	14.00
SMDFFHQX8AD	2.52	20.44

Functional Schematic
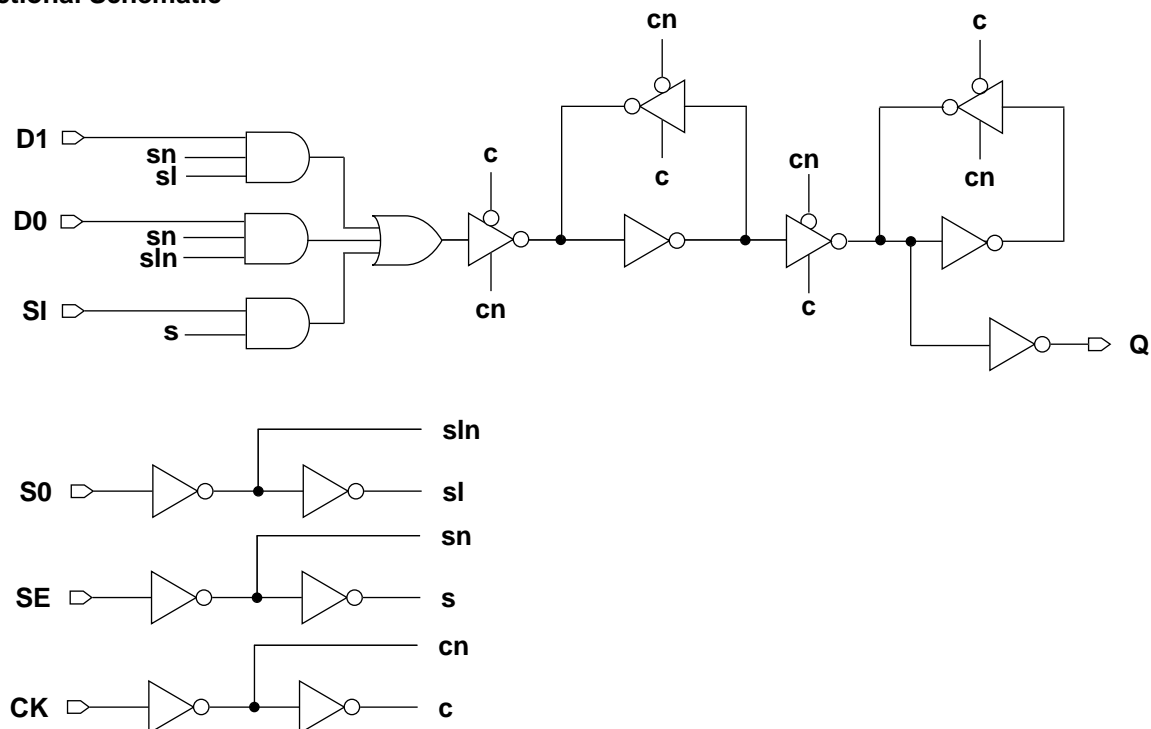
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
SI	0.0085	0.0111	0.0173	0.0292
SE	0.0136	0.0162	0.0232	0.0402
D0	0.0087	0.0114	0.0178	0.0308
D1	0.0086	0.0112	0.0176	0.0310
S0	0.0139	0.0165	0.0233	0.0358
CK	0.0139	0.0178	0.0271	0.0445
Q	0.0040	0.0056	0.0084	0.0144

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
SI	0.0011	0.0011	0.0014	0.0022
SE	0.0033	0.0034	0.0033	0.0036
D0	0.0013	0.0016	0.0025	0.0046
D1	0.0014	0.0016	0.0025	0.0045
S0	0.0026	0.0026	0.0027	0.0029
CK	0.0023	0.0023	0.0032	0.0053

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→ Q	↑	0.0784	0.0752	0.0685	0.0621	3.6191	2.3157	1.1803	0.6062
CK	→ Q	↓	0.0881	0.0818	0.0730	0.0647	3.2312	1.3796	0.6649	0.3267

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	X2	X4	X8
SI	setup	↑	→	CK	0.0977	0.0938	0.0898	0.0820
	setup	↓	→	CK	0.1406	0.1523	0.1406	0.1445
	hold	↑	→	CK	-0.0586	-0.0586	-0.0547	-0.0430
	hold	↓	→	CK	-0.1055	-0.1172	-0.1055	-0.1055
SE	setup	↑	→	CK	0.1523	0.1641	0.1523	0.1680
	setup	↓	→	CK	0.1719	0.1484	0.1445	0.1562
	hold	↑	→	CK	-0.0586	-0.0625	-0.0664	-0.0586
	hold	↓	→	CK	-0.1055	-0.0898	-0.0781	-0.0820
D0	setup	↑	→	CK	0.0938	0.0742	0.0586	0.0586
	setup	↓	→	CK	0.1055	0.0781	0.0625	0.0781
	hold	↑	→	CK	-0.0547	-0.0391	-0.0273	-0.0195
	hold	↓	→	CK	-0.0742	-0.0508	-0.0352	-0.0430
D1	setup	↑	→	CK	0.0977	0.0742	0.0625	0.0586
	setup	↓	→	CK	0.1094	0.0820	0.0664	0.0781
	hold	↑	→	CK	-0.0586	-0.0391	-0.0273	-0.0234
	hold	↓	→	CK	-0.0781	-0.0508	-0.0352	-0.0430
S0	setup	↑	→	CK	0.1328	0.1133	0.1094	0.1094
	setup	↓	→	CK	0.1484	0.1289	0.1211	0.1406
	hold	↑	→	CK	-0.0938	-0.0742	-0.0664	-0.0703
	hold	↓	→	CK	-0.0977	-0.0820	-0.0742	-0.0781
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The TBUF cell provides the logical buffer of a single input (A) with an active-high output enable (OE). When the enable is high, the output (Y) is represented by the logic equation:

$Y = A$

Logic Symbol

A — ▷ — Y

OE
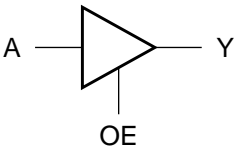
Function Table

OE	A	Y
0	x	Z
1	0	0
1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
TBUFXLAD	2.52	2.52
TBUFX1AD	2.52	2.52
TBUFX2AD	2.52	2.80
TBUFX3AD	2.52	3.08
TBUFX4AD	2.52	3.08
TBUFX6AD	2.52	3.92
TBUFX8AD	2.52	4.48
TBUFX12AD	2.52	5.88
TBUFX16AD	2.52	6.72
TBUFX20AD	2.52	8.40

Functional Schematic

A ▷———————▷ Y

OE ▷
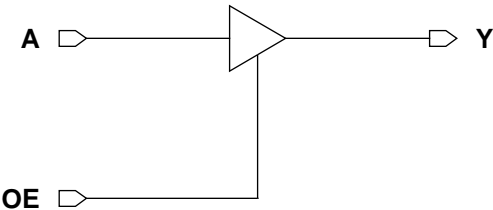
AC Power

Pin	Power (uW/MHz)							
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**
A	0.0043	0.0047	0.0060	0.0076	0.0087	0.0126	0.0161	0.0237
OE	0.0029	0.0033	0.0046	0.0056	0.0063	0.0093	0.0116	0.0176

AC Power (Cont'd.)

Pin	Power (uW/MHz)	
	X16	**X20**
A	0.0305	0.0390
OE	0.0224	0.0296

Pin Capacitance

Pin	Capacitance (pF)							
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**
A	0.0013	0.0013	0.0015	0.0017	0.0021	0.0036	0.0045	0.0066
OE	0.0022	0.0022	0.0025	0.0027	0.0027	0.0027	0.0034	0.0042
Y	0.0010	0.0012	0.0016	0.0023	0.0027	0.0043	0.0054	0.0085

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)	
	X16	**X20**
A	0.0084	0.0101
OE	0.0050	0.0062
Y	0.0111	0.0143

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)							
			XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**
A	→ Y	↑	0.0518	0.0536	0.0514	0.0473	0.0492	0.0462	0.0446	0.0432
A	→ Y	↓	0.0907	0.0945	0.0745	0.0695	0.0649	0.0609	0.0586	0.0596
OE	→ Y	↑	0.0344	0.0362	0.0332	0.0345	0.0363	0.0371	0.0364	0.0353
OE	→ Y	↓	0.0608	0.0629	0.0558	0.0517	0.0514	0.0517	0.0470	0.0496

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description				Intrinsic Delay (ns)	
				X16	**X20**
A	→	Y	↑	0.0446	0.0456
A	→	Y	↓	0.0591	0.0606
OE	→	Y	↑	0.0368	0.0370
OE	→	Y	↓	0.0478	0.0509

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)							
				XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**
A	→	Y	↑	5.7125	3.7473	2.5625	1.6035	1.3382	0.8893	0.6797	0.4550
A	→	Y	↓	5.1704	3.4547	1.5931	0.9743	0.7738	0.5056	0.3749	0.2511
OE	→	Y	↑	5.7028	3.7386	2.5594	1.6027	1.3379	0.8890	0.6800	0.4553
OE	→	Y	↓	5.1420	3.4312	1.5834	0.9673	0.7701	0.5044	0.3738	0.2504

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)	
				X16	**X20**
A	→	Y	↑	0.3489	0.2780
A	→	Y	↓	0.1873	0.1425
OE	→	Y	↑	0.3492	0.2780
OE	→	Y	↓	0.1867	0.1421

TSMC CLN90G

Cell Description

The TIEHI cell drives the output (Y) to a logic high. The output is driven through diffusion and not tied directly to the power rail to provide some ESD protection. The output (Y) is represented by the logic equation:

$Y = 1$

Logic Symbol
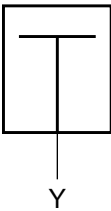
Function Table

Y
1

Cell Size

Drive Strength	Height (um)	Width (um)
TIEHIAD	2.52	0.84

Functional Schematic

Y

Cell Description

The TIELO cell drives the output (Y) to a logic low. The output is driven through diffusion and not tied directly to the power rail to provide some ESD protection. The output (Y) is represented by the logic equation:

$Y = 0$

Logic Symbol

Y

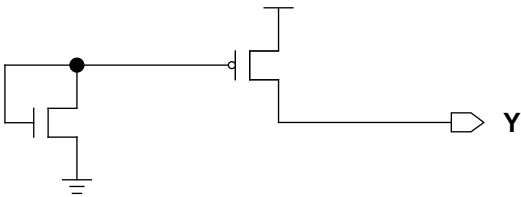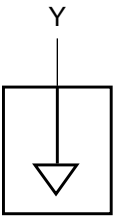**Function Table**

Y
0

Cell Size

Drive Strength	Height (um)	Width (um)
TIELOAD	2.52	0.84

Functional Schematic

Y
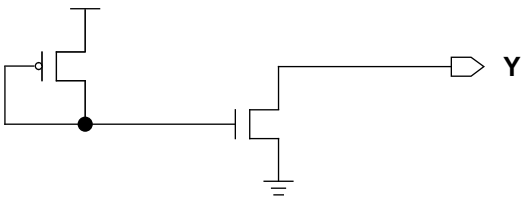
Cell Description

The TLAT cell is an active-high D-type transparent latch. When the enable (G) is high, data is transferred to the outputs (Q,QN).

Logic Symbol
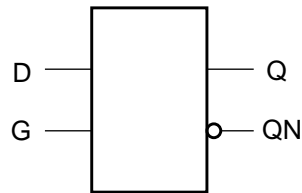
Function Table

G	D	Q[n+1]	QN[n+1]
1	0	0	1
1	1	1	0
0	x	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
TLATXLAD	2.52	3.64
TLATX1AD	2.52	3.64
TLATX2AD	2.52	3.92
TLATX4AD	2.52	5.60

Functional Schematic
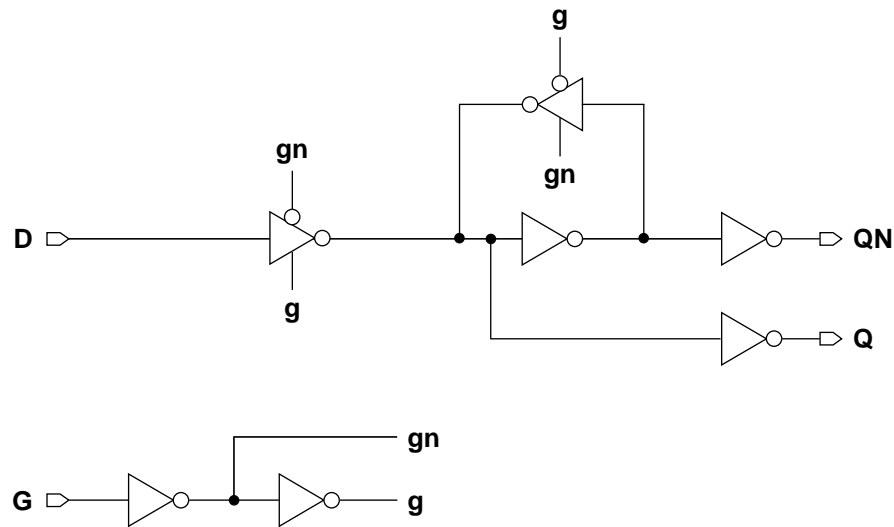
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0011	0.0013	0.0016	0.0032
G	0.0043	0.0044	0.0046	0.0063
Q	0.0052	0.0061	0.0085	0.0150

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0016	0.0019	0.0024	0.0047
G	0.0012	0.0012	0.0015	0.0021

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
D	→	Q	↑	0.0439	0.0413	0.0387	0.0393	5.6962	3.7611	2.3499	1.2277
D	→	Q	↓	0.0734	0.0687	0.0643	0.0627	4.9663	3.2559	1.4268	0.7052
G	→	Q	↑	0.0980	0.0966	0.0893	0.0866	5.6926	3.7604	2.3490	1.2272
G	→	Q	↓	0.0855	0.0818	0.0706	0.0659	4.9664	3.2598	1.4267	0.7044
D	→	QN	↑	0.1049	0.1010	0.1022	0.0989	5.6507	3.6300	2.3455	1.2080
D	→	QN	↓	0.0827	0.0862	0.0847	0.0811	4.5111	3.1000	1.3921	0.6714
G	→	QN	↑	0.1173	0.1145	0.1086	0.1021	5.6527	3.6314	2.3461	1.2082
G	→	QN	↓	0.1372	0.1419	0.1357	0.1287	4.5130	3.1012	1.3923	0.6715

Timing Constraints at 25°C, 1.0V, Typical Process

| Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	G	-0.0117	-0.0117	-0.0078	-0.0039
	setup	↓	→	G	0.0508	0.0430	0.0469	0.0469
	hold	↑	→	G	0.0195	0.0195	0.0156	0.0117
	hold	↓	→	G	-0.0430	-0.0391	-0.0430	-0.0391
G	minpwh				0.8332	0.8332	0.8332	0.8332

Cell Description

The TLATN cell is an active-low D-type transparent latch. When the enable (GN) is low, data is transferred to the outputs (Q,QN).

Logic Symbol
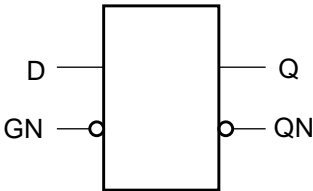
Function Table

GN	D	Q[n+1]	QN[n+1]
0	0	0	1
0	1	1	0
1	x	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
TLATNXLAD	2.52	3.92
TLATNX1AD	2.52	3.92
TLATNX2AD	2.52	3.92
TLATNX4AD	2.52	5.60

Functional Schematic
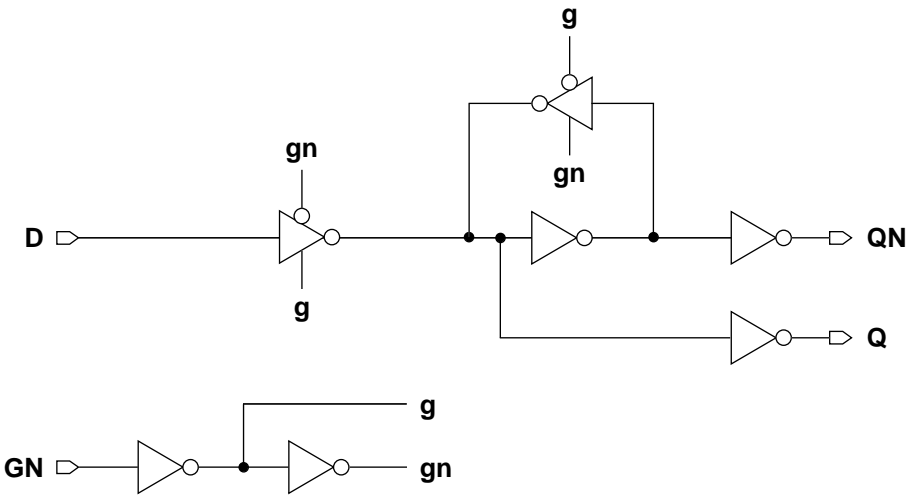
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0010	0.0012	0.0016	0.0033
GN	0.0045	0.0048	0.0052	0.0087
Q	0.0054	0.0064	0.0089	0.0156

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0016	0.0019	0.0024	0.0049
GN	0.0016	0.0016	0.0015	0.0022

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
D	→	Q	↑	0.0421	0.0404	0.0409	0.0371	5.7144	3.6507	2.3557	1.2239
D	→	Q	↓	0.0709	0.0676	0.0626	0.0627	4.9032	3.2151	1.4229	0.7026
GN	→	Q	↑	0.0686	0.0671	0.0691	0.0602	5.7338	3.6604	2.3596	1.2258
GN	→	Q	↓	0.1130	0.1111	0.1078	0.0967	4.8997	3.2140	1.4224	0.7023
D	→	QN	↑	0.0998	0.0966	0.1007	0.0990	5.6469	3.6289	2.3457	1.2075
D	→	QN	↓	0.0812	0.0852	0.0878	0.0791	4.5146	3.1027	1.3912	0.6718
GN	→	QN	↑	0.1420	0.1402	0.1459	0.1330	5.6489	3.6295	2.3458	1.2075
GN	→	QN	↓	0.1092	0.1136	0.1176	0.1031	4.5170	3.1038	1.3913	0.6720

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	GN	0.0273	0.0273	0.0273	0.0234
	setup	↓	→	GN	0.0352	0.0273	0.0234	0.0273
	hold	↑	→	GN	-0.0234	-0.0195	-0.0195	-0.0195
	hold	↓	→	GN	-0.0273	-0.0195	-0.0156	-0.0195
GN	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The TLATNCA cell is a positive-edge triggered clock-gating latch. The positive-edge clock (CK) is qualified by the latched enable signal (E) to create the gated positive-edge clock (ECK).

Logic Symbol
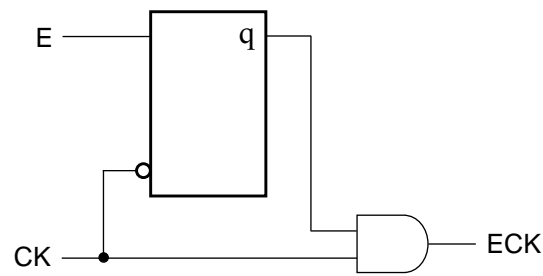
Function Table

CK	E	q[n+1]	ECK[n+1]
1	x	q[n]	q[n]
0	0	0	0
0	1	1	0

- *Note: q is an internal node, and is not accessible.*

Cell Size

Drive Strength	Height (um)	Width (um)
TLATNCAX2AD	2.52	3.64
TLATNCAX3AD	2.52	4.20
TLATNCAX4AD	2.52	5.60
TLATNCAX6AD	2.52	6.44
TLATNCAX8AD	2.52	7.56
TLATNCAX12AD	2.52	10.08
TLATNCAX16AD	2.52	12.60
TLATNCAX20AD	2.52	15.68

Functional Schematic
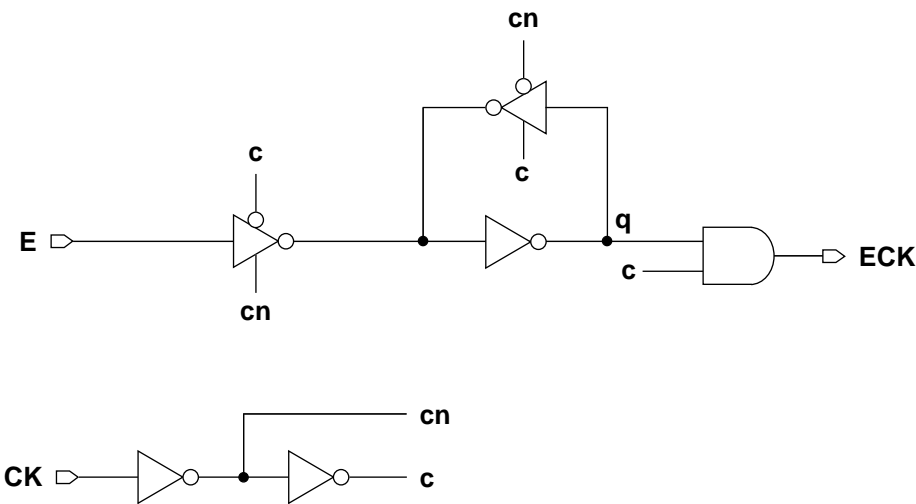
AC Power

Pin	Power (uW/MHz)							
	X2	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**	**X20**
E	0.0062	0.0075	0.0099	0.0124	0.0158	0.0219	0.0270	0.0341
CK	0.0064	0.0073	0.0092	0.0119	0.0151	0.0235	0.0288	0.0367
ECK	0.0064	0.0081	0.0099	0.0134	0.0166	0.0238	0.0307	0.0377

Pin Capacitance

Pin	Capacitance (pF)							
	X2	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**	**X20**
E	0.0022	0.0024	0.0042	0.0052	0.0070	0.0098	0.0119	0.0158
CK	0.0021	0.0025	0.0027	0.0041	0.0051	0.0077	0.0100	0.0125

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)							
			X2	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**	**X20**
CK	→ ECK	↑	0.0397	0.0424	0.0414	0.0417	0.0413	0.0461	0.0465	0.0482
CK	→ ECK	↓	0.0546	0.0549	0.0551	0.0506	0.0507	0.0523	0.0506	0.0517

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)							
			X2	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**	**X20**
CK	→ ECK	↑	4.6226	3.1691	2.3907	1.6287	1.2373	0.8530	0.6522	0.5317
CK	→ ECK	↓	3.5303	2.3228	1.7689	1.1467	0.8555	0.5710	0.4277	0.3366

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)							
					X2	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**	**X20**
E	setup	↑	→	CK	0.0312	0.0312	0.0273	0.0273	0.0234	0.0234	0.0273	0.0273
	setup	↓	→	CK	0.0117	0.0156	0.0039	0.0078	0.0078	0.0039	0.0078	0.0078
	hold	↑	→	CK	-0.0156	-0.0195	-0.0156	-0.0156	-0.0156	-0.0156	-0.0195	-0.0156
	hold	↓	→	CK	0.0234	0.0234	0.0273	0.0234	0.0234	0.0234	0.0195	0.0195
CK	minpwl				0.8332	0.8332	0.8332	0.8332	0.8332	0.8332	0.8332	0.8332

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Cell Description

The TLATNSR cell is an active-low D-type transparent latch with asynchronous active-low set (SN) and reset (RN), and set dominating reset. When the enable (GN) is low, data is transferred to the outputs (Q,QN).

Logic Symbol
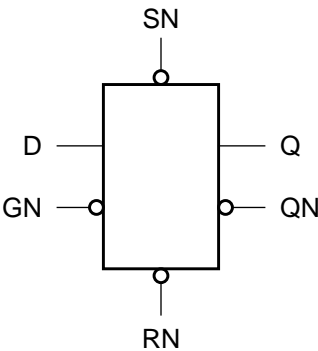
Function Table

RN	SN	GN	D	Q[n+1]	QN[n+1]
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	x	Q[n]	QN[n]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
TLATNSRXLAD	2.52	5.60
TLATNSRX1AD	2.52	5.88
TLATNSRX2AD	2.52	6.16
TLATNSRX4AD	2.52	8.96

Functional Schematic
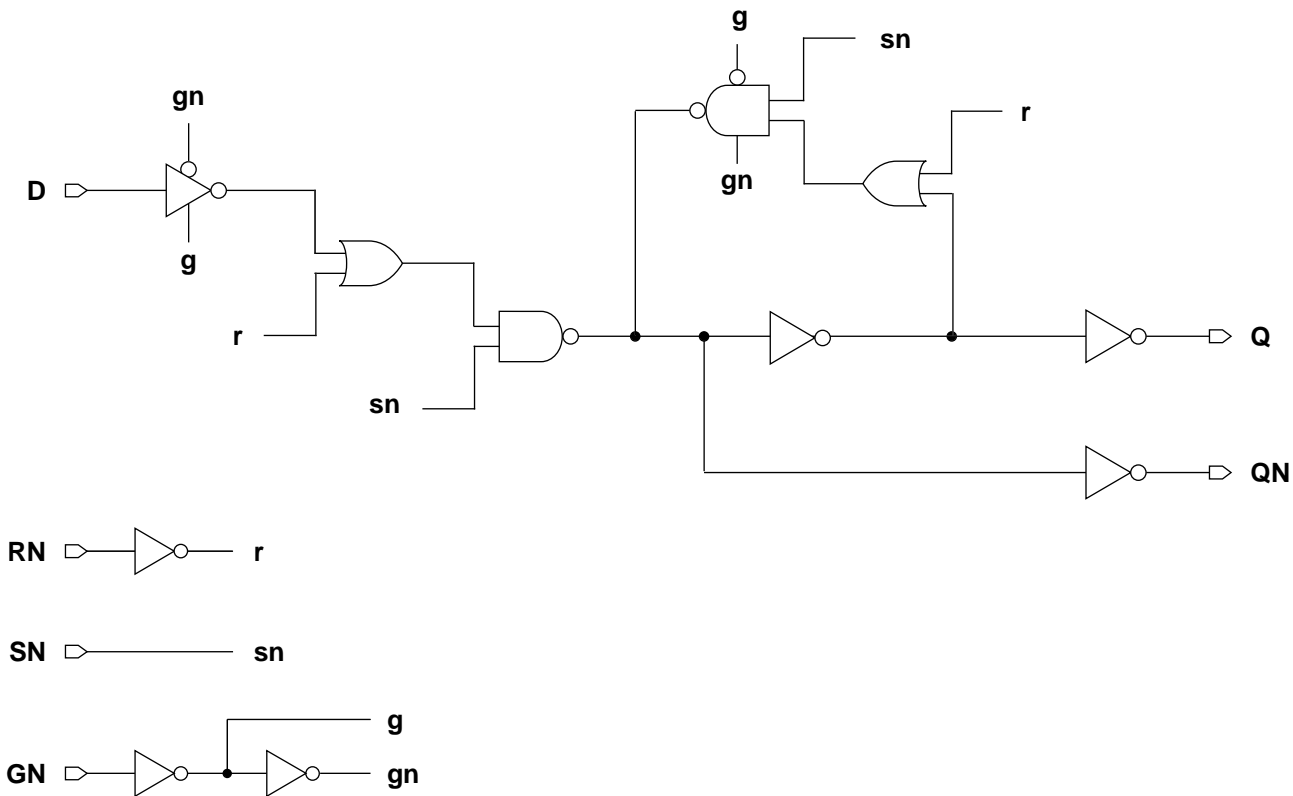
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0012	0.0015	0.0019	0.0037
GN	0.0056	0.0062	0.0070	0.0110
SN	0.0031	0.0038	0.0045	0.0075
RN	0.0012	0.0015	0.0018	0.0034
Q	0.0089	0.0108	0.0138	0.0232

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0015	0.0021	0.0025	0.0049
GN	0.0015	0.0014	0.0014	0.0019
SN	0.0012	0.0015	0.0018	0.0028
RN	0.0019	0.0023	0.0027	0.0049

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
D	→	Q	↑	0.0858	0.0765	0.0761	0.0699	6.0942	3.8301	2.4410	1.2497
D	→	Q	↓	0.1502	0.1363	0.1247	0.1225	6.3249	3.7021	1.6697	0.8287
GN	→	Q	↑	0.0987	0.0925	0.0927	0.0918	6.1136	3.8376	2.4479	1.2535
GN	→	Q	↓	0.1948	0.1711	0.1651	0.1579	6.3226	3.7018	1.6698	0.8285
SN	→	Q	↑	0.1087	0.0962	0.0930	0.0853	5.8556	3.7438	2.4065	1.2346
SN	→	Q	↓	0.1720	0.1533	0.1398	0.1348	6.2952	3.6878	1.6600	0.8226
RN	→	Q	↑	0.0834	0.0741	0.0738	0.0668	6.0940	3.8301	2.4410	1.2497
RN	→	Q	↓	0.1364	0.1189	0.1072	0.0949	6.7853	3.8905	1.7696	0.8537
D	→	QN	↑	0.1945	0.1702	0.1728	0.1695	5.7502	3.6658	2.3705	1.2164
D	→	QN	↓	0.1211	0.1042	0.1263	0.1134	4.6396	2.9379	1.3554	0.6592
GN	→	QN	↑	0.2396	0.2053	0.2136	0.2051	5.7550	3.6673	2.3711	1.2166
GN	→	QN	↓	0.1348	0.1207	0.1440	0.1361	4.6438	2.9392	1.3572	0.6598
SN	→	QN	↑	0.2160	0.1868	0.1874	0.1811	5.7507	3.6658	2.3708	1.2165
SN	→	QN	↓	0.1428	0.1234	0.1418	0.1277	4.6114	2.9298	1.3506	0.6574
RN	→	QN	↑	0.1833	0.1537	0.1574	0.1416	5.7875	3.6772	2.3745	1.2177
RN	→	QN	↓	0.1189	0.1019	0.1241	0.1104	4.6401	2.9380	1.3557	0.6592

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	GN	0.0742	0.0625	0.0664	0.0547
	setup	↓	→	GN	0.1133	0.0859	0.0781	0.0781
	hold	↑	→	GN	-0.0664	-0.0547	-0.0625	-0.0508
	hold	↓	→	GN	-0.0938	-0.0703	-0.0625	-0.0664
GN	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.1328	0.1016	0.0898	0.0898
	removal				-0.1289	-0.0977	-0.0859	-0.0859
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.0703	0.0586	0.0664	0.0508
	removal				-0.0664	-0.0547	-0.0625	-0.0469

Cell Description

The TLATNTSCA cell is a positive-edge triggered clock-gating latch. The positive-edge clock (CK) is qualified by the latched enable signals (SE) and (E) to create the gated positive-edge clock (ECK).

Logic Symbol
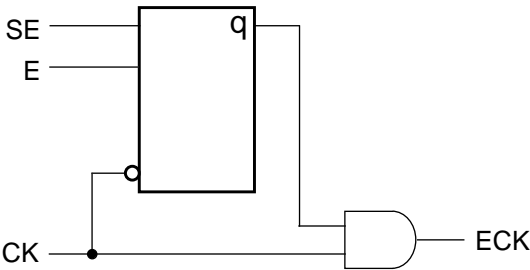
Function Table

CK	SE	E	q[n+1]	ECK[n+1]
1	x	x	q[n]	q[n]
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0

- Note: q is an internal node and is not accessible.

Cell Size

Drive Strength	Height (um)	Width (um)
TLATNTSCAX2AD	2.52	5.04
TLATNTSCAX3AD	2.52	5.60
TLATNTSCAX4AD	2.52	6.44
TLATNTSCAX6AD	2.52	8.40
TLATNTSCAX8AD	2.52	9.52
TLATNTSCAX12AD	2.52	11.48
TLATNTSCAX16AD	2.52	13.16
TLATNTSCAX20AD	2.52	16.24

Functional Schematic
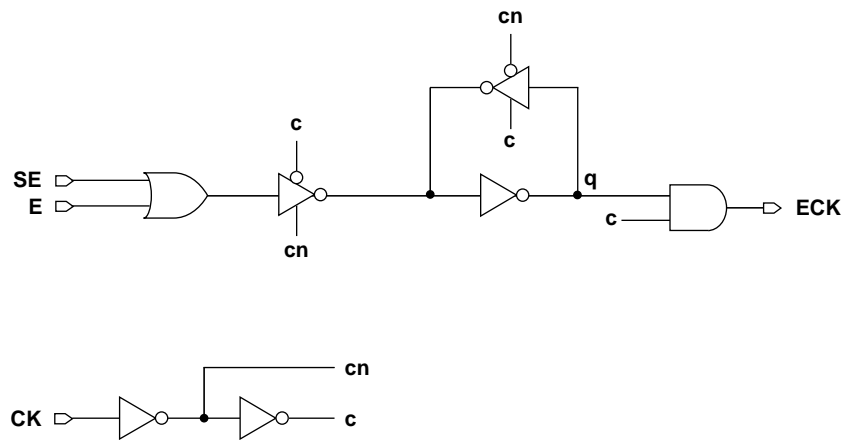
AC Power

Pin	Power (uW/MHz)							
	X2	X3	X4	X6	X8	X12	X16	X20
E	0.0099	0.0106	0.0134	0.0172	0.0210	0.0275	0.0316	0.0377
SE	0.0102	0.0109	0.0137	0.0175	0.0214	0.0281	0.0325	0.0386
CK	0.0069	0.0076	0.0095	0.0132	0.0164	0.0228	0.0274	0.0331
ECK	0.0066	0.0079	0.0097	0.0141	0.0172	0.0215	0.0277	0.0318

Pin Capacitance

Pin	Capacitance (pF)							
	X2	X3	X4	X6	X8	X12	X16	X20
E	0.0013	0.0014	0.0016	0.0014	0.0016	0.0020	0.0024	0.0028
SE	0.0014	0.0013	0.0014	0.0012	0.0015	0.0018	0.0025	0.0027
CK	0.0022	0.0025	0.0028	0.0042	0.0052	0.0077	0.0100	0.0124

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)							
			X2	X3	X4	X6	X8	X12	X16	X20
CK	→	ECK ↑	0.0423	0.0430	0.0427	0.0433	0.0434	0.0455	0.0464	0.0481
CK	→	ECK ↓	0.0574	0.0553	0.0558	0.0523	0.0515	0.0473	0.0472	0.0457

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)							
			X2	X3	X4	X6	X8	X12	X16	X20
CK	→	ECK ↑	4.6386	3.1922	2.4002	1.6360	1.2442	1.0074	0.7289	0.6429
CK	→	ECK ↓	3.6460	2.3067	1.7541	1.0765	0.8592	0.5648	0.4208	0.3364

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)							
					X2	X3	X4	X6	X8	X12	X16	X20
E	setup	↑	→	CK	0.0898	0.0820	0.0742	0.0820	0.0781	0.0781	0.0703	0.0703
	setup	↓	→	CK	0.0859	0.0820	0.0820	0.0859	0.0781	0.0703	0.0703	0.0781
	hold	↑	→	CK	-0.0742	-0.0664	-0.0625	-0.0703	-0.0664	-0.0664	-0.0586	-0.0586
	hold	↓	→	CK	-0.0469	-0.0430	-0.0508	-0.0508	-0.0469	-0.0391	-0.0391	-0.0508
SE	setup	↑	→	CK	0.0938	0.0820	0.0781	0.0820	0.0781	0.0781	0.0742	0.0703
	setup	↓	→	CK	0.0938	0.0859	0.0859	0.0898	0.0820	0.0742	0.0742	0.0820
	hold	↑	→	CK	-0.0742	-0.0664	-0.0664	-0.0703	-0.0703	-0.0664	-0.0625	-0.0625
	hold	↓	→	CK	-0.0508	-0.0469	-0.0547	-0.0547	-0.0508	-0.0430	-0.0469	-0.0547
CK	minpwl				0.8332	0.8332	0.8332	0.8332	0.8332	0.8332	0.8332	0.8332

Cell Description

The TLATSR cell is an active-high D-type transparent latch with asynchronous active-low set (SN) and reset (RN), and set dominating reset. When the enable (G) is high, data is transferred to the outputs (Q,QN).
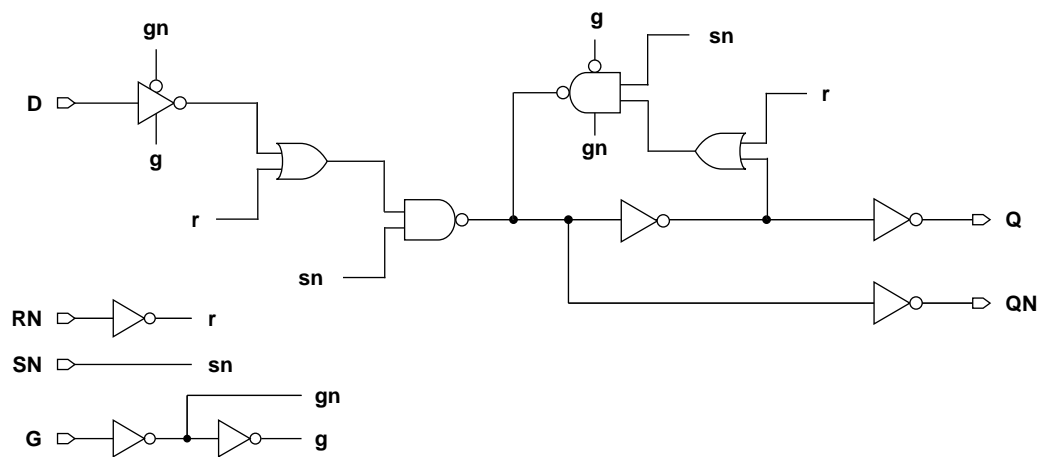
Logic Symbol
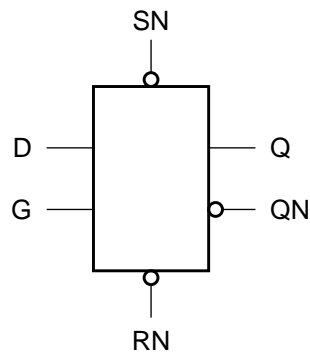
Function Table

RN	SN	G	D	Q[n+1]	QN[n+1]
1	1	1	0	0	1
1	1	1	1	1	0
1	1	0	x	Q[n]	QN[n]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
TLATSRXLAD	2.52	5.60
TLATSRX1AD	2.52	5.60
TLATSRX2AD	2.52	6.16
TLATSRX4AD	2.52	8.96

Functional Schematic

AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0011	0.0013	0.0017	0.0037
G	0.0049	0.0051	0.0054	0.0092
SN	0.0031	0.0033	0.0043	0.0072
RN	0.0011	0.0012	0.0018	0.0033
Q	0.0084	0.0096	0.0139	0.0222

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0014	0.0017	0.0023	0.0049
G	0.0014	0.0014	0.0015	0.0018
SN	0.0012	0.0013	0.0018	0.0028
RN	0.0018	0.0020	0.0027	0.0047

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
D	→	Q	↑	0.0895	0.0818	0.0756	0.0704	6.1494	3.9414	2.4309	1.2508
D	→	Q	↓	0.1573	0.1453	0.1433	0.1217	6.4099	3.8411	1.7558	0.8246
G	→	Q	↑	0.1284	0.1227	0.1239	0.1179	6.1443	3.9390	2.4293	1.2498
G	→	Q	↓	0.1546	0.1420	0.1362	0.1108	6.4137	3.8431	1.7563	0.8239
SN	→	Q	↑	0.1087	0.1028	0.0900	0.0849	5.8411	3.8406	2.3962	1.2372
SN	→	Q	↓	0.1792	0.1642	0.1582	0.1340	6.3805	3.8287	1.7449	0.8192
RN	→	Q	↑	0.0871	0.0793	0.0737	0.0666	6.1497	3.9416	2.4310	1.2509
RN	→	Q	↓	0.1445	0.1382	0.1051	0.1046	6.8656	4.1488	1.7218	0.8955
D	→	QN	↑	0.2008	0.1882	0.1953	0.1685	5.7501	3.7982	2.3680	1.2165
D	→	QN	↓	0.1384	0.1359	0.1249	0.1138	4.6303	3.0582	1.3551	0.6601
G	→	QN	↑	0.1988	0.1855	0.1886	0.1578	5.7550	3.8006	2.3686	1.2167
G	→	QN	↓	0.1780	0.1775	0.1737	0.1616	4.6346	3.0604	1.3562	0.6605
SN	→	QN	↑	0.2226	0.2069	0.2096	0.1803	5.7499	3.7983	2.3681	1.2167
SN	→	QN	↓	0.1546	0.1548	0.1378	0.1272	4.5906	3.0467	1.3499	0.6585
RN	→	QN	↑	0.1903	0.1837	0.1545	0.1548	5.7866	3.8175	2.3678	1.2186
RN	→	QN	↓	0.1363	0.1337	0.1231	0.1101	4.6314	3.0588	1.3554	0.6602

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	X1	X2	X4
D	setup	↑	→	G	0.0469	0.0352	0.0195	0.0117
	setup	↓	→	G	0.1367	0.1250	0.1289	0.1055
	hold	↑	→	G	-0.0352	-0.0234	-0.0078	0.0000
	hold	↓	→	G	-0.1289	-0.1172	-0.1211	-0.0977
G	minpwh				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.1602	0.1406	0.1406	0.1172
	removal				-0.1562	-0.1367	-0.1367	-0.1133
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.0430	0.0312	0.0156	0.0000
	removal				-0.0391	-0.0273	-0.0117	0.0039

Cell Description

The XNOR2 cell provides a logical EXCLUSIVE NOR of two inputs (A,B). The output (Y) is represented by the logic equation:

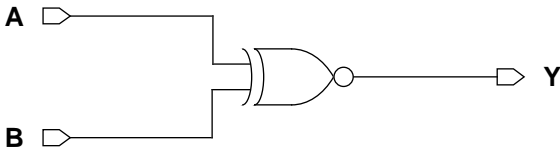$$Y = (A \bullet B) + (\overline{A} \bullet \overline{B})$$

Logic Symbol
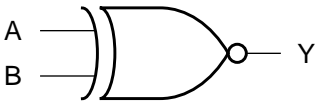
Function Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
XNOR2XLAD	2.52	2.24
XNOR2X1AD	2.52	2.24
XNOR2X2AD	2.52	3.08
XNOR2X4AD	2.52	4.48

Functional Schematic

AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A	0.0031	0.0037	0.0063	0.0119
B	0.0040	0.0050	0.0097	0.0170

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A	0.0018	0.0019	0.0025	0.0037
B	0.0014	0.0017	0.0027	0.0053

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A	→ Y	↑	0.0282	0.0255	0.0256	0.0258	8.1723	5.9989	3.0983	1.5889
A	→ Y	↓	0.0323	0.0332	0.0359	0.0346	5.9720	4.4915	1.8998	0.9508
B	→ Y	↑	0.0500	0.0439	0.0460	0.0404	8.2186	5.8832	3.2000	1.5778
B	→ Y	↓	0.0526	0.0465	0.0468	0.0417	6.3533	4.6734	2.0634	1.0020

Cell Description

The XNOR3 cell provides a logical EXCLUSIVE NOR of three inputs (A,B,C). The output (Y) is represented by the following equation:

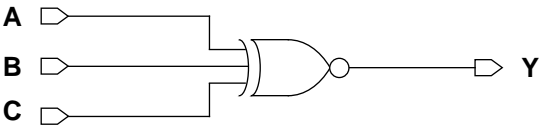$$Y = \overline{A \oplus B \oplus C}$$

Logic Symbol
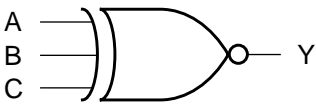
Function Table

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
XNOR3XLAD	2.52	4.76
XNOR3X1AD	2.52	5.32
XNOR3X2AD	2.52	5.32
XNOR3X4AD	2.52	6.16

Functional Schematic

AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A	0.0120	0.0150	0.0197	0.0290
B	0.0108	0.0128	0.0161	0.0241
C	0.0055	0.0064	0.0090	0.0123

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A	0.0020	0.0024	0.0027	0.0027
B	0.0020	0.0022	0.0024	0.0024
C	0.0018	0.0018	0.0022	0.0023

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A	→ Y	↑	0.1258	0.1135	0.1081	0.1198	5.7088	3.6164	2.3214	1.2282
A	→ Y	↓	0.1445	0.1325	0.1178	0.1341	5.0941	3.2759	1.5199	0.8501
B	→ Y	↑	0.1066	0.0995	0.0989	0.1156	5.7045	3.6823	2.3704	1.2275
B	→ Y	↓	0.1463	0.1349	0.1174	0.1224	5.0937	3.2762	1.4019	0.8489
C	→ Y	↑	0.0614	0.0644	0.0664	0.0741	5.7529	3.6569	2.3573	1.2218
C	→ Y	↓	0.0692	0.0618	0.0538	0.0603	5.0851	3.2721	1.4427	0.8003

Cell Description

The XOR2 cell provides a logical EXCLUSIVE OR of two inputs (A,B). The output (Y) is represented by the logic equation:

$$Y = (A \bullet \overline{B}) + (\overline{A} \bullet B)$$

Logic Symbol

Function Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0
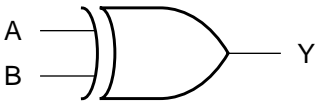
Cell Size

Drive Strength	Height (um)	Width (um)
XOR2XLAD	2.52	2.24
XOR2X1AD	2.52	2.24
XOR2X2AD	2.52	2.80
XOR2X3AD	2.52	4.48
XOR2X4AD	2.52	4.48
XOR2X8AD	2.52	7.84

Functional Schematic
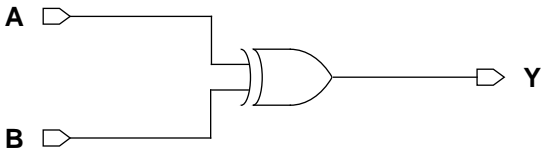
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X3**	**X4**	**X8**
A	0.0031	0.0037	0.0063	0.0094	0.0114	0.0217
B	0.0043	0.0053	0.0094	0.0147	0.0182	0.0360

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X3**	**X4**	**X8**
A	0.0018	0.0019	0.0024	0.0031	0.0037	0.0072
B	0.0014	0.0018	0.0027	0.0042	0.0053	0.0106

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			XL	**X1**	**X2**	**X3**	**X4**	**X8**
A	→ Y	↑	0.0293	0.0261	0.0255	0.0264	0.0245	0.0241
A	→ Y	↓	0.0328	0.0333	0.0368	0.0360	0.0328	0.0320
B	→ Y	↑	0.0492	0.0429	0.0384	0.0394	0.0368	0.0367
B	→ Y	↓	0.0542	0.0469	0.0441	0.0454	0.0420	0.0419

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)					
			XL	**X1**	**X2**	**X3**	**X4**	**X8**
A	→ Y	↑	8.1224	5.9384	3.2722	2.0743	1.5744	0.8011
A	→ Y	↓	6.0025	4.5293	2.0071	1.2570	0.9614	0.4763
B	→ Y	↑	8.1142	5.8867	3.2548	2.1161	1.5937	0.8123
B	→ Y	↓	6.2696	4.6809	2.1006	1.3182	1.0004	0.4946

TSMC CLN90G

Cell Description

The XOR3 cell provides a logical EXCLUSIVE OR of three inputs (A,B,C). The output (Y) is represented by the following equation:

$Y = A \oplus B \oplus C$

Logic Symbol
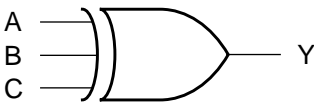
Function Table
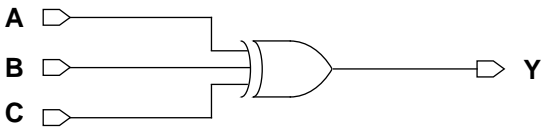
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
XOR3XLAD	2.52	4.76
XOR3X1AD	2.52	5.32
XOR3X2AD	2.52	5.32
XOR3X4AD	2.52	6.16

Functional Schematic

AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A	0.0128	0.0158	0.0210	0.0300
B	0.0108	0.0126	0.0159	0.0249
C	0.0056	0.0067	0.0090	0.0130

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A	0.0020	0.0024	0.0027	0.0027
B	0.0021	0.0022	0.0025	0.0024
C	0.0029	0.0030	0.0038	0.0040

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A	→	Y	↑	0.1276	0.1152	0.1100	0.1190	5.7435	3.6231	2.3230	1.2288
A	→	Y	↓	0.1433	0.1319	0.1165	0.1354	5.0977	3.2906	1.5632	0.8522
B	→	Y	↑	0.1079	0.1010	0.0985	0.1145	5.7388	3.6222	2.3758	1.2287
B	→	Y	↓	0.1462	0.1349	0.1151	0.1232	5.0972	3.2910	1.4246	0.8517
C	→	Y	↑	0.0749	0.0720	0.0613	0.0619	5.7139	3.6126	2.3182	1.1839
C	→	Y	↓	0.0669	0.0610	0.0608	0.0709	5.0532	3.2683	1.5673	0.8288