ARM-Cadence Encounter™ Reference Methodology Release Note

CORTEXM0INTEGRATION
Release RM7.1USR2
00rel1

Confidential
Cadence Design Systems Inc

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REVISION HISTORY

No.	Description	Date
00rel0	RM7.1USR1 production release	April 2008
00rel1	RM7.1USR2 production release	August 2008

REFERENCED DOCUMENTS

No.	Description
1	ARM-Cadence Encounter Reference Methodology User Guide
2	Encounter User Guide, Product Version 7.1.2

INTRODUCTION

This document is a release note for the ARM-Cadence Encounter Implementation Reference Methodology for implementing ARM CORTEXM0INTEGRATION microprocessor core. This document is specific to the iRM accompanying the current release of the RTL and information in it may change. For a full user guide and flow details see the user guides.

This methodology should allow users to quickly set up and take a core from RTL to GDSII without a detailed knowledge of all the tools used. For expert users, this document describes the steps in sufficient detail to allow users to make adjustments to the flow.

MACHINE REQUIREMENTS

The ARM CORTEXM0INTEGRATION iRM was tested on 64bit opteron machines.

Users should expect runtimes in the order of 5 hours for the entire flow

ERRORS AND WARNINGS

Errors

No errors found.

Warnings

These warnings and others like them are expected and can be safely ignored. More detail is provided as appropriate.

cortexm0integration_synthesis.log Warning : Replacing previously read Verilog description. [VLOGPT-6]Replacing Verilog description 'cm0_acg' with Verilog module in file './../../../misc/cells/fe_tsmc090g_sc-adv_v10_2007q4v2/cm0_acg.v' on line 23, column 14.

Explanation: This warning occurs as the clock gating RTL description read from the RTL dir is overwritten by the hand instantiated description read in from the misc/cells directory.

cortexm0integration_synthesis.log Warning : Unconnected bits of instance input port detected. [ELABUTL-124] : Unconnected bits of input port 'SI' of instance 'HANDINST_rst_sync0' of module 'SDFFRX1AD' in file './../../../misc/cells/fe_tsmc090g_sc-adv_v10_2007q4v2/cm0_reset_sync.v' on line 55, column 33.

Explanation: This warning says that the SI port in hand-instantiated module is not connected. The SI port will be connected while connecting scan chains in the synthesis.

Warning : Ignored option. [DFT-127] : Specified source 'SE' matched an existing port/pin; ignoring option '-create_port'. : A given option can be safely ignored.

Explanation: This warning states that since SE signal was already existing the RTL, synthesis tool will be using that signal instead of creating a new one.

cortexm0integration_synthesis.log:Warning : The variant range of wire parameters is too large. [PHYS-12]

cortexm0integration_synthesis.log:Warning : Relaxing an attribute value in the library. [LBR-39]

cortexm0integration_synthesis.log:Warning: Ignored 'hdl_ff_keep_feedback' and 'hdl_ff_keep_explicit_feedback' attributes. [CDFG-277]

cortexm0integration_synthesis.log:Warning : Unreachable statements for case item. [CDFG-472]

cortexm0integration_synthesis.log:Warning : Possible timing problems have been detected in this design. [TIM-11]

cortexm0integration_synthesis.log:Warning : This attribute will be obsolete in a next major release. [TUI-32]

cortexm0integration_synthesis.log:**WARN: (TCLCMD-1013): The SDC set_operating_conditions assertion is not supported. Please use the Encounter setOpCond command to specify library and operating condition information. Use the setAnalysisMode command to control single vs. bestCase/worstCase vs. on-chip variation timing analysis. (File ./.rcenc__29271cortexm0/rc2enc.sdc, Line 462323).

cortexm0integration_synthesis.log:Warning : Annotated physical data will be ignored for timing analysis. [PHYS-256]
cortexm0integration_synthesis.log:Warning : Cannot annotate physical data on this net. [PHYS-254]

cortexm0integration_synthesis.log:Warning : Removing unused register. [CDFG-508]

cortexm0integration_synthesis.log:Warning : Ignoring delay specifier. [VLOGPT-35]

cortexm0integration_synthesis.log: **WARN: (SOCLF-200): Pin 'A' in macro 'ANTENNAAD' has no ANTENNAGATEAREA attribute defined.
cortexm0integration_synthesis.log: WARNING: scanDEF chains have been created for analyzed top-level scan chains.

cortexm0integration_synthesis.log:**WARN: (SOCOPT-3465): The buffer cells were automatically identified. The command setBufFootPrint is ignored. If you want to use this manual setting, rerun encounter with dbgGPSAutoCellFunction set to 0.

cortexm0integration_synthesis.log:**WARN: (SOCDC-1159): Invalid input transition time. The default 0.1ps input transition time will be used.

cortexm0integration_synthesis.log:**WARN: (SOCEXT-2760): Layer M10 in the cap table is larger than max number of layers, 9, defined in the LEF file.

cortexm0integration_synthesis.log:**WARN: (SOCEXT-2771): Top layer, M10, of Via VIA_9 in the cap table is larger than max number of layers, 9, defined in the LEF file.

cortexm0integration_synthesis.log:**WARN: (SOCEXT-2710): Cap table for M10 is ignored, the layer is not defined in the design.

cortexm0integration_synthesis.log:**WARN: (SOCOPT-3466): The inverter cells were automatically identified. The command setInvFootPrint is ignored. If you want to use this manual setting, rerun encounter with dbgGPSAutoCellFunction set to 0.

cortexm0integration_floorplan.log:WARNING (CTE-25): Line: 9, 10 of File ../data/cortexm0integration_constraints.sdc : Skipped unsupported command: set_units

cortexm0integration_floorplan.log:**WARN: (SOCSP-5134): Setting cellInterval to 39.760 (microns) as a multiple of cell FILL2AD's

cortexm0integration_floorplan.log:WARNING (SOCFP-0157): Provided Box is not fully inside CoreBox, might be modified to fit in.

cortexm0integration_floorplan.log:**WARN: (SOCPP-2008): AddStripe option -remove_floating_stripe_over_block is ON so all fragmented stripes within a block will be removed.

cortexm0integration_floorplan.log:**WARN: (SOCPP-358): The bottom edge of the area you specified has been reset to bottom edge of design boundary : 0.00.

cortexm0integration_floorplan.log:**WARN: ViaGen Warning: intersection area too small to fit 1 cut, no via created:

cortexm0integration_floorplan.log:**WARN: ViaGen messages reach 100 limit, stop issuing.

cortexm0integration_floorplan.log:**WARN: (SOCSR-554): Top target layer is beyond top routing layer. Set top target layer to 1.

cortexm0integration_placement.log:**WARN: (SOCOPT-3186): *** switching analysis mode to "setAnalysisMode -usefulskew true" so that newly generated latencies are taken in account by the timing engine***

cortexm0integration_placement.log:**WARN: (SOCOPT-3034): Optimization process capabilities limited due to 2 assigned nets

cortexm0integration_placement.log: **WARN: (SOCDC-1629): The variable rdaUseDefaultDelayLimit was set to 101. This is less than the default 1000 and may result in inaccurate results for high fanout nets. To change the variable, run command setUseDefaultDelayLimit.

cortexm0integration_placement.log:**WARN: (SOCOPT-3035): Optimization process capabilities limited due to 1 assigned net

cortexm0integration_placement.log:**WARN: (SOCOPT-3039): skewClock: latency file: latency_file.sdc. Will be overwritten.

cortexm0integration_cts.log: #WARNING (NRDB-812) Cuts within VIA VIA7_4CUT violate adjacent cut spacing rule

cortexm0integration_cts.log:#WARNING (NRCM-25) file .timing_file.tif does not exist.

cortexm0integration_cts.log: **WARN: (SOCCK-661): Clock FCLK has multiple definitions in the clock tree specification file.

cortexm0integration_cts.log:#WARNING (NRDB-187)

cortexm0integration_cts.log:**WARN: (TCLCMD-986): Clock waveform 'VCLK' cannot be used in propagated modes since this is a virtual clock. (File ../data/cortexm0integration_propagated.sdc, Line 20679).

cortexm0integration_cts.log: #WARNING (NRDB-812) Cuts within VIA VIA7_4CUT violate adjacent cut spacing rule.

cortexm0integration_cts.log:**WARN: (SOCOPT-3050): setUsefulSkewMode -useCells in the .mode file is pointing to the cell CLKBUFX8AD which is set as dont_use in the library. Be aware that usefulSkew algorithm will potentially insert such cell

This is due to fixed clock nets, these are cleaned up later in the flow

cortexm0integration_route.log: **WARN: (SOCOPT-3186): *** switching analysis mode to "setAnalysisMode -usefulskew true" so that newly generated latencies are taken in account by the timing engine***

cortexm0integration_route.log #WARNING (NRDB-874) Net u_top/u_core/mul_res_28 is completely routed, but has dangling wires. NanoRoute will remove these dangling wires.

cortexm0integration_route.log. #WARNING (NRGR-22) Design is already detail routed.

cortexm0integration_route.log:#WARNING (NRDR-123) Some nets are not detail routed. Can not do post route wire optimization (widening or spreading). Will do normal detail routing if possible.

cortexm0integration_route.log:**WARN: (SOCMF-125): Skip layer M8 due to missing FillMinWidth

cortexm0integration_route.log:**WARN: (SOCMF-138): Layer [1] Active spacing(600) should be greater than the value in LEF file. Program default change to (1220)

cortexm0integration_route.log:**WARN: (SOCEXT-3400): Option '-noReduce' is obsolete. Use option '-reduce 0.0' instead.

cortexm0integration_si_fixing.log: **WARN: (SI-2086) Number of Timing Window Data ignored: 636 [load_timing]

cortexm0integration_si_fixing.log:**WARN: (SI-2129) Net DBGPWRDOWN (type 1) has no outputs; cannot analyze

cortexm0integration_si_fixing.log.**WARN: (SDF-425): TIMESCALE in SDF file is not the same as the library time units. Automatically scaling delays by 0.001000 (Line 10)

cortexm0integration_si_fixing.log #WARNING (NRDB-51) SPECIAL_NET _FILLS_RESERVED does not have connection and wire, ignore it.

cortexm0integration_si_fixing.log:**WARN: (SOCEXT-3261): The timing is reset by command extractRC. Run command sdfIn after command extractRC if you intend to use sdf file.

cortexm0integration_si_fixing.log #WARNING (NRDB-874 Repeated 20 times. Will be suppressed.) Net u_top/u_core/u_ctl/u_dec/n_939 is completely routed, but has dangling wires. NanoRoute will remove these dangling wires file.

cortexm0integration_si_fixing.log:WARNING: The reportTA command is obsolete.

cortexm0integration_si_fixing.log:#WARNING (NRDB-51) SPECIAL_NET _FILLS_RESERVED does not have connection and wire, ignore it.

cortexm0integration_si_fixing.log:**WARN: (SI-2190) The default for report generation has changed from HTML to text. To generate an HTML report, specify the -html option to the generate_report command. [reports]

cortexm0integration_qrc.log:WARNING (EXTSNZ-114) : There are 20 vias which have non-zero center point.

cortexm0integration_qrc.log:WARNING (EXTRDL-117) : There were 24 incomplete nets which have no pins,

Can be fixed using LPE spice netlists to make cdb’s

cortexm0integration_signoff_bc.log:**WARN: (SI-10036) There is no incremental delay for the net FE_OFN1043_IOBUF_N_42because no significant switchable attackers could be enabled. [ets]

cortexm0integration_signoff_bc.log: **WARN: (SI-2239) The victim net u_top/u_core/mul_res_1 has a receiver, u_top/u_core/u_dmx/g945:B (cell OR2X2AD), with a non-monotonic output waveform. The bumpy transition can cause incorrect delay uncertainty measurements to be reported. Perform ECO on this net to reduce the coupling capacitance. [ets]

cortexm0integration_signoff_bc.log:**WARN: (SI-4557) 124 Nets have no outputs; they cannot be analyzed [process_netlist]

cortexm0integration_signoff_bc.log:**WARN: (SOCDB-2139): Input netlist has a cell BUFX11BA12TR which is marked dont_use in the library.

cortexm0integration_rtl_vs_netlist_lec.log// Warning: (RTL14) Signal with fanin drive and no fanout load detected (occurrence:671)

cortexm0integration_rtl_vs_netlist_lec.log// Warning: (DIR6.1) Compiler directive ignored (occurrence:627)

cortexm0integration_rtl_vs_netlist_lec.log// Warning: (DIR6.2) Compiler directive supported (occurrence:1288)

cortexm0integration_rtl_vs_netlist_lec.log// Warning: (HRC3.8) Port positional association exist in instantiation (occurrence:304)

cortexm0integration_rtl_vs_netlist_lec.log// Warning: (RTL1.5b) Potential loss of RHS msb or carry-out bit (occurrence:5)

cortexm0integration_rtl_vs_netlist_lec.log// Warning: (RTL2.5) Undriven net is found (occurrence:2)

cortexm0integration_rtl_vs_netlist_lec.log// Warning: (RTL2.13) Undriven pin is found (occurrence:2)

cortexm0integration_rtl_vs_netlist_lec.log// Warning: (RTL14) Signal with fanin drive and no fanout load detected (occurrence:144)

cortexm0integration_rtl_vs_netlist_lec.log// Warning: (DIR6.2) Compiler directive supported (occurrence:45)

cortexm0integration_rtl_vs_netlist_lec.log// Warning: There are 2 undriven nets in Golden

cortexm0integration_rtl_vs_netlist_lec.log// Warning: There are 2 undriven pins in Golden

cortexm0integration_rtl_vs_netlist_lec.log// Warning: Golden root module is already at 'CORTEXM0'

cortexm0integration_rtl_vs_netlist_lec.log// Warning: (RTL2.5) Undriven net is found (occurrence:9)

cortexm0integration_rtl_vs_netlist_lec.log// Warning: (RTL2.13) Undriven pin is found (occurrence:6)

cortexm0integration_rtl_vs_netlist_lec.log// Warning: (RTL14) Signal with fanin drive and no fanout load detected (occurrence:235)

cortexm0integration_rtl_vs_netlist_lec.log// Warning: There are 6 undriven nets in Revised

cortexm0integration_rtl_vs_netlist_lec.log// Warning: There are 6 undriven pins in Revised

cortexm0integration_rtl_vs_netlist_lec.log// Warning: Revised root module is already at 'CORTEXM0'

cortexm0integration_rtl_vs_netlist_lec.log// Warning: Module 'VDW_mult_wall_u32_u32_64' exists in Golden only. Skip it for hierarchical comparison

cortexm0integration_rtl_vs_netlist_lec.log// Warning: Revised module 'cortexm0integration_core_pfu_CBAW0_DBG1' has extra input(s): RC_CG_CLK_PORT

cortexm0integration_rtl_vs_netlist_lec.log// Warning: Module 'cortexm0integration_core_pfu_CBAW0_DBG1' and 'cortexm0integration_core_pfu_CBAW0_DBG1' have mis-match ports

cortexm0integration_rtl_vs_netlist_lec.log// Warning: Revised module 'cortexm0integration_core_dec' has extra output(s): spu_ctl_raw[0]

cortexm0integration_rtl_vs_netlist_lec.log// Warning: Ports of module 'cortexm0integration_nvic_CBAW0_OS1_DBG1_NUMIRQ32_BE0_WIC1_WICLINES34' in Golden are declared with different direction from those in Revised

cortexm0integration_rtl_vs_netlist_lec.log// Warning: Primary input 'ctl_i[9]' in Revised has no correspondence in Golden

cortexm0integration_rtl_vs_netlist_lec.log// Warning: Total black box modules referenced in Revised = 5

cortexm0integration_rtl_vs_netlist_lec.log// Warning: There are 2 undriven nets in Revised

cortexm0integration_rtl_vs_netlist_lec.log// Warning: There are 2 undriven pins in Revised

cortexm0integration_rtl_vs_netlist_lec.log// Warning: Golden and Revised have different numbers of key points:

cortexm0integration_ampkg_sdf_worst.log:ncelab: *W,SDFNET: Failed Attempt to annotate to non-existent timing check (PERIOD (negedge CK) (0)) of instance cortexm0.u_cpu0.u_cpu_ram.u_dside_ram_drive.douterram_addr_q_reg_0 of module SDFFQX1MA12TR <../data/cortexm0integration_post_route_si.model.sdf, line 2420814>.

cortexm0integration_vstorm2_static.log: WARNING (EXTZCORE-102) : ignore_shorts and port/label cmds are not compatible options.

cortexm0integration_powermeter_static.summary.log :Warning: 2 cell(s) in the design have Synopsys Timing Library models but do not have internal power data. Internal power will not be calculated for these cells:

TIEHIAD

TIELOAD

End