FUJITSU Processor A64FX

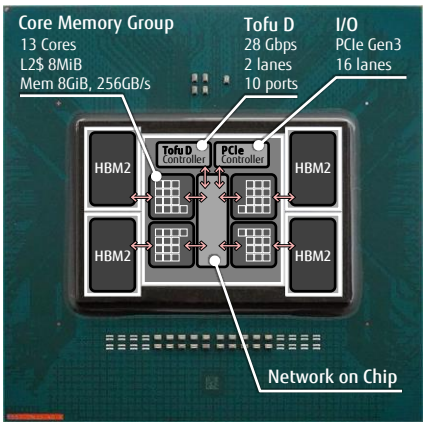
Innovative Arm-based HPC processor

Designed for the new generation of massive parallel computing

The A64FX processor (called A64FX, below) is a superscalar processor of the out-of-order execution type. The A64FX is designed for high-performance computing (HPC) and complies with the Armv8-A architecture profile and the Scalable Vector Extension for Armv8-A.

The processor integrates 52 processor cores including assistant cores; a memory controller supporting HBM2; a Tofu interconnect D controller; and a root complex supporting PCI-Express Gen3. The A64FX adopts several characteristic architectures for HPC.

The A64FX becomes the heart of supercomputers that can perform quick simulations and analyze large data sets. Supercomputers with this processor perform at a high level, are highly reliable and offer a strong performance vs. power ratio.



A64FX Main Features	
Predicated Operations	Enable selectively operate, load, and store only specific SIMD elements.
Four-operand FMA	In the operation of A x B + C => D, the register of A, B, C, and D can be freely selected Although Armv8-A SIMD has only A x B + C => C operations, the A64FX realizes Four-operand FMA by packing with MOVPRFX instruction.
Gather/Scatter	Reads discontinuous data in memory and converts to SIMD (vectorization) Writes SIMD (Vector) data to non-contiguous area in memory.
Math. Acceleration	Speeds up when finding trigonometric and exponential functions.
Compress	Aggregates data that is sparse on registers.
First Fault Load	Suppresses and records traps other than the first element in memory access instructions.
Hardware Barrier	Supports synchronization between software processes or threads through hardware for simplification of programs and higher-speed synchronization processing.
Sector Cache	Provides software with a method of controlling the use of the L1 and L2 cache by partitioning each cache.
FP16/ INT16/ INT8 Dot Product	Introduced for AI applications.

Fujitsu Processor A64FX Specifications

CPU Specifications		
ISA		Armv8.2-A + SVE
Number of Processor Cores		48 compute cores, and 2 or 4 assistant cores *
Threads		48
Base Frequency		1.8GHz, 2.0GHz, 2.2GHz
Turbo Frequency		None (same as base frequency)
SIMD Width		512bit
L1I Cache Size		3MiB (64KiB /core)
L1D Cache Size		3MiB (64KiB /core)
L2 Cache Size		32MiB (8MiB x 4)
Cache-Line Size		256 bytes
Memory Controller		4
SVE-Implemented Vector Length		128 / 256 / 512bits
Peak Flops; D / S / H [FLOPS]	1.8GHz	2.7648T / 5.5296T / 11.0592T
	2.0GHz	3.072T / 6.144T / 12.288T
	2.2GHz	3.3792T / 6.7584T / 13.5168T
Peak Int Ops; 8 / 4 / 2 / 1B [OPS]	1.8GHz	2.7648T / 5.5296T / 11.0592T / 22.1184T
	2.0GHz	3.072T / 6.144T / 12.288T / 24.576T
	2.2GHz	3.3792T / 6.7584T / 13.5168T / 27.0336T
Network		Tofu interconnect D [68GB/s x2 (in/out)] *
IO / Socket		PCIe Gen3 16 lanes [15.75GB/s(in/out)] (Need chipsets for USB/SATA)
Process Technology		7 nm CMOS FinFET
Number of Transistors		8,786M pcs
Package Signal Pins		594 BGA pins

* Only when the frequency is 2.2 GHz

Memory Specifications		
Memory Bandwidth		1,024 GB/s
Memory Capacity		32 GiB
Number of HBM2 Stacks Per Package		4
HBM2	Data Signal Transfer Rate	2.0 Gbps
	Data Width	1,024 bits
	Memory Bandwidth	256 GB/s
	Memory Capacity	8 GiB

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