ARM-SYNOPSYS Galaxy™ Implementation Reference Methodology (iRM) 2008.09

Release Note

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Feedback on the ARM-Synopsys Galaxy Implementation Reference Methodology

If you have any comments or suggestions about this product, please contact your supplier giving:

- The Product name
- A concise explanation of your comments.

Change history

This is the first draft of the release note for the fully featured 2008.09 iRM release.

Contents

1 LIBRARY AND TOOL SUPPORT

1.1 Technical data

The ARM-Synopsys Galaxy Implementation Reference Methodology scripts support the following tool versions:

Synopsys Product	Supported Version
Design Compiler	2008.09-SP2
IC Compiler	2008.09-SP2
Formality	2008.09-SP2
PrimeTime SI	2008.06-SP3
PrimeTime PX	2008.06-SP3
TetraMAX	2008.09-SP2
Star-RCXT	2008.12
PrimeRail	2008.12

1.2 What's New in This Release

This updated release of the iRM introduces a number of new features. The major updates are listed below.

1.2.1 Design Compiler Topographical

- Library consistency checking

The *check_library* command is used to perform library consistency checking. Checks are made between logic and physical libraries, cross logic libraries, and intra-physical libraries. These checking functions are available in both IC Compiler and Design Compiler

- New UI for clock gating

Power Compiler clock gating is now performed using the *gate_clock* argument to *compile_ultra.* This replaces the *insert_clock_gating* command which was used in earlier releases.

1.2.2 DFT Compiler

- Automatic connection of clock-gating test ports

The functionality of the *hookup_testports* command has been moved into the DFT insertion step. Explicit use of *hookup_testports* command is no longer required

- Concurrent implementation of Scan Compression and Test Wrappers

The Methodology has supported the implementation of Test Wrappers for some time, and more recently support for DFT-MAX scan compression has been added. Until recently these two features were mutually exclusive: however, this new release now supports the co-existence of both test wrappers and DFT-MAX scan compression. Each of these features is optional and controlled by flow variables.

1.2.3 IC Compiler

- Command updates for Floorplanning

The design planning scripts have been updated to use current ICC Design Planning tool commands.

- Z-Route functionality

This release introduces the use of Zroute router to the Methodology. Zroute is state-of-the-art routing technology which delivers the following advantages compared to traditional routers:

Considerable runtime and QoR improvements

Concurrent Design-for-Manufacturing (DFM) optimization

Employs multi-threading algorithms to take advantage of multi-core compute resources

- MCMM scenario enhancements

Multi-Corner, Multi-Mode support was introduced in the previous release of the iRM. This update enhances MCMM support with the introduction of a test-mode scenario for optimization steps.

1.2.4 TetraMAX ATPG

- Enhanced support for power-aware ATPG

TetraMAX generates power-aware patterns to avoid excessive power consumption during test. This can damage devices or cause false failures. TetraMAX is now power-aware during ATPG for both shift AND capture. Clock gating logic is now utilized during ATPG to keep patterns within a switching budget. Analysis is made on all patterns to be able to report on switching activity.

- Comprehensive Support for Dynamic Bridging Faults

ATPG now supports a dynamic bridge fault model to allow detection of resistive bridges

- Fast-Sequential ATPG for Small Delay Defects (SDD)

SDD support is now extended to fast sequential ATPG to allow detection of small delay defects around non-scan logic such as RAMs.

2 RTL CONFIGURATION

2.1 Introduction

CORTEXM0 requires some configuration before it may be implemented but the default configuration is supported out-of-box by the inclusion of files in the *misc* directory (see later).

3 INSTALLATION

3.1 Directory Structure

The iRM directory structure is intended to match the existing structures used in other ARM deliverables. If you already have the ARM processor product and it's associated RTL files, the iRM delivery can be easily integrated.

<top>/doc/implementation_reference_methodology/SNPS_CORTEXM0_Release_Notes_2008_09.pdf

<top>/doc/implementation_reference_methodology/SNPS_CORTEXM0_User_Guide_ICC_2008_09.pdf

<top>/implementation_tsmc90_g_lowk/cortexm0/synopsys/build_dir/

<top>/implementation_tsmc90_g_lowk/cortexm0/misc/cells/fe_tsmc090g_sc-adv_v10_2007q4v2/*.v

<top>/implementation_tsmc90_g_lowk/cortexm0/misc/wrappers/fe_tsmc090g_sc-adv_v10_2007q4v2/

<top>/implementation_tsmc90_g_lowk/cortexm0_integration/synopsys/build_dir/

<top>/implementation_tsmc90_g_lowk/cortexm0_integration/misc/cells/fe_tsmc090g_sc-adv_v10_2007q4v2/*.v

<top>/implementation_tsmc90_g_lowk/cortexm0_integration/misc/wrappers/fe_tsmc090g_sc-adv_v10_2007q4v2/

<top>/implementation_tsmc90_g_lowk/design_kits/tsmc/star-rcxt/README

<top>/implementation_tsmc90_g_lowk/design_kits/tsmc/star-rcxt/*.map

<top>/implementation_tsmc90_g_lowk/design_kits/arm/fe_tsmc090g_sc-adv_v10_2007q4v2/README.*

<top>/implementation_tsmc90_g_lowk/design_kits/arm/fe_tsmc090g_sc-adv_v10_2007q4v2/aci/sc-ad/cell_list

<top>/implementation_tsmc90_g_lowk/design_kits/arm/fe_tsmc090g_sc-adv_v10_2007q4v2/aci/sc-ad/doc/

<top>/implementation_tsmc90_g_lowk/design_kits/arm/fe_tsmc090g_sc-adv_v10_2007q4v2/aci/sc-ad/verilog/

<top>/implementation_tsmc90_g_lowk/design_kits/arm/fe_tsmc090g_sc-adv_v10_2007q4v2/aci/sc-ad/astro/

<top>/implementation_tsmc90_g_lowk/design_kits/arm/fe_tsmc090g_sc-adv_v10_2007q4v2/aci/sc-ad/synopsys/

<top>/implementation_tsmc90_g_lowk/design_kits/arm/fe_tsmc090g-hvt_sc-adv_v10_2007q4v1/README.*

<top>/implementation_tsmc90_g_lowk/design_kits/arm/fe_tsmc090g-hvt_sc-adv_v10_2007q4v1/aci/sc-ad/cell_list

<top>/implementation_tsmc90_g_lowk/design_kits/arm/fe_tsmc090g-hvt_sc-adv_v10_2007q4v1/aci/sc-ad/doc/

<top>/implementation_tsmc90_g_lowk/design_kits/arm/fe_tsmc090g-hvt_sc-adv_v10_2007q4v1/aci/sc-ad/verilog/

<top>/implementation_tsmc90_g_lowk/design_kits/arm/fe_tsmc090g-hvt_sc-adv_v10_2007q4v1/aci/sc-ad/astro/

<top>/implementation_tsmc90_g_lowk/design_kits/arm/fe_tsmc090g-hvt_sc-adv_v10_2007q4v1/aci/sc-ad/synopsys/

The directory *doc/implementation_reference_methodology* contains two documents related to ARM-Synopsys iRM:

- SNPS_CORTEXM0_Release_Notes_2008_09.pdf contains this release note.
- SNPS_CORTEXM0_User_Guide_ICC_2008_09.pdf contains details on the ARM-Synopsys iRM scripts and flow.

The directory *synopsys* contains the iRM scripts and a floorplan to implement the CORTEXM0 processor under *build_dir*. The library specific directory under *misc/cells* contains specific library cell instantiations used in the CORTEXM0. See the Configuration and Sign-off Guide, and the header in each file for comments on their functionality. For a User's implementation using the iRM, these extra files should not appear on the search path but User-configured RTL should be used instead. The library specific directory under *misc/wrappers* contains a top level wrapper for the core to be implemented. This file can be used to set parameters in order to configure the core being implemented. User I/O pins can also be added to this top level wrapper verilog. In the iRM scripts these are located higher up the search path than the RTL and so are used first.

3.2 Design Kits Structure and Content

All libraries contained within the design kit are sourced from the ARM-Artisan Physical IP Division. The design kit contains two directories containing the standard cell libraries and technology files. These are explained further below:

- *tsmc*: will contain all the process corner .tluplus and .nxtgrd files required for Star-RCXT extract.

Note Foundry related data is not being shipped with the design_kit and should be obtained directly from the foundry. TLUPlus files will need to be generated from the foundry deliverables, see later.

- *arm*: This directory consists of the Milkyway and Tetramax views, and documentation for all the regular and high-Vt standard cells in directories named for the tar-balls from which they come.

Note Files in the Milkyway library may have been re-compiled with tool versions compatible with the ones used for this release

4 CONFIGURATION AND DATA PREPARATION

4.1 RTL Configuration

See the Configuration and Signoff Guide for an explanation of this configuration process.

4.2 nxtgrd File Sourcing & TLUPlus File Generation

nxtgrd and TLUPlus models are a set of interconnect models containing advanced process effects that can be used by the extractors and estimators in Synopsys synthesis and place-and-route tools for parasitic modeling.

A list of the required nxtgrd and TLUPlus files are given in the README located here:
implementation_tsmc90_g_lowk/design_kits/tsmc/star-rcxt/README

TLUPlus models are generated using the **grdgenxo** binary in Synopsys' Star-RCXT tool release. A description of the process must be provided in an Interconnect Technology Format (ITF) file, obtained from the foundry along with the nxtgrd files..

% grdgenxo -itf2TLUPlus -i <ITF file> {-f <format file>} -o <TLU file>

The output TLUPlus model file is in a binary format having an ASCII header section with the input file information, so that you can verify which input files were used for the binary model. When ICC TLU parasitic extraction is performed, it must be attached to the Milkyway library using the Milkyway cmItfToTLUPlus command (done automatically by the iRM scripts).

The command **grdgenxo -itf2TLUPlus** generates a directory called <TECHNOLOGY_NAME>.TLUPlus, and saves temporary results under that directory. The input ITF file and the format file (not usually required) are also saved as .itf and .format, respectively, under the directory. The directory can be discarded when generation of the TLUPlus file is complete.

Note1: It is mandatory that the option **-itf2TLUPlus** is specified first after **grdgenxo**.
Note2: Multiple **grdgenxo** jobs can be run simultaneously in the same directory on the same .itf file by running the same **grdgenxo** command multiple times. This greatly speeds up TLUPlus file generation.

5 KNOWN ISSUES

5.1 Errors and Warnings

The following is a list of Warnings and Errors that may appear in the output logs when running the iRM scripts on the reference implementation. The list may not be complete (since some Warnings are not unusual to Users and are regularly ignored) and may also contain Warnings that do not occur for this particular core (they are common warnings for these tool versions).

Warning: Value for <delay> is negative. (UID-450)

DESCRIPTION:

This warning message indicates that a negative delay has been set. In the case of the early falling clock edge to model duty-cycle distortion, this is correct and safe to ignore.

Warning: The following ports of sub-design 'ARM926EJSCore' have no corresponding Signals in its test core: 'uCORE_u9EJ_uARM9_uDbg_uDbgctl_uICEctl_uDbgCommsctl_uCORE_u9EJ_uARM9_uDbg_uDbgctl_uICEctl_uDbgCommsctl_N104_out'... (UIT-500)

Warning: The following test core Signals have no corresponding ports in sub-design 'ARM926EJSCore': 'uCORE/u9EJ/uARM9/uDbg/uDbgctl/uICEctl/uDbgCommsctl_uCORE/u9EJ/uARM9/uDbg/uDbgctl/uICEctl/uDbgCommsctl/N104_out'… (UIT-501)

DESCRIPTION:

These warnings are the subject of DFT Compiler STAR 9000232985.

Warning: The trip points for the library named RF32X26m2wo differ from those in the library named scadv_tsmc_cln90g_lvt_ss_0p9v_125c. (TIM-164)

DESCRIPTION:

This warning message occurs when two libraries with different trip-point values are being used. This may result in a loss of timing accuracy when cells from one library are connected to cells of the other library.

This is a warning only - no action is required.

Warning: In the design TestWrapper, net 'DBGTCKEN' is connecting multiple ports. (UCN-1)
Warning: Port 'nFIQ' is connected to 2 input registers and 2 other logic, IO registers are not used to wrap the port. (TEST-1060)
Warning: IO register 'uCORE/uBIU/uDBIU/clk_gate_HLOCK_reg/latch' is violated by drc, the register is not used to wrap the port. (TEST-1066)

DESCRIPTION:

These warnings are seen during test wrapping. A complex input, flagged here, requires a different wrapping technique

These are warnings only - no action is required.

Warning: Created physical library cell for logical library cell <CORE>_DW_wc_s1_s_rst_mode0_test_111. (OPT-1413)

DESCRIPTION:

This warning is issued when Test-wrapping is performed. Wrapper cells are chosen from the DesignWare library; there is no physical representations for these cells. Design Compiler version Z-2007.03 supports designs with macros or cells that do not have a physical representation. This feature is enabled by default. Design Compiler topographical will issue a OPT-1413 warning when creating physical library cells.

This is a warning only - no action is required.

Warning: Found 8 percent of cells (4684) without DC Topographical data. Generating data for those cells... (OPT-1404)

DESCRIPTION:

This is related to the OPT-1413 warning. The wrapper insertion process has chosen cells from the Designware library; these cells are still to be placed and optimized by DC-Topographical.

This is a warning only - no action is required.

Warning: Port 'WSEIN' cannot be isolated because the connected net 'WSEIN' is dont_touch. (OPT-143)

DESCRIPTION:

Occurs when test wrapping is enabled. The port is automatically marked as a requiring different treatment than a regular port when adding isolation cells to the design.

This is a warning only - no action is required.

Warning: Cell <MACRO> has no function specification. Warning: Violations occurred during test design rule checking. (TEST-124)

DESCRIPTION:

Typically seen on all instantiated macros because they do not have a functional specification, unlike a standard cell, that can be understood by DFT Compiler

This is a warning only - no action is required.

Warning: Verilog writer has added 29 nets to module <CORE> using SYNOPSYS_UNCONNECTED_ as prefix. Please use the change_names command to make the correct changes before invoking the verilog writer. (VO-11)

DESCRIPTION:

The Verilog netlist writer issues a VO-11 warning message if it modifies the netlist, that is, it renames any identifiers while writing it out.

This is a warning only - no action is required.

Warning: no core_area specified for remove (MWUI-203)

DESCRIPTION:

This warning is issued when a floorplan file is loaded that was generated by the ICC-DP command `write_floorplan`. It is intended to overwrite an existing core area. By default the design will not have a defined floorplan before the replay file is loaded.

This is a warning only - no action is required.

Warning: Undo stack cleared by command 'create_fp_placement' (HDU-104)

DESCRIPTION:

This warning gets issued when a floorplan file is loaded that was generated by ICC-DP command `write_floorplan`. It is intended to force the floorplan to update itself with the new criteria that has been read in. This command has no undo support so the current undo stack was cleared.

This is a warning only - no action is required.

Warning: Scanchain "1" already exists and will be ignored! (DDEFR-056)

DESCRIPTION:

This message is issued when SCANDEF data is sourced during the placement step in IC Compiler. Scan chain order data is now stored within the DDC database generated in the Compile step, and is maintained in the database when transferred to IC Compiler. The message occurs when read_def tries to import a scanchain which has already been defined in Milkyway database.

This is a warning only - no action is required.

Warning: CTS will use a library cell BUFX0P7BA12TR , which has dont_touch or dont_use attribute. (CTS-099)
DESCRIPTION:
Low drive strength cells are specified as dont_touch to synthesis so they are not used within the regular logic. CTS is allowed to use low drive strength buffers (in rm_clock_cells) but the attribute is still on them.
This is a warning only - no action is required.

Warning: Skew target 0.000 ns is very low for global optimization. Using 0.041 ns. (CTS-355)
DESCRIPTION:
No specific skew target has been set with the set_clock_tree_options command. Your skew target will only be used in operations which work specifically on problem clock paths
This is a warning only - no action is required.

Warning: Both adjacent cut rule and enclosed cut rule are specified, supporting only enclosed cut rule. (ZRT-006)
DESCRIPTION:
The enclosed cut rule is a super set of adjacent cut rule which is an older rule the
router supports for backward compatibility. So if both rules are specified, only
enclosed cut rule is honored. This is a warning only - no action is required.

Warning: Hidden int parameter optXtalkDly of droute is not supported by Zroute. (ZRT-403)
DESCRIPTION:
The ZRoute parameter to option translator does not support translation of this
parameter. This is a warning only - no action is required.

WARNING : No Fill/Notch/Gap cell would be output!
DESCRIPTION:
This design-finishing step is not present in the iRM and the tool is warning that the cell resulting from that does not exist.
This is a warning only - no action is required.

Warning: Cell ‘<CORE>’ can not find child cell ' OA22X6MA12TR ' (MWSTRM-062)
DESCRIPTION:
This warning is issued during ‘export’ and occurs because the libraries in design_kits do not contain CEL views. This will not occur for a fully populated library unless there is a problem with it.
This is a warning only - no action is required.
Warning: Unconnected hierarchy pin 'uCORE/uCP15/uCPctl/udffCPINSTR/q_reg_25_/cfo_n' is missing in the RC annotation for net 'uCORE/uCP15/uCPctl/udffCPINSTR/q_reg_25_/cfo_n'. (PARA-007)
DESCRIPTION:
Nets that are created during synthesis may be removed by later optimisations. If the net crossed a hierarchical boundary then a port may be created but not, subsequently, removed.
This is a warning only - no action is required.

Warning: Switching activity at TESTMODE is reset. (PSW-189)
DESCRIPTION:
This message is generated by Primetime-PX, to indicate that non-mission mode ports are set constant.
This is a warning only - no action is required.

Warning: Generated clock 'CLK_wft1' has no path to its master clock. (PTE-075)
DESCRIPTION:

This warning is issued by Primetime, when running test-mode timing analysis. In this mode, generated clocks are created from virtual clocks for purposes of constraining I/O paths.
This is a warning only - no action is required.

Warning: Design r:/RF512X32M4BY/RF512X32m4by is a black box and there are cells referencing it (FM-160)
DESCRIPTION:
Instantiated macros are treated as black-boxes during LEC (assuming they are functionally correct).
This is a warning only - no action is required.

Warning: 0 (512) undriven nets found in reference (implementation) design; see formality.log for list (FM-399)
DESCRIPTION:
If this warning is seen and the design does not pass LEC this can be an indicator that there is something wrong with the Verilog netlist. When the design does pass LEC then these nets are things such as nets driven by black-boxes.
This is a warning only - no action is required, unless design fails LEC.

Warning: 23 (23) black-box references found in reference (implementation) design; see formality.log for list (FM-182)
DESCRIPTION:
The number of black-boxes seen in a design should equal the number of instantiated macros. If it does not then this indicates a problem
This is a warning only - no action is required, unless the number does not equal the number of macros.

Warning: Latch inferred in design A1176ICacheSelect read with 'hdlin_check_no_latch' (ELAB-395)
DESCRIPTION:
The variable hdlin_check_no_latch directs the read command to ensure no latch is inferred in the HDL file. For those cores which infer latches in the design, this warning can be ignored
This is a warning only - no action is required.

Warning: No scan equivalent exists for cell uNoRAM/uMain/uICache/uA1176ICacheSelect/Ram0DataLtch_reg[63] (LATQNX4MA12TL). (TEST-120)
DESCRIPTION:
This message identifies a cell for which no equivalent scan cell can be found in the library (a functional latch, in this case).
This is a warning only - no action is required.

Warning: IO register 'u_cortexr4noram_u_cr4caches_axim_u_cr4dc_axim_axi_awaddr_reg_reg_1_' associated with port 'AWADDRM[1]' can't be swapped with a shared wrapper cell, adding a dedicated wrapper cell to wrap the port. (TEST-1055)
DESCRIPTION:
The IO register specified is not valid for swapping with a shared wrapper cell, when test wrapping is enabled; possibly because the port is constrained with test constraints.
This is a warning only - no action is required.

Warning: There are design rule checking (DRC) violations in constant nets, due to hierarchy. (PSYN-381)
DESCRIPTION:
ICC tries to preserve design hierarchy and so constant nets that pass across hierarchy levels can not be optimised for DRC violations. This can happen with RAM configurations that tie off a few data or address bits.
This is a warning only - no action is required.

Warning: Object 'uRAM/uBRAM/uTagRAM_0_1/D[31]' is not a valid endpoint. (UITE-216)

DESCRIPTION:

Some tag ram data ports are tied low in the configuration shipped so these ports are correctly reported as invalid endpoints during timing analysis

This is a warning only - no action is required.

Warning: The following ports of sub-design 'ARM926EJSCore' have no corresponding Signals in its test core: xxx. (UIT-500)

DESCRIPTION:

This warning suggests that ports have been removed at the block level of hierarchy. This is expected behaviour for the ARM926EJ-S core, as the built-in test wrapper is being tied off and removed in synthesis.

This is a warning only - no action is required.

Warning: The preferred wire track direction hasn't been set in main library, set it according to the wire direction of the "unitTile" in main library or reference library. (DDEFR-054)

DESCRIPTION:

This occurs when the preferred wire track direction is not set in the main library. The wire direction of the "unitTile" in main library or reference library is then used as the preferred wire track direction.

This is a warning only - no action is required.

Warning: Either the driven net has been synthesized previously or clock path overlaps/reconverges at pin u_cortexr4noram_u_cr4lsu_u_main_u_store_u_sq_clk_gate_w_outer_sq0_reg/latch/ECK. (CTS-209

DESCRIPTION:

Either the net driven by the pin has been synthesized or the pin is reachable from multiple clock paths that belong to either different clocks or the same clock. Commonly this will be seen at, for example, output ports of clock-gating latches.

This is a warning only - no action is required.

Warning: Cell contains tie connections which are not connected to real PG. (MW-349)

DESCRIPTION:

Tie cell insertion occurs later in the flow and so the design planning step will produce this warning during power grid creation.

Warning: Attribute 'mv_charz' does not exist on cell 'uCORE/uFCSE/uSmpIA/clk_gate_q_reg'. (UID-101)

DESCRIPTION:

This warning is the subject of IC Compiler STAR 9000238004 and is safe to ignore.

WARNING: StarXtract

WARNING: MAX Process corner is not found in CORTEXM0NTEGRATIONIMP design library's LM view

DESCRIPTION:

This is a warning only - no action is required.

ERROR : OUTPUT PortInst u_cortexm0integration_u_cortexm0_u_top_u_sys/u_nvic_u_reg_pend_irq_r_reg_28_ QN doesn't connect to any net.

These are reported when running cell level LVS during the export stage. These refer to unused output ports on cells. In the above example the inverted QN output of a flop is not utilized. This is expected, no action is required.

ERROR : area [(225.790,318.860), (225.930,319.000)] 0.0196 um sqr.

These may be reported when running cell level LVS during the export stage, and refer to unconnected top level input/output pins which may be absent due to RTL configuration options. These can be safely ignored.