ARM Cortex A9

Alyssa Colyette
Xiao Ling Zhuang

Outline

- Introduction
- ARMv7-A ISA
- Cortex-A9 Microarchitecture
  - Single and Multicore Processor
- Advanced Multicore Technologies
- Integrating System on Chips

Introduction

- ARM Cortex-A9 is the 2nd generation of ARM MPCore technology series
- High performance
- Uses ARMv7-A ISA
- Used many embedded devices due to its ability to control different level of power consumption
  - essential for mobile devices

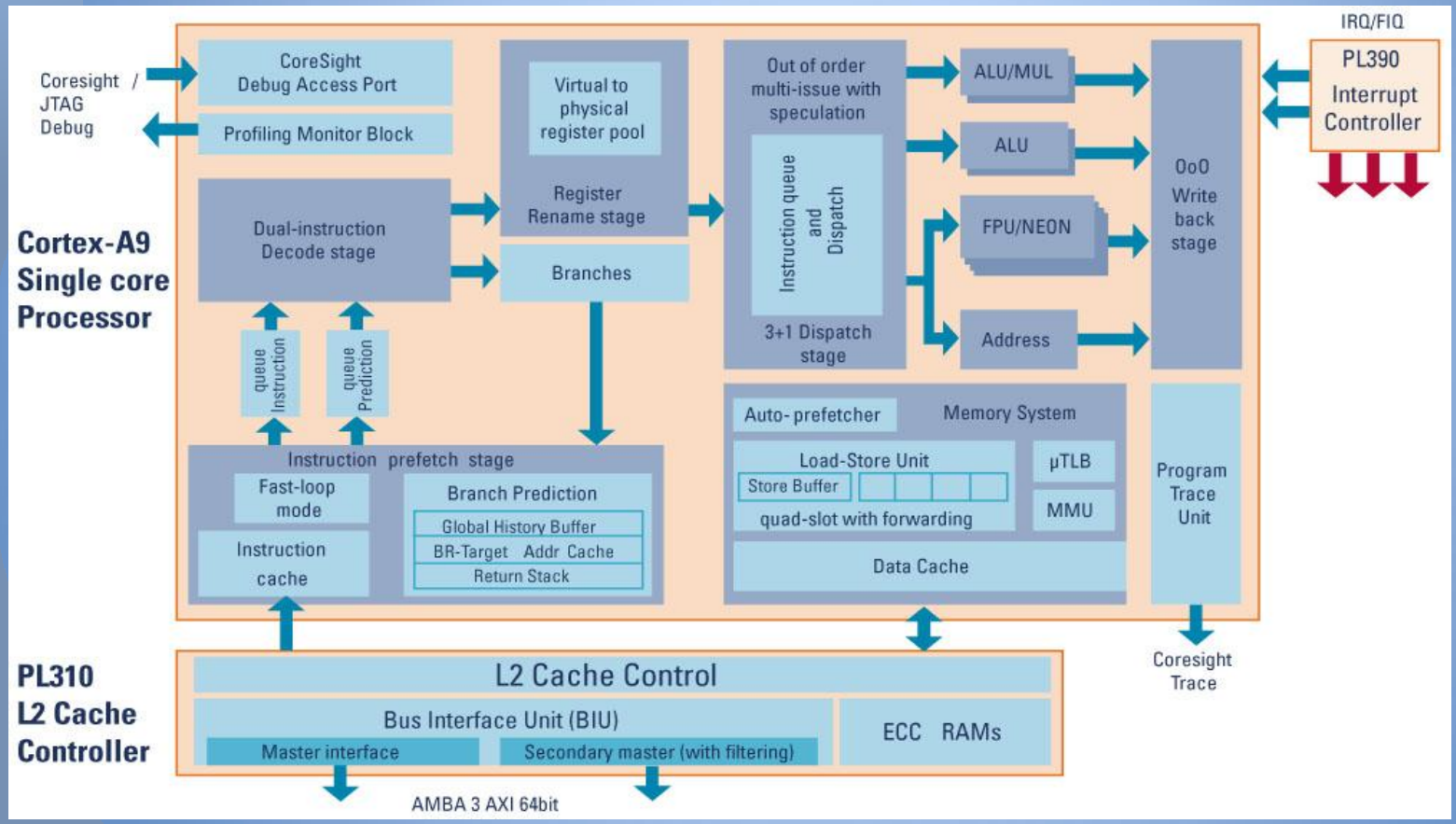
ARMv7-A Architecture

- RISC-based
- Implement two instruction sets
  - 32-bit ARM instruction set
  - 16-bit Thumb-2 instruction set
  - switch ISA as branch or exception
- 37 registers, all 32-bit long
- Support shared and local memory
- Has configurable cache policy
- Backward compatibility

Application Specific Optimization

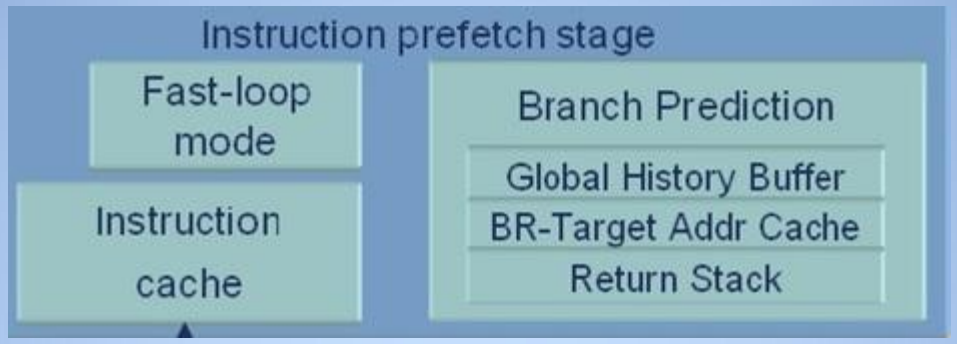
- 2.50 DMIPS/MHz (Dhrystone)
- Clock rate: 800MHz ~ 2GHz
- NEON Media and Floating Point Processing Engine
- Cache coherence option for enhanced inter-process communication
- Thumb-2 Technology: 30% reduction in memory required to store instruction
- TrustZone Technology
- L2 Cache Controller

Cortex-A9 Single Core Microarchitecture



Cortex-A9 Microarchitecture Structure and the Single Core Interfaces

Microarchitecture: Instruction Fetch

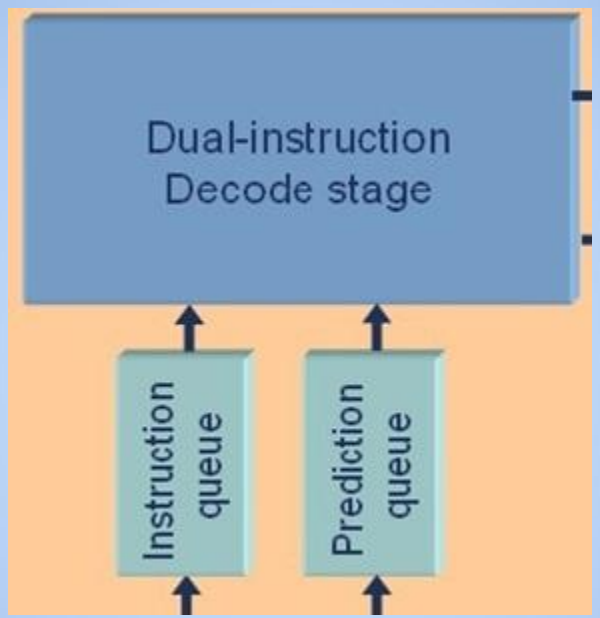


- Instruction cache size: 16, 32, or 64KB
- Fetching two instructions
- Branch prediction:

- Global History Buffer: 1-16K entries, 2-bit
- Branch-Target Address Cache: 512- 4K entries, 2-way
- Return stack of 8 x 32 bits

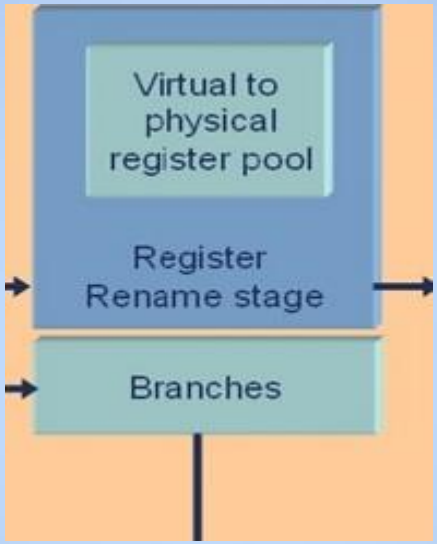
- Fast-loop mode: instruction loop smaller than 64 bytes complete without additional cache accesses

Microarchitecture: Instruction Decode



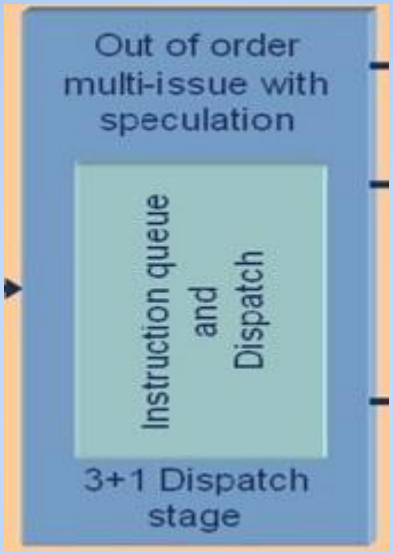
- Superscalar Decoder
  - capable of decoding two full instructions per cycle

Microarchitecture: Rename



- Register Renaming
  - resolving data dependencies
  - loop unrolling

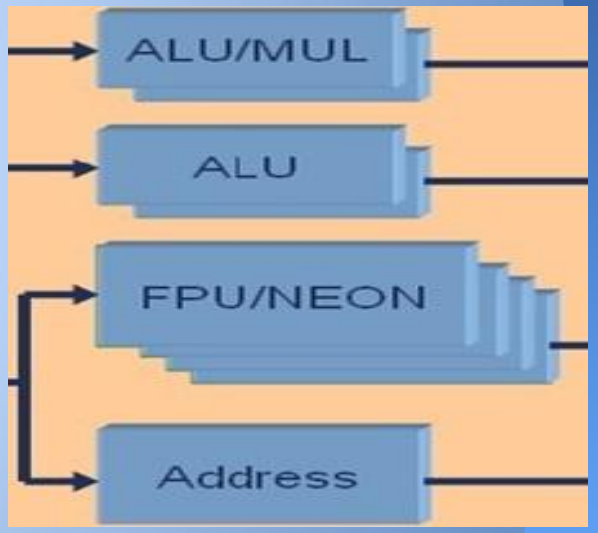
Microarchitecture: Issue



- Issue can fed max. of 2 instructions per cycle
- Can dispatch up to 4 instructions per cycle
- Out of order selection of instructions from the issue queue

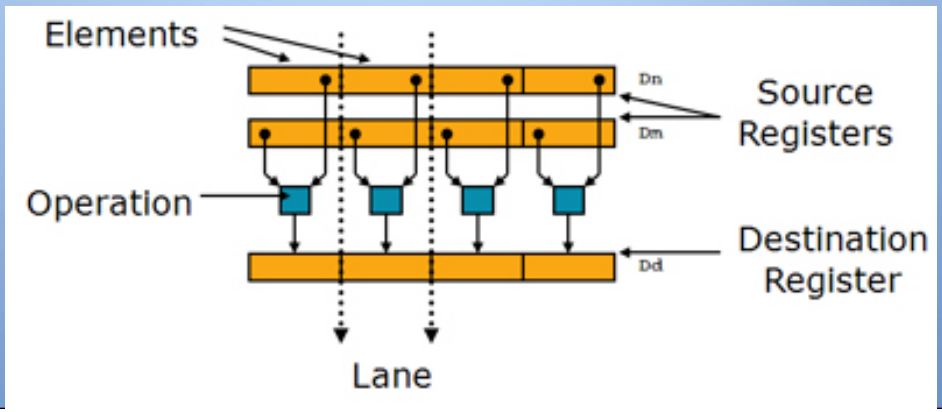
Microarchitecture: Execute

- Concurrent execution
- variable length of executing stage (1-3 cycles)
  - ADD R0, R1, R2 (1 cycle)
  - ADD R0, R1, R2 LSL #2 (2 cycle)
  - ADD R0, R1, R2 LSL R3 (3 cycle)
- Neon media and/or floating point processing engine



NEON Media Process Engine (MPE)

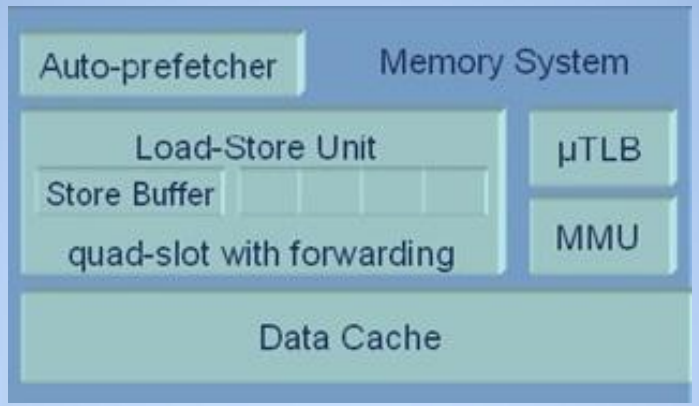
- 128-bit SIMD (single instruction multiple data)
- accelerate multimedia and signal processing algorithms
  - video, 2D/3D graphic, audio and speech processing
- has 32 registers (vectors of elements), 64-bits wide
- data type: signed/unsigned 8-bit, 32-bit, 64-bit, and single precision floating point



Floating Point Unit (FPU)

- High-performance single, and double precision floating point instructions
- Double the performance of previous ARM floating point units
- Capable significant enhancing solution with rich graphic, 3D, imaging and scientific computation

Microarchitecture: Memory



- Data forwarding
- 2-level TLB structure
  - Micro and main TLB
- Data prefetcher
  - monitor cache line requests by processor
  - supports 4 cache line fill requests

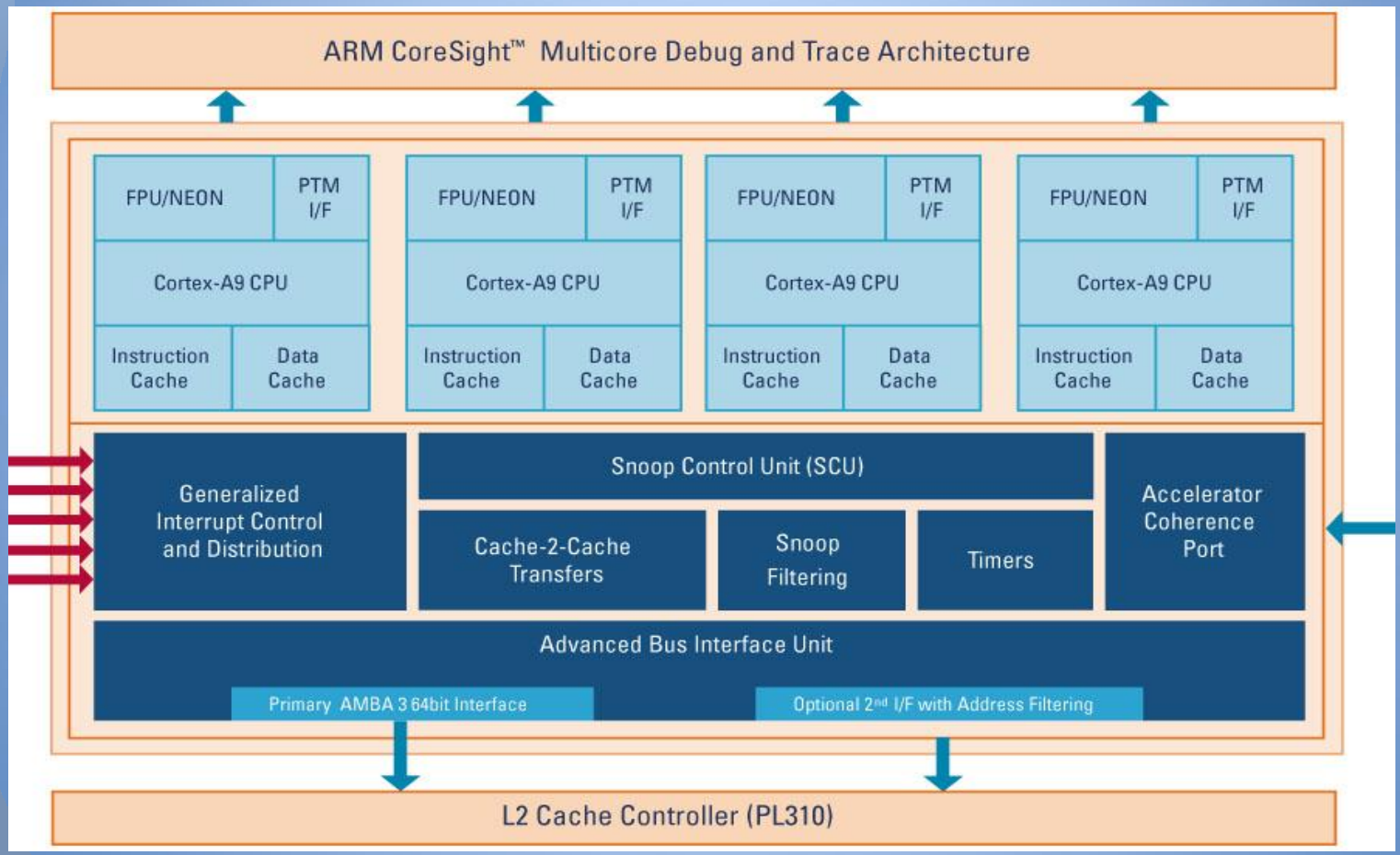
Memory Hierarchy

- L1 cache
  - split, non-unified
    - 32KB data and 32KB instruction
  - 4-way associative
- L2 cache
  - shared, unified
  - 128KB to 8MB
  - 4 to 16-way associative

Microarchitecture: Writeback

- Out of order write back of instructions

Cortex-A9 MultiCore Processor



Cortex-A9 Multicore Processor Configuration

Cortex-A9 MultiCore Processor

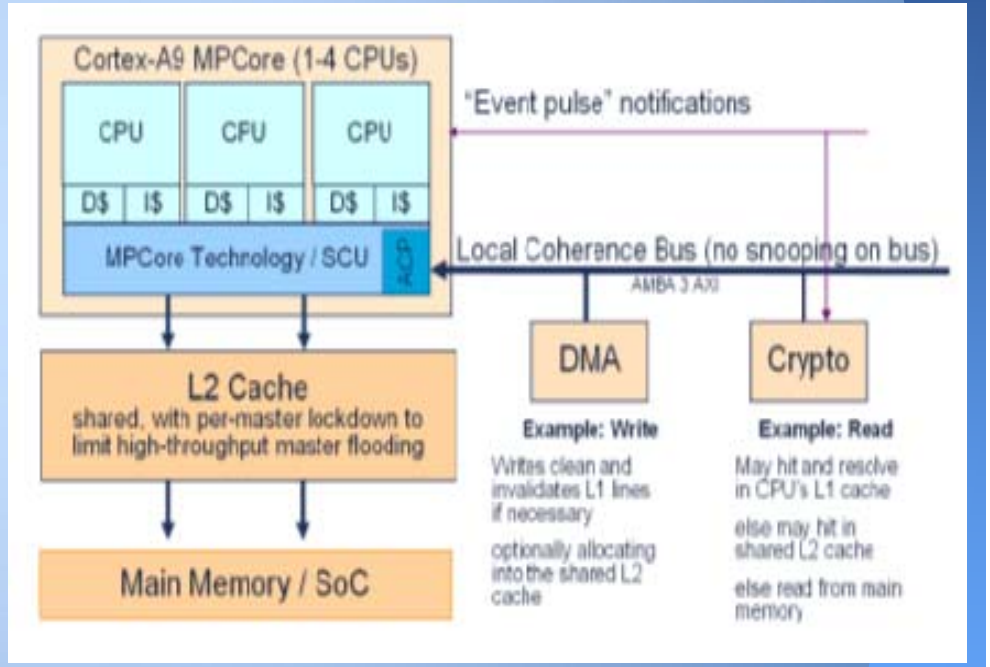
- support between 1-4 CPU in an integrated cache coherent manner
- cache size, FPU (float point unit), PTM (program flow trace macrocell), MPE (media processing engine) interfaces can be configured
- support either single or dual 64-bit AMBA 3 AXI interface

Cortex-A9 MPCore Technology: Snoop Control Unit (SCU)

- central intelligence
- responsible for managing:
  - interconnect
  - arbitration
  - communication
  - cache-2-cache
  - system memory transfer
  - cache data coherence

Cortex-A9 MPCore Technology: Accelerator Coherence Port

- 64-bit slave port
- supports all standard read and write transactions
- follow L1 write through and L2 write back policy



Cortex-A9 MPCore Technology: Generic Interrupt Controller

- supports up to 224 independent interrupts
- can interpret private (TrustZone) I/O interrupts and regular interrupts (OS layer)
- distributed across CPU and hardware prioritized

Cortex-A9 MPCore Technology: Advanced Bus Interface Unit

- enhance the interface between processor and system
- capable of exceeding 12GB/s into the system interconnect
- offer different CPU to bus frequency ratios
- support advance power management

Advanced L2 Cache Controller

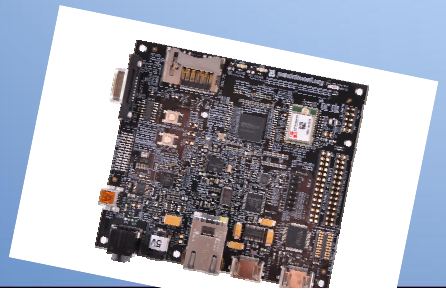
- Used to help utilized the the performance and throughput of the processor
  - disabled by default
- Serves as a monitor for memory accesses to the L2 cache between CPUs
- supporting up to 8MB, with between 4 and 16-way associative L2 cache

Apple A5

- IPhone 4s, IPad2, IPad mini
- consists of a dual-core ARM Cortex-A9 MPCore CPU
- Max. CPU clock rate
  - 0.8GHz for IPhone 4s
  - 1GHz for IPad2, mini\
- L1 cache: 32 KB instruction + 32 KB data
- L2 cache: 1 MB

OMAP4

- Motorola Razr, kindle Fire, PandaBoard
- version 4430, 4460, and 4470
  - 4470 has increased power efficiency up to 50-90%
- CPU frequency 1 to 1.5 GHz
- MIT Project: Ubuntu mini-cluster of 48 PandaBoards operating a 200W



PlayStation Vita SoC

- 4 Cortex-A9 processors
- Graphics: Quad-core PowerVR SGX543MP4+
- 2 GHz CPU clock rate
- Power: 2200 mAh, 3-5 hours
- 2.2 million units sold

Exynos 4

- Samsung Galaxy S III, Galaxy Note
- Quad-core ARM Cortex A-9
- CPU: 1.4-1.6 GHz
- over 10 million note sold
- over 50 million of S III sold

References

- http://www.arm.com/products/processors/cortex-a/cortex-a9.php
- http://www.arm.com/files/pdf/ARMCortexA-9Processors.pdf
- http://www.arm.com/products/processors/technologies/neon.php
- http://www.arm.com/products/processors/technologies/vector-floating-point.php
- http://en.wikipedia.org/wiki/ARM_Cortex-A9_MPCore
- http://en.wikipedia.org/wiki/Apple_A5
- http://en.wikipedia.org/wiki/Exynos
- http://en.wikipedia.org/wiki/Texas_Instruments_OMAP#OMAP_4
- http://en.wikipedia.org/wiki/PlayStation_Vita
- http://www.phoronix.com/scan.php?page=article&item=mit_cluster_build&num=1