TSMC 90nm CLN90G Process HVT 1.0-Volt Advantage^{TM} v1.0 Standard Cell Library Databook

ARM®

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Preface

Revision History

This document contains the release history for the TSMC 90nm CLN90G Process HVT 1.0-Volt Advantage^{TM} v1.0 Standard Cell Library Databook.

Part Number	Release Number	Date of Release	Updates
DB-Advantage-TSM075-1.0/90@1.0-1.0	1.0	May 2006	Initial Release

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Introduction

ARM's Artisan Physical IP Advantage^{TM} standard cell library builds upon the SAGE architecture, producing the optimum combination of high-density with high-performance. The cell line-up is derived from extensive customer design, synthesis, and place-and-route benchmark analysis. Library optimization is achieved by carefully matching the library functions and drive strengths to leading synthesis and place-and-route tools, producing superior RTL-to-GDSII results.

How This Book Is Organized

This introduction is organized into three sections:

- *Global Parameters* provides an overview of parameters specific to your Advantage library.
- *Special Cells* details the types of special cells included in the library.
- *Reading the Datasheet* describes the components of each datasheet.

Datasheets for each cell in this library are provided after the introduction. The datasheets are included in alphabetical order.

Global Parameters

This section specifies global parameters for the TSMC 90nm CLN90G Process HVT Advantage v1.0 Standard Cell Library. Some of the following sections may be covered: physical specifications, electrical specifications, derating factors, propagation delay calculation, timing constraints, power calculation, and power-rail strapping.

Physical Specifications

Table 1 shows the physical design specifications of this library.

Table 1. Physical Specifications

Drawn Gate Length (um)	0.1
Layers of Metal	4, 5, 6, 7, 8 and 9
Layout Grid (um)	0.005
Vertical Pin Grid (um)	0.28
Horizontal Pin Grid (um)	0.28
Cell Power and Ground Rail Width (um)	0.42
Cell Height (um)	2.52

In the Advantage library, all pins are located on the vertical and horizontal pin grids. Most place-and-route tools work more efficiently with all pins on grids, and some tools even require it.

The Advantage library also supports designs with four, five, six, seven, eight or nine layers of metal. You may need to change the design rules in the technology file, because the top-level metal has a greater minimum width and greater minimum spacing requirement. See "TSMC 90nm CMOS Logic Design Rule (G/GT/LP)" design rule manual. You must define these rules correctly for the place-and-route tool.

Table 2 describes the electrical specifications for this library.

Table 2. Electrical Specifications

Parameter	Minimum	Typical	Maximum
DC Supply Voltage (Vdd)	0.9V	1.0V	1.1V
Junction Temperature	-40°C	25°C	125°C

Table 3 shows the derating factors for this library.

Table 3. Derating Factors

$K_{Process}$ (slow)	1.314
$K_{Process}$ (typical)	1.000 (by definition)
$K_{Process}$ (fast)	0.746
K_{Volt} (1.0V to 0.9V)	-2.497/V
K_{Volt} (1.0V to 1.1V)	-1.555/V
K_{Temp} (25°C to -40°C)	0.00060/°C
K_{Temp} (25°C to 125°C)	0.00051/°C

Propagation Delay and Transition Time

The propagation delay through a cell is the sum of the intrinsic delay, the load-dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing 50% of Vdd and the output crossing 50% of Vdd. Figure 1 illustrates the propagation delay.

Figure 1. Propagation Delay
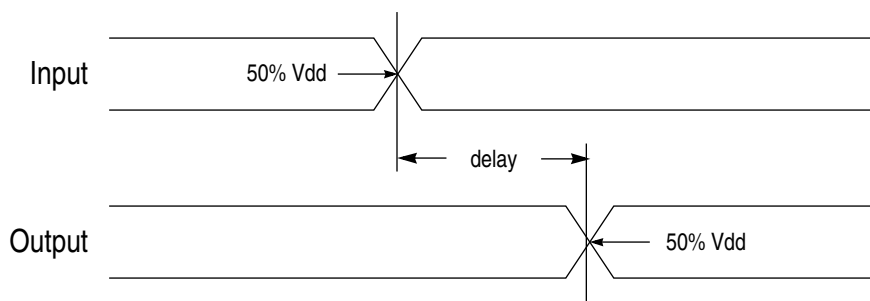
The transition times (slews) on input and output pins are defined as the time interval between the signal crossing 10% of Vdd and 90% of Vdd. Figure 2 illustrates transition time measurements for rising and falling signals.

Figure 2. Transition Time
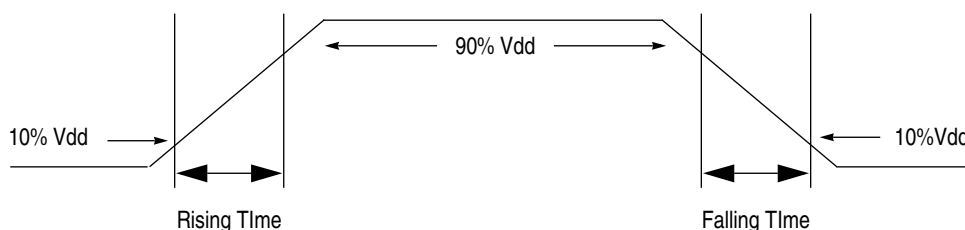
Factors that affect propagation delays and transition time include: temperature, supply voltage, process variations, fanout loading, interconnect loading, input-transition time, input-signal polarity, and timing constraints. The timing models provided with this library include the effects of input-transition time on propagation delays. Also, all timing models use a table lookup method to calculate accurate timing. To simplify calculations, the standard cell datasheets provide all timing numbers for an input slew of 0.018ns and a linearized load factor, K_{load}, which is not as accurate as the timing models. All cells have been characterized with a fully populated metal2 (0.28um horizontal pitch) and metal3 (0.28um vertical pitch) routing grid across the entire cell layout.

The Advantage library may contain negative propagation delays. Although most third-party verification tools can handle negative propagation delays, some tools will turn negative delays into a zero value.

Derating Factors

Derating factors are coefficients that the typical process characterization data is multiplied by to arrive at timing data that reflects appropriate operating conditions. The deratings table provides derating factors for variations in process case, temperature, and voltage.

Derating factors are derived by averaging the performance of many different cells in the library. A particular combination of cells may perform better or worse than indicated by these derating factors.

Delay Calculation

Using the delay data in the datasheets ($t_{intrinsic}$, K_{load}, and C_{load}) and the delay derating factors, the estimated total propagation delay is calculated as such:

$$t_{TPD} = (K_{Process}) * [1 + (K_{Volt} * \Delta Vdd)] * [1 + (K_{Temp} * \Delta T)] * t_{typical}$$

$$t_{typical} = t_{intrinsic} + (K_{load} * C_{load})$$

where:

t_{TPD} = total propagation delay (ns);

$t_{typical}$ = delay at typical corner-1.0V, 25°C, typical process (ns);

$t_{intrinsic}$ = delay through the cell when there is no output load (ns);

K_{load} = load delay multiplier (ns/pF);

C_{load} = total output load capacitance (pF);

$K_{Process}$ = process derating factor, where process is slow, typical, or fast;

K_{Volt} = voltage derating factor (/V);

$\Delta Vdd = Vdd - 1.0V;$

K_{Temp} = temperature derating factor (/°C);

ΔT = junction temperature - 25°C.

Timing Constraints

Timing constraints define minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing constraints include: setup time, hold time, recovery time, and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time and data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for 0.018ns data slew and 0.018ns clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process case variations. All cells have been characterized with a fully populated metal2 (0.28um horizontal pitch) and metal3 (0.28um vertical pitch) routing grid across the entire cell layout.

Timing constraints can affect propagation delays. The intrinsic delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, and pulse widths). The use of shorter timing constraint intervals may increase delay. Each cell is considered functional as long as the actual delay does not exceed the delay given in the datasheets by more than 10%.

Setup Time

The setup time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%. Setup-constraint values are measured as the interval between the data signal crossing 50% of Vdd for rising data (or 50% of Vdd for falling data) and the clock signal crossing 50% of Vdd for rising clocks (or 50% of Vdd for falling clocks). For the measurement of setup time, the data input signal is kept stable after the active clock edge for an infinite hold time. Figure 3 illustrates setup time for a positive-edge-triggered sequential cell.

Figure 3. Setup Time
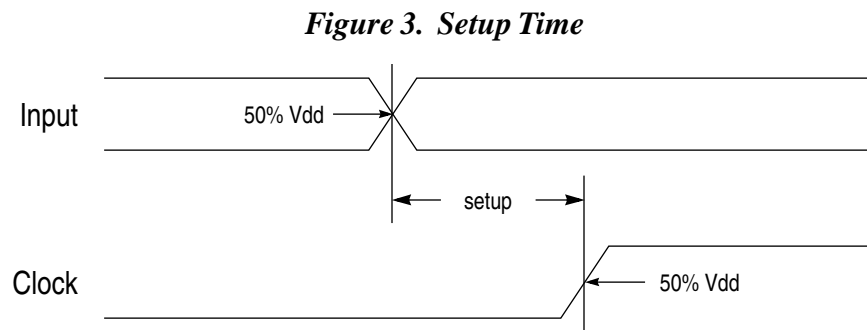
Hold Time

The hold time for a sequential cell is the minimum length of time the data-input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%. Hold-constraint values are measured as the interval between the data signal crossing 50% of Vdd for rising data (or 50% of Vdd for falling data) and the clock signal crossing 50% of Vdd for rising clocks (or 50% of Vdd for falling clocks). For the measurement of hold time, the data input signal is held stable before the active clock edge for an infinite setup time. Figure 4 illustrates hold time for a positive-edge-triggered sequential cell.

NOTE: ARM does not incorporate any hold time margins in the Synopsys, TLF, StarDC, or any other timing models. Chip designers should develop a timing methodology to account for chip-level timing inaccuracies inherent to extraction and timing analysis tools.

Figure 4. Hold Time
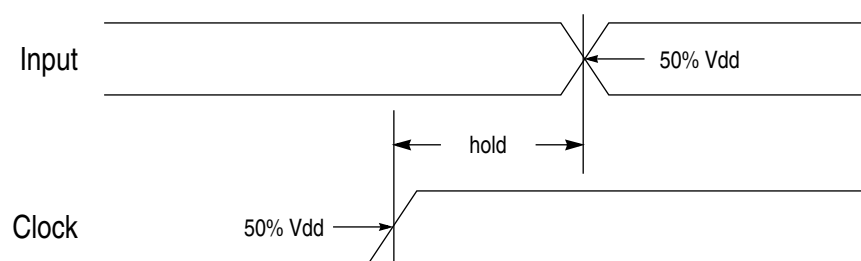
Recovery Time

Recovery time for sequential cells is the minimum length of time that the active-low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd for rising clocks (or 50% of Vdd for falling clocks). For the measurement of recovery time, the set or reset signal is held stable after the active clock edge for an infinite hold time. Figure 5 illustrates recovery time.

Figure 5. Recovery Time
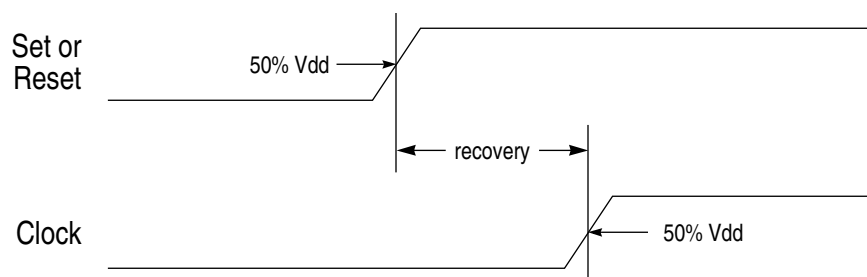
Removal Time

Removal time for sequential cells is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the active clock edge does not latch in a new data value from that programmed by the asynchronous set or reset signal. Removal constraint values are measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd for rising clocks (or 50% of Vdd for falling clocks). For the measurement of removal time, the set or reset signal is held stable before the active clock edge for an infinite setup time. Figure 6 illustrates removal time.

Figure 6. Removal Time
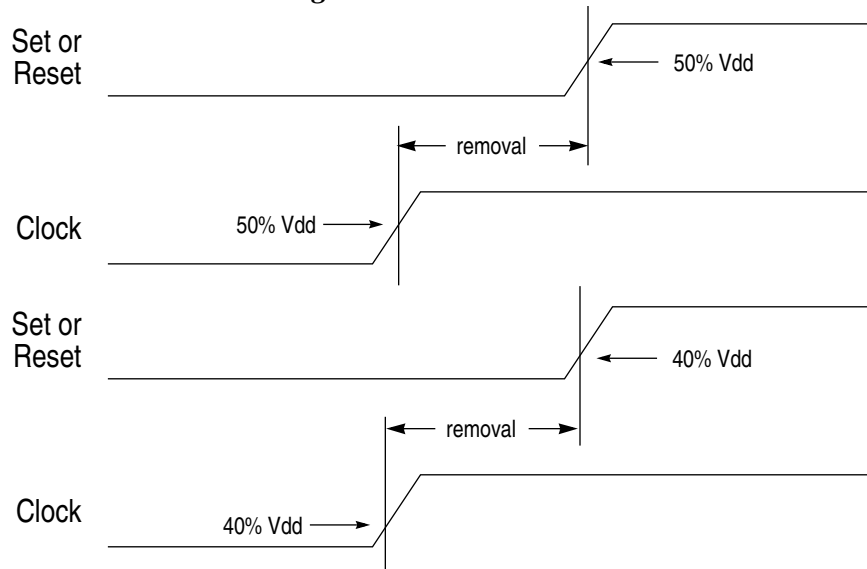
Minimum Pulse Width

Minimum pulse width is the minimum length of time between the leading and trailing edges of a pulse waveform. Minimum pulse width high (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of Vdd and the falling edge of the signal crossing 50% of Vdd. Minimum pulse width low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of Vdd and the rising edge of the signal crossing 50% of Vdd. Figure 7 illustrates minimum pulse width.

Figure 7. Minimum Pulse Width
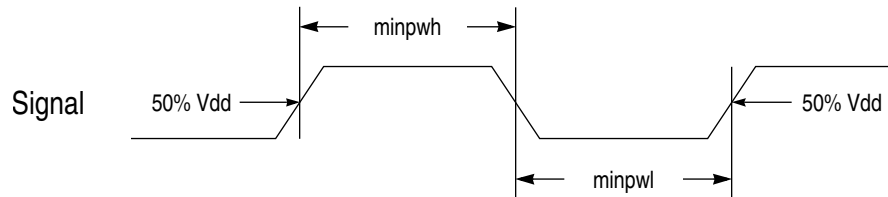
Minimum pulse width is defined as 0.83325ns for all set/reset pins (SN, RN) and 0.83325ns for all clock pins (G, GN, CK, CKN). These are the largest minimum pulse widths measured from all the cells in the library. An input pulse of shorter duration will produce unpredictable results.

Electromigration

min_period Property

All sequential cells in the .lib file have this clock pin property set:

min_period : 1.000000;

This property has the effect of limiting a design's clock frequency to 1.0GHz. Commonly used design flows may not be able to support the required accuracy for designs targeted for clock frequencies higher than this limit. Contact ARM technical support for designs targeting higher clock frequencies.

Electromigration Guideline Compliance

Artisan standard cell libraries are designed to meet foundry electromigration guidelines for normal chip design usage; however, it is the chip designer's responsibility to ensure that electromigration guidelines are met at the chip level with regard to foundry guidelines as well as ARM's guidelines for how the library will be used. The following three Electromigration guidelines must be met in order to ensure safe use of the standard cell library within the electromigration guidelines of the foundry.

1. The width of the Metal1 VDD and VSS power buses in the standard cells has been sized to provide adequate current to the cells. Vertical power straps must be placed with sufficient frequency to provide adequate current distribution to the standard cell power buses. For more details, see the section entitled Power-Rail Strapping in the standard cell user guide.

2. The output pin metal for each standard cell has been sized to accommodate multiple vias necessary (for worst case electromigration conditions) to meet via electromigration guidelines, although oversized Metal1 output pins do not necessarily require multiple vias. The number of vias required to meet electromigration guidelines is design dependent, and the chip designer must use an appropriate number of vias and wire width when routing from an output pin.

3. The internal layouts of the standard cells have been designed and verified to comply with the manufacturer's electromigration guidelines under normal usage. Normal usage is defined as follows:

•   The current required by the cell does not exceed the maximum current that can be supplied by the Metal1 power buses.

- The output transition times (measured using 10% and 90% thresholds), for a cell outside the clock tree network, must be no greater than 20% of the total cycle time, or must be no greater than 10% of the cycle time for any of the output pins of that particular cell. Limiting the output transition time has the effect of limiting the load driven by the cell which will reduce the cell's current draw, making it comply with electromigration guidelines. Ratios larger than 20% are not appropriate for commonly used design flows and are unlikely to be encountered in normal designs.

- For a cell in the clock tree network, transition times must not exceed 10% of the total cycle time for that cell.

Power Dissipation

The Advantage library is designed to dissipate only AC power, except for the small reverse-bias leakage currents which are normally present in all CMOS circuits.

The power dissipation internal to a cell when a given input switches is primarily dependent upon the cell design itself. The power dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The Advantage library datasheets contain both an AC power table which documents the internal energy consumption of each cell and a pin capacitance table which gives input-pin capacitance data used to compute output loading. This information, coupled with design-specific information, can be used to estimate the total power dissipation of a cell within a design.

The AC power tables specify the amount of energy consumed within a cell (uW/MHz) when the corresponding pin changes state at 25°C, 1.0V, and typical process. The energy data in the tables were measured for an input slew of 0.018ns and no loading at the outputs.

For combinatorial cells, energy values are provided for only input pins. The energy value for each input pin is the average of energies associated with the input transitions which result in an output transition.

For sequential cells, the energy associated with each input pin is the average energy of those input transitions which *do not* result in an output transition. The energy associated with the output pin of a sequential cell is the average energy of all cases where an output transition is the result of a clock-input transition, minus the energy associated with the clock input pin. In the event that a sequential cell has multiple outputs, all output energy data will be associated with only one output pin.

Power Calculation

Power dissipation is dependent upon the power-supply voltage, frequency of operation, internal capacitance, and output load. The power dissipated by each cell is:

$$P_{avg} = \sum_{n=1}^{x}(E_{in} * f_{in}) + \sum_{n=1}^{y}(C_{on} * Vdd^2 * \frac{1}{2}f_{on}) + E_{os} * f_{01}$$

where:

P_{avg} = average power (uW);

x = number of input pins;

E_{in} = energy associated with the nth input pin (uW/MHz);

f_{in} = frequency at which the nth input pin changes state during the normal operation of the design (MHz);

y = number of output pins;

C_{on} = external capacitive loading on the nth output pin, including the capacitance of each input pin connected to the output driver, plus the route wire capacitance, actual or estimated (pF);

Vdd = operating voltage = 1.0V;

f_{on} = frequency at which the nth output pin changes state during the normal operation of the design (MHz);

E_{os} = energy associated with the output pin for sequential cells only (uW/MHz).

The switching frequency of inputs and outputs of a particular cell in a design can be obtained from a gate-level logic simulator (e.g. Verilog) by applying typical input stimuli and measuring the activity on each node of interest. The total average power for the design can be computed by adding the average power for each cell.

EXAMPLE: Calculating Power for a DFFXL Cell

For this exercise, assume that a DFFXL cell has clock switching at 133MHz (clock frequency = 66.5MHz), input and output pins switching at 20MHz, and an external capacitive loading on the output pin of 0.02pF. Using the AC Power table provided in the **sample** DFF datasheet at the end of the introduction, the power dissipated by the DFFXL can be calculated by using the following equation:

$$P_{avg} = \sum_{n=1}^{x}(E_{in} * f_{in}) + \sum_{n=1}^{y}(C_{on} * Vdd^2 * \frac{1}{2}f_{on}) + E_{os} * f_{01}$$

Given:

$x = 2;$

$E_{i1} = 0.0056$ <uW/MHz;

$E_{i2} = 0.0063$ uW/MHz;

$f_{i1} = 20$ MHz;

$f_{i2} = 133$ MHz;

$y = 2$;

$C_{o1} = 0.02$ pF;

$C_{o2} = 0.02$ pF;

$Vdd = 1.0$V;

$f_{o1} = 20$ MHz;

$f_{o2} = 20$ MHz;

$E_{os} = 0.0060$ uW/MHz,

we have:

$$P_{avg} = \sum_{n=1}^{2}(E_{in} * f_{in}) + \sum_{n=1}^{2}(C_{on} * Vdd^2 * \frac{1}{2}f_{on}) + E_{os} * f_{01}$$

$$P_{avg} = (E_{i1} * f_{i1}) + (E_{i2} * f_{i2}) + (C_{o1} * VDD^2 * \frac{1}{2}f_{o1})$$

$$+ (C_{o2} * VDD^2 * \frac{1}{2}f_{o2}) + (E_{os} * f_{01})$$

$$P_{avg} = (0.0056 * 20) + (0.0063 * 133) + \left(0.02 * 1.0 * \frac{1}{2}(20)\right)$$

$$+ \left(0.02 * 1.0 * \frac{1}{2}(20)\right) + (0.0060 * 20)$$

$$P_{avg} = 1.46 \text{ uW}$$

Power-Rail Strapping

You must determine the required amount of vertical power-rail strapping to satisfy all requirements imposed by the design methodology for a given design. Power-rail strapping should be sized small enough to optimize standard cell height and maximize router efficiency, yet it must be large enough to provide sufficient power to the cells.

The guidelines below provide a rough estimate with many simplifying assumptions. For a given module design, you can estimate the amount of vertical power-rail strapping that is required to fulfill electromigration requirements.

Given:

I_{avg} = total average current for the module, calculated from previous section (mA);

w_{m1} = VSS/VDD metal1 wire width (um), see Physical Specifications;

r = number of rows in module;

d_{m1} = maximum metal1 current density allowed for the process (mA/um);

d_{m2} = maximum metal2 current density allowed for the process (mA/um);

I_{m1} = maximum current that can be supported by all horizontal metal1 wires (mA);

I_{strap} = total current that must be supported by the vertical metal2 strapping (mA);

w_{m2} = metal2 wire width required for vertical strapping (um);

c = minimum number of metal2 straps;

we have:

$$I_{m1} = w_{m1} * r * 2 * d_{m1},$$

where multiplying by 2 assumes metal1 wires are supplied from both ends;

$$I_{strap} = \frac{(I_{avg} - I_{m1})}{2},$$

where dividing by 2 assumes the metal2 vertical strap wires are supplied from both ends;

$$w_{m2} = \frac{I_{strap}}{d_{m2}},$$

It is recommended that the metal2 wire width, w_{m2}, be divided into c equal portions which are spaced equidistant across the module, where

$$c = \frac{I_{avg}}{I_{m1}},$$ rounded up to the next integer.

The same consideration must be given to the number of vias used to connect the metal1 and metal2 straps.

Adding Routing Channels

In the Advantage library, each cell is designed with a uniform cell height of 2.52um (i.e., 9 tracks tall with 0.28um per track). The cell layouts allow neighboring rows of cells to share common power or ground rails when cells abut each other at the top and bottom edges of the cell bounding box. The sea-of-cells layout with no channels between rows will usually yield the minimum area. In case of extremely congested areas, you may want to separate some rows of cells to increase the number of routing channels within a particular layout region. Because geometries must overlap cell boundaries, a particular spacing between the rows may result in DRC violations for layer spacing. It is recommended that you do not use spacings that cause DRC violations. If these spacings must be used, the DRC violations must be fixed manually by filling the void between the rows with the appropriate layer(s).

Table 4 indicates which DRC violations to expect and how to correct them for a separation between rows of cells.

Table 4. Correcting DRC Violations

Row Separation in Number of Grids	Expected DRC Violations	Action to Correct DRC Violations
0 (Rows Abut)	None	None
1	NP/PP space < 0.24um	Draw NP/PP layer between rows to merge implant regions above and below row separation
2	NWELL space < 0.62 depending on the well bias up to 1.2um M1 space < 0.12 depending on the width of Metal1 up to 1.5um	Draw NWELL layer between rows to merge NWELL regions above and below row separation Draw Metal1 layer between rows to merge Metal1 regions above and below row separation
3	NWELL space < 0.62 depending on the well bias up to 1.2um	Draw NWELL layer between rows to merge NWELL regions above and below row separation
4	None	None
5 or more	None	None

Special Cells

This section discusses special cells in the Advantage library.

Antenna-Fix Cell

The library contains an antenna-fix cell which must be inserted manually. However, most place and route tools will indicate which nets require the antenna-fix cell. The TSMC antenna effect prevention guideline, "TSMC 90nm CMOS Logic Design Rule", specifies a maximum wire length. During place and route, the router may connect wires to the input gates of cells that are longer than the maximum length allowable by the guideline. The antenna cell can be used in this case to add an optional diode on the net close to the input gates which do not meet the guideline. Pin A on the antenna cell connects to a diode, reverse biased to ground. A diode can be added to either P or N.

Delay Cells

The library contains delay cells that have the same width. These delay cells allow you to adjust a given delay path with a simple cell substitution after place and route.

FILL Cells

The library contains several FILL cells: FILL1, FILL2, FILL4, FILL8, FILL16, FILL32, FILL64. The number appended to FILL in the cell name denotes the width of the cell in tracks.

During place and route, the FILL cells are used to connect power and ground rails across an area containing no cells. The FILL cells are also used to ensure gaps do not occur between well or implant layers which could cause design rule violations. Using wider cells where appropriate reduces the size of the layout database.

FILLCAP Cells

FILLCAPs function as FILL cells. Inside the FILLCAP, PMOS and NMOS devices form decoupling capacitors between the VDD and VSS rails, reducing ground bounce in the power grids. Figure 8 illustrates the FILLCAP functional schematic.

Figure 8. FILLCAP Functional Schematic
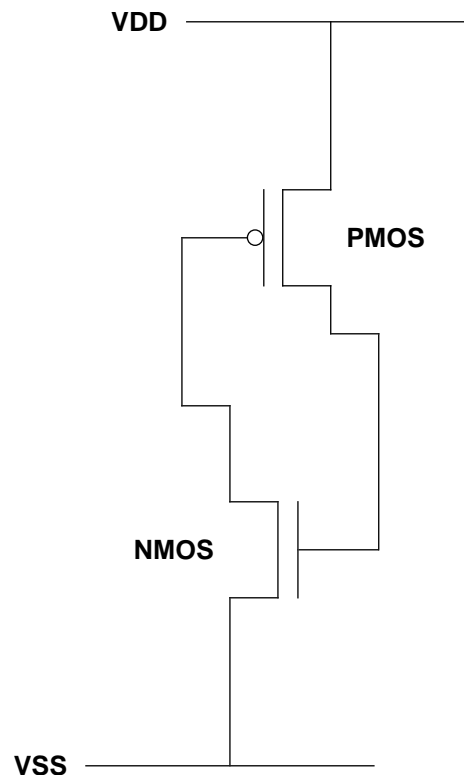
Low-Power (XL) Cells

The library contains a wide variety of cells, denoted by an "XL" suffix in the cell name, that are designed specifically for low-power applications. Input capacitance for the XL cells is much lower than that for corresponding X1 (1x drive strength) cells. Because XL cells have been designed for the sole purpose of reducing power consumption, output rise and fall times for these cells may not be equal, and due to the low-drive capability of the XL cells, these cells are not intended for use in critical timing paths, or to drive heavily loaded nets.

NWELL and Substrate Tie Cell

The library does not have well or substrate ties inside the cells. You are required to tie the NWELLS to Vdd and the substrate to Vss before place-and-route using the FILLTIE cell. Before place-and-route, pre-place the FILLTIE cell periodically in every placement row. You must place the FILLTIE cell as frequently as the design requires.

For example, if the design rules require a well or substrate connection every 20um, then the FILLTIE cell must be pre-placed every 20um. See Figure 9.

Figure 9. Sample Placement of FILLTIE Cells for 20um NWELL and Substrate Tie Design Rule
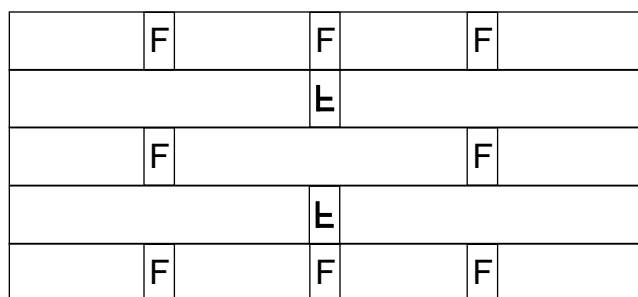
Note: The letter "F" indicates a FILLTIE cell placed in normal orientation, and the letter "F" flipped upside down indicates a FILLTIE cell placed in MY orientation.

In all rows except for the top and bottom rows, the NWELL and substrate are shared by two adjacent placement rows. This allows you to place the FILLTIE cell only half as frequently as the design rules require. But don't forget to stagger the placement in the adjacent rows by an amount equal to the design row.

Assuming that the rule is every 20um, you will need to place FILLTIE cells every 20um in the top and bottom rows. If you stagger the placement by 20um between adjacent rows, you can place FILLTIE cells every 40um for all rows between the top and bottom rows. This method will allow every row to have well and substrate ties every 20um.

Register File Cells

Register file cells (RF*) are provided to support creating very small memories from standard cells. The register file bit cells (RF1R1W, RF2R1W) have tri-state outputs. Users must tie these tri-state outputs together on a bit line and have this bit line drive function as an output buffer. The library contains a number of inverting and non-inverting buffers (INV*, BUF*, TRI*) that can buffer the bit lines.

It is possible to make a memory that has a non-power-of-two word depth. If this is employed, it is possible to input an address to the memory such that none of the bit cells are addressed and nothing is driving the bit line. A floating bit line can cause the logic following it to go into a high power state, therefore, users must take special care when designing a memory with a non-power-of-two word depth. Users must guarantee that the bit line is never allowed to float by ensuring that at least one bit cell is always driving the bit line, or that a floating bit line does not cause subsequent logic to go into a high power state. One way to achieve the latter is to use an output buffer with an enable. NAND or AND gates or tri-state output buffers (NAND*, AND*, TRI*) can be used for this purpose. Whichever is used, be sure to generate an enable signal that only enables the output buffer when the bit line is not floating.

Figure 10 shows a sample circuit for generating an enable signal when the bit line is not floating in a register file of up to 64 words.

Figure 10. Enable Signal Circuit Example
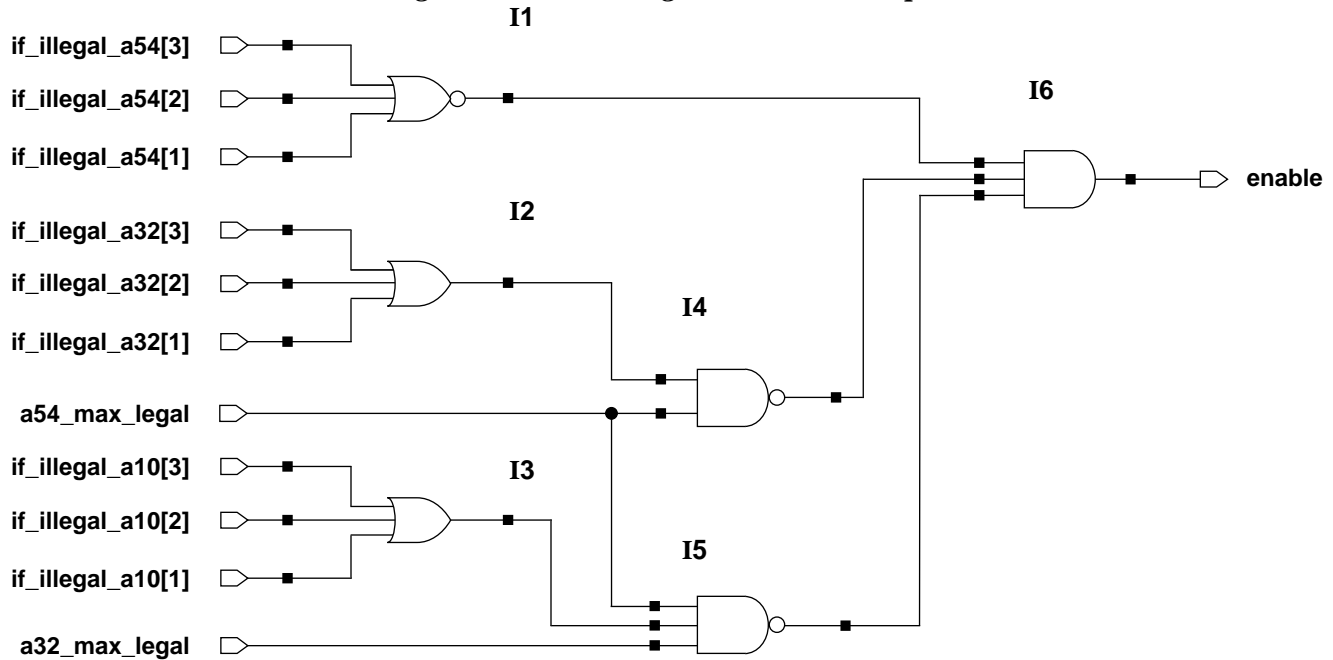
The circuit in Figure 10 assumes the address lines are pre-decoded in pairs. The circuit is a comparator. Program it with the number of words in the memory. The circuit compares the address input of the memory to the pre-programmed number of words. When the address is less than or equal to the size of the memory, it generates an enable signal for the output buffers. When the address input is higher than the number of words in the memory, the output of the comparator is false and the outputs are disabled, which prevents them from going into a high power state.

To program the example comparator, connect predecoded address lines to gates I1, I2 and I3 if the address should be larger than the size of the memory when those signals are active, and more significant address bits have not resolved the comparison. If, when those signals are active, the address should not be larger than the size of the memory, either ground that pin or reduce the number of inputs to the gate. To enable the comparison of lower address bits, connect to gates I4 and I5 signals that signify that the higher address bits have not been able to resolve the comparison. To I4, connect the signal that is true when the most significant two address bits are exactly equal to what they are in the highest address that exists in the memory. To I5, connect the signals that are true when the most significant for bits are exactly equal to what they are in the highest address that exists in the memory.

Figure 11 shows an example for a memory that has 21 words.

Figure 11. 21-Word Memory Example
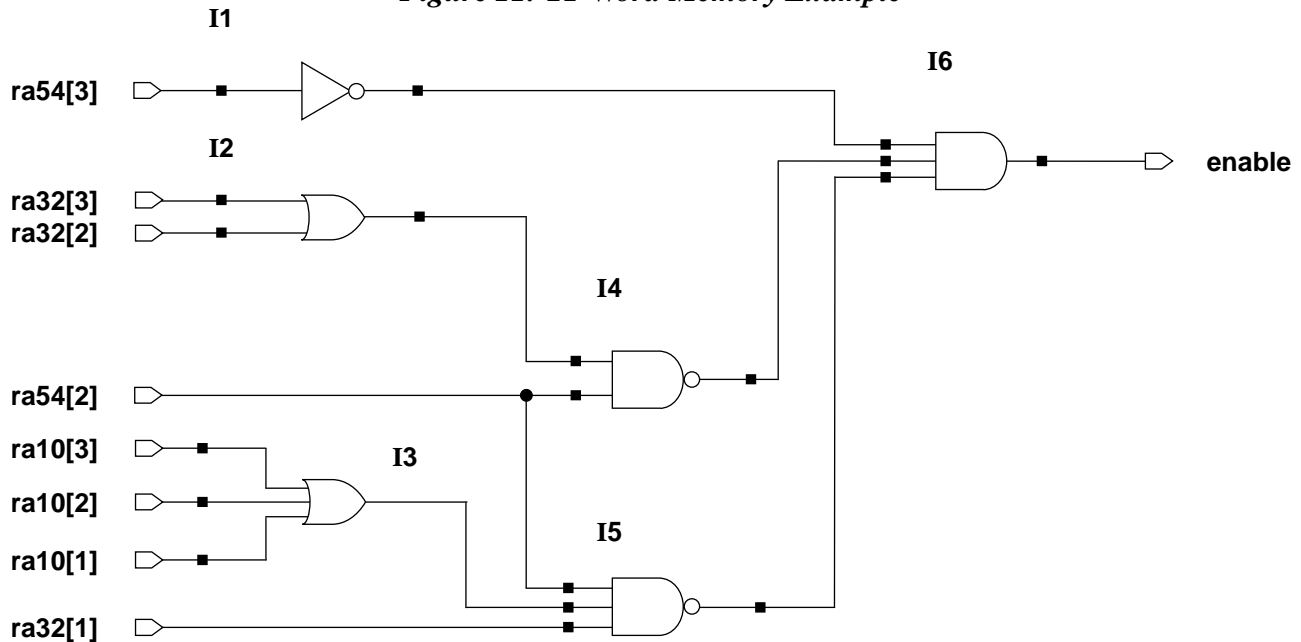
In binary mode, the highest address that exists in the memory is 100100. The read address RA[5:0] is pre-decoded into RA54[3:0] which are the four possible combinations of the two most significant address bits. RA32[3:0] is the four possible combinations of address bits 3 and 2. RA10[3:0] is the four possible combinations of address bits 1 and 0. If RA54[3] is true, we are accessing address 11XXXX in the memory. This address does not exist, so the comparison does not need to continue to the remaining address bits. Gate I1 needs only RA54[3] as an input because this is the only combination of these 2 address bits which is never in the memory. We connect RA54[2] to gate I4 because if this signal is true we don't know if the address exists and we have to continue the comparison to the next pair of addresses. To gate I2 we connect RA32[3] and RA32[2] because if RA54[2] is true and either of RA32[3] or RA32[2] are true, the address doesn't exist and we are done. If RA54[2] and RA32[1] are true, we are addressing word 1001XX which might be in the memory so we connect these two signals to I5 and check RA10. We connect RA10[3], RA10[2] and RA10[1] to I3 because of the memory addresses 1001XX, only 100100 exists in the memory. I6 generates the enable signal based on the results of all of the comparisons.

TIEHI/LO Cells

The library contains a TIEHI cell and a TIELO cell. The outputs of the TIEHI and TIELO cells are driven through diffusion to provide isolation from the power and ground rails for better ESD protection. The standard cell abstract methodology assumes that the TIEHI and TIELO cells are used to tie off any inputs to power and ground. If these cells are not used and the router is allowed to drop vias on the power rail, DRC errors or shorts may result.

Advantage Naming Convention

Reading the Datasheet

Please refer to the **sample** datasheet for DFF at the end of the introduction for the arrangement of each of the following datasheet sections. Datasheet titles reference standard Artisan cell names. Cell names for your specific library are reflected in the cell size table on each datasheet.

NOTE: This datasheet contains **sample** characterization values.

1. Base Cell Name

The cell name field contains the cell name. The datasheets are presented alphabetically by cell name. The cell name presented here is the base cell name. The Cell Size table displays cell names for your specific library.

2. Cell Description

The cell description gives the function of the cell. When applicable, the equation(s) for the output pins are provided.

3. Functions

The function table gives all possible combinations of input and output signals for the cell. Table 5 defines the symbols used in datasheet function tables.

Table 5. Functions Key

Symbol	Description
0	Logic Low
1	Logic High
⌐‿	High to Low Transition
‿⌐	Low to High Transition
X	Don't Care
IL	Illegal/Undefined
Z	High Impedance

4. Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

5. Cell Size

This cell size table gives the height and width (μm) for each drive strength of the cell.

6. Functional Schematic

The functional schematic provides a functional representation of the cell.

7. Drive Strength

The drive strength of each cell is indicated by an "X" followed by the unit strength.

8. AC Power

The AC power table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state. The energy data for each drive strength of the cell in the **sample** DFF datasheet are calculated at 25°C, 1.0V, typical process, input slew of 0.018ns, and no external load at the output pins.

9. Delay

The delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF). The delays and load multiplier for each drive strength of the cell in the sample DFF datasheet are calculated at 25°C, 1.0V, typical process, and input slew of 0.018ns.

10. Timing Constraints

The timing constraints table in the **sample** DFF datasheet shows the timing conditions (ns) required at 25°C, 1.0V, and typical process to maintain proper functionality. Setup constraint values are measured for 0.018ns data slew and 0.018ns clock slew. Hold constraint values are measured for 0.018ns data slew and 0.018ns clock slew. Minimum pulse width is defined to be 0.83325ns for all set/reset pins and 0.83325ns for all clock pins. These are the largest minimum pulse widths measured from all the cells in the library.

11. Pin Capacitance

The pin capacitance table shows the typical loading at the input pins of the cell (pF) for each drive strength of the cell.

▼ *This datasheet contains sample characterization values.* ▼

① DFF

Process Technology:
CustomerName & Code

Cell Description

The DFF cell is a positive-edge triggered, static D-type flip-flop.

②

Logic Symbol

④

D — Q
CK — QN

⑤

Function Table

③
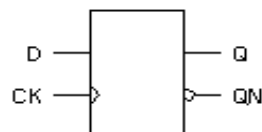
D	CK	Q[n+1]	QN[n+1]
0	⤴	0	1
1	⤴	1	0
×	⤵	Q[n]	QN[n]

Cell Size

Drive Strength	Height (μm)	Width (μm)
DFFXL	1.000	1.000
DFFX1	2.000	2.000
DFFX2	3.000	3.000
DFFX4	4.000	4.000
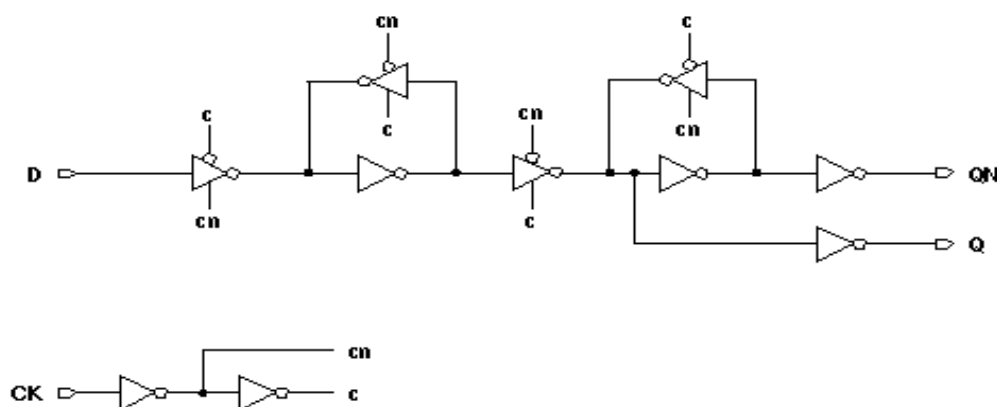
⑦

⑥

Functional Schematic

▼ *This datasheet contains sample characterization values.* ▼

Process Technology:
CustomerName & Code

DFF

AC Power

⑧

⑦

Pin	Power (μW/MHz)			
	XL	X1	X2	X4
D	1.000	1.000	1.000	1.000
CK	2.000	2.000	2.000	2.000
Q	3.000	3.000	3.000	3.000

Pin Capacitance

⑪

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	1.000	1.000	1.000	1.000
CK	2.000	2.000	2.000	2.000

Delays at TypTemp°C, TypVoltV, Typical Process

⑨

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	1.000	1.000	1.000	1.000	1.000	1.000	1.000	1.000
CK → Q↓	2.000	2.000	2.000	2.000	2.000	2.000	2.000	2.000
CK → QN↑	3.000	3.000	3.000	3.000	3.000	3.000	3.000	3.000
CK → QN↓	4.000	4.000	4.000	4.000	4.000	4.000	4.000	4.000

Timing Constraints at TypTemp°C, TypVoltV, Typical Process

⑩

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	1.000	1.000	1.000	1.000
	setup↓ → CK	2.000	2.000	2.000	2.000
	hold↑ → CK	3.000	3.000	3.000	3.000
	hold↓ → CK	4.000	4.000	4.000	4.000
CK	minpwh	5.000	5.000	5.000	5.000
	minpwh	6.000	6.000	6.000	6.000

Cell Description

The ACCSHCIN cell provides a carry-select addercarry generation function with active-low carry inputs. The function produces the carryouts (CO0,CO1) of the operands (A,B) with active-low carry-ins (CI0N,CI1N). The outputs (CO0,CO1) are represented by the logic equations:

$$CO0 = (A \bullet B) + (A \bullet \overline{CI0N}) + (B \bullet CI0N)$$

$$CO1 = (A \bullet B) + (A \bullet \overline{CI1N}) + (B \bullet \overline{CI1N})$$

Logic Symbol

Function Table

A	B	CI0N	CI1N	CO0	CO1
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	1	1
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	0
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1
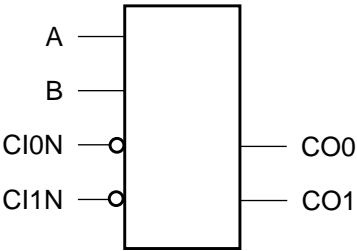
Cell Size

Drive Strength	Height (um)	Width (um)
ACCSHCINX2ADTH	2.52	9.52
ACCSHCINX4ADTH	2.52	9.52

Functional Schematic
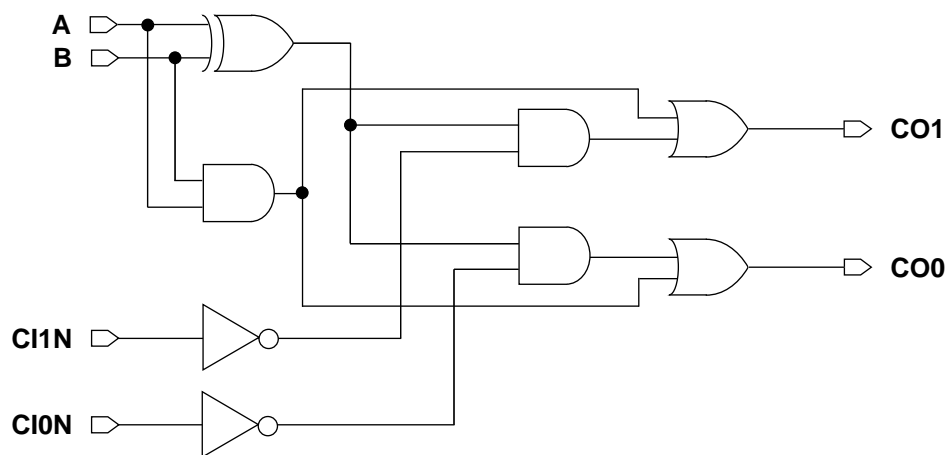
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
A	0.0238	0.0231
B	0.0198	0.0191
CI0N	0.0045	0.0044
CI1N	0.0057	0.0055

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
A	0.0025	0.0025
B	0.0060	0.0058
CI0N	0.0024	0.0025
CI1N	0.0026	0.0026

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
A	$\rightarrow$	CO0	$\uparrow$	0.1155	0.1224	5.1723	5.0824
A	$\rightarrow$	CO0	$\downarrow$	0.1500	0.1513	3.0933	3.0777
B	$\rightarrow$	CO0	$\uparrow$	0.0914	0.0934	4.9496	5.0032
B	$\rightarrow$	CO0	$\downarrow$	0.1001	0.1018	3.0637	3.0699
CI0N	$\rightarrow$	CO0	$\uparrow$	0.0353	0.0344	4.8189	4.9336
CI0N	$\rightarrow$	CO0	$\downarrow$	0.0241	0.0239	2.8406	2.8878
A	$\rightarrow$	CO1	$\uparrow$	0.1260	0.1310	5.0297	4.9895
A	$\rightarrow$	CO1	$\downarrow$	0.1524	0.1541	2.9860	2.9790
B	$\rightarrow$	CO1	$\uparrow$	0.0777	0.0826	4.9392	4.9573
B	$\rightarrow$	CO1	$\downarrow$	0.0984	0.1011	2.9589	2.9723
CI1N	$\rightarrow$	CO1	$\uparrow$	0.0428	0.0415	4.7649	4.8925
CI1N	$\rightarrow$	CO1	$\downarrow$	0.0291	0.0288	2.8914	2.9484

Cell Description

The ACCSHCON cell provides a carry-select addercarry generation function that produces active-low carryouts (CO0N,CO1N) of the operands (A,B) with carry-ins (CI0,CI1).The outputs (CO0N,CO1N) are represented by the logic equations:

$$CO0N = \overline{(A \bullet B) + (A \bullet CI0) + (B \bullet CI0)}$$

$$CO1N = \overline{(A \bullet B) + (A \bullet CI1) + (B \bullet CI1)}$$

Logic Symbol

Function Table

A	B	CI0	CI1	CO0N	CO1N
0	0	0	0	1	1
0	0	0	1	1	1
0	0	1	0	1	1
0	0	1	1	1	1
0	1	0	0	1	1
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	0
1	1	0	0	0	0
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	0	0
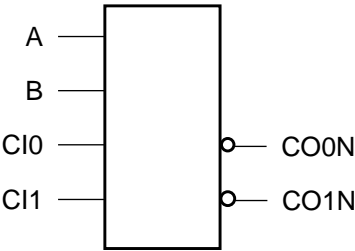
Cell Size

Drive Strength	Height (um)	Width (um)
ACCSHCONX2ADTH	2.52	8.68
ACCSHCONX4ADTH	2.52	10.36

Functional Schematic
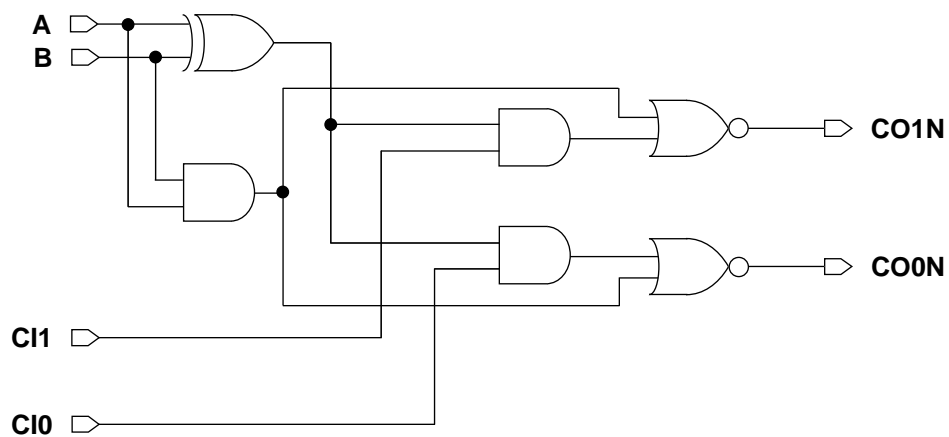
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
A	0.0226	0.0263
B	0.0210	0.0244
CI0	0.0049	0.0089
CI1	0.0059	0.0096

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
A	0.0052	0.0053
B	0.0077	0.0076
CI0	0.0027	0.0052
CI1	0.0027	0.0053

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
A	→	CO0N	↑	0.1463	0.1743	4.2786	4.2750
A	→	CO0N	↓	0.1444	0.1771	2.9220	2.7887
B	→	CO0N	↑	0.1167	0.1467	4.3119	4.2766
B	→	CO0N	↓	0.1175	0.1493	2.9271	2.7924
CI0	→	CO0N	↑	0.0350	0.0320	4.3899	2.1923
CI0	→	CO0N	↓	0.0234	0.0220	2.5847	1.3245
A	→	CO1N	↑	0.1471	0.1737	4.2281	4.1408
A	→	CO1N	↓	0.1417	0.1713	2.7629	2.6717
B	→	CO1N	↑	0.1185	0.1460	4.1740	4.1373
B	→	CO1N	↓	0.1139	0.1430	2.7626	2.6692
CI1	→	CO1N	↑	0.0421	0.0343	4.3865	2.2520
CI1	→	CO1N	↓	0.0285	0.0236	2.7012	1.3883

Cell Description

The ACCSIHCON cell provides a carry-select addercarry generation function for the first stage of a carry-select adder block (i.e., there are no carry-inputs). The function produces active-low carryouts (CO0N,CO1N) of the operands (A,B).The outputs (CO0N,CO1N) are represented by the logic equations:

$$CO0N = \overline{A \cdot B}$$
$$CO1N = \overline{A + B}$$

Logic Symbol
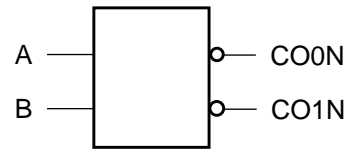
Function Table

A	B	CO0N	CO1N
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
ACCSIHCONX2ADTH	2.52	1.96
ACCSIHCONX4ADTH	2.52	3.36

Functional Schematic
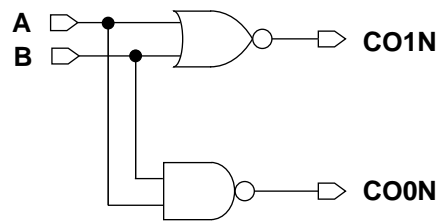
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
A	0.0045	0.0088
B	0.0052	0.0103

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
A	0.0043	0.0087
B	0.0049	0.0095

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
A	→	CO0N	↑	0.0197	0.0197	2.9711	1.4880
A	→	CO0N	↓	0.0186	0.0183	2.8704	1.4074
B	→	CO0N	↑	0.0168	0.0162	2.9018	1.5151
B	→	CO0N	↓	0.0167	0.0153	2.8723	1.4079
A	→	CO1N	↑	0.0266	0.0253	6.0853	3.1032
A	→	CO1N	↓	0.0116	0.0110	1.5745	0.7780
B	→	CO1N	↑	0.0319	0.0329	6.0771	3.1013
B	→	CO1N	↓	0.0128	0.0129	1.5531	0.7778

Cell Description

The ACHCIN cell is a full adder carry-generator that provides the arithmetic carryout (CO) of two operands (A,B) with active low carry-in (CIN). The output (CO) is represented by the logic equation:

$$CO = (A \bullet B) + (A \bullet \overline{CIN}) + (B \bullet \overline{CIN})$$

Logic Symbol
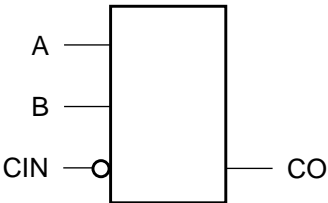
Function Table

A	B	CIN	CO
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
ACHCINX2ADTH	2.52	5.88
ACHCINX4ADTH	2.52	7.28

Functional Schematic
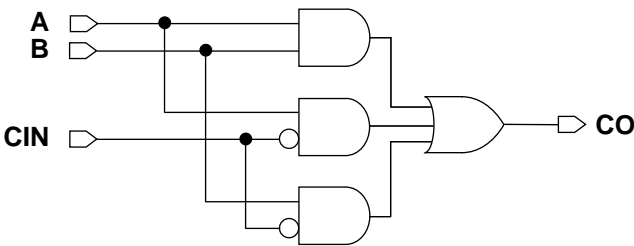
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
A	0.0156	0.0192
B	0.0171	0.0199
CIN	0.0052	0.0089

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
A	0.0027	0.0028
B	0.0061	0.0067
CIN	0.0028	0.0052

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
A	→	CO	↑	0.0943	0.1129	4.6142	4.4599
A	→	CO	↓	0.1114	0.1306	2.6909	2.5990
B	→	CO	↑	0.0801	0.0926	4.4183	4.3726
B	→	CO	↓	0.0910	0.0978	2.6367	2.5865
CIN	→	CO	↑	0.0364	0.0305	4.1850	2.1448
CIN	→	CO	↓	0.0263	0.0231	2.6092	1.3301

Cell Description

The ACHCON cell is a full adder carry-generator that provides the arithmetic activelow carry-out (CON) of two operands (A,B) with carryin (CI). The output (CON) is represented by the logic equation:

$$CON = \overline{(A \bullet B) + (A \bullet CI) + (B \bullet CI)}$$

Logic Symbol
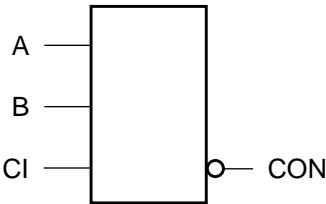
Function Table

A	B	CI	CON
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
ACHCONX2ADTH	2.52	5.88
ACHCONX4ADTH	2.52	7.28

Functional Schematic
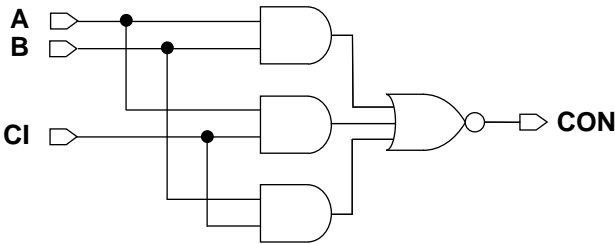
AC Power

Pin	Power (uW/MHz)	
	X2	X4
A	0.0170	0.0207
B	0.0167	0.0191
CI	0.0052	0.0088

Pin Capacitance

Pin	Capacitance (pF)	
	X2	X4
A	0.0027	0.0028
B	0.0083	0.0085
CI	0.0028	0.0052

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	X4	X2	X4
A	→	CON	↑	0.1277	0.1406	4.1886	4.2962
A	→	CON	↓	0.1255	0.1338	2.4988	2.4921
B	→	CON	↑	0.0853	0.0916	4.2740	4.3322
B	→	CON	↓	0.0786	0.0862	2.5591	2.5364
CI	→	CON	↑	0.0364	0.0304	4.1850	2.1448
CI	→	CON	↓	0.0263	0.0232	2.6078	1.3312
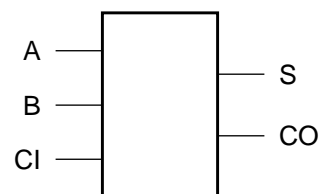
Cell Description

The ADDF cell provides the arithmetic sum (S) and carry out (CO) of two operands (A,B) with carry in (CI). The two outputs (S,CO) are represented by the logic equations:

$S = (A \oplus B \oplus CI)$

$CO = (A \oplus B) \bullet CI + (A \bullet B)$

Logic Symbol

Function Table

CI	A	B	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
ADDFXLADTH	2.52	7.00
ADDFX1ADTH	2.52	7.00
ADDFX2ADTH	2.52	7.00
ADDFX4ADTH	2.52	7.84

Functional Schematic
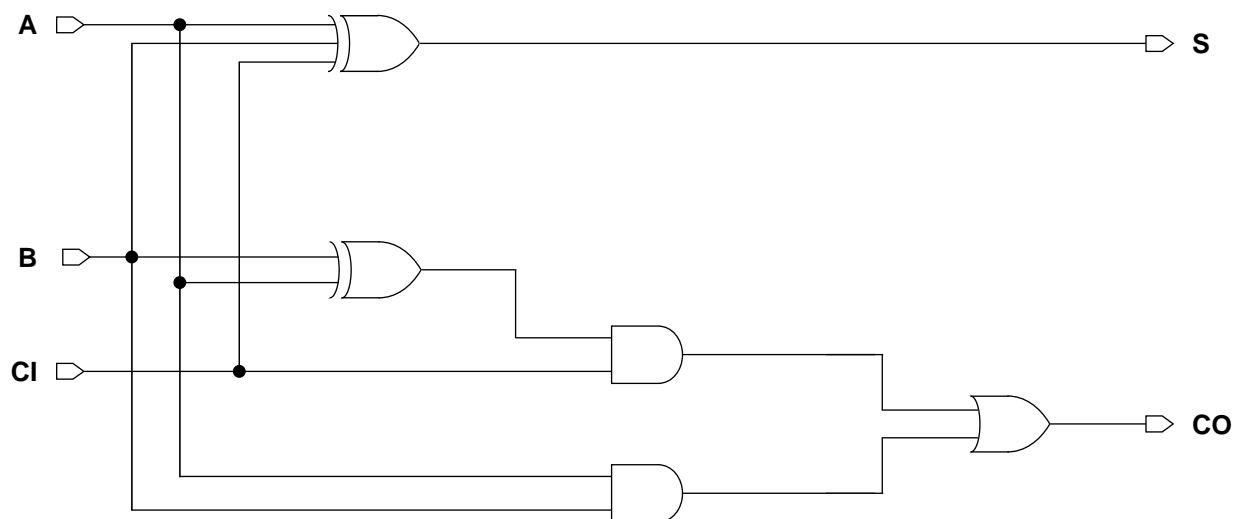
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A	0.0146	0.0154	0.0183	0.0235
B	0.0175	0.0182	0.0213	0.0262
CI	0.0077	0.0085	0.0111	0.0166

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A	0.0026	0.0026	0.0028	0.0028
B	0.0025	0.0025	0.0028	0.0028
CI	0.0027	0.0027	0.0029	0.0030

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A	→	S	↑	0.1464	0.1499	0.1510	0.1751	7.1728	4.8662	2.9788	1.5520
A	→	S	↓	0.1999	0.2103	0.2067	0.2393	6.5618	4.3986	1.9833	1.0614
B	→	S	↑	0.1725	0.1759	0.1753	0.1956	7.1775	4.8676	2.9857	1.5604
B	→	S	↓	0.2239	0.2344	0.2307	0.2623	6.5637	4.3995	1.9839	1.0617
CI	→	S	↑	0.1095	0.1141	0.1179	0.1467	7.0987	4.8360	2.9761	1.5618
CI	→	S	↓	0.1053	0.1156	0.1190	0.1535	6.5242	4.3973	1.9947	1.0790
A	→	CO	↑	0.1863	0.1923	0.1914	0.2226	6.9901	4.5232	2.9278	1.5184
A	→	CO	↓	0.1773	0.1883	0.1890	0.2255	6.1132	4.1857	1.8897	1.0190
B	→	CO	↑	0.2103	0.2163	0.2153	0.2456	6.9909	4.5238	2.9281	1.5185
B	→	CO	↓	0.2030	0.2130	0.2115	0.2462	5.8353	4.0052	1.7751	0.9378
CI	→	CO	↑	0.0953	0.1012	0.1107	0.1388	7.1303	4.6001	2.9783	1.5499
CI	→	CO	↓	0.1187	0.1300	0.1330	0.1667	6.2669	4.2447	1.9098	1.0386

Cell Description

The ADDFH cell is a high-speed cell providing the arithmetic sum (S) and carry out (CO) of two operands (A,B) with carry in (CI). The two outputs (S,CO) are represented by the logic equations:

$S = (A \oplus B \oplus CI)$

$CO = (A \oplus B) \bullet CI + (A \bullet B)$

Logic Symbol
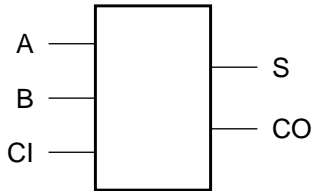
Function Table

CI	A	B	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
ADDFHXLADTH	2.52	7.56
ADDFHX1ADTH	2.52	8.12
ADDFHX2ADTH	2.52	10.92
ADDFHX4ADTH	2.52	17.64

Functional Schematic
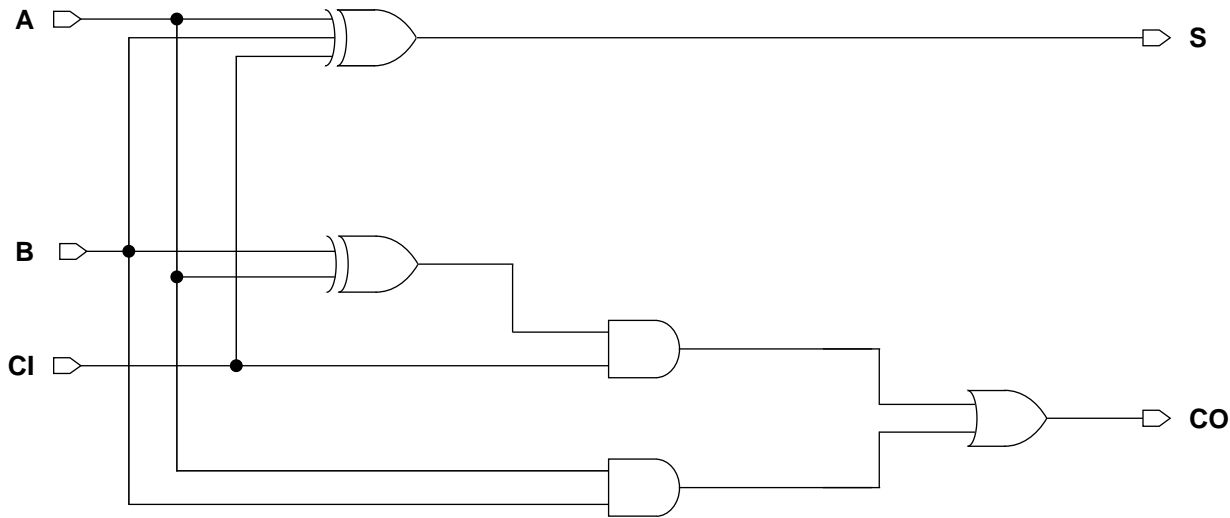
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A	0.0164	0.0200	0.0333	0.0579
B	0.0141	0.0179	0.0282	0.0511
CI	0.0085	0.0103	0.0154	0.0305

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A	0.0025	0.0030	0.0049	0.0093
B	0.0044	0.0061	0.0096	0.0172
CI	0.0016	0.0019	0.0027	0.0052

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A	→	S	↑	0.1814	0.1573	0.1498	0.1364	7.0761	4.6642	2.9022	1.4866
A	→	S	↓	0.1851	0.1677	0.1587	0.1447	6.2291	4.0286	1.7154	0.8427
B	→	S	↑	0.1386	0.1177	0.1081	0.1083	7.1248	4.6575	2.9051	1.4886
B	→	S	↓	0.1614	0.1391	0.1263	0.1187	6.2364	4.0298	1.7264	0.8465
CI	→	S	↑	0.1399	0.1199	0.1096	0.1106	7.1102	4.6736	2.9070	1.4889
CI	→	S	↓	0.1538	0.1305	0.1145	0.1120	6.2723	4.0417	1.7303	0.8488
A	→	CO	↑	0.1815	0.1572	0.1513	0.1353	7.0494	4.5064	2.9618	1.4934
A	→	CO	↓	0.1854	0.1690	0.1593	0.1461	5.7790	3.9556	1.7546	0.8535
B	→	CO	↑	0.1293	0.1120	0.1031	0.0946	7.0614	4.5117	2.9644	1.4947
B	→	CO	↓	0.1524	0.1341	0.1222	0.1168	5.7813	3.9324	1.7440	0.8376
CI	→	CO	↑	0.0799	0.0686	0.0642	0.0613	7.1076	4.5295	2.9704	1.4977
CI	→	CO	↓	0.1128	0.1032	0.0968	0.0936	6.2728	4.1077	1.7920	0.8777

Cell Description

The ADDH cell provides the arithmetic sum
(S) and carry out (CO) of two operands (A,B).
The two outputs (S,CO) are represented by the
logic equations:

$$S = (\overline{A} \bullet B) + (A \bullet \overline{B})$$

$$CO = A \bullet B$$

Logic Symbol
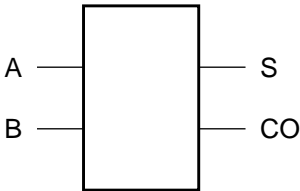
Function Table

A	B	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Cell Size

Drive Strength	Height (um)	Width (um)
ADDHXLADTH	2.52	4.20
ADDHX1ADTH	2.52	4.20
ADDHX2ADTH	2.52	4.48
ADDHX4ADTH	2.52	6.44

Functional Schematic
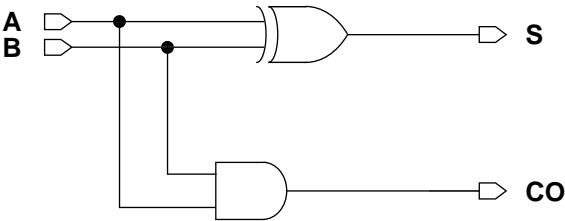
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A	0.0073	0.0092	0.0149	0.0273
B	0.0050	0.0058	0.0084	0.0153

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A	0.0019	0.0029	0.0048	0.0087
B	0.0025	0.0026	0.0030	0.0050

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A	→ S	↑	0.0781	0.0585	0.0541	0.0491	11.3250	7.9891	4.2860	2.2135
A	→ S	↓	0.0903	0.0798	0.0608	0.0541	8.4583	6.3394	2.6816	1.3441
B	→ S	↑	0.0362	0.0339	0.0339	0.0337	11.5761	8.0705	4.3459	2.2315
B	→ S	↓	0.0410	0.0432	0.0473	0.0445	8.0001	6.0817	2.5400	1.2803
A	→ CO	↑	0.0498	0.0569	0.0501	0.0494	6.7353	4.4588	2.9118	1.4504
A	→ CO	↓	0.0636	0.0757	0.0623	0.0585	5.6719	3.8726	1.6438	0.8286
B	→ CO	↑	0.0494	0.0551	0.0488	0.0479	6.7532	4.4606	2.9095	1.4498
B	→ CO	↓	0.0590	0.0690	0.0569	0.0529	5.6645	3.8578	1.6367	0.8232

Cell Description

The AFCSHCIN cell provides a carry-select adder function that produces the arithmetic sum (S) and carryouts (CO0,CO1) of the operands (A,B) with active-low carry-ins (CI0N,CI1N).The three outputs (S,CO0,CO1) are represented by the logic equations:

$$S = CS \bullet (A \oplus B \oplus \overline{CI1N}) + \overline{CS} \bullet (A \oplus B \oplus \overline{CI0N})$$

$$CO0 = (A \bullet B) + (A \bullet \overline{CI0N}) + (B \bullet \overline{CI0N})$$

$$CO1 = (A \bullet B) + (A \bullet \overline{CI1N}) + (B \bullet \overline{CI1N})$$

Logic Symbol
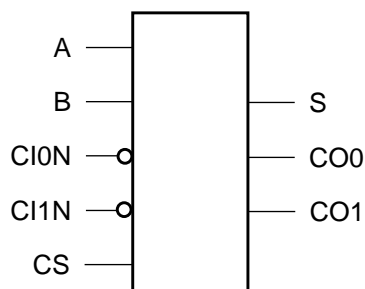
Cell Size

Drive Strength	Height (um)	Width (um)
AFCSHCINX2ADTH	2.52	15.96
AFCSHCINX4ADTH	2.52	16.52

Function Table

A	B	CI0N	CI1N	CS	S	CO0	CO1
0	0	0	0	0	1	0	0
0	0	0	0	1	1	0	0
0	0	0	1	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	0	0	0
0	0	1	0	1	1	0	0
0	0	1	1	0	0	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	0	1	1
0	1	0	0	1	0	1	1
0	1	0	1	0	0	1	0
0	1	0	1	1	1	1	0
0	1	1	0	0	1	0	1
0	1	1	0	1	0	0	1
0	1	1	1	0	1	0	0
0	1	1	1	1	1	0	0

Function Table (Cont'd.)

A	B	CI0N	CI1N	CS	S	CO0	CO1
1	0	0	0	0	0	1	1
1	0	0	0	1	0	1	1
1	0	0	1	0	0	1	0
1	0	0	1	1	1	1	0
1	0	1	0	0	1	0	1
1	0	1	0	1	0	0	1
1	0	1	1	0	1	0	0
1	0	1	1	1	1	0	0
1	1	0	0	0	1	1	1
1	1	0	0	1	1	1	1
1	1	0	1	0	1	1	1
1	1	0	1	1	0	1	1
1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	1
1	1	1	1	0	0	1	1
1	1	1	1	1	0	1	1

Functional Schematic
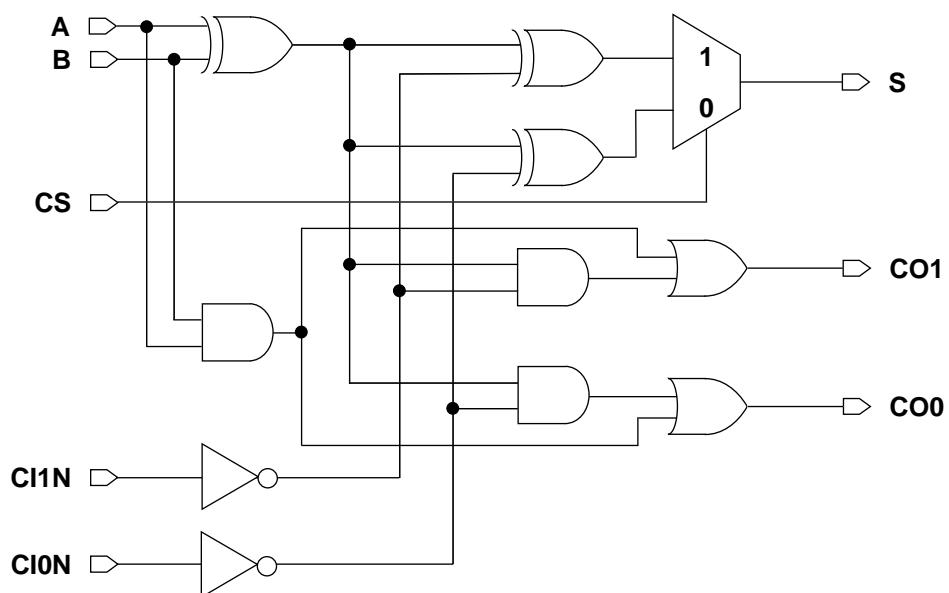
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
CS	0.0083	0.0083
A	0.0394	0.0395
B	0.0362	0.0362
CI0N	0.0181	0.0203
CI1N	0.0188	0.0201

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
CS	0.0019	0.0019
A	0.0028	0.0028
B	0.0060	0.0060
CI0N	0.0047	0.0074
CI1N	0.0051	0.0068

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
CS	→	S	↑	0.1131	0.1138	2.8851	2.8508
CS	→	S	↓	0.1068	0.1112	1.7421	1.6515
A	→	S	↑	0.3086	0.3116	2.8900	2.8520
A	→	S	↓	0.3069	0.3083	1.7512	1.6518
B	→	S	↑	0.2597	0.2618	2.8898	2.8526
B	→	S	↓	0.2619	0.2639	1.7513	1.6519
CI0N	→	S	↑	0.1961	0.1940	2.8900	2.8526
CI0N	→	S	↓	0.1951	0.1881	1.7510	1.6517
CI1N	→	S	↑	0.1636	0.1653	2.8696	2.8446
CI1N	→	S	↓	0.1639	0.1699	1.7425	1.6516
A	→	CO0	↑	0.1367	0.1430	5.1443	4.9575
A	→	CO0	↓	0.1718	0.1777	3.1681	3.0522
B	→	CO0	↑	0.1077	0.1148	5.0309	4.8947
B	→	CO0	↓	0.1206	0.1255	3.1392	3.0427
CI0N	→	CO0	↑	0.0398	0.0318	4.3525	3.2623
CI0N	→	CO0	↓	0.0260	0.0237	2.5226	2.0194
A	→	CO1	↑	0.1304	0.1389	5.1381	4.9319
A	→	CO1	↓	0.1764	0.1820	3.2410	3.1254
B	→	CO1	↑	0.0932	0.0975	5.0290	4.9005
B	→	CO1	↓	0.1220	0.1269	3.2221	3.1181
CI1N	→	CO1	↑	0.0385	0.0309	4.3595	3.3673
CI1N	→	CO1	↓	0.0259	0.0201	2.6009	1.9487

Cell Description

The AFCSHCON cell provides a carry-select adder function that produces the arithmetic sum (S) and active-low carryouts (CO0N,CO1N) of two operands (A,B) with carry-ins (CI0,CI1). The three outputs (S,CO0N,CO1N) are represented by the logic equations:

$$S = CS \bullet (A \oplus B \oplus CI1) + \overline{CS} \bullet (A \oplus B \oplus CI0)$$

$$CO0N = \overline{(A \bullet B) + (A \bullet CI0) + (B \bullet CI0)}$$

$$CO1N = \overline{(A \bullet B) + (A \bullet CI1) + (B \bullet CI1)}$$

Logic Symbol
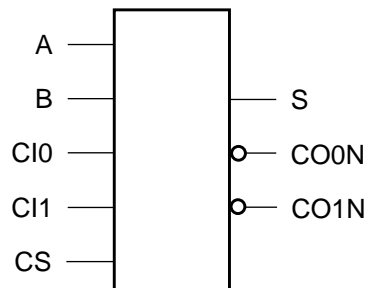
Cell Size

Drive Strength	Height (um)	Width (um)
AFCSHCONX2ADTH	2.52	15.12
AFCSHCONX4ADTH	2.52	16.24

Function Table

A	B	CI0	CI1	CS	S	CO0N	CO1N
0	0	0	0	0	0	1	1
0	0	0	0	1	0	1	1
0	0	0	1	0	0	1	1
0	0	0	1	1	1	1	1
0	0	1	0	0	1	1	1
0	0	1	0	1	0	1	1
0	0	1	1	0	1	1	1
0	0	1	1	1	1	1	1
0	1	0	0	0	1	1	1
0	1	0	0	1	1	1	1
0	1	0	1	0	1	1	0
0	1	0	1	1	0	1	0
0	1	1	0	0	0	0	1
0	1	1	0	1	1	0	1
0	1	1	1	0	0	0	0
0	1	1	1	1	0	0	0

Function Table (Cont'd.)

A	B	CI0	CI1	CS	S	CO0N	CO1N
1	0	0	0	0	1	1	1
1	0	0	0	1	1	1	1
1	0	0	1	0	1	1	0
1	0	0	1	1	0	1	0
1	0	1	0	0	0	0	1
1	0	1	0	1	1	0	1
1	0	1	1	0	0	0	0
1	0	1	1	1	0	0	0
1	1	0	0	0	0	0	0
1	1	0	0	1	0	0	0
1	1	0	1	0	0	0	0
1	1	0	1	1	1	0	0
1	1	1	0	0	1	0	0
1	1	1	0	1	0	0	0
1	1	1	1	0	1	0	0
1	1	1	1	1	1	0	0

Functional Schematic
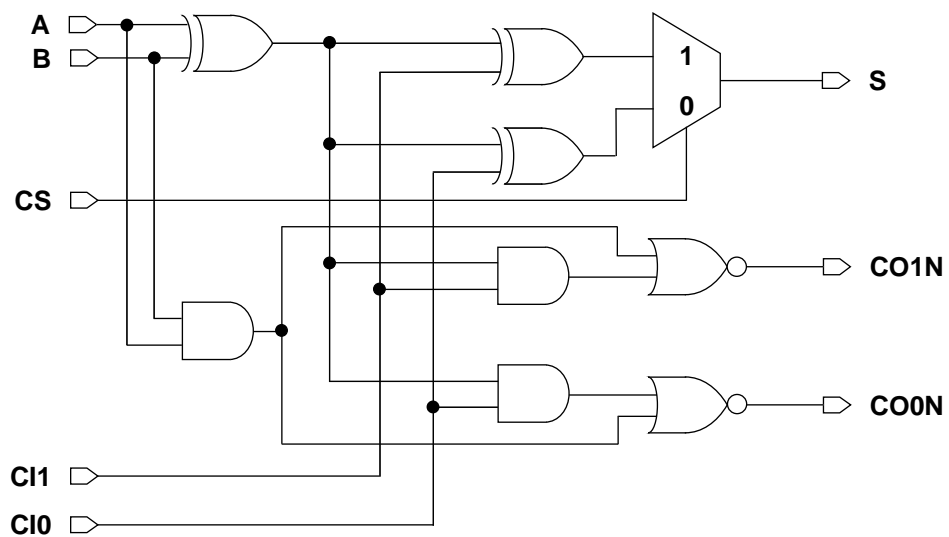
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
CS	0.0085	0.0084
A	0.0373	0.0383
B	0.0374	0.0383
CI0	0.0164	0.0216
CI1	0.0171	0.0199

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
CS	0.0039	0.0039
A	0.0050	0.0051
B	0.0065	0.0065
CI0	0.0046	0.0103
CI1	0.0054	0.0090

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)		K_{load} (ns/pF)	
			X2	**X4**	**X2**	**X4**
CS	→	S ↑	0.1092	0.1082	2.8803	2.8511
CS	→	S ↓	0.1086	0.1121	1.7463	1.6519
A	→	S ↑	0.3533	0.3594	2.8856	2.8526
A	→	S ↓	0.3310	0.3355	1.7565	1.6536
B	→	S ↑	0.3363	0.3423	2.8855	2.8531
B	→	S ↓	0.3142	0.3185	1.7563	1.6536
CI0	→	S ↑	0.1902	0.1879	2.8856	2.8530
CI0	→	S ↓	0.1904	0.1797	1.7553	1.6531
CI1	→	S ↑	0.1607	0.1575	2.8704	2.8476
CI1	→	S ↓	0.1659	0.1614	1.7467	1.6520
A	→	CO0N ↑	0.1501	0.1578	4.5222	4.1050
A	→	CO0N ↓	0.1878	0.1982	2.8915	2.6818
B	→	CO0N ↑	0.1373	0.1427	5.0456	4.1013
B	→	CO0N ↓	0.1705	0.1809	2.8893	2.6807
CI0	→	CO0N ↑	0.0368	0.0260	5.0793	3.8710
CI0	→	CO0N ↓	0.0263	0.0235	2.9084	2.2885
A	→	CO1N ↑	0.1614	0.1688	5.2181	4.3291
A	→	CO1N ↓	0.1918	0.2023	2.8381	2.6283
B	→	CO1N ↑	0.1343	0.1430	4.5643	4.0962
B	→	CO1N ↓	0.1746	0.1851	2.8350	2.6265
CI1	→	CO1N ↑	0.0357	0.0298	5.0399	4.2594
CI1	→	CO1N ↓	0.0268	0.0231	3.1231	2.5962

Cell Description

The AFCSIHCON cell provides a carry-select adder function for the initial stage of carry-select adder block. The function produces the arithmetic sum (S) and activelow carryouts (CO0N,CO1N) of two operands (A,B).The three outputs (S,CO0N,CO1N) are represented by the logic equations:

$S = A \oplus B \oplus CS$

$CO0N = \overline{A \bullet B}$

$CO1N = \overline{A + B}$

Logic Symbol
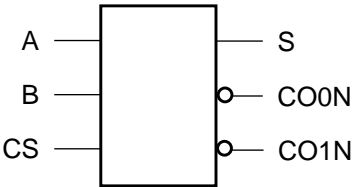
Function Table

A	B	CS	S	CO0N	CO1N
0	0	0	0	1	1
0	0	1	1	1	1
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	0	0	0
1	1	1	1	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
AFCSIHCONX2ADTH	2.52	6.16
AFCSIHCONX4ADTH	2.52	7.56

Functional Schematic
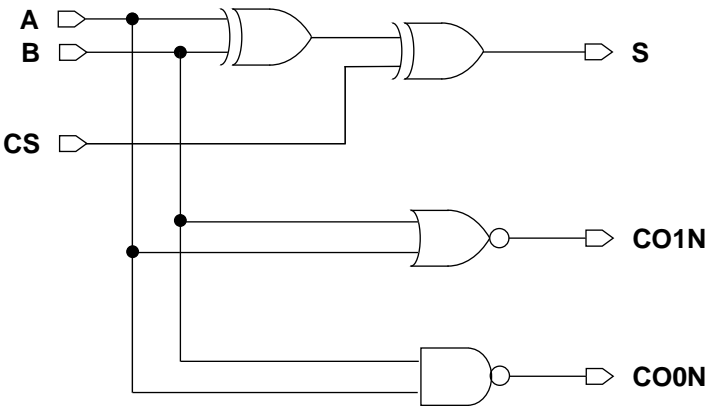
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
A	0.0176	0.0215
B	0.0173	0.0217
CS	0.0083	0.0084

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
A	0.0063	0.0105
B	0.0079	0.0120
CS	0.0039	0.0038

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
A	→	S	↑	0.1881	0.1905	2.8811	2.8517
A	→	S	↓	0.2153	0.2274	2.0726	1.8352
B	→	S	↑	0.1698	0.1717	2.9767	2.8883
B	→	S	↓	0.1969	0.2011	1.8703	1.7744
CS	→	S	↑	0.0998	0.1007	2.8744	2.8494
CS	→	S	↓	0.1023	0.1128	2.0484	1.8234
A	→	CO0N	↑	0.0192	0.0177	3.8556	1.9461
A	→	CO0N	↓	0.0169	0.0149	3.1895	1.5224
B	→	CO0N	↑	0.0233	0.0216	3.9567	1.9366
B	→	CO0N	↓	0.0190	0.0173	3.1870	1.5216
A	→	CO1N	↑	0.0256	0.0259	6.3605	3.0739
A	→	CO1N	↓	0.0128	0.0141	2.0279	0.9793
B	→	CO1N	↑	0.0332	0.0310	6.3587	3.0706
B	→	CO1N	↓	0.0153	0.0145	2.0257	0.9892

Cell Description

The AFHCIN cell is a full adder that provides the arithmetic sum (S) and carry-out (CO) of two operands (A,B) with active-low carry-in (CIN). The outputs (S,CO) are represented by the logic equations:

$$S = A \oplus B \oplus \overline{CIN}$$

$$CO = (A \bullet B) + (A \bullet \overline{CIN}) + (B \bullet \overline{CIN})$$

Logic Symbol
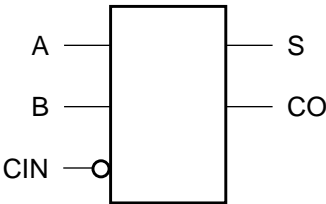
Function Table

A	B	CIN	S	CO
0	0	0	1	0
0	0	1	0	0
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

Cell Size

Drive Strength	Height (um)	Width (um)
AFHCINX2ADTH	2.52	8.96
AFHCINX4ADTH	2.52	11.48

Functional Schematic

TSMC CLN90G HVT
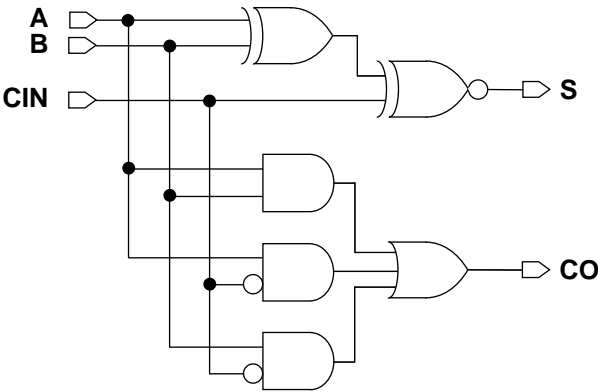
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
A	0.0233	0.0293
B	0.0242	0.0327
CIN	0.0159	0.0251

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
A	0.0028	0.0028
B	0.0067	0.0070
CIN	0.0051	0.0100

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
A	→	S	↑	0.1742	0.2109	3.0627	3.0978
A	→	S	↓	0.1885	0.2211	1.8190	1.6809
B	→	S	↑	0.1354	0.1788	3.0660	3.1004
B	→	S	↓	0.1517	0.1712	1.8194	1.6789
CIN	→	S	↑	0.0917	0.0917	3.0510	3.0901
CIN	→	S	↓	0.1066	0.1156	1.8186	1.6821
A	→	CO	↑	0.1021	0.1219	4.7819	3.4154
A	→	CO	↓	0.1318	0.1548	2.8551	2.0229
B	→	CO	↑	0.0863	0.1031	4.5527	3.3223
B	→	CO	↓	0.1072	0.1262	2.8099	1.9626
CIN	→	CO	↑	0.0366	0.0336	4.0835	2.1153
CIN	→	CO	↓	0.0286	0.0272	2.6336	1.2673

Cell Description

The AFHCON cell is a full adder that provides the arithmetic sum (S) and active-low carry-out (CON) of two operands (A,B) with carry-in (CI). The outputs (S,CON) are represented by the logic equations:

$$S = A \oplus B \oplus CI$$

$$CON = \overline{(A \bullet B) + (A \bullet CI) + (B \bullet CI)}$$

Logic Symbol

A — S

B — CON

CI
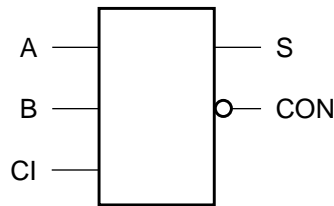
Function Table

A	B	CI	S	CON
0	0	0	0	1
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
AFHCONX2ADTH	2.52	8.96
AFHCONX4ADTH	2.52	9.52

Functional Schematic
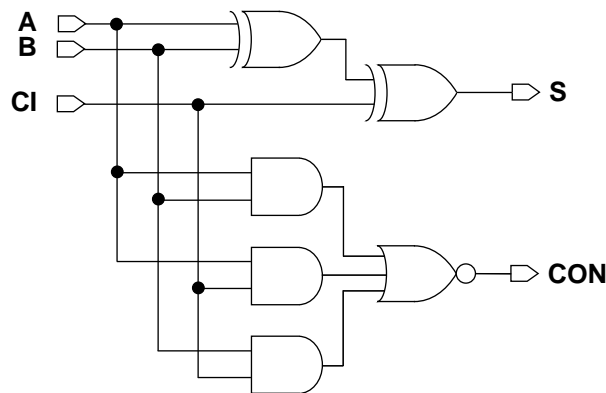
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
A	0.0233	0.0253
B	0.0220	0.0236
CI	0.0163	0.0201

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
A	0.0027	0.0027
B	0.0081	0.0080
CI	0.0051	0.0075

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
A	→	S	↑	0.1615	0.1695	3.0515	3.0760
A	→	S	↓	0.1802	0.1898	1.8067	1.6976
B	→	S	↑	0.1218	0.1286	3.0521	3.0764
B	→	S	↓	0.1386	0.1473	1.8067	1.6972
CI	→	S	↑	0.0889	0.0918	3.0398	3.0687
CI	→	S	↓	0.1058	0.1103	1.8071	1.6967
A	→	CON	↑	0.1388	0.1517	4.4312	4.4410
A	→	CON	↓	0.1261	0.1408	2.6743	2.6963
B	→	CON	↑	0.1005	0.1138	4.4802	4.4686
B	→	CON	↓	0.0858	0.0998	2.7276	2.7290
CI	→	CON	↑	0.0386	0.0313	4.3527	2.2358
CI	→	CON	↓	0.0286	0.0241	2.7736	1.3421

Cell Description

The AHCSHCIN cell provides a carry-select halfadder function that produces the arithmetic sum (S) and carryout (CO) of a single operand (A) with activelow carry-in (CIN). The outputs (S,CO) are represented by the following equations:

$$S = CS \bullet (A \oplus \overline{CIN}) + (\overline{CS} \bullet (A)$$

$$CO = A \bullet \overline{CIN}$$

Logic Symbol
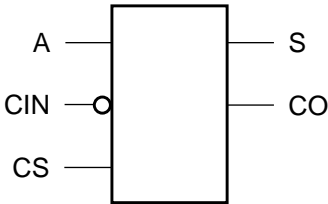
Function Table

A	CIN	CS	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	1	0
1	1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
AHCSHCINX2ADTH	2.52	5.32
AHCSHCINX4ADTH	2.52	6.16

Functional Schematic
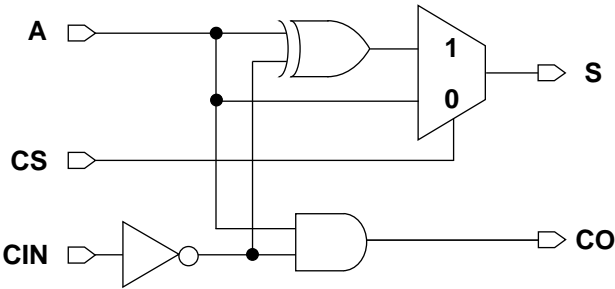
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
CS	0.0079	0.0080
A	0.0163	0.0192
CIN	0.0145	0.0171

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
CS	0.0038	0.0038
A	0.0028	0.0028
CIN	0.0071	0.0093

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
CS	→	S	↑	0.0796	0.0822	2.8670	2.8297
CS	→	S	↓	0.0950	0.1032	1.9396	1.7367
A	→	S	↑	0.1461	0.1601	2.9128	2.8463
A	→	S	↓	0.1869	0.1997	1.9553	1.7441
CIN	→	S	↑	0.1330	0.1347	2.9118	2.8458
CIN	→	S	↓	0.1434	0.1510	1.9548	1.7439
A	→	CO	↑	0.0629	0.0681	6.1474	3.1187
A	→	CO	↓	0.0839	0.0939	2.1686	1.1035
CIN	→	CO	↑	0.0249	0.0233	6.1521	3.1164
CIN	→	CO	↓	0.0128	0.0121	1.9983	0.9851

Cell Description

The AHCSHCON cell provides a carry-select halfadder function that produces the arithmetic sum (S) and active-low carryout (CON) of a single operand (A) with carry-in (CI). The outputs (S,CON) are represented by the following equations:

$$S = CS \bullet (A \oplus CI) + \overline{CS} \bullet (A)$$

$$CON = \overline{A \bullet CI}$$

Logic Symbol
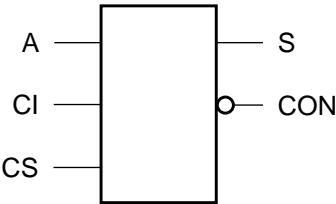
Function Table

A	CI	CS	S	CON
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	0
1	1	1	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
AHCSHCONX2ADTH	2.52	5.32
AHCSHCONX4ADTH	2.52	6.16

Functional Schematic
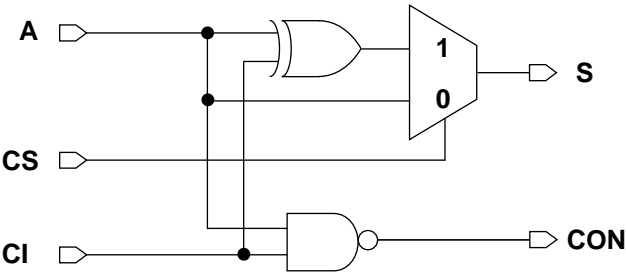
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
CS	0.0078	0.0078
A	0.0162	0.0195
CI	0.0119	0.0139

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
CS	0.0039	0.0039
A	0.0047	0.0072
CI	0.0060	0.0073

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
CS	→	S	↑	0.0798	0.0806	2.8649	2.8575
CS	→	S	↓	0.0961	0.1029	1.9565	1.7507
A	→	S	↑	0.1316	0.1343	2.9123	2.8748
A	→	S	↓	0.1877	0.1951	1.9742	1.7593
CI	→	S	↑	0.1071	0.1085	2.8953	2.8677
CI	→	S	↓	0.1799	0.1870	1.9734	1.7592
A	→	CON	↑	0.0234	0.0229	3.9850	1.9778
A	→	CON	↓	0.0171	0.0171	2.7416	1.4125
CI	→	CON	↑	0.0189	0.0182	3.8683	2.0181
CI	→	CON	↓	0.0148	0.0141	2.7403	1.4120

Cell Description

The AHHCIN cell is a half adder that provides the arithmetic sum (S) and carry-out (CO) of the input operand (A) with an active-low carry-in (CIN). The outputs (S,CO) are represented by the logic equations:

$S = A \oplus \overline{CIN}$

$CO = A \bullet \overline{CIN}$

Logic Symbol
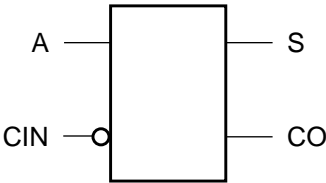
Function Table

A	CIN	S	CO
0	0	1	0
0	1	0	0
1	0	0	1
1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
AHHCINX2ADTH	2.52	4.20
AHHCINX4ADTH	2.52	5.04

Functional Schematic
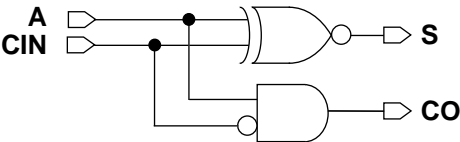
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
A	0.0126	0.0157
CIN	0.0111	0.0148

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
A	0.0038	0.0048
CIN	0.0067	0.0088

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
A	→	S	↑	0.0577	0.0566	4.2231	4.3198
A	→	S	↓	0.0615	0.0621	2.4808	2.4742
CIN	→	S	↑	0.0390	0.0388	4.2904	4.3472
CIN	→	S	↓	0.0526	0.0507	2.2657	2.3304
A	→	CO	↑	0.0469	0.0435	5.9371	3.0596
A	→	CO	↓	0.0510	0.0453	1.6307	0.8036
CIN	→	CO	↑	0.0326	0.0328	5.9274	3.0564
CIN	→	CO	↓	0.0129	0.0127	1.5758	0.7934

Cell Description

The AHHCON cell is a half adder that provides the arithmetic sum (S) and active-low carry-out (CON) of the input operand (A) with carry-in (CI). The outputs (S,CON) are represented by the logic equations:

$S = A \oplus CI$

$CON = \overline{A \bullet CI}$

Logic Symbol
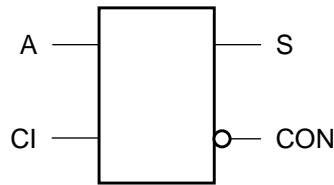
Function Table

A	CI	S	CON
0	0	0	1
0	1	1	1
1	0	1	1
1	1	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
AHHCONX2ADTH	2.52	3.64
AHHCONX4ADTH	2.52	6.16

Functional Schematic
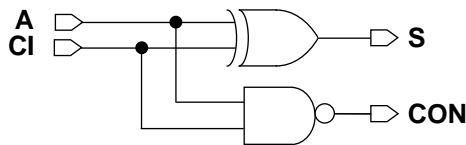
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
A	0.0127	0.0250
CI	0.0077	0.0144

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
A	0.0049	0.0104
CI	0.0069	0.0130

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
A	→	S	↑	0.0526	0.0518	4.3837	2.2402
A	→	S	↓	0.0629	0.0595	2.6736	1.3574
CI	→	S	↑	0.0371	0.0360	4.3103	2.2610
CI	→	S	↓	0.0503	0.0472	2.5239	1.2918
A	→	CON	↑	0.0201	0.0205	3.0089	1.5121
A	→	CON	↓	0.0188	0.0192	2.8650	1.4480
CI	→	CON	↑	0.0169	0.0174	2.9257	1.4884
CI	→	CON	↓	0.0167	0.0171	2.8661	1.4488

Cell Description

The AND2 cell provides the logical AND of two inputs (A,B). The output (Y) is represented by the logic equation:

$Y = (A \bullet B)$

Logic Symbol

A — Y
B
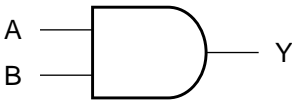
Function Table

A	B	Y
0	x	0
x	0	0
1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
AND2XLADTH	2.52	1.40
AND2X1ADTH	2.52	1.40
AND2X2ADTH	2.52	1.40
AND2X4ADTH	2.52	2.24
AND2X6ADTH	2.52	2.80
AND2X8ADTH	2.52	3.92

Functional Schematic

A
B — Y
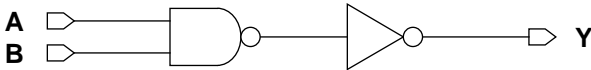
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0024	0.0028	0.0041	0.0073	0.0107	0.0145
B	0.0027	0.0031	0.0047	0.0084	0.0125	0.0166

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0010	0.0010	0.0014	0.0027	0.0037	0.0052
B	0.0011	0.0011	0.0016	0.0028	0.0041	0.0051

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	0.0506	0.0543	0.0484	0.0456	0.0429	0.0449
A	→ Y	↓	0.0579	0.0664	0.0568	0.0531	0.0537	0.0528
B	→ Y	↑	0.0544	0.0581	0.0517	0.0484	0.0462	0.0477
B	→ Y	↓	0.0658	0.0745	0.0643	0.0585	0.0591	0.0598

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	6.8549	4.3778	2.8748	1.4468	0.9939	0.7419
A	→ Y	↓	5.0700	3.8443	1.6431	0.8139	0.5438	0.4043
B	→ Y	↑	6.8558	4.3784	2.8750	1.4462	0.9938	0.7418
B	→ Y	↓	5.1101	3.8650	1.6542	0.8176	0.5454	0.4076

TSMC CLN90G HVT

Cell Description

The AND3 cell provides the logical AND of three inputs (A,B,C). The output (Y) is represented by the logic equation:

$Y = (A \bullet B \bullet C)$

Logic Symbol
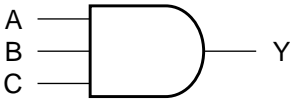
Function Table

A	B	C	Y
0	x	x	0
x	0	x	0
x	x	0	0
1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
AND3XLADTH	2.52	1.68
AND3X1ADTH	2.52	1.68
AND3X2ADTH	2.52	1.68
AND3X4ADTH	2.52	3.08
AND3X6ADTH	2.52	3.64
AND3X8ADTH	2.52	5.04

Functional Schematic
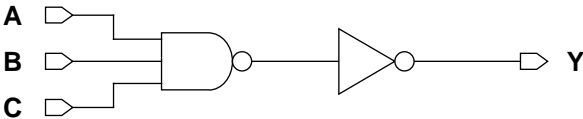
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0026	0.0031	0.0046	0.0081	0.0117	0.0161
B	0.0030	0.0035	0.0053	0.0094	0.0138	0.0186
C	0.0033	0.0040	0.0060	0.0110	0.0160	0.0212

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0010	0.0011	0.0016	0.0028	0.0039	0.0062
B	0.0011	0.0011	0.0016	0.0030	0.0043	0.0058
C	0.0012	0.0012	0.0017	0.0036	0.0047	0.0058

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	0.0746	0.0696	0.0610	0.0555	0.0514	0.0531
A	→ Y	↓	0.0718	0.0801	0.0655	0.0612	0.0594	0.0589
B	→ Y	↑	0.0796	0.0746	0.0659	0.0605	0.0569	0.0579
B	→ Y	↓	0.0751	0.0871	0.0746	0.0679	0.0669	0.0663
C	→ Y	↑	0.0840	0.0787	0.0694	0.0647	0.0602	0.0605
C	→ Y	↓	0.0820	0.0952	0.0816	0.0738	0.0734	0.0728

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	7.0736	4.4503	2.8978	1.4868	1.0062	0.7528
A	→ Y	↓	5.2388	3.9018	1.6630	0.8232	0.5417	0.4075
B	→ Y	↑	7.0739	4.4501	2.8982	1.4865	1.0064	0.7526
B	→ Y	↓	5.2471	3.9247	1.6810	0.8282	0.5449	0.4110
C	→ Y	↑	7.0763	4.4500	2.8983	1.4868	1.0064	0.7526
C	→ Y	↓	5.2844	3.9463	1.6920	0.8307	0.5479	0.4145

Cell Description

The AND4 cell provides the logical AND of four inputs (A,B,C,D). The output (Y) is represented by the logic equation:

$Y = (A \bullet B \bullet C \bullet D)$

Logic Symbol

A
B
C
D
Y
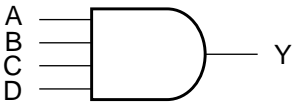
Function Table

A	B	C	D	Y
0	x	x	x	0
x	0	x	x	0
x	x	0	x	0
x	x	x	0	0
1	1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
AND4XLADTH	2.52	2.24
AND4X1ADTH	2.52	2.24
AND4X2ADTH	2.52	2.24
AND4X4ADTH	2.52	3.64
AND4X6ADTH	2.52	5.04
AND4X8ADTH	2.52	6.44

Functional Schematic

A
B
C
D
Y
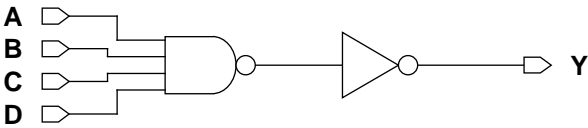
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0028	0.0033	0.0049	0.0083	0.0132	0.0172
B	0.0032	0.0039	0.0058	0.0100	0.0155	0.0202
C	0.0036	0.0044	0.0066	0.0115	0.0177	0.0233
D	0.0039	0.0048	0.0074	0.0132	0.0203	0.0268

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0010	0.0011	0.0017	0.0030	0.0054	0.0066
B	0.0011	0.0012	0.0017	0.0034	0.0052	0.0066
C	0.0010	0.0011	0.0016	0.0034	0.0050	0.0070
D	0.0013	0.0014	0.0019	0.0038	0.0055	0.0077

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	0.0926	0.0772	0.0688	0.0608	0.0654	0.0645
A	→ Y	↓	0.0712	0.0817	0.0701	0.0624	0.0685	0.0661
B	→ Y	↑	0.0997	0.0846	0.0760	0.0691	0.0726	0.0718
B	→ Y	↓	0.0768	0.0899	0.0806	0.0731	0.0753	0.0726
C	→ Y	↑	0.1039	0.0890	0.0807	0.0736	0.0775	0.0769
C	→ Y	↓	0.0816	0.0971	0.0881	0.0804	0.0846	0.0824
D	→ Y	↑	0.1123	0.0959	0.0857	0.0775	0.0817	0.0812
D	→ Y	↓	0.0918	0.1097	0.0957	0.0880	0.0917	0.0891

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)					
				XL	X1	X2	X4	X6	X8
A	→	Y	↑	7.4555	4.6348	2.9223	1.5008	1.0169	0.7678
A	→	Y	↓	5.2209	3.8875	1.6718	0.8231	0.5585	0.4150
B	→	Y	↑	7.4559	4.6346	2.9218	1.5006	1.0168	0.7678
B	→	Y	↓	5.2595	3.9132	1.6928	0.8324	0.5606	0.4165
C	→	Y	↑	7.4559	4.6341	2.9220	1.5008	1.0167	0.7679
C	→	Y	↓	5.3012	3.9407	1.7072	0.8399	0.5674	0.4217
D	→	Y	↑	7.4582	4.6350	2.9224	1.5010	1.0170	0.7680
D	→	Y	↓	5.3589	3.9787	1.7190	0.8477	0.5714	0.4247

Cell Description

The AO21 cell provides the logical OR of one
AND group and an additional input. The output
(Y) is represented by the logic equation:

$$Y = (A0 \bullet A1) + \overline{B0}$$

Logic Symbol

A0
A1

B0 —————————— Y
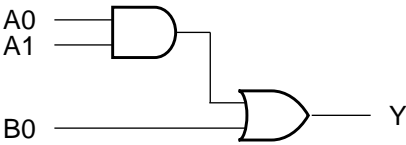
Function Table

A0	A1	B0	Y
0	x	0	0
x	0	0	0
x	x	1	1
1	1	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
AO21XLADTH	2.52	1.96
AO21X1ADTH	2.52	1.96
AO21X2ADTH	2.52	1.96
AO21X4ADTH	2.52	2.52

Functional Schematic

A0
A1

B0

Y
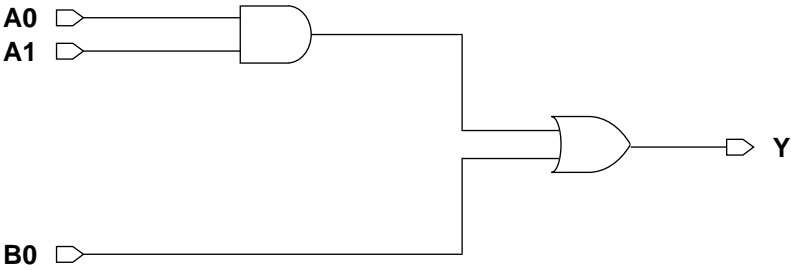
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0027	0.0032	0.0049	0.0091
A1	0.0030	0.0035	0.0054	0.0100
B0	0.0028	0.0032	0.0049	0.0089

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0010	0.0011	0.0015	0.0026
A1	0.0009	0.0010	0.0014	0.0025
B0	0.0011	0.0012	0.0015	0.0025

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→ Y	↑	0.0574	0.0638	0.0573	0.0561	6.8842	4.4642	2.8583	1.4561
A0	→ Y	↓	0.1225	0.1175	0.0972	0.0910	6.0859	4.0594	1.7515	0.8534
A1	→ Y	↑	0.0594	0.0657	0.0596	0.0586	6.8853	4.4644	2.8585	1.4562
A1	→ Y	↓	0.1298	0.1228	0.1034	0.0976	6.1044	4.0657	1.7561	0.8575
B0	→ Y	↑	0.0371	0.0387	0.0426	0.0400	6.7117	4.3612	2.8310	1.4425
B0	→ Y	↓	0.1151	0.1086	0.0914	0.0859	6.1052	4.0662	1.7563	0.8576

Cell Description

The AO22 cell provides the logical OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = (A0 \bullet A1) + (B0 \bullet B1)$$

Logic Symbol
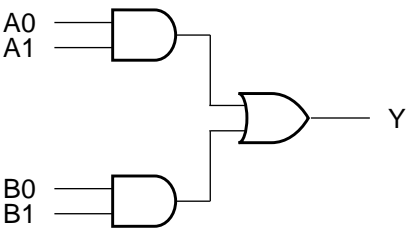
Function Table

A0	A1	B0	B1	Y
0	x	0	x	0
0	x	x	0	0
x	0	0	x	0
x	0	x	0	0
x	x	1	1	1
1	1	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
AO22XLADTH	2.52	2.24
AO22X1ADTH	2.52	2.24
AO22X2ADTH	2.52	2.52
AO22X4ADTH	2.52	2.80

Functional Schematic
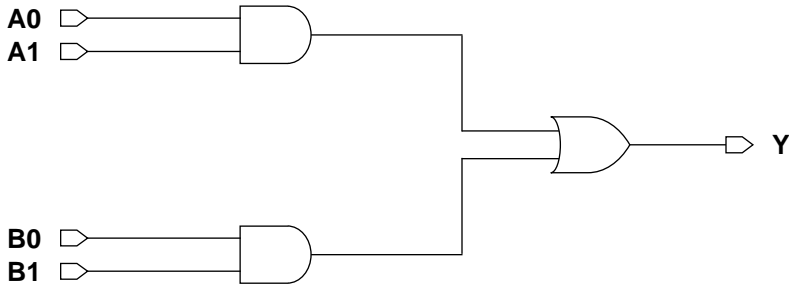
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0031	0.0034	0.0054	0.0095
A1	0.0035	0.0037	0.0060	0.0105
B0	0.0036	0.0037	0.0062	0.0110
B1	0.0039	0.0040	0.0067	0.0120

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0011	0.0011	0.0016	0.0027
A1	0.0012	0.0011	0.0017	0.0027
B0	0.0010	0.0010	0.0016	0.0026
B1	0.0009	0.0009	0.0015	0.0025

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0582	0.0592	0.0551	0.0541	6.9046	4.4015	2.8482	1.4505
A0	→	Y	↓	0.1298	0.1367	0.1060	0.0926	6.3518	4.2845	1.8129	0.8759
A1	→	Y	↑	0.0620	0.0628	0.0585	0.0570	6.9046	4.4017	2.8478	1.4503
A1	→	Y	↓	0.1434	0.1489	0.1156	0.1008	6.3874	4.2943	1.8204	0.8799
B0	→	Y	↑	0.0666	0.0703	0.0651	0.0646	7.0072	4.4669	2.8689	1.4607
B0	→	Y	↓	0.1514	0.1668	0.1264	0.1107	6.3629	4.2951	1.8170	0.8774
B1	→	Y	↑	0.0686	0.0722	0.0677	0.0673	7.0091	4.4674	2.8691	1.4608
B1	→	Y	↓	0.1591	0.1721	0.1323	0.1168	6.3887	4.2955	1.8207	0.8798

Cell Description

The AO2B2 cell provides the logical OR of two AND groups consisting of two inputs each: (A0,A1N) and (B0,B1). The output (Y) is represented by the logic equation:

$$Y = (A0 \bullet \overline{A1N}) + (B0 \bullet B1)$$

Logic Symbol

A0
A1N

B0
B1

Y
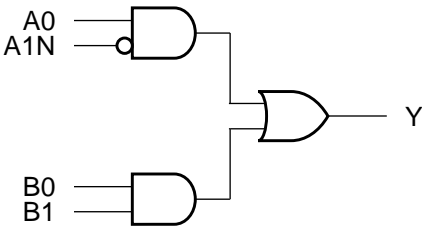
Function Table

A0	A1N	B0	B1	Y
1	0	x	x	1
x	x	1	1	1
0	x	0	x	0
x	1	0	x	0
0	x	x	0	0
x	1	x	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
AO2B2XLADTH	2.52	2.80
AO2B2X1ADTH	2.52	2.80
AO2B2X2ADTH	2.52	2.80
AO2B2X4ADTH	2.52	3.08

Functional Schematic

A0
A1N

B0
B1

Y
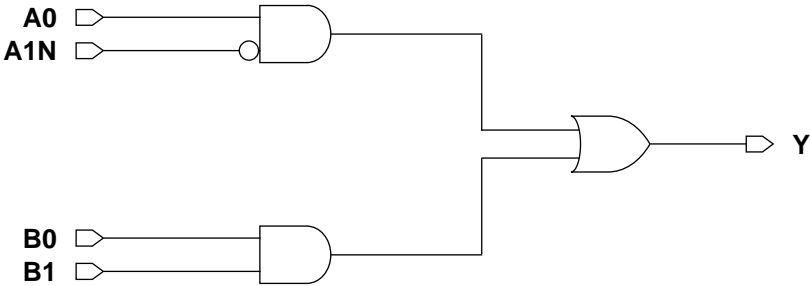
AC Power

Pin	Power (uW/MHz)			
	XL	X1	X2	X4
A0	0.0031	0.0035	0.0053	0.0095
A1N	0.0036	0.0041	0.0062	0.0109
B0	0.0036	0.0041	0.0063	0.0114
B1	0.0039	0.0044	0.0068	0.0123

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0008	0.0007	0.0011	0.0018
A1N	0.0009	0.0009	0.0012	0.0014
B0	0.0010	0.0010	0.0015	0.0027
B1	0.0009	0.0009	0.0014	0.0025

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	X1	X2	X4	XL	X1	X2	X4
A0	→	Y	↑	0.0616	0.0646	0.0587	0.0574	7.0389	4.5025	2.8700	1.4666
A0	→	Y	↓	0.1314	0.1496	0.1058	0.0958	6.5347	4.4294	1.8366	0.8917
A1N	→	Y	↑	0.1015	0.1048	0.0991	0.1031	7.0445	4.5046	2.8721	1.4674
A1N	→	Y	↓	0.1581	0.1763	0.1304	0.1265	6.5618	4.4427	1.8435	0.8953
B0	→	Y	↑	0.0714	0.0761	0.0698	0.0677	7.1608	4.5741	2.8949	1.4753
B0	→	Y	↓	0.1641	0.1829	0.1285	0.1158	6.5617	4.4465	1.8428	0.8931
B1	→	Y	↑	0.0733	0.0781	0.0721	0.0701	7.1603	4.5741	2.8947	1.4753
B1	→	Y	↓	0.1692	0.1876	0.1333	0.1214	6.5599	4.4418	1.8430	0.8954

Cell Description

The AO2B2B cell provides the logical OR of two AND groups consisting of two inputs each: (A0,A1N) and (B0,B1N). The output (Y) is represented by the logic equation:

$$Y = (A0 \bullet \overline{A1N}) + (B0 \bullet \overline{B1N})$$

Logic Symbol
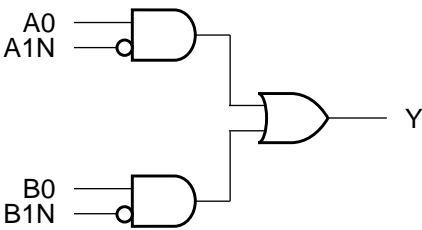
Function Table

A0	A1N	B0	B1N	Y
0	x	0	x	0
0	x	x	1	0
x	1	0	x	0
x	1	x	1	0
x	x	1	0	1
1	0	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
AO2B2BXLADTH	2.52	3.36
AO2B2BX1ADTH	2.52	3.36
AO2B2BX2ADTH	2.52	3.36
AO2B2BX4ADTH	2.52	3.92

Functional Schematic
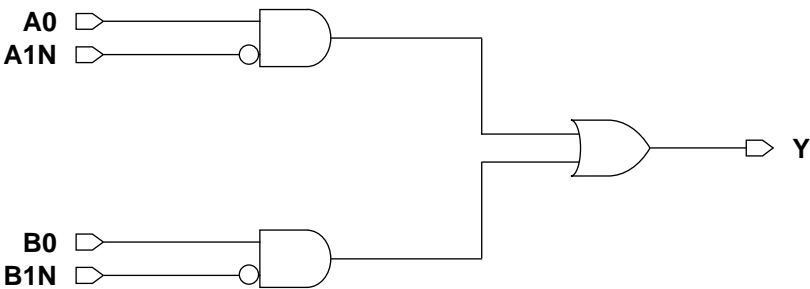
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0030	0.0035	0.0054	0.0095
A1N	0.0036	0.0041	0.0063	0.0109
B0	0.0036	0.0041	0.0063	0.0112
B1N	0.0043	0.0047	0.0070	0.0123

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0011	0.0011	0.0017	0.0027
A1N	0.0009	0.0009	0.0012	0.0013
B0	0.0010	0.0010	0.0016	0.0026
B1N	0.0011	0.0011	0.0013	0.0014

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0610	0.0658	0.0603	0.0575	7.0342	4.5114	2.8666	1.4706
A0	→	Y	↓	0.1301	0.1496	0.1069	0.0958	6.5210	4.4247	1.8384	0.8910
A1N	→	Y	↑	0.1010	0.1059	0.1004	0.1022	7.0399	4.5136	2.8687	1.4714
A1N	→	Y	↓	0.1566	0.1755	0.1309	0.1262	6.5450	4.4341	1.8434	0.8952
B0	→	Y	↑	0.0697	0.0743	0.0693	0.0669	7.1485	4.5664	2.8880	1.4790
B0	→	Y	↓	0.1626	0.1809	0.1288	0.1164	6.5362	4.4361	1.8421	0.8938
B1N	→	Y	↑	0.1087	0.1137	0.1077	0.1087	7.1469	4.5664	2.8874	1.4788
B1N	→	Y	↓	0.1846	0.2024	0.1493	0.1442	6.5426	4.4339	1.8435	0.8954

Cell Description

The AOI21 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + B0}$$

Logic Symbol
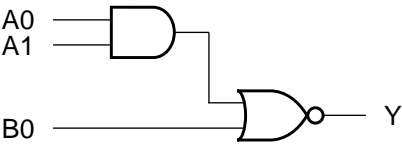
Function Table

A0	A1	B0	Y
0	x	0	1
x	0	0	1
x	x	1	0
1	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI21XLADTH	2.52	1.40
AOI21X1ADTH	2.52	1.40
AOI21X2ADTH	2.52	1.68
AOI21X3ADTH	2.52	2.52
AOI21X4ADTH	2.52	2.52
AOI21X6ADTH	2.52	3.64
AOI21X8ADTH	2.52	4.76

Functional Schematic
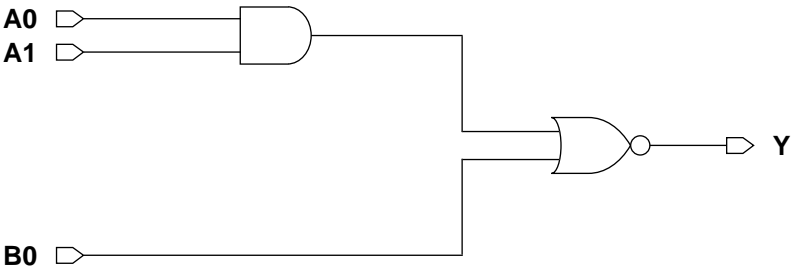
AC Power

Pin	Power (uW/MHz)						
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A0	0.0019	0.0027	0.0045	0.0071	0.0091	0.0133	0.0173
A1	0.0022	0.0031	0.0055	0.0084	0.0110	0.0163	0.0214
B0	0.0018	0.0024	0.0043	0.0066	0.0085	0.0126	0.0164

Pin Capacitance

Pin	Capacitance (pF)						
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A0	0.0012	0.0016	0.0026	0.0044	0.0055	0.0079	0.0102
A1	0.0011	0.0015	0.0025	0.0038	0.0048	0.0076	0.0103
B0	0.0014	0.0018	0.0028	0.0041	0.0052	0.0078	0.0102

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)						
				XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A0	$\rightarrow$	Y	$\uparrow$	0.0423	0.0365	0.0394	0.0409	0.0397	0.0396	0.0391
A0	$\rightarrow$	Y	$\downarrow$	0.0318	0.0307	0.0222	0.0226	0.0221	0.0216	0.0209
A1	$\rightarrow$	Y	$\uparrow$	0.0457	0.0411	0.0455	0.0479	0.0464	0.0471	0.0465
A1	$\rightarrow$	Y	$\downarrow$	0.0338	0.0331	0.0247	0.0244	0.0242	0.0240	0.0235
B0	$\rightarrow$	Y	$\uparrow$	0.0318	0.0302	0.0345	0.0359	0.0347	0.0351	0.0342
B0	$\rightarrow$	Y	$\downarrow$	0.0146	0.0144	0.0117	0.0118	0.0116	0.0115	0.0112

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)						
				XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A0	$\rightarrow$	Y	$\uparrow$	14.1697	9.2449	6.0565	4.1097	3.0764	2.1002	1.6060
A0	$\rightarrow$	Y	$\downarrow$	9.7032	6.8045	2.8832	1.9112	1.4429	0.9515	0.7088
A1	$\rightarrow$	Y	$\uparrow$	13.8630	9.3266	5.9831	4.1769	3.1179	2.1063	1.5892
A1	$\rightarrow$	Y	$\downarrow$	9.7028	6.8019	2.8827	1.9108	1.4425	0.9514	0.7087
B0	$\rightarrow$	Y	$\uparrow$	13.9929	9.3526	5.9973	4.1864	3.1248	2.1108	1.5927
B0	$\rightarrow$	Y	$\downarrow$	5.2459	3.6885	1.5463	1.0381	0.7883	0.5148	0.3870

Cell Description

The AOI211 cell provides the logical inverted OR of one AND group and two additional inputs. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + B0 + C0}$$

Logic Symbol

A0
A1

B0

C0

Y
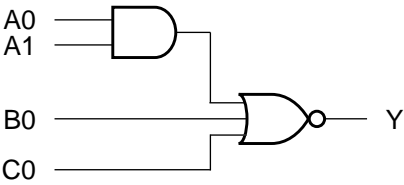
Function Table

A0	A1	B0	C0	Y
0	x	0	0	1
x	0	0	0	1
x	x	x	1	0
x	x	1	x	0
1	1	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI211XLADTH	2.52	1.68
AOI211X1ADTH	2.52	1.68
AOI211X2ADTH	2.52	1.68
AOI211X4ADTH	2.52	3.08

Functional Schematic

A0
A1

B0

Y

C0
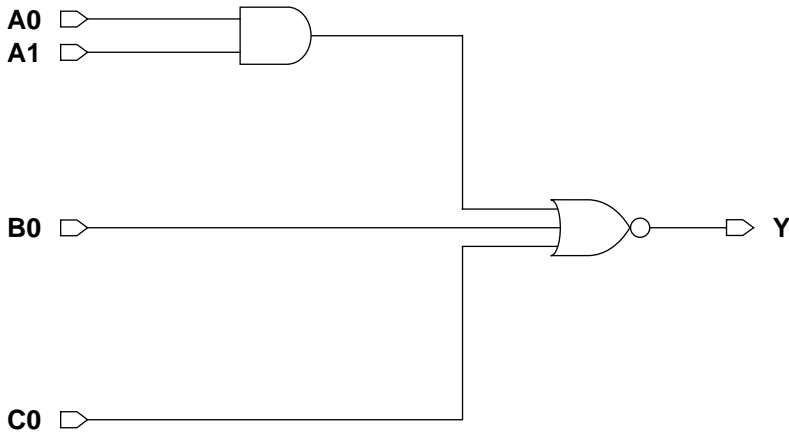
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0029	0.0038	0.0060	0.0121
A1	0.0032	0.0042	0.0069	0.0139
B0	0.0023	0.0029	0.0050	0.0099
C0	0.0026	0.0034	0.0058	0.0117

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0014	0.0018	0.0027	0.0055
A1	0.0012	0.0016	0.0025	0.0048
B0	0.0014	0.0018	0.0028	0.0052
C0	0.0014	0.0017	0.0027	0.0054

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0777	0.0683	0.0706	0.0715	21.9755	14.3303	9.3492	4.7465
A0	→	Y	↓	0.0356	0.0382	0.0258	0.0255	9.0326	6.8634	2.9110	1.4557
A1	→	Y	↑	0.0838	0.0736	0.0802	0.0820	21.7211	14.1672	9.2515	4.7887
A1	→	Y	↓	0.0374	0.0402	0.0282	0.0275	9.0303	6.8641	2.9113	1.4554
B0	→	Y	↑	0.0603	0.0495	0.0567	0.0553	21.8183	14.2077	9.2707	4.7973
B0	→	Y	↓	0.0178	0.0165	0.0132	0.0125	5.2148	3.6742	1.5731	0.7675
C0	→	Y	↑	0.0741	0.0635	0.0714	0.0727	21.7746	14.1874	9.2646	4.7951
C0	→	Y	↓	0.0198	0.0190	0.0148	0.0146	5.1542	3.6289	1.5536	0.7774

Cell Description

The AOI21B cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + \overline{B0N}}$$

Logic Symbol

A0
A1

B0N

Y
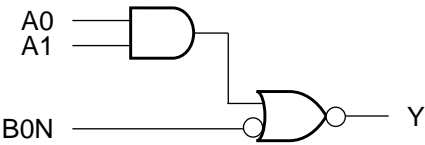
Function Table

A0	A1	B0N	Y
x	x	0	0
x	0	1	1
0	x	1	1
1	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI21BXLADTH	2.52	2.24
AOI21BX1ADTH	2.52	2.24
AOI21BX2ADTH	2.52	2.24
AOI21BX4ADTH	2.52	2.52

Functional Schematic

A0
A1

B0N

Y
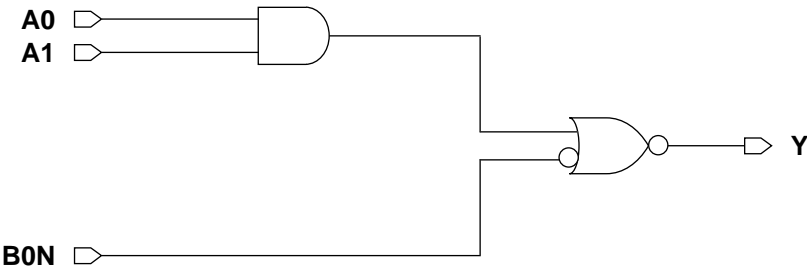
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0039	0.0042	0.0060	0.0094
A1	0.0036	0.0040	0.0056	0.0089
B0N	0.0022	0.0026	0.0040	0.0073

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0011	0.0011	0.0013	0.0014
A1	0.0011	0.0011	0.0013	0.0014
B0N	0.0010	0.0010	0.0014	0.0024

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→ Y	↑	0.1069	0.1100	0.1002	0.1039	7.0802	4.4808	2.8850	1.4825
A0	→ Y	↓	0.1035	0.1094	0.0930	0.0949	5.7463	3.9796	1.6982	0.8287
A1	→ Y	↑	0.0990	0.1020	0.0928	0.0969	7.0773	4.4797	2.8846	1.4824
A1	→ Y	↓	0.1013	0.1071	0.0907	0.0929	5.7463	3.9796	1.6981	0.8288
B0N	→ Y	↑	0.0528	0.0558	0.0531	0.0534	7.0707	4.4773	2.8847	1.4821
B0N	→ Y	↓	0.0683	0.0733	0.0622	0.0575	5.7643	3.9860	1.7015	0.8283

Cell Description

The AOI22 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + (B0 \bullet B1)}$$

Logic Symbol
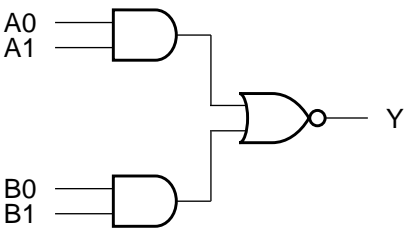
Function Table

A0	A1	B0	B1	Y
0	x	0	x	1
0	x	x	0	1
x	0	0	x	1
x	0	x	0	1
x	x	1	1	0
1	1	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI22XLADTH	2.52	1.68
AOI22X1ADTH	2.52	1.96
AOI22X2ADTH	2.52	1.96
AOI22X4ADTH	2.52	3.36

Functional Schematic

TSMC CLN90G HVT
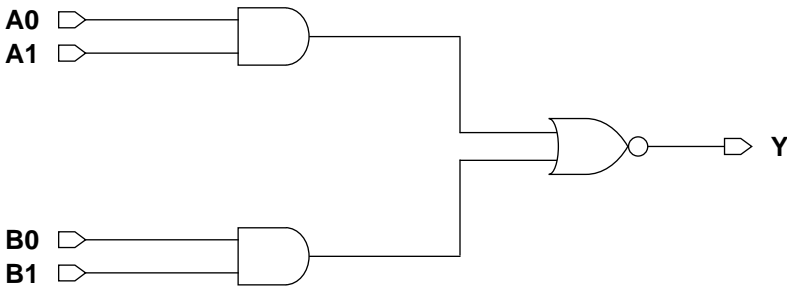
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0020	0.0028	0.0047	0.0092
A1	0.0023	0.0032	0.0057	0.0113
B0	0.0026	0.0038	0.0062	0.0123
B1	0.0029	0.0042	0.0072	0.0143

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0018	0.0028	0.0053
A1	0.0014	0.0018	0.0028	0.0055
B0	0.0013	0.0017	0.0026	0.0051
B1	0.0011	0.0016	0.0025	0.0053

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0352	0.0343	0.0384	0.0389	14.2268	9.4025	6.1066	3.1275
A0	→	Y	↓	0.0252	0.0255	0.0187	0.0182	9.5449	6.7268	2.8755	1.4157
A1	→	Y	↑	0.0412	0.0395	0.0454	0.0465	14.0293	9.3200	6.0567	3.0997
A1	→	Y	↓	0.0288	0.0291	0.0219	0.0212	9.5488	6.7278	2.8751	1.4154
B0	→	Y	↑	0.0594	0.0527	0.0558	0.0558	14.2355	9.4171	6.1325	3.1382
B0	→	Y	↓	0.0441	0.0428	0.0289	0.0280	9.6743	6.7653	2.8823	1.4227
B1	→	Y	↑	0.0624	0.0561	0.0615	0.0628	13.8492	9.2418	6.0179	3.0955
B1	→	Y	↓	0.0464	0.0452	0.0314	0.0308	9.6724	6.7642	2.8817	1.4225

Cell Description

The AOI221 cell provides the logical inverted OR of two AND groups and a third input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + (B0 \bullet B1) + C0}$$

Logic Symbol
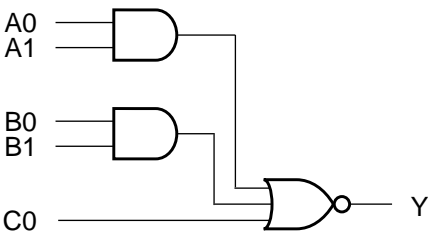
Function Table

A0	A1	B0	B1	C0	Y
0	x	0	x	0	1
0	x	x	0	0	1
x	0	0	x	0	1
x	0	x	0	0	1
x	x	x	x	1	0
x	x	1	1	x	0
1	1	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI221XLADTH	2.52	2.24
AOI221X1ADTH	2.52	2.52
AOI221X2ADTH	2.52	2.52
AOI221X4ADTH	2.52	4.48

Functional Schematic
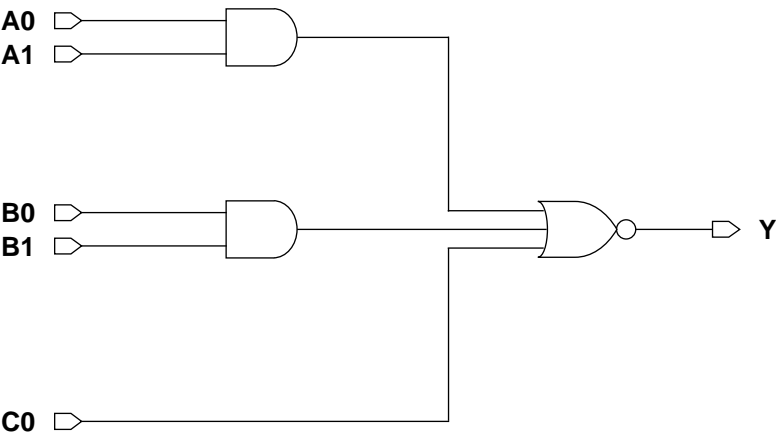
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0028	0.0039	0.0066	0.0121
A1	0.0030	0.0043	0.0075	0.0142
B0	0.0034	0.0049	0.0079	0.0149
B1	0.0037	0.0053	0.0089	0.0170
C0	0.0026	0.0035	0.0064	0.0119

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0016	0.0026	0.0049
A1	0.0013	0.0017	0.0026	0.0050
B0	0.0013	0.0016	0.0025	0.0049
B1	0.0012	0.0016	0.0025	0.0052
C0	0.0014	0.0018	0.0028	0.0052

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0817	0.0744	0.0829	0.0781	20.7828	13.9621	9.1134	4.7320
A0	→	Y	↓	0.0365	0.0358	0.0256	0.0233	9.4895	6.6526	2.8427	1.4045
A1	→	Y	↑	0.0898	0.0825	0.0942	0.0884	21.1099	14.0732	9.1839	4.6835
A1	→	Y	↓	0.0385	0.0385	0.0281	0.0257	9.4876	6.6519	2.8425	1.4044
B0	→	Y	↑	0.0972	0.0894	0.0963	0.0926	21.1205	14.0918	9.1934	4.7443
B0	→	Y	↓	0.0439	0.0449	0.0295	0.0271	9.9318	6.8986	2.9314	1.4546
B1	→	Y	↑	0.1042	0.0957	0.1070	0.1031	21.1039	14.0702	9.1836	4.6728
B1	→	Y	↓	0.0461	0.0469	0.0320	0.0299	9.9329	6.8974	2.9312	1.4545
C0	→	Y	↑	0.0590	0.0545	0.0682	0.0627	21.1818	14.1039	9.2007	4.6891
C0	→	Y	↓	0.0171	0.0167	0.0136	0.0125	5.2291	3.6603	1.5699	0.7743

Cell Description

The AOI222 cell provides the logical inverted OR of three AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + (B0 \bullet B1) + (C0 \bullet C1)}$$

Logic Symbol
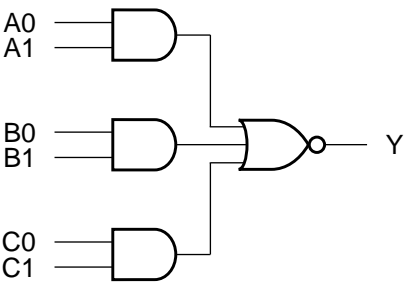
Function Table

A0	A1	B0	B1	C0	C1	Y
0	x	0	x	0	x	1
0	x	0	x	x	0	1
0	x	x	0	0	x	1
0	x	x	0	x	0	1
x	0	0	x	0	x	1
x	0	0	x	x	0	1
x	0	x	0	0	x	1
x	0	x	0	x	0	1
x	x	x	x	1	1	0
x	x	1	1	x	x	0
1	1	x	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI222XLADTH	2.52	2.52
AOI222X1ADTH	2.52	2.80
AOI222X2ADTH	2.52	2.80
AOI222X4ADTH	2.52	5.04

Functional Schematic
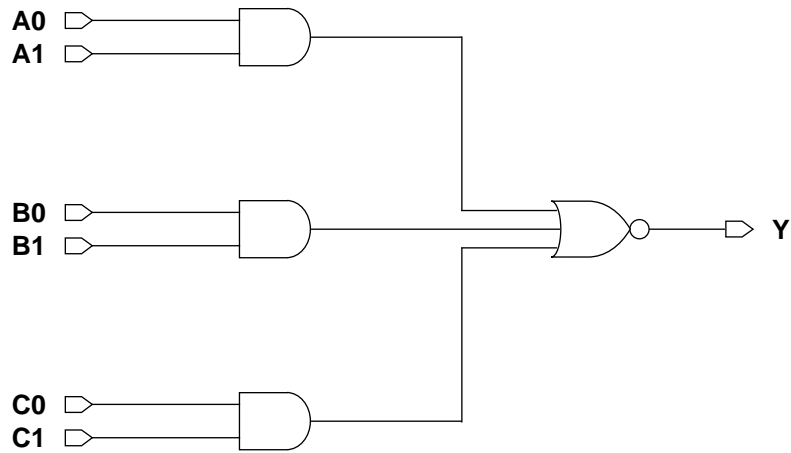
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0029	0.0039	0.0068	0.0129
A1	0.0032	0.0043	0.0078	0.0150
B0	0.0035	0.0049	0.0082	0.0157
B1	0.0038	0.0054	0.0091	0.0178
C0	0.0042	0.0060	0.0096	0.0186
C1	0.0045	0.0064	0.0106	0.0206

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0017	0.0027	0.0051
A1	0.0014	0.0018	0.0027	0.0055
B0	0.0013	0.0017	0.0027	0.0051
B1	0.0013	0.0017	0.0025	0.0053
C0	0.0012	0.0016	0.0026	0.0050
C1	0.0013	0.0017	0.0026	0.0053

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0619	0.0595	0.0711	0.0702	21.0794	14.0268	9.2009	4.7333
A0	→	Y	↓	0.0302	0.0300	0.0215	0.0206	9.5216	6.7097	2.8522	1.4159
A1	→	Y	↑	0.0718	0.0671	0.0821	0.0819	20.8406	13.9488	9.1436	4.7001
A1	→	Y	↓	0.0343	0.0335	0.0245	0.0235	9.5267	6.7100	2.8517	1.4157
B0	→	Y	↑	0.1115	0.0991	0.1084	0.1058	21.1426	14.0975	9.2605	4.7412
B0	→	Y	↓	0.0495	0.0476	0.0317	0.0303	9.4736	6.6403	2.8203	1.4051
B1	→	Y	↑	0.1168	0.1048	0.1173	0.1164	20.7332	13.8959	9.1386	4.7003
B1	→	Y	↓	0.0518	0.0500	0.0340	0.0328	9.4720	6.6396	2.8200	1.4050
C0	→	Y	↑	0.1249	0.1118	0.1205	0.1205	20.8449	13.9957	9.1491	4.7595
C0	→	Y	↓	0.0617	0.0600	0.0384	0.0365	9.8560	6.8789	2.9180	1.4479
C1	→	Y	↑	0.1322	0.1184	0.1312	0.1305	20.8370	13.9470	9.1444	4.6893
C1	→	Y	↓	0.0640	0.0627	0.0409	0.0393	9.8559	6.8783	2.9186	1.4482

Cell Description

The AOI2B1 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet \overline{A1N}) + B0}$$

Logic Symbol

A0
A1N

B0

Y
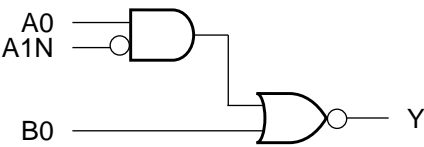
**Function Table**

A0	A1N	B0	Y
0	x	0	1
x	1	0	1
x	x	1	0
1	0	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI2B1XLADTH	2.52	1.96
AOI2B1X1ADTH	2.52	1.96
AOI2B1X2ADTH	2.52	2.24
AOI2B1X4ADTH	2.52	3.36

Functional Schematic

A0
A1N

B0

Y
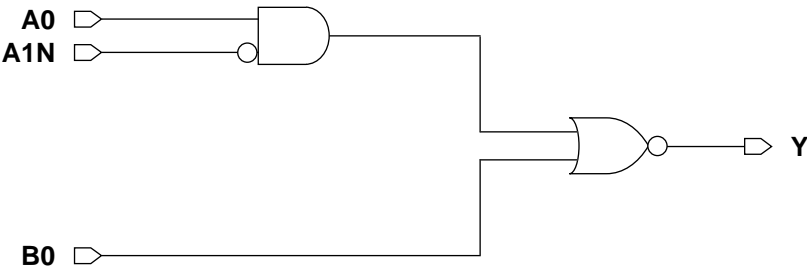
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0020	0.0027	0.0043	0.0088
A1N	0.0027	0.0033	0.0054	0.0113
B0	0.0018	0.0024	0.0042	0.0086

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0016	0.0027	0.0054
A1N	0.0011	0.0011	0.0014	0.0022
B0	0.0014	0.0018	0.0028	0.0052

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→ Y	↑	0.0409	0.0368	0.0392	0.0399	14.1741	9.2343	6.0557	3.0756
A0	→ Y	↓	0.0303	0.0303	0.0218	0.0219	9.4881	6.7007	2.8531	1.4447
A1N	→ Y	↑	0.0623	0.0610	0.0684	0.0711	13.9179	9.2485	5.9844	3.1280
A1N	→ Y	↓	0.0732	0.0778	0.0650	0.0636	9.5077	6.7114	2.8600	1.4482
B0	→ Y	↑	0.0332	0.0299	0.0341	0.0347	13.9911	9.2741	5.9984	3.1342
B0	→ Y	↓	0.0147	0.0143	0.0118	0.0116	5.2022	3.6680	1.5749	0.7880

Cell Description

The AOI2BB1 cell provides the logical inverted OR of one AND group of two inverted inputs (A0N,A1N) and an additional non-inverted input (B0). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} \bullet \overline{A1N}) + B0}$$

Logic Symbol
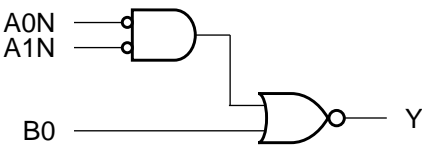
Function Table

A0N	A1N	B0	Y
1	x	0	1
x	1	0	1
x	x	1	0
0	0	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI2BB1XLADTH	2.52	1.68
AOI2BB1X1ADTH	2.52	1.68
AOI2BB1X2ADTH	2.52	1.68
AOI2BB1X4ADTH	2.52	2.52

Functional Schematic

TSMC CLN90G HVT
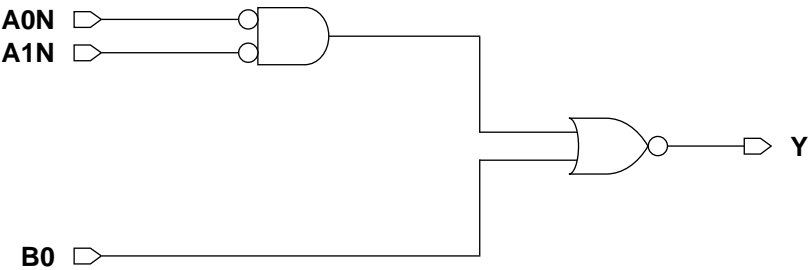
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0N	0.0027	0.0032	0.0045	0.0080
A1N	0.0031	0.0035	0.0049	0.0089
B0	0.0017	0.0023	0.0038	0.0078

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0N	0.0012	0.0012	0.0015	0.0026
A1N	0.0012	0.0012	0.0015	0.0025
B0	0.0012	0.0016	0.0026	0.0054

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0N	→ Y	↑	0.0513	0.0505	0.0534	0.0500	14.4637	9.2740	6.0124	3.0871
A0N	→ Y	↓	0.0799	0.0901	0.0880	0.0810	5.7645	4.0001	1.7373	0.8511
A1N	→ Y	↑	0.0534	0.0528	0.0556	0.0523	14.4808	9.2821	6.0167	3.0887
A1N	→ Y	↓	0.0867	0.0970	0.0944	0.0873	5.7634	3.9991	1.7367	0.8509
B0	→ Y	↑	0.0338	0.0313	0.0340	0.0345	14.4055	9.2545	6.0025	3.0835
B0	→ Y	↓	0.0158	0.0162	0.0131	0.0129	5.1574	3.6701	1.5793	0.7823

Cell Description

The AOI2BB2 cell provides the logical inverted OR of one AND group of two inverted inputs (A0N,A1N) and one AND group of two non-inverted inputs (B0,B1). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} \bullet \overline{A1N}) + (B0 \bullet B1)}$$

Logic Symbol
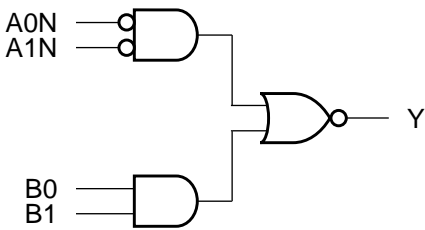
Function Table

A0N	A1N	B0	B1	Y
1	x	0	x	1
1	x	x	0	1
x	1	0	x	1
x	1	x	0	1
x	x	1	1	0
0	0	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI2BB2XLADTH	2.52	2.24
AOI2BB2X1ADTH	2.52	2.24
AOI2BB2X2ADTH	2.52	2.24
AOI2BB2X4ADTH	2.52	3.64

Functional Schematic
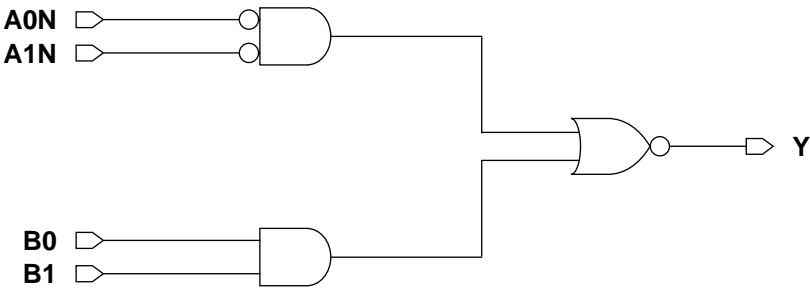
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0N	0.0029	0.0032	0.0045	0.0084
A1N	0.0031	0.0035	0.0048	0.0088
B0	0.0021	0.0028	0.0044	0.0086
B1	0.0024	0.0032	0.0054	0.0107

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0N	0.0014	0.0014	0.0016	0.0025
A1N	0.0011	0.0011	0.0013	0.0025
B0	0.0013	0.0017	0.0026	0.0051
B1	0.0012	0.0016	0.0026	0.0052

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0N	→	Y	↑	0.0575	0.0553	0.0601	0.0567	14.0868	9.2049	6.0331	3.0880
A0N	→	Y	↓	0.0818	0.0903	0.0879	0.0783	5.6976	3.9317	1.7274	0.8291
A1N	→	Y	↑	0.0598	0.0579	0.0632	0.0591	14.1052	9.2136	6.0368	3.0889
A1N	→	Y	↓	0.0850	0.0934	0.0919	0.0852	5.6977	3.9320	1.7269	0.8290
B0	→	Y	↑	0.0431	0.0393	0.0412	0.0403	14.2733	9.2914	6.1012	3.1231
B0	→	Y	↓	0.0310	0.0308	0.0219	0.0209	9.5331	6.6941	2.8686	1.4191
B1	→	Y	↑	0.0464	0.0425	0.0473	0.0472	14.0060	9.1174	5.9983	3.0788
B1	→	Y	↓	0.0326	0.0326	0.0242	0.0237	9.5300	6.6923	2.8682	1.4189

Cell Description

The AOI31 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1 \bullet A2) + B0}$$

Logic Symbol
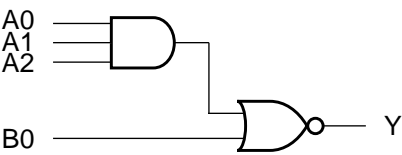
Function Table

A0	A1	A2	B0	Y
0	x	x	0	1
x	0	x	0	1
x	x	0	0	1
x	x	x	1	0
1	1	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI31XLADTH	2.52	1.68
AOI31X1ADTH	2.52	1.68
AOI31X2ADTH	2.52	1.96
AOI31X4ADTH	2.52	3.36

Functional Schematic

TSMC CLN90G HVT
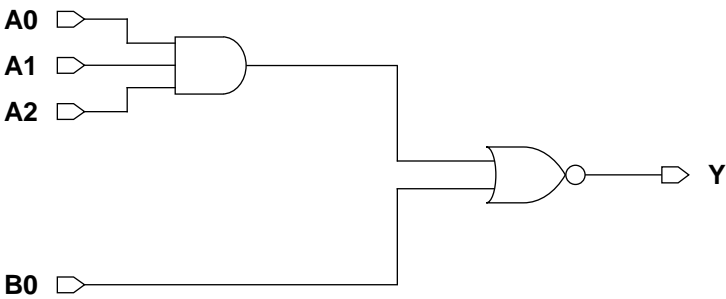
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0021	0.0029	0.0048	0.0098
A1	0.0025	0.0034	0.0058	0.0117
A2	0.0028	0.0038	0.0068	0.0135
B0	0.0021	0.0028	0.0053	0.0107

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0012	0.0017	0.0027	0.0056
A1	0.0012	0.0016	0.0026	0.0053
A2	0.0012	0.0015	0.0025	0.0047
B0	0.0013	0.0018	0.0028	0.0052

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0431	0.0395	0.0430	0.0436	14.2821	9.3049	6.1032	3.0926
A0	→	Y	↓	0.0437	0.0443	0.0307	0.0310	13.4891	9.5068	3.9901	2.0119
A1	→	Y	↑	0.0483	0.0453	0.0501	0.0518	14.3040	9.5012	6.1174	3.1358
A1	→	Y	↓	0.0485	0.0493	0.0353	0.0357	13.4850	9.5021	3.9894	2.0115
A2	→	Y	↑	0.0511	0.0481	0.0555	0.0580	13.9849	9.2814	6.0104	3.1652
A2	→	Y	↓	0.0504	0.0514	0.0378	0.0375	13.4830	9.5044	3.9894	2.0115
B0	→	Y	↑	0.0365	0.0330	0.0409	0.0421	14.1864	9.4457	6.0660	3.1724
B0	→	Y	↓	0.0144	0.0142	0.0120	0.0116	5.2342	3.6788	1.5761	0.7750

Cell Description

The AOI32 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1 \bullet A2) + (B0 \bullet B1)}$$

Logic Symbol
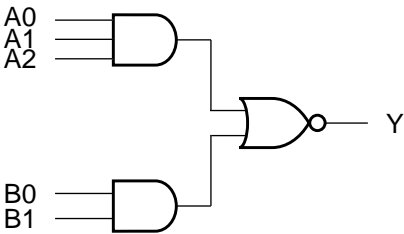
**Function Table**

A0	A1	A2	B0	B1	Y
0	x	x	0	x	1
0	x	x	x	0	1
x	0	x	0	x	1
x	0	x	x	0	1
x	x	0	0	x	1
x	x	0	x	0	1
x	x	x	1	1	0
1	1	1	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI32XLADTH	2.52	1.96
AOI32X1ADTH	2.52	2.24
AOI32X2ADTH	2.52	2.24
AOI32X4ADTH	2.52	4.20

Functional Schematic
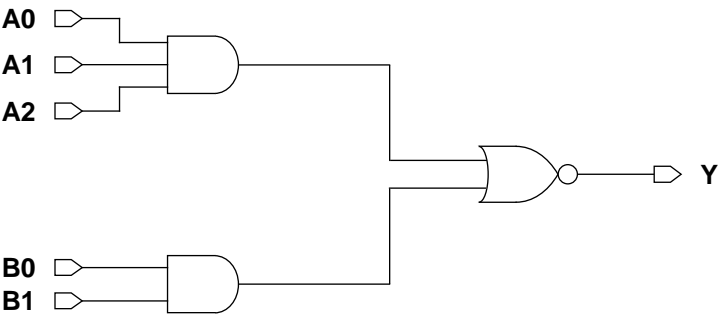
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0027	0.0040	0.0064	0.0128
A1	0.0030	0.0044	0.0074	0.0150
A2	0.0033	0.0048	0.0084	0.0170
B0	0.0023	0.0032	0.0057	0.0115
B1	0.0027	0.0037	0.0067	0.0135

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0016	0.0026	0.0049
A1	0.0012	0.0016	0.0025	0.0054
A2	0.0012	0.0015	0.0025	0.0054
B0	0.0013	0.0018	0.0028	0.0052
B1	0.0014	0.0018	0.0028	0.0055

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0619	0.0551	0.0584	0.0601	14.3118	9.5592	6.1903	3.1809
A0	→	Y	↓	0.0631	0.0609	0.0397	0.0391	13.4517	9.4010	4.0160	1.9794
A1	→	Y	↑	0.0660	0.0596	0.0658	0.0682	14.2491	9.5479	6.1693	3.1584
A1	→	Y	↓	0.0672	0.0657	0.0447	0.0446	13.4460	9.3994	4.0157	1.9793
A2	→	Y	↑	0.0687	0.0624	0.0710	0.0742	13.9433	9.3638	6.0506	3.1230
A2	→	Y	↓	0.0694	0.0680	0.0472	0.0474	13.4482	9.3997	4.0156	1.9793
B0	→	Y	↑	0.0407	0.0387	0.0451	0.0471	14.3030	9.5758	6.1747	3.1649
B0	→	Y	↓	0.0252	0.0254	0.0187	0.0185	9.5120	6.7117	2.8691	1.4106
B1	→	Y	↑	0.0469	0.0435	0.0523	0.0545	14.0214	9.3831	6.1091	3.1275
B1	→	Y	↓	0.0292	0.0290	0.0218	0.0214	9.5189	6.7124	2.8687	1.4103

Cell Description

The AOI33 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1 \bullet A2) + (B0 \bullet B1 \bullet B2)}$$

Logic Symbol
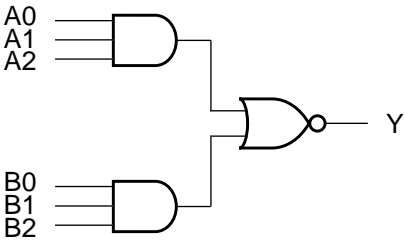
Function Table

A0	A1	A2	B0	B1	B2	Y
0	x	x	0	x	x	1
0	x	x	x	0	x	1
0	x	x	x	x	0	1
x	0	x	0	x	x	1
x	0	x	x	0	x	1
x	0	x	x	x	0	1
x	x	0	0	x	x	1
x	x	0	x	0	x	1
x	x	0	x	x	0	1
x	x	x	1	1	1	0
1	1	1	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI33XLADTH	2.52	2.52
AOI33X1ADTH	2.52	2.52
AOI33X2ADTH	2.52	2.52
AOI33X4ADTH	2.52	4.76

Functional Schematic
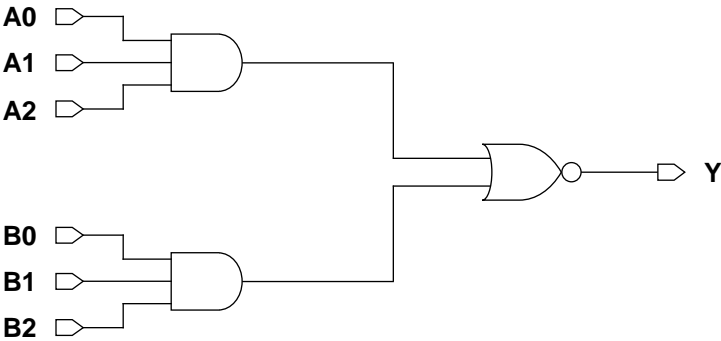
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0027	0.0036	0.0063	0.0123
A1	0.0030	0.0040	0.0073	0.0145
A2	0.0033	0.0045	0.0083	0.0165
B0	0.0036	0.0049	0.0082	0.0162
B1	0.0039	0.0054	0.0091	0.0183
B2	0.0042	0.0058	0.0101	0.0203

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0018	0.0028	0.0050
A1	0.0014	0.0018	0.0027	0.0055
A2	0.0014	0.0018	0.0028	0.0057
B0	0.0013	0.0017	0.0026	0.0049
B1	0.0013	0.0016	0.0026	0.0053
B2	0.0012	0.0016	0.0025	0.0054

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→ Y	↑	0.0507	0.0451	0.0520	0.0510	14.6275	9.5503	6.2098	3.1617
A0	→ Y	↓	0.0401	0.0393	0.0279	0.0260	12.9519	9.1593	3.9957	1.9745
A1	→ Y	↑	0.0568	0.0504	0.0597	0.0600	14.5785	9.5327	6.1909	3.1549
A1	→ Y	↓	0.0462	0.0451	0.0332	0.0318	12.9516	9.1579	3.9947	1.9743
A2	→ Y	↑	0.0624	0.0550	0.0662	0.0672	14.3960	9.4170	6.1174	3.1313
A2	→ Y	↓	0.0501	0.0485	0.0363	0.0347	12.9579	9.1597	3.9954	1.9746
B0	→ Y	↑	0.0775	0.0700	0.0752	0.0761	14.6395	9.5710	6.2199	3.1794
B0	→ Y	↓	0.0763	0.0768	0.0497	0.0485	13.3166	9.3961	4.0033	1.9803
B1	→ Y	↑	0.0822	0.0746	0.0825	0.0843	14.5685	9.5258	6.1894	3.1639
B1	→ Y	↓	0.0808	0.0816	0.0547	0.0539	13.3150	9.3960	4.0026	1.9801
B2	→ Y	↑	0.0851	0.0772	0.0874	0.0902	14.2938	9.3301	6.0744	3.1287
B2	→ Y	↓	0.0831	0.0839	0.0572	0.0567	13.3150	9.3963	4.0029	1.9802

Cell Description

The booth encoder block, BENC, cell performs a 2bit multiplier recoding per a modified Booth's algorithm. Each BENC cell examines 3 bits of the multiplier (M0,M1,M2) and generates the appropriate control signals to adjust the multiplicand for subsequent partial product reduction. The outputs (S,A,X2) are represented by the logic equations:

$A = M2 + (\overline{M0} \bullet \overline{M1})$

$S = \overline{M2} + (M0 \bullet M1)$

$X2 = \overline{M1 \oplus M0}$

Logic Symbol
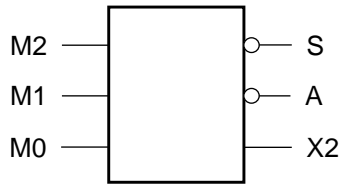
Function Table

M2	M1	M0	X2	A	S
0	0	0	1	1	1
0	0	1	0	0	1
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
BENCX1ADTH	2.52	11.20
BENCX2ADTH	2.52	14.00
BENCX4ADTH	2.52	21.84

Functional Schematic
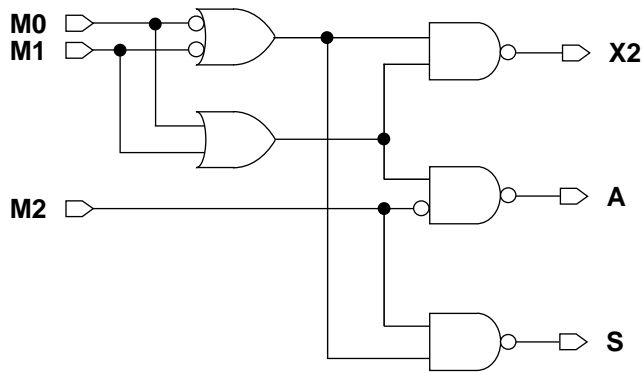
AC Power

Pin	Power (uW/MHz)		
	X1	**X2**	**X4**
M2	0.0173	0.0314	0.0598
M1	0.0181	0.0341	0.0638
M0	0.0192	0.0371	0.0668

Pin Capacitance

Pin	Capacitance (pF)		
	X1	**X2**	**X4**
M2	0.0033	0.0041	0.0058
M1	0.0043	0.0062	0.0106
M0	0.0039	0.0062	0.0092

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)			K_{load} (ns/pF)		
				X1	**X2**	**X4**	**X1**	**X2**	**X4**
M2	→	A	↑	0.1407	0.1386	0.1355	1.7290	0.7753	0.3954
M2	→	A	↓	0.1480	0.1379	0.1551	1.1590	0.4920	0.2480
M1	→	A	↑	0.1393	0.1300	0.1205	1.7263	0.7731	0.3946
M1	→	A	↓	0.1250	0.1079	0.1178	1.1589	0.4920	0.2478
M0	→	A	↑	0.1366	0.1260	0.1138	1.7253	0.7729	0.3946
M0	→	A	↓	0.1202	0.1023	0.1110	1.1567	0.4908	0.2476
M2	→	S	↑	0.1286	0.1174	0.1088	1.7236	0.7770	0.3951
M2	→	S	↓	0.1165	0.0955	0.1002	1.1597	0.4946	0.2467
M1	→	S	↑	0.1822	0.1628	0.1512	1.7217	0.7752	0.3945
M1	→	S	↓	0.1948	0.1682	0.1571	1.1629	0.4957	0.2472
M0	→	S	↑	0.1718	0.1425	0.1336	1.7207	0.7747	0.3945
M0	→	S	↓	0.1717	0.1339	0.1447	1.1597	0.4942	0.2473
M1	→	X2	↑	0.1287	0.1204	0.1245	1.7224	0.7898	0.4031
M1	→	X2	↓	0.1422	0.1354	0.1228	1.1501	0.4934	0.2551
M0	→	X2	↑	0.1617	0.1442	0.1412	1.7222	0.7897	0.4031
M0	→	X2	↓	0.1580	0.1421	0.1462	1.1500	0.4937	0.2558

Cell Description

The BMX cell performs the shifting and 2's complement inversion of the multiplicand bits (M1,M0) based on the recode control signals (X2,A,S) from the booth encoder block cell. The partial product output (PP) is represented by the logic equation:

$$PP = X2\bullet((M0\bullet\overline{A}) + (\overline{M0}\bullet\overline{S})) + \overline{X2}\bullet((M1\bullet\overline{A}) + (\overline{M1}\bullet\overline{S}))$$

Logic Symbol

Function Table

X2	A	S	M0	M1	PP
0	0	0	x	x	x
0	0	1	x	0	0
0	0	1	x	1	1
0	1	0	x	0	1
0	1	0	x	1	0
0	1	1	x	x	0
1	0	0	x	x	x
1	0	1	0	x	0
1	0	1	1	x	1
1	1	0	0	x	1
1	1	0	1	x	0
1	1	1	x	x	0
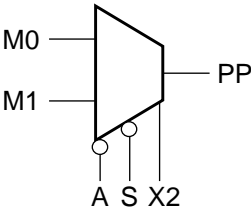
Cell Size

Drive Strength	Height (um)	Width (um)
BMXX2ADTH	2.52	7.56
BMXX4ADTH	2.52	9.80

Functional Schematic
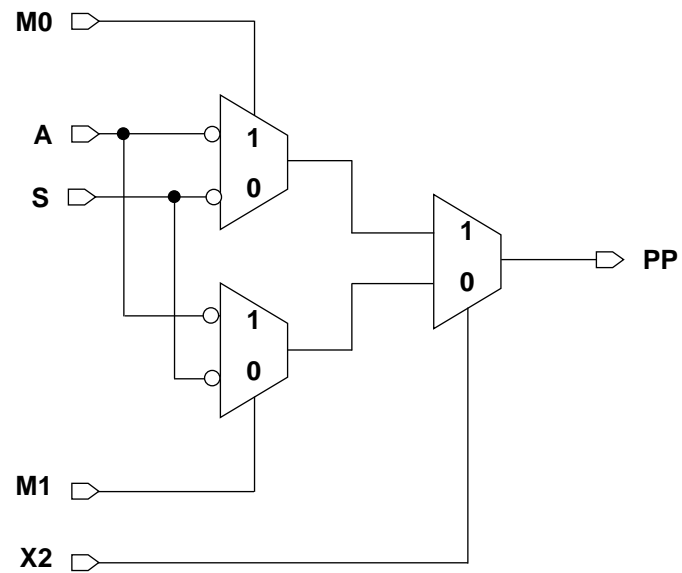
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
X2	0.0080	0.0151
M0	0.0125	0.0211
A	0.0172	0.0303
S	0.0154	0.0273
M1	0.0105	0.0188

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
X2	0.0023	0.0037
M0	0.0033	0.0036
A	0.0023	0.0046
S	0.0024	0.0045
M1	0.0028	0.0037

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
X2	→	PP	↑	0.0823	0.0802	2.8517	1.4613
X2	→	PP	↓	0.0771	0.0743	1.7617	0.8725
M0	→	PP	↑	0.1309	0.1228	2.8569	1.4614
M0	→	PP	↓	0.1536	0.1510	1.7641	0.8735
A	→	PP	↑	0.1589	0.1422	2.8590	1.4633
A	→	PP	↓	0.1415	0.1285	1.7647	0.8740
S	→	PP	↑	0.1515	0.1384	2.8589	1.4635
S	→	PP	↓	0.1428	0.1302	1.7654	0.8741
M1	→	PP	↑	0.1232	0.1228	2.8549	1.4627
M1	→	PP	↓	0.1433	0.1452	1.7649	0.8704

Cell Description

The BMXI cell performs the shifting and 2's complement inversion of the multiplicand bits (M1,M0) based on the recode control signals (X2,A,S) from the booth encoder block cell. The inverted partial product output (PPN) is represented by the logic equation:

$$PPN = \overline{X2\bullet((M0\bullet\overline{A})+(\overline{M0}\bullet\overline{S}))+\overline{X2}\bullet((M1\bullet\overline{A})+(\overline{M1}\bullet\overline{S}))}$$

Logic Symbol

Function Table

X2	A	S	M0	M1	PPN
0	0	0	x	x	x
0	0	1	x	0	1
0	0	1	x	1	0
0	1	0	x	0	0
0	1	0	x	1	1
0	1	1	x	x	1
1	0	0	x	x	x
1	0	1	0	x	1
1	0	1	1	x	0
1	1	0	0	x	0
1	1	0	1	x	1
1	1	1	x	x	1
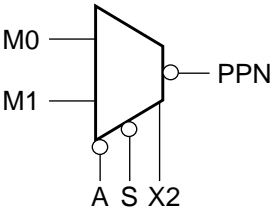
Cell Size

Drive Strength	Height (um)	Width (um)
BMXIX2ADTH	2.52	6.72
BMXIX4ADTH	2.52	10.08

Functional Schematic
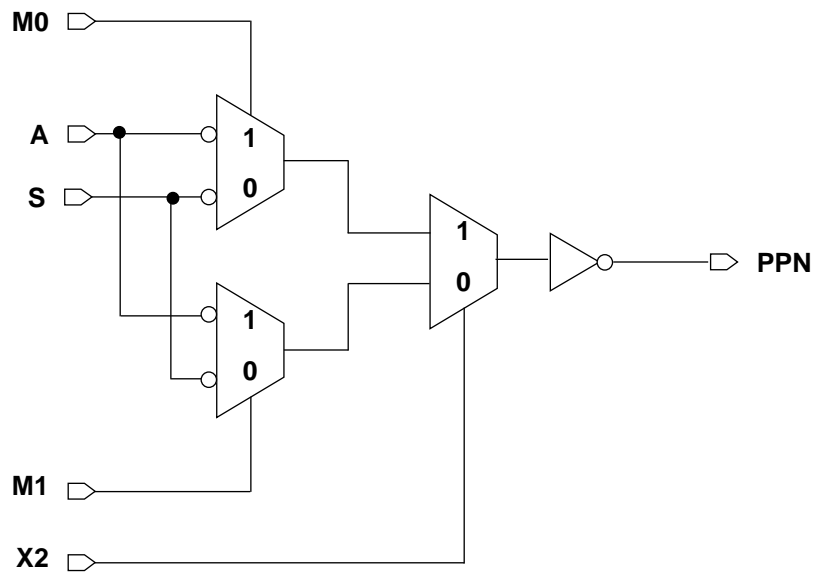
AC Power

Pin	Power (uW/MHz)	
	X2	**X4**
X2	0.0070	0.0130
M0	0.0096	0.0173
A	0.0151	0.0274
S	0.0129	0.0234
M1	0.0087	0.0162

Pin Capacitance

Pin	Capacitance (pF)	
	X2	**X4**
X2	0.0031	0.0053
M0	0.0038	0.0060
A	0.0026	0.0050
S	0.0028	0.0050
M1	0.0032	0.0054

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)		K_{load} (ns/pF)	
				X2	**X4**	**X2**	**X4**
X2	→	PPN	↑	0.0899	0.0918	2.8897	1.4795
X2	→	PPN	↓	0.0933	0.0979	1.9364	0.9598
M0	→	PPN	↑	0.1161	0.1153	2.8927	1.4802
M0	→	PPN	↓	0.1300	0.1268	1.9484	0.9621
A	→	PPN	↑	0.1021	0.0971	2.8936	1.4812
A	→	PPN	↓	0.1576	0.1459	1.9722	0.9703
S	→	PPN	↑	0.1058	0.1003	2.8950	1.4815
S	→	PPN	↓	0.1479	0.1385	1.9461	0.9710
M1	→	PPN	↑	0.1137	0.1144	2.8916	1.4802
M1	→	PPN	↓	0.1229	0.1202	1.9282	0.9618

Cell Description

The BUF cell provides the logical buffer of a single input (A). The output (Y) is represented by the logic equation:

Y = A

Logic Symbol

A $\longrightarrow$ Y

Function Table

A	Y
0	0
1	1
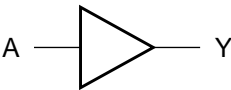
Cell Size

Drive Strength	Height (um)	Width (um)
BUFX2ADTH	2.52	1.12
BUFX3ADTH	2.52	1.40
BUFX4ADTH	2.52	1.68
BUFX5ADTH	2.52	1.96
BUFX6ADTH	2.52	2.24
BUFX8ADTH	2.52	2.52
BUFX10ADTH	2.52	3.08
BUFX12ADTH	2.52	3.64
BUFX14ADTH	2.52	4.20
BUFX16ADTH	2.52	4.48
BUFX18ADTH	2.52	5.04
BUFX20ADTH	2.52	5.60

Functional Schematic

A ▷—▷o—▷o—▷ Y

AC Power

Pin	Power (uW/MHz)							
	X2	**X3**	**X4**	**X5**	**X6**	**X8**	**X10**	**X12**
A	0.0038	0.0053	0.0069	0.0090	0.0104	0.0133	0.0165	0.0199

AC Power (Cont'd.)

Pin	Power (uW/MHz)			
	X14	**X16**	**X18**	**X20**
A	0.0232	0.0259	0.0296	0.0325

Pin Capacitance

Pin	Capacitance (pF)							
	X2	**X3**	**X4**	**X5**	**X6**	**X8**	**X10**	**X12**
A	0.0014	0.0018	0.0024	0.0028	0.0036	0.0045	0.0053	0.0065

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)			
	X14	**X16**	**X18**	**X20**
A	0.0075	0.0080	0.0096	0.0105

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X2	**X3**	**X4**	**X5**	**X6**	**X8**	**X10**	**X12**
A → Y ↑	0.0375	0.0361	0.0354	0.0368	0.0345	0.0340	0.0335	0.0343
A → Y ↓	0.0527	0.0502	0.0491	0.0506	0.0483	0.0476	0.0471	0.0485

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)			
	X14	**X16**	**X18**	**X20**
A → Y ↑	0.0343	0.0347	0.0339	0.0335
A → Y ↓	0.0479	0.0500	0.0475	0.0477

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X2	**X3**	**X4**	**X5**	**X6**	**X8**	**X10**	**X12**
A → Y ↑	2.8403	1.9659	1.4608	1.2006	0.9865	0.7460	0.6053	0.5034
A → Y ↓	1.6548	1.0749	0.8041	0.6483	0.5387	0.4019	0.3209	0.2673

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)			
	X14	**X16**	**X18**	**X20**
A → Y ↑	0.4377	0.3837	0.3423	0.3085
A → Y ↓	0.2292	0.2005	0.1780	0.1598

Cell Description

The CLKAND2 cell provides the logical AND of two inputs (A,B). The output (Y) is represented by the logic equation:

$Y = A \bullet B$

Logic Symbol

A ─────┐
) ─── Y
B ─────┘
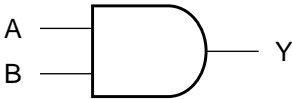
Function Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
CLKAND2X2ADTH	2.52	1.40
CLKAND2X3ADTH	2.52	1.68
CLKAND2X4ADTH	2.52	1.96
CLKAND2X6ADTH	2.52	2.24
CLKAND2X8ADTH	2.52	3.36
CLKAND2X12ADTH	2.52	4.20

Functional Schematic
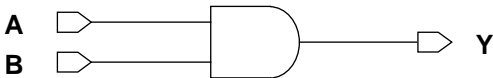
AC Power

Pin	Power (uW/MHz)					
	X2	**X3**	**X4**	**X6**	**X8**	**X12**
A	0.0034	0.0048	0.0060	0.0088	0.0115	0.0163
B	0.0038	0.0053	0.0066	0.0096	0.0126	0.0180

Pin Capacitance

Pin	Capacitance (pF)					
	X2	**X3**	**X4**	**X6**	**X8**	**X12**
A	0.0013	0.0017	0.0020	0.0026	0.0038	0.0050
B	0.0013	0.0018	0.0021	0.0027	0.0040	0.0053

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)					
				X2	**X3**	**X4**	**X6**	**X8**	**X12**
A	→	Y	↑	0.0624	0.0645	0.0618	0.0597	0.0639	0.0571
A	→	Y	↓	0.0554	0.0553	0.0516	0.0566	0.0526	0.0568
B	→	Y	↑	0.0643	0.0677	0.0651	0.0626	0.0669	0.0600
B	→	Y	↓	0.0596	0.0605	0.0558	0.0614	0.0544	0.0592

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)					
				X2	**X3**	**X4**	**X6**	**X8**	**X12**
A	→	Y	↑	2.8768	1.9817	1.4853	1.0052	0.7656	0.5110
A	→	Y	↓	3.2973	2.2597	1.6193	1.0778	0.8036	0.5349
B	→	Y	↑	2.8766	1.9820	1.4850	1.0050	0.7656	0.5112
B	→	Y	↓	3.3035	2.2648	1.6219	1.0802	0.8037	0.5354

Cell Description

The CLKBUF cell provides the logical buffer of a single input (A), with balanced delays for clock signals. The output (Y) is represented by the logic equation:

$Y = A$

Logic Symbol

A ————▷———— Y

Function Table

A	Y
0	0
1	1
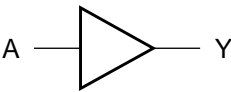
Cell Size

Drive Strength	Height (um)	Width (um)
CLKBUFX1ADTH	2.52	1.12
CLKBUFX2ADTH	2.52	1.12
CLKBUFX3ADTH	2.52	1.40
CLKBUFX4ADTH	2.52	1.40
CLKBUFX6ADTH	2.52	1.96
CLKBUFX8ADTH	2.52	2.52
CLKBUFX12ADTH	2.52	3.36
CLKBUFX16ADTH	2.52	3.92
CLKBUFX20ADTH	2.52	5.04
CLKBUFX24ADTH	2.52	5.60
CLKBUFX32ADTH	2.52	6.72
CLKBUFX40ADTH	2.52	8.12

Functional Schematic

A ▷———▷o———▷o———▷ Y

AC Power

Pin	Power (uW/MHz)							
	X1	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**
A	0.0030	0.0037	0.0044	0.0052	0.0077	0.0100	0.0144	0.0188

AC Power (Cont'd.)

Pin	Power (uW/MHz)			
	X20	**X24**	**X32**	**X40**
A	0.0239	0.0285	0.0373	0.0465

Pin Capacitance

Pin	Capacitance (pF)							
	X1	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**
A	0.0017	0.0017	0.0016	0.0016	0.0022	0.0030	0.0041	0.0052

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)			
	X20	**X24**	**X32**	**X40**
A	0.0067	0.0079	0.0099	0.0125

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X1	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**
A → Y ↑	0.0387	0.0413	0.0487	0.0527	0.0527	0.0519	0.0506	0.0493
A → Y ↓	0.0392	0.0428	0.0487	0.0543	0.0531	0.0518	0.0509	0.0502

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)			
	X20	**X24**	**X32**	**X40**
A → Y ↑	0.0501	0.0495	0.0488	0.0491
A → Y ↓	0.0510	0.0508	0.0507	0.0508

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X1	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**
A → Y ↑	4.7904	2.8514	1.9725	1.4634	0.9926	0.7562	0.5055	0.3788
A → Y ↓	5.2513	3.2909	2.1370	1.6376	1.1081	0.8120	0.5484	0.4102

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)			
	X20	**X24**	**X32**	**X40**
A → Y ↑	0.3072	0.2497	0.1884	0.1511
A → Y ↓	0.3241	0.2715	0.2037	0.1623

Cell Description

The CLKINV cell provides the logical inversion of a single input (A), with balanced delays for clock signals. The output (Y) is represented by the logic equation:

$Y = \overline{A}$

Logic Symbol

A —▷o— Y

Function Table

A	Y
0	1
1	0
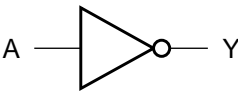
Cell Size

Drive Strength	Height (um)	Width (um)
CLKINVX1ADTH	2.52	0.84
CLKINVX2ADTH	2.52	0.84
CLKINVX3ADTH	2.52	1.12
CLKINVX4ADTH	2.52	1.12
CLKINVX6ADTH	2.52	1.68
CLKINVX8ADTH	2.52	1.96
CLKINVX12ADTH	2.52	2.52
CLKINVX16ADTH	2.52	3.36
CLKINVX20ADTH	2.52	3.64
CLKINVX24ADTH	2.52	4.48
CLKINVX32ADTH	2.52	5.60
CLKINVX40ADTH	2.52	7.00

Functional Schematic

A ▷———▷o———▷ Y
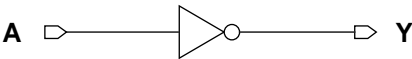
AC Power

Pin	Power (uW/MHz)							
	X1	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**
A	0.0014	0.0021	0.0029	0.0037	0.0056	0.0075	0.0110	0.0149

AC Power (Cont'd.)

Pin	Power (uW/MHz)			
	X20	**X24**	**X32**	**X40**
A	0.0185	0.0224	0.0295	0.0367

Pin Capacitance

Pin	Capacitance (pF)							
	X1	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**
A	0.0015	0.0022	0.0032	0.0042	0.0061	0.0082	0.0121	0.0164

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)			
	X20	**X24**	**X32**	**X40**
A	0.0202	0.0244	0.0322	0.0404

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X1	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**
A → Y ↑	0.0131	0.0126	0.0118	0.0117	0.0118	0.0119	0.0120	0.0123
A → Y ↓	0.0145	0.0144	0.0135	0.0129	0.0133	0.0132	0.0134	0.0134

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)			
	X20	**X24**	**X32**	**X40**
A → Y ↑	0.0123	0.0127	0.0133	0.0135
A → Y ↓	0.0133	0.0137	0.0143	0.0144

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X1	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**
A → Y ↑	4.6553	2.8082	1.9266	1.4341	0.9721	0.7351	0.4967	0.3753
A → Y ↓	5.3212	3.3294	2.2515	1.6292	1.1034	0.8234	0.5476	0.4098

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)			
	X20	**X24**	**X32**	**X40**
A → Y ↑	0.2966	0.2499	0.1875	0.1512
A → Y ↓	0.3229	0.2704	0.2019	0.1612

Cell Description

The CLKMX2 cell is a non-inverting 2 to 1 multiplexer with balanced delays for clock signals. The state of the select input (S0) determines which data input (A,B) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (S0 \bullet B) + (\overline{S0} \bullet A)$$

Logic Symbol
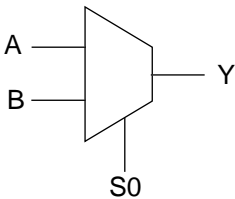
Function Table

S0	A	B	Y
0	0	x	0
0	1	x	1
1	x	0	0
1	x	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
CLKMX2X2ADTH	2.52	2.80
CLKMX2X3ADTH	2.52	3.36
CLKMX2X4ADTH	2.52	3.36
CLKMX2X6ADTH	2.52	3.92
CLKMX2X8ADTH	2.52	4.20
CLKMX2X12ADTH	2.52	5.04

Functional Schematic
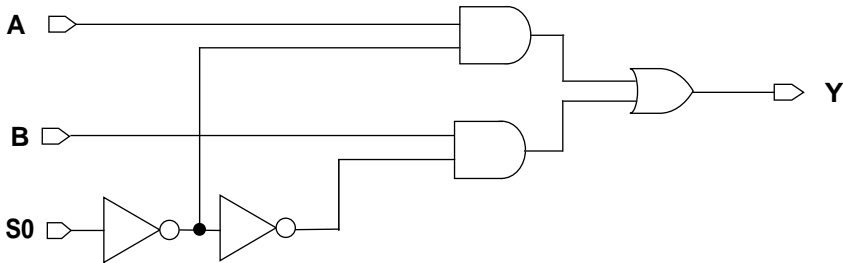
AC Power

Pin	Power (uW/MHz)					
	X2	**X3**	**X4**	**X6**	**X8**	**X12**
S0	0.0068	0.0087	0.0096	0.0115	0.0137	0.0178
B	0.0062	0.0076	0.0085	0.0106	0.0126	0.0171
A	0.0056	0.0067	0.0076	0.0097	0.0118	0.0161

Pin Capacitance

Pin	Capacitance (pF)					
	X2	**X3**	**X4**	**X6**	**X8**	**X12**
S0	0.0036	0.0041	0.0041	0.0041	0.0041	0.0040
B	0.0019	0.0021	0.0021	0.0021	0.0021	0.0021
A	0.0020	0.0023	0.0023	0.0023	0.0023	0.0023

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			X2	**X3**	**X4**	**X6**	**X8**	**X12**
S0	→ Y	↑	0.0763	0.0801	0.0844	0.0951	0.1057	0.1216
S0	→ Y	↓	0.0819	0.0879	0.0937	0.1056	0.1173	0.1398
B	→ Y	↑	0.0731	0.0750	0.0803	0.0922	0.1039	0.1224
B	→ Y	↓	0.0784	0.0841	0.0906	0.1041	0.1171	0.1408
A	→ Y	↑	0.0748	0.0766	0.0814	0.0934	0.1051	0.1231
A	→ Y	↓	0.0768	0.0810	0.0882	0.1022	0.1156	0.1399

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)					
			X2	**X3**	**X4**	**X6**	**X8**	**X12**
S0	→ Y	↑	2.9259	2.0330	1.5175	1.0338	0.7881	0.5417
S0	→ Y	↓	3.3373	2.2916	1.7305	1.1490	0.8608	0.5908
B	→ Y	↑	2.9270	2.0321	1.5176	1.0336	0.7881	0.5429
B	→ Y	↓	3.3365	2.2913	1.7304	1.1491	0.8609	0.5909
A	→ Y	↑	2.9248	2.0322	1.5171	1.0336	0.7883	0.5419
A	→ Y	↓	3.3338	2.2882	1.7294	1.1491	0.8614	0.5914

Cell Description

The CLKNAND2 cell provides the logical NAND of two inputs (A,B), with balanced delays for clock signals. The output (Y) is represented by the logic equation:

$$Y = \overline{(A \bullet B)}$$

Logic Symbol

Function Table

A	B	Y
0	x	1
x	0	1
1	1	0
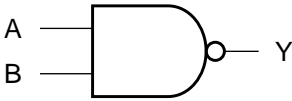
Cell Size

Drive Strength	Height (um)	Width (um)
CLKNAND2X2ADTH	2.52	1.12
CLKNAND2X4ADTH	2.52	1.96
CLKNAND2X8ADTH	2.52	3.36
CLKNAND2X12ADTH	2.52	4.76

Functional Schematic

AC Power

Pin	Power (uW/MHz)			
	X2	**X4**	**X8**	**X12**
A	0.0025	0.0050	0.0101	0.0147
B	0.0032	0.0065	0.0130	0.0189

Pin Capacitance

Pin	Capacitance (pF)			
	X2	**X4**	**X8**	**X12**
A	0.0024	0.0046	0.0094	0.0137
B	0.0022	0.0049	0.0095	0.0139

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			X2	**X4**	**X8**	**X12**	**X2**	**X4**	**X8**	**X12**
A	→ Y	↑	0.0152	0.0155	0.0158	0.0156	2.8696	1.4928	0.7642	0.5144
A	→ Y	↓	0.0194	0.0197	0.0196	0.0195	4.0371	2.0645	1.0172	0.6919
B	→ Y	↑	0.0170	0.0177	0.0180	0.0178	2.8707	1.4487	0.7493	0.5064
B	→ Y	↓	0.0217	0.0227	0.0223	0.0223	4.0343	2.0646	1.0167	0.6916

Cell Description

The CLKXOR2 cell provides a logical EXCLUSIVE OR of two inputs (A,B) with balanced delays for clock signals. The output (Y) is represented by the logic equation:

$$Y = (A \bullet \overline{B}) + (\overline{A} \bullet B)$$

Logic Symbol

A —)) XOR — Y
B —))

Function Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0
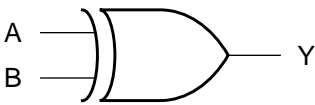
Cell Size

Drive Strength	Height (um)	Width (um)
CLKXOR2X1ADTH	2.52	2.80
CLKXOR2X2ADTH	2.52	2.80
CLKXOR2X4ADTH	2.52	4.20
CLKXOR2X8ADTH	2.52	6.72
CLKXOR2X12ADTH	2.52	10.08

Functional Schematic

A ▷

B ▷

Y ▷
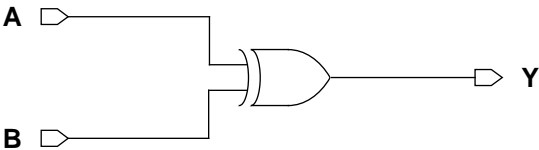
AC Power

Pin	Power (uW/MHz)				
	X1	**X2**	**X4**	**X8**	**X12**
A	0.0059	0.0064	0.0105	0.0198	0.0291
B	0.0064	0.0072	0.0136	0.0263	0.0403

Pin Capacitance

Pin	Capacitance (pF)				
	X1	**X2**	**X4**	**X8**	**X12**
A	0.0031	0.0032	0.0042	0.0070	0.0096
B	0.0017	0.0020	0.0036	0.0068	0.0104

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	X1	**X2**	**X4**	**X8**	**X12**
A → Y ↑	0.0767	0.0760	0.0783	0.0856	0.0892
A → Y ↓	0.0820	0.0881	0.0848	0.0947	0.0971
B → Y ↑	0.1076	0.1044	0.1015	0.0991	0.0995
B → Y ↓	0.1126	0.1143	0.1060	0.1081	0.1093

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)				
	X1	**X2**	**X4**	**X8**	**X12**
A → Y ↑	4.9440	2.9367	1.4865	0.7674	0.5070
A → Y ↓	5.3926	3.3683	1.6389	0.8221	0.5624
B → Y ↑	4.9205	2.9385	1.4883	0.7692	0.5083
B → Y ↓	5.3892	3.3667	1.6384	0.8219	0.5622

Cell Description

The CMPR42 cell takes in 4 bits of the partial product (A,B,C,D) and compresses them into 2-bits of partial product (S,CO). The cell requires an intermediate carry-in input (ICI) from the n-1 compressor and an intermediate carry-out output (CO) to the n+1 compressor. The CMPR42 cell also contains an internal sum IS. The internal sum IS, carry-in output (ICO), and the two outputs (S,CO) are represented by the logic equations:

$IS = A \oplus B \oplus C$

$ICO = (A \bullet B) + (A \bullet C) + (B \bullet C)$

$S = IS \oplus D \oplus ICI$

$CO = (IS \bullet D) + (IS \bullet ICI) + (D \bullet ICI)$

Logic Symbol
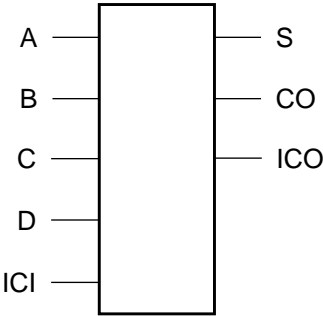
Cell Size

Drive Strength	Height (um)	Width (um)
CMPR42X1ADTH	2.52	12.88
CMPR42X2ADTH	2.52	12.88
CMPR42X4ADTH	2.52	18.48

Function Table

A	B	C	IS	ICO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Function Table (Cont'd.)

IS	D	ICI	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Functional Schematic
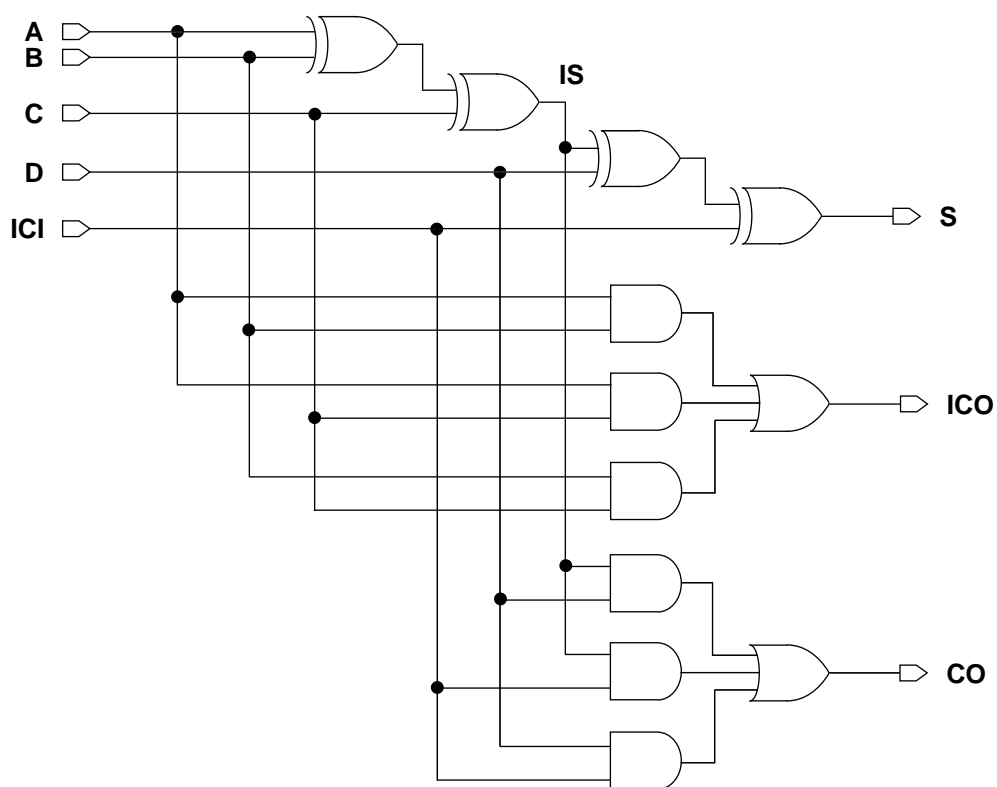
AC Power

Pin	Power (uW/MHz)		
	X1	**X2**	**X4**
A	0.0273	0.0370	0.0580
B	0.0265	0.0357	0.0562
C	0.0256	0.0339	0.0525
D	0.0209	0.0281	0.0480
ICI	0.0100	0.0141	0.0260

Pin Capacitance

Pin	Capacitance (pF)		
	X1	**X2**	**X4**
A	0.0046	0.0063	0.0099
B	0.0054	0.0072	0.0112
C	0.0043	0.0053	0.0065
D	0.0029	0.0036	0.0037
ICI	0.0018	0.0022	0.0026

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)			K_{load} (ns/pF)		
				X1	**X2**	**X4**	**X1**	**X2**	**X4**
A	→	S	↑	0.3459	0.3489	0.3999	4.6817	2.9960	1.4975
A	→	S	↓	0.4190	0.4032	0.4539	4.1149	1.7860	0.8750
B	→	S	↑	0.3001	0.2827	0.3285	4.6811	2.9940	1.4951
B	→	S	↓	0.3732	0.3371	0.3830	4.1152	1.7864	0.8752
C	→	S	↑	0.2678	0.2781	0.3100	4.6788	2.9953	1.4964
C	→	S	↓	0.3417	0.3334	0.3660	4.1154	1.7863	0.8752
D	→	S	↑	0.2345	0.2207	0.2624	4.6019	2.9742	1.4982
D	→	S	↓	0.2973	0.2721	0.3210	4.1155	1.7859	0.8739
ICI	→	S	↑	0.1196	0.1122	0.1426	4.6343	2.9773	1.4845
ICI	→	S	↓	0.1429	0.1325	0.1472	4.1192	1.7874	0.8757
A	→	ICO	↑	0.0633	0.0570	0.0564	4.5463	2.9035	1.4796
A	→	ICO	↓	0.1173	0.0982	0.1018	4.0060	1.7367	0.8660
B	→	ICO	↑	0.0638	0.0572	0.0569	4.5483	2.9048	1.4802
B	→	ICO	↓	0.1101	0.0937	0.0940	4.0075	1.7381	0.8996
C	→	ICO	↑	0.0535	0.0503	0.0496	4.5231	2.8988	1.4754
C	→	ICO	↓	0.0922	0.0812	0.0885	4.0612	1.7764	0.8851
A	→	CO	↑	0.3305	0.3327	0.3948	4.4219	3.0547	1.5186
A	→	CO	↓	0.3884	0.3828	0.4493	3.9556	2.4282	0.9253
B	→	CO	↑	0.2895	0.2944	0.3553	4.4219	3.0547	1.5186
B	→	CO	↓	0.3474	0.3445	0.4098	3.9559	2.4283	0.9253
C	→	CO	↑	0.2677	0.2633	0.3214	4.4211	3.0550	1.5186
C	→	CO	↓	0.2898	0.2801	0.3442	3.9562	2.4286	0.9252

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description				Intrinsic Delay (ns)			K_{load} (ns/pF)		
				X1	X2	X4	X1	X2	X4
D	→	CO	↑	0.2206	0.1954	0.2294	4.3875	3.0334	1.4979
D	→	CO	↓	0.2077	0.1983	0.2443	3.9341	2.4127	0.9202
ICI	→	CO	↑	0.0652	0.0714	0.0868	4.4291	3.0569	1.5136
ICI	→	CO	↓	0.0981	0.0907	0.1245	4.0422	2.4604	0.9630

Cell Description

The DFF cell is a positive-edge triggered, static D-type flipflop.

Logic Symbol
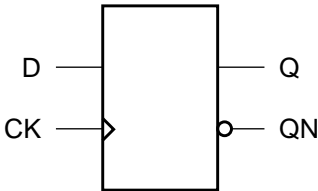
Function Table

D	CK	Q[n+1]	QN[n+1]
0	⤒	0	1
1	⤒	1	0
x	⤓	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFXLADTH	2.52	6.16
DFFX1ADTH	2.52	6.16
DFFX2ADTH	2.52	6.16
DFFX4ADTH	2.52	7.84

Functional Schematic
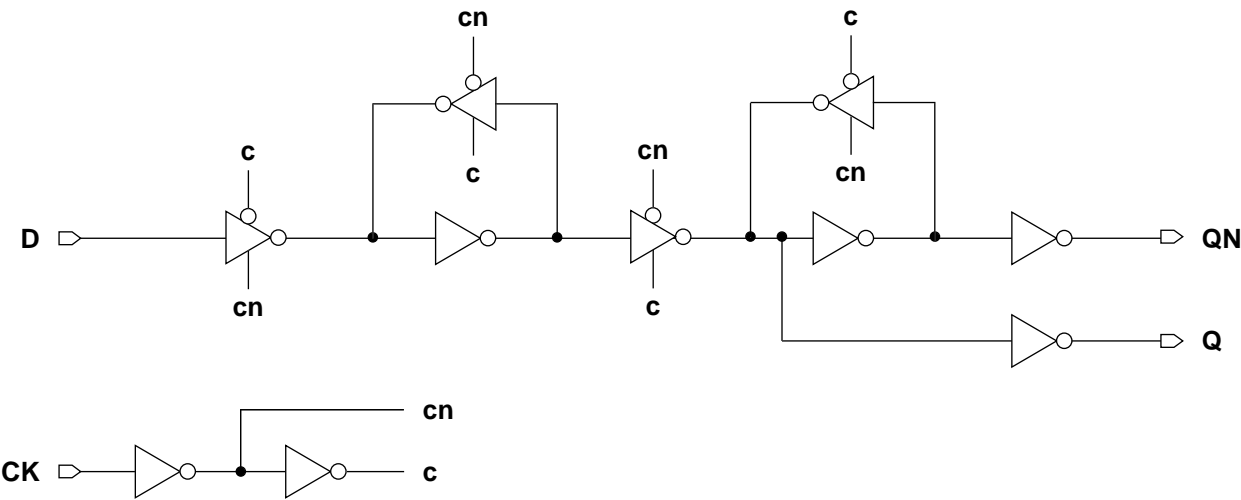
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0046	0.0047	0.0049	0.0060
CK	0.0100	0.0101	0.0105	0.0123
Q	0.0046	0.0055	0.0077	0.0131

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0011	0.0011	0.0011	0.0011
CK	0.0015	0.0015	0.0015	0.0017

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→ Q	↑	0.1447	0.1414	0.1412	0.1393	7.2031	4.5980	2.9259	1.4988
CK	→ Q	↓	0.1593	0.1563	0.1428	0.1380	6.6342	4.2729	1.8327	0.9041
CK	→ QN	↑	0.2024	0.1977	0.2001	0.1996	7.0090	4.5233	2.9095	1.4846
CK	→ QN	↓	0.1977	0.2018	0.2128	0.2049	5.6007	3.8754	1.7245	0.8348

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	CK	0.0469	0.0469	0.0469	0.0547
	setup	↓	→	CK	0.0625	0.0625	0.0703	0.0820
	hold	↑	→	CK	-0.0312	-0.0312	-0.0312	-0.0312
	hold	↓	→	CK	-0.0117	-0.0117	-0.0078	-0.0156
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The DFFH cell is a positive-edge triggered,
static D-type flipflop and fast clock-to-Q-path.

Logic Symbol

D — Q
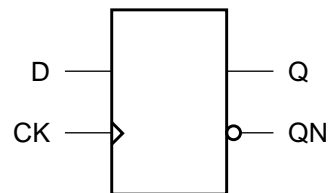
CK — QN

Function Table

D	CK	Q[n+1]	QN[n+1]
0	⌐⌐	0	1
1	⌐⌐	1	0
x	⌐⌐	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFHX1ADTH	2.52	7.28
DFFHX2ADTH	2.52	7.56
DFFHX4ADTH	2.52	8.96
DFFHX8ADTH	2.52	14.28

Functional Schematic
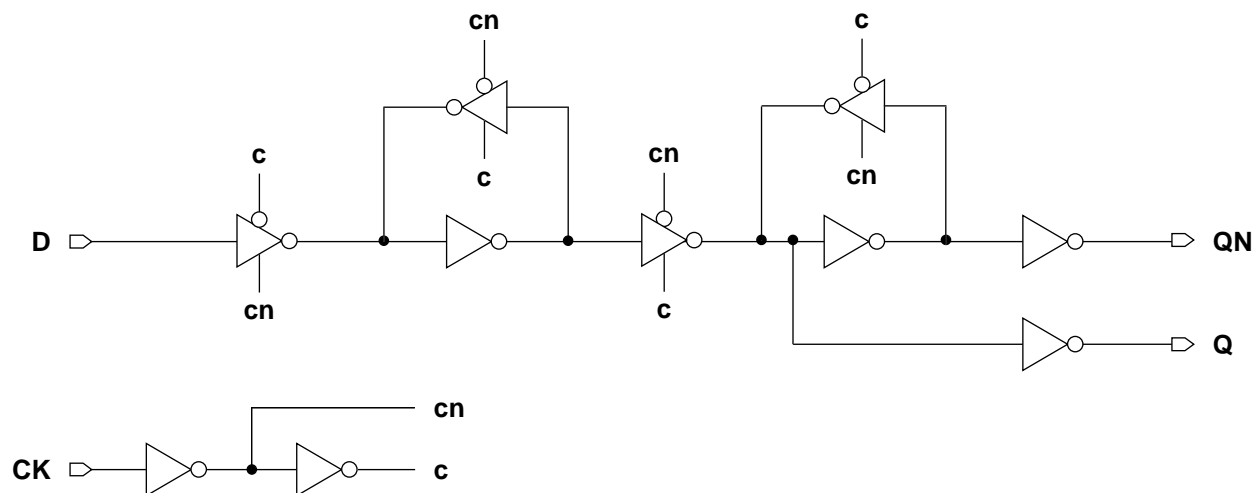
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
D	0.0064	0.0085	0.0118	0.0210
CK	0.0138	0.0177	0.0231	0.0430
Q	0.0049	0.0065	0.0086	0.0146

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
D	0.0011	0.0012	0.0016	0.0024
CK	0.0023	0.0024	0.0031	0.0052

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→	Q ↑	0.0995	0.0998	0.0893	0.0852	4.5077	2.9252	1.4791	0.7428
CK	→	Q ↓	0.1080	0.1093	0.1017	0.0910	3.9927	1.7762	0.8782	0.4117
CK	→	QN ↑	0.1408	0.1481	0.1466	0.1345	6.8802	6.7904	6.6997	6.6635
CK	→	QN ↓	0.1503	0.1537	0.1560	0.1546	5.3373	5.2443	5.2286	5.2193

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
D	setup	↑	→	CK	0.0664	0.0625	0.0547	0.0547
	setup	↓	→	CK	0.0703	0.0703	0.0742	0.0625
	hold	↑	→	CK	-0.0156	-0.0156	-0.0078	-0.0039
	hold	↓	→	CK	-0.0352	-0.0352	-0.0391	-0.0234
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The DFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop. The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol
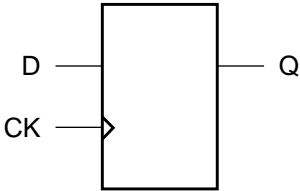
Function Table

D	CK	Q[n+1]
0	⌐	0
1	⌐	1
x	⌐	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFHQX1ADTH	2.52	6.72
DFFHQX2ADTH	2.52	7.00
DFFHQX4ADTH	2.52	8.40
DFFHQX8ADTH	2.52	14.00

Functional Schematic
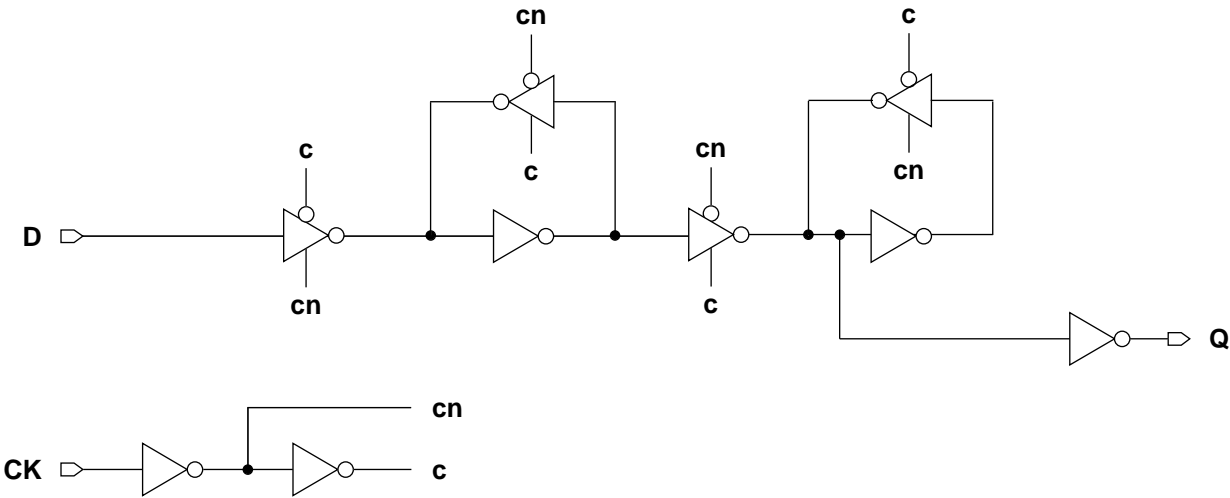
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
D	0.0064	0.0079	0.0123	0.0221
CK	0.0131	0.0161	0.0229	0.0430
Q	0.0036	0.0048	0.0075	0.0129

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
D	0.0015	0.0016	0.0020	0.0035
CK	0.0023	0.0023	0.0031	0.0052

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK → Q ↑			0.1023	0.0994	0.0895	0.0846	4.3984	2.9059	1.4813	0.7426
CK → Q ↓			0.1127	0.1062	0.1020	0.0905	4.0825	1.7965	0.8824	0.4127

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
D	setup	↑	→	CK	0.0742	0.0625	0.0586	0.0547
	setup	↓	→	CK	0.0547	0.0469	0.0508	0.0430
	hold	↑	→	CK	-0.0195	-0.0156	-0.0117	-0.0078
	hold	↓	→	CK	-0.0195	-0.0156	-0.0195	-0.0117
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The DFFNH cell is a negative-edge triggered, static D-type flip-flop and fast clock-to-Q-path.

Logic Symbol

Function Table
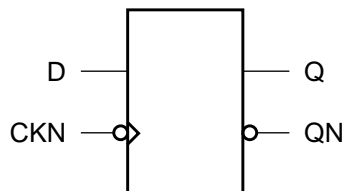
D	CKN	Q[n+1]	QN[n+1]
0	⌐⌐	0	1
1	⌐⌐	1	0
x	⌐	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFNHX1ADTH	2.52	7.00
DFFNHX2ADTH	2.52	7.00
DFFNHX4ADTH	2.52	9.24
DFFNHX8ADTH	2.52	13.72

Functional Schematic
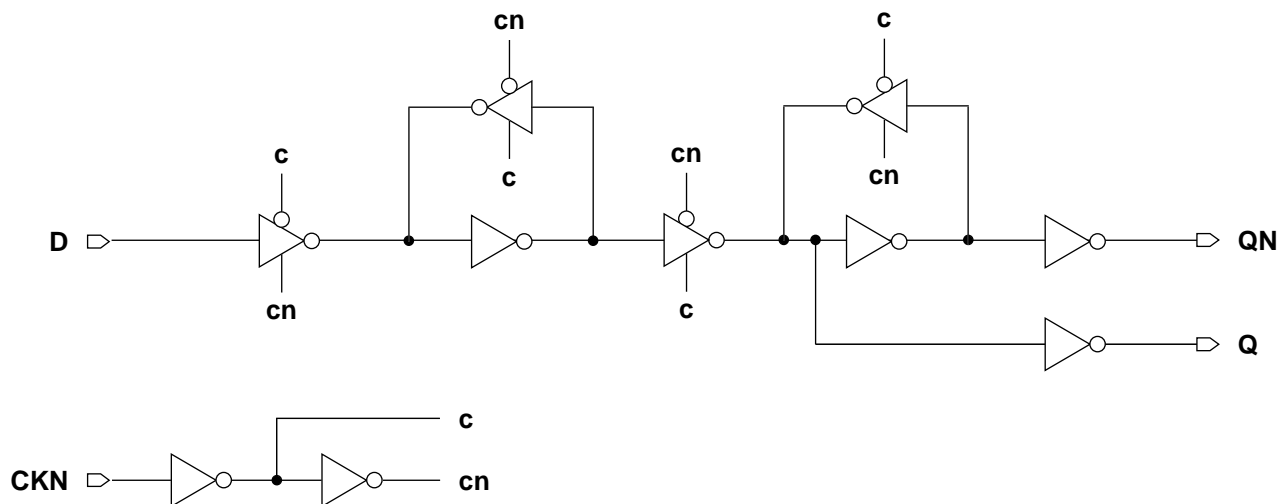
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
D	0.0064	0.0081	0.0124	0.0199
CKN	0.0106	0.0127	0.0186	0.0290
Q	0.0053	0.0065	0.0094	0.0154

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
D	0.0014	0.0018	0.0025	0.0045
CKN	0.0020	0.0021	0.0026	0.0041

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CKN	→	Q ↑	0.2010	0.1994	0.1995	0.1831	4.5067	2.8584	1.4581	0.7437
CKN	→	Q ↓	0.1701	0.1565	0.1507	0.1322	4.0886	1.7476	0.8435	0.4153
CKN	→	QN ↑	0.2067	0.1948	0.1952	0.1774	6.7064	6.6705	6.7150	6.7128
CKN	→	QN ↓	0.2537	0.2506	0.2669	0.2448	5.3809	5.3238	5.2292	5.2157

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
D	setup	↑	→	CKN	-0.0195	-0.0352	-0.0430	-0.0273
	setup	↓	→	CKN	0.0195	0.0078	0.0117	0.0273
	hold	↑	→	CKN	0.0664	0.0664	0.0703	0.0586
	hold	↓	→	CKN	0.0117	0.0156	0.0156	0.0078
CKN	minpwl				0.8332	0.8332	0.8332	0.8332
	minpwh				0.8332	0.8332	0.8332	0.8332

Cell Description

The DFFNSRH cell is a negative-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset, and fast clock-to-Q-path.

Logic Symbol
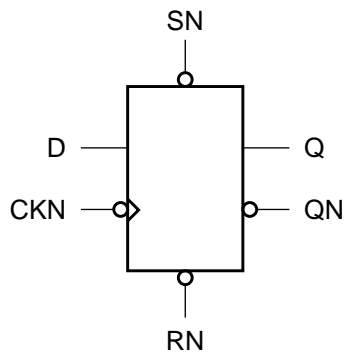
Function Table

RN	SN	D	CKN	Q[n+1]	QN[n+1]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0
1	1	0	⌐_	0	1
1	1	1	⌐_	1	0
1	1	x	_⌐	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFNSRHX1ADTH	2.52	9.80
DFFNSRHX2ADTH	2.52	9.80
DFFNSRHX4ADTH	2.52	12.88
DFFNSRHX8ADTH	2.52	14.00

Functional Schematic
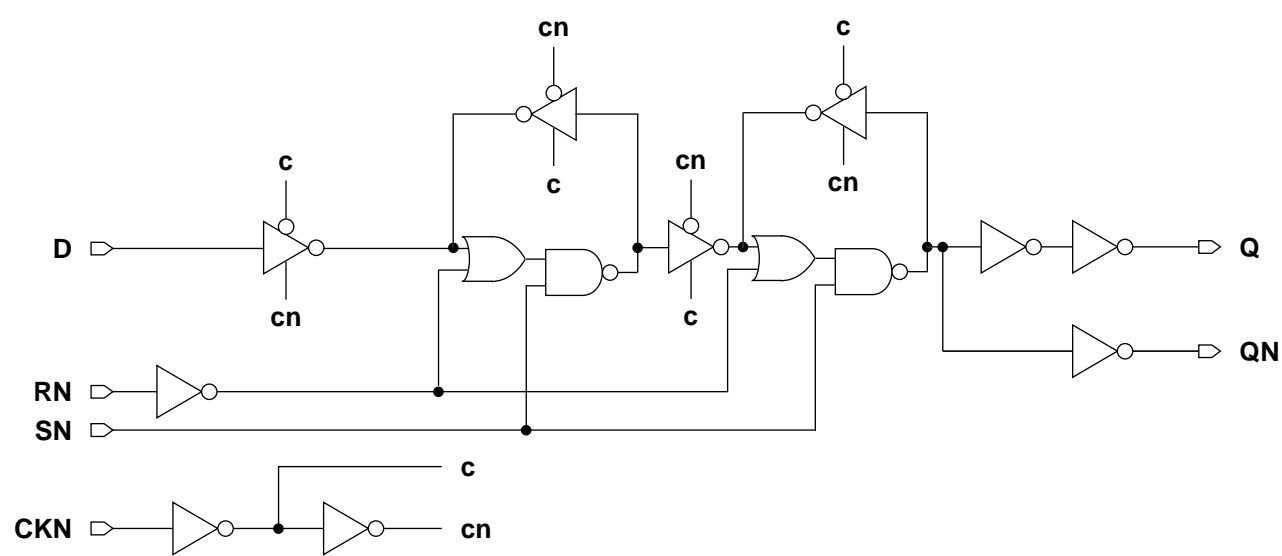
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
D	0.0073	0.0089	0.0144	0.0167
CKN	0.0114	0.0134	0.0208	0.0222
SN	0.0039	0.0041	0.0050	0.0059
RN	0.0011	0.0012	0.0021	0.0025
Q	0.0068	0.0080	0.0118	0.0169

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
D	0.0013	0.0017	0.0025	0.0043
CKN	0.0021	0.0023	0.0028	0.0040
SN	0.0021	0.0025	0.0034	0.0039
RN	0.0020	0.0023	0.0036	0.0039

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CKN	→	Q	↑	0.2297	0.2206	0.2279	0.2149	4.6535	3.0009	1.4873	0.7670
CKN	→	Q	↓	0.1870	0.1617	0.1587	0.1601	4.2779	1.8150	0.8811	0.4534
SN	→	Q	↑	0.1448	0.1688	0.2081	0.1542	4.5119	2.9911	1.4945	0.7583
SN	→	Q	↓	0.2718	0.2704	0.2381	0.2374	4.9817	2.2447	1.0834	0.5370
RN	→	Q	↓	0.2365	0.2289	0.1904	0.1995	5.0335	2.2461	1.0842	0.5372
CKN	→	QN	↑	0.2310	0.2084	0.2069	0.2148	6.6940	6.6947	6.7031	6.8800
CKN	→	QN	↓	0.2972	0.2871	0.2973	0.2896	5.5682	5.4772	5.3684	5.4353
SN	→	QN	↑	0.3263	0.3270	0.2960	0.3027	6.7398	6.7115	6.7074	6.8811
SN	→	QN	↓	0.2091	0.2346	0.2780	0.2279	5.5480	5.4693	5.3671	5.4347
RN	→	QN	↑	0.2922	0.2856	0.2483	0.2648	6.7413	6.7099	6.7062	6.8802

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	X2	X4	X8
D	setup	↑	→	CKN	-0.0039	-0.0195	-0.0273	-0.0234
	setup	↓	→	CKN	0.0234	0.0156	0.0156	0.0273
	hold	↑	→	CKN	0.0703	0.0703	0.0703	0.0703
	hold	↓	→	CKN	0.0156	0.0195	0.0195	0.0117
CKN	minpwl				0.8332	0.8332	0.8332	0.8332
	minpwh				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0039	-0.0078	-0.0078	0.0078
	removal				0.0273	0.0273	0.0312	0.0156
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.1211	-0.1211	-0.1289	-0.1055
	removal				0.1641	0.1758	0.2188	0.1875

Cell Description

The DFFQ cell is a positive-edge triggered, static D-type flip-flop. The cell has a single output (Q) .

Logic Symbol

D — Q

CK ——▷
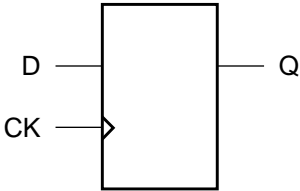
Function Table

D	CK	Q[n+1]
0	⌐⌐	0
1	⌐⌐	1
x	⌐⌐	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFQXLADTH	2.52	5.32
DFFQX1ADTH	2.52	5.60
DFFQX2ADTH	2.52	5.60
DFFQX4ADTH	2.52	7.00

Functional Schematic
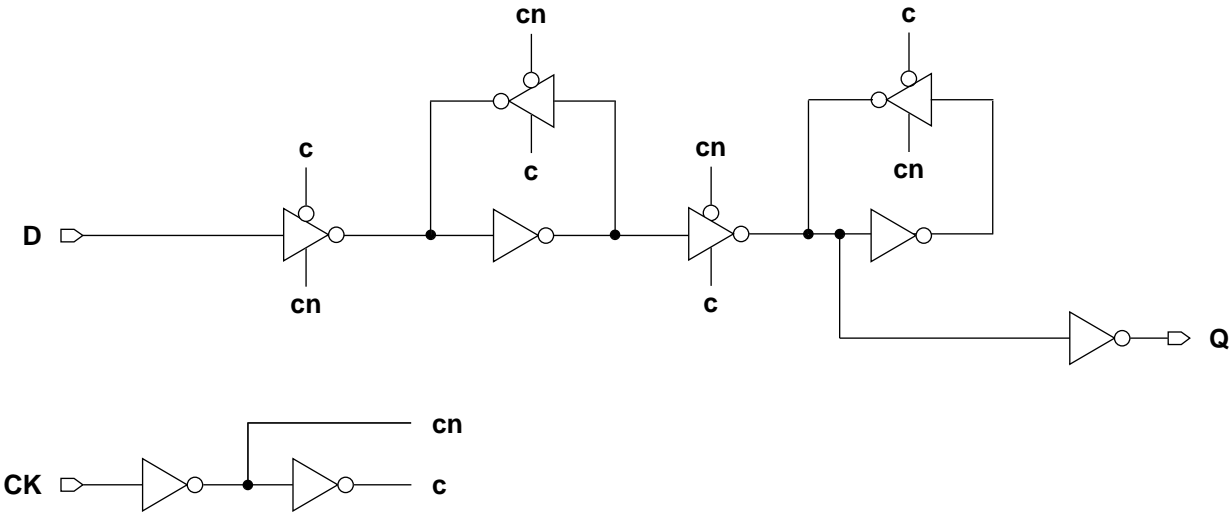
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0043	0.0044	0.0045	0.0057
CK	0.0095	0.0095	0.0097	0.0121
Q	0.0035	0.0041	0.0050	0.0082

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0010	0.0010	0.0010	0.0011
CK	0.0017	0.0017	0.0016	0.0017

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→ Q	↑	0.1379	0.1355	0.1355	0.1438	7.0397	4.4913	2.8548	1.4566
CK	→ Q	↓	0.1634	0.1608	0.1439	0.1393	6.6957	4.3310	1.8559	0.9029

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	CK	0.0430	0.0430	0.0391	0.0547
	setup	↓	→	CK	0.0625	0.0625	0.0664	0.0781
	hold	↑	→	CK	-0.0273	-0.0273	-0.0234	-0.0312
	hold	↓	→	CK	-0.0156	-0.0156	-0.0117	-0.0117
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The DFFR cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN).

Logic Symbol
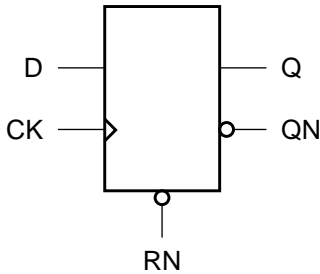
Function Table

RN	D	CK	Q[n+1]	QN[n+1]
0	x	x	0	1
1	0	⌐	0	1
1	1	⌐	1	0
1	x	⌐	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFRXLADTH	2.52	6.72
DFFRX1ADTH	2.52	6.72
DFFRX2ADTH	2.52	7.00
DFFRX4ADTH	2.52	7.84

Functional Schematic
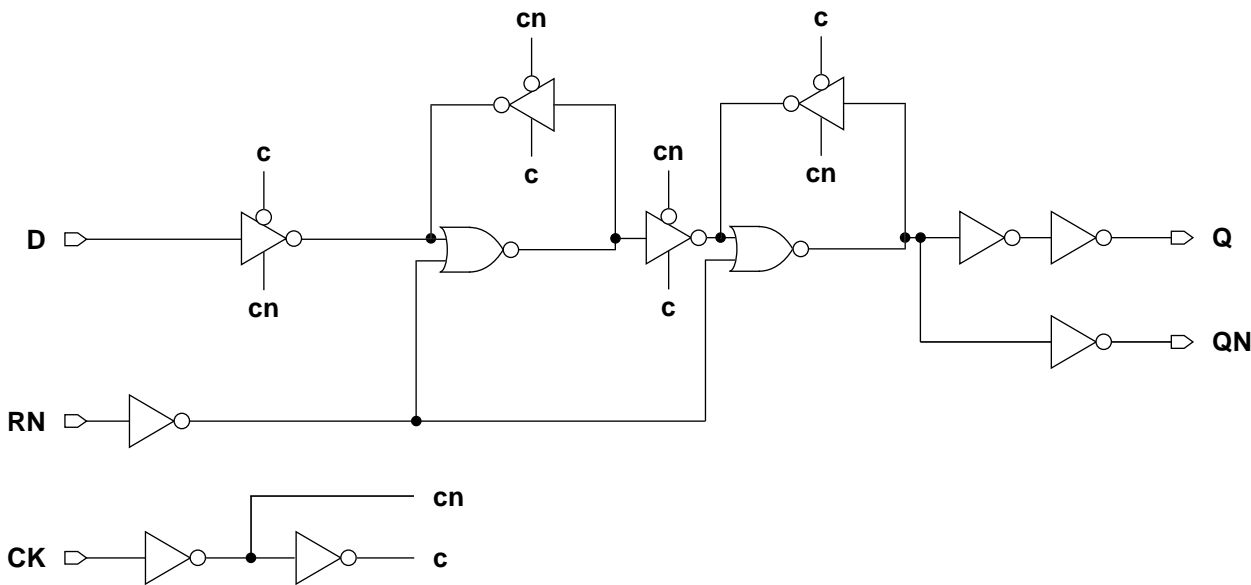
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0050	0.0050	0.0064	0.0071
CK	0.0105	0.0105	0.0120	0.0132
RN	0.0010	0.0011	0.0011	0.0013
Q	0.0046	0.0053	0.0077	0.0127

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0011	0.0011	0.0013	0.0014
CK	0.0016	0.0016	0.0017	0.0022
RN	0.0031	0.0031	0.0033	0.0040

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1777	0.1892	0.1762	0.1918	7.0919	4.7140	2.9313	1.4984
CK	→	Q	↓	0.2060	0.2200	0.2192	0.2205	5.4520	4.0120	1.7950	0.8928
RN	→	Q	↓	0.0923	0.1028	0.1175	0.1111	5.5873	4.0554	1.8330	0.9078
CK	→	QN	↑	0.1322	0.1340	0.1238	0.1195	7.1461	4.7519	2.9039	1.5265
CK	→	QN	↓	0.1180	0.1277	0.1090	0.1202	5.8360	4.2429	1.7670	0.9324
RN	→	QN	↑	0.1954	0.1978	0.2215	0.2550	7.0559	4.6899	2.9609	1.5824

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	CK	0.1133	0.1133	0.1055	0.0938
	setup	↓	→	CK	0.0469	0.0469	0.0312	0.0430
	hold	↑	→	CK	-0.0625	-0.0625	-0.0586	-0.0469
	hold	↓	→	CK	0.0117	0.0117	0.0156	0.0117
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.1133	0.1094	0.1016	0.0938
	removal				-0.0820	-0.0820	-0.0742	-0.0664

Cell Description

The DFFRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol
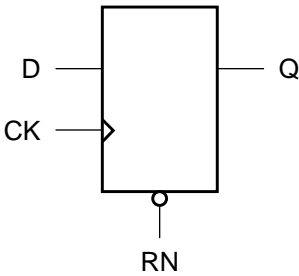
Function Table

RN	D	CK	Q[n+1]
0	x	x	0
1	0	_/	0
1	1	_/	1
1	x	‾_	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFRHQX1ADTH	2.52	7.56
DFFRHQX2ADTH	2.52	7.56
DFFRHQX4ADTH	2.52	9.24
DFFRHQX8ADTH	2.52	10.64

Functional Schematic
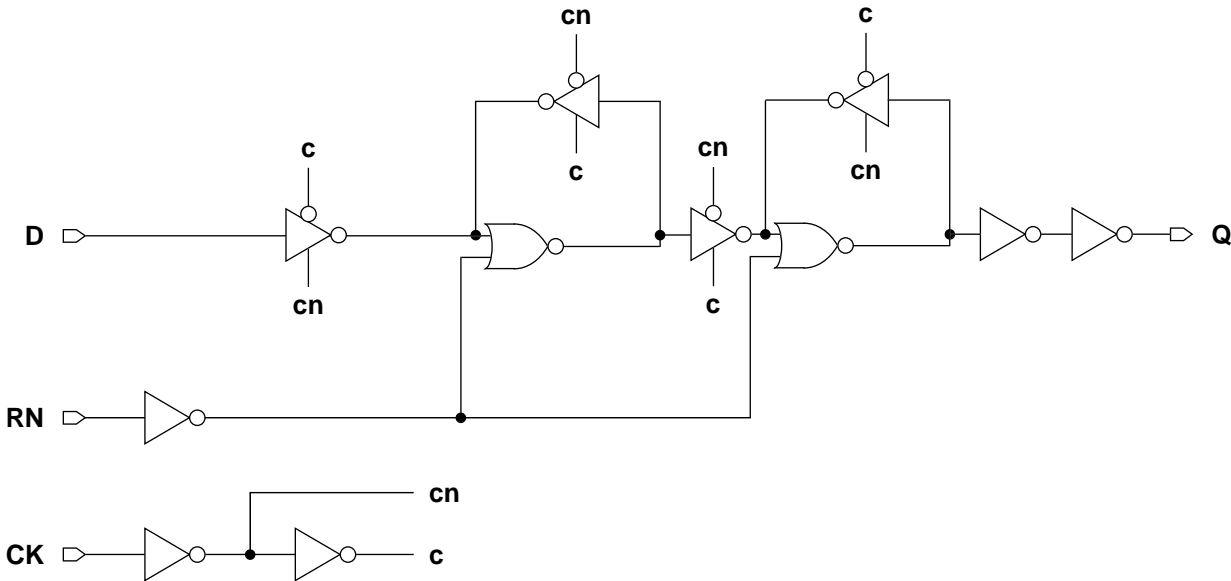
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
D	0.0070	0.0087	0.0132	0.0156
CK	0.0127	0.0153	0.0239	0.0289
RN	0.0011	0.0014	0.0022	0.0027
Q	0.0037	0.0050	0.0081	0.0134

Pin Capacitance

| Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
D	0.0015	0.0016	0.0022	0.0037
CK	0.0020	0.0022	0.0030	0.0053
RN	0.0018	0.0024	0.0036	0.0041

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→	Q	↑	0.1109	0.1060	0.1004	0.1051	4.5620	2.8986	1.4679	0.7570
CK	→	Q	↓	0.1102	0.1024	0.1028	0.1104	4.0995	1.7453	0.8583	0.4447
RN	→	Q	↓	0.1107	0.1108	0.0948	0.0876	4.2383	1.8715	0.8986	0.4350

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
D	setup	↑	→	CK	0.0898	0.0742	0.0703	0.0664
	setup	↓	→	CK	0.0625	0.0508	0.0469	0.0430
	hold	↑	→	CK	-0.0234	-0.0156	-0.0156	-0.0039
	hold	↓	→	CK	-0.0195	-0.0156	-0.0117	-0.0078
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0156	-0.0195	-0.0234	-0.0156
	removal				0.0469	0.0586	0.0820	0.0703

Cell Description

The DFFRQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN). The cell has a single output (Q).

Logic Symbol
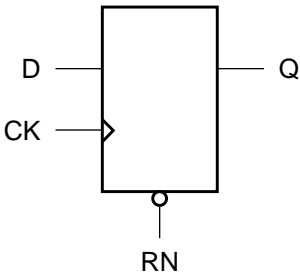
Function Table

RN	D	CK	Q[n+1]
0	x	x	0
1	0	_/	0
1	1	_/	1
1	x	‾_	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFRQXLADTH	2.52	6.16
DFFRQX1ADTH	2.52	6.16
DFFRQX2ADTH	2.52	6.16
DFFRQX4ADTH	2.52	6.44

Functional Schematic
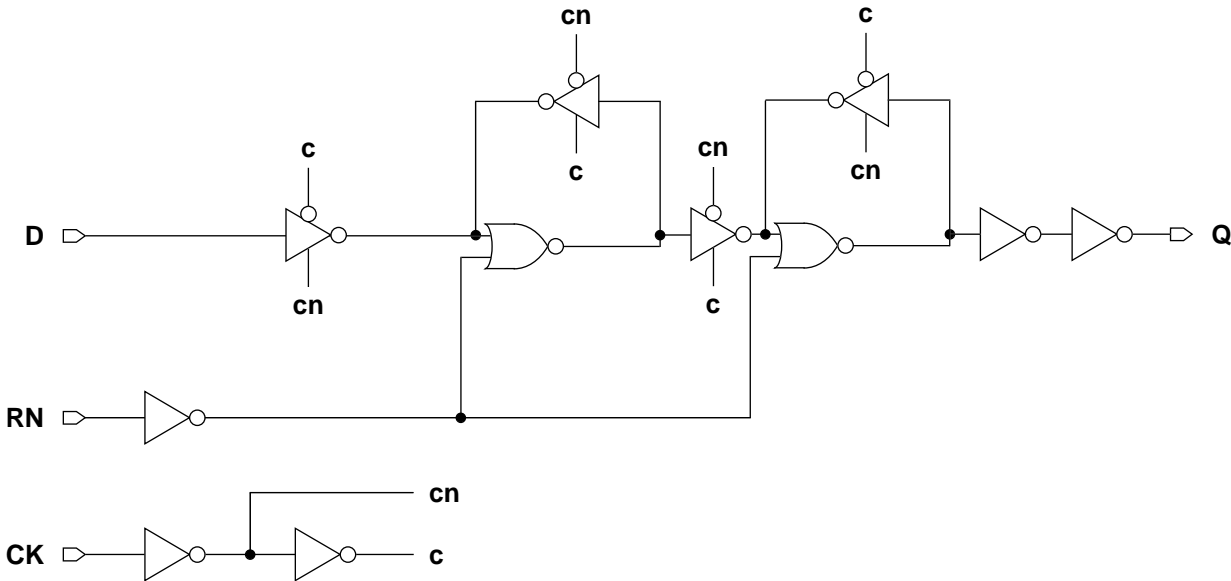
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0039	0.0039	0.0040	0.0040
CK	0.0080	0.0080	0.0080	0.0080
RN	0.0008	0.0008	0.0008	0.0010
Q	0.0036	0.0040	0.0051	0.0077

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0010	0.0010	0.0010	0.0010
CK	0.0012	0.0012	0.0012	0.0012
RN	0.0028	0.0028	0.0028	0.0033

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1664	0.1720	0.1749	0.1759	7.1051	4.5561	2.8950	1.4803
CK	→	Q	↓	0.2041	0.2146	0.2297	0.2281	5.9089	4.0708	1.8314	0.9011
RN	→	Q	↓	0.0865	0.0976	0.1139	0.1077	6.0255	4.0903	1.8209	0.8927

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	CK	0.1016	0.0977	0.0977	0.1016
	setup	↓	→	CK	0.0234	0.0195	0.0195	0.0195
	hold	↑	→	CK	-0.0547	-0.0547	-0.0547	-0.0547
	hold	↓	→	CK	0.0156	0.0156	0.0156	0.0195
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.1016	0.1016	0.1016	0.1016
	removal				-0.0703	-0.0703	-0.0703	-0.0703

Cell Description

The DFFS cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low set (SN).

Logic Symbol
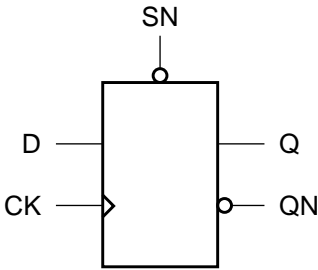
Function Table

SN	D	CK	Q[n+1]	QN[n+1]
0	x	x	1	0
1	0	⌐‾	0	1
1	1	⌐‾	1	0
1	x	‾⌐	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFSXLADTH	2.52	6.16
DFFSX1ADTH	2.52	6.16
DFFSX2ADTH	2.52	6.16
DFFSX4ADTH	2.52	7.28

Functional Schematic
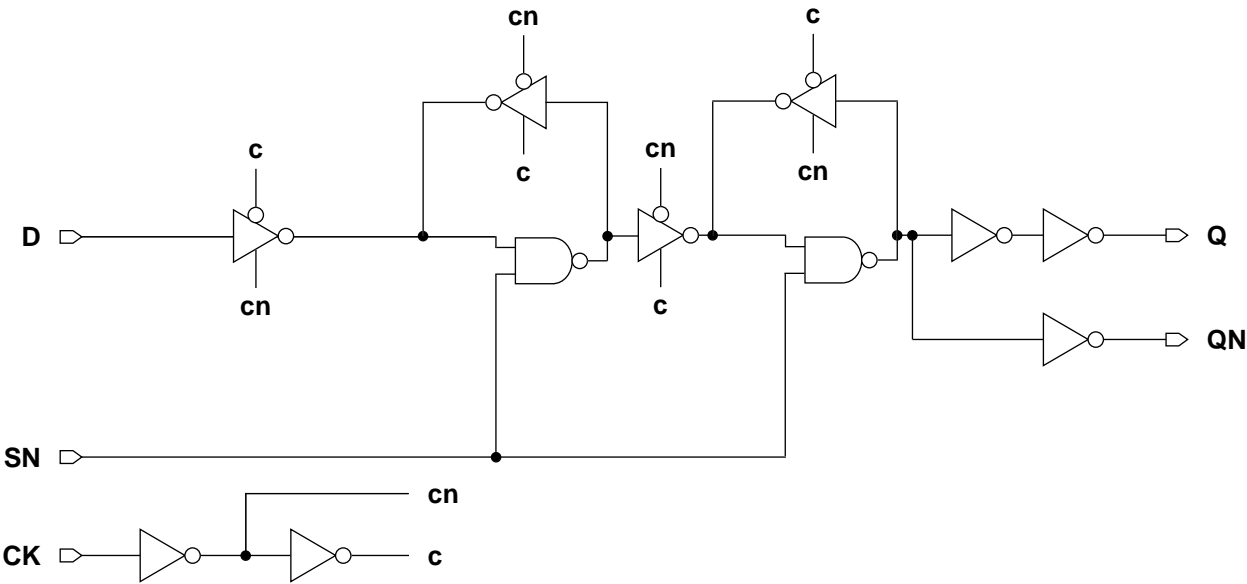
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0049	0.0050	0.0053	0.0068
CK	0.0104	0.0104	0.0109	0.0126
SN	0.0010	0.0010	0.0010	0.0013
Q	0.0050	0.0057	0.0077	0.0127

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0014	0.0014	0.0014	0.0015
CK	0.0019	0.0019	0.0020	0.0021
SN	0.0019	0.0019	0.0022	0.0028

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1955	0.2082	0.2121	0.2043	6.9957	4.6747	2.9132	1.4957
CK	→	Q	↓	0.1947	0.2055	0.2090	0.2101	5.6286	3.8895	1.7291	0.8755
SN	→	Q	↑	0.1628	0.1727	0.2120	0.2974	6.9518	4.6520	2.9094	1.4984
CK	→	QN	↑	0.1399	0.1427	0.1331	0.1188	7.3400	4.8540	2.9574	1.5228
CK	→	QN	↓	0.1474	0.1601	0.1443	0.1254	7.0861	4.7079	2.0334	0.9458
SN	→	QN	↓	0.1197	0.1292	0.1451	0.1991	6.1952	4.1818	1.9430	1.0519

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	CK	0.0859	0.0820	0.0742	0.0820
	setup	↓	→	CK	0.0234	0.0234	0.0234	0.0352
	hold	↑	→	CK	-0.0352	-0.0352	-0.0352	-0.0430
	hold	↓	→	CK	0.0156	0.0156	0.0156	0.0039
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0430	-0.0430	-0.0469	-0.0430
	removal				0.0703	0.0703	0.0703	0.0703

Cell Description

The DFFSHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low set (SN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol
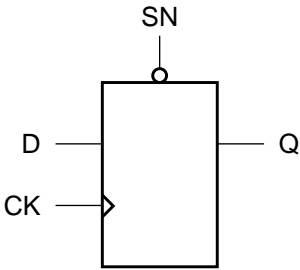
Function Table

SN	D	CK	Q[n+1]
0	x	x	1
1	0	⟋	0
1	1	⟋	1
1	x	⟍	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFSHQX1ADTH	2.52	7.84
DFFSHQX2ADTH	2.52	7.84
DFFSHQX4ADTH	2.52	9.24
DFFSHQX8ADTH	2.52	10.64

Functional Schematic
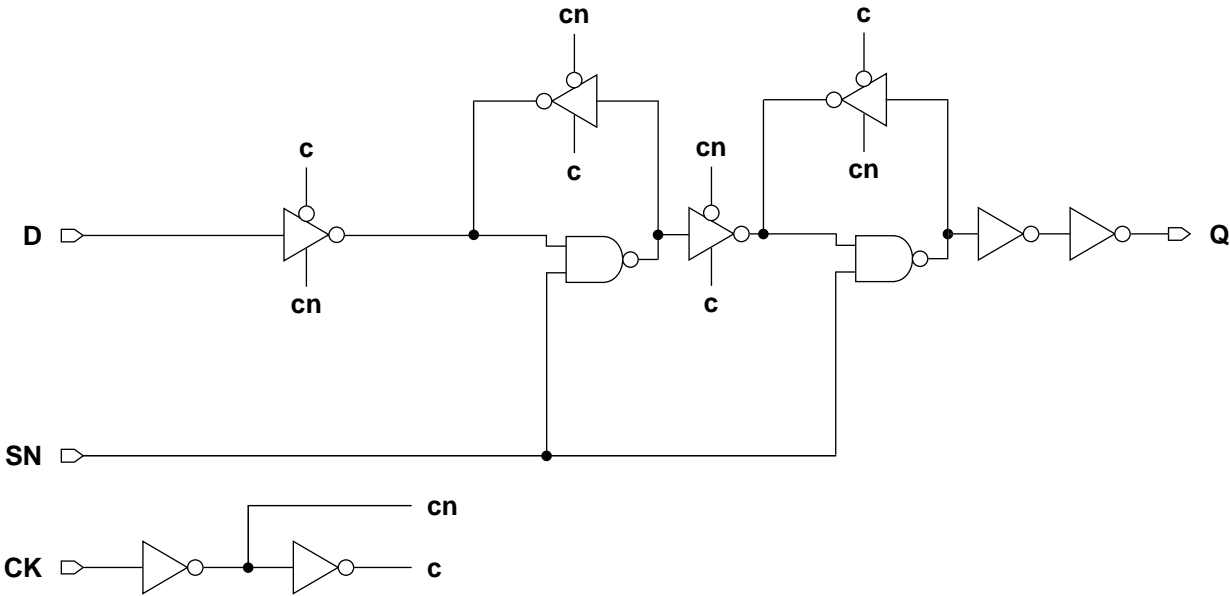
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
D	0.0063	0.0072	0.0101	0.0112
CK	0.0127	0.0145	0.0197	0.0217
SN	0.0032	0.0033	0.0039	0.0041
Q	0.0043	0.0052	0.0085	0.0133

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
D	0.0011	0.0011	0.0016	0.0024
CK	0.0021	0.0021	0.0031	0.0044
SN	0.0023	0.0026	0.0029	0.0029

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→	Q	↑	0.1049	0.1005	0.0917	0.0962	4.5164	2.8737	1.4609	0.7550
CK	→	Q	↓	0.1151	0.1143	0.1007	0.1028	4.0403	1.7855	0.8661	0.4443
SN	→	Q	↑	0.1624	0.1777	0.1504	0.1523	4.8901	2.9759	1.4564	0.7481

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
D	setup	↑	→	CK	0.0859	0.0664	0.0703	0.0742
	setup	↓	→	CK	0.0742	0.0742	0.0781	0.0781
	hold	↑	→	CK	-0.0273	-0.0156	-0.0117	-0.0039
	hold	↓	→	CK	-0.0352	-0.0312	-0.0273	-0.0234
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.0391	0.0352	0.0469	0.0625
	removal				-0.0234	-0.0195	-0.0273	-0.0352

Cell Description

The DFFSQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low set (SN). The cell has a single output (Q).

Logic Symbol
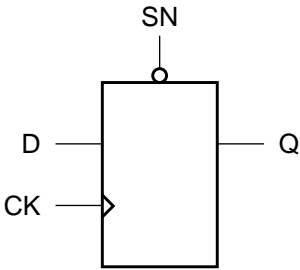
Function Table

SN	D	CK	Q[n+1]
0	x	x	1
1	0	⌐_	0
1	1	_⌐	1
1	x	‾⌐_	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFSQXLADTH	2.52	5.60
DFFSQX1ADTH	2.52	5.88
DFFSQX2ADTH	2.52	5.88
DFFSQX4ADTH	2.52	6.16

Functional Schematic

TSMC CLN90G HVT
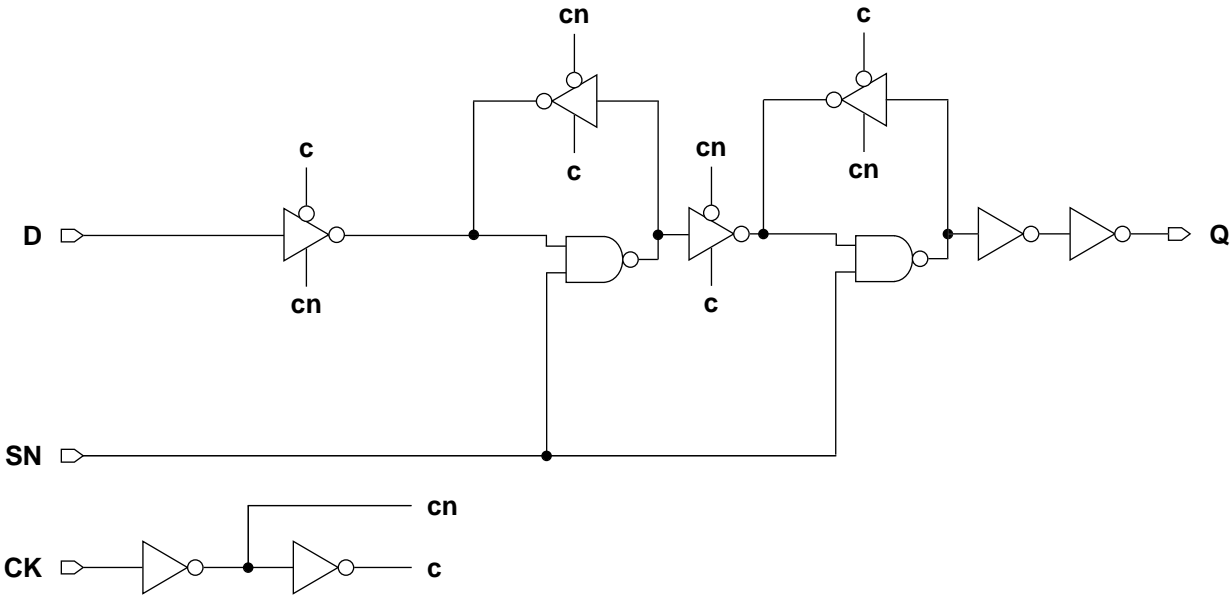
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0044	0.0044	0.0044	0.0044
CK	0.0098	0.0099	0.0099	0.0099
SN	0.0009	0.0010	0.0010	0.0010
Q	0.0039	0.0044	0.0053	0.0079

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0010	0.0010	0.0010	0.0010
CK	0.0019	0.0020	0.0019	0.0019
SN	0.0019	0.0019	0.0019	0.0019

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1598	0.1646	0.1755	0.1941	6.7711	4.4936	2.8899	1.4736
CK	→	Q	↓	0.1733	0.1833	0.1937	0.2101	5.6639	3.9576	1.7510	0.8880
SN	→	Q	↑	0.1389	0.1471	0.1544	0.1708	6.7476	4.4812	2.8851	1.4703

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	CK	0.0859	0.0859	0.0820	0.0781
	setup	↓	→	CK	0.0781	0.0781	0.0781	0.0781
	hold	↑	→	CK	-0.0234	-0.0273	-0.0273	-0.0273
	hold	↓	→	CK	-0.0078	-0.0117	-0.0117	-0.0117
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0312	-0.0312	-0.0352	-0.0352
	removal				0.0586	0.0547	0.0586	0.0586

Cell Description

The DFFSR cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset.

Logic Symbol
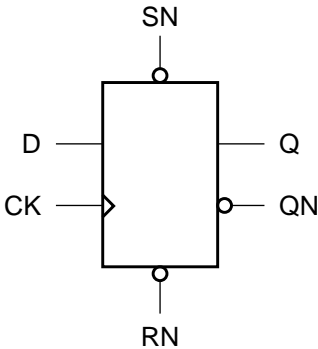
Function Table

RN	SN	D	CK	Q[n+1]	QN[n+1]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0
1	1	0	⌐	0	1
1	1	1	⌐	1	0
1	1	x	⌐	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFSRXLADTH	2.52	7.84
DFFSRX1ADTH	2.52	8.12
DFFSRX2ADTH	2.52	8.40
DFFSRX4ADTH	2.52	10.36

Functional Schematic
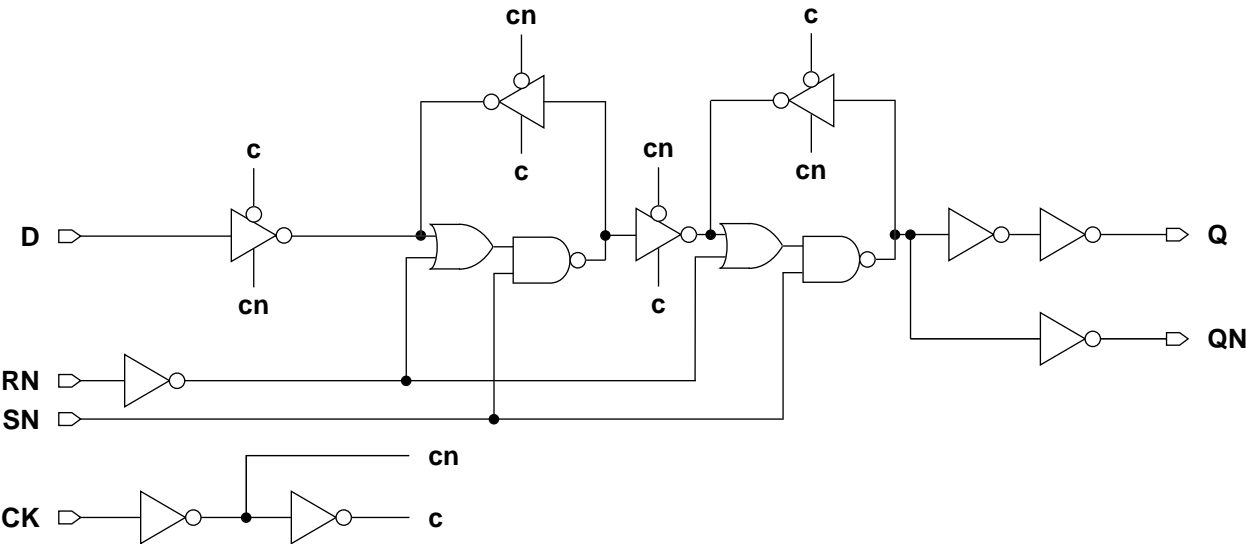
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0049	0.0049	0.0056	0.0083
CK	0.0105	0.0105	0.0116	0.0152
SN	0.0010	0.0010	0.0011	0.0013
RN	0.0022	0.0022	0.0023	0.0026
Q	0.0055	0.0063	0.0085	0.0126

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0010	0.0010	0.0010	0.0013
CK	0.0017	0.0017	0.0018	0.0021
SN	0.0020	0.0020	0.0023	0.0029
RN	0.0012	0.0012	0.0012	0.0012

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.2129	0.2260	0.2274	0.2084	7.0585	4.5639	2.9258	1.4973
CK	→	Q	↓	0.2072	0.2200	0.2183	0.2231	5.2655	3.9039	1.7171	0.8752
SN	→	Q	↑	0.1839	0.1944	0.2334	0.3160	6.9920	4.5250	2.9186	1.4993
SN	→	Q	↓	0.1636	0.1750	0.1916	0.2189	5.2224	3.8847	1.7134	0.8760
RN	→	Q	↓	0.1921	0.2036	0.2277	0.2748	5.2347	3.8899	1.7149	0.8762
CK	→	QN	↑	0.1491	0.1507	0.1444	0.1323	7.5832	4.8644	3.0113	1.5314
CK	→	QN	↓	0.1609	0.1753	0.1611	0.1284	7.2171	5.0513	2.1222	0.9664
SN	→	QN	↑	0.1074	0.1084	0.1154	0.1179	7.3053	4.7008	3.0047	1.5627
SN	→	QN	↓	0.1384	0.1491	0.1685	0.2163	5.9990	4.2879	1.9706	1.0661
RN	→	QN	↑	0.1345	0.1356	0.1508	0.1771	7.4042	4.7458	3.0180	1.5729

Timing Constraints at 25°C,1.0V, Typical Process

| Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	CK	0.1055	0.1016	0.0859	0.0898
	setup	↓	→	CK	0.0898	0.0898	0.0977	0.0938
	hold	↑	→	CK	-0.0273	-0.0273	-0.0312	-0.0312
	hold	↓	→	CK	-0.0156	-0.0195	-0.0195	-0.0156
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0312	-0.0312	-0.0430	-0.0508
	removal				0.0547	0.0547	0.0703	0.0820
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.0938	0.0898	0.0664	0.0703
	removal				-0.0312	-0.0312	-0.0234	-0.0195

Cell Description

The DFFSRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (RN) and set (SN), and set dominating reset. The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol
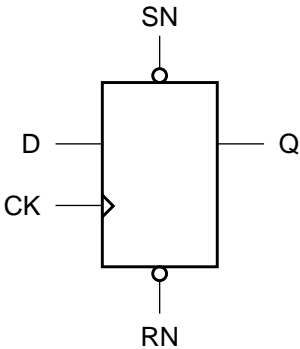
Function Table

RN	SN	D	CK	Q[n+1]
0	1	x	x	0
1	0	x	x	1
0	0	x	x	1
1	1	0	⌐	0
1	1	1	⌐	1
1	1	x	⌐	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFSRHQX1ADTH	2.52	9.24
DFFSRHQX2ADTH	2.52	9.24
DFFSRHQX4ADTH	2.52	11.76
DFFSRHQX8ADTH	2.52	13.16

Functional Schematic
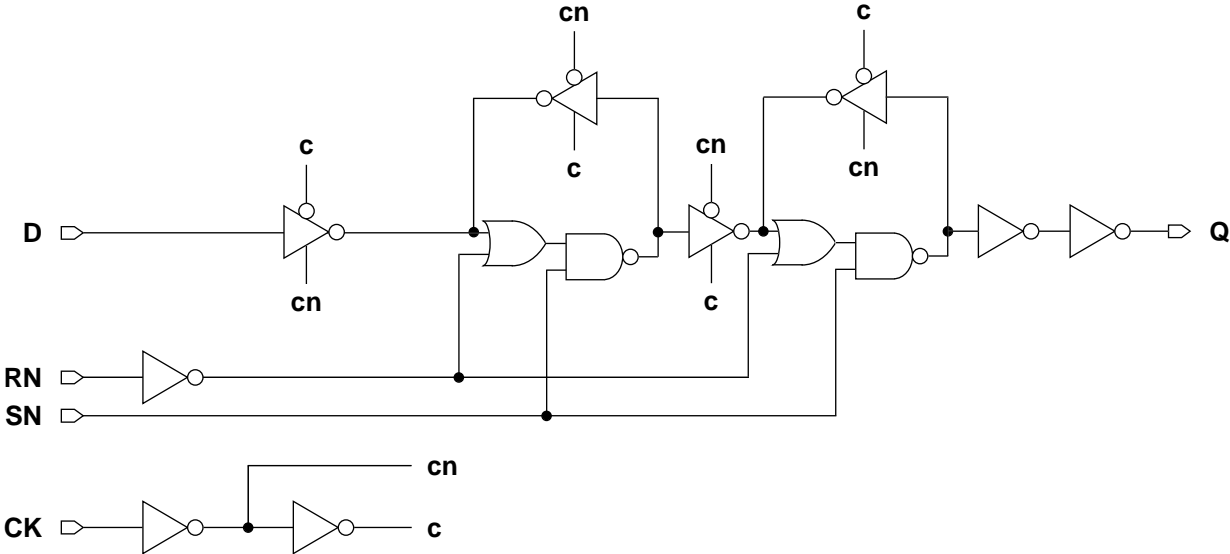
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
D	0.0069	0.0082	0.0123	0.0152
CK	0.0133	0.0152	0.0222	0.0276
SN	0.0039	0.0040	0.0050	0.0059
RN	0.0010	0.0012	0.0020	0.0026
Q	0.0047	0.0060	0.0090	0.0149

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
D	0.0012	0.0012	0.0015	0.0023
CK	0.0021	0.0021	0.0028	0.0040
SN	0.0022	0.0025	0.0032	0.0042
RN	0.0019	0.0022	0.0034	0.0040

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→ Q	↑	0.1259	0.1187	0.1114	0.1080	4.6865	2.9354	1.4826	0.7662
CK	→ Q	↓	0.1325	0.1225	0.1165	0.1080	4.3279	1.8512	0.8945	0.4539
SN	→ Q	↑	0.1393	0.1601	0.2088	0.1574	4.5560	2.9165	1.4823	0.7566
SN	→ Q	↓	0.2745	0.2586	0.2397	0.2409	4.7871	2.2064	1.0736	0.5432
RN	→ Q	↓	0.2426	0.2174	0.1886	0.2011	4.8150	2.2077	1.0754	0.5435

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
D	setup	↑	→	CK	0.1055	0.0859	0.0977	0.0781
	setup	↓	→	CK	0.0820	0.0742	0.0703	0.0742
	hold	↑	→	CK	-0.0312	-0.0234	-0.0273	-0.0078
	hold	↓	→	CK	-0.0312	-0.0273	-0.0195	-0.0195
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.0508	0.0352	0.0352	0.0469
	removal				-0.0273	-0.0195	-0.0195	-0.0234
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0117	-0.0195	-0.0195	-0.0078
	removal				0.0430	0.0547	0.0664	0.0586

Cell Description

The DFFTR cell is a positive-edge triggered, static D-type flip-flop with synchronous active-low reset (RN).

Logic Symbol
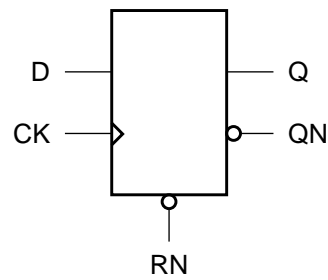
Function Table

RN	D	CK	Q[n+1]	QN[n+1]
0	x	⌐	0	1
x	x	⌐	Q[n]	QN[n]
1	0	⌐	0	1
1	1	⌐	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
DFFTRXLADTH	2.52	5.88
DFFTRX1ADTH	2.52	6.16
DFFTRX2ADTH	2.52	6.16
DFFTRX4ADTH	2.52	8.12

Functional Schematic
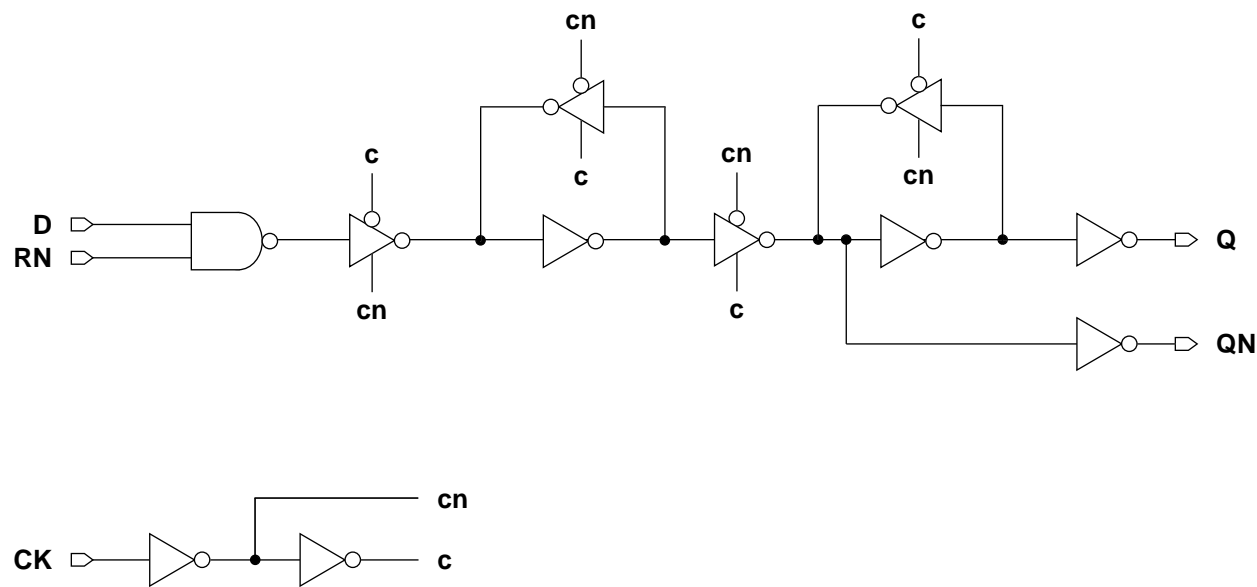
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0045	0.0049	0.0058	0.0093
CK	0.0100	0.0103	0.0115	0.0162
RN	0.0049	0.0052	0.0062	0.0100
Q	0.0051	0.0057	0.0077	0.0125

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0010	0.0010	0.0012	0.0019
CK	0.0016	0.0016	0.0017	0.0022
RN	0.0010	0.0010	0.0011	0.0015

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	$\rightarrow$	Q	$\uparrow$	0.1626	0.1572	0.1611	0.1485	6.9682	4.5070	2.9034	1.4823
CK	$\rightarrow$	Q	$\downarrow$	0.1801	0.1854	0.1917	0.1830	5.1819	3.8752	1.7052	0.8304
CK	$\rightarrow$	QN	$\uparrow$	0.1278	0.1222	0.1237	0.1203	7.1859	4.5529	2.9010	1.4992
CK	$\rightarrow$	QN	$\downarrow$	0.1182	0.1162	0.1097	0.0984	5.8378	4.0985	1.7406	0.8413

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	$\uparrow$	$\rightarrow$	CK	0.0977	0.0977	0.0781	0.0703
	setup	$\downarrow$	$\rightarrow$	CK	0.1289	0.1367	0.1094	0.0781
	hold	$\uparrow$	$\rightarrow$	CK	-0.0430	-0.0430	-0.0352	-0.0312
	hold	$\downarrow$	$\rightarrow$	CK	-0.0352	-0.0352	-0.0234	-0.0078
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
RN	setup	$\uparrow$	$\rightarrow$	CK	0.0977	0.1016	0.0820	0.0703
	setup	$\downarrow$	$\rightarrow$	CK	0.1367	0.1406	0.1641	0.1562
	hold	$\uparrow$	$\rightarrow$	CK	-0.0430	-0.0469	-0.0352	-0.0312
	hold	$\downarrow$	$\rightarrow$	CK	-0.0312	-0.0352	-0.0508	-0.0430

Cell Description

The DFFYQ cell is a positive-edge triggered, static D-type flip-flop to be used in synchronizing circuitry between asynchronous systems. The cell has a single output (Q) and overdriven feedback loops to increase MTBF due to metastability.

Logic Symbol
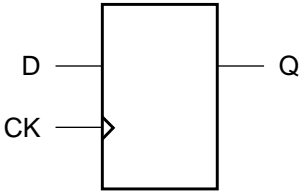
Function Table

D	CK	Q[n+1]
0	⌐⌐	0
1	⌐⌐	1
x	⌐⌐	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFYQX2ADTH	2.52	6.16

Functional Schematic
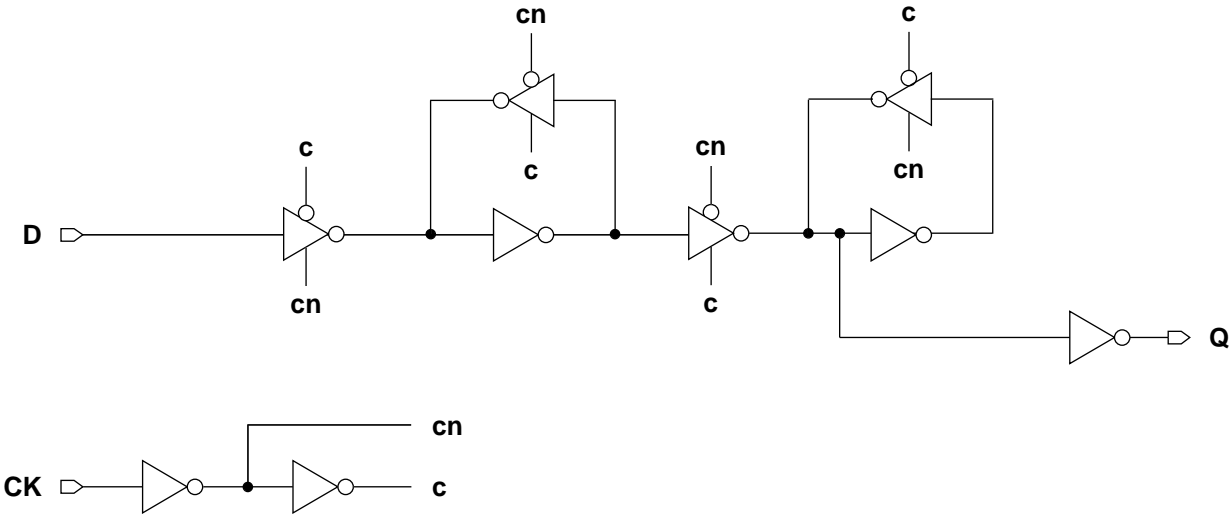
AC Power

Pin	Power (uW/MHz)
	X2
D	0.0087
CK	0.0159
Q	0.0051

Pin Capacitance

Pin	Capacitance (pF)
	X2
D	0.0022
CK	0.0025

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X2	**X2**
CK → Q ↑	0.1227	2.8586
CK → Q ↓	0.1343	1.8417

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)
		X2
D	setup ↑ → CK	0.0273
	setup ↓ → CK	0.0547
	hold ↑ → CK	-0.0195
	hold ↓ → CK	-0.0156
CK	minpwh	0.8332
	minpwl	0.8332

Cell Description

The DLY1 cell provides the logical delay of a
single input (A). The output (Y) is represented
by the logic equation:

$Y = A$

Logic Symbol

A ——□—— Y

Function Table

A	Y
0	0
1	1
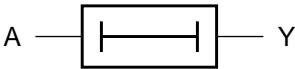
Cell Size

Drive Strength	Height (um)	Width (um)
DLY1X1ADTH	2.52	2.52
DLY1X4ADTH	2.52	3.08

Functional Schematic

A ▷———▷o———▷o———▷o———▷o———▷ Y

AC Power

Pin	Power (uW/MHz)	
	X1	**X4**
A	0.0054	0.0091

Pin Capacitance

Pin	Capacitance (pF)	
	X1	**X4**
A	0.0014	0.0019

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X1	**X4**	**X1**	**X4**
A → Y ↑	0.0839	0.0791	4.6661	1.4651
A → Y ↓	0.1060	0.1014	3.7649	1.7021

Cell Description

The DLY2 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Logic Symbol

A ⊣□⊢ Y

Function Table

A	Y
0	0
1	1
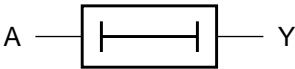
Cell Size

Drive Strength	Height (um)	Width (um)
DLY2X1ADTH	2.52	2.52
DLY2X4ADTH	2.52	3.08

Functional Schematic

A ▷ —▷○—▷○—▷○—▷○— ▷ Y

AC Power

Pin	Power (uW/MHz)	
	X1	**X4**
A	0.0063	0.0106

Pin Capacitance

Pin	Capacitance (pF)	
	X1	**X4**
A	0.0014	0.0019

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X1	**X4**	**X1**	**X4**
A → Y ↑	0.1589	0.1521	4.7209	1.4812
A → Y ↓	0.1763	0.1779	3.9906	1.7546

Cell Description

The DLY3 cell provides the logical delay of a
single input (A). The output (Y) is represented
by the logic equation:

Y = A

Logic Symbol

A ───┤ ├─── Y

Function Table

A	Y
0	0
1	1
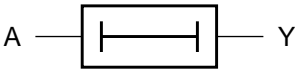
Cell Size

Drive Strength	Height (um)	Width (um)
DLY3X1ADTH	2.52	2.52
DLY3X4ADTH	2.52	3.08

Functional Schematic

A ▷───▷○──▷○──▷○──▷○───▷ Y

AC Power

Pin	Power (uW/MHz)	
	X1	**X4**
A	0.0073	0.0123

Pin Capacitance

Pin	Capacitance (pF)	
	X1	**X4**
A	0.0014	0.0020

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X1	**X4**	**X1**	**X4**
A → Y ↑	0.2511	0.2400	4.8057	1.5045
A → Y ↓	0.2510	0.2589	4.2788	1.8296

Cell Description

The DLY4 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Logic Symbol

A ――▭―― Y

Function Table

A	Y
0	0
1	1
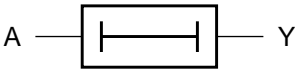
Cell Size

Drive Strength	Height (um)	Width (um)
DLY4X1ADTH	2.52	2.52
DLY4X4ADTH	2.52	3.08

Functional Schematic

A ▷———▷o———▷o———▷o———▷o———▷ Y

AC Power

Pin	Power (uW/MHz)	
	X1	**X4**
A	0.0084	0.0141

Pin Capacitance

Pin	Capacitance (pF)	
	X1	**X4**
A	0.0014	0.0020

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)		K_{load} (ns/pF)	
	X1	**X4**	**X1**	**X4**
A → Y ↑	0.3641	0.3478	4.9348	1.5429
A → Y ↓	0.3368	0.3510	4.6048	1.9205

Cell Description

The EDFF cell is a positive-edge triggered, static D-type flip-flop with synchronous active-high enable (E).

Logic Symbol
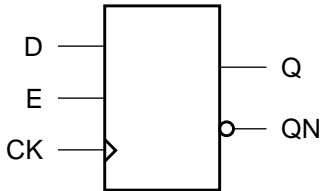
Function Table

E	D	CK	Q[n+1]	QN[n+1]
0	x	x	Q[n]	QN[n]
1	0	⌐	0	1
1	1	⌐	1	0
1	x	⌐	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
EDFFXLADTH	2.52	7.56
EDFFX1ADTH	2.52	7.56
EDFFX2ADTH	2.52	7.56
EDFFX4ADTH	2.52	10.08

Functional Schematic
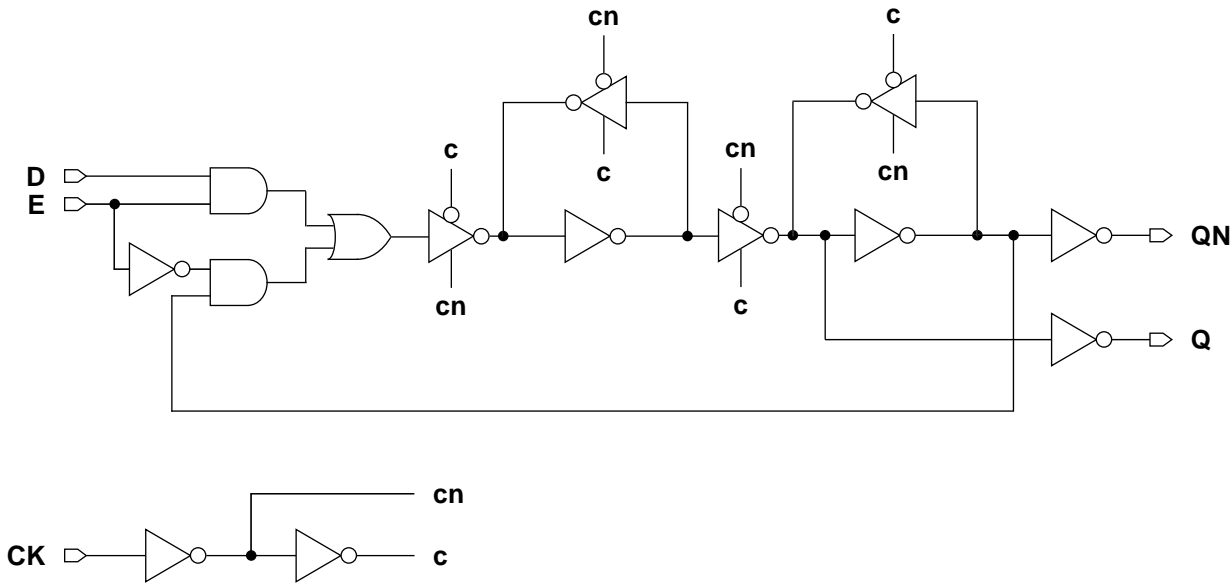
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0055	0.0056	0.0059	0.0068
CK	0.0099	0.0100	0.0104	0.0129
E	0.0081	0.0082	0.0085	0.0097
Q	0.0062	0.0070	0.0092	0.0154

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0014	0.0014	0.0014	0.0013
CK	0.0015	0.0015	0.0015	0.0017
E	0.0026	0.0026	0.0026	0.0026

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→ Q	↑	0.1394	0.1342	0.1370	0.1476	7.0705	4.4618	2.9340	1.4945
CK	→ Q	↓	0.1581	0.1521	0.1359	0.1365	6.6325	4.2708	1.8087	0.9065
CK	→ QN	↑	0.2264	0.2176	0.2006	0.2017	7.0899	4.5275	2.8883	1.4861
CK	→ QN	↓	0.2173	0.2209	0.2134	0.2174	5.9563	4.0489	1.7419	0.8432

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	CK	0.1133	0.1133	0.1172	0.1172
	setup	↓	→	CK	0.1133	0.1133	0.1211	0.1328
	hold	↑	→	CK	-0.0859	-0.0859	-0.0859	-0.0859
	hold	↓	→	CK	-0.0664	-0.0664	-0.0625	-0.0586
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
E	setup	↑	→	CK	0.1445	0.1445	0.1484	0.1602
	setup	↓	→	CK	0.1484	0.1484	0.1484	0.1484
	hold	↑	→	CK	-0.0938	-0.0938	-0.0938	-0.0938
	hold	↓	→	CK	-0.0586	-0.0547	-0.0547	-0.0508

Cell Description

The EDFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with a synchronous, active-high enable (E). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol
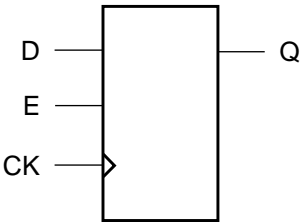
Function Table

E	D	CK	Q[n+1]
0	x	x	Q[n]
1	0	⌐_	0
1	1	⌐_	1
x	x	‾‾_	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
EDFFHQX1ADTH	2.52	8.68
EDFFHQX2ADTH	2.52	8.96
EDFFHQX4ADTH	2.52	11.76
EDFFHQX8ADTH	2.52	15.40

Functional Schematic
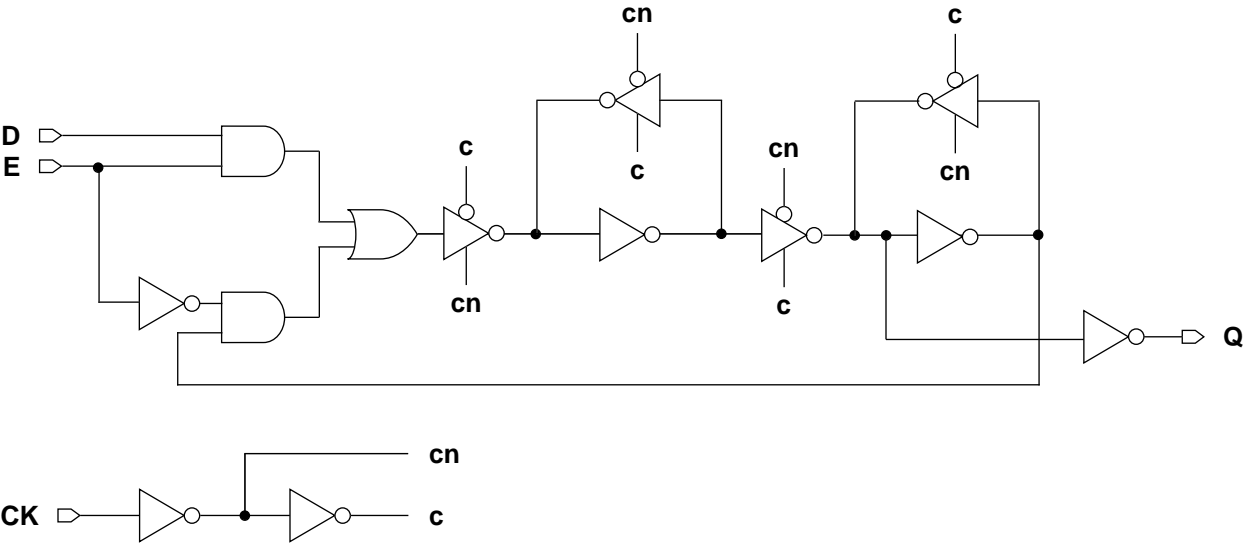
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
D	0.0086	0.0112	0.0168	0.0295
CK	0.0142	0.0168	0.0251	0.0365
E	0.0100	0.0114	0.0169	0.0263
Q	0.0046	0.0062	0.0092	0.0159

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
D	0.0017	0.0022	0.0037	0.0075
CK	0.0022	0.0024	0.0033	0.0044
E	0.0035	0.0035	0.0038	0.0058

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK → Q ↑	0.1073	0.1032	0.0913	0.0815	4.5076	2.8869	1.4608	0.7445
CK → Q ↓	0.1175	0.1113	0.0965	0.0875	4.0584	1.7550	0.8516	0.4165

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
D	setup	↑	→	CK	0.0938	0.0781	0.0703	0.0820
	setup	↓	→	CK	0.0898	0.0703	0.0742	0.0859
	hold	↑	→	CK	-0.0391	-0.0312	-0.0273	-0.0273
	hold	↓	→	CK	-0.0508	-0.0352	-0.0312	-0.0391
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
E	setup	↑	→	CK	0.0938	0.0742	0.0781	0.0938
	setup	↓	→	CK	0.1133	0.1250	0.1289	0.1406
	hold	↑	→	CK	-0.0586	-0.0430	-0.0391	-0.0469
	hold	↓	→	CK	-0.0859	-0.0898	-0.0977	-0.0898

Cell Description

The EDFFTR cell is a positive-edge triggered, static D-type flip-flop with synchronous active-high enable (E) and synchronous active-low reset (RN).

Logic Symbol

Function Table

RN	E	D	CK	Q[n+1]	QN[n+1]
0	x	x	⌐	0	1
x	x	x	⌐	Q[n]	QN[n]
1	0	x	⌐	Q[n]	QN[n]
1	1	0	⌐	0	1
1	1	1	⌐	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
EDFFTRXLADTH	2.52	8.68
EDFFTRX1ADTH	2.52	8.68
EDFFTRX2ADTH	2.52	8.68
EDFFTRX4ADTH	2.52	10.08

Functional Schematic

AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0048	0.0049	0.0051	0.0061
CK	0.0098	0.0100	0.0103	0.0123
E	0.0074	0.0075	0.0078	0.0088
RN	0.0053	0.0054	0.0057	0.0067
Q	0.0055	0.0063	0.0085	0.0142

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0011	0.0011	0.0011	0.0011
CK	0.0015	0.0015	0.0016	0.0018
E	0.0030	0.0030	0.0030	0.0029
RN	0.0010	0.0010	0.0010	0.0010

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1437	0.1397	0.1445	0.1358	7.1311	4.5733	2.9352	1.5012
CK	→	Q	↓	0.1559	0.1535	0.1407	0.1285	6.1473	4.2360	1.8029	0.8873
CK	→	QN	↑	0.2182	0.2119	0.2054	0.1926	7.0916	4.5637	2.9205	1.4869
CK	→	QN	↓	0.2167	0.2225	0.2270	0.2086	5.4855	4.0163	1.7569	0.8486

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	CK	0.1055	0.1055	0.1094	0.1211
	setup	↓	→	CK	0.2773	0.2773	0.2812	0.3047
	hold	↑	→	CK	-0.0859	-0.0859	-0.0859	-0.0898
	hold	↓	→	CK	-0.2188	-0.2148	-0.2148	-0.2266
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
E	setup	↑	→	CK	0.3047	0.3086	0.3086	0.3359
	setup	↓	→	CK	0.2344	0.2344	0.2344	0.2500
	hold	↑	→	CK	-0.0859	-0.0859	-0.0859	-0.0938
	hold	↓	→	CK	-0.1328	-0.1328	-0.1328	-0.1367
RN	setup	↑	→	CK	0.1133	0.1172	0.1172	0.1289
	setup	↓	→	CK	0.1992	0.1992	0.2031	0.2266
	hold	↑	→	CK	-0.0977	-0.0977	-0.0977	-0.1016
	hold	↓	→	CK	-0.1367	-0.1328	-0.1328	-0.1445

Cell Description

The INV cell provides the logical inversion of a single input (A). The output (Y) is represented by the logic equation:

$Y = \overline{A}$

Logic Symbol

A —▷o— Y

Function Table

A	Y
0	1
1	0
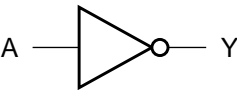
Cell Size

Drive Strength	Height (um)	Width (um)
INVXLADTH	2.52	0.84
INVX1ADTH	2.52	0.84
INVX2ADTH	2.52	0.84
INVX3ADTH	2.52	1.12
INVX4ADTH	2.52	1.12
INVX5ADTH	2.52	1.40
INVX6ADTH	2.52	1.68
INVX8ADTH	2.52	1.96
INVX10ADTH	2.52	2.24
INVX12ADTH	2.52	2.52
INVX14ADTH	2.52	3.08
INVX16ADTH	2.52	3.36
INVX18ADTH	2.52	3.64
INVX20ADTH	2.52	4.20

Functional Schematic

A ▷———▷o———▷ Y
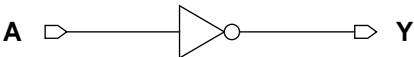
AC Power

Pin	Power (uW/MHz)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A	0.0011	0.0015	0.0025	0.0036	0.0045	0.0057	0.0069	0.0090

AC Power (Cont'd.)

Pin	Power (uW/MHz)					
	X10	**X12**	**X14**	**X16**	**X18**	**X20**
A	0.0115	0.0136	0.0161	0.0181	0.0205	0.0227

Pin Capacitance

Pin	Capacitance (pF)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A	0.0012	0.0016	0.0027	0.0041	0.0052	0.0064	0.0077	0.0103

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)					
	X10	**X12**	**X14**	**X16**	**X18**	**X20**
A	0.0129	0.0154	0.0180	0.0205	0.0232	0.0258

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)							
				XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A	→	Y	↑	0.0140	0.0133	0.0139	0.0137	0.0132	0.0134	0.0135	0.0135
A	→	Y	↓	0.0124	0.0125	0.0106	0.0102	0.0100	0.0102	0.0101	0.0100

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description				Intrinsic Delay (ns)					
				X10	**X12**	**X14**	**X16**	**X18**	**X20**
A	→	Y	↑	0.0137	0.0137	0.0139	0.0140	0.0141	0.0142
A	→	Y	↓	0.0101	0.0101	0.0102	0.0104	0.0104	0.0104

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Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A → Y ↑	6.6985	4.3418	2.8064	1.9315	1.4467	1.1565	0.9744	0.7367
A → Y ↓	5.3349	3.7587	1.6038	1.0388	0.7853	0.6389	0.5205	0.3882

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)					
	X10	**X12**	**X14**	**X16**	**X18**	**X20**
A → Y ↑	0.5940	0.4989	0.4289	0.3761	0.3355	0.3025
A → Y ↓	0.3135	0.2598	0.2219	0.1929	0.1718	0.1544

Cell Description

The MDFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with a 2-to-1data select control (S0) for the data inputs (D1,D0). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol
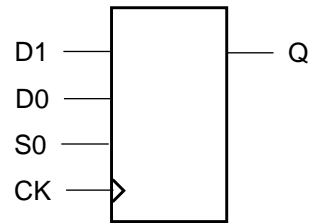
Function Table

S0	D1	D0	CK	Q[n+1]
0	x	0	⎍	0
0	x	1	⎍	1
1	0	x	⎍	0
1	1	x	⎍	1
x	x	x	⎍	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
MDFFHQX1ADTH	2.52	8.12
MDFFHQX2ADTH	2.52	8.40
MDFFHQX4ADTH	2.52	11.48
MDFFHQX8ADTH	2.52	16.80

Functional Schematic
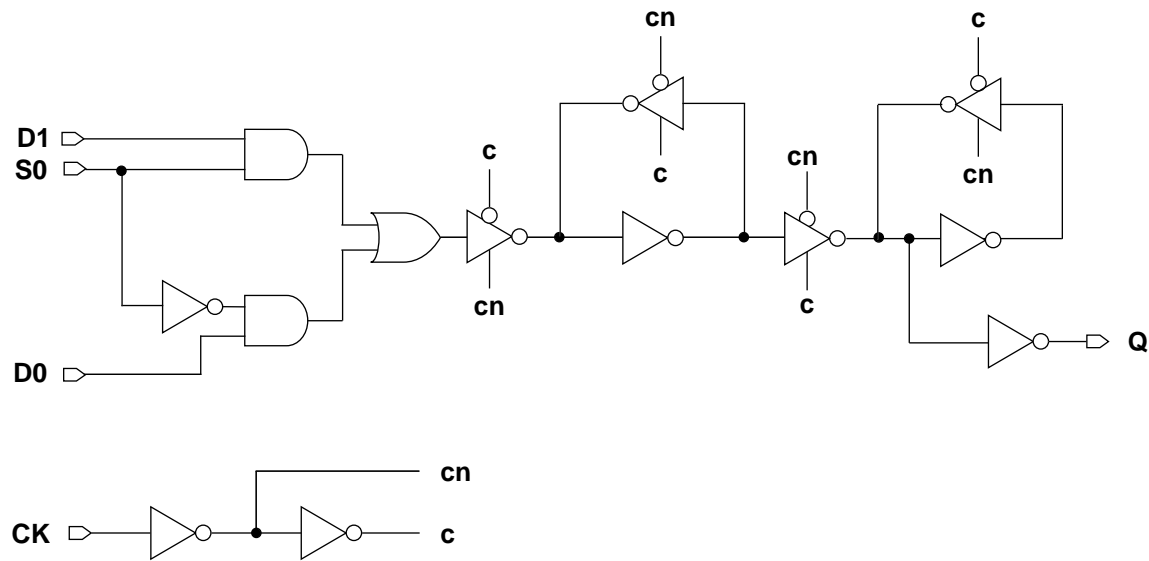
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
D0	0.0067	0.0092	0.0153	0.0259
D1	0.0072	0.0099	0.0169	0.0283
S0	0.0085	0.0111	0.0178	0.0305
CK	0.0126	0.0153	0.0246	0.0399
Q	0.0040	0.0053	0.0081	0.0133

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
D0	0.0012	0.0015	0.0025	0.0045
D1	0.0011	0.0016	0.0025	0.0045
S0	0.0022	0.0025	0.0030	0.0047
CK	0.0024	0.0024	0.0032	0.0052

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→ Q	↑	0.1041	0.0990	0.0917	0.0833	4.4813	2.8488	1.4501	0.7416
CK	→ Q	↓	0.1179	0.1131	0.1011	0.0885	4.0746	1.7399	0.8421	0.4098

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
D0	setup	↑	→	CK	0.1133	0.0977	0.0859	0.0781
	setup	↓	→	CK	0.1289	0.1094	0.0898	0.1055
	hold	↑	→	CK	-0.0625	-0.0469	-0.0352	-0.0273
	hold	↓	→	CK	-0.0859	-0.0664	-0.0508	-0.0586
D1	setup	↑	→	CK	0.1094	0.0898	0.0820	0.0742
	setup	↓	→	CK	0.1328	0.1133	0.0977	0.1133
	hold	↑	→	CK	-0.0586	-0.0430	-0.0312	-0.0234
	hold	↓	→	CK	-0.0898	-0.0703	-0.0586	-0.0664
S0	setup	↑	→	CK	0.1250	0.1094	0.0977	0.1172
	setup	↓	→	CK	0.1289	0.1211	0.1211	0.1211
	hold	↑	→	CK	-0.0469	-0.0312	-0.0195	-0.0117
	hold	↓	→	CK	-0.0781	-0.0625	-0.0469	-0.0547
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The MX2 cell is a 2-to-1 multiplexer. The state of the select input (S0) determines which data input (A,B) is presented to the output (Y). The output (Y) is represented by the logic equation:

$Y = (\overline{S0} \bullet A) + (S0 \bullet B)$

Logic Symbol
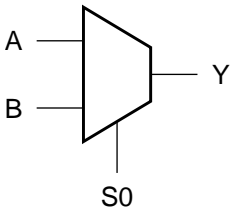
Function Table

S0	A	B	Y
0	0	x	0
0	1	x	1
1	x	0	0
1	x	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
MX2XLADTH	2.52	2.52
MX2X1ADTH	2.52	2.52
MX2X2ADTH	2.52	3.08
MX2X3ADTH	2.52	3.36
MX2X4ADTH	2.52	3.36
MX2X6ADTH	2.52	3.92
MX2X8ADTH	2.52	4.20

Functional Schematic
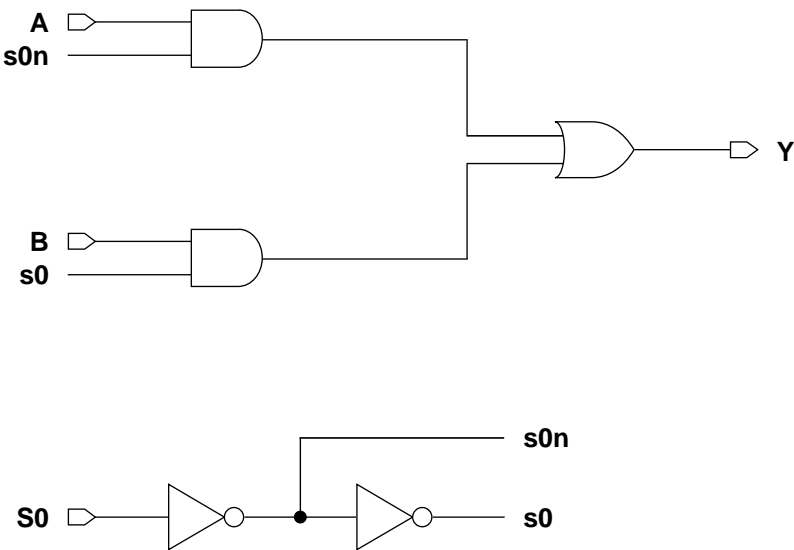
AC Power

Pin	Power (uW/MHz)						
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
S0	0.0043	0.0053	0.0089	0.0107	0.0116	0.0140	0.0164
A	0.0034	0.0043	0.0070	0.0090	0.0099	0.0130	0.0159
B	0.0038	0.0048	0.0077	0.0101	0.0110	0.0141	0.0170

Pin Capacitance

Pin	Capacitance (pF)						
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
S0	0.0026	0.0029	0.0041	0.0046	0.0046	0.0047	0.0047
A	0.0013	0.0016	0.0024	0.0028	0.0028	0.0028	0.0028
B	0.0013	0.0015	0.0022	0.0025	0.0025	0.0025	0.0025

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)						
				XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
S0	→	Y	↑	0.0798	0.0779	0.0911	0.0878	0.0898	0.0954	0.1018
S0	→	Y	↓	0.0865	0.0814	0.0808	0.0799	0.0838	0.0962	0.1115
A	→	Y	↑	0.0642	0.0576	0.0577	0.0588	0.0608	0.0692	0.0765
A	→	Y	↓	0.0950	0.0861	0.0790	0.0806	0.0862	0.0989	0.1109
B	→	Y	↑	0.0621	0.0552	0.0533	0.0541	0.0563	0.0648	0.0722
B	→	Y	↓	0.0968	0.0869	0.0801	0.0820	0.0867	0.1009	0.1130

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)						
				XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
S0	→	Y	↑	6.9944	4.4737	2.9190	2.0133	1.4903	1.0069	0.7628
S0	→	Y	↓	6.0567	3.8524	1.7204	1.1370	0.8754	0.5998	0.4646
A	→	Y	↑	6.9935	4.4703	2.9174	2.0124	1.4903	1.0071	0.7631
A	→	Y	↓	6.0262	3.8532	1.7276	1.1476	0.8800	0.6008	0.4649
B	→	Y	↑	6.9972	4.4722	2.9177	2.0124	1.4903	1.0072	0.7633
B	→	Y	↓	6.0604	3.8537	1.7203	1.1372	0.8692	0.6001	0.4645

Process Technology:
TSMC CLN90G HVT

Cell Description

The MX3 cell is a 3-to-1 multiplexer. The state of the select inputs (S1,S0) determines which data input (A,B,C) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (\overline{S0} \bullet \overline{S1} \bullet A) + (S0 \bullet \overline{S1} \bullet B) + (S1 \bullet C)$$

Logic Symbol
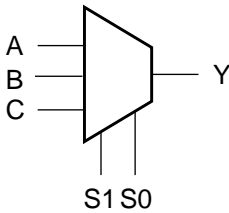
Function Table

S1	S0	A	B	C	Y
0	0	0	x	x	0
0	0	1	x	x	1
0	1	x	0	x	0
0	1	x	1	x	1
1	x	x	x	0	0
1	x	x	x	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
MX3XLADTH	2.52	5.04
MX3X1ADTH	2.52	5.04
MX3X2ADTH	2.52	5.60
MX3X4ADTH	2.52	6.16

Functional Schematic
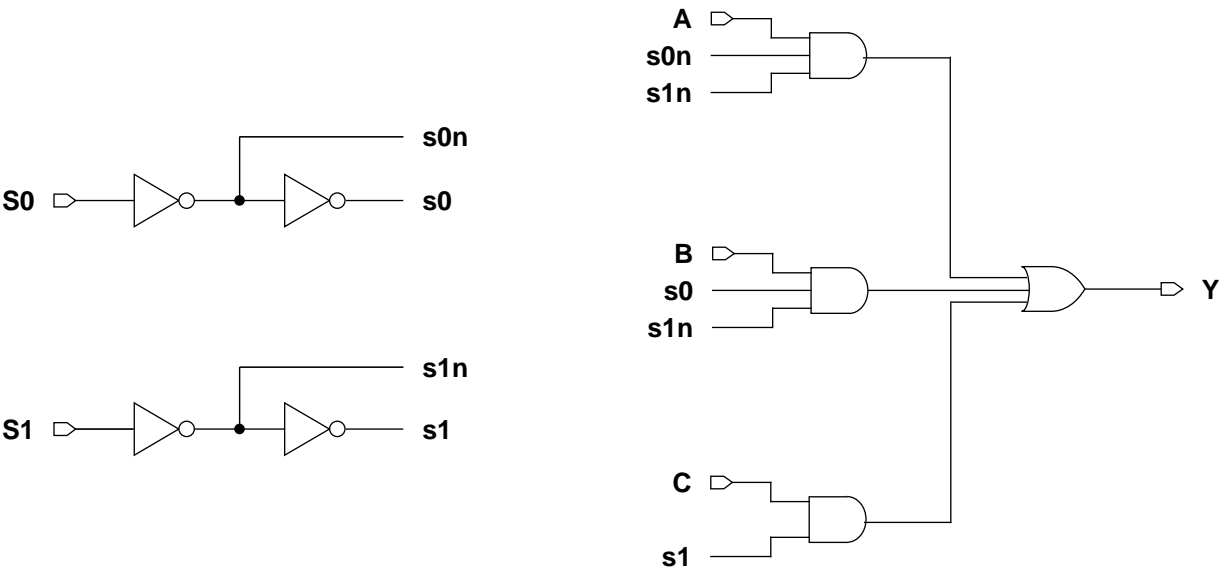
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
S0	0.0068	0.0085	0.0123	0.0145
S1	0.0051	0.0062	0.0082	0.0107
A	0.0058	0.0075	0.0106	0.0135
B	0.0064	0.0082	0.0118	0.0147
C	0.0046	0.0057	0.0092	0.0123

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
S0	0.0028	0.0033	0.0054	0.0054
S1	0.0028	0.0031	0.0040	0.0043
A	0.0015	0.0020	0.0027	0.0027
B	0.0014	0.0018	0.0026	0.0026
C	0.0011	0.0014	0.0023	0.0027

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
S0	→ Y	↑	0.1137	0.1136	0.1117	0.1224	7.0428	4.4838	2.8665	1.4734
S0	→ Y	↓	0.1370	0.1308	0.1235	0.1436	6.2918	4.3817	1.9397	0.9951
S1	→ Y	↑	0.0860	0.0854	0.0810	0.0904	7.0314	4.4850	2.8660	1.4741
S1	→ Y	↓	0.0884	0.0875	0.0753	0.0931	5.6930	4.1038	1.8195	0.9883
A	→ Y	↑	0.0980	0.0926	0.0882	0.0996	7.0461	4.4843	2.8674	1.4738
A	→ Y	↓	0.1386	0.1308	0.1226	0.1407	6.2973	4.3821	1.9408	0.9951
B	→ Y	↑	0.0962	0.0924	0.0861	0.0976	7.0437	4.4907	2.8684	1.4750
B	→ Y	↓	0.1427	0.1352	0.1283	0.1463	6.3156	4.3918	1.9458	0.9974
C	→ Y	↑	0.0719	0.0672	0.0613	0.0625	6.8968	4.4252	2.8431	1.4505
C	→ Y	↓	0.1087	0.1004	0.0894	0.0928	5.7097	4.1077	1.7822	0.8823

Cell Description

The MX4 cell is a 4-to-1 multiplexer. The state of the select inputs (S1,S0) determines which data input (A,B,C,D) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (\overline{S0}\bullet\overline{S1}\bullet A) + (S0\bullet\overline{S1}\bullet B) + (\overline{S0}\bullet S1\bullet C) + (S0\bullet S1\bullet D)$$

Logic Symbol
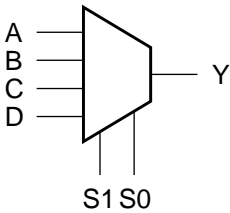
Function Table

S1	S0	A	B	C	D	Y
0	0	0	x	x	x	0
0	0	1	x	x	x	1
0	1	x	0	x	x	0
0	1	x	1	x	x	1
1	0	x	x	0	x	0
1	0	x	x	1	x	1
1	1	x	x	x	0	0
1	1	x	x	x	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
MX4XLADTH	2.52	6.72
MX4X1ADTH	2.52	7.00
MX4X2ADTH	2.52	7.28
MX4X4ADTH	2.52	7.84

Functional Schematic
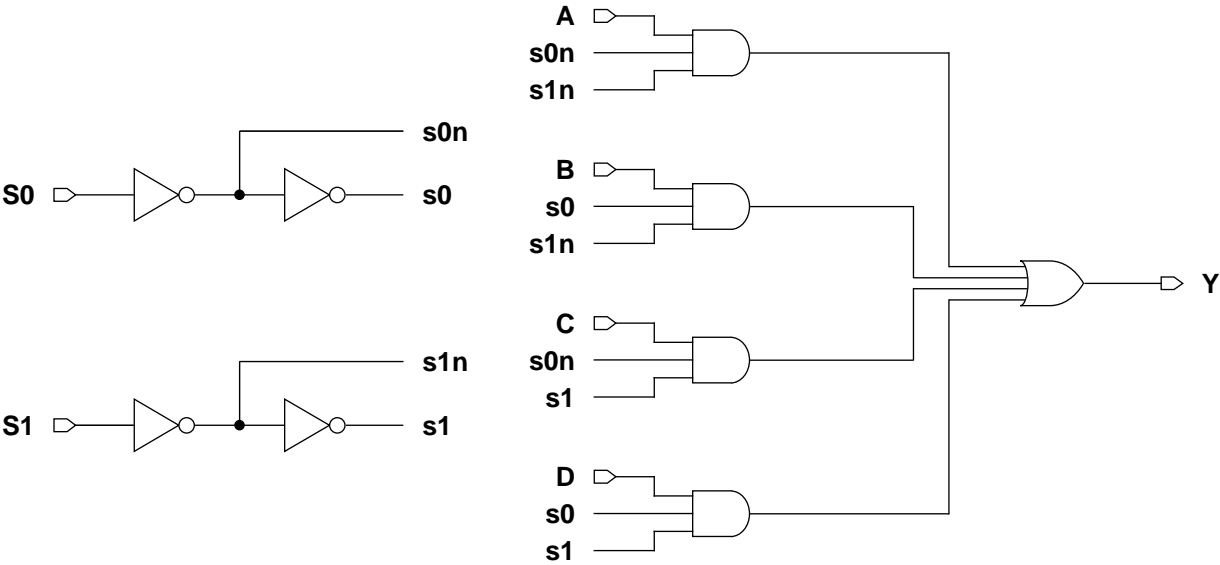
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
S0	0.0122	0.0144	0.0202	0.0232
S1	0.0050	0.0060	0.0087	0.0110
A	0.0058	0.0071	0.0106	0.0136
B	0.0064	0.0080	0.0118	0.0147
C	0.0074	0.0088	0.0128	0.0158
D	0.0077	0.0092	0.0136	0.0166

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
S0	0.0065	0.0074	0.0101	0.0101
S1	0.0033	0.0034	0.0044	0.0044
A	0.0015	0.0018	0.0026	0.0026
B	0.0014	0.0017	0.0025	0.0025
C	0.0014	0.0019	0.0027	0.0027
D	0.0013	0.0018	0.0026	0.0026

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
S0	→ Y	↑	0.1339	0.1158	0.1089	0.1200	7.0612	4.9684	2.9031	1.4758
S0	→ Y	↓	0.1711	0.1480	0.1407	0.1606	6.9880	4.4297	1.9603	1.0020
S1	→ Y	↑	0.0809	0.0849	0.0806	0.0906	6.9762	5.0078	2.8996	1.4756
S1	→ Y	↓	0.0803	0.0847	0.0830	0.1015	6.8417	4.4365	1.9517	1.0025
A	→ Y	↑	0.0950	0.0879	0.0859	0.0978	6.9840	4.9540	2.8991	1.4748
A	→ Y	↓	0.1374	0.1344	0.1240	0.1423	6.8060	4.4456	1.9461	0.9949
B	→ Y	↑	0.0948	0.1021	0.0862	0.0982	6.9845	5.0138	2.9011	1.4764
B	→ Y	↓	0.1411	0.1302	0.1268	0.1452	6.8067	4.3708	1.9462	0.9946
C	→ Y	↑	0.1034	0.0908	0.0876	0.0990	7.0531	4.9657	2.9027	1.4769
C	→ Y	↓	0.1551	0.1375	0.1335	0.1520	6.9943	4.4324	1.9612	1.0020
D	→ Y	↑	0.0990	0.0923	0.0867	0.0984	7.0327	4.9865	2.9046	1.4786
D	→ Y	↓	0.1555	0.1478	0.1368	0.1557	6.9870	4.4800	1.9677	1.0059

Cell Description

The MXI2 cell is a 2-to-1 multiplexer with inverted output. The state of the select input (S0) determines which data input (A,B) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{S0} \bullet A) + (S0 \bullet B)}$$

Logic Symbol

A — [▷] — Y
B —
S0
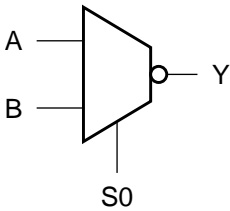
Function Table

S0	A	B	Y
0	0	x	1
0	1	x	0
1	x	0	1
1	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
MXI2XLADTH	2.52	2.24
MXI2X1ADTH	2.52	2.24
MXI2X2ADTH	2.52	3.08
MXI2X3ADTH	2.52	4.48
MXI2X4ADTH	2.52	4.48
MXI2X6ADTH	2.52	6.16
MXI2X8ADTH	2.52	8.68

Functional Schematic

A
s0n

B
s0

Y

s0n
S0
s0
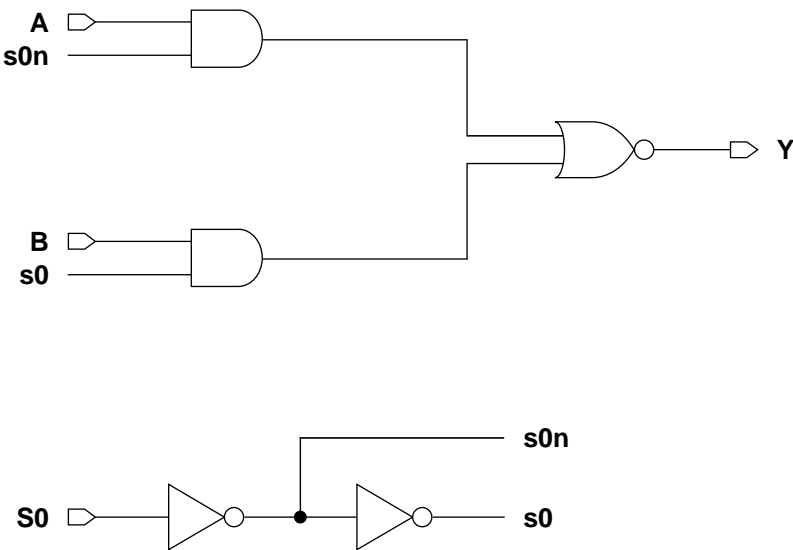
AC Power

Pin	Power (uW/MHz)						
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
S0	0.0035	0.0044	0.0066	0.0102	0.0127	0.0163	0.0233
A	0.0024	0.0031	0.0056	0.0088	0.0103	0.0149	0.0204
B	0.0029	0.0038	0.0067	0.0098	0.0119	0.0177	0.0253

Pin Capacitance

Pin	Capacitance (pF)						
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
S0	0.0027	0.0031	0.0044	0.0068	0.0078	0.0111	0.0156
A	0.0013	0.0016	0.0027	0.0043	0.0052	0.0075	0.0099
B	0.0014	0.0017	0.0026	0.0040	0.0050	0.0076	0.0100

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)						
				XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
S0	→	Y	↑	0.0358	0.0352	0.0385	0.0392	0.0396	0.0327	0.0340
S0	→	Y	↓	0.0452	0.0474	0.0480	0.0501	0.0560	0.0417	0.0428
A	→	Y	↑	0.0377	0.0331	0.0364	0.0382	0.0357	0.0349	0.0357
A	→	Y	↓	0.0333	0.0323	0.0273	0.0295	0.0285	0.0266	0.0270
B	→	Y	↑	0.0399	0.0364	0.0405	0.0400	0.0372	0.0383	0.0400
B	→	Y	↓	0.0324	0.0307	0.0248	0.0246	0.0231	0.0227	0.0239

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)						
				XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
S0	→	Y	↑	10.2592	6.8232	4.0595	2.7230	2.1876	1.4540	1.0556
S0	→	Y	↓	7.2578	5.0901	2.2681	1.5517	1.2001	0.8150	0.5837
A	→	Y	↑	10.1202	6.7452	4.0418	2.7072	2.1598	1.4526	1.0585
A	→	Y	↓	7.8199	5.4554	2.3965	1.6445	1.2742	0.8505	0.6126
B	→	Y	↑	10.0195	6.7927	4.0108	2.7402	2.1182	1.4658	1.0513
B	→	Y	↓	7.8264	5.4744	2.3779	1.6356	1.2600	0.8289	0.6025

Cell Description

The MXI2D cell is a 2-to-1 multiplexer with inverted output. The state of the select input (S0) determines which data input (A, B) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{S0} \bullet A) + (S0 \bullet B)}$$

Note: The MXI2D cell architecture uses transmission gate inputs for the data input pins and a double-buffered select signal to minimize the risk associated with transmission gate inputs. Do not drive MXI2D inputs from MXI2, ACCSHCIN, ACCSHCON, ACHCIN, ACHCON, ADDH, AFHCIN, AFHCON, AHHCIN, and AHHCON cells. Furthermore, special care should be taken in designs that use multiple voltage domains for standard cell regions. Do not allow high voltage signals to be coupled into the input pins, A and B, when the cell is used in a low voltage domain; otherwise, it may be possible for the cell to latch. If your design methodology does not permit cells with transmission gate inputs, the MXI2 cell may be used as an alternative.

Logic Symbol
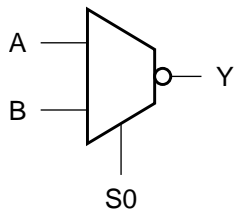
Function Table

S0	A	B	Y
0	0	x	1
0	1	x	0
1	x	0	1
1	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
MXI2DXLADTH	2.52	2.80
MXI2DX1ADTH	2.52	2.80
MXI2DX2ADTH	2.52	2.80
MXI2DX4ADTH	2.52	4.20

Functional Schematic
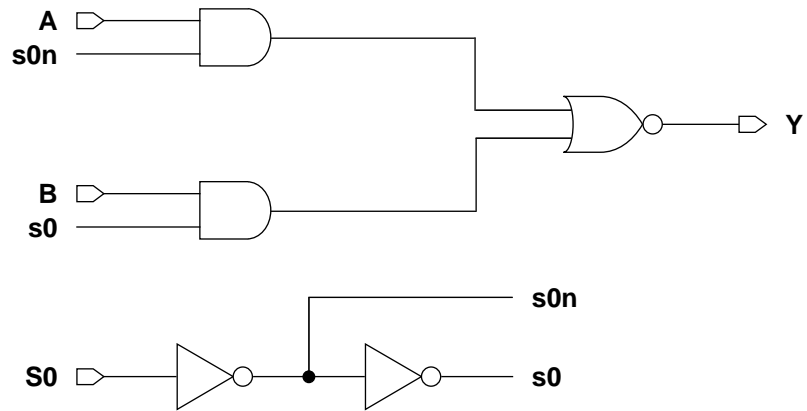
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
S0	0.0053	0.0062	0.0086	0.0153
A	0.0022	0.0029	0.0046	0.0087
B	0.0023	0.0030	0.0047	0.0090

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
S0	0.0012	0.0012	0.0016	0.0025
A	0.0035	0.0046	0.0071	0.0138
B	0.0041	0.0051	0.0076	0.0145

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
S0	→ Y	↑	0.1118	0.1152	0.1040	0.0925	6.7392	4.4197	2.8223	1.4357
S0	→ Y	↓	0.1306	0.1186	0.1041	0.0931	5.6558	3.8719	1.6526	0.8082
A	→ Y	↑	0.0350	0.0315	0.0294	0.0289	6.7313	4.4151	2.8220	1.4352
A	→ Y	↓	0.0390	0.0364	0.0313	0.0303	5.6512	3.8684	1.6506	0.8074
B	→ Y	↑	0.0371	0.0335	0.0317	0.0303	6.7339	4.4165	2.8223	1.4357
B	→ Y	↓	0.0400	0.0369	0.0316	0.0293	5.6531	3.8713	1.6568	0.8082

Cell Description

The MXI3 cell is a 3-to-1 multiplexer with inverted output. The state of the select inputs (S1,S0) determines which data input (A,B,C) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (S0 \bullet S1 \bullet \overline{A}) + (\overline{S0} \bullet S1 \bullet \overline{B}) + (\overline{S1} \bullet \overline{C})$$

Logic Symbol
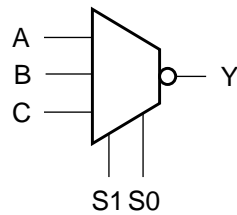
Function Table

S1	S0	A	B	C	Y
0	0	0	x	x	1
0	0	1	x	x	0
0	1	x	0	x	1
0	1	x	1	x	0
1	0	x	x	0	1
1	0	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
MXI3XLADTH	2.52	5.32
MXI3X1ADTH	2.52	5.32
MXI3X2ADTH	2.52	5.60
MXI3X4ADTH	2.52	6.44

Functional Schematic
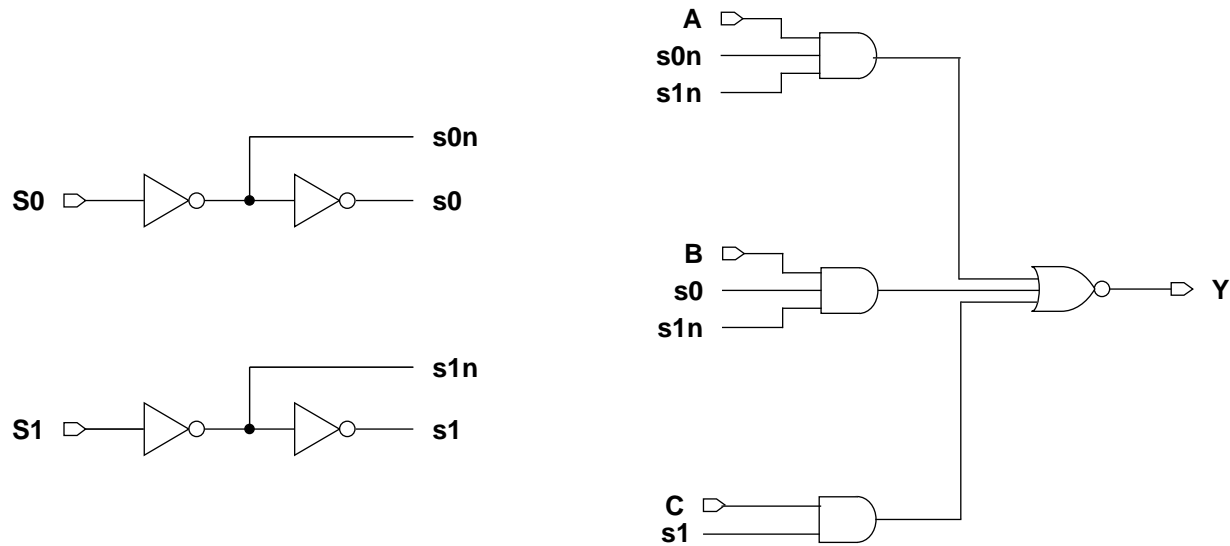
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
S0	0.0071	0.0083	0.0118	0.0166
S1	0.0044	0.0054	0.0079	0.0105
A	0.0061	0.0073	0.0109	0.0150
B	0.0061	0.0075	0.0114	0.0163
C	0.0043	0.0053	0.0079	0.0109

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
S0	0.0025	0.0026	0.0032	0.0038
S1	0.0019	0.0020	0.0025	0.0025
A	0.0013	0.0014	0.0020	0.0022
B	0.0012	0.0013	0.0020	0.0022
C	0.0013	0.0012	0.0013	0.0015

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
S0	→	Y	↑	0.1563	0.1490	0.1341	0.1523	7.0259	4.4570	2.8933	1.4555
S0	→	Y	↓	0.1719	0.1618	0.1493	0.1682	6.2294	4.0586	1.7890	0.8915
S1	→	Y	↑	0.0813	0.0806	0.0851	0.0841	6.9984	4.4449	2.8904	1.4530
S1	→	Y	↓	0.0893	0.0835	0.0765	0.0882	6.2112	4.0450	1.7853	0.9093
A	→	Y	↑	0.1723	0.1612	0.1391	0.1469	7.0149	4.4520	2.8917	1.4553
A	→	Y	↓	0.1624	0.1489	0.1255	0.1379	6.2159	4.0519	1.7868	0.8917
B	→	Y	↑	0.1658	0.1582	0.1395	0.1547	7.0237	4.4562	2.8934	1.4551
B	→	Y	↓	0.1552	0.1440	0.1216	0.1347	6.2279	4.0576	1.7884	0.8916
C	→	Y	↑	0.1029	0.0994	0.1030	0.1027	6.9813	4.4374	2.8872	1.4490
C	→	Y	↓	0.1227	0.1130	0.1042	0.1201	6.2120	4.0428	1.7849	0.9098

TSMC CLN90G HVT

Cell Description

The MXI4 cell is a 4-to-1 multiplexer with inverted output. The state of the select inputs (S1,S0) determines which data input (A,B,C,D) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{S0}\bullet\overline{S1}\bullet A) + (S0\bullet\overline{S1}\bullet B) + (\overline{S0}\bullet S1\bullet C) + (S0\bullet S1\bullet D)}$$

Logic Symbol
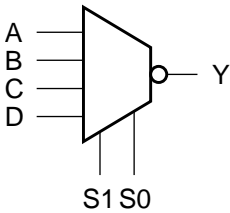
Function Table

S1	S0	A	B	C	D	Y
0	0	0	x	x	x	1
0	0	1	x	x	x	0
0	1	x	0	x	x	1
0	1	x	1	x	x	0
1	0	x	x	0	x	1
1	0	x	x	1	x	0
1	1	x	x	x	0	1
1	1	x	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
MXI4XLADTH	2.52	7.00
MXI4X1ADTH	2.52	7.00
MXI4X2ADTH	2.52	7.00
MXI4X4ADTH	2.52	7.56

Functional Schematic
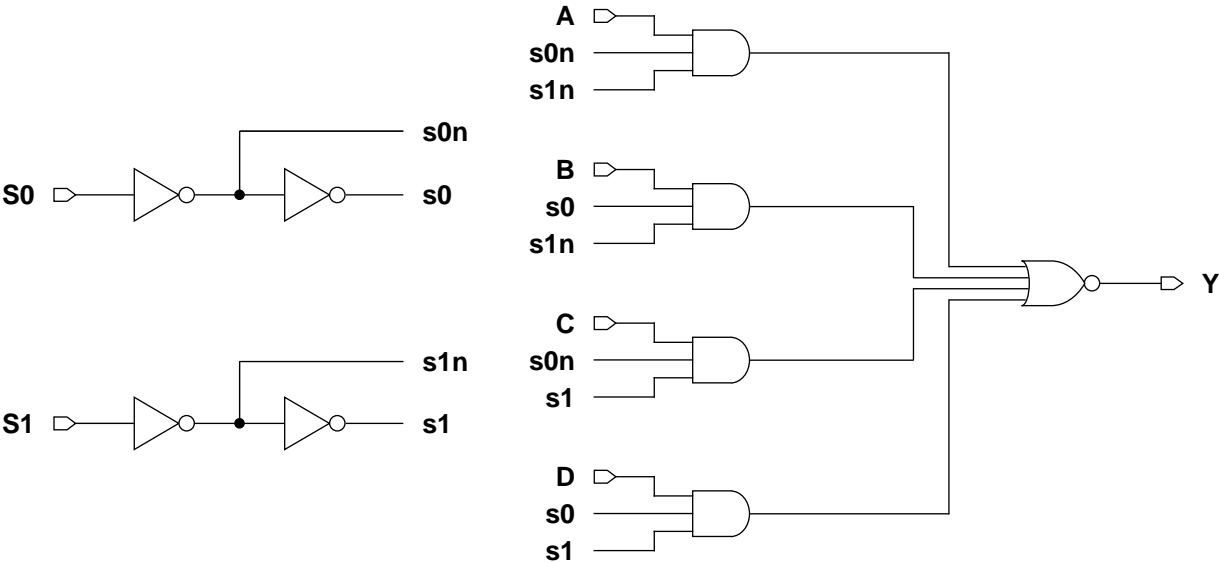
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
S0	0.0116	0.0135	0.0194	0.0246
S1	0.0046	0.0056	0.0083	0.0106
A	0.0061	0.0073	0.0110	0.0152
B	0.0066	0.0078	0.0117	0.0159
C	0.0054	0.0065	0.0099	0.0131
D	0.0058	0.0070	0.0106	0.0138

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
S0	0.0040	0.0042	0.0058	0.0067
S1	0.0020	0.0020	0.0024	0.0024
A	0.0012	0.0013	0.0019	0.0021
B	0.0012	0.0013	0.0019	0.0020
C	0.0013	0.0015	0.0020	0.0024
D	0.0012	0.0013	0.0018	0.0019

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
S0	→	Y	↑	0.1703	0.1626	0.1413	0.1552	6.9417	4.4333	2.8386	1.4841
S0	→	Y	↓	0.1960	0.1902	0.1636	0.1611	6.3842	4.1801	1.8120	0.9033
S1	→	Y	↑	0.0845	0.0831	0.0899	0.0846	6.9007	4.4179	2.8351	1.4818
S1	→	Y	↓	0.0938	0.0895	0.0809	0.0895	6.4158	4.1725	1.7859	0.9028
A	→	Y	↑	0.1670	0.1592	0.1392	0.1527	6.9402	4.4331	2.8384	1.4837
A	→	Y	↓	0.1629	0.1544	0.1358	0.1373	6.3843	4.1791	1.8110	0.8848
B	→	Y	↑	0.1739	0.1655	0.1430	0.1600	6.9421	4.4335	2.8384	1.4838
B	→	Y	↓	0.1619	0.1531	0.1337	0.1380	6.3841	4.1795	1.8113	0.8850
C	→	Y	↑	0.1563	0.1486	0.1313	0.1276	6.9293	4.4260	2.8323	1.4789
C	→	Y	↓	0.1563	0.1470	0.1258	0.1368	6.4233	4.1759	1.7870	0.9037
D	→	Y	↑	0.1571	0.1483	0.1299	0.1351	6.9295	4.4256	2.8320	1.4792
D	→	Y	↓	0.1550	0.1456	0.1255	0.1399	6.4246	4.1765	1.7872	0.9037

Cell Description

The NAND2 cell provides the logical NAND of two inputs (A,B). The output (Y) is represented by the logic equation:

$Y = \overline{(A \bullet B)}$

Logic Symbol

A — ⟩o— Y
B

Function Table

A	B	Y
0	x	1
x	0	1
1	1	0
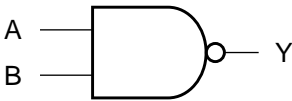
Cell Size

Drive Strength	Height (um)	Width (um)
NAND2XLADTH	2.52	1.12
NAND2X1ADTH	2.52	1.12
NAND2X2ADTH	2.52	1.12
NAND2X3ADTH	2.52	1.96
NAND2X4ADTH	2.52	1.96
NAND2X5ADTH	2.52	2.52
NAND2X6ADTH	2.52	2.52
NAND2X8ADTH	2.52	3.36

Functional Schematic

A ⟩
B ⟩ ⟩o— ⟩ Y

AC Power

Pin	Power (uW/MHz)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A	0.0014	0.0019	0.0030	0.0044	0.0054	0.0071	0.0082	0.0108
B	0.0016	0.0023	0.0039	0.0061	0.0077	0.0097	0.0112	0.0149

Pin Capacitance

Pin	Capacitance (pF)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A	0.0014	0.0018	0.0028	0.0043	0.0053	0.0071	0.0081	0.0105
B	0.0012	0.0016	0.0026	0.0045	0.0055	0.0067	0.0077	0.0105

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)							
			XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A	→ Y	↑	0.0182	0.0168	0.0170	0.0174	0.0164	0.0169	0.0165	0.0167
A	→ Y	↓	0.0229	0.0233	0.0172	0.0162	0.0154	0.0158	0.0160	0.0158
B	→ Y	↑	0.0191	0.0180	0.0195	0.0207	0.0198	0.0202	0.0196	0.0199
B	→ Y	↓	0.0235	0.0245	0.0192	0.0193	0.0185	0.0183	0.0184	0.0185

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)							
			XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A	→ Y	↑	6.8718	4.4578	2.8719	2.0041	1.4947	1.1926	0.9947	0.7688
A	→ Y	↓	9.2888	6.8622	2.9254	1.8192	1.3692	1.0843	0.9526	0.7082
B	→ Y	↑	6.8587	4.4558	2.8714	1.9469	1.4620	1.1926	0.9945	0.7522
B	→ Y	↓	9.2696	6.8535	2.9233	1.8190	1.3691	1.0839	0.9522	0.7081

Cell Description

The NAND2B cell provides the logical NAND of one inverted input (AN) and one non-inverted input (B). The output (Y) is represented by the logic equation:

$Y = \overline{(\overline{AN} \cdot B)}$

Logic Symbol
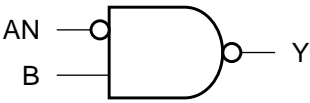
Function Table

AN	B	Y
1	x	1
x	0	1
0	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND2BXLADTH	2.52	1.40
NAND2BX1ADTH	2.52	1.40
NAND2BX2ADTH	2.52	1.40
NAND2BX4ADTH	2.52	2.24
NAND2BX8ADTH	2.52	3.92

Functional Schematic
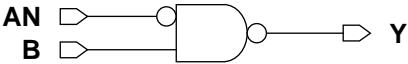
AC Power

Pin	Power (uW/MHz)				
	XL	**X1**	**X2**	**X4**	**X8**
AN	0.0025	0.0030	0.0043	0.0082	0.0156
B	0.0013	0.0018	0.0029	0.0060	0.0117

Pin Capacitance

Pin	Capacitance (pF)				
	XL	**X1**	**X2**	**X4**	**X8**
AN	0.0011	0.0011	0.0014	0.0024	0.0043
B	0.0013	0.0017	0.0026	0.0055	0.0105

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				
			XL	**X1**	**X2**	**X4**	**X8**
AN	→ Y	↑	0.0371	0.0377	0.0403	0.0393	0.0374
AN	→ Y	↓	0.0687	0.0734	0.0585	0.0556	0.0525
B	→ Y	↑	0.0186	0.0174	0.0189	0.0195	0.0197
B	→ Y	↓	0.0237	0.0248	0.0205	0.0203	0.0203

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)				
			XL	**X1**	**X2**	**X4**	**X8**
AN	→ Y	↑	6.9076	4.4780	2.8839	1.5045	0.7698
AN	→ Y	↓	9.3004	6.5640	2.8712	1.3712	0.6947
B	→ Y	↑	6.8714	4.4199	2.9043	1.4790	0.7589
B	→ Y	↓	9.2112	6.5265	2.8601	1.3664	0.6928

Cell Description

The NAND3 cell provides the logical NAND of three inputs (A,B,C). The output (Y) is represented by the logic equation:

$$Y = \overline{(A \bullet B \bullet C)}$$

Logic Symbol
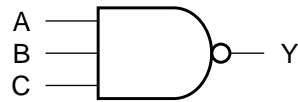
Function Table

A	B	C	Y
0	x	x	1
x	0	x	1
x	x	0	1
1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND3XLADTH	2.52	1.40
NAND3X1ADTH	2.52	1.40
NAND3X2ADTH	2.52	1.68
NAND3X3ADTH	2.52	2.52
NAND3X4ADTH	2.52	2.52
NAND3X6ADTH	2.52	3.64
NAND3X8ADTH	2.52	4.76

Functional Schematic
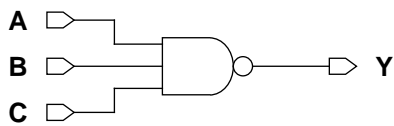
AC Power

Pin	Power (uW/MHz)						
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A	0.0016	0.0022	0.0034	0.0049	0.0060	0.0094	0.0124
B	0.0018	0.0026	0.0044	0.0066	0.0082	0.0124	0.0166
C	0.0022	0.0030	0.0053	0.0083	0.0104	0.0155	0.0209

Pin Capacitance

Pin	Capacitance (pF)						
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A	0.0014	0.0018	0.0028	0.0041	0.0051	0.0082	0.0106
B	0.0013	0.0017	0.0027	0.0045	0.0055	0.0079	0.0107
C	0.0012	0.0016	0.0025	0.0047	0.0056	0.0079	0.0111

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)						
			XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A	→ Y	↑	0.0212	0.0198	0.0198	0.0192	0.0185	0.0192	0.0191
A	→ Y	↓	0.0355	0.0355	0.0246	0.0225	0.0213	0.0224	0.0218
B	→ Y	↑	0.0232	0.0218	0.0234	0.0230	0.0222	0.0226	0.0227
B	→ Y	↓	0.0387	0.0394	0.0294	0.0280	0.0267	0.0271	0.0269
C	→ Y	↑	0.0244	0.0230	0.0254	0.0255	0.0245	0.0257	0.0260
C	→ Y	↓	0.0412	0.0419	0.0314	0.0309	0.0294	0.0300	0.0302

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)						
			XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A	→ Y	↑	6.9118	4.4832	2.8891	2.0048	1.5178	1.0050	0.7667
A	→ Y	↓	13.1845	9.3205	3.9760	2.5871	1.9441	1.2966	0.9647
B	→ Y	↑	7.0593	4.5779	2.9494	1.9898	1.5062	1.0124	0.7637
B	→ Y	↓	13.1678	9.3126	3.9736	2.5857	1.9434	1.2961	0.9644
C	→ Y	↑	6.8503	4.4558	2.9007	1.9390	1.4693	1.0113	0.7581
C	→ Y	↓	13.1686	9.3155	3.9724	2.5864	1.9434	1.2960	0.9647

Cell Description

The NAND3B cell provides the logical NAND of one inverted input (AN) and two non-inverted inputs (B,C). The output (Y) is represented by the logic equation:

$Y = \overline{(\overline{AN} \bullet B \bullet C)}$

Logic Symbol
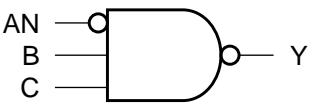
Function Table

AN	B	C	Y
1	x	x	1
x	0	x	1
x	x	0	1
0	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND3BXLADTH	2.52	1.68
NAND3BX1ADTH	2.52	1.68
NAND3BX2ADTH	2.52	1.96
NAND3BX4ADTH	2.52	3.08

Functional Schematic
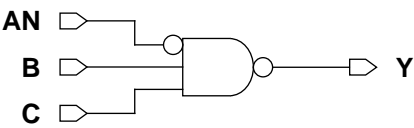
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
AN	0.0028	0.0035	0.0052	0.0089
B	0.0016	0.0021	0.0034	0.0068
C	0.0017	0.0024	0.0043	0.0089

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
AN	0.0011	0.0012	0.0014	0.0023
B	0.0013	0.0017	0.0026	0.0053
C	0.0013	0.0017	0.0025	0.0058

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
AN	→	Y	↑	0.0406	0.0422	0.0447	0.0414	6.8597	4.4443	2.8993	1.5250
AN	→	Y	↓	0.0821	0.0881	0.0680	0.0606	13.0920	9.3081	3.9629	1.9381
B	→	Y	↑	0.0225	0.0210	0.0227	0.0223	7.0127	4.5329	2.9633	1.5162
B	→	Y	↓	0.0386	0.0400	0.0308	0.0288	13.0380	9.2844	3.9557	1.9361
C	→	Y	↑	0.0241	0.0225	0.0255	0.0254	6.9057	4.4411	2.9319	1.4884
C	→	Y	↓	0.0417	0.0433	0.0335	0.0323	13.0298	9.2802	3.9546	1.9361

Cell Description

The NAND4 cell provides a logical NAND of four
inputs (A,B,C,D). The output (Y) is represented
by the logic equation:

$Y = \overline{(A \bullet B \bullet C \bullet D)}$

Logic Symbol
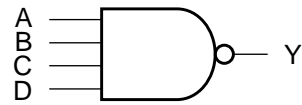
Function Table

A	B	C	D	Y
0	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
1	1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND4XLADTH	2.52	1.68
NAND4X1ADTH	2.52	1.68
NAND4X2ADTH	2.52	1.96
NAND4X4ADTH	2.52	3.36
NAND4X6ADTH	2.52	5.04
NAND4X8ADTH	2.52	6.72

Functional Schematic
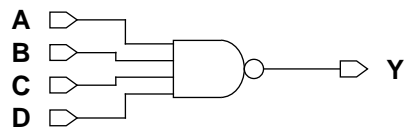
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0018	0.0025	0.0037	0.0069	0.0107	0.0142
B	0.0020	0.0029	0.0047	0.0092	0.0139	0.0185
C	0.0024	0.0033	0.0057	0.0111	0.0170	0.0226
D	0.0026	0.0037	0.0066	0.0134	0.0203	0.0271

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0014	0.0018	0.0028	0.0049	0.0085	0.0108
B	0.0012	0.0017	0.0026	0.0053	0.0082	0.0109
C	0.0013	0.0017	0.0026	0.0053	0.0082	0.0112
D	0.0012	0.0016	0.0025	0.0059	0.0086	0.0120

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	0.0227	0.0212	0.0218	0.0213	0.0220	0.0222
A	→ Y	↓	0.0483	0.0485	0.0326	0.0293	0.0304	0.0299
B	→ Y	↑	0.0252	0.0237	0.0255	0.0253	0.0258	0.0260
B	→ Y	↓	0.0536	0.0547	0.0394	0.0376	0.0376	0.0374
C	→ Y	↑	0.0275	0.0258	0.0286	0.0282	0.0293	0.0293
C	→ Y	↓	0.0590	0.0601	0.0445	0.0423	0.0429	0.0426
D	→ Y	↑	0.0275	0.0260	0.0300	0.0306	0.0326	0.0326
D	→ Y	↓	0.0604	0.0618	0.0468	0.0465	0.0469	0.0470

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)					
				XL	X1	X2	X4	X6	X8
A	→	Y	↑	6.7559	4.4004	2.9023	1.5405	1.0331	0.7913
A	→	Y	↓	17.0269	12.0564	5.1350	2.5080	1.6757	1.2490
B	→	Y	↑	7.0293	4.5696	2.9758	1.5230	1.0371	0.7837
B	→	Y	↓	17.0012	12.0474	5.1313	2.5075	1.6747	1.2486
C	→	Y	↑	7.0563	4.5832	2.9866	1.5142	1.0404	0.7823
C	→	Y	↓	17.0026	12.0505	5.1319	2.5077	1.6753	1.2487
D	→	Y	↑	6.8258	4.4359	2.9192	1.4747	1.0426	0.7783
D	→	Y	↓	17.0001	12.0459	5.1315	2.5082	1.6758	1.2495

Cell Description

The NAND4B cell provides a logical NAND of one inverted input (AN) and three non-inverted inputs (B,C,D). The output (Y) is represented by the logic equation:

$$Y = (\overline{\overline{AN}\bullet B\bullet C\bullet D})$$

Logic Symbol
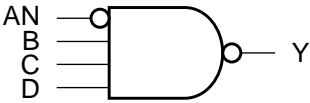
Function Table

AN	B	C	D	Y
1	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
0	1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND4BXLADTH	2.52	2.24
NAND4BX1ADTH	2.52	2.24
NAND4BX2ADTH	2.52	2.24
NAND4BX4ADTH	2.52	3.92

Functional Schematic
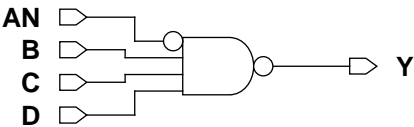
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
AN	0.0032	0.0039	0.0055	0.0101
B	0.0017	0.0023	0.0037	0.0076
C	0.0020	0.0027	0.0046	0.0094
D	0.0023	0.0032	0.0056	0.0118

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
AN	0.0011	0.0012	0.0014	0.0023
B	0.0013	0.0016	0.0026	0.0052
C	0.0013	0.0017	0.0026	0.0054
D	0.0013	0.0017	0.0026	0.0061

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
AN	→	Y	↑	0.0447	0.0462	0.0467	0.0443	6.9580	4.5158	2.9081	1.5583
AN	→	Y	↓	0.0987	0.1027	0.0755	0.0685	16.8495	11.9640	5.1319	2.5101
B	→	Y	↑	0.0259	0.0240	0.0246	0.0253	7.1592	4.6364	2.9827	1.5419
B	→	Y	↓	0.0556	0.0567	0.0403	0.0392	16.8004	11.9387	5.1262	2.5087
C	→	Y	↑	0.0283	0.0263	0.0281	0.0287	7.1985	4.6542	2.9947	1.5344
C	→	Y	↓	0.0608	0.0623	0.0458	0.0447	16.8014	11.9391	5.1270	2.5094
D	→	Y	↑	0.0291	0.0270	0.0299	0.0323	7.1194	4.5846	2.9549	1.5409
D	→	Y	↓	0.0622	0.0639	0.0480	0.0491	16.7990	11.9349	5.1260	2.5101

Cell Description

The NAND4BB cell provides a logical NAND of two inverted inputs (AN,BN) and two non-inverted inputs (C,D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} \bullet \overline{BN} \bullet C \bullet D)}$$

Logic Symbol
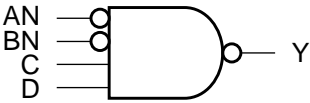
Function Table

AN	BN	C	D	Y
1	x	x	x	1
x	1	x	x	1
x	x	0	x	1
x	x	x	0	1
0	0	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND4BBXLADTH	2.52	2.80
NAND4BBX1ADTH	2.52	2.80
NAND4BBX2ADTH	2.52	2.80
NAND4BBX4ADTH	2.52	4.48

Functional Schematic
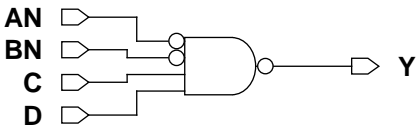
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
AN	0.0033	0.0041	0.0058	0.0106
BN	0.0032	0.0041	0.0061	0.0117
C	0.0017	0.0024	0.0039	0.0080
D	0.0019	0.0027	0.0048	0.0101

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
AN	0.0011	0.0011	0.0014	0.0023
BN	0.0010	0.0010	0.0013	0.0023
C	0.0012	0.0017	0.0026	0.0054
D	0.0013	0.0017	0.0026	0.0061

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
AN	→	Y	↑	0.0467	0.0487	0.0491	0.0458	6.9542	4.4992	2.9073	1.5566
AN	→	Y	↓	0.1016	0.1085	0.0778	0.0691	17.1190	12.1029	5.1469	2.5197
BN	→	Y	↑	0.0452	0.0472	0.0497	0.0489	7.1388	4.6163	2.9779	1.5409
BN	→	Y	↓	0.0994	0.1077	0.0818	0.0781	17.1039	12.1023	5.1517	2.5226
C	→	Y	↑	0.0274	0.0259	0.0278	0.0283	7.1643	4.6281	2.9840	1.5299
C	→	Y	↓	0.0609	0.0640	0.0475	0.0462	17.0538	12.0777	5.1438	2.5193
D	→	Y	↑	0.0283	0.0269	0.0298	0.0315	6.9923	4.5380	2.9300	1.5045
D	→	Y	↓	0.0637	0.0669	0.0504	0.0512	17.0608	12.0774	5.1435	2.5204

Cell Description

The NOR2 cell provides a logical NOR of two inputs (A,B). The output (Y) is represented by the logic equation:

$$Y = \overline{(A + B)}$$

Logic Symbol
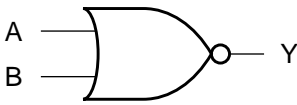
Function Table

A	B	Y
0	0	1
x	1	0
1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR2XLADTH	2.52	1.12
NOR2X1ADTH	2.52	1.12
NOR2X2ADTH	2.52	1.12
NOR2X3ADTH	2.52	1.96
NOR2X4ADTH	2.52	1.96
NOR2X5ADTH	2.52	2.52
NOR2X6ADTH	2.52	2.52
NOR2X8ADTH	2.52	3.36

Functional Schematic
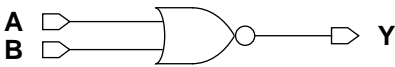
AC Power

Pin	Power (uW/MHz)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A	0.0014	0.0019	0.0031	0.0046	0.0060	0.0078	0.0090	0.0119
B	0.0018	0.0024	0.0039	0.0060	0.0078	0.0098	0.0115	0.0154

Pin Capacitance

Pin	Capacitance (pF)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A	0.0014	0.0018	0.0028	0.0040	0.0052	0.0070	0.0081	0.0105
B	0.0012	0.0016	0.0025	0.0043	0.0053	0.0067	0.0075	0.0106

Delays at 25°C, 1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A → Y ↑	0.0285	0.0253	0.0271	0.0258	0.0255	0.0274	0.0265	0.0262
A → Y ↓	0.0149	0.0145	0.0120	0.0112	0.0112	0.0116	0.0114	0.0112
B → Y ↑	0.0332	0.0302	0.0323	0.0333	0.0323	0.0337	0.0327	0.0332
B → Y ↓	0.0168	0.0168	0.0133	0.0132	0.0130	0.0131	0.0129	0.0130

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	XL	**X1**	**X2**	**X3**	**X4**	**X5**	**X6**	**X8**
A → Y ↑	13.9153	9.0765	5.8857	4.0348	3.0332	2.4888	2.0614	1.5580
A → Y ↓	5.2599	3.7025	1.5855	1.0211	0.7835	0.6268	0.5206	0.3889
B → Y ↑	13.8670	9.0585	5.8764	4.0329	3.0300	2.4858	2.0588	1.5568
B → Y ↓	5.2807	3.7165	1.5787	1.0377	0.7835	0.6283	0.5217	0.3908

Cell Description

The NOR2B cell provides a logical NOR of one inverted input (AN) and one non-inverted input (B). The output (Y) is represented by the logic equation:

$Y = \overline{(\overline{AN} + B)}$

Logic Symbol
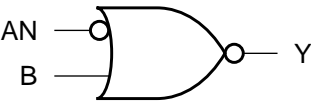
Function Table

AN	B	Y
1	0	1
x	1	0
0	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR2BXLADTH	2.52	1.40
NOR2BX1ADTH	2.52	1.40
NOR2BX2ADTH	2.52	1.68
NOR2BX4ADTH	2.52	2.24
NOR2BX8ADTH	2.52	4.20

Functional Schematic
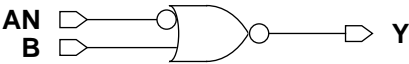
AC Power

Pin	Power (uW/MHz)				
	XL	**X1**	**X2**	**X4**	**X8**
AN	0.0021	0.0026	0.0041	0.0073	0.0144
B	0.0016	0.0023	0.0039	0.0078	0.0155

Pin Capacitance

Pin	Capacitance (pF)				
	XL	**X1**	**X2**	**X4**	**X8**
AN	0.0011	0.0011	0.0014	0.0024	0.0044
B	0.0012	0.0016	0.0026	0.0055	0.0105

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				
				XL	**X1**	**X2**	**X4**	**X8**
AN	→	Y	↑	0.0432	0.0449	0.0499	0.0472	0.0467
AN	→	Y	↓	0.0584	0.0652	0.0557	0.0515	0.0501
B	→	Y	↑	0.0328	0.0311	0.0343	0.0346	0.0351
B	→	Y	↓	0.0158	0.0162	0.0130	0.0129	0.0128

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)				
				XL	**X1**	**X2**	**X4**	**X8**
AN	→	Y	↑	14.0435	9.1425	5.9738	3.0581	1.5773
AN	→	Y	↓	5.4514	3.8099	1.6353	0.8055	0.3997
B	→	Y	↑	14.0210	9.1290	5.9649	3.0555	1.5757
B	→	Y	↓	5.1959	3.6746	1.5659	0.7781	0.3895

Cell Description

The NOR3 cell provides a logical NOR of three inputs (A,B,C). The output (Y) is represented by the logic equation:

$Y = \overline{(A + B + C)}$

Logic Symbol
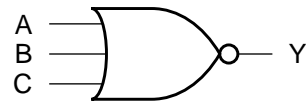
Function Table

A	B	C	Y
0	0	0	1
x	x	1	0
x	1	x	0
1	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR3XLADTH	2.52	1.40
NOR3X1ADTH	2.52	1.40
NOR3X2ADTH	2.52	1.68
NOR3X4ADTH	2.52	2.52
NOR3X6ADTH	2.52	3.92
NOR3X8ADTH	2.52	5.32

Functional Schematic
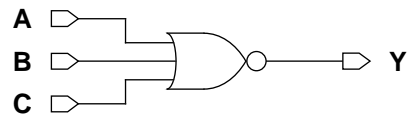
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0017	0.0023	0.0039	0.0075	0.0110	0.0147
B	0.0021	0.0028	0.0047	0.0092	0.0132	0.0178
C	0.0024	0.0033	0.0054	0.0109	0.0157	0.0212

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0013	0.0018	0.0028	0.0050	0.0084	0.0107
B	0.0012	0.0016	0.0026	0.0053	0.0078	0.0105
C	0.0012	0.0016	0.0025	0.0055	0.0077	0.0109

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	0.0454	0.0390	0.0430	0.0405	0.0420	0.0415
A	→ Y	↓	0.0165	0.0159	0.0130	0.0122	0.0125	0.0123
B	→ Y	↑	0.0586	0.0521	0.0567	0.0575	0.0564	0.0573
B	→ Y	↓	0.0186	0.0183	0.0145	0.0142	0.0140	0.0140
C	→ Y	↑	0.0649	0.0580	0.0620	0.0642	0.0631	0.0652
C	→ Y	↓	0.0199	0.0199	0.0151	0.0151	0.0148	0.0149

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	21.7610	14.0283	9.1478	4.7048	3.2068	2.4326
A	→ Y	↓	5.2475	3.6879	1.5723	0.7661	0.5211	0.3879
B	→ Y	↑	21.7001	14.0052	9.1376	4.7017	3.2023	2.4298
B	→ Y	↓	5.1936	3.6447	1.5580	0.7728	0.5206	0.3903
C	→ Y	↑	21.6983	14.0030	9.1342	4.7027	3.2027	2.4306
C	→ Y	↓	5.3620	3.7452	1.5880	0.7949	0.5341	0.3992

Cell Description

The NOR3B cell provides a logical NOR of one inverted input (AN) and two non-inverted inputs (B,C). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + B + C)}$$

Logic Symbol
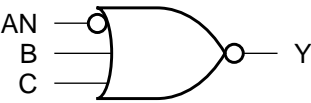
Function Table

AN	B	C	Y
1	0	0	1
x	x	1	0
x	1	x	0
0	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR3BXLADTH	2.52	1.68
NOR3BX1ADTH	2.52	1.68
NOR3BX2ADTH	2.52	1.96
NOR3BX4ADTH	2.52	3.08

Functional Schematic
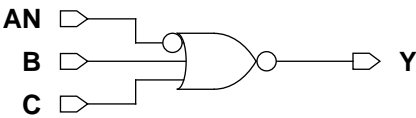
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
AN	0.0027	0.0031	0.0042	0.0077
B	0.0020	0.0027	0.0047	0.0092
C	0.0023	0.0032	0.0055	0.0109

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
AN	0.0011	0.0011	0.0014	0.0024
B	0.0012	0.0016	0.0025	0.0052
C	0.0012	0.0016	0.0025	0.0056

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
AN	→	Y	↑	0.0653	0.0613	0.0659	0.0634	21.7282	14.1232	9.2532	4.7808
AN	→	Y	↓	0.0666	0.0737	0.0572	0.0537	5.4394	3.8007	1.6208	0.7890
B	→	Y	↑	0.0573	0.0521	0.0592	0.0586	21.6544	14.0934	9.2403	4.7755
B	→	Y	↓	0.0178	0.0177	0.0145	0.0139	5.1615	3.6310	1.5560	0.7712
C	→	Y	↑	0.0633	0.0579	0.0650	0.0662	21.6484	14.0942	9.2383	4.7761
C	→	Y	↓	0.0188	0.0192	0.0151	0.0149	5.2541	3.7050	1.5747	0.7877

Cell Description

The NOR4 cell provides a logical NOR of four inputs (A,B,C,D). The output (Y) is represented by the logic equation:

$$Y = \overline{(A + B + C + D)}$$

Logic Symbol
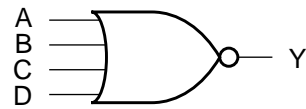
Function Table

A	B	C	D	Y
0	0	0	0	1
x	x	x	1	0
x	x	1	x	0
x	1	x	x	0
1	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR4XLADTH	2.52	1.68
NOR4X1ADTH	2.52	1.68
NOR4X2ADTH	2.52	2.80
NOR4X4ADTH	2.52	5.60
NOR4X6ADTH	2.52	8.68
NOR4X8ADTH	2.52	11.48

Functional Schematic
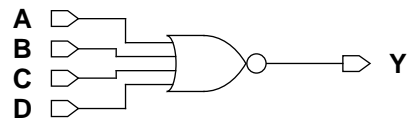
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0021	0.0026	0.0056	0.0117	0.0193	0.0264
B	0.0025	0.0031	0.0073	0.0149	0.0256	0.0353
C	0.0028	0.0036	0.0089	0.0182	0.0313	0.0431
D	0.0032	0.0042	0.0105	0.0212	0.0369	0.0509

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0014	0.0018	0.0039	0.0084	0.0131	0.0179
B	0.0014	0.0017	0.0042	0.0086	0.0125	0.0172
C	0.0013	0.0016	0.0045	0.0091	0.0124	0.0171
D	0.0013	0.0016	0.0046	0.0092	0.0123	0.0170

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	0.0581	0.0528	0.0336	0.0368	0.0337	0.0333
A	→ Y	↓	0.0184	0.0172	0.0160	0.0165	0.0171	0.0170
B	→ Y	↑	0.0829	0.0773	0.0586	0.0628	0.0630	0.0628
B	→ Y	↓	0.0212	0.0199	0.0200	0.0205	0.0221	0.0222
C	→ Y	↑	0.0958	0.0904	0.0744	0.0804	0.0795	0.0795
C	→ Y	↓	0.0223	0.0212	0.0223	0.0231	0.0244	0.0246
D	→ Y	↑	0.1015	0.0959	0.0813	0.0867	0.0859	0.0860
D	→ Y	↓	0.0229	0.0219	0.0232	0.0237	0.0247	0.0248

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)					
				XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→	Y	↑	26.7489	19.3063	6.4028	3.3254	1.9865	1.4438
A	→	Y	↓	5.2744	3.7099	1.5866	0.7865	0.5157	0.3764
B	→	Y	↑	26.7023	19.2830	6.3943	3.3209	1.9824	1.4411
B	→	Y	↓	5.1472	3.6241	1.5600	0.7788	0.5156	0.3774
C	→	Y	↑	26.6805	19.2761	6.3965	3.3233	1.9826	1.4410
C	→	Y	↓	5.2417	3.6719	1.5890	0.7941	0.5277	0.3867
D	→	Y	↑	26.6750	19.2737	6.3980	3.3232	1.9825	1.4410
D	→	Y	↓	5.5211	3.8386	1.6563	0.8277	0.5476	0.4009

Cell Description

The NOR4B cell provides a logical NOR of one inverted input (AN) and three non-inverted inputs (B,C,D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + B + C + D)}$$

Logic Symbol
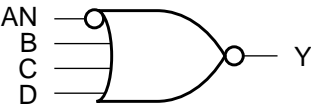
Function Table

AN	B	C	D	Y
1	0	0	0	1
x	x	x	1	0
x	x	1	x	0
x	1	x	x	0
0	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR4BXLADTH	2.52	2.24
NOR4BX1ADTH	2.52	2.24
NOR4BX2ADTH	2.52	3.36
NOR4BX4ADTH	2.52	3.36

Functional Schematic

TSMC CLN90G HVT
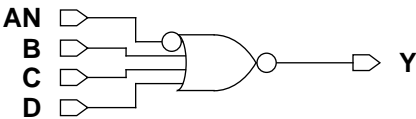
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
AN	0.0026	0.0030	0.0061	0.0077
B	0.0024	0.0030	0.0073	0.0089
C	0.0027	0.0035	0.0088	0.0103
D	0.0031	0.0040	0.0106	0.0121

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
AN	0.0011	0.0012	0.0021	0.0027
B	0.0013	0.0016	0.0040	0.0050
C	0.0013	0.0016	0.0043	0.0047
D	0.0013	0.0016	0.0048	0.0051

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
AN	→	Y	↑	0.0776	0.0733	0.0541	0.0659	27.0507	19.3741	6.4827	6.5009
AN	→	Y	↓	0.0696	0.0630	0.0558	0.0488	5.4347	3.7482	1.6103	0.9963
B	→	Y	↑	0.0802	0.0754	0.0602	0.0739	26.9730	19.3424	6.4750	6.4983
B	→	Y	↓	0.0202	0.0192	0.0198	0.0142	5.1486	3.6139	1.5598	0.8016
C	→	Y	↑	0.0956	0.0900	0.0753	0.0873	26.9668	19.3405	6.4756	6.4927
C	→	Y	↓	0.0217	0.0207	0.0221	0.0210	5.2254	3.6537	1.5878	1.2587
D	→	Y	↑	0.1011	0.0956	0.0842	0.0963	26.9598	19.3361	6.4795	6.4953
D	→	Y	↓	0.0215	0.0210	0.0235	0.0223	5.3377	3.7530	1.6553	1.2955

Cell Description

The NOR4BB cell provides a logical NOR of two inverted inputs (AN,BN) and two non-inverted inputs (C,D). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{AN} + \overline{BN} + C + D)}$$

Logic Symbol
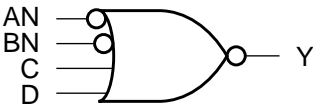
Function Table

AN	BN	C	D	Y
1	1	0	0	1
x	x	x	1	0
x	x	1	x	0
x	0	x	x	0
0	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR4BBXLADTH	2.52	2.80
NOR4BBX1ADTH	2.52	2.80
NOR4BBX2ADTH	2.52	3.92
NOR4BBX4ADTH	2.52	3.92

Functional Schematic
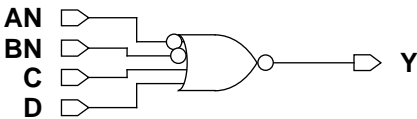
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
AN	0.0028	0.0033	0.0063	0.0073
BN	0.0029	0.0035	0.0076	0.0086
C	0.0027	0.0035	0.0090	0.0100
D	0.0031	0.0040	0.0108	0.0118

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
AN	0.0011	0.0012	0.0020	0.0022
BN	0.0011	0.0011	0.0020	0.0022
C	0.0013	0.0016	0.0043	0.0046
D	0.0013	0.0016	0.0048	0.0050

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
AN	→	Y	↑	0.0780	0.0766	0.0560	0.0745	26.5833	19.3177	6.4788	6.5351
AN	→	Y	↓	0.0757	0.0689	0.0562	0.0463	5.4721	3.7554	1.6065	1.0334
BN	→	Y	↑	0.0974	0.0967	0.0824	0.0892	26.4915	19.2767	6.4699	6.5209
BN	→	Y	↓	0.0718	0.0659	0.0650	0.0698	5.3211	3.6803	1.5850	1.4913
C	→	Y	↑	0.0935	0.0904	0.0782	0.0875	26.4864	19.2732	6.4682	6.5221
C	→	Y	↓	0.0216	0.0207	0.0224	0.0207	5.2683	3.6738	1.5873	1.2635
D	→	Y	↑	0.0990	0.0960	0.0872	0.0961	26.4748	19.2686	6.4739	6.5245
D	→	Y	↓	0.0221	0.0213	0.0240	0.0217	5.5067	3.8242	1.6540	1.2831

Cell Description

The OA21 cell provides the logical AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = (A0 + A1) \bullet B0$$

Logic Symbol
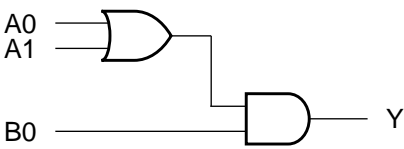
Function Table

A0	A1	B0	Y
x	x	0	0
0	0	x	0
x	1	1	1
1	x	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
OA21XLADTH	2.52	1.68
OA21X1ADTH	2.52	1.68
OA21X2ADTH	2.52	2.24
OA21X4ADTH	2.52	2.52

Functional Schematic
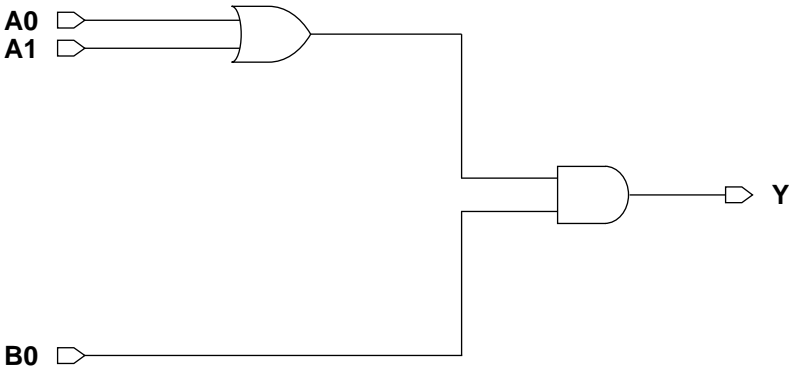
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0031	0.0036	0.0053	0.0095
A1	0.0033	0.0038	0.0057	0.0102
B0	0.0025	0.0030	0.0045	0.0081

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0010	0.0010	0.0015	0.0024
A1	0.0009	0.0009	0.0014	0.0023
B0	0.0011	0.0011	0.0016	0.0026

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→ Y	↑	0.0572	0.0610	0.0530	0.0520	6.8352	4.3742	2.8633	1.4775
A0	→ Y	↓	0.1387	0.1513	0.1227	0.1118	6.4235	4.3451	1.8559	0.9005
A1	→ Y	↑	0.0609	0.0650	0.0569	0.0563	6.8642	4.3898	2.8700	1.4809
A1	→ Y	↓	0.1440	0.1567	0.1287	0.1181	6.4240	4.3464	1.8559	0.9004
B0	→ Y	↑	0.0562	0.0603	0.0525	0.0516	6.8649	4.3902	2.8704	1.4810
B0	→ Y	↓	0.0706	0.0778	0.0646	0.0580	5.8562	4.0287	1.7344	0.8421

Cell Description

The OA22 cell provides the logical AND of two OR groups. The output (Y) is represented by the logic equation:

$Y = (A0 + A1) \bullet (B0 + B1)$

Logic Symbol
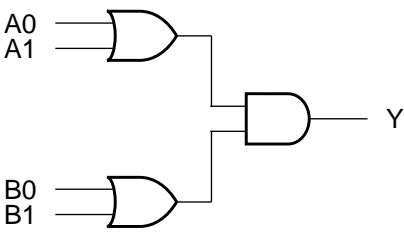
Function Table

A0	A1	B0	B1	Y
x	x	0	0	0
0	0	x	x	0
x	1	x	1	1
x	1	1	x	1
1	x	x	1	1
1	x	1	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
OA22XLADTH	2.52	2.24
OA22X1ADTH	2.52	2.24
OA22X2ADTH	2.52	2.52
OA22X4ADTH	2.52	3.08

Functional Schematic
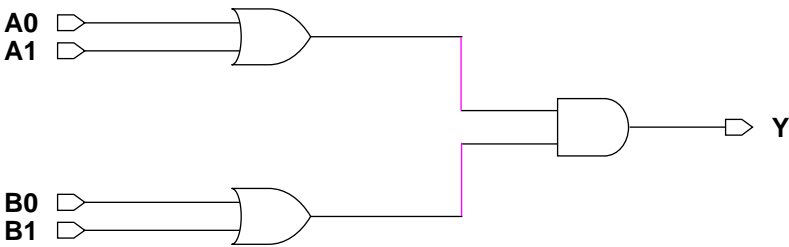
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0028	0.0033	0.0052	0.0092
A1	0.0030	0.0036	0.0057	0.0100
B0	0.0038	0.0043	0.0067	0.0118
B1	0.0040	0.0046	0.0072	0.0126

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0011	0.0012	0.0016	0.0027
A1	0.0010	0.0011	0.0016	0.0026
B0	0.0012	0.0012	0.0017	0.0027
B1	0.0010	0.0011	0.0017	0.0026

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0572	0.0638	0.0595	0.0579	6.9879	4.5070	2.9071	1.4980
A0	→	Y	↓	0.1244	0.1225	0.1034	0.0942	6.6816	4.3641	1.8879	0.9189
A1	→	Y	↑	0.0602	0.0678	0.0639	0.0623	7.0109	4.5215	2.9133	1.5015
A1	→	Y	↓	0.1299	0.1281	0.1096	0.1003	6.6813	4.3642	1.8878	0.9187
B0	→	Y	↑	0.0668	0.0738	0.0680	0.0656	6.9950	4.5132	2.9091	1.4989
B0	→	Y	↓	0.1657	0.1545	0.1301	0.1170	6.8352	4.4563	1.9326	0.9396
B1	→	Y	↑	0.0693	0.0767	0.0722	0.0700	7.0031	4.5181	2.9126	1.5012
B1	→	Y	↓	0.1711	0.1603	0.1378	0.1243	6.8330	4.4547	1.9325	0.9394

Cell Description

The OAI21 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet B0}$$

Logic Symbol

A0
A1

B0 ──────────────── Y
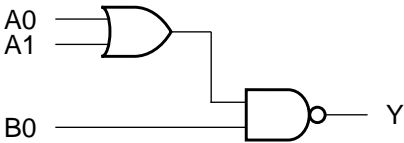
Function Table

A0	A1	B0	Y
0	0	x	1
x	x	0	1
x	1	1	0
1	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI21XLADTH	2.52	1.40
OAI21X1ADTH	2.52	1.40
OAI21X2ADTH	2.52	1.68
OAI21X3ADTH	2.52	2.52
OAI21X4ADTH	2.52	2.52
OAI21X6ADTH	2.52	3.64
OAI21X8ADTH	2.52	4.76

Functional Schematic

A0
A1

B0

Y
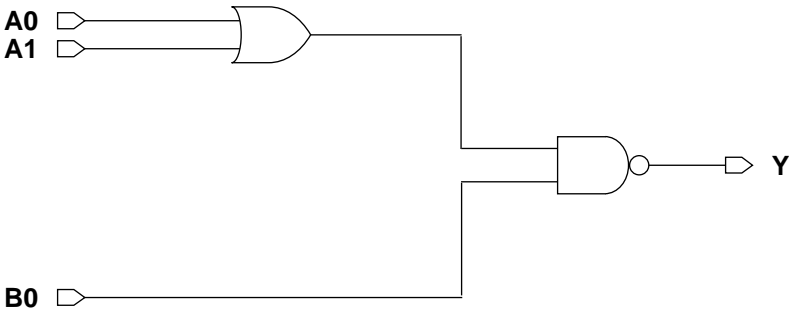
AC Power

Pin	Power (uW/MHz)						
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A0	0.0020	0.0026	0.0047	0.0072	0.0089	0.0136	0.0177
A1	0.0024	0.0032	0.0055	0.0085	0.0107	0.0160	0.0211
B0	0.0017	0.0023	0.0036	0.0054	0.0067	0.0105	0.0134

Pin Capacitance

Pin	Capacitance (pF)						
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A0	0.0012	0.0017	0.0027	0.0041	0.0050	0.0079	0.0102
A1	0.0011	0.0015	0.0025	0.0042	0.0052	0.0076	0.0102
B0	0.0013	0.0018	0.0028	0.0041	0.0051	0.0076	0.0100

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)						
			XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A0	→ Y	↑	0.0395	0.0353	0.0408	0.0423	0.0395	0.0415	0.0402
A0	→ Y	↓	0.0272	0.0269	0.0211	0.0213	0.0204	0.0210	0.0202
A1	→ Y	↑	0.0459	0.0413	0.0472	0.0493	0.0465	0.0481	0.0472
A1	→ Y	↓	0.0328	0.0329	0.0250	0.0249	0.0240	0.0242	0.0238
B0	→ Y	↑	0.0179	0.0168	0.0171	0.0172	0.0163	0.0170	0.0166
B0	→ Y	↓	0.0282	0.0287	0.0201	0.0196	0.0189	0.0195	0.0189

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)						
			XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**
A0	→ Y	↑	14.3280	9.2437	6.1201	4.1561	3.0984	2.1068	1.5867
A0	→ Y	↓	9.1667	6.4753	2.7444	1.8174	1.3740	0.9179	0.6841
A1	→ Y	↑	14.3096	9.2361	6.1163	4.1543	3.0968	2.1058	1.5860
A1	→ Y	↓	9.3298	6.5927	2.8008	1.8244	1.3769	0.9157	0.6859
B0	→ Y	↑	6.8853	4.4910	2.9353	1.9920	1.4819	1.0002	0.7589
B0	→ Y	↓	9.3592	6.6065	2.8044	1.8271	1.3786	0.9167	0.6868

Cell Description

The OAI211 cell provides the logical inverted
OR of one OR group and two additional inputs.
The output (Y) is represented by the logic
equation:

$$Y = \overline{(A0 + A1) \bullet B0 \bullet C0}$$

Logic Symbol
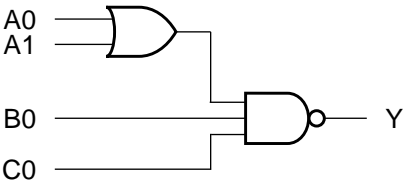
Function Table

A0	A1	B0	C0	Y
0	0	x	x	1
x	x	0	x	1
x	x	x	0	1
x	1	1	1	0
1	x	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI211XLADTH	2.52	1.68
OAI211X1ADTH	2.52	1.68
OAI211X2ADTH	2.52	1.96
OAI211X4ADTH	2.52	3.36

Functional Schematic

TSMC CLN90G HVT
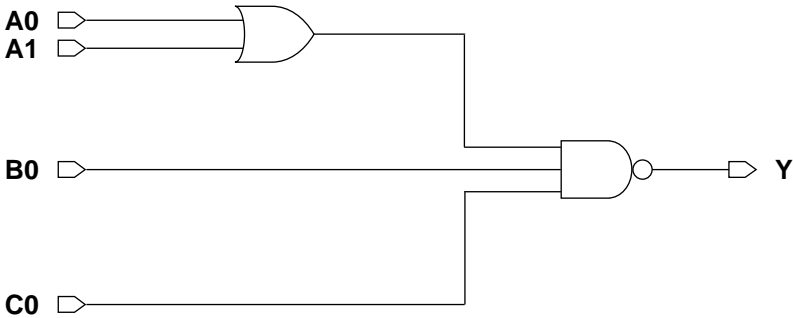
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0026	0.0035	0.0062	0.0120
A1	0.0029	0.0040	0.0070	0.0135
B0	0.0019	0.0027	0.0041	0.0078
C0	0.0022	0.0031	0.0051	0.0101

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0017	0.0027	0.0054
A1	0.0012	0.0015	0.0025	0.0048
B0	0.0015	0.0019	0.0028	0.0051
C0	0.0013	0.0017	0.0026	0.0055

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0513	0.0461	0.0535	0.0543	14.3630	9.3196	6.0842	3.1354
A0	→	Y	↓	0.0460	0.0455	0.0342	0.0337	13.3624	9.4600	3.9194	1.9529
A1	→	Y	↑	0.0570	0.0516	0.0596	0.0603	14.3566	9.3168	6.0824	3.1344
A1	→	Y	↓	0.0545	0.0546	0.0401	0.0389	13.5384	9.5885	3.9824	1.9629
B0	→	Y	↑	0.0217	0.0206	0.0201	0.0199	6.8764	4.6282	2.9014	1.5100
B0	→	Y	↓	0.0466	0.0469	0.0308	0.0291	13.5801	9.6080	3.9876	1.9651
C0	→	Y	↑	0.0234	0.0224	0.0237	0.0237	7.0524	4.7455	2.9796	1.4893
C0	→	Y	↓	0.0491	0.0501	0.0354	0.0350	13.5614	9.6007	3.9852	1.9647

Cell Description

The OAI21B cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet \overline{B0N}}$$

Logic Symbol
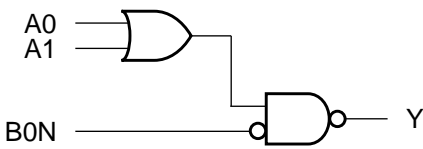
Function Table

A0	A1	B0N	Y
0	0	x	1
x	x	1	1
x	1	0	0
1	x	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI21BXLADTH	2.52	1.96
OAI21BX1ADTH	2.52	1.96
OAI21BX2ADTH	2.52	2.24
OAI21BX4ADTH	2.52	3.36

Functional Schematic
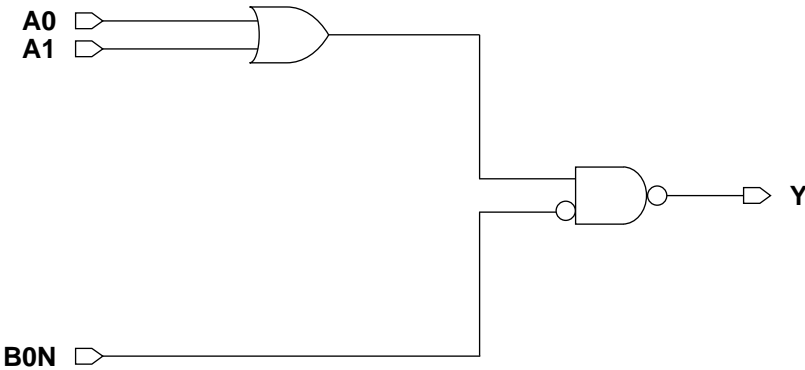
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0018	0.0024	0.0037	0.0070
A1	0.0022	0.0028	0.0045	0.0087
B0N	0.0027	0.0034	0.0049	0.0092

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0012	0.0017	0.0026	0.0050
A1	0.0011	0.0015	0.0025	0.0051
B0N	0.0012	0.0012	0.0014	0.0024

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→ Y	↑	0.0444	0.0382	0.0405	0.0396	14.5437	9.2997	6.0869	3.1051
A0	→ Y	↓	0.0321	0.0318	0.0242	0.0236	9.3594	6.5983	2.7749	1.3819
A1	→ Y	↑	0.0496	0.0433	0.0465	0.0466	14.5183	9.2883	6.0820	3.1038
A1	→ Y	↓	0.0377	0.0379	0.0282	0.0274	9.5175	6.7019	2.8270	1.3834
B0N	→ Y	↑	0.0394	0.0407	0.0415	0.0385	7.1027	4.5841	2.9394	1.5027
B0N	→ Y	↓	0.0773	0.0835	0.0629	0.0578	9.5676	6.7275	2.8338	1.3865

Cell Description

The OAI22 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet (B0 + B1)}$$

Logic Symbol
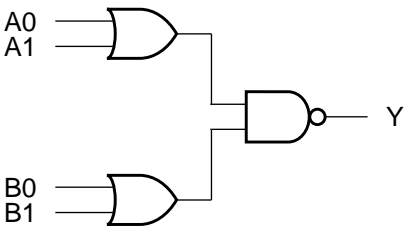
Function Table

A0	A1	B0	B1	Y
0	0	x	x	1
x	x	0	0	1
x	1	x	1	0
x	1	1	x	0
1	x	x	1	0
1	x	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI22XLADTH	2.52	1.68
OAI22X1ADTH	2.52	1.68
OAI22X2ADTH	2.52	1.96
OAI22X4ADTH	2.52	3.36

Functional Schematic
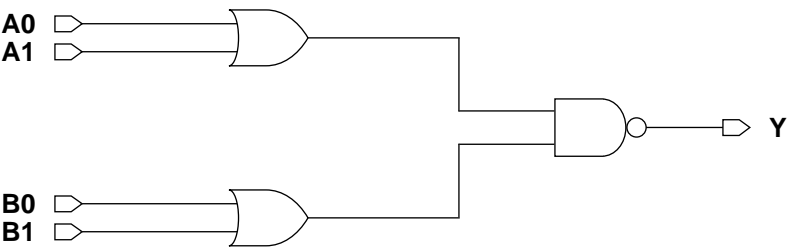
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0021	0.0028	0.0043	0.0083
A1	0.0025	0.0033	0.0051	0.0101
B0	0.0031	0.0040	0.0066	0.0129
B1	0.0035	0.0046	0.0074	0.0147

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0014	0.0018	0.0027	0.0051
A1	0.0013	0.0016	0.0025	0.0055
B0	0.0014	0.0018	0.0028	0.0051
B1	0.0012	0.0016	0.0026	0.0053

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0373	0.0319	0.0324	0.0325	14.3280	9.3095	6.1062	3.1308
A0	→	Y	↓	0.0315	0.0305	0.0214	0.0211	9.2335	6.5206	2.7825	1.3749
A1	→	Y	↑	0.0439	0.0381	0.0388	0.0403	14.3056	9.3000	6.1004	3.1293
A1	→	Y	↓	0.0379	0.0372	0.0253	0.0252	9.4276	6.6473	2.8172	1.3710
B0	→	Y	↑	0.0570	0.0478	0.0523	0.0519	14.3918	9.3770	6.1202	3.1252
B0	→	Y	↓	0.0426	0.0399	0.0288	0.0277	9.2903	6.5396	2.7867	1.3688
B1	→	Y	↑	0.0625	0.0537	0.0584	0.0591	14.3744	9.3700	6.1172	3.1233
B1	→	Y	↓	0.0482	0.0463	0.0327	0.0316	9.4248	6.6463	2.8164	1.3704

Cell Description

The OAI221 cell provides the logical inverted
AND of two OR groups and an additional input.
The output (Y) is represented by the logic
equation:

$$Y = \overline{(A0 + A1) \bullet (B0 + B1) \bullet C0}$$

Logic Symbol
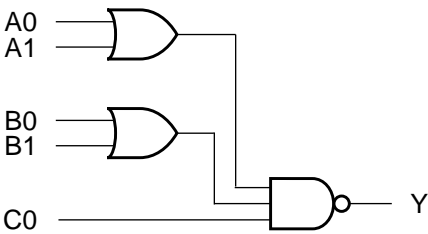
Function Table

A0	A1	B0	B1	C0	Y
0	0	x	x	x	1
x	x	0	0	x	1
x	x	x	x	0	1
x	1	x	1	1	0
x	1	1	x	1	0
1	x	x	1	1	0
1	x	1	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI221XLADTH	2.52	2.52
OAI221X1ADTH	2.52	2.52
OAI221X2ADTH	2.52	2.52
OAI221X4ADTH	2.52	4.48

Functional Schematic
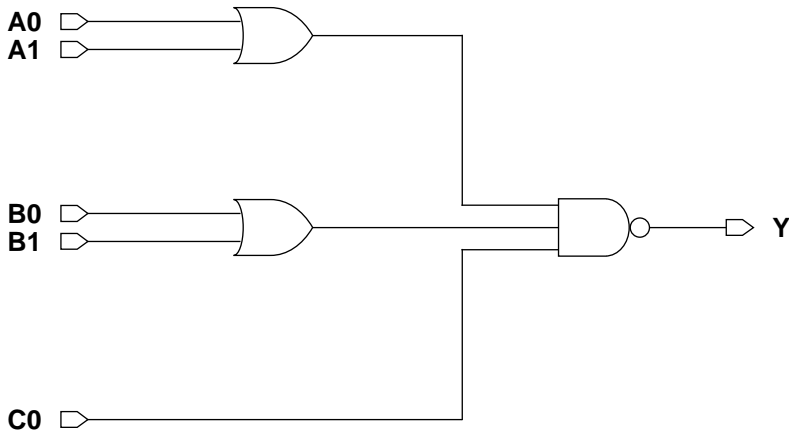
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0028	0.0037	0.0060	0.0117
A1	0.0032	0.0042	0.0068	0.0131
B0	0.0036	0.0047	0.0079	0.0158
B1	0.0040	0.0053	0.0087	0.0173
C0	0.0023	0.0032	0.0049	0.0095

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0016	0.0027	0.0055
A1	0.0012	0.0016	0.0026	0.0047
B0	0.0012	0.0016	0.0026	0.0054
B1	0.0011	0.0015	0.0025	0.0048
C0	0.0013	0.0017	0.0028	0.0051

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0559	0.0483	0.0512	0.0509	14.8975	9.6474	6.2633	3.2016
A0	→	Y	↓	0.0611	0.0594	0.0416	0.0399	13.4453	9.5112	4.0777	1.9977
A1	→	Y	↑	0.0627	0.0551	0.0579	0.0566	14.8888	9.6439	6.2610	3.1996
A1	→	Y	↓	0.0696	0.0686	0.0470	0.0450	13.3671	9.4535	4.0313	2.0067
B0	→	Y	↑	0.0670	0.0571	0.0638	0.0655	14.6639	9.4340	6.1322	3.1594
B0	→	Y	↓	0.0684	0.0657	0.0468	0.0461	13.3486	9.4325	4.0366	2.0103
B1	→	Y	↑	0.0726	0.0631	0.0699	0.0714	14.6603	9.4314	6.1305	3.1585
B1	→	Y	↓	0.0765	0.0749	0.0524	0.0514	13.3690	9.4544	4.0318	2.0066
C0	→	Y	↑	0.0234	0.0213	0.0212	0.0206	6.9119	4.5245	2.9135	1.4923
C0	→	Y	↓	0.0569	0.0574	0.0381	0.0365	13.3944	9.4668	4.0362	2.0086

Cell Description

The OAI222 cell provides the logical inverted AND of three OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet (B0 + B1) \bullet (C0 + C1)}$$

**Logic Symbol**
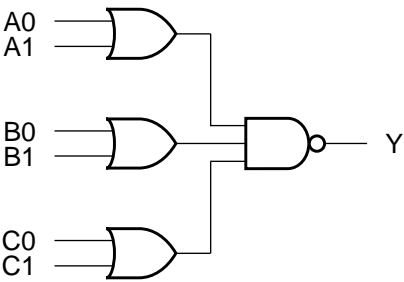
Function Table

A0	A1	B0	B1	C0	C1	Y
0	0	x	x	x	x	1
x	x	0	0	x	x	1
x	x	x	x	0	0	1
x	1	x	1	1	x	0
x	1	x	1	x	1	0
x	1	1	x	1	x	0
x	1	1	x	x	1	0
1	x	x	1	1	x	0
1	x	x	1	x	1	0
1	x	1	x	1	x	0
1	x	1	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI222XLADTH	2.52	2.80
OAI222X1ADTH	2.52	2.80
OAI222X2ADTH	2.52	3.08
OAI222X4ADTH	2.52	5.04

Functional Schematic
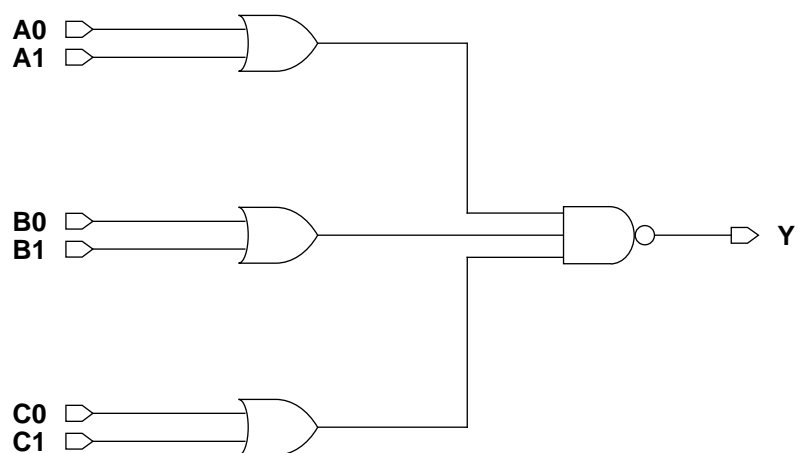
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0040	0.0050	0.0079	0.0154
A1	0.0043	0.0056	0.0088	0.0170
B0	0.0047	0.0060	0.0099	0.0197
B1	0.0051	0.0066	0.0107	0.0212
C0	0.0026	0.0036	0.0056	0.0110
C1	0.0030	0.0041	0.0063	0.0126

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0014	0.0018	0.0027	0.0054
A1	0.0013	0.0016	0.0026	0.0048
B0	0.0012	0.0016	0.0026	0.0054
B1	0.0012	0.0015	0.0025	0.0049
C0	0.0013	0.0017	0.0027	0.0057
C1	0.0013	0.0017	0.0026	0.0049

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0723	0.0599	0.0637	0.0623	14.9253	9.6815	6.3310	3.2150
A0	→	Y	↓	0.0822	0.0781	0.0530	0.0510	13.3987	9.4563	4.0368	2.0005
A1	→	Y	↑	0.0785	0.0660	0.0706	0.0688	14.9161	9.6773	6.3292	3.2136
A1	→	Y	↓	0.0895	0.0862	0.0583	0.0566	13.2685	9.3613	3.9846	2.0034
B0	→	Y	↑	0.0827	0.0686	0.0771	0.0789	14.5733	9.4301	6.1387	3.1693
B0	→	Y	↓	0.0882	0.0836	0.0584	0.0577	13.2927	9.3750	3.9936	2.0081
B1	→	Y	↑	0.0887	0.0746	0.0830	0.0848	14.5683	9.4277	6.1365	3.1684
B1	→	Y	↓	0.0966	0.0927	0.0638	0.0630	13.2681	9.3616	3.9845	2.0033
C0	→	Y	↑	0.0470	0.0410	0.0422	0.0424	14.6434	9.4418	6.1710	3.1644
C0	→	Y	↓	0.0588	0.0597	0.0404	0.0397	13.3464	9.4171	4.0453	2.0031
C1	→	Y	↑	0.0526	0.0469	0.0483	0.0481	14.6190	9.4321	6.1662	3.1614
C1	→	Y	↓	0.0660	0.0678	0.0451	0.0448	13.2720	9.3638	3.9852	2.0036

Cell Description

The OAI2B1 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + \overline{A1N}) \bullet B0}$$

Logic Symbol
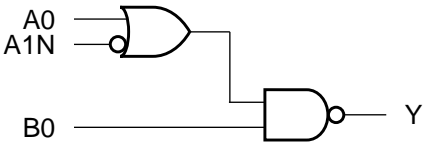
Function Table

A0	A1N	B0	Y
0	1	x	1
x	x	0	1
x	0	1	0
1	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI2B1XLADTH	2.52	1.96
OAI2B1X1ADTH	2.52	1.96
OAI2B1X2ADTH	2.52	2.24
OAI2B1X4ADTH	2.52	3.36

Functional Schematic
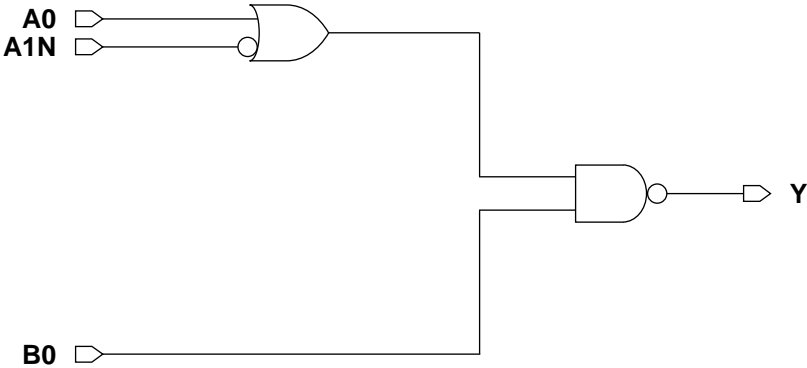
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0021	0.0028	0.0047	0.0090
A1N	0.0026	0.0033	0.0056	0.0109
B0	0.0017	0.0023	0.0035	0.0065

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0018	0.0027	0.0051
A1N	0.0011	0.0011	0.0014	0.0023
B0	0.0014	0.0018	0.0028	0.0051

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→ Y	↑	0.0412	0.0370	0.0406	0.0404	14.2475	9.3454	6.1078	3.1496
A0	→ Y	↓	0.0284	0.0279	0.0211	0.0206	9.1662	6.4683	2.7469	1.3780
A1N	→ Y	↑	0.0655	0.0638	0.0706	0.0710	14.2103	9.3297	6.1039	3.1488
A1N	→ Y	↓	0.0799	0.0859	0.0688	0.0667	9.3736	6.6148	2.8155	1.3881
B0	→ Y	↑	0.0184	0.0171	0.0170	0.0163	6.9064	4.4991	2.9405	1.4818
B0	→ Y	↓	0.0287	0.0292	0.0200	0.0189	9.3697	6.6098	2.8083	1.3837

Cell Description

The OAI2B11 cell provides the logical inverted OR of one OR group and two additional inputs. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + \overline{A1N}) \bullet B0 \bullet C0}$$

Logic Symbol
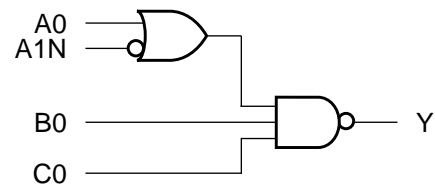
Function Table

A0	A1N	B0	C0	Y
0	1	x	x	1
x	x	0	x	1
x	x	x	0	1
x	0	1	1	0
1	x	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI2B11XLADTH	2.52	2.24
OAI2B11X1ADTH	2.52	2.24
OAI2B11X2ADTH	2.52	2.24
OAI2B11X4ADTH	2.52	3.92

Functional Schematic
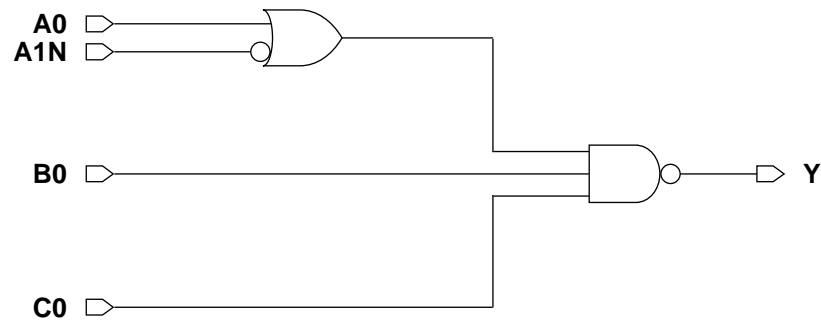
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0026	0.0034	0.0062	0.0121
A1N	0.0030	0.0040	0.0069	0.0138
B0	0.0017	0.0024	0.0040	0.0074
C0	0.0020	0.0029	0.0050	0.0097

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0017	0.0027	0.0055
A1N	0.0011	0.0011	0.0014	0.0022
B0	0.0013	0.0017	0.0028	0.0051
C0	0.0012	0.0016	0.0027	0.0055

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→ Y	↑		0.0523	0.0470	0.0539	0.0546	14.4406	9.4961	6.1490	3.1374
A0	→ Y	↓		0.0471	0.0461	0.0348	0.0339	13.4448	9.4961	4.0279	1.9538
A1N	→ Y	↑		0.0777	0.0749	0.0831	0.0839	14.4332	9.4912	6.1469	3.1368
A1N	→ Y	↓		0.1021	0.1060	0.0814	0.0776	13.6418	9.6252	4.1158	1.9659
B0	→ Y	↑		0.0209	0.0195	0.0203	0.0199	6.9510	4.5061	2.9032	1.5099
B0	→ Y	↓		0.0449	0.0457	0.0321	0.0292	13.6625	9.6309	4.1182	1.9658
C0	→ Y	↑		0.0237	0.0221	0.0239	0.0238	7.1596	4.6331	2.9811	1.4893
C0	→ Y	↓		0.0495	0.0506	0.0367	0.0352	13.6538	9.6285	4.1166	1.9657

Cell Description

The OAI2B2 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + \overline{A1N}) \bullet (B0 + B1)}$$

Logic Symbol
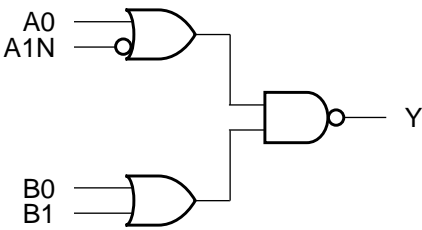
Function Table

A0	A1N	B0	B1	Y
0	1	x	x	1
x	x	0	0	1
x	0	x	1	0
x	0	1	x	0
1	x	x	1	0
1	x	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI2B2XLADTH	2.52	2.24
OAI2B2X1ADTH	2.52	2.24
OAI2B2X2ADTH	2.52	2.52
OAI2B2X4ADTH	2.52	3.92

Functional Schematic
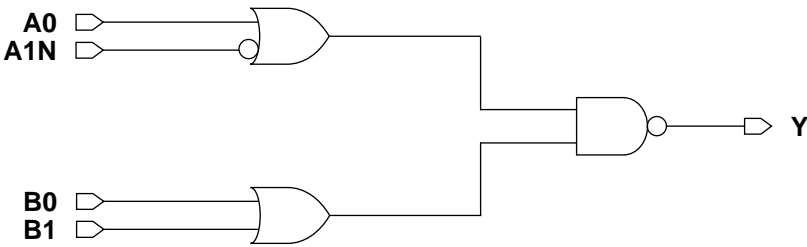
AC Power

Pin	Power (uW/MHz)			
	XL	X1	X2	X4
A0	0.0021	0.0026	0.0041	0.0081
A1N	0.0030	0.0037	0.0056	0.0109
B0	0.0028	0.0035	0.0058	0.0112
B1	0.0032	0.0040	0.0067	0.0129

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0	0.0015	0.0018	0.0028	0.0051
A1N	0.0011	0.0011	0.0015	0.0023
B0	0.0013	0.0016	0.0027	0.0051
B1	0.0012	0.0015	0.0025	0.0053

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	X1	X2	X4	XL	X1	X2	X4
A0	→	Y	↑	0.0382	0.0315	0.0322	0.0318	14.6489	9.4698	6.1377	3.1689
A0	→	Y	↓	0.0319	0.0302	0.0212	0.0207	9.3103	6.5474	2.7650	1.3813
A1N	→	Y	↑	0.0629	0.0597	0.0626	0.0625	14.6074	9.4577	6.1337	3.1675
A1N	→	Y	↓	0.0860	0.0907	0.0692	0.0658	9.5358	6.7006	2.8316	1.3807
B0	→	Y	↑	0.0560	0.0459	0.0512	0.0508	14.4613	9.3203	6.0756	3.1181
B0	→	Y	↓	0.0438	0.0418	0.0316	0.0305	9.3508	6.5782	2.7941	1.3816
B1	→	Y	↑	0.0619	0.0515	0.0576	0.0581	14.4456	9.3132	6.0715	3.1170
B1	→	Y	↓	0.0500	0.0484	0.0358	0.0346	9.5246	6.6947	2.8305	1.3803

Cell Description

The OAI2BB1 cell provides the logical inverted AND of one OR group of two inverted inputs (A0N,A1N) and an additional non-inverted input (B0). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} + \overline{A1N}) \bullet B0}$$

Logic Symbol
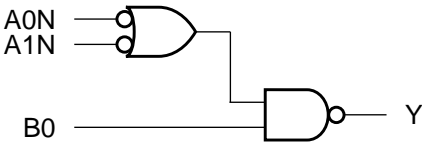
Function Table

A0N	A1N	B0	Y
1	1	x	1
x	x	0	1
x	0	1	0
0	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI2BB1XLADTH	2.52	1.68
OAI2BB1X1ADTH	2.52	1.68
OAI2BB1X2ADTH	2.52	1.96
OAI2BB1X4ADTH	2.52	2.52

Functional Schematic
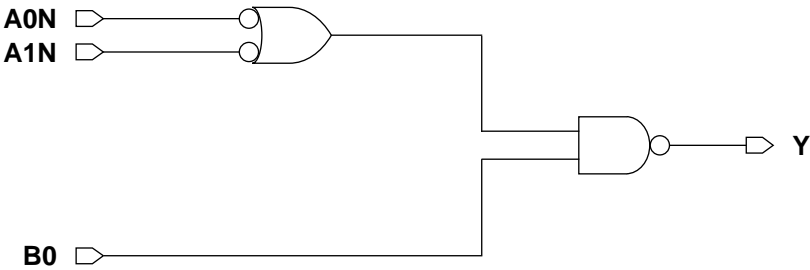
AC Power

Pin	Power (uW/MHz)			
	XL	X1	X2	X4
A0N	0.0030	0.0035	0.0053	0.0096
A1N	0.0027	0.0032	0.0048	0.0086
B0	0.0013	0.0018	0.0029	0.0060

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
A0N	0.0008	0.0009	0.0012	0.0020
A1N	0.0007	0.0007	0.0010	0.0016
B0	0.0010	0.0014	0.0022	0.0044

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	X1	X2	X4	XL	X1	X2	X4
A0N	→ Y	↑	0.0585	0.0606	0.0553	0.0530	7.0109	4.5446	2.9064	1.5286
A0N	→ Y	↓	0.0797	0.0854	0.0721	0.0639	9.6752	6.8327	2.8937	1.3678
A1N	→ Y	↑	0.0568	0.0588	0.0527	0.0504	7.0106	4.5439	2.9060	1.5288
A1N	→ Y	↓	0.0731	0.0784	0.0658	0.0578	9.6407	6.8151	2.8865	1.3638
B0	→ Y	↑	0.0187	0.0175	0.0191	0.0196	6.8567	4.4311	2.9147	1.4793
B0	→ Y	↓	0.0241	0.0252	0.0203	0.0200	9.5391	6.7734	2.8675	1.3574

Cell Description

The OAI2BB2 cell provides the logical inverted AND of one OR group of two inverted inputs (A0N,A1N) and one OR group of two non-inverted inputs (B0,B1). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{A0N} + \overline{A1N}) \bullet (B0 + B1)}$$

Logic Symbol
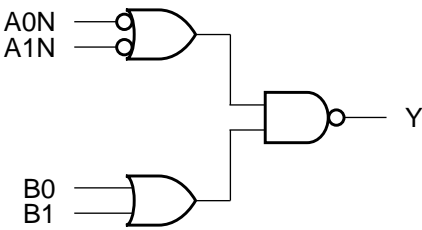
Function Table

A0N	A1N	B0	B1	Y
1	1	x	x	1
x	x	0	0	1
x	0	x	1	0
x	0	1	x	0
0	x	x	1	0
0	x	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI2BB2XLADTH	2.52	2.24
OAI2BB2X1ADTH	2.52	2.24
OAI2BB2X2ADTH	2.52	2.24
OAI2BB2X4ADTH	2.52	3.64

Functional Schematic

TSMC CLN90G HVT
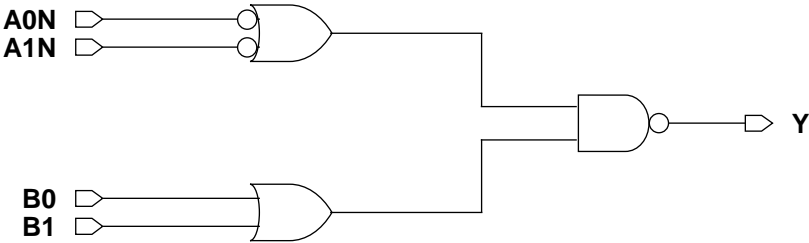
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0N	0.0033	0.0039	0.0060	0.0112
A1N	0.0030	0.0036	0.0056	0.0103
B0	0.0017	0.0022	0.0037	0.0069
B1	0.0020	0.0027	0.0044	0.0088

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0N	0.0010	0.0010	0.0014	0.0024
A1N	0.0011	0.0011	0.0016	0.0026
B0	0.0013	0.0017	0.0027	0.0051
B1	0.0012	0.0015	0.0025	0.0052

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0N	→	Y	↑	0.0588	0.0628	0.0583	0.0562	7.0149	4.5659	2.9383	1.4961
A0N	→	Y	↓	0.0830	0.0911	0.0750	0.0698	9.5125	6.6852	2.8549	1.3926
A1N	→	Y	↑	0.0571	0.0612	0.0563	0.0540	7.0149	4.5659	2.9379	1.4961
A1N	→	Y	↓	0.0814	0.0899	0.0731	0.0668	9.5068	6.6830	2.8529	1.3912
B0	→	Y	↑	0.0406	0.0361	0.0404	0.0404	14.4513	9.3467	6.1093	3.1611
B0	→	Y	↓	0.0288	0.0291	0.0237	0.0237	9.2665	6.5375	2.7703	1.3838
B1	→	Y	↑	0.0463	0.0417	0.0468	0.0474	14.4331	9.3391	6.1049	3.1595
B1	→	Y	↓	0.0349	0.0357	0.0283	0.0275	9.4322	6.6457	2.8404	1.3859

Cell Description

The OAI31 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1 + A2) \bullet B0}$$

Logic Symbol
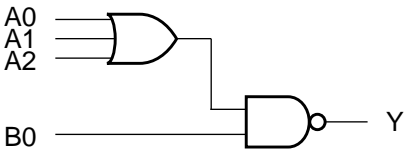
Function Table

A0	A1	A2	B0	Y
0	0	0	x	1
x	x	x	0	1
x	x	1	1	0
x	1	x	1	0
1	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI31XLADTH	2.52	1.68
OAI31X1ADTH	2.52	1.68
OAI31X2ADTH	2.52	1.96
OAI31X4ADTH	2.52	3.36

Functional Schematic
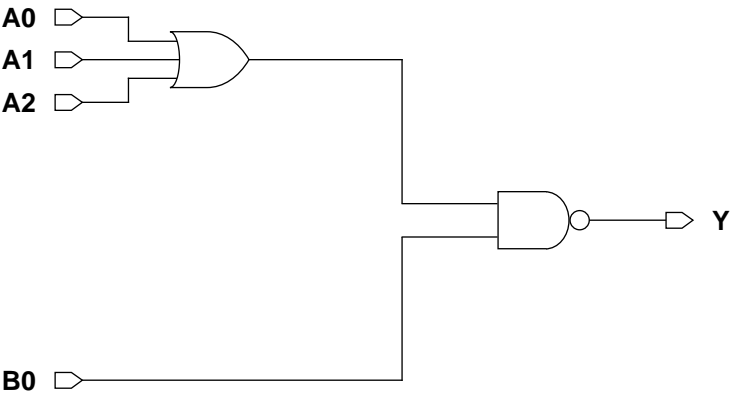
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0021	0.0028	0.0051	0.0101
A1	0.0024	0.0033	0.0059	0.0118
A2	0.0028	0.0039	0.0067	0.0134
B0	0.0020	0.0028	0.0044	0.0084

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0017	0.0027	0.0050
A1	0.0012	0.0015	0.0025	0.0052
A2	0.0011	0.0015	0.0025	0.0054
B0	0.0013	0.0017	0.0028	0.0052

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0589	0.0519	0.0614	0.0620	21.9439	14.2715	9.3237	4.7853
A0	→	Y	↓	0.0283	0.0277	0.0221	0.0220	9.1199	6.4330	2.7348	1.3786
A1	→	Y	↑	0.0736	0.0661	0.0757	0.0781	21.9195	14.2601	9.3173	4.7833
A1	→	Y	↓	0.0338	0.0338	0.0258	0.0258	9.2054	6.4969	2.7633	1.3721
A2	→	Y	↑	0.0791	0.0716	0.0813	0.0850	21.9162	14.2595	9.3169	4.7835
A2	→	Y	↓	0.0375	0.0381	0.0279	0.0278	9.4896	6.6700	2.8211	1.3895
B0	→	Y	↑	0.0178	0.0166	0.0169	0.0165	6.9482	4.5050	2.9029	1.4817
B0	→	Y	↓	0.0315	0.0327	0.0222	0.0211	9.5193	6.6862	2.8252	1.3912

Cell Description

The OAI32 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1 + A2) \bullet (B0 + B1)}$$

Logic Symbol
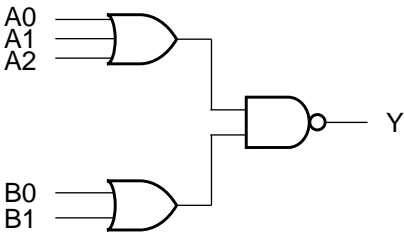
## Function Table

A0	A1	A2	B0	B1	Y
0	0	0	x	x	1
x	x	x	0	0	1
x	x	1	x	1	0
x	x	1	1	x	0
x	1	x	1	x	0
x	1	x	x	1	0
1	x	x	1	x	0
1	x	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI32XLADTH	2.52	1.96
OAI32X1ADTH	2.52	2.24
OAI32X2ADTH	2.52	2.24
OAI32X4ADTH	2.52	4.20

Functional Schematic
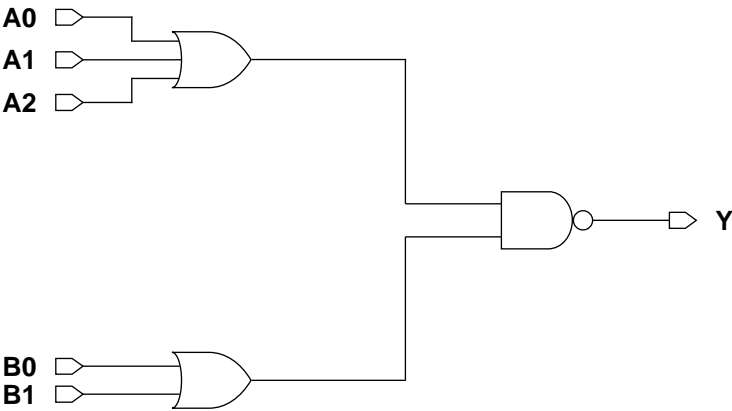
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0034	0.0041	0.0070	0.0140
A1	0.0036	0.0045	0.0078	0.0157
A2	0.0040	0.0051	0.0085	0.0173
B0	0.0023	0.0032	0.0049	0.0099
B1	0.0027	0.0038	0.0057	0.0117

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0017	0.0027	0.0050
A1	0.0011	0.0016	0.0025	0.0053
A2	0.0011	0.0015	0.0025	0.0054
B0	0.0013	0.0018	0.0027	0.0051
B1	0.0013	0.0016	0.0026	0.0053

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0843	0.0676	0.0788	0.0807	22.2394	14.3805	9.3760	4.8005
A0	→	Y	↓	0.0419	0.0391	0.0291	0.0292	9.2705	6.4681	2.7533	1.3779
A1	→	Y	↑	0.0996	0.0814	0.0932	0.0973	22.2173	14.3684	9.3698	4.7989
A1	→	Y	↓	0.0480	0.0452	0.0330	0.0333	9.3140	6.4970	2.7667	1.3703
A2	→	Y	↑	0.1056	0.0873	0.0990	0.1039	22.2152	14.3685	9.3704	4.7985
A2	→	Y	↓	0.0528	0.0500	0.0357	0.0355	9.5787	6.6227	2.8224	1.3827
B0	→	Y	↑	0.0344	0.0315	0.0316	0.0326	14.4408	9.3614	6.0871	3.1200
B0	→	Y	↓	0.0333	0.0346	0.0232	0.0234	9.3952	6.5393	2.7833	1.3941
B1	→	Y	↑	0.0428	0.0377	0.0380	0.0400	14.4349	9.3506	6.0815	3.1184
B1	→	Y	↓	0.0416	0.0416	0.0276	0.0275	9.5885	6.6250	2.8228	1.3829

Cell Description

The OAI33 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1 + A2) \bullet (B0 + B1 + B2)}$$

Logic Symbol
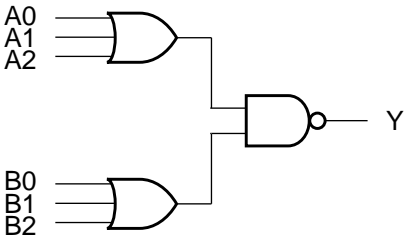
Function Table

A0	A1	A2	B0	B1	B2	Y
0	0	0	x	x	x	1
x	x	x	0	0	0	1
x	x	1	x	x	1	0
x	x	1	x	1	x	0
x	x	1	1	x	x	0
x	1	x	x	x	1	0
x	1	x	x	1	x	0
x	1	x	1	x	x	0
1	x	x	x	x	1	0
1	x	x	x	1	x	0
1	x	x	1	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI33XLADTH	2.52	2.52
OAI33X1ADTH	2.52	2.52
OAI33X2ADTH	2.52	2.52
OAI33X4ADTH	2.52	4.76

Functional Schematic
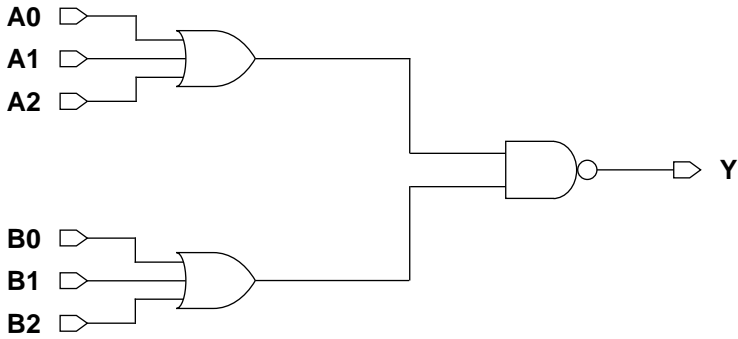
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A0	0.0027	0.0037	0.0057	0.0113
A1	0.0031	0.0043	0.0065	0.0130
A2	0.0035	0.0048	0.0074	0.0146
B0	0.0038	0.0051	0.0088	0.0175
B1	0.0042	0.0057	0.0097	0.0192
B2	0.0045	0.0062	0.0104	0.0208

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A0	0.0013	0.0017	0.0027	0.0051
A1	0.0012	0.0016	0.0026	0.0053
A2	0.0013	0.0017	0.0026	0.0056
B0	0.0012	0.0017	0.0026	0.0049
B1	0.0012	0.0016	0.0026	0.0052
B2	0.0011	0.0015	0.0025	0.0053

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A0	→	Y	↑	0.0576	0.0503	0.0508	0.0509	22.1831	14.5194	9.4172	4.8281
A0	→	Y	↓	0.0376	0.0379	0.0252	0.0247	9.2699	6.5568	2.7695	1.3792
A1	→	Y	↑	0.0736	0.0656	0.0661	0.0678	22.1573	14.5057	9.4097	4.8256
A1	→	Y	↓	0.0445	0.0450	0.0298	0.0294	9.3066	6.5716	2.7912	1.3821
A2	→	Y	↑	0.0820	0.0732	0.0731	0.0752	22.1682	14.5086	9.4113	4.8266
A2	→	Y	↓	0.0506	0.0511	0.0332	0.0325	9.5068	6.6833	2.8447	1.3933
B0	→	Y	↑	0.0936	0.0809	0.0956	0.0970	22.2362	14.4834	9.4035	4.8168
B0	→	Y	↓	0.0480	0.0473	0.0345	0.0345	9.2537	6.4776	2.7808	1.3957
B1	→	Y	↑	0.1089	0.0961	0.1108	0.1131	22.2166	14.4746	9.3991	4.8149
B1	→	Y	↓	0.0545	0.0550	0.0390	0.0387	9.2921	6.5805	2.7920	1.3859
B2	→	Y	↑	0.1155	0.1018	0.1167	0.1204	22.2165	14.4730	9.3988	4.8151
B2	→	Y	↓	0.0600	0.0603	0.0421	0.0413	9.5049	6.6840	2.8441	1.3933

Cell Description

The OR2 cell provides the logical OR of two inputs (A,B). The output (Y) is represented by the logic equation:

$Y = (A + B)$

Logic Symbol

A ———
B ——— Y
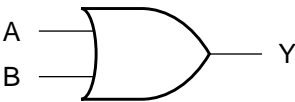
Function Table

A	B	Y
0	0	0
x	1	1
1	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
OR2XLADTH	2.52	1.40
OR2X1ADTH	2.52	1.40
OR2X2ADTH	2.52	1.40
OR2X4ADTH	2.52	2.52
OR2X6ADTH	2.52	2.80
OR2X8ADTH	2.52	3.64

Functional Schematic

A
B   Y
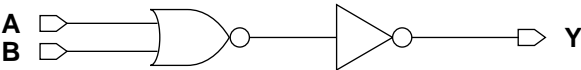
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0024	0.0029	0.0044	0.0081	0.0120	0.0163
B	0.0027	0.0033	0.0051	0.0094	0.0138	0.0187

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0011	0.0012	0.0017	0.0032	0.0043	0.0064
B	0.0011	0.0013	0.0018	0.0034	0.0046	0.0063

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)					
				XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→	Y	↑	0.0347	0.0383	0.0421	0.0390	0.0384	0.0392
A	→	Y	↓	0.0926	0.0818	0.0676	0.0629	0.0641	0.0638
B	→	Y	↑	0.0368	0.0414	0.0463	0.0436	0.0428	0.0434
B	→	Y	↓	0.1012	0.0897	0.0751	0.0707	0.0718	0.0709

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)					
				XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→	Y	↑	6.8600	4.4383	2.8716	1.4713	1.0001	0.7526
A	→	Y	↓	5.9146	3.9623	1.7058	0.8366	0.5579	0.4157
B	→	Y	↑	6.8710	4.4462	2.8760	1.4737	1.0015	0.7539
B	→	Y	↓	5.9133	3.9620	1.7055	0.8365	0.5578	0.4157

Cell Description

The OR3 cell provides the logical OR of three inputs (A,B,C). The output (Y) is represented by the logic equation:

$Y = (A + B + C)$

Logic Symbol

A
B —— Y
C
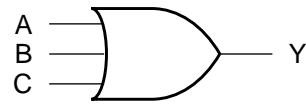
Function Table

A	B	C	Y
0	0	0	0
x	x	1	1
x	1	x	1
1	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
OR3XLADTH	2.52	1.68
OR3X1ADTH	2.52	1.68
OR3X2ADTH	2.52	1.68
OR3X4ADTH	2.52	2.80
OR3X6ADTH	2.52	4.20
OR3X8ADTH	2.52	5.60

Functional Schematic

A
B   Y
C
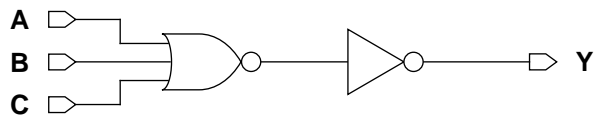
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0030	0.0036	0.0053	0.0097	0.0147	0.0192
B	0.0033	0.0041	0.0061	0.0113	0.0173	0.0223
C	0.0036	0.0045	0.0069	0.0130	0.0196	0.0257

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0013	0.0015	0.0021	0.0038	0.0060	0.0081
B	0.0013	0.0015	0.0021	0.0040	0.0062	0.0079
C	0.0012	0.0015	0.0021	0.0042	0.0060	0.0083

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	0.0395	0.0437	0.0474	0.0441	0.0445	0.0438
A	→ Y	↓	0.1097	0.0969	0.0797	0.0734	0.0753	0.0739
B	→ Y	↑	0.0423	0.0482	0.0539	0.0509	0.0511	0.0502
B	→ Y	↓	0.1248	0.1121	0.0948	0.0894	0.0923	0.0889
C	→ Y	↑	0.0442	0.0514	0.0585	0.0556	0.0556	0.0552
C	→ Y	↓	0.1312	0.1184	0.1009	0.0961	0.0987	0.0967

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	6.9369	4.4933	2.9096	1.4891	1.0049	0.7577
A	→ Y	↓	6.2937	4.1317	1.7843	0.8696	0.5848	0.4311
B	→ Y	↑	6.9572	4.5065	2.9178	1.4930	1.0075	0.7598
B	→ Y	↓	6.2925	4.1306	1.7838	0.8695	0.5847	0.4311
C	→ Y	↑	6.9932	4.5294	2.9297	1.4989	1.0119	0.7631
C	→ Y	↓	6.2934	4.1300	1.7837	0.8693	0.5847	0.4311

Cell Description

The OR4 cell provides the logical OR of four inputs (A,B,C,D). The output (Y) is represented by the logic equation:

$Y = (A + B + C + D)$

Logic Symbol
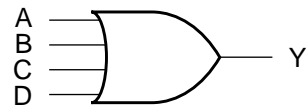
Function Table

A	B	C	D	Y
0	0	0	0	0
x	x	x	1	1
x	x	1	x	1
x	1	x	x	1
1	x	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
OR4XLADTH	2.52	2.24
OR4X1ADTH	2.52	2.24
OR4X2ADTH	2.52	2.24
OR4X4ADTH	2.52	3.64
OR4X6ADTH	2.52	5.32
OR4X8ADTH	2.52	7.00

Functional Schematic
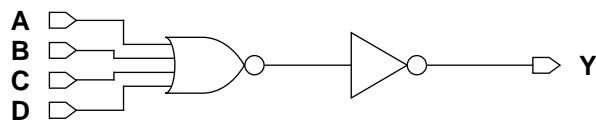
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0032	0.0038	0.0056	0.0101	0.0159	0.0203
B	0.0034	0.0041	0.0062	0.0116	0.0179	0.0230
C	0.0036	0.0045	0.0069	0.0128	0.0199	0.0257
D	0.0040	0.0049	0.0077	0.0145	0.0223	0.0289

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	0.0012	0.0014	0.0021	0.0035	0.0061	0.0077
B	0.0011	0.0013	0.0018	0.0037	0.0058	0.0075
C	0.0011	0.0013	0.0018	0.0039	0.0059	0.0079
D	0.0012	0.0013	0.0020	0.0043	0.0061	0.0091

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→ Y	↑	0.0401	0.0438	0.0482	0.0447	0.0458	0.0446
A	→ Y	↓	0.1631	0.1382	0.1093	0.1004	0.1049	0.1006
B	→ Y	↑	0.0419	0.0471	0.0533	0.0504	0.0516	0.0504
B	→ Y	↓	0.1864	0.1618	0.1327	0.1263	0.1302	0.1261
C	→ Y	↑	0.0435	0.0499	0.0577	0.0544	0.0560	0.0549
C	→ Y	↓	0.2030	0.1771	0.1476	0.1404	0.1456	0.1418
D	→ Y	↑	0.0445	0.0516	0.0605	0.0573	0.0590	0.0585
D	→ Y	↓	0.2136	0.1862	0.1555	0.1498	0.1548	0.1513

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)					
				XL	**X1**	**X2**	**X4**	**X6**	**X8**
A	→	Y	↑	6.9566	4.4959	2.9066	1.4838	1.0062	0.7560
A	→	Y	↓	7.2809	4.5382	1.9559	0.9534	0.6450	0.4739
B	→	Y	↑	6.9731	4.5070	2.9138	1.4871	1.0088	0.7579
B	→	Y	↓	7.2794	4.5375	1.9553	0.9533	0.6449	0.4740
C	→	Y	↑	7.0068	4.5279	2.9268	1.4936	1.0133	0.7613
C	→	Y	↓	7.2806	4.5372	1.9550	0.9534	0.6448	0.4740
D	→	Y	↑	7.0522	4.5591	2.9441	1.5023	1.0195	0.7662
D	→	Y	↓	7.2771	4.5377	1.9552	0.9534	0.6449	0.4740

Cell Description

The RF1R1W register file cell is an active-high D-type transparent latch with an active-high tristate output. The output (RB) is inverted.

Logic Symbol
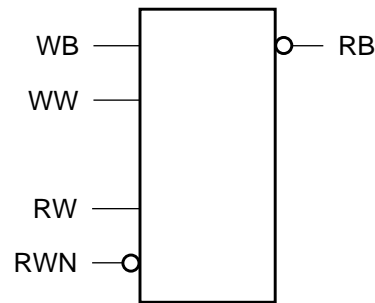
Cell Size

Drive Strength	Height (um)	Width (um)
RF1R1WX1ADTH	2.52	3.36

Function Table

WW	WB	q[n+1]
0	x	q[n]
1	0	0
1	1	1

- Functions for Write Operations

Function Table (Cont'd.)

RW	RWN	q	RB
0	0	0	1
0	0	1	Hi-Z
0	1	0	Hi-Z
0	1	1	Hi-Z
1	0	0	1
1	0	1	0
1	1	0	Hi-Z
1	1	1	0

- Functions for Read Operations
- Shaded areas represent operations that are legal only during RW/RWN transitions.

Functional Schematic
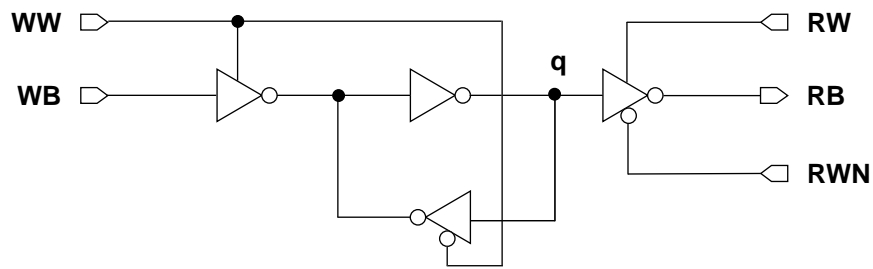
AC Power

Pin	Power (uW/MHz)
	X1
WW	0.0041
WB	0.0044
RW	0.0003
RB	0.0013

Pin Capacitance

Pin	Capacitance (pF)
	X1
WW	0.0023
WB	0.0011
RW	0.0007
RWN	0.0003
RB	0.2456

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)	K_{load} (ns/pF)
			X1	**X1**
WW	→ RB	↑	0.1682	16.2261
WW	→ RB	↓	0.0979	8.1496
WB	→ RB	↑	0.1463	16.2262
WB	→ RB	↓	0.1123	8.1500
RW	→ RB	↑	0.0209	16.2131
RW	→ RB	↓	0.0130	8.1275

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)
					X1
WW	minpwh				0.8332
WB	setup	↑	→	WW	0.0703
	setup	↓	→	WW	0.0664
	hold	↑	→	WW	-0.0586
	hold	↓	→	WW	-0.0586

Cell Description

The RF2R1W register file cell is an active-high D-type transparent latch with two independently controlled, active-high tri-state outputs. The cell has two read ports and one write port. The outputs (R1B,R2B) are inverted.

Logic Symbol
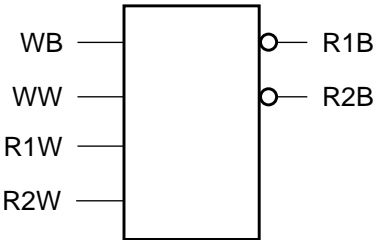
Cell Size

Drive Strength	Height (um)	Width (um)
RF2R1WX1ADTH	2.52	5.32

Function Table

WW	WB	q[n+1]
0	0	q[n]
0	1	q[n]
1	0	0
1	1	1

- Functions for Write Operations

Function Table (Cont'd.)

R1W/R2W	q	R1B/R2B
0	0	Hi-Z
0	1	Hi-Z
1	0	1
1	1	0

- Functions for Read Operations

Functional Schematic
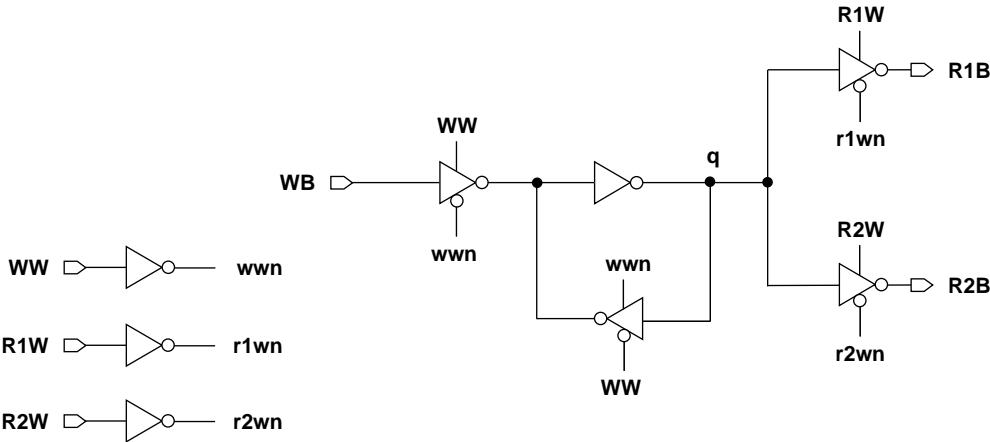
AC Power

Pin	Power (uW/MHz)
	X1
WB	0.0049
WW	0.0026
R1W	0.0014
R2W	0.0014
R1B	0.0073

Pin Capacitance

Pin	Capacitance (pF)
	X1
WB	0.0010
WW	0.0019
R1W	0.0014
R2W	0.0016
R1B	0.0010
R2B	0.0009

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)	K_{load} (ns/pF)
				X1	**X1**
WB	→	R1B	↑	0.1838	16.2035
WB	→	R1B	↓	0.1332	8.1518
WW	→	R1B	↑	0.2092	16.2047
WW	→	R1B	↓	0.1213	8.1514
R1W	→	R1B	↑	0.0443	16.1755
R1W	→	R1B	↓	0.0115	8.0960
WB	→	R2B	↑	0.1805	16.1054
WB	→	R2B	↓	0.1320	8.1994
WW	→	R2B	↑	0.2058	16.1054
WW	→	R2B	↓	0.1201	8.1995
R2W	→	R2B	↑	0.0420	16.0826
R2W	→	R2B	↓	0.0110	8.1398

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)
					X1
WB	setup	↑	→	WW	0.0742
	setup	↓	→	WW	0.0898
	hold	↑	→	WW	-0.0586
	hold	↓	→	WW	-0.0781
WW	minpwh				0.8332

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Cell Description

The SDFF cell is a positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE).

Logic Symbol
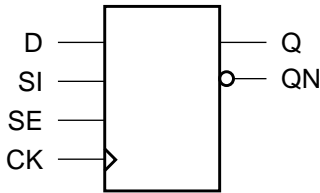
Function Table

D	SI	SE	CK	Q[n+1]	QN[n+1]
1	x	0	⌐	1	0
0	x	0	⌐	0	1
x	x	x	⌐	Q[n]	QN[n]
x	1	1	⌐	1	0
x	0	1	⌐	0	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFXLADTH	2.52	7.56
SDFFX1ADTH	2.52	7.56
SDFFX2ADTH	2.52	7.56
SDFFX4ADTH	2.52	9.52

Functional Schematic
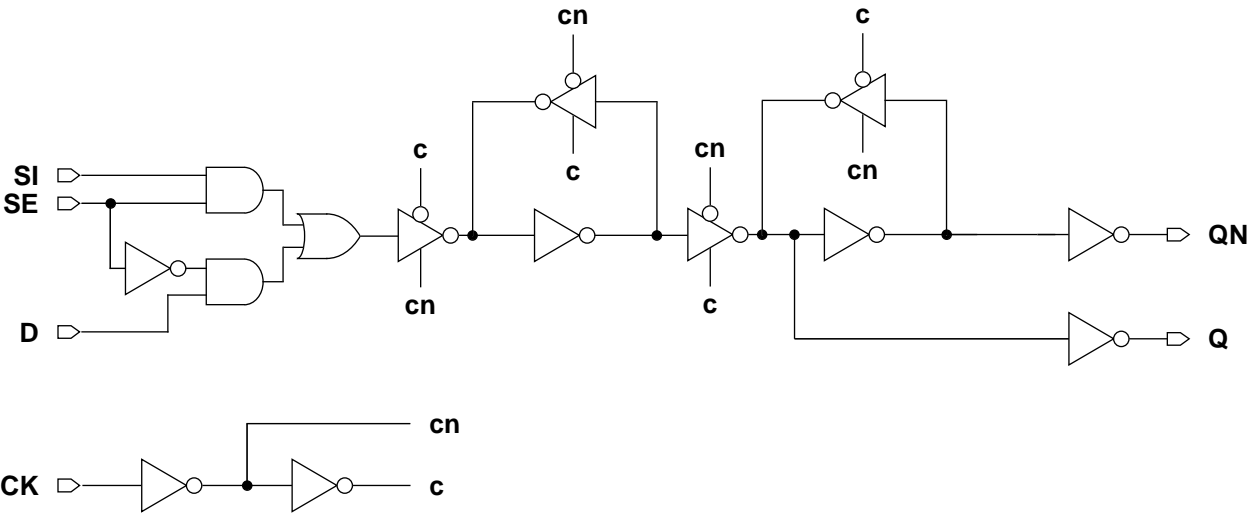
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
SI	0.0061	0.0062	0.0063	0.0072
SE	0.0077	0.0079	0.0079	0.0088
D	0.0054	0.0056	0.0057	0.0066
CK	0.0105	0.0106	0.0107	0.0123
Q	0.0049	0.0058	0.0075	0.0129

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
SI	0.0010	0.0010	0.0010	0.0010
SE	0.0030	0.0030	0.0029	0.0030
D	0.0013	0.0014	0.0014	0.0014
CK	0.0017	0.0017	0.0016	0.0018

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q ↑	0.1475	0.1434	0.1364	0.1322	7.2367	4.6172	2.9248	1.4910
CK	→	Q ↓	0.1718	0.1666	0.1396	0.1312	6.8536	4.3658	1.7997	0.8967
CK	→	QN ↑	0.2098	0.2039	0.1928	0.1896	7.0330	4.5326	2.9057	1.4827
CK	→	QN ↓	0.1979	0.2018	0.2035	0.1963	5.7350	3.9406	1.6969	0.8318

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
SI	setup	↑	→	CK	0.1094	0.1133	0.1133	0.1211
	setup	↓	→	CK	0.2695	0.2734	0.2812	0.3047
	hold	↑	→	CK	-0.0898	-0.0898	-0.0859	-0.0898
	hold	↓	→	CK	-0.2188	-0.2188	-0.2188	-0.2305
SE	setup	↑	→	CK	0.2734	0.2734	0.2773	0.3008
	setup	↓	→	CK	0.1289	0.1289	0.1250	0.1367
	hold	↑	→	CK	-0.0859	-0.0859	-0.0820	-0.0859
	hold	↓	→	CK	-0.0547	-0.0547	-0.0547	-0.0625
D	setup	↑	→	CK	0.0938	0.0977	0.0977	0.1055
	setup	↓	→	CK	0.1016	0.1055	0.1133	0.1289
	hold	↑	→	CK	-0.0742	-0.0781	-0.0742	-0.0781
	hold	↓	→	CK	-0.0508	-0.0547	-0.0547	-0.0625
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The SDFFH cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and fast clock-to-Q-path.

Logic Symbol

D — Q
SI —
SE —
CK —
QN
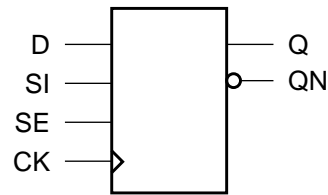
Function Table

D	SI	SE	CK	Q[n+1]	QN[n+1]
1	x	0	⌿	1	0
0	x	0	⌿	0	1
x	x	x	⌐	Q[n]	QN[n]
x	1	1	⌿	1	0
x	0	1	⌿	0	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFHX1ADTH	2.52	8.40
SDFFHX2ADTH	2.52	9.24
SDFFHX4ADTH	2.52	10.64
SDFFHX8ADTH	2.52	18.20

Functional Schematic
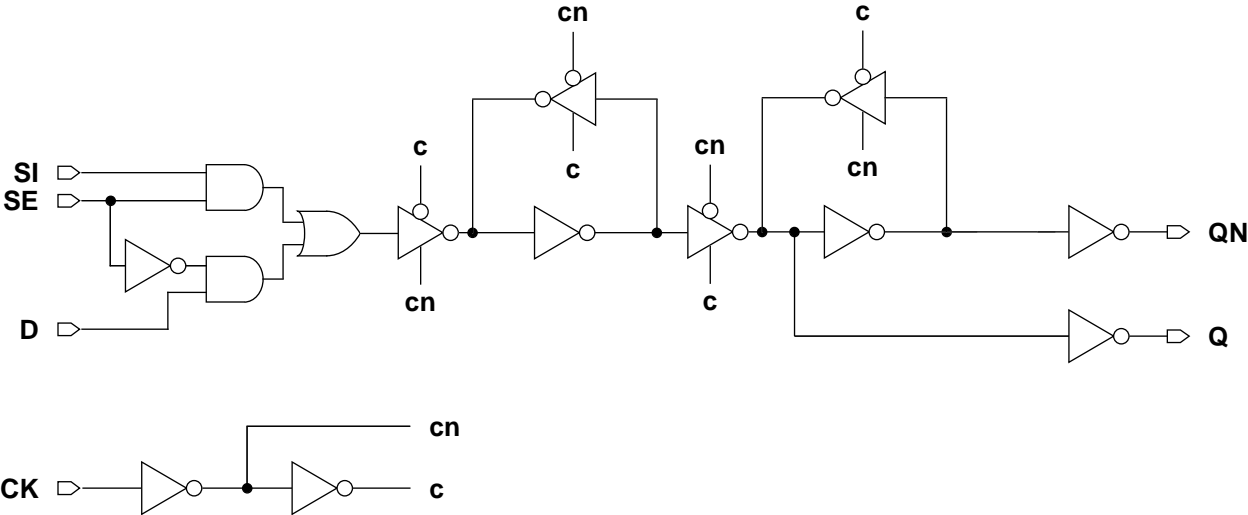
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
SI	0.0069	0.0088	0.0125	0.0233
SE	0.0100	0.0121	0.0154	0.0304
D	0.0078	0.0102	0.0144	0.0282
CK	0.0142	0.0174	0.0236	0.0441
Q	0.0052	0.0064	0.0086	0.0146

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
SI	0.0014	0.0014	0.0017	0.0026
SE	0.0032	0.0035	0.0033	0.0061
D	0.0012	0.0016	0.0020	0.0049
CK	0.0023	0.0022	0.0031	0.0053

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→	Q ↑	0.1084	0.1046	0.0910	0.0875	4.4571	2.9241	1.4776	0.7423
CK	→	Q ↓	0.1130	0.1100	0.1037	0.0937	4.0835	1.7664	0.8777	0.4121
CK	→	QN ↑	0.1538	0.1507	0.1481	0.1378	6.8070	6.7085	6.7267	6.6654
CK	→	QN ↓	0.1829	0.1779	0.1665	0.1675	5.4148	5.2673	5.2322	5.2199

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
SI	setup	↑	→	CK	0.1016	0.0977	0.0859	0.0859
	setup	↓	→	CK	0.1523	0.1602	0.1484	0.1406
	hold	↑	→	CK	-0.0430	-0.0430	-0.0352	-0.0352
	hold	↓	→	CK	-0.1055	-0.1094	-0.1016	-0.0898
SE	setup	↑	→	CK	0.1875	0.1992	0.1797	0.1953
	setup	↓	→	CK	0.1367	0.1172	0.1055	0.1289
	hold	↑	→	CK	-0.0391	-0.0430	-0.0352	-0.0352
	hold	↓	→	CK	-0.0781	-0.0508	-0.0586	-0.0391
D	setup	↑	→	CK	0.1094	0.0898	0.0820	0.0781
	setup	↓	→	CK	0.1367	0.1055	0.1094	0.0898
	hold	↑	→	CK	-0.0508	-0.0352	-0.0352	-0.0273
	hold	↓	→	CK	-0.0898	-0.0625	-0.0664	-0.0469
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The SDFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol

D — [ ] — Q
SI —
SE —
CK —▷
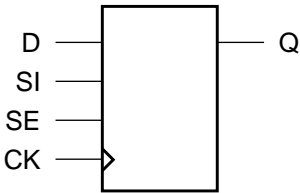
Function Table

D	SI	SE	CK	Q[n+1]
1	x	0	⌐	1
0	x	0	⌐	0
x	x	x	⌐	Q[n]
x	1	1	⌐	1
x	0	1	⌐	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFHQX1ADTH	2.52	8.12
SDFFHQX2ADTH	2.52	8.96
SDFFHQX4ADTH	2.52	10.08
SDFFHQX8ADTH	2.52	10.92

Functional Schematic
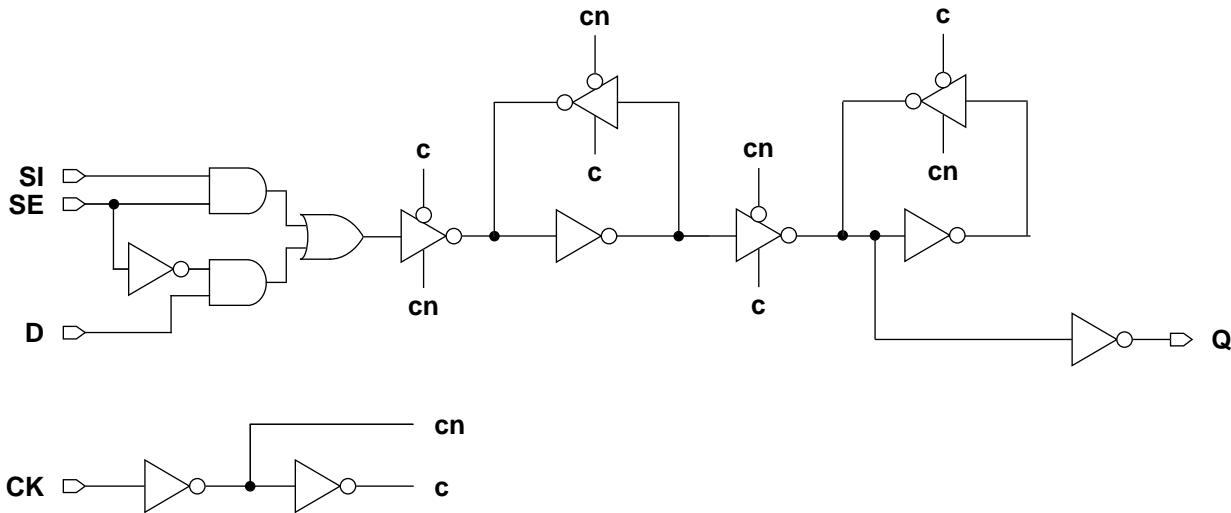
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
SI	0.0066	0.0085	0.0125	0.0125
SE	0.0096	0.0118	0.0152	0.0150
D	0.0078	0.0104	0.0143	0.0133
CK	0.0137	0.0169	0.0234	0.0223
Q	0.0035	0.0048	0.0074	0.0120

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
SI	0.0014	0.0014	0.0017	0.0014
SE	0.0031	0.0034	0.0033	0.0036
D	0.0016	0.0022	0.0020	0.0020
CK	0.0023	0.0022	0.0031	0.0031

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→ Q	↑	0.1123	0.1053	0.0913	0.1020	4.4796	2.9275	1.4813	0.7543
CK	→ Q	↓	0.1133	0.1107	0.1043	0.1122	4.0620	1.7640	0.8825	0.4292

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
SI	setup	↑	→	CK	0.1016	0.0977	0.0859	0.1094
	setup	↓	→	CK	0.1523	0.1562	0.1445	0.1914
	hold	↑	→	CK	-0.0391	-0.0430	-0.0352	-0.0469
	hold	↓	→	CK	-0.1055	-0.1094	-0.0977	-0.1328
SE	setup	↑	→	CK	0.1914	0.1953	0.1797	0.2148
	setup	↓	→	CK	0.1445	0.1211	0.1094	0.1250
	hold	↑	→	CK	-0.0391	-0.0430	-0.0352	-0.0391
	hold	↓	→	CK	-0.0703	-0.0391	-0.0547	-0.0469
D	setup	↑	→	CK	0.1211	0.0938	0.0820	0.0898
	setup	↓	→	CK	0.1172	0.0859	0.1055	0.1055
	hold	↑	→	CK	-0.0547	-0.0430	-0.0352	-0.0312
	hold	↓	→	CK	-0.0703	-0.0430	-0.0625	-0.0586
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The SDFFNH cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and fast clock-to-Q-path.

Logic Symbol

D — Q
SI —
SE —
CKN —○ QN
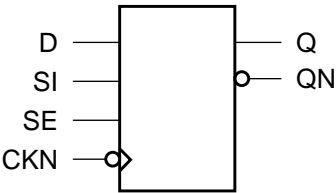
Function Table

D	SI	SE	CKN	Q[n+1]	QN[n+1]
1	x	0	⤵	1	0
0	x	0	⤵	0	1
x	x	x	⤴	Q[n]	QN[n]
x	1	1	⤵	1	0
x	0	1	⤵	0	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFNHX1ADTH	2.52	8.12
SDFFNHX2ADTH	2.52	8.40
SDFFNHX4ADTH	2.52	11.20
SDFFNHX8ADTH	2.52	15.12

Functional Schematic
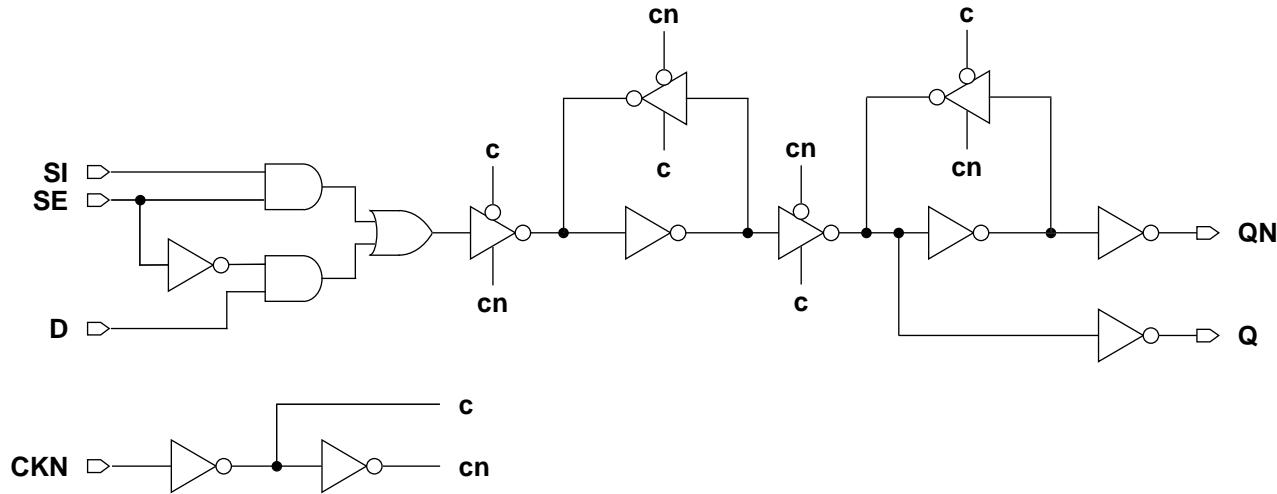
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
SI	0.0065	0.0079	0.0120	0.0182
SE	0.0091	0.0104	0.0150	0.0226
D	0.0075	0.0091	0.0141	0.0225
CKN	0.0111	0.0130	0.0189	0.0294
Q	0.0058	0.0065	0.0094	0.0157

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
SI	0.0013	0.0013	0.0017	0.0021
SE	0.0027	0.0027	0.0031	0.0037
D	0.0014	0.0017	0.0023	0.0045
CKN	0.0021	0.0022	0.0027	0.0041

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CKN	→	Q	↑	0.2129	0.2049	0.1999	0.1872	4.4836	2.8591	1.4570	0.7437
CKN	→	Q	↓	0.1774	0.1579	0.1492	0.1331	4.1473	1.7459	0.8433	0.4151
CKN	→	QN	↑	0.2190	0.1968	0.1936	0.1779	6.7762	6.6892	6.7151	6.7126
CKN	→	QN	↓	0.2700	0.2569	0.2675	0.2486	5.3037	5.3239	5.2293	5.2156

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	X2	X4	X8
SI	setup	↑	→	CKN	0.0000	-0.0039	-0.0078	0.0117
	setup	↓	→	CKN	0.0898	0.1016	0.0938	0.0898
	hold	↑	→	CKN	0.0469	0.0430	0.0391	0.0234
	hold	↓	→	CKN	-0.0547	-0.0664	-0.0586	-0.0508
SE	setup	↑	→	CKN	0.1211	0.1328	0.1250	0.1289
	setup	↓	→	CKN	0.0664	0.0625	0.0664	0.0625
	hold	↑	→	CKN	0.0508	0.0469	0.0391	0.0234
	hold	↓	→	CKN	0.0195	0.0156	0.0078	-0.0117
D	setup	↑	→	CKN	0.0078	-0.0039	-0.0078	0.0117
	setup	↓	→	CKN	0.0742	0.0625	0.0664	0.0703
	hold	↑	→	CKN	0.0352	0.0352	0.0352	0.0234
	hold	↓	→	CKN	-0.0391	-0.0312	-0.0352	-0.0352
CKN	minpwl				0.8332	0.8332	0.8332	0.8332
	minpwh				0.8332	0.8332	0.8332	0.8332

Cell Description

The SDFFNSRH cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN). Set (SN) dominates reset (RN). This cell has a fast clock-to-Q path.

Logic Symbol
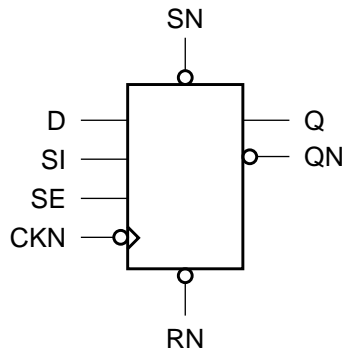
Function Table

RN	SN	D	SI	SE	CKN	Q[n+1]	QN[n+1]
1	1	1	x	0	⤵	1	0
1	1	0	x	0	⤵	0	1
1	1	x	x	x	⤴	Q[n]	QN[n]
1	1	x	1	1	⤵	1	0
1	1	x	0	1	⤵	0	1
0	1	x	x	x	x	0	1
1	0	x	x	x	x	1	0
0	0	x	x	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFNSRHX1ADTH	2.52	11.76
SDFFNSRHX2ADTH	2.52	11.76
SDFFNSRHX4ADTH	2.52	14.84
SDFFNSRHX8ADTH	2.52	15.68

Functional Schematic
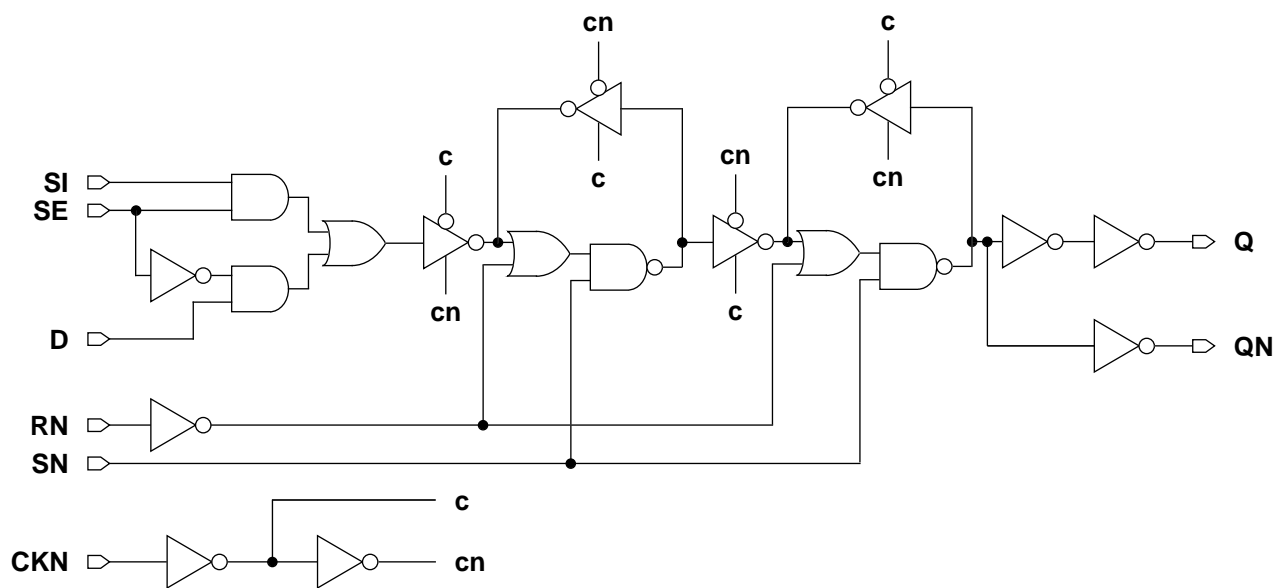
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
SI	0.0082	0.0095	0.0148	0.0162
SE	0.0095	0.0108	0.0161	0.0178
D	0.0090	0.0106	0.0165	0.0178
CKN	0.0119	0.0139	0.0211	0.0229
SN	0.0039	0.0041	0.0051	0.0057
RN	0.0011	0.0013	0.0022	0.0023
Q	0.0068	0.0082	0.0119	0.0169

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
SI	0.0012	0.0012	0.0015	0.0018
SE	0.0026	0.0026	0.0029	0.0032
D	0.0013	0.0017	0.0024	0.0024
CKN	0.0021	0.0023	0.0028	0.0039
SN	0.0022	0.0025	0.0034	0.0039
RN	0.0021	0.0024	0.0037	0.0038

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CKN	→	Q	↑	0.2391	0.2298	0.2342	0.2191	4.6576	3.0028	1.4876	0.7658
CKN	→	Q	↓	0.1910	0.1651	0.1603	0.1614	4.2719	1.8192	0.8803	0.4511
SN	→	Q	↑	0.1461	0.1712	0.2089	0.1765	4.5128	2.9909	1.4942	0.7614
SN	→	Q	↓	0.2722	0.2554	0.2381	0.2544	4.9826	2.2171	1.0830	0.5500
RN	→	Q	↓	0.2366	0.2139	0.1903	0.2175	5.0346	2.2187	1.0838	0.5503
CKN	→	QN	↑	0.2350	0.2119	0.2085	0.2163	6.6951	6.6954	6.7035	6.7026
CKN	→	QN	↓	0.3070	0.2967	0.3038	0.2960	5.5689	5.4778	5.3684	5.3606
SN	→	QN	↑	0.3268	0.3109	0.2959	0.3230	6.7407	6.7110	6.7076	6.7050
SN	→	QN	↓	0.2104	0.2370	0.2788	0.2554	5.5482	5.4695	5.3671	5.3597
RN	→	QN	↑	0.2923	0.2695	0.2481	0.2871	6.7425	6.7094	6.7062	6.7042

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
SI	setup	↑	→	CKN	0.0234	0.0156	0.0078	0.0039
	setup	↓	→	CKN	0.1094	0.1172	0.1211	0.1523
	hold	↑	→	CKN	0.0469	0.0391	0.0352	0.0469
	hold	↓	→	CKN	-0.0625	-0.0742	-0.0742	-0.0977
SE	setup	↑	→	CKN	0.1445	0.1523	0.1602	0.1914
	setup	↓	→	CKN	0.0859	0.0820	0.0781	0.1016
	hold	↑	→	CKN	0.0469	0.0391	0.0391	0.0469
	hold	↓	→	CKN	0.0156	0.0117	0.0078	0.0078
D	setup	↑	→	CKN	0.0312	0.0156	0.0078	0.0117
	setup	↓	→	CKN	0.0938	0.0781	0.0742	0.0938
	hold	↑	→	CKN	0.0352	0.0352	0.0352	0.0391
	hold	↓	→	CKN	-0.0469	-0.0391	-0.0312	-0.0391
CKN	minpwl				0.8332	0.8332	0.8332	0.8332
	minpwh				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0078	-0.0078	-0.0078	0.0039
	removal				0.0312	0.0273	0.0312	0.0195
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.1328	-0.1289	-0.1367	-0.1094
	removal				0.1758	0.1836	0.2266	0.1914

Cell Description

The SDFFQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE). The cell has a single output (Q).

Logic Symbol
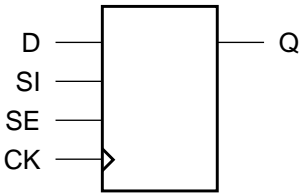
Function Table

D	SI	SE	CK	Q[n+1]
1	x	0	⌐	1
0	x	0	⌐	0
x	x	x	⌐	Q[n]
x	1	1	⌐	1
x	0	1	⌐	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFQXLADTH	2.52	7.00
SDFFQX1ADTH	2.52	7.00
SDFFQX2ADTH	2.52	7.00
SDFFQX4ADTH	2.52	8.68

Functional Schematic
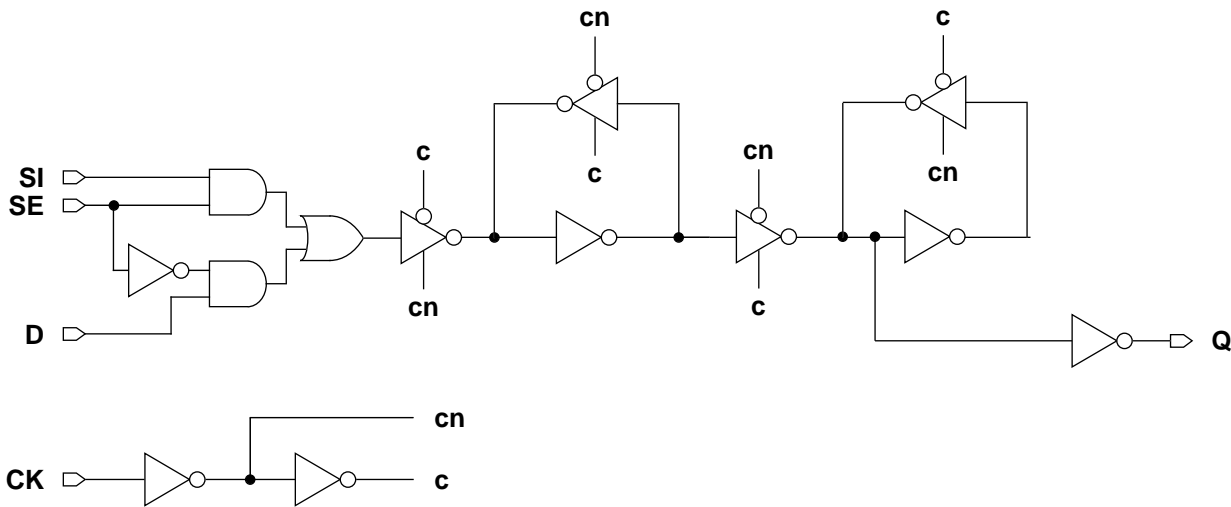
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
SI	0.0061	0.0062	0.0064	0.0070
SE	0.0077	0.0078	0.0081	0.0086
D	0.0055	0.0056	0.0059	0.0064
CK	0.0105	0.0106	0.0109	0.0123
Q	0.0036	0.0040	0.0051	0.0085

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
SI	0.0010	0.0010	0.0011	0.0010
SE	0.0029	0.0030	0.0030	0.0030
D	0.0014	0.0014	0.0016	0.0014
CK	0.0017	0.0017	0.0017	0.0018

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→ Q	↑	0.1439	0.1410	0.1392	0.1390	7.0232	4.4696	2.8535	1.4580
CK	→ Q	↓	0.1686	0.1641	0.1515	0.1429	6.7668	4.3343	1.8810	0.9050

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
SI	setup	↑	→	CK	0.1094	0.1133	0.1133	0.1250
	setup	↓	→	CK	0.2734	0.2734	0.2812	0.2969
	hold	↑	→	CK	-0.0898	-0.0898	-0.0898	-0.0938
	hold	↓	→	CK	-0.2188	-0.2188	-0.2188	-0.2227
SE	setup	↑	→	CK	0.2734	0.2734	0.2812	0.2930
	setup	↓	→	CK	0.1289	0.1289	0.1328	0.1367
	hold	↑	→	CK	-0.0859	-0.0859	-0.0859	-0.0898
	hold	↓	→	CK	-0.0547	-0.0547	-0.0508	-0.0586
D	setup	↑	→	CK	0.0977	0.0977	0.0977	0.1055
	setup	↓	→	CK	0.1055	0.1055	0.1094	0.1211
	hold	↑	→	CK	-0.0781	-0.0781	-0.0781	-0.0781
	hold	↓	→	CK	-0.0547	-0.0547	-0.0508	-0.0547
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The SDFFR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN).

Logic Symbol
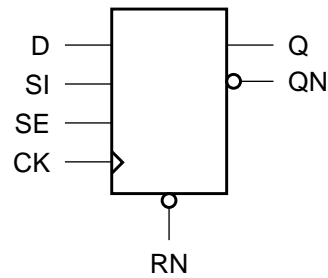
Function Table

RN	D	SI	SE	CK	Q[n+1]	QN[n+1]
1	1	x	0	⌐	1	0
1	0	x	0	⌐	0	1
1	x	x	x	⌐	Q[n]	QN[n]
1	x	1	1	⌐	1	0
1	x	0	1	⌐	0	1
0	x	x	x	x	0	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFRXLADTH	2.52	8.40
SDFFRX1ADTH	2.52	8.40
SDFFRX2ADTH	2.52	8.40
SDFFRX4ADTH	2.52	8.96

Functional Schematic
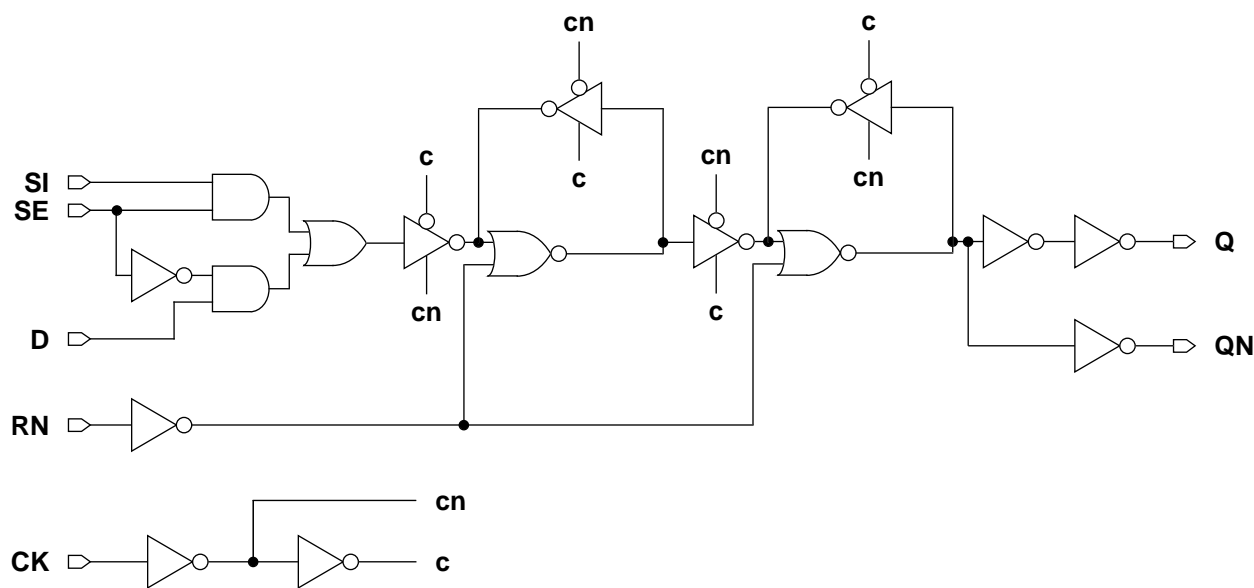
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
SI	0.0057	0.0059	0.0068	0.0077
SE	0.0069	0.0070	0.0077	0.0092
D	0.0056	0.0057	0.0066	0.0079
CK	0.0090	0.0091	0.0102	0.0114
RN	0.0010	0.0010	0.0011	0.0015
Q	0.0047	0.0055	0.0077	0.0127

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
SI	0.0009	0.0009	0.0008	0.0009
SE	0.0022	0.0022	0.0022	0.0026
D	0.0010	0.0010	0.0010	0.0014
CK	0.0017	0.0017	0.0017	0.0022
RN	0.0036	0.0036	0.0037	0.0045

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1812	0.1951	0.1771	0.2007	7.1387	4.6050	2.9348	1.5055
CK	→	Q	↓	0.1990	0.2049	0.2205	0.2236	5.8155	3.9916	1.8042	0.8928
RN	→	Q	↓	0.0901	0.1014	0.1184	0.1091	5.9543	4.0401	1.8390	0.9058
CK	→	QN	↑	0.1248	0.1209	0.1216	0.1222	7.2453	4.6014	2.9335	1.5435
CK	→	QN	↓	0.1182	0.1282	0.1095	0.1215	6.2415	4.2384	1.7580	0.9306
RN	→	QN	↑	0.1759	0.1733	0.2211	0.2489	7.1318	4.5934	2.9779	1.5928

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
SI	setup	↑	→	CK	0.1211	0.1211	0.1328	0.1250
	setup	↓	→	CK	0.1875	0.1836	0.2031	0.2031
	hold	↑	→	CK	-0.0703	-0.0742	-0.0742	-0.0508
	hold	↓	→	CK	-0.0859	-0.0898	-0.0938	-0.0859
SE	setup	↑	→	CK	0.1953	0.1914	0.2109	0.2109
	setup	↓	→	CK	0.1328	0.1328	0.1406	0.1289
	hold	↑	→	CK	-0.0547	-0.0586	-0.0625	-0.0430
	hold	↓	→	CK	-0.0391	-0.0391	-0.0469	-0.0234
D	setup	↑	→	CK	0.1055	0.1094	0.1172	0.1016
	setup	↓	→	CK	0.1406	0.1367	0.1562	0.1055
	hold	↑	→	CK	-0.0625	-0.0625	-0.0664	-0.0430
	hold	↓	→	CK	-0.0586	-0.0586	-0.0664	-0.0391
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.1133	0.1133	0.1250	0.1055
	removal				-0.0898	-0.0938	-0.0938	-0.0820

Cell Description

The SDFFRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol
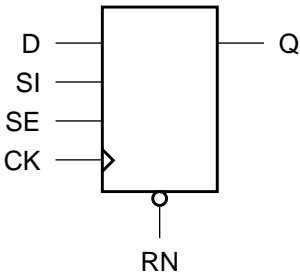
Function Table

RN	D	SI	SE	CK	Q[n+1]
1	1	x	0	⟋	1
1	0	x	0	⟋	0
1	x	x	x	⟍	Q[n]
1	x	1	1	⟋	1
1	x	0	1	⟋	0
0	x	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFRHQX1ADTH	2.52	9.52
SDFFRHQX2ADTH	2.52	9.52
SDFFRHQX4ADTH	2.52	11.20
SDFFRHQX8ADTH	2.52	12.32

Functional Schematic
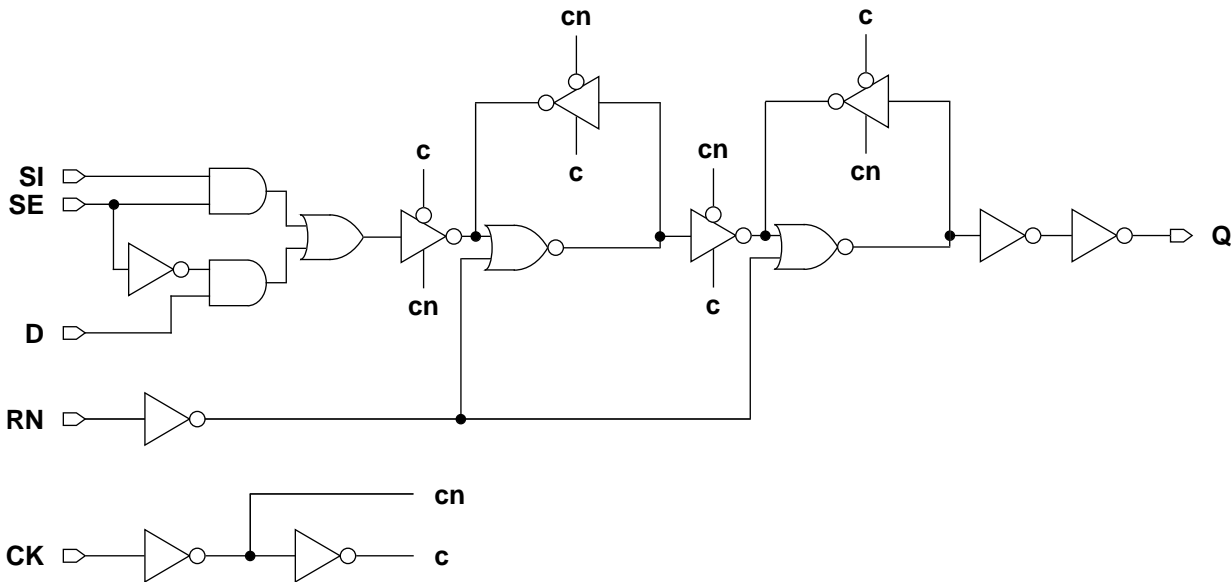
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
SI	0.0080	0.0094	0.0144	0.0160
SE	0.0092	0.0109	0.0167	0.0177
D	0.0085	0.0107	0.0156	0.0164
CK	0.0138	0.0161	0.0248	0.0293
RN	0.0012	0.0014	0.0022	0.0027
Q	0.0041	0.0050	0.0081	0.0134

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
SI	0.0012	0.0012	0.0017	0.0021
SE	0.0030	0.0032	0.0040	0.0043
D	0.0016	0.0023	0.0027	0.0026
CK	0.0021	0.0022	0.0030	0.0053
RN	0.0023	0.0028	0.0044	0.0049

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→	Q	↑	0.1183	0.1105	0.1043	0.1096	4.5819	2.8985	1.4680	0.7570
CK	→	Q	↓	0.1163	0.1073	0.1069	0.1133	4.0841	1.7455	0.8591	0.4447
RN	→	Q	↓	0.1199	0.1108	0.0948	0.0876	4.1837	1.8714	0.8986	0.4350

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
SI	setup	↑	→	CK	0.1133	0.1055	0.1094	0.0859
	setup	↓	→	CK	0.1641	0.1680	0.1680	0.1445
	hold	↑	→	CK	-0.0430	-0.0469	-0.0508	-0.0234
	hold	↓	→	CK	-0.1055	-0.1172	-0.1133	-0.0938
SE	setup	↑	→	CK	0.1758	0.1875	0.1953	0.1719
	setup	↓	→	CK	0.1406	0.1133	0.1211	0.1289
	hold	↑	→	CK	-0.0352	-0.0391	-0.0391	-0.0156
	hold	↓	→	CK	-0.0508	-0.0312	-0.0312	-0.0430
D	setup	↑	→	CK	0.1211	0.0898	0.0820	0.0898
	setup	↓	→	CK	0.1055	0.0742	0.0781	0.0898
	hold	↑	→	CK	-0.0508	-0.0352	-0.0273	-0.0273
	hold	↓	→	CK	-0.0547	-0.0352	-0.0391	-0.0430
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0195	-0.0234	-0.0273	-0.0195
	removal				0.0508	0.0625	0.0859	0.0781

Cell Description

The SDFFRQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN). The cell has a single output (Q).

Logic Symbol
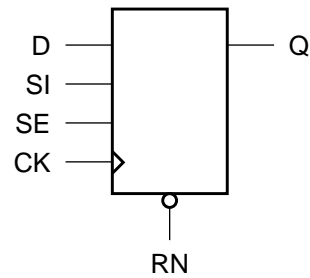
Function Table

RN	D	SI	SE	CK	Q[n+1]
1	1	x	0	⌐⌐	1
1	0	x	0	⌐⌐	0
1	x	x	x	⌐⌐	Q[n]
1	x	1	1	⌐⌐	1
1	x	0	1	⌐⌐	0
0	x	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFRQXLADTH	2.52	7.84
SDFFRQX1ADTH	2.52	7.84
SDFFRQX2ADTH	2.52	7.84
SDFFRQX4ADTH	2.52	8.40

Functional Schematic
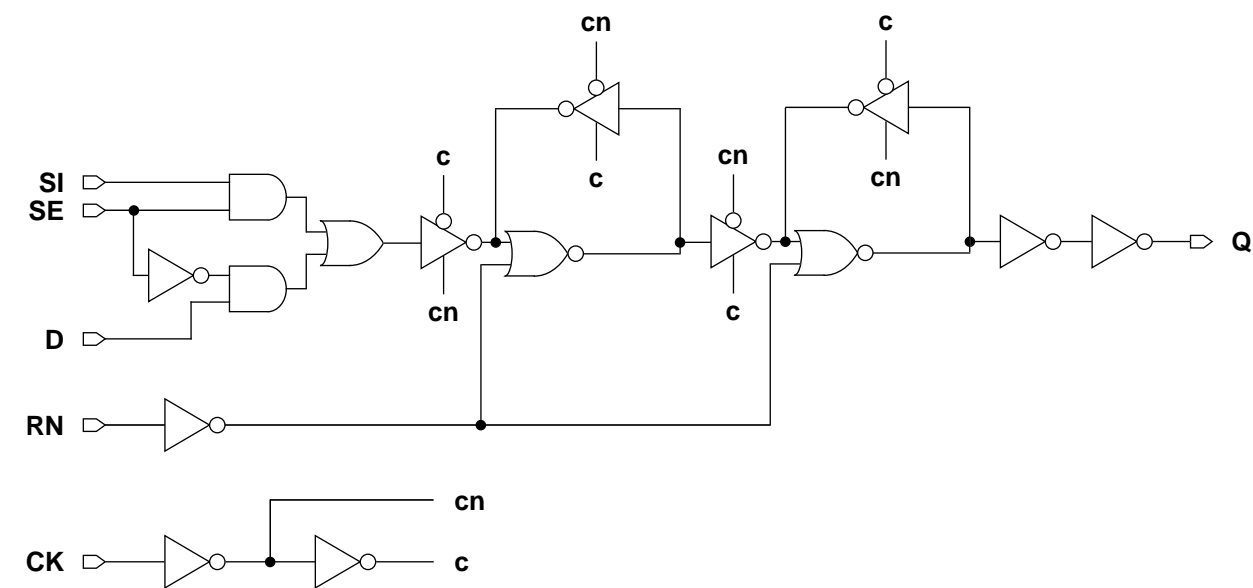
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
SI	0.0058	0.0058	0.0056	0.0057
SE	0.0069	0.0069	0.0069	0.0069
D	0.0056	0.0056	0.0056	0.0056
CK	0.0089	0.0089	0.0090	0.0088
RN	0.0011	0.0011	0.0009	0.0013
Q	0.0037	0.0041	0.0049	0.0076

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
SI	0.0009	0.0009	0.0008	0.0008
SE	0.0022	0.0022	0.0022	0.0022
D	0.0010	0.0010	0.0010	0.0010
CK	0.0017	0.0017	0.0017	0.0016
RN	0.0037	0.0037	0.0037	0.0043

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1581	0.1625	0.1564	0.1619	7.0672	4.5261	2.8758	1.4711
CK	→	Q	↓	0.1880	0.1984	0.2089	0.2072	5.5034	4.0709	1.8412	0.9021
RN	→	Q	↓	0.0891	0.1004	0.1133	0.1060	5.6521	4.1047	1.8339	0.8944

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	X1	X2	X4
SI	setup	↑	→	CK	0.1250	0.1250	0.1211	0.1211
	setup	↓	→	CK	0.1875	0.1875	0.1836	0.1836
	hold	↑	→	CK	-0.0742	-0.0742	-0.0742	-0.0742
	hold	↓	→	CK	-0.0898	-0.0938	-0.0938	-0.0898
SE	setup	↑	→	CK	0.1953	0.1953	0.1914	0.1914
	setup	↓	→	CK	0.1367	0.1367	0.1328	0.1328
	hold	↑	→	CK	-0.0586	-0.0586	-0.0625	-0.0586
	hold	↓	→	CK	-0.0430	-0.0430	-0.0469	-0.0430
D	setup	↑	→	CK	0.1094	0.1094	0.1094	0.1094
	setup	↓	→	CK	0.1406	0.1367	0.1406	0.1406
	hold	↑	→	CK	-0.0625	-0.0625	-0.0625	-0.0625
	hold	↓	→	CK	-0.0586	-0.0625	-0.0664	-0.0625
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.1172	0.1172	0.1133	0.1133
	removal				-0.0898	-0.0898	-0.0859	-0.0898

Cell Description

The SDFFS cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN).

Logic Symbol
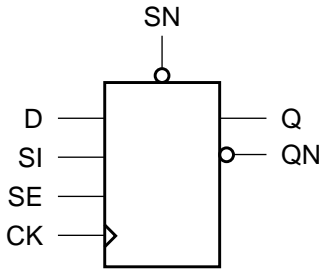
Function Table

SN	D	SI	SE	CK	Q[n+1]	QN[n+1]
1	1	x	0	⟋	1	0
1	0	x	0	⟋	0	1
1	x	x	x	⟍	Q[n]	QN[n]
1	x	1	1	⟋	1	0
1	x	0	1	⟋	0	1
0	x	x	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFSXLADTH	2.52	7.56
SDFFSX1ADTH	2.52	7.56
SDFFSX2ADTH	2.52	7.56
SDFFSX4ADTH	2.52	8.68

Functional Schematic
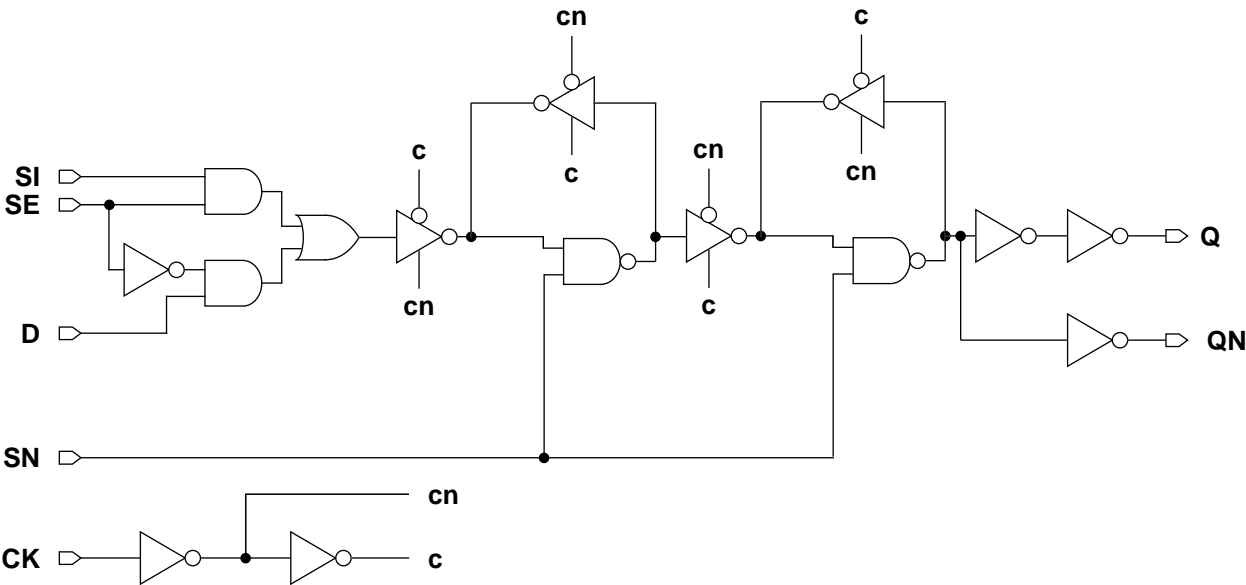
AC Power

Pin	Power (uW/MHz)			
	XL	X1	X2	X4
SI	0.0061	0.0061	0.0066	0.0085
SE	0.0073	0.0073	0.0077	0.0091
D	0.0057	0.0057	0.0061	0.0079
CK	0.0104	0.0104	0.0109	0.0127
SN	0.0010	0.0010	0.0011	0.0013
Q	0.0052	0.0059	0.0078	0.0128

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0014	0.0014	0.0014	0.0015
SE	0.0023	0.0023	0.0023	0.0023
D	0.0012	0.0012	0.0012	0.0013
CK	0.0019	0.0019	0.0020	0.0021
SN	0.0019	0.0019	0.0021	0.0028

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	X1	X2	X4	XL	X1	X2	X4
CK	→	Q	↑	0.1966	0.2091	0.2090	0.2053	6.9924	4.6711	2.9118	1.4962
CK	→	Q	↓	0.1935	0.2056	0.2061	0.2112	5.2252	3.8927	1.7262	0.8757
SN	→	Q	↑	0.1638	0.1737	0.2096	0.2983	6.9495	4.6482	2.9080	1.4989
CK	→	QN	↑	0.1394	0.1416	0.1320	0.1200	7.3429	4.8553	2.9576	1.5286
CK	→	QN	↓	0.1465	0.1600	0.1441	0.1263	6.6912	4.7090	2.0281	0.9470
SN	→	QN	↓	0.1192	0.1293	0.1451	0.1999	5.8094	4.1831	1.9370	1.0523

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	X1	X2	X4
SI	setup	↑	→	CK	0.1328	0.1289	0.1250	0.1406
	setup	↓	→	CK	0.1875	0.1836	0.1875	0.2227
	hold	↑	→	CK	-0.0703	-0.0703	-0.0742	-0.0820
	hold	↓	→	CK	-0.0938	-0.0938	-0.0977	-0.1133
SE	setup	↑	→	CK	0.2031	0.2031	0.2031	0.2383
	setup	↓	→	CK	0.1680	0.1641	0.1602	0.1680
	hold	↑	→	CK	-0.0547	-0.0547	-0.0586	-0.0703
	hold	↓	→	CK	-0.0430	-0.0430	-0.0430	-0.0586
D	setup	↑	→	CK	0.1328	0.1289	0.1250	0.1328
	setup	↓	→	CK	0.1445	0.1445	0.1445	0.1758
	hold	↑	→	CK	-0.0703	-0.0703	-0.0742	-0.0781
	hold	↓	→	CK	-0.0664	-0.0664	-0.0703	-0.0820
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0391	-0.0391	-0.0430	-0.0391
	removal				0.0625	0.0625	0.0664	0.0664

Cell Description

The SDFFSHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN). The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol
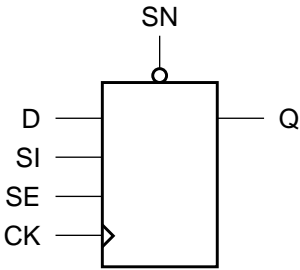
Function Table

SN	D	SI	SE	CK	Q[n+1]
1	1	x	0	⌐⌐	1
1	0	x	0	⌐⌐	0
1	x	x	x	⌐⌐	Q[n]
1	x	1	1	⌐⌐	1
1	x	0	1	⌐⌐	0
0	x	x	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFSHQX1ADTH	2.52	9.52
SDFFSHQX2ADTH	2.52	9.52
SDFFSHQX4ADTH	2.52	11.48
SDFFSHQX8ADTH	2.52	12.32

Functional Schematic
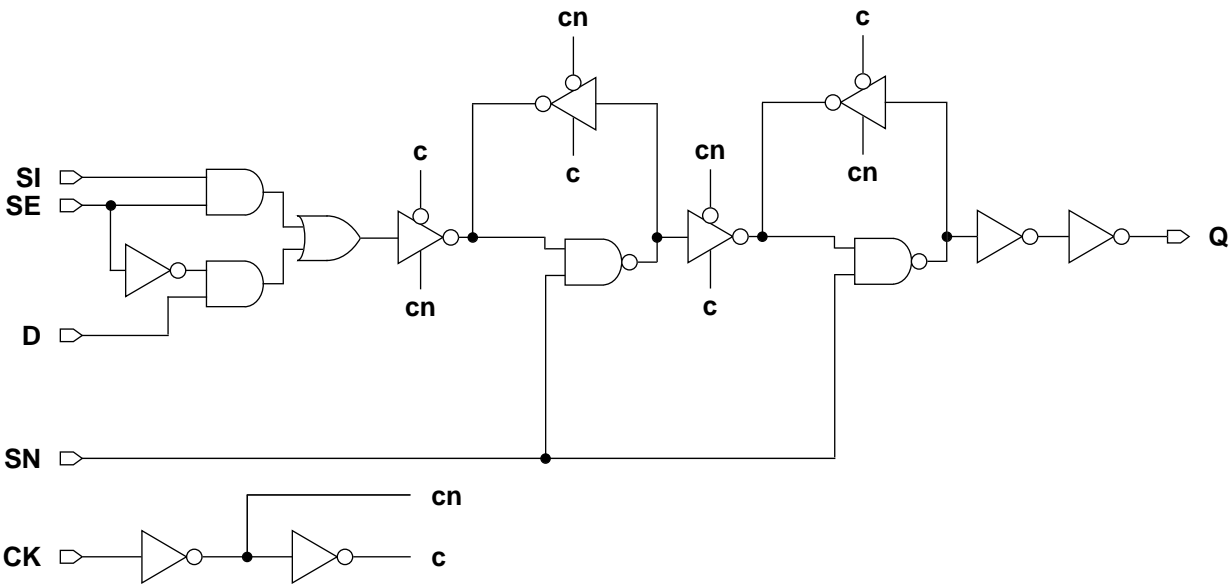
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
SI	0.0074	0.0085	0.0114	0.0127
SE	0.0089	0.0103	0.0136	0.0147
D	0.0074	0.0091	0.0126	0.0130
CK	0.0128	0.0149	0.0203	0.0216
SN	0.0032	0.0033	0.0040	0.0042
Q	0.0041	0.0052	0.0084	0.0133

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
SI	0.0012	0.0012	0.0013	0.0019
SE	0.0028	0.0030	0.0036	0.0039
D	0.0013	0.0017	0.0023	0.0023
CK	0.0020	0.0021	0.0030	0.0039
SN	0.0023	0.0026	0.0029	0.0030

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→	Q	↑	0.1080	0.1022	0.0951	0.1009	4.5157	2.8874	1.4733	0.7566
CK	→	Q	↓	0.1177	0.1163	0.1031	0.1134	4.0314	1.7789	0.8624	0.4443
SN	→	Q	↑	0.1634	0.1835	0.1507	0.1569	4.8919	2.9941	1.4688	0.7496

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
SI	setup	↑	→	CK	0.1172	0.1055	0.1211	0.1016
	setup	↓	→	CK	0.1602	0.1680	0.1914	0.1406
	hold	↑	→	CK	-0.0586	-0.0547	-0.0547	-0.0352
	hold	↓	→	CK	-0.1094	-0.1133	-0.1250	-0.0820
SE	setup	↑	→	CK	0.1797	0.1914	0.2188	0.1680
	setup	↓	→	CK	0.1406	0.1133	0.1172	0.1328
	hold	↑	→	CK	-0.0469	-0.0430	-0.0469	-0.0273
	hold	↓	→	CK	-0.0547	-0.0352	-0.0352	-0.0391
D	setup	↑	→	CK	0.1172	0.0859	0.0859	0.0977
	setup	↓	→	CK	0.1250	0.0977	0.1016	0.1094
	hold	↑	→	CK	-0.0586	-0.0352	-0.0273	-0.0312
	hold	↓	→	CK	-0.0742	-0.0508	-0.0469	-0.0508
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.0391	0.0312	0.0469	0.0508
	removal				-0.0195	-0.0156	-0.0234	-0.0312

Cell Description

The SDFFSQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN). The cell has a single output (Q).

Logic Symbol
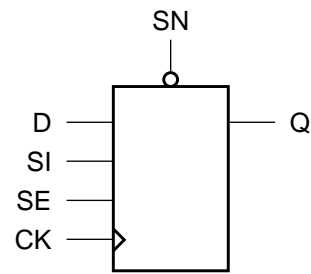
Function Table

SN	D	SI	SE	CK	Q[n+1]
1	1	x	0	⌐⌐	1
1	0	x	0	⌐⌐	0
1	x	x	x	⌐⌐	Q[n]
1	x	1	1	⌐⌐	1
1	x	0	1	⌐⌐	0
0	x	x	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFSQXLADTH	2.52	7.00
SDFFSQX1ADTH	2.52	7.28
SDFFSQX2ADTH	2.52	7.28
SDFFSQX4ADTH	2.52	7.56

Functional Schematic
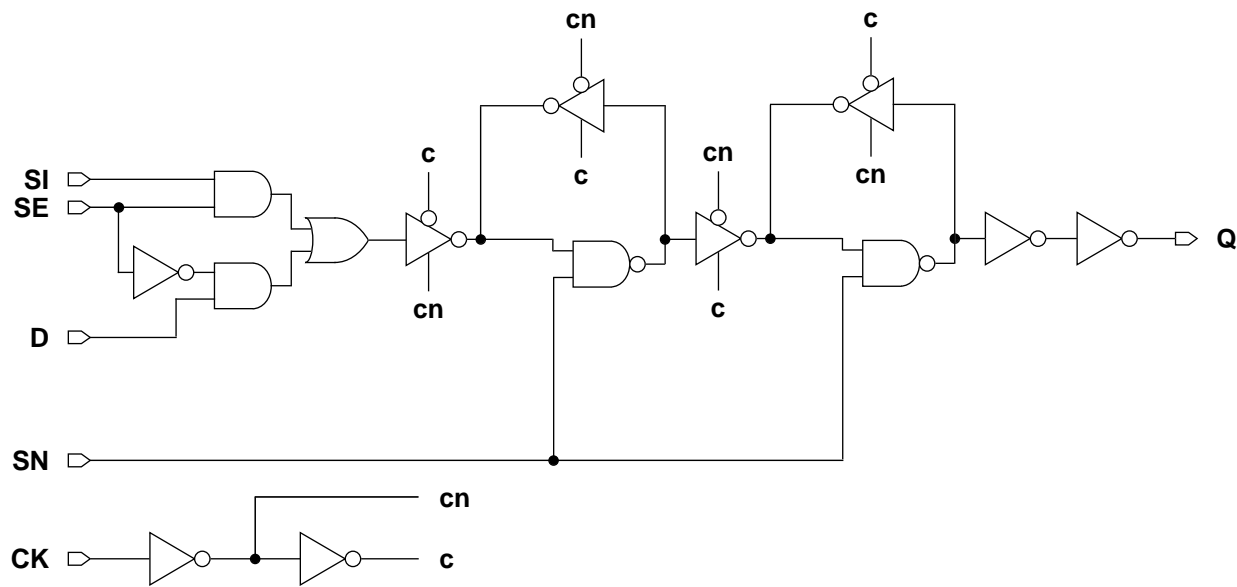
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
SI	0.0063	0.0063	0.0063	0.0064
SE	0.0072	0.0072	0.0072	0.0073
D	0.0058	0.0058	0.0058	0.0059
CK	0.0102	0.0102	0.0102	0.0103
SN	0.0010	0.0010	0.0010	0.0011
Q	0.0039	0.0044	0.0053	0.0079

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
SI	0.0015	0.0015	0.0015	0.0015
SE	0.0023	0.0023	0.0023	0.0023
D	0.0012	0.0012	0.0012	0.0012
CK	0.0019	0.0020	0.0019	0.0019
SN	0.0019	0.0019	0.0019	0.0019

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1595	0.1652	0.1756	0.1943	6.7446	4.4943	2.8936	1.4747
CK	→	Q	↓	0.1733	0.1842	0.1935	0.2112	5.6589	3.9591	1.7505	0.8885
SN	→	Q	↑	0.1386	0.1475	0.1553	0.1707	6.7214	4.4821	2.8887	1.4715

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
SI	setup	↑	→	CK	0.1484	0.1484	0.1406	0.1406
	setup	↓	→	CK	0.1914	0.1914	0.1875	0.1875
	hold	↑	→	CK	-0.0742	-0.0742	-0.0742	-0.0742
	hold	↓	→	CK	-0.0938	-0.0938	-0.0977	-0.0977
SE	setup	↑	→	CK	0.2070	0.2109	0.2031	0.2070
	setup	↓	→	CK	0.1836	0.1836	0.1797	0.1758
	hold	↑	→	CK	-0.0586	-0.0586	-0.0586	-0.0586
	hold	↓	→	CK	-0.0430	-0.0430	-0.0430	-0.0469
D	setup	↑	→	CK	0.1523	0.1484	0.1445	0.1406
	setup	↓	→	CK	0.1484	0.1523	0.1445	0.1484
	hold	↑	→	CK	-0.0742	-0.0742	-0.0742	-0.0742
	hold	↓	→	CK	-0.0664	-0.0664	-0.0664	-0.0703
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0312	-0.0312	-0.0352	-0.0352
	removal				0.0586	0.0547	0.0586	0.0586

Cell Description

The SDFFSR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN). Set (SN) dominates reset (RN).

Logic Symbol
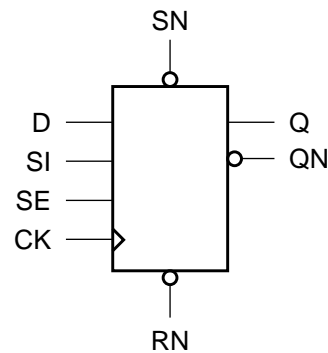
Function Table

RN	SN	D	SI	SE	CK	Q[n+1]	QN[n+1]
1	1	1	x	0	⌐╱	1	0
1	1	0	x	0	╱	0	1
1	1	x	x	x	╲	Q[n]	QN[n]
1	1	x	1	1	╱	1	0
1	1	x	0	1	╱	0	1
0	1	x	x	x	x	0	1
1	0	x	x	x	x	1	0
0	0	x	x	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFSRXLADTH	2.52	9.24
SDFFSRX1ADTH	2.52	9.52
SDFFSRX2ADTH	2.52	9.80
SDFFSRX4ADTH	2.52	11.76

Functional Schematic
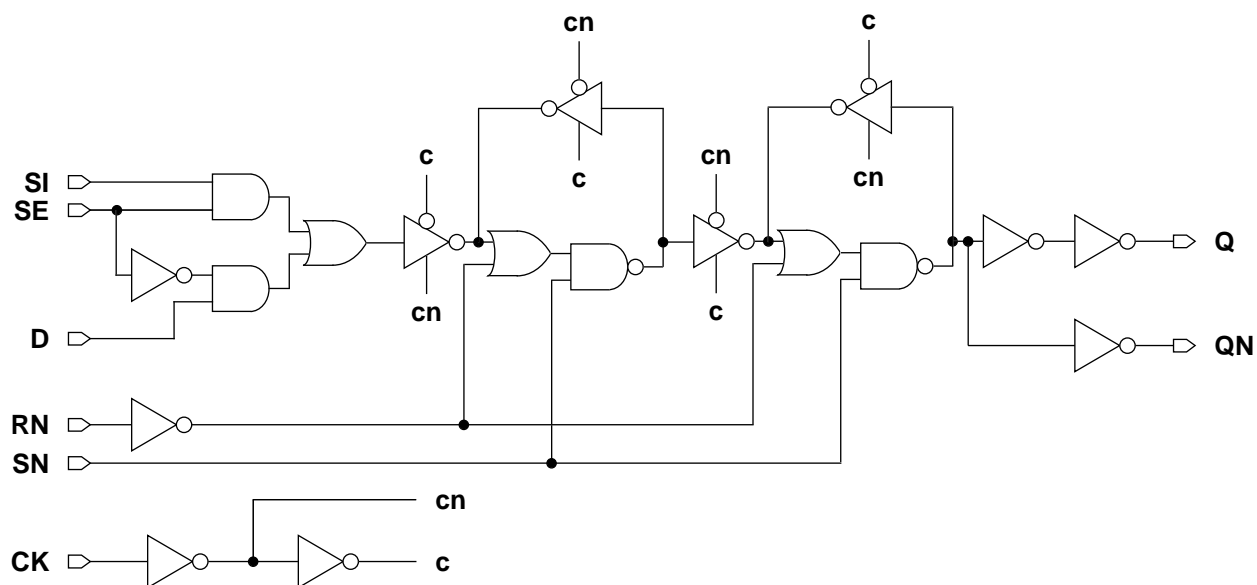
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
SI	0.0067	0.0068	0.0074	0.0105
SE	0.0081	0.0081	0.0088	0.0111
D	0.0063	0.0063	0.0070	0.0099
CK	0.0109	0.0109	0.0121	0.0161
SN	0.0010	0.0011	0.0011	0.0013
RN	0.0022	0.0022	0.0023	0.0026
Q	0.0054	0.0062	0.0085	0.0127

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
SI	0.0013	0.0013	0.0013	0.0013
SE	0.0023	0.0023	0.0023	0.0024
D	0.0012	0.0012	0.0012	0.0014
CK	0.0017	0.0017	0.0018	0.0021
SN	0.0020	0.0020	0.0023	0.0030
RN	0.0012	0.0012	0.0012	0.0012

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.2124	0.2252	0.2273	0.2093	7.0571	4.5627	2.9258	1.4974
CK	→	Q	↓	0.2075	0.2203	0.2185	0.2237	5.2630	3.9025	1.7173	0.8755
SN	→	Q	↑	0.1833	0.1937	0.2333	0.3174	6.9907	4.5243	2.9185	1.4994
SN	→	Q	↓	0.1636	0.1749	0.1914	0.2194	5.2188	3.8835	1.7132	0.8764
RN	→	Q	↓	0.1916	0.2030	0.2276	0.2757	5.2319	3.8880	1.7148	0.8765
CK	→	QN	↑	0.1499	0.1512	0.1446	0.1328	7.5805	4.8641	3.0115	1.5315
CK	→	QN	↓	0.1609	0.1748	0.1611	0.1292	7.1984	5.0455	2.1221	0.9667
SN	→	QN	↑	0.1080	0.1085	0.1153	0.1184	7.3029	4.7003	3.0046	1.5630
SN	→	QN	↓	0.1384	0.1486	0.1685	0.2174	5.9823	4.2825	1.9703	1.0668
RN	→	QN	↑	0.1343	0.1351	0.1507	0.1776	7.4117	4.7494	3.0180	1.5727

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
SI	setup	↑	→	CK	0.1680	0.1641	0.1484	0.1719
	setup	↓	→	CK	0.2031	0.2031	0.2109	0.2500
	hold	↑	→	CK	-0.0742	-0.0742	-0.0781	-0.0938
	hold	↓	→	CK	-0.1016	-0.1055	-0.1055	-0.1211
SE	setup	↑	→	CK	0.2227	0.2227	0.2266	0.2734
	setup	↓	→	CK	0.2070	0.2031	0.1875	0.1797
	hold	↑	→	CK	-0.0586	-0.0625	-0.0664	-0.0781
	hold	↓	→	CK	-0.0508	-0.0508	-0.0508	-0.0586
D	setup	↑	→	CK	0.1719	0.1680	0.1523	0.1445
	setup	↓	→	CK	0.1602	0.1602	0.1641	0.1836
	hold	↑	→	CK	-0.0781	-0.0781	-0.0820	-0.0742
	hold	↓	→	CK	-0.0742	-0.0781	-0.0781	-0.0859
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0312	-0.0312	-0.0430	-0.0508
	removal				0.0547	0.0547	0.0664	0.0820
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.1016	0.0938	0.0703	0.0742
	removal				-0.0312	-0.0312	-0.0234	-0.0195

Cell Description

The SDFFSRHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN), and set dominating reset. The cell has a single output (Q) and fast clock-to-out path.

Logic Symbol
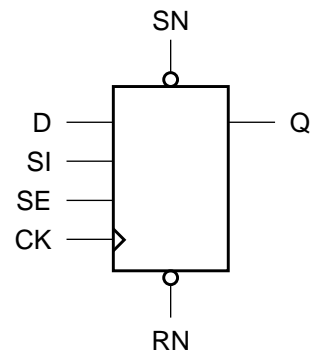
Function Table

RN	SN	D	SI	SE	CK	Q[n+1]
1	1	1	x	0	⤒	1
1	1	0	x	0	⤒	0
1	1	x	x	x	⤓	Q[n]
1	1	x	1	1	⤒	1
1	1	x	0	1	⤒	0
0	1	x	x	x	x	0
1	0	x	x	x	x	1
0	0	x	x	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFSRHQX1ADTH	2.52	11.48
SDFFSRHQX2ADTH	2.52	11.48
SDFFSRHQX4ADTH	2.52	13.72
SDFFSRHQX8ADTH	2.52	14.56

Functional Schematic
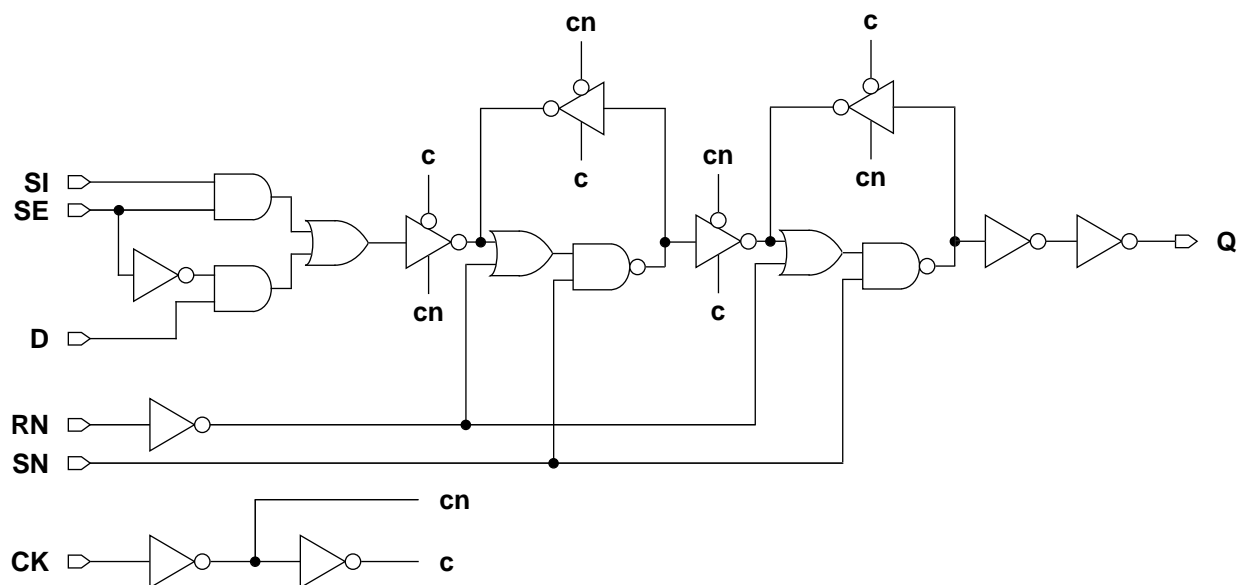
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
SI	0.0080	0.0092	0.0138	0.0155
SE	0.0093	0.0105	0.0149	0.0170
D	0.0081	0.0096	0.0146	0.0161
CK	0.0140	0.0160	0.0231	0.0265
SN	0.0039	0.0040	0.0051	0.0059
RN	0.0010	0.0012	0.0020	0.0026
Q	0.0048	0.0059	0.0089	0.0147

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
SI	0.0013	0.0012	0.0016	0.0020
SE	0.0030	0.0029	0.0033	0.0040
D	0.0012	0.0016	0.0023	0.0026
CK	0.0021	0.0021	0.0028	0.0040
SN	0.0022	0.0025	0.0032	0.0036
RN	0.0019	0.0022	0.0034	0.0039

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→ Q	↑	0.1328	0.1249	0.1155	0.1146	4.6877	2.9350	1.4823	0.7689
CK	→ Q	↓	0.1390	0.1275	0.1203	0.1136	4.3484	1.8451	0.8937	0.4592
SN	→ Q	↑	0.1404	0.1617	0.2096	0.1948	4.5602	2.9161	1.4822	0.7555
SN	→ Q	↓	0.2782	0.2571	0.2398	0.2644	4.7906	2.1980	1.0737	0.5500
RN	→ Q	↓	0.2431	0.2154	0.1887	0.2246	4.8186	2.1991	1.0753	0.5518

**Timing Constraints at 25°C,1.0V, Typical Process**

Pin	Requirement				Interval (ns)			
					X1	X2	X4	X8
SI	setup	↑	→	CK	0.1328	0.1211	0.1289	0.1328
	setup	↓	→	CK	0.1680	0.1602	0.1484	0.1758
	hold	↑	→	CK	-0.0547	-0.0547	-0.0586	-0.0391
	hold	↓	→	CK	-0.1094	-0.1055	-0.0859	-0.0977
SE	setup	↑	→	CK	0.1914	0.1836	0.1719	0.1992
	setup	↓	→	CK	0.1641	0.1406	0.1602	0.1758
	hold	↑	→	CK	-0.0469	-0.0430	-0.0469	-0.0312
	hold	↓	→	CK	-0.0625	-0.0469	-0.0391	-0.0391
D	setup	↑	→	CK	0.1367	0.1094	0.1172	0.1367
	setup	↓	→	CK	0.1367	0.1055	0.0938	0.1055
	hold	↑	→	CK	-0.0586	-0.0469	-0.0469	-0.0430
	hold	↓	→	CK	-0.0820	-0.0547	-0.0391	-0.0391
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.0469	0.0312	0.0352	0.0508
	removal				-0.0273	-0.0156	-0.0156	-0.0273
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				-0.0195	-0.0273	-0.0234	-0.0039
	removal				0.0508	0.0625	0.0703	0.0508

Cell Description

The SDFFTR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-low reset (RN). Scan enable (SE) dominates reset (RN).

Logic Symbol

Function Table
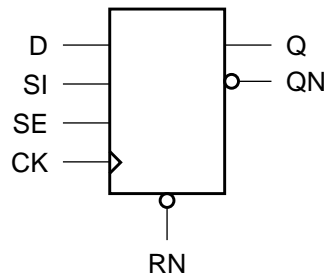
RN	D	SI	SE	CK	Q[n+1]	QN[n+1]
x	x	0	1	⌐⌐	0	1
x	x	1	1	⌐⌐	1	0
0	x	x	0	⌐⌐	0	1
1	0	x	0	⌐⌐	0	1
1	1	x	0	⌐⌐	1	0
x	x	x	x	⌐⌐	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFTRXLADTH	2.52	7.84
SDFFTRX1ADTH	2.52	8.12
SDFFTRX2ADTH	2.52	8.12
SDFFTRX4ADTH	2.52	10.08

Functional Schematic
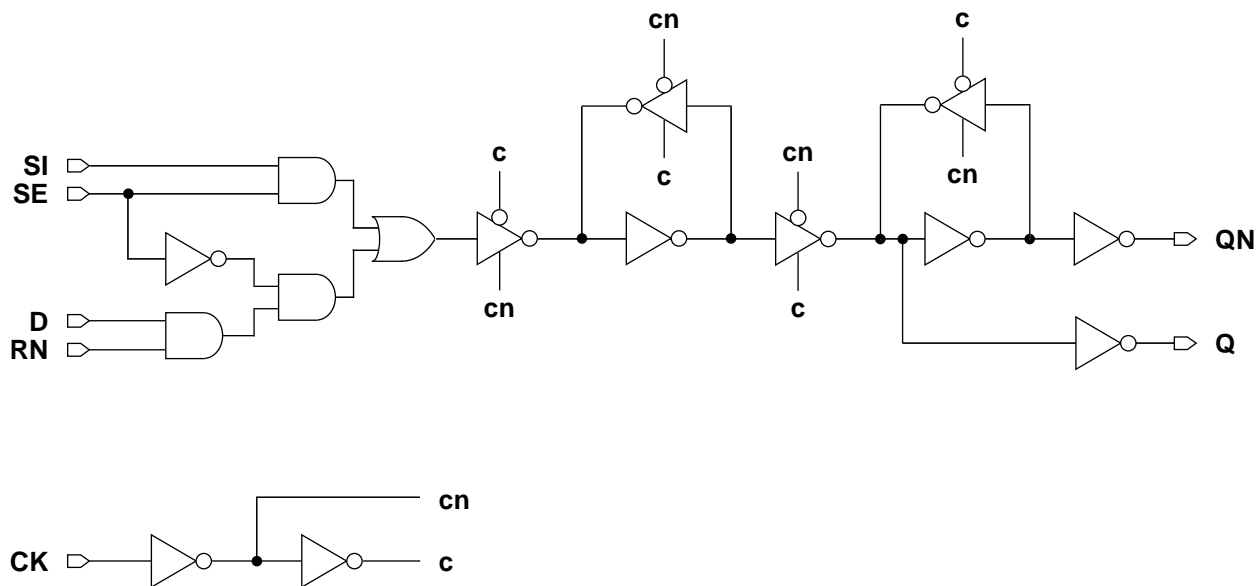
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
SI	0.0063	0.0067	0.0075	0.0116
SE	0.0080	0.0083	0.0090	0.0126
D	0.0060	0.0064	0.0071	0.0110
CK	0.0092	0.0096	0.0106	0.0150
RN	0.0066	0.0070	0.0078	0.0128
Q	0.0050	0.0057	0.0077	0.0125

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
SI	0.0011	0.0011	0.0011	0.0012
SE	0.0036	0.0037	0.0036	0.0040
D	0.0010	0.0010	0.0010	0.0013
CK	0.0017	0.0017	0.0018	0.0022
RN	0.0018	0.0018	0.0018	0.0021

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→	Q	↑	0.1589	0.1550	0.1596	0.1481	6.9726	4.5036	2.9033	1.4815
CK	→	Q	↓	0.1789	0.1828	0.1906	0.1792	5.2163	3.8725	1.7074	0.8293
CK	→	QN	↑	0.1248	0.1195	0.1222	0.1164	7.2156	4.5659	2.9027	1.4895
CK	→	QN	↓	0.1169	0.1145	0.1088	0.0976	6.2712	4.0927	1.7397	0.8438

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
SI	setup	↑	→	CK	0.1211	0.1211	0.1211	0.1484
	setup	↓	→	CK	0.2109	0.2148	0.2305	0.2734
	hold	↑	→	CK	-0.0664	-0.0703	-0.0703	-0.0820
	hold	↓	→	CK	-0.1094	-0.1094	-0.1211	-0.1367
SE	setup	↑	→	CK	0.2188	0.2227	0.2383	0.2891
	setup	↓	→	CK	0.1602	0.1641	0.1641	0.1562
	hold	↑	→	CK	-0.0586	-0.0625	-0.0586	-0.0742
	hold	↓	→	CK	-0.0586	-0.0586	-0.0703	-0.0508
D	setup	↑	→	CK	0.1328	0.1328	0.1328	0.1250
	setup	↓	→	CK	0.1602	0.1641	0.1797	0.1562
	hold	↑	→	CK	-0.0781	-0.0781	-0.0781	-0.0703
	hold	↓	→	CK	-0.0781	-0.0781	-0.0898	-0.0703
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
RN	setup	↑	→	CK	0.1367	0.1367	0.1367	0.1289
	setup	↓	→	CK	0.2266	0.2305	0.2461	0.3086
	hold	↑	→	CK	-0.0820	-0.0859	-0.0859	-0.0742
	hold	↓	→	CK	-0.1133	-0.1133	-0.1289	-0.1484

Cell Description

The SDFFYQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE). The cell has a single output (Q) and overdriven feedback loops to increase mean time between failure (MTBF) due to metastability.
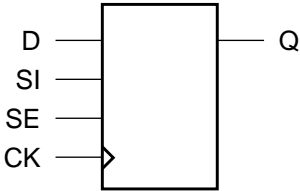
Logic Symbol

Function Table

D	SI	SE	CK	Q[n+1]
1	x	0	⌐	1
0	x	0	⌐	0
x	x	x	⌐	Q[n]
x	1	1	⌐	1
x	0	1	⌐	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFYQX2ADTH	2.52	8.12

Functional Schematic
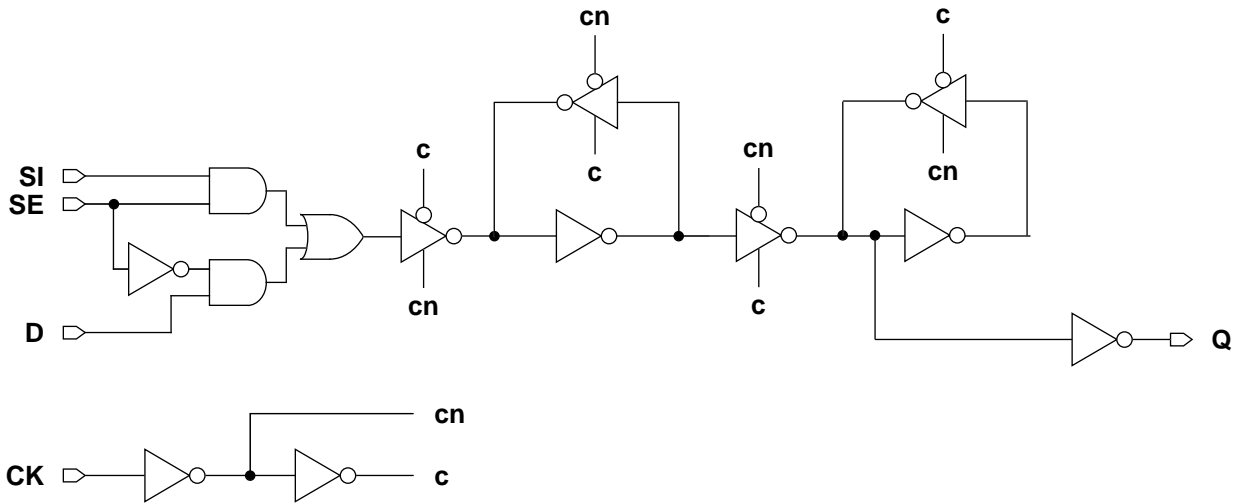
AC Power

Pin	Power (uW/MHz)
	X2
SI	0.0104
SE	0.0137
D	0.0095
CK	0.0166
Q	0.0051

Pin Capacitance

Pin	Capacitance (pF)
	X2
SI	0.0010
SE	0.0049
D	0.0023
CK	0.0023

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X2	**X2**
CK → Q ↑	0.1313	2.8699
CK → Q ↓	0.1349	1.8338

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)
		X2
SI	setup ↑ → CK	0.1445
	setup ↓ → CK	0.4414
	hold ↑ → CK	-0.1250
	hold ↓ → CK	-0.3906
SE	setup ↑ → CK	0.4609
	setup ↓ → CK	0.1211
	hold ↑ → CK	-0.1250
	hold ↓ → CK	-0.0547
D	setup ↑ → CK	0.0469
	setup ↓ → CK	0.1211
	hold ↑ → CK	-0.0352
	hold ↓ → CK	-0.0742
CK	minpwh	0.8332
	minpwl	0.8332

Cell Description

The SEDFF cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-high enable (E).

Logic Symbol
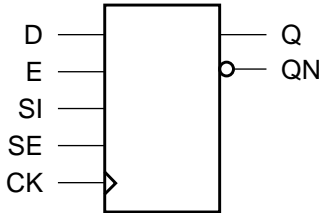
Function Table

D	E	SI	SE	CK	Q[n+1]	QN[n+1]
x	x	1	1	⌐	1	0
x	x	0	1	⌐	0	1
x	0	x	0	⌐	Q[n]	QN[n]
0	1	x	0	⌐	0	1
1	1	x	0	⌐	1	0
x	x	x	x	⌐	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
SEDFFXLADTH	2.52	8.68
SEDFFX1ADTH	2.52	8.96
SEDFFX2ADTH	2.52	9.24
SEDFFX4ADTH	2.52	11.48

Functional Schematic
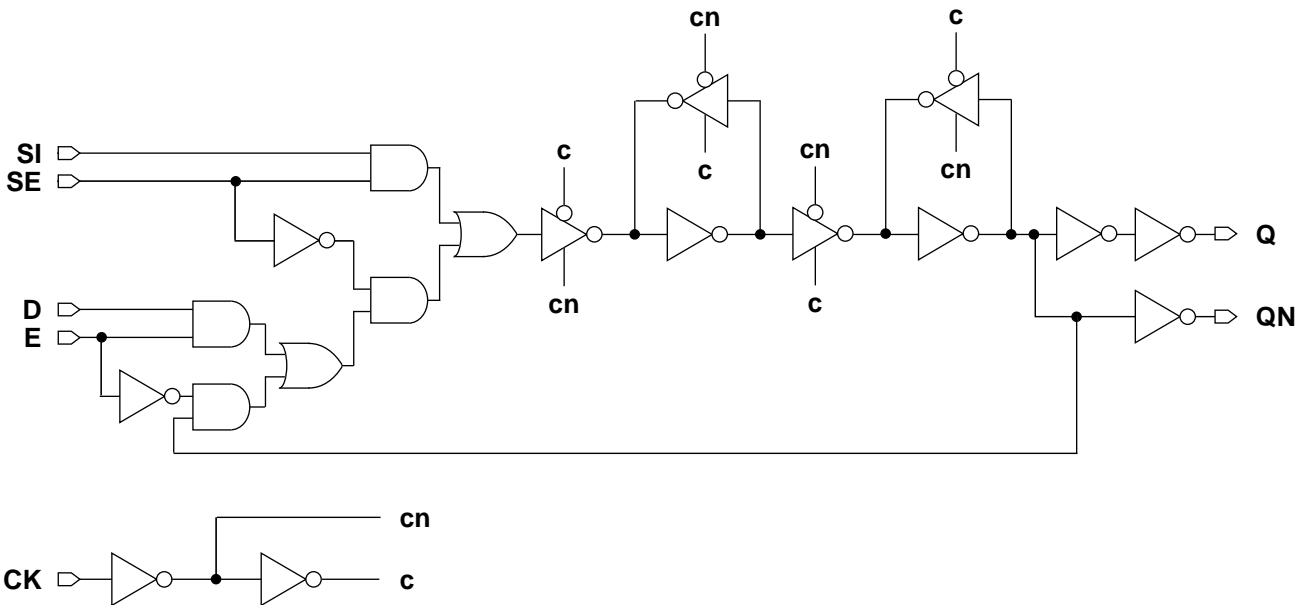
AC Power

Pin	Power (uW/MHz)			
	XL	X1	X2	X4
SI	0.0062	0.0063	0.0077	0.0087
SE	0.0081	0.0082	0.0097	0.0109
D	0.0052	0.0053	0.0062	0.0071
CK	0.0098	0.0100	0.0108	0.0133
E	0.0077	0.0078	0.0091	0.0102
Q	0.0061	0.0068	0.0094	0.0155

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
SI	0.0010	0.0010	0.0010	0.0010
SE	0.0023	0.0023	0.0026	0.0026
D	0.0010	0.0010	0.0014	0.0014
CK	0.0015	0.0015	0.0015	0.0017
E	0.0024	0.0024	0.0028	0.0028

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	X1	X2	X4	XL	X1	X2	X4
CK	→	Q	↑	0.1397	0.1321	0.1337	0.1475	7.1740	4.4627	2.8668	1.4946
CK	→	Q	↓	0.1588	0.1518	0.1349	0.1359	6.2375	4.2737	1.8082	0.9073
CK	→	QN	↑	0.2291	0.2149	0.1987	0.2007	7.1035	4.5152	2.8869	1.4857
CK	→	QN	↓	0.2133	0.2168	0.2088	0.2157	5.4832	4.0358	1.7371	0.8406

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
SI	setup	↑	→	CK	0.0977	0.0977	0.1641	0.1680
	setup	↓	→	CK	0.3633	0.3633	0.3633	0.3945
	hold	↑	→	CK	-0.0820	-0.0820	-0.1211	-0.1211
	hold	↓	→	CK	-0.2930	-0.2930	-0.2969	-0.3086
SE	setup	↑	→	CK	0.3711	0.3750	0.3516	0.3789
	setup	↓	→	CK	0.4102	0.4141	0.2148	0.2227
	hold	↑	→	CK	-0.0703	-0.0703	-0.1211	-0.1211
	hold	↓	→	CK	-0.1406	-0.1406	-0.1250	-0.1172
D	setup	↑	→	CK	0.1133	0.1133	0.1680	0.1758
	setup	↓	→	CK	0.3828	0.3828	0.1562	0.1680
	hold	↑	→	CK	-0.0898	-0.0898	-0.1250	-0.1289
	hold	↓	→	CK	-0.3164	-0.3164	-0.0977	-0.0898
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
E	setup	↑	→	CK	0.4180	0.4180	0.1914	0.2070
	setup	↓	→	CK	0.3438	0.3477	0.1992	0.2031
	hold	↑	→	CK	-0.0938	-0.0938	-0.1406	-0.1367
	hold	↓	→	CK	-0.1328	-0.1328	-0.0938	-0.0820

TSMC CLN90G HVT

Cell Description

The SEDFFHQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-high enable (E). The cell has a single output (Q) and fast clock-to-output path.

Logic Symbol
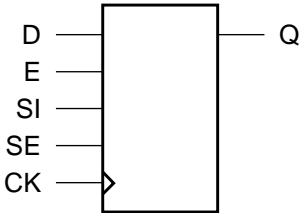
Function Table

D	E	SI	SE	CK	Q[n+1]
x	x	1	1	⎍	1
x	x	0	1	⎍	0
x	0	x	0	⎍	Q[n]
0	1	x	0	⎍	0
1	1	x	0	⎍	1
x	x	x	x	⎍	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
SEDFFHQX1ADTH	2.52	11.76
SEDFFHQX2ADTH	2.52	13.44
SEDFFHQX4ADTH	2.52	15.12
SEDFFHQX8ADTH	2.52	19.60

Functional Schematic
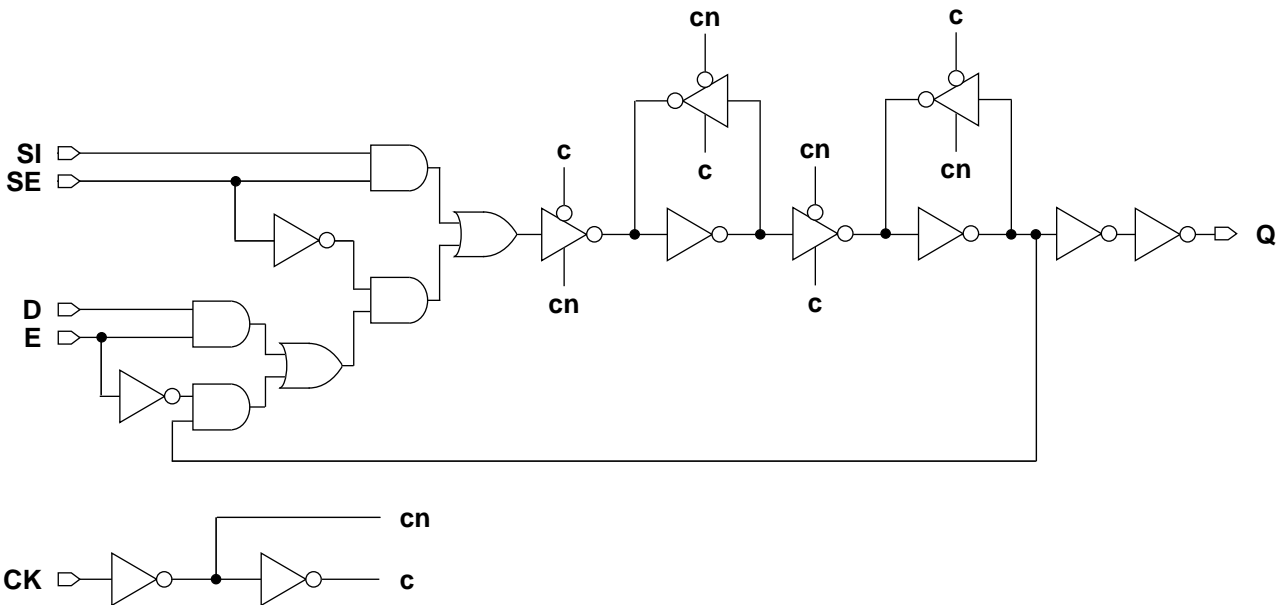
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
SI	0.0076	0.0101	0.0140	0.0220
SE	0.0132	0.0161	0.0199	0.0309
D	0.0081	0.0116	0.0165	0.0284
CK	0.0137	0.0186	0.0253	0.0366
E	0.0135	0.0165	0.0204	0.0290
Q	0.0053	0.0070	0.0091	0.0155

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
SI	0.0011	0.0011	0.0011	0.0014
SE	0.0034	0.0034	0.0036	0.0046
D	0.0016	0.0026	0.0038	0.0074
CK	0.0025	0.0026	0.0033	0.0044
E	0.0025	0.0026	0.0026	0.0027

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→ Q	↑	0.0998	0.0990	0.0919	0.0813	4.4448	2.8506	1.4610	0.7439
CK	→ Q	↓	0.1195	0.1155	0.0978	0.0866	4.1313	1.7802	0.8519	0.4162

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	**X2**	**X4**	**X8**
SI	setup	↑	→	CK	0.1289	0.1328	0.1484	0.1680
	setup	↓	→	CK	0.1992	0.2266	0.2773	0.2852
	hold	↑	→	CK	-0.0781	-0.0820	-0.0898	-0.0977
	hold	↓	→	CK	-0.1484	-0.1719	-0.2070	-0.2070
SE	setup	↑	→	CK	0.2695	0.3047	0.3711	0.3984
	setup	↓	→	CK	0.2266	0.2109	0.1992	0.2227
	hold	↑	→	CK	-0.0938	-0.1055	-0.1289	-0.1523
	hold	↓	→	CK	-0.1680	-0.1484	-0.1406	-0.1445
D	setup	↑	→	CK	0.1172	0.1016	0.0820	0.0938
	setup	↓	→	CK	0.1094	0.0898	0.0781	0.0898
	hold	↑	→	CK	-0.0664	-0.0547	-0.0352	-0.0352
	hold	↓	→	CK	-0.0664	-0.0508	-0.0352	-0.0430
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
E	setup	↑	→	CK	0.1758	0.1602	0.1484	0.1758
	setup	↓	→	CK	0.2422	0.2695	0.2617	0.2539
	hold	↑	→	CK	-0.1445	-0.1250	-0.1133	-0.1211
	hold	↓	→	CK	-0.1367	-0.1406	-0.1367	-0.1367

Cell Description

The SEDFFTR cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), synchronous active-high enable (E) and synchronous active low reset (RN). Scan enable (SE) dominates reset (RN) and enable (E).

Logic Symbol
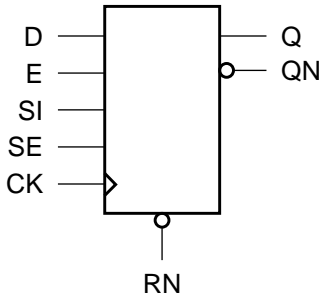
Function Table

RN	D	E	SI	SE	CK	Q[n+1]	QN[n+1]
x	x	x	0	1	⌐	0	1
x	x	x	1	1	⌐	1	0
1	x	0	x	0	⌐	Q[n]	QN[n]
0	x	x	x	0	⌐	0	1
1	1	1	x	0	⌐	1	0
1	0	1	x	0	⌐	0	1
x	x	x	x	x	⌐⌐	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
SEDFFTRXLADTH	2.52	12.60
SEDFFTRX1ADTH	2.52	12.60
SEDFFTRX2ADTH	2.52	12.60
SEDFFTRX4ADTH	2.52	14.56

Functional Schematic
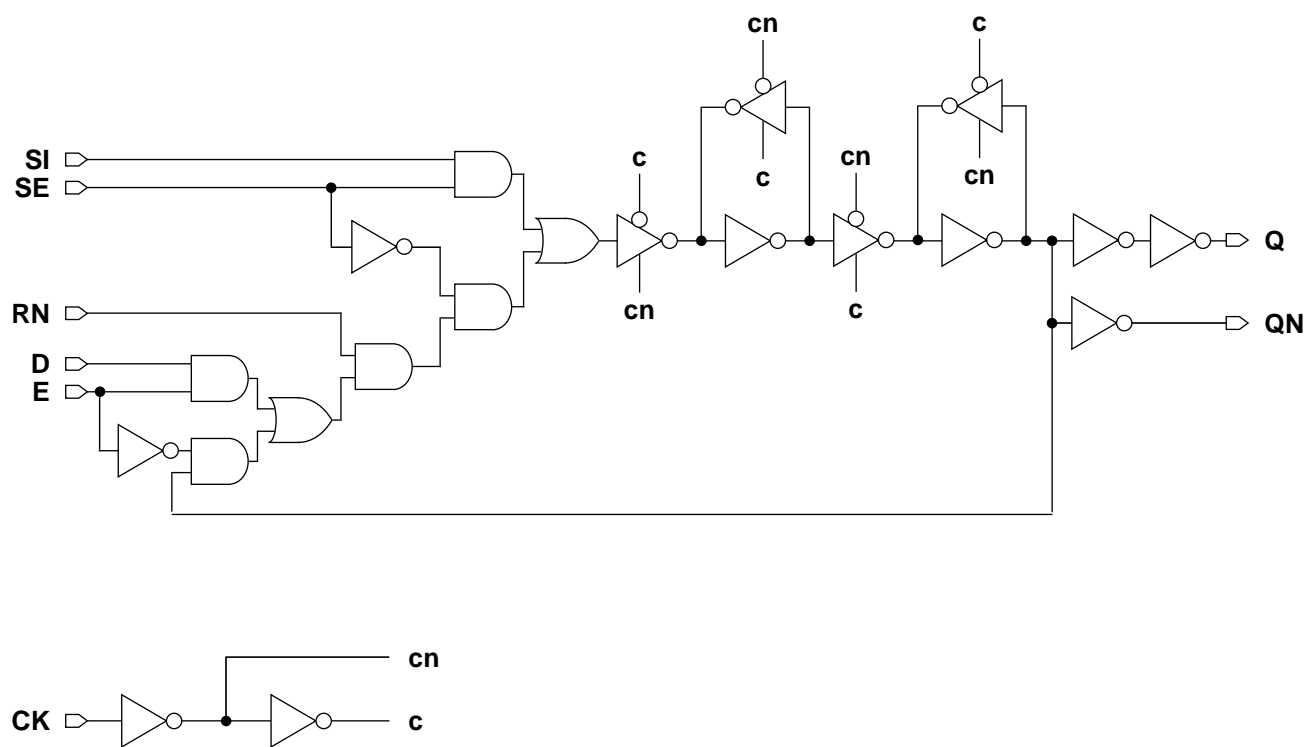
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
SI	0.0082	0.0085	0.0092	0.0120
SE	0.0110	0.0113	0.0120	0.0149
D	0.0102	0.0105	0.0112	0.0141
CK	0.0113	0.0117	0.0124	0.0163
E	0.0125	0.0128	0.0135	0.0163
RN	0.0079	0.0083	0.0089	0.0116
Q	0.0060	0.0069	0.0090	0.0149

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
SI	0.0011	0.0011	0.0011	0.0011
SE	0.0023	0.0023	0.0022	0.0023
D	0.0012	0.0012	0.0012	0.0012
CK	0.0015	0.0015	0.0016	0.0019
E	0.0013	0.0013	0.0012	0.0013
RN	0.0013	0.0013	0.0013	0.0013

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
CK	→ Q	↑	0.1988	0.1892	0.1789	0.1753	7.0166	4.5147	2.8998	1.4808
CK	→ Q	↓	0.1853	0.1848	0.1744	0.1801	5.2638	3.8799	1.6606	0.8273
CK	→ QN	↑	0.1277	0.1239	0.1212	0.1219	7.0774	4.5216	2.8926	1.4965
CK	→ QN	↓	0.1455	0.1431	0.1306	0.1225	6.0450	4.1820	1.7839	0.8759

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	X1	X2	X4
SI	setup	↑	→	CK	0.1484	0.1523	0.1641	0.1836
	setup	↓	→	CK	0.1953	0.1953	0.2031	0.2070
	hold	↑	→	CK	-0.0977	-0.0977	-0.0977	-0.1055
	hold	↓	→	CK	-0.1758	-0.1758	-0.1758	-0.1797
SE	setup	↑	→	CK	0.2148	0.2188	0.2227	0.2344
	setup	↓	→	CK	0.2422	0.2422	0.2500	0.2539
	hold	↑	→	CK	-0.1484	-0.1484	-0.1484	-0.1562
	hold	↓	→	CK	-0.1641	-0.1641	-0.1680	-0.1719
D	setup	↑	→	CK	0.2031	0.2070	0.2188	0.2422
	setup	↓	→	CK	0.2422	0.2461	0.2500	0.2578
	hold	↑	→	CK	-0.1523	-0.1523	-0.1523	-0.1602
	hold	↓	→	CK	-0.2227	-0.2227	-0.2266	-0.2305
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332
E	setup	↑	→	CK	0.2734	0.2734	0.2812	0.2891
	setup	↓	→	CK	0.2578	0.2539	0.2461	0.2422
	hold	↑	→	CK	-0.2070	-0.2070	-0.2070	-0.2148
	hold	↓	→	CK	-0.1172	-0.1172	-0.1367	-0.1758
RN	setup	↑	→	CK	0.1250	0.1289	0.1445	0.1641
	setup	↓	→	CK	0.1523	0.1523	0.1562	0.1602
	hold	↑	→	CK	-0.0742	-0.0742	-0.0781	-0.0820
	hold	↓	→	CK	-0.1328	-0.1328	-0.1328	-0.1367

Cell Description

The SMDFFHQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with a 2to1data select control (S0) for the data inputs (D1,D0), scan input (SI), and activehigh scan enable (SE). The cell has a single output (Q) and fast clocktoout path.

Logic Symbol
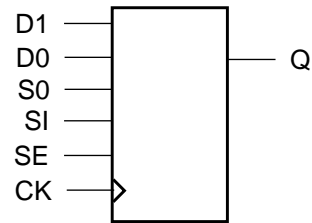
Function Table

SE	SI	S0	D1	D0	CK	Q[n+1]
0	x	0	x	0	⌐	0
0	x	0	x	1	⌐	1
0	x	1	0	x	⌐	0
0	x	1	1	x	⌐	1
1	0	x	x	x	⌐	0
1	1	x	x	x	⌐	1
x	x	x	x	x	⌐	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
SMDFFHQX1ADTH	2.52	11.20
SMDFFHQX2ADTH	2.52	12.04
SMDFFHQX4ADTH	2.52	14.00
SMDFFHQX8ADTH	2.52	20.44

Functional Schematic
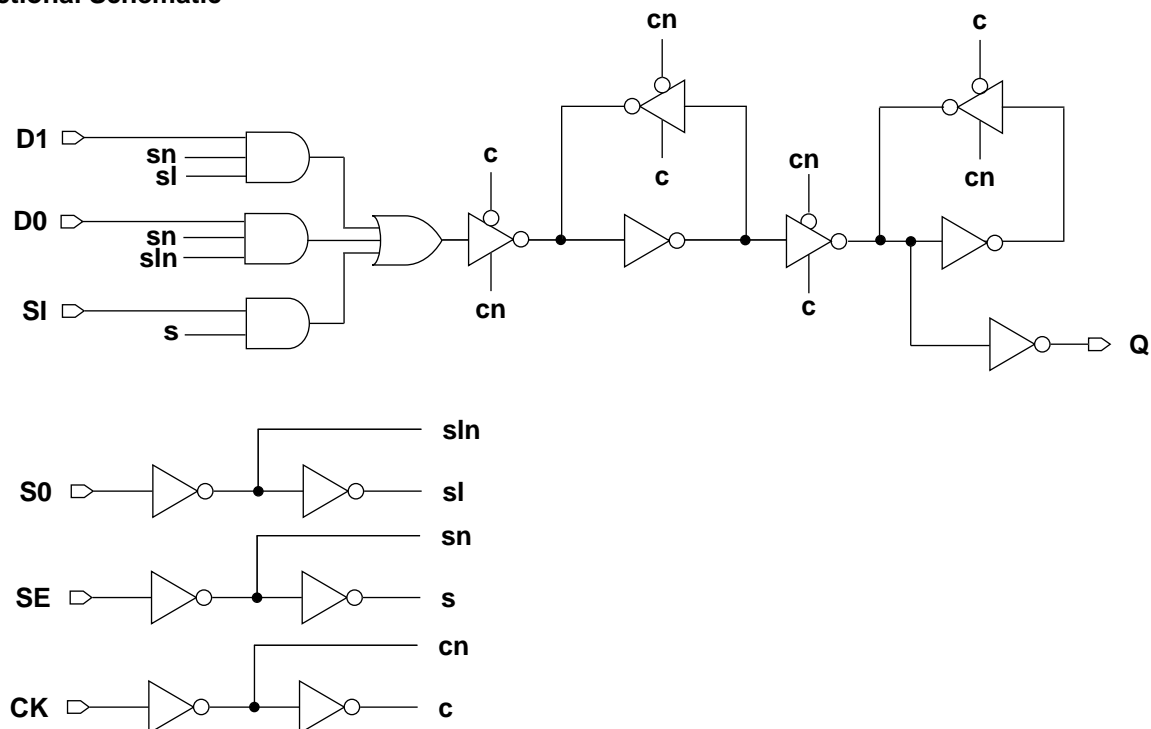
AC Power

Pin	Power (uW/MHz)			
	X1	**X2**	**X4**	**X8**
SI	0.0074	0.0094	0.0145	0.0245
SE	0.0125	0.0149	0.0203	0.0349
D0	0.0076	0.0100	0.0157	0.0270
D1	0.0075	0.0099	0.0156	0.0273
S0	0.0127	0.0151	0.0207	0.0318
CK	0.0128	0.0161	0.0246	0.0400
Q	0.0038	0.0052	0.0077	0.0133

Pin Capacitance

Pin	Capacitance (pF)			
	X1	**X2**	**X4**	**X8**
SI	0.0011	0.0011	0.0013	0.0021
SE	0.0033	0.0034	0.0033	0.0036
D0	0.0012	0.0016	0.0024	0.0045
D1	0.0014	0.0016	0.0025	0.0044
S0	0.0025	0.0026	0.0026	0.0028
CK	0.0022	0.0022	0.0032	0.0052

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			X1	**X2**	**X4**	**X8**	**X1**	**X2**	**X4**	**X8**
CK	→ Q	↑	0.1048	0.1008	0.0920	0.0835	4.4769	2.8500	1.4488	0.7417
CK	→ Q	↓	0.1190	0.1122	0.1005	0.0885	4.0312	1.7274	0.8332	0.4098

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					X1	X2	X4	X8
SI	setup	↑	→	CK	0.1367	0.1328	0.1289	0.1172
	setup	↓	→	CK	0.1953	0.2148	0.1992	0.2031
	hold	↑	→	CK	-0.0781	-0.0820	-0.0742	-0.0586
	hold	↓	→	CK	-0.1484	-0.1602	-0.1445	-0.1445
SE	setup	↑	→	CK	0.2148	0.2305	0.2148	0.2344
	setup	↓	→	CK	0.2305	0.2070	0.1992	0.2188
	hold	↑	→	CK	-0.0820	-0.0859	-0.0859	-0.0781
	hold	↓	→	CK	-0.1406	-0.1250	-0.1094	-0.1172
D0	setup	↑	→	CK	0.1328	0.1055	0.0859	0.0859
	setup	↓	→	CK	0.1562	0.1211	0.0977	0.1133
	hold	↑	→	CK	-0.0781	-0.0547	-0.0391	-0.0312
	hold	↓	→	CK	-0.1055	-0.0742	-0.0547	-0.0664
D1	setup	↑	→	CK	0.1328	0.1055	0.0898	0.0859
	setup	↓	→	CK	0.1602	0.1250	0.1016	0.1172
	hold	↑	→	CK	-0.0781	-0.0547	-0.0391	-0.0312
	hold	↓	→	CK	-0.1133	-0.0781	-0.0586	-0.0664
S0	setup	↑	→	CK	0.1875	0.1602	0.1523	0.1562
	setup	↓	→	CK	0.2148	0.1836	0.1719	0.1992
	hold	↑	→	CK	-0.1289	-0.1094	-0.0977	-0.0977
	hold	↓	→	CK	-0.1328	-0.1133	-0.1055	-0.1094
CK	minpwh				0.8332	0.8332	0.8332	0.8332
	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The TBUF cell provides the logical buffer of a single input (A) with an active-high output enable (OE). When the enable is high, the output (Y) is represented by the logic equation:

$Y = A$

Logic Symbol

A ▷— Y
OE
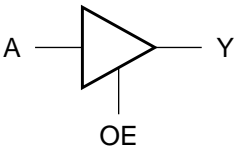
Function Table

OE	A	Y
0	x	Z
1	0	0
1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
TBUFXLADTH	2.52	2.52
TBUFX1ADTH	2.52	2.52
TBUFX2ADTH	2.52	2.80
TBUFX3ADTH	2.52	3.08
TBUFX4ADTH	2.52	3.08
TBUFX6ADTH	2.52	3.92
TBUFX8ADTH	2.52	4.48
TBUFX12ADTH	2.52	5.88
TBUFX16ADTH	2.52	6.72
TBUFX20ADTH	2.52	8.40

Functional Schematic

A ▷——▷ Y
OE ▷
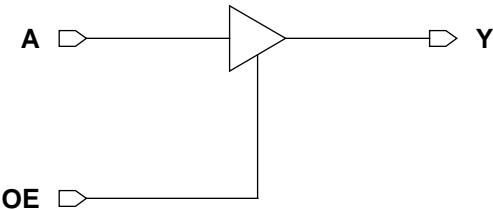
AC Power

Pin	Power (uW/MHz)							
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**
A	0.0041	0.0044	0.0057	0.0072	0.0083	0.0121	0.0154	0.0226
OE	0.0028	0.0031	0.0044	0.0054	0.0061	0.0090	0.0113	0.0171

AC Power (Cont'd.)

Pin	Power (uW/MHz)	
	X16	**X20**
A	0.0291	0.0374
OE	0.0218	0.0289

Pin Capacitance

Pin	Capacitance (pF)							
	XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**
A	0.0013	0.0013	0.0015	0.0017	0.0021	0.0035	0.0044	0.0064
OE	0.0022	0.0022	0.0024	0.0027	0.0026	0.0026	0.0034	0.0041
Y	0.0010	0.0013	0.0017	0.0024	0.0029	0.0045	0.0057	0.0089

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)	
	X16	**X20**
A	0.0081	0.0098
OE	0.0048	0.0060
Y	0.0116	0.0149

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)							
			XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**
A	→ Y	↑	0.0692	0.0721	0.0694	0.0639	0.0668	0.0630	0.0608	0.0585
A	→ Y	↓	0.1250	0.1306	0.1070	0.1017	0.0939	0.0874	0.0841	0.0862
OE	→ Y	↑	0.0461	0.0490	0.0452	0.0468	0.0495	0.0506	0.0498	0.0478
OE	→ Y	↓	0.0874	0.0907	0.0830	0.0785	0.0761	0.0757	0.0694	0.0737

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description				Intrinsic Delay (ns)	
				X16	**X20**
A	→	Y	↑	0.0606	0.0620
A	→	Y	↓	0.0851	0.0877
OE	→	Y	↑	0.0500	0.0504
OE	→	Y	↓	0.0709	0.0759

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)							
				XL	**X1**	**X2**	**X3**	**X4**	**X6**	**X8**	**X12**
A	→	Y	↑	7.0307	4.6239	3.1499	1.9703	1.6385	1.0893	0.8335	0.5561
A	→	Y	↓	6.2581	4.2351	1.9644	1.1983	0.9566	0.6269	0.4653	0.3109
OE	→	Y	↑	7.0245	4.6159	3.1470	1.9705	1.6392	1.0899	0.8336	0.5563
OE	→	Y	↓	6.1960	4.1953	1.9533	1.1905	0.9529	0.6248	0.4638	0.3096

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description				K_{load} (ns/pF)	
				X16	**X20**
A	→	Y	↑	0.4256	0.3389
A	→	Y	↓	0.2320	0.1764
OE	→	Y	↑	0.4255	0.3390
OE	→	Y	↓	0.2311	0.1757

Cell Description

The TIEHI cell drives the output (Y) to a logic high. The output is driven through diffusion and not tied directly to the power rail to provide some ESD protection. The output (Y) is represented by the logic equation:

$Y = 1$

Logic Symbol

Y
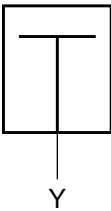
Function Table

Y
1

Cell Size

Drive Strength	Height (um)	Width (um)
TIEHIADTH	2.52	0.84

Functional Schematic

Y

Cell Description

The TIELO cell drives the output (Y) to a logic low. The output is driven through diffusion and not tied directly to the power rail to provide some ESD protection. The output (Y) is represented by the logic equation:
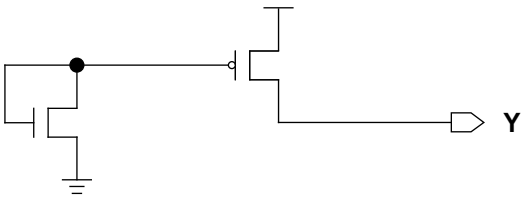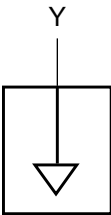
$Y = 0$

Logic Symbol

Y

Function Table

Y
0

Cell Size

Drive Strength	Height (um)	Width (um)
TIELOADTH	2.52	0.84

Functional Schematic

Y
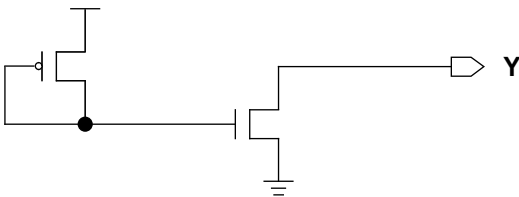
Cell Description

The TLAT cell is an active-high D-type transparent latch. When the enable (G) is high, data is transferred to the outputs (Q,QN).

Logic Symbol
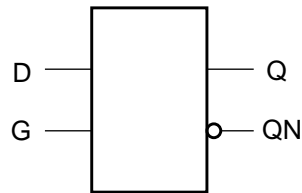
Function Table

G	D	Q[n+1]	QN[n+1]
1	0	0	1
1	1	1	0
0	x	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
TLATXLADTH	2.52	3.64
TLATX1ADTH	2.52	3.64
TLATX2ADTH	2.52	3.92
TLATX4ADTH	2.52	5.60

Functional Schematic
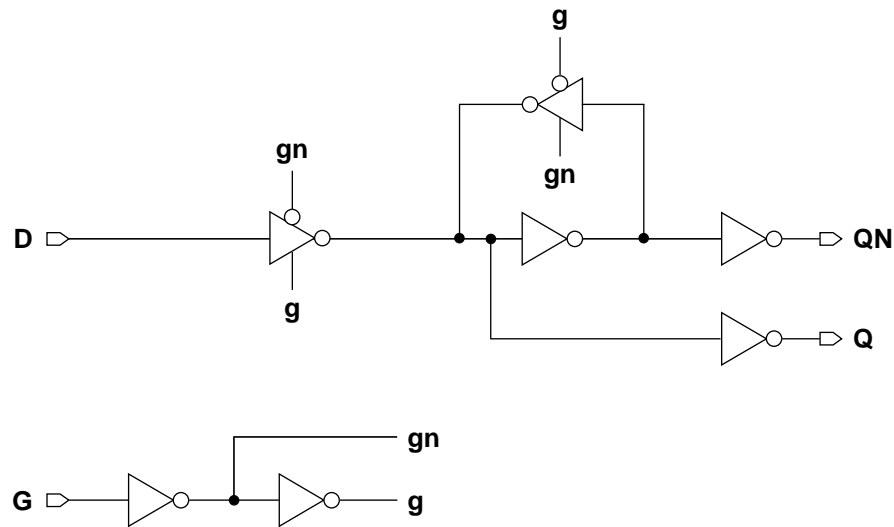
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0009	0.0010	0.0012	0.0025
G	0.0041	0.0041	0.0042	0.0057
Q	0.0051	0.0059	0.0079	0.0137

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0016	0.0018	0.0023	0.0045
G	0.0012	0.0012	0.0015	0.0021

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
D	→	Q	↑	0.0592	0.0563	0.0527	0.0537	7.0196	4.6539	2.8863	1.5005
D	→	Q	↓	0.0978	0.0927	0.0885	0.0861	6.1617	4.0717	1.7904	0.8825
G	→	Q	↑	0.1294	0.1282	0.1186	0.1154	7.0161	4.6532	2.8857	1.5002
G	→	Q	↓	0.1135	0.1098	0.0965	0.0901	6.1746	4.0810	1.7948	0.8846
D	→	QN	↑	0.1397	0.1348	0.1359	0.1327	6.9582	4.4872	2.8832	1.4789
D	→	QN	↓	0.1096	0.1145	0.1135	0.1094	5.5668	3.8633	1.7392	0.8400
G	→	QN	↑	0.1558	0.1525	0.1443	0.1372	6.9622	4.4895	2.8836	1.4789
G	→	QN	↓	0.1802	0.1868	0.1798	0.1713	5.5706	3.8641	1.7396	0.8401

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	G	-0.0117	-0.0156	-0.0078	-0.0039
	setup	↓	→	G	0.0664	0.0586	0.0586	0.0586
	hold	↑	→	G	0.0195	0.0234	0.0195	0.0156
	hold	↓	→	G	-0.0586	-0.0547	-0.0547	-0.0547
G	minpwh				0.8332	0.8332	0.8332	0.8332

## Cell Description

The TLATN cell is an active-low D-type
transparent latch. When the enable (GN) is low,
data is transferred to the outputs (Q,QN).

Logic Symbol
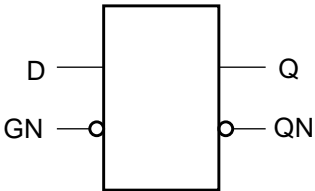
Function Table

GN	D	Q[n+1]	QN[n+1]
0	0	0	1
0	1	1	0
1	x	Q[n]	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
TLATNXLADTH	2.52	3.92
TLATNX1ADTH	2.52	3.92
TLATNX2ADTH	2.52	3.92
TLATNX4ADTH	2.52	5.60

Functional Schematic
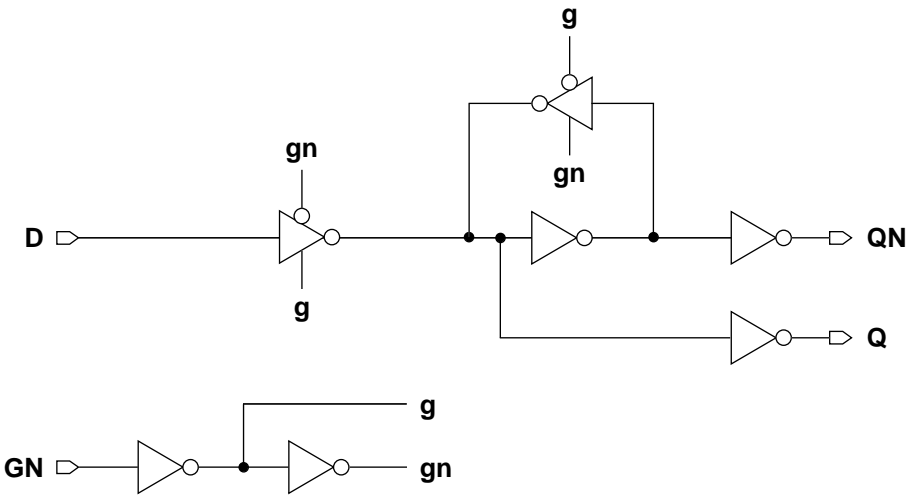
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0008	0.0010	0.0013	0.0026
GN	0.0043	0.0046	0.0049	0.0081
Q	0.0051	0.0060	0.0082	0.0141

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0015	0.0018	0.0023	0.0047
GN	0.0015	0.0015	0.0015	0.0021

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
D	→	Q	↑	0.0566	0.0548	0.0556	0.0505	7.0380	4.5122	2.8938	1.4967
D	→	Q	↓	0.0943	0.0911	0.0862	0.0857	6.0781	4.0187	1.7867	0.8802
GN	→	Q	↑	0.0910	0.0897	0.0925	0.0803	7.0620	4.5243	2.8989	1.4990
GN	→	Q	↓	0.1495	0.1479	0.1452	0.1313	6.0747	4.0175	1.7863	0.8800
D	→	QN	↑	0.1327	0.1289	0.1339	0.1326	6.9530	4.4843	2.8826	1.4782
D	→	QN	↓	0.1074	0.1130	0.1175	0.1063	5.5699	3.8654	1.7386	0.8404
GN	→	QN	↑	0.1880	0.1859	0.1930	0.1782	6.9558	4.4862	2.8831	1.4784
GN	→	QN	↓	0.1435	0.1499	0.1562	0.1373	5.5741	3.8667	1.7392	0.8408

Timing Constraints at 25°C, 1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	**X1**	**X2**	**X4**
D	setup	↑	→	GN	0.0352	0.0352	0.0352	0.0352
	setup	↓	→	GN	0.0469	0.0430	0.0352	0.0391
	hold	↑	→	GN	-0.0312	-0.0312	-0.0312	-0.0273
	hold	↓	→	GN	-0.0352	-0.0273	-0.0234	-0.0273
GN	minpwl				0.8332	0.8332	0.8332	0.8332

Cell Description

The TLATNCA cell is a positive-edge triggered clock-gating latch. The positive-edge clock (CK) is qualified by the latched enable signal (E) to create the gated positive-edge clock (ECK).

Logic Symbol
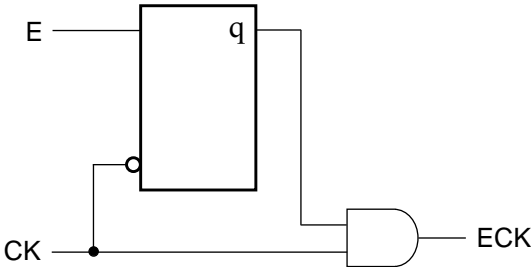
Function Table

CK	E	q[n+1]	ECK[n+1]
1	x	q[n]	q[n]
0	0	0	0
0	1	1	0

- Note: q is an internal node, and is not accessible.

Cell Size

Drive Strength	Height (um)	Width (um)
TLATNCAX2ADTH	2.52	3.64
TLATNCAX3ADTH	2.52	4.20
TLATNCAX4ADTH	2.52	5.60
TLATNCAX6ADTH	2.52	6.44
TLATNCAX8ADTH	2.52	7.56
TLATNCAX12ADTH	2.52	10.08
TLATNCAX16ADTH	2.52	12.60
TLATNCAX20ADTH	2.52	15.68

Functional Schematic
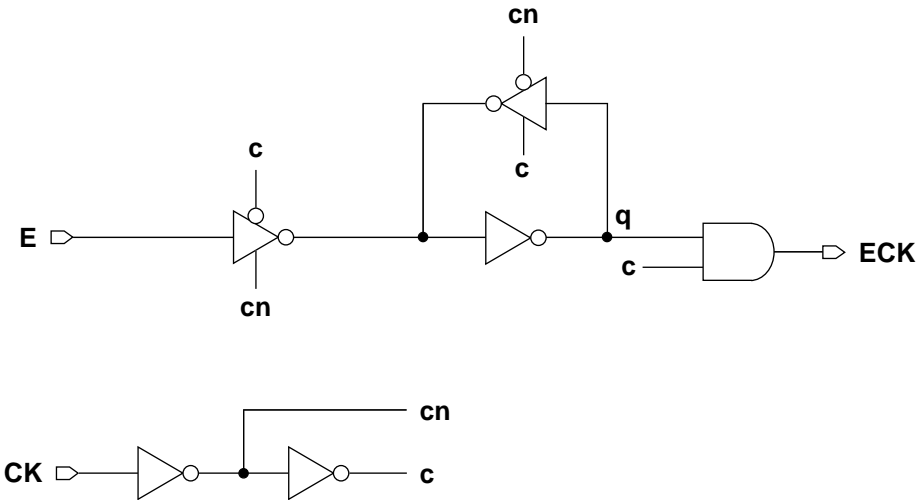
AC Power

Pin	Power (uW/MHz)							
	X2	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**	**X20**
E	0.0059	0.0072	0.0094	0.0118	0.0149	0.0207	0.0254	0.0321
CK	0.0061	0.0070	0.0088	0.0113	0.0143	0.0222	0.0271	0.0345
ECK	0.0064	0.0082	0.0099	0.0135	0.0168	0.0241	0.0311	0.0382

Pin Capacitance

Pin	Capacitance (pF)							
	X2	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**	**X20**
E	0.0021	0.0023	0.0041	0.0050	0.0068	0.0094	0.0114	0.0152
CK	0.0020	0.0024	0.0026	0.0040	0.0049	0.0074	0.0097	0.0121

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X2	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**	**X20**
CK → ECK ↑	0.0521	0.0562	0.0548	0.0550	0.0542	0.0610	0.0615	0.0637
CK → ECK ↓	0.0703	0.0714	0.0719	0.0655	0.0658	0.0679	0.0656	0.0669

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X2	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**	**X20**
CK → ECK ↑	5.9982	4.0822	3.0887	2.1021	1.5938	1.0971	0.8378	0.6824
CK → ECK ↓	4.4131	2.9137	2.2266	1.4379	1.0768	0.7188	0.5384	0.4237

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)							
		X2	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**	**X20**
E	setup ↑ → CK	0.0430	0.0469	0.0391	0.0352	0.0352	0.0312	0.0352	0.0352
	setup ↓ → CK	0.0156	0.0234	0.0078	0.0117	0.0117	0.0078	0.0117	0.0078
	hold ↑ → CK	-0.0234	-0.0273	-0.0234	-0.0234	-0.0234	-0.0234	-0.0234	-0.0234
	hold ↓ → CK	0.0352	0.0312	0.0352	0.0312	0.0273	0.0312	0.0273	0.0273
CK	minpwl	0.8332	0.8332	0.8332	0.8332	0.8332	0.8332	0.8332	0.8332

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Cell Description

The TLATNSR cell is an active-low D-type transparent latch with asynchronous active-low set (SN) and reset (RN), and set dominating reset. When the enable (GN) is low, data is transferred to the outputs (Q,QN).

Logic Symbol
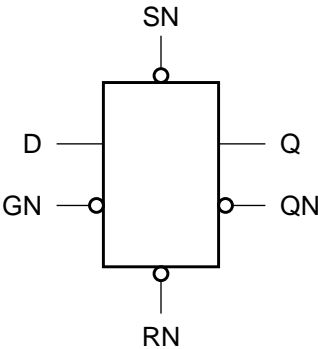
Function Table

RN	SN	GN	D	Q[n+1]	QN[n+1]
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	x	Q[n]	QN[n]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
TLATNSRXLADTH	2.52	5.60
TLATNSRX1ADTH	2.52	5.88
TLATNSRX2ADTH	2.52	6.16
TLATNSRX4ADTH	2.52	8.96

Functional Schematic
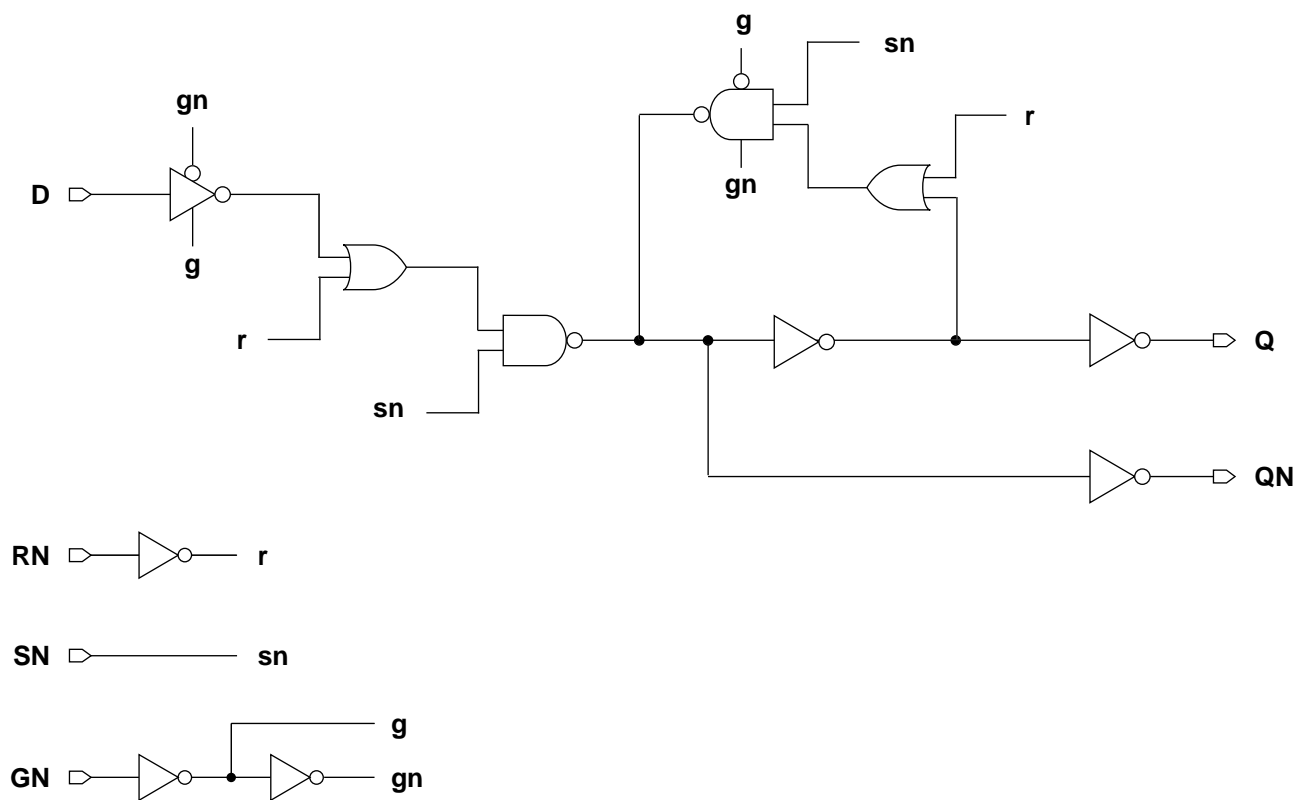
AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
D	0.0010	0.0013	0.0017	0.0033
GN	0.0050	0.0054	0.0060	0.0091
SN	0.0027	0.0033	0.0038	0.0064
RN	0.0007	0.0010	0.0012	0.0024
Q	0.0080	0.0095	0.0119	0.0193

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
D	0.0015	0.0020	0.0024	0.0047
GN	0.0014	0.0014	0.0014	0.0019
SN	0.0012	0.0015	0.0017	0.0027
RN	0.0018	0.0023	0.0026	0.0048

Delays at 25°C,1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
D	→	Q	↑	0.1176	0.1059	0.1051	0.0964	7.5234	4.7359	3.0025	1.5317
D	→	Q	↓	0.2031	0.1877	0.1762	0.1720	8.0219	4.6990	2.1255	1.0518
GN	→	Q	↑	0.1256	0.1189	0.1196	0.1181	7.5148	4.7351	3.0057	1.5328
GN	→	Q	↓	0.2567	0.2267	0.2218	0.2112	8.0184	4.6978	2.1251	1.0514
SN	→	Q	↑	0.1394	0.1248	0.1213	0.1110	7.2466	4.6394	2.9632	1.5144
SN	→	Q	↓	0.2327	0.2107	0.1965	0.1887	7.9289	4.6561	2.1022	1.0381
RN	→	Q	↑	0.1142	0.1025	0.1017	0.0920	7.5238	4.7359	3.0025	1.5317
RN	→	Q	↓	0.1797	0.1596	0.1488	0.1317	8.6917	4.9793	2.2792	1.0949
D	→	QN	↑	0.2635	0.2335	0.2371	0.2343	7.0966	4.5352	2.9175	1.4910
D	→	QN	↓	0.1650	0.1435	0.1714	0.1547	5.7268	3.6660	1.6920	0.8240
GN	→	QN	↑	0.3174	0.2728	0.2829	0.2736	7.1008	4.5366	2.9181	1.4909
GN	→	QN	↓	0.1734	0.1567	0.1867	0.1769	5.7297	3.6667	1.6935	0.8245
SN	→	QN	↑	0.2918	0.2557	0.2562	0.2494	7.0887	4.5325	2.9168	1.4907
SN	→	QN	↓	0.1850	0.1616	0.1862	0.1680	5.6973	3.6581	1.6871	0.8223
RN	→	QN	↑	0.2427	0.2059	0.2117	0.1933	7.1497	4.5497	2.9247	1.4928
RN	→	QN	↓	0.1616	0.1400	0.1681	0.1503	5.7270	3.6660	1.6921	0.8241

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	X1	X2	X4
D	setup	↑	→	GN	0.0977	0.0859	0.0898	0.0781
	setup	↓	→	GN	0.1484	0.1211	0.1094	0.1094
	hold	↑	→	GN	-0.0938	-0.0781	-0.0820	-0.0664
	hold	↓	→	GN	-0.1211	-0.0977	-0.0898	-0.0938
GN	minpwl				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.1758	0.1406	0.1250	0.1250
	removal				-0.1719	-0.1367	-0.1211	-0.1211
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.0977	0.0781	0.0859	0.0703
	removal				-0.0938	-0.0742	-0.0820	-0.0664

Cell Description

The TLATNTSCA cell is a positive-edge triggered clock-gating latch. The positive-edge clock (CK) is qualified by the latched enable signals (SE) and (E) to create the gated positive-edge clock (ECK).

Logic Symbol
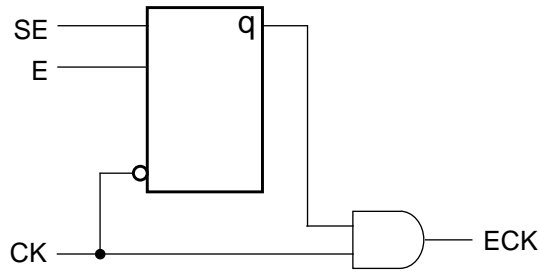
Function Table

CK	SE	E	q[n+1]	ECK[n+1]
1	x	x	q[n]	q[n]
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0

- Note: q is an internal node and is not accessible.

Cell Size

Drive Strength	Height (um)	Width (um)
TLATNTSCAX2ADTH	2.52	5.04
TLATNTSCAX3ADTH	2.52	5.60
TLATNTSCAX4ADTH	2.52	6.44
TLATNTSCAX6ADTH	2.52	8.40
TLATNTSCAX8ADTH	2.52	9.52
TLATNTSCAX12ADTH	2.52	11.48
TLATNTSCAX16ADTH	2.52	13.16
TLATNTSCAX20ADTH	2.52	16.24

Functional Schematic
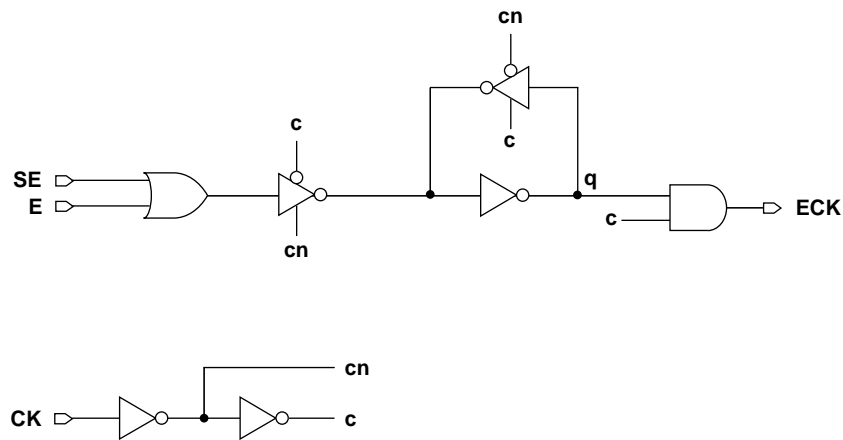
AC Power

Pin	Power (uW/MHz)							
	X2	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**	**X20**
E	0.0093	0.0100	0.0127	0.0161	0.0197	0.0257	0.0293	0.0347
SE	0.0097	0.0103	0.0129	0.0164	0.0201	0.0262	0.0301	0.0355
CK	0.0065	0.0072	0.0089	0.0124	0.0153	0.0214	0.0255	0.0308
ECK	0.0066	0.0080	0.0098	0.0142	0.0174	0.0217	0.0280	0.0321

Pin Capacitance

Pin	Capacitance (pF)							
	X2	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**	**X20**
E	0.0013	0.0014	0.0015	0.0014	0.0016	0.0020	0.0024	0.0027
SE	0.0014	0.0012	0.0014	0.0012	0.0014	0.0018	0.0024	0.0026
CK	0.0021	0.0024	0.0027	0.0040	0.0051	0.0074	0.0097	0.0120

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)							
			X2	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**	**X20**
CK	→ ECK	↑	0.0563	0.0569	0.0568	0.0573	0.0574	0.0600	0.0613	0.0634
CK	→ ECK	↓	0.0737	0.0719	0.0728	0.0678	0.0670	0.0614	0.0612	0.0592

Delays at 25°C, 1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)							
			X2	**X3**	**X4**	**X6**	**X8**	**X12**	**X16**	**X20**
CK	→ ECK	↑	6.0192	4.1087	3.1014	2.1112	1.6032	1.2974	0.9375	0.8261
CK	→ ECK	↓	4.5592	2.8930	2.2077	1.3513	1.0817	0.7109	0.5296	0.4234

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)							
					X2	X3	X4	X6	X8	X12	X16	X20
E	setup	↑	→	CK	0.1211	0.1094	0.1016	0.1055	0.1016	0.1016	0.0938	0.0938
	setup	↓	→	CK	0.1172	0.1172	0.1172	0.1211	0.1133	0.0977	0.0977	0.1094
	hold	↑	→	CK	-0.0977	-0.0898	-0.0859	-0.0938	-0.0898	-0.0859	-0.0781	-0.0781
	hold	↓	→	CK	-0.0664	-0.0625	-0.0742	-0.0742	-0.0703	-0.0625	-0.0625	-0.0742
SE	setup	↑	→	CK	0.1250	0.1094	0.1016	0.1094	0.1055	0.1055	0.0977	0.0938
	setup	↓	→	CK	0.1250	0.1211	0.1211	0.1250	0.1172	0.1055	0.1055	0.1172
	hold	↑	→	CK	-0.1016	-0.0898	-0.0859	-0.0977	-0.0938	-0.0898	-0.0820	-0.0820
	hold	↓	→	CK	-0.0742	-0.0664	-0.0781	-0.0781	-0.0742	-0.0664	-0.0703	-0.0820
CK	minpwl				0.8332	0.8332	0.8332	0.8332	0.8332	0.8332	0.8332	0.8332

Cell Description

The TLATSR cell is an active-high D-type transparent latch with asynchronous active-low set (SN) and reset (RN), and set dominating reset. When the enable (G) is high, data is transferred to the outputs (Q,QN).
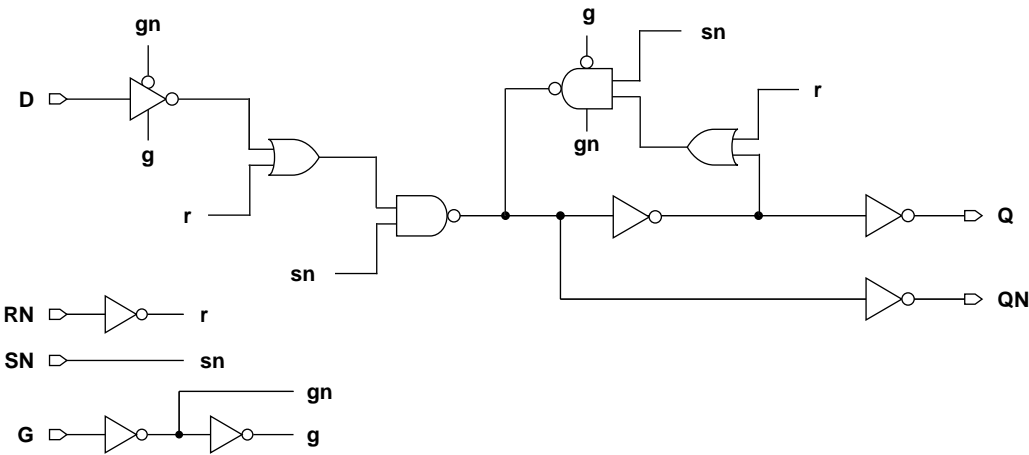
Logic Symbol
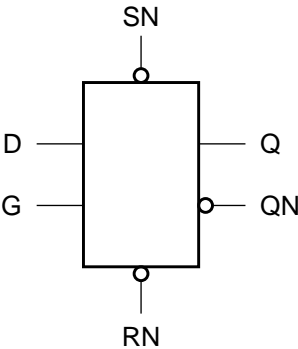
Function Table

RN	SN	G	D	Q[n+1]	QN[n+1]
1	1	1	0	0	1
1	1	1	1	1	0
1	1	0	x	Q[n]	QN[n]
0	1	x	x	0	1
1	0	x	x	1	0
0	0	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
TLATSRXLADTH	2.52	5.60
TLATSRX1ADTH	2.52	5.60
TLATSRX2ADTH	2.52	6.16
TLATSRX4ADTH	2.52	8.96

Functional Schematic

AC Power

Pin	Power (uW/MHz)			
	XL	X1	X2	X4
D	0.0009	0.0011	0.0014	0.0032
G	0.0045	0.0046	0.0048	0.0074
SN	0.0027	0.0029	0.0037	0.0061
RN	0.0007	0.0008	0.0012	0.0023
Q	0.0073	0.0083	0.0114	0.0184

Pin Capacitance

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	0.0014	0.0016	0.0022	0.0047
G	0.0014	0.0014	0.0014	0.0017
SN	0.0012	0.0013	0.0017	0.0027
RN	0.0017	0.0019	0.0026	0.0045

Delays at 25°C, 1.0V, Typical Process

Description				Intrinsic Delay (ns)				K_{load} (ns/pF)			
				XL	X1	X2	X4	XL	X1	X2	X4
D	→	Q	↑	0.1223	0.1129	0.1043	0.0971	7.6063	4.8835	2.9901	1.5329
D	→	Q	↓	0.2121	0.1994	0.2021	0.1713	8.1578	4.8768	2.2420	1.0452
G	→	Q	↑	0.1646	0.1581	0.1608	0.1519	7.5994	4.8800	2.9882	1.5318
G	→	Q	↓	0.2007	0.1864	0.1808	0.1463	8.1641	4.8807	2.2439	1.0482
SN	→	Q	↑	0.1392	0.1326	0.1173	0.1104	7.2287	4.7678	2.9493	1.5176
SN	→	Q	↓	0.2419	0.2248	0.2222	0.1880	8.0637	4.8370	2.2139	1.0330
RN	→	Q	↑	0.1189	0.1093	0.1014	0.0918	7.6069	4.8834	2.9902	1.5330
RN	→	Q	↓	0.1894	0.1841	0.1457	0.1446	8.8248	5.3312	2.2070	1.1528
D	→	QN	↑	0.2738	0.2572	0.2676	0.2332	7.0963	4.7041	2.9154	1.4908
D	→	QN	↓	0.1866	0.1834	0.1698	0.1552	5.7088	3.8078	1.6912	0.8255
G	→	QN	↑	0.2628	0.2447	0.2468	0.2088	7.1024	4.7065	2.9161	1.4911
G	→	QN	↓	0.2294	0.2291	0.2268	0.2103	5.7152	3.8104	1.6925	0.8259
SN	→	QN	↑	0.3023	0.2817	0.2864	0.2486	7.0887	4.7011	2.9146	1.4907
SN	→	QN	↓	0.1995	0.2007	0.1811	0.1673	5.6635	3.7950	1.6862	0.8239
RN	→	QN	↑	0.2536	0.2450	0.2077	0.2108	7.1481	4.7337	2.9152	1.4947
RN	→	QN	↓	0.1833	0.1799	0.1669	0.1500	5.7090	3.8079	1.6913	0.8255

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement				Interval (ns)			
					XL	X1	X2	X4
D	setup	↑	→	G	0.0664	0.0508	0.0312	0.0195
	setup	↓	→	G	0.1836	0.1641	0.1719	0.1406
	hold	↑	→	G	-0.0508	-0.0352	-0.0156	-0.0039
	hold	↓	→	G	-0.1719	-0.1523	-0.1602	-0.1328
G	minpwh				0.8332	0.8332	0.8332	0.8332
SN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.2109	0.1875	0.1914	0.1562
	removal				-0.2070	-0.1836	-0.1875	-0.1523
RN	minpwl				0.8332	0.8332	0.8332	0.8332
	recovery				0.0625	0.0469	0.0234	0.0039
	removal				-0.0586	-0.0430	-0.0195	0.0000

Cell Description

The XNOR2 cell provides a logical EXCLUSIVE NOR of two inputs (A,B). The output (Y) is represented by the logic equation:

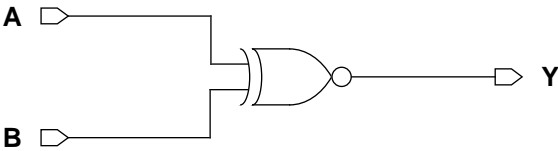$Y = (A \bullet B) + (\overline{A} \bullet \overline{B})$

Logic Symbol
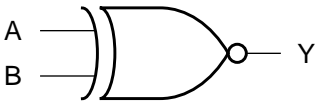
Function Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
XNOR2XLADTH	2.52	2.24
XNOR2X1ADTH	2.52	2.24
XNOR2X2ADTH	2.52	3.08
XNOR2X4ADTH	2.52	4.48

Functional Schematic

AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A	0.0029	0.0034	0.0057	0.0110
B	0.0038	0.0047	0.0093	0.0161

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A	0.0018	0.0019	0.0025	0.0037
B	0.0013	0.0017	0.0027	0.0051

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A	→ Y	↑	0.0369	0.0338	0.0355	0.0358	11.4024	8.2071	4.3009	2.1974
A	→ Y	↓	0.0418	0.0430	0.0477	0.0459	7.8157	5.9271	2.5394	1.2675
B	→ Y	↑	0.0667	0.0589	0.0627	0.0551	11.3495	8.0302	4.4162	2.1694
B	→ Y	↓	0.0687	0.0615	0.0632	0.0561	8.3409	6.1886	2.7699	1.3413

Cell Description

The XNOR3 cell provides a logical EXCLUSIVE
NOR of three inputs (A,B,C). The output (Y) is
represented by the following equation:

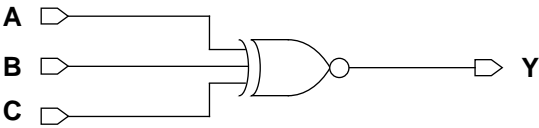$$Y = \overline{A \oplus B \oplus C}$$

Logic Symbol
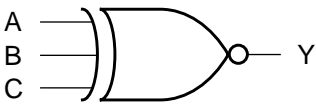
Function Table

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
XNOR3XLADTH	2.52	4.76
XNOR3X1ADTH	2.52	5.32
XNOR3X2ADTH	2.52	5.32
XNOR3X4ADTH	2.52	6.16

Functional Schematic

AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A	0.0111	0.0141	0.0175	0.0227
B	0.0100	0.0118	0.0148	0.0190
C	0.0048	0.0056	0.0079	0.0103

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A	0.0019	0.0023	0.0026	0.0026
B	0.0020	0.0022	0.0024	0.0024
C	0.0018	0.0018	0.0022	0.0023

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A	→ Y	↑	0.1756	0.1594	0.1540	0.1667	7.0336	4.4714	2.8560	1.5072
A	→ Y	↓	0.2002	0.1842	0.1697	0.2073	6.3021	4.0817	1.9755	1.0412
B	→ Y	↑	0.1490	0.1395	0.1366	0.1593	7.0280	4.4909	2.9153	1.5083
B	→ Y	↓	0.2006	0.1859	0.1640	0.1902	6.3025	4.0819	1.7947	1.0416
C	→ Y	↑	0.0836	0.0875	0.0899	0.1002	7.0897	4.5253	2.9022	1.5009
C	→ Y	↓	0.0958	0.0864	0.0770	0.0888	6.2965	4.0781	1.8246	1.0146

Cell Description

The XOR2 cell provides a logical EXCLUSIVE OR of two inputs (A,B). The output (Y) is represented by the logic equation:

$$Y = (A \bullet \overline{B}) + (\overline{A} \bullet B)$$

Logic Symbol

Function Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0
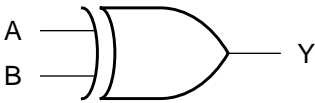
Cell Size

Drive Strength	Height (um)	Width (um)
XOR2XLADTH	2.52	2.24
XOR2X1ADTH	2.52	2.24
XOR2X2ADTH	2.52	2.80
XOR2X3ADTH	2.52	4.48
XOR2X4ADTH	2.52	4.48
XOR2X8ADTH	2.52	7.84

Functional Schematic
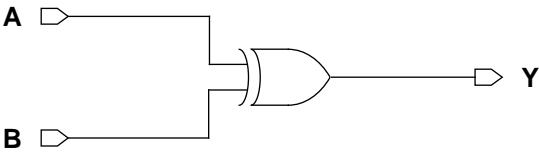
AC Power

Pin	Power (uW/MHz)					
	XL	**X1**	**X2**	**X3**	**X4**	**X8**
A	0.0029	0.0035	0.0058	0.0087	0.0105	0.0198
B	0.0041	0.0051	0.0090	0.0140	0.0172	0.0340

Pin Capacitance

Pin	Capacitance (pF)					
	XL	**X1**	**X2**	**X3**	**X4**	**X8**
A	0.0018	0.0019	0.0024	0.0031	0.0037	0.0072
B	0.0013	0.0017	0.0026	0.0041	0.0052	0.0102

Delays at 25°C,1.0V, Typical Process

Description			Intrinsic Delay (ns)					
			XL	**X1**	**X2**	**X3**	**X4**	**X8**
A	→ Y	↑	0.0383	0.0343	0.0348	0.0365	0.0343	0.0335
A	→ Y	↓	0.0423	0.0430	0.0485	0.0474	0.0433	0.0421
B	→ Y	↑	0.0656	0.0575	0.0524	0.0534	0.0499	0.0498
B	→ Y	↓	0.0709	0.0620	0.0596	0.0612	0.0568	0.0565

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description			K_{load} (ns/pF)					
			XL	**X1**	**X2**	**X3**	**X4**	**X8**
A	→ Y	↑	11.2974	8.1338	4.5425	2.8578	2.1796	1.1069
A	→ Y	↓	7.8676	5.9803	2.6798	1.6757	1.2821	0.6335
B	→ Y	↑	11.1637	8.0323	4.4833	2.8883	2.1864	1.1119
B	→ Y	↓	8.2337	6.1935	2.8170	1.7652	1.3403	0.6607

Cell Description

The XOR3 cell provides a logical EXCLUSIVE OR of three inputs (A,B,C). The output (Y) is represented by the following equation:

$Y = A \oplus B \oplus C$

Logic Symbol
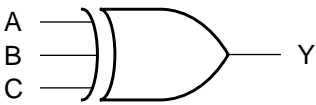
Function Table
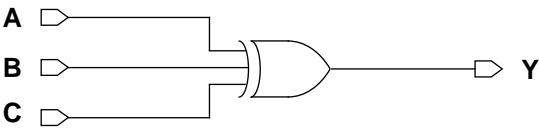
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
XOR3XLADTH	2.52	4.76
XOR3X1ADTH	2.52	5.32
XOR3X2ADTH	2.52	5.32
XOR3X4ADTH	2.52	6.16

Functional Schematic

AC Power

Pin	Power (uW/MHz)			
	XL	**X1**	**X2**	**X4**
A	0.0118	0.0145	0.0184	0.0237
B	0.0100	0.0117	0.0144	0.0190
C	0.0050	0.0059	0.0079	0.0101

Pin Capacitance

Pin	Capacitance (pF)			
	XL	**X1**	**X2**	**X4**
A	0.0019	0.0023	0.0026	0.0026
B	0.0021	0.0022	0.0025	0.0024
C	0.0028	0.0030	0.0037	0.0039

Delays at 25°C, 1.0V, Typical Process

Description			Intrinsic Delay (ns)				K_{load} (ns/pF)			
			XL	**X1**	**X2**	**X4**	**XL**	**X1**	**X2**	**X4**
A	→ Y	↑	0.1784	0.1622	0.1571	0.1674	7.0772	4.4801	2.8585	1.4981
A	→ Y	↓	0.1989	0.1837	0.1734	0.2097	6.3061	4.0978	1.9822	1.0420
B	→ Y	↑	0.1512	0.1428	0.1376	0.1580	7.0718	4.4796	2.9030	1.5091
B	→ Y	↓	0.2005	0.1862	0.1615	0.1922	6.3062	4.0980	1.8679	1.0422
C	→ Y	↑	0.0983	0.0953	0.0823	0.0831	7.0400	4.4693	2.8537	1.4536
C	→ Y	↓	0.0927	0.0831	0.0924	0.1096	6.2752	4.1432	1.9533	1.0299