1.3.1 Processors

The ‘‘brain’’ of the computer is the CPU. It fetches instructions from memoryand executes them. The basic cycle of every CPU is to fetch the first instructionfrom memory, decode it to determine its type and operands, execute it, and thenfetch, decode, and execute subsequent instructions. The cycle is repeated until theprogram finishes. In this way, programs are carried out.Each CPU has a specific set of instructions that it can execute

Because accessing memory to get an instruction or data word takes much longer than executing an instruction, all CPUs contain some registers insideto hold key variables and temporary results. Thus the instruction set generally con-tains instructions to load a word from memory into a register, and store a wordfrom a register into memory. Other instructions combine two operands from regis-ters, memory, or both into a result, such as adding two words and storing the resultin a register or in memory.In addition to the general registers used to hold variables and temporary re-sults, most computers have sev eral special registers that are visible to the pro-grammer. One of these is theprogram counter, which contains the memory ad-dress of the next instruction to be fetched. After that instruction has been fetched,the program counter is updated to point to its successor.Another register is thestack pointer, which points to the top of the currentstack in memory. The stack contains one frame for each procedure that has beenentered but not yet exited. A procedure’s stack frame holds those input parameters,local variables, and temporary variables that are not kept in registers.Yet another register is thePSW(Program Status Word). This register con-tains the condition code bits, which are set by comparison instructions, the CPUpriority, the mode (user or kernel), and various other control bits. User programsmay normally read the entire PSW but typically may write only some of its fields.The PSW plays an important role in system calls and I/O.The operating system must be fully aware of all the registers. When time mul-tiplexing the CPU, the operating system will often stop the running program to(re)start another one. Every time it stops a running program, the operating systemmust save all the registers so they can be restored when the program runs later.To improve performance, CPU designers have long abandoned the simplemodel of fetching, decoding, and executing one instruction at a time. Many modernCPUs have facilities for executing more than one instruction at the same time. Forexample, a CPU might have separate fetch, decode, and execute units, so that whileit is executing instructionn, it could also be decoding instructionn+1 and fetch-ing instructionn+2. Such an organization is called a pipeline and is illustrated.

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**Kernel perspective:**

[Memory segmentation](http://en.wikipedia.org/wiki/Memory_segmentation) is the old way of accessing memory regions. All major operating systems including OSX, Linux, (from version 0.1) and Windows (from NT) are now using [paging](http://en.wikipedia.org/wiki/Paging) which is a better way (IMHO) of accessing memory.

Before paging, the segment registers were used like this

**Let's see some examples (286-386 era) :**

The 286 architecture introduced 4 segments: **CS** (code segment) **DS** (data segment) SS (stack segment) **ES** (extra segment) the 386 architecture introduced two new general segment registers **FS**, **GS**.