

1-2 ON External 5V
2-3 ON USB 5V

The schematic diagram illustrates a 12-bit DAC using a resistor ladder network. The ladder is connected to a +3.3V supply and ground (GND). The output of the ladder is connected to a series of capacitors (C38 to C43) which are connected to a common output node. The capacitors are labeled C38, C39, C40, C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, and C43, all with a value of 0.1uF. The output node is connected to a 10uF capacitor (C43) which is connected to ground. The output of the DAC is taken from the node between C43 and ground.

The schematic diagram illustrates the pin configuration and power management for the STM32F103C8T6 microcontroller. The microcontroller is shown with its pins connected to various external components and power sources.

Power and Ground Connections:

- VDD:** Connected to a +3.3V supply.
- VSS:** Connected to GND.
- VDDA:** Connected to a +3.3V supply.
- VSSA:** Connected to GND.
- NC:** Not Connected.

Peripheral Connections:

- PA0-PA15:** General Purpose I/O pins.
- PB0-PB15:** General Purpose I/O pins.
- PC0-PC15:** General Purpose I/O pins.
- PF6-PF11:** General Purpose I/O pins.
- PG7-PG15:** General Purpose I/O pins.
- FSMC:** Flexible Static Memory Controller pins (FSMC_A0-FSMC_A25, FSMC_D0-FSMC_D15, FSMC_NOE, FSMC_NWE, FSMC_NWAIT, FSMC_NCE2, FSMC_NBL0, FSMC_NBL1, FSMC_INT2, FSMC_NE2, FSMC_NE3, FSMC_NE4).
- BOOT0:** Boot pin.
- VBAT:** Backup battery pin.
- OSC_IN/OSC_OUT:** Oscillator pins.
- NRST:** Reset pin.
- VREF+:** Reference voltage pin.
- VREF-:** Reference voltage pin.

Passive Components:

- Resistors:** R51 (10K), R28 (2K), R32 (1M).
- Capacitors:** C23 (15PF), C22 (15PF), C24 (100N).
- Crystal:** 32.768KHz.

Pin diagram of the FSMC_D[15:0] bus. The diagram shows a 16-bit data bus with pins 1 through 32. Pins 1-17 are on the left side, and pins 18-32 are on the right side. The pins are labeled FSMC_D0 through FSMC_D15 on the left and FSMC_D1 through FSMC_D15 on the right. A 3.3V supply is connected to pin 1, and a GND connection is shown near pin 2. The diagram is part of a larger schematic showing various peripheral connections to the FSMC.

The schematic diagram illustrates the JTAG interface for the AT91SAM7S256 microcontroller. The connections are as follows:

- Power Supply:**
 - +3.3V:** Connected to the TCK pin (PB4) and the TMS pin (PA15) via 10K pull-up resistors (R5 and R8).
 - +5V:** Connected to the TDI pin (PA13) and the TDO pin (PB3) via 10K pull-up resistors (R9 and R10).
- JTAG Pins:**
 - TCK (PB4):** Connected to pin 1 of the JTAG controller.
 - TMS (PA15):** Connected to pin 3 of the JTAG controller.
 - TDI (PA13):** Connected to pin 5 of the JTAG controller.
 - TDO (PB3):** Connected to pin 7 of the JTAG controller.
 - TRST:** Connected to pin 9 of the JTAG controller. The TRST pin is also connected to the RESET pin (PB3) via a 10K resistor (R7).
- Other Connections:**
 - RESET (PB3):** Connected to pin 11 of the JTAG controller.
 - NC (Not Connected):** Pins 13, 15, 17, and 19 of the JTAG controller are marked as NC.

The JTAG controller is represented by a block labeled JTAG with pins 1 through 20. The pins are connected to the microcontroller pins as follows:

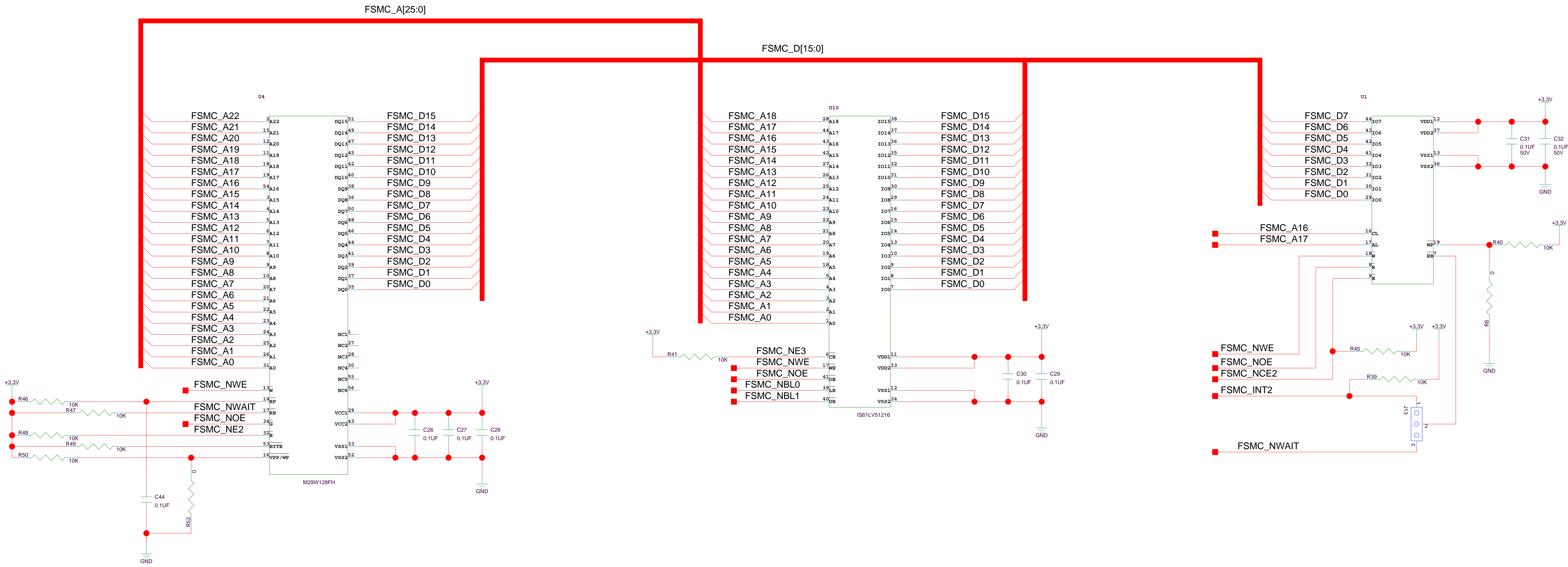
JTAG Pin	Microcontroller Pin
1	TCK (PB4)
3	TMS (PA15)
5	TDI (PA13)
7	TDO (PB3)
9	TRST (PB3)
11	RESET (PB3)
13	NC
15	NC
17	NC
19	NC

J9		J10		
1-2	2-3	1-2	2-3	
ON		ON		Boot from User Flash (Default Setting)
ON			ON	
ON				
	ON	ON		Boot from System Memory
	ON		ON	Boot from Embedded SRAM

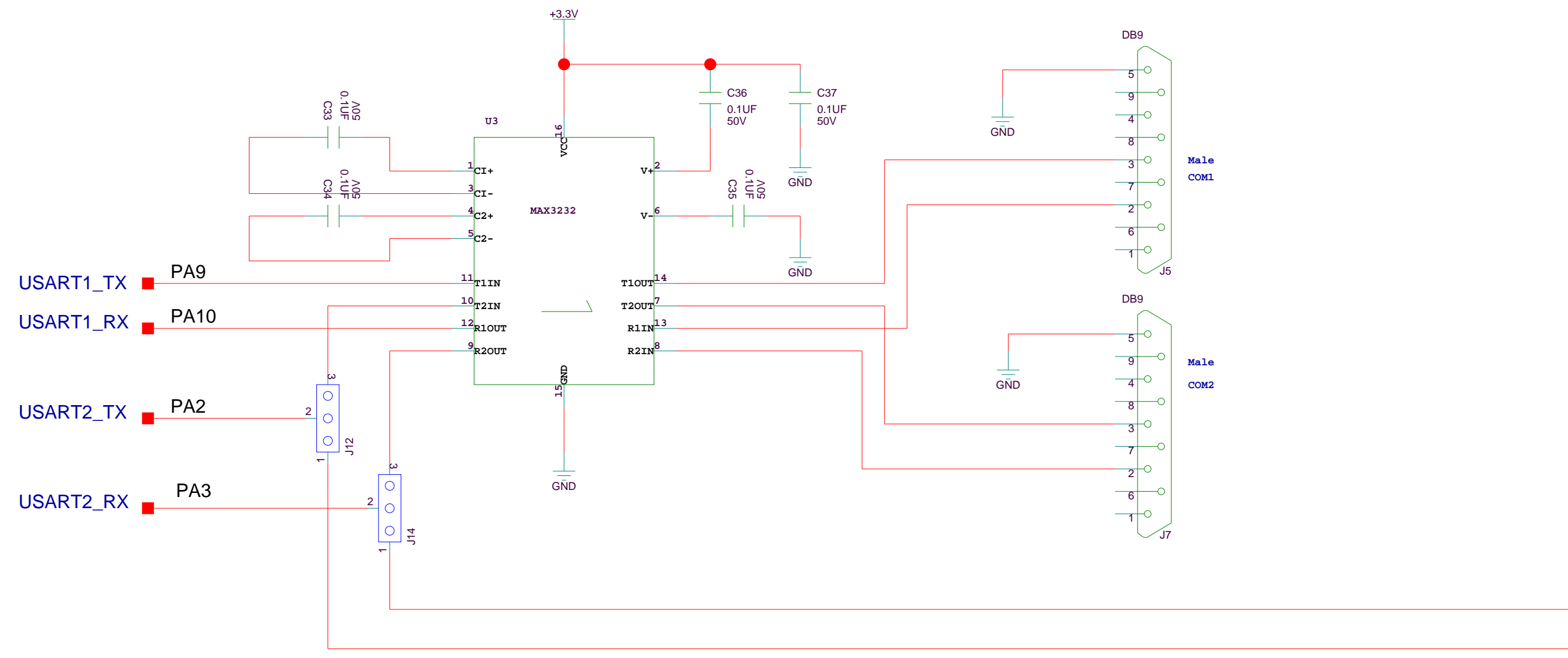
PROJECT NAME

SHEET 1 OF 6 REV V??

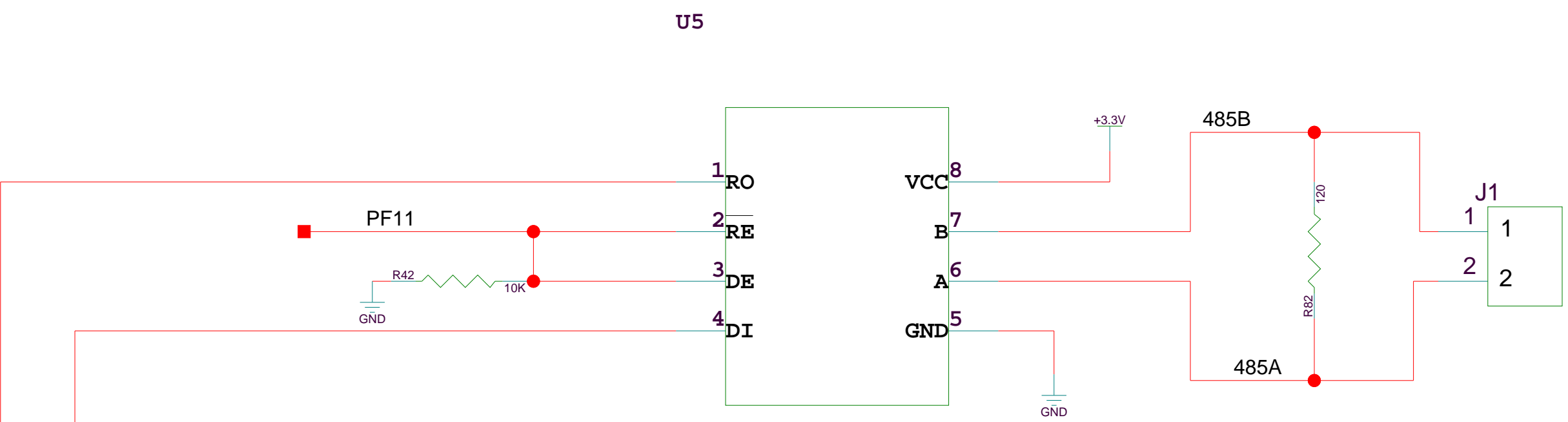
FLASH AND SRAM



RS-232



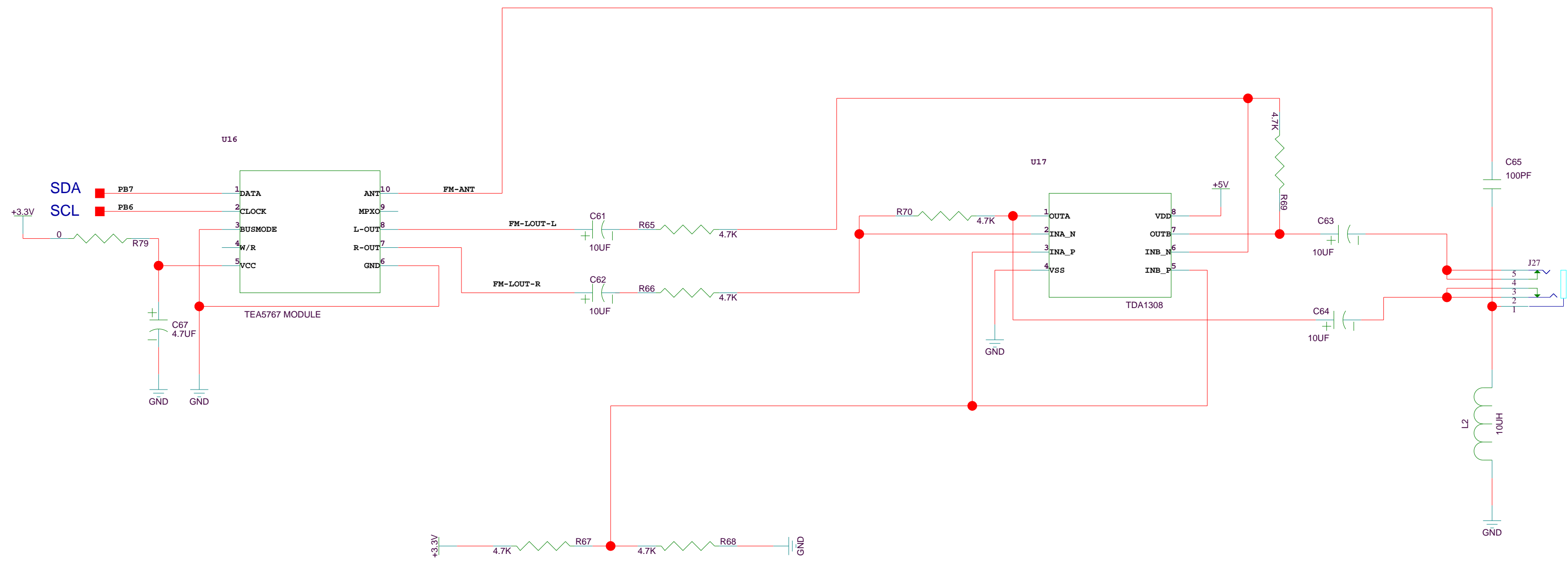
RS-485



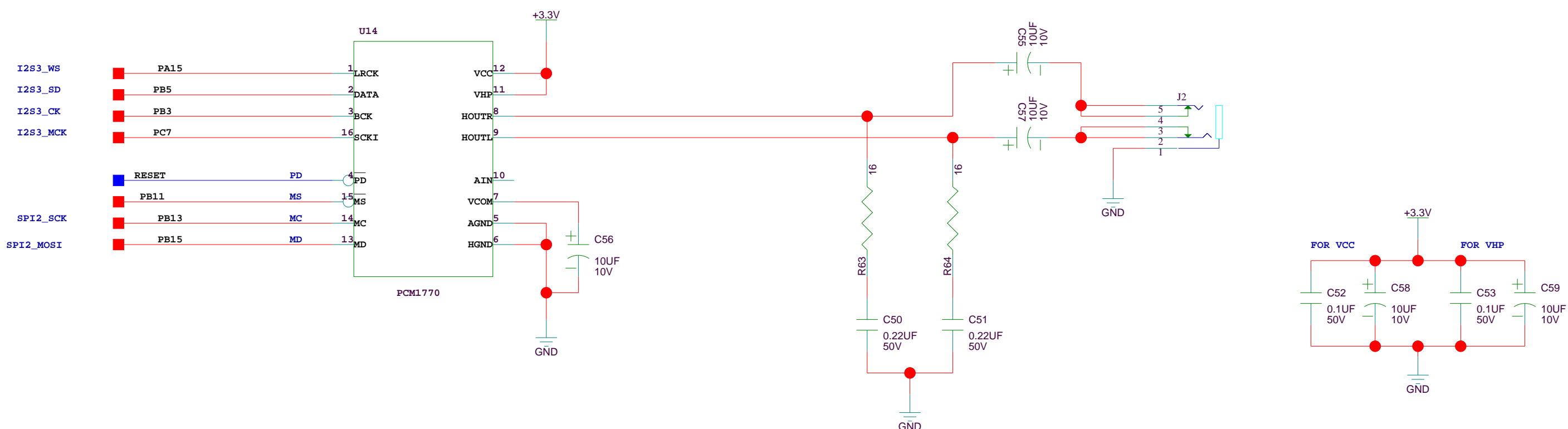
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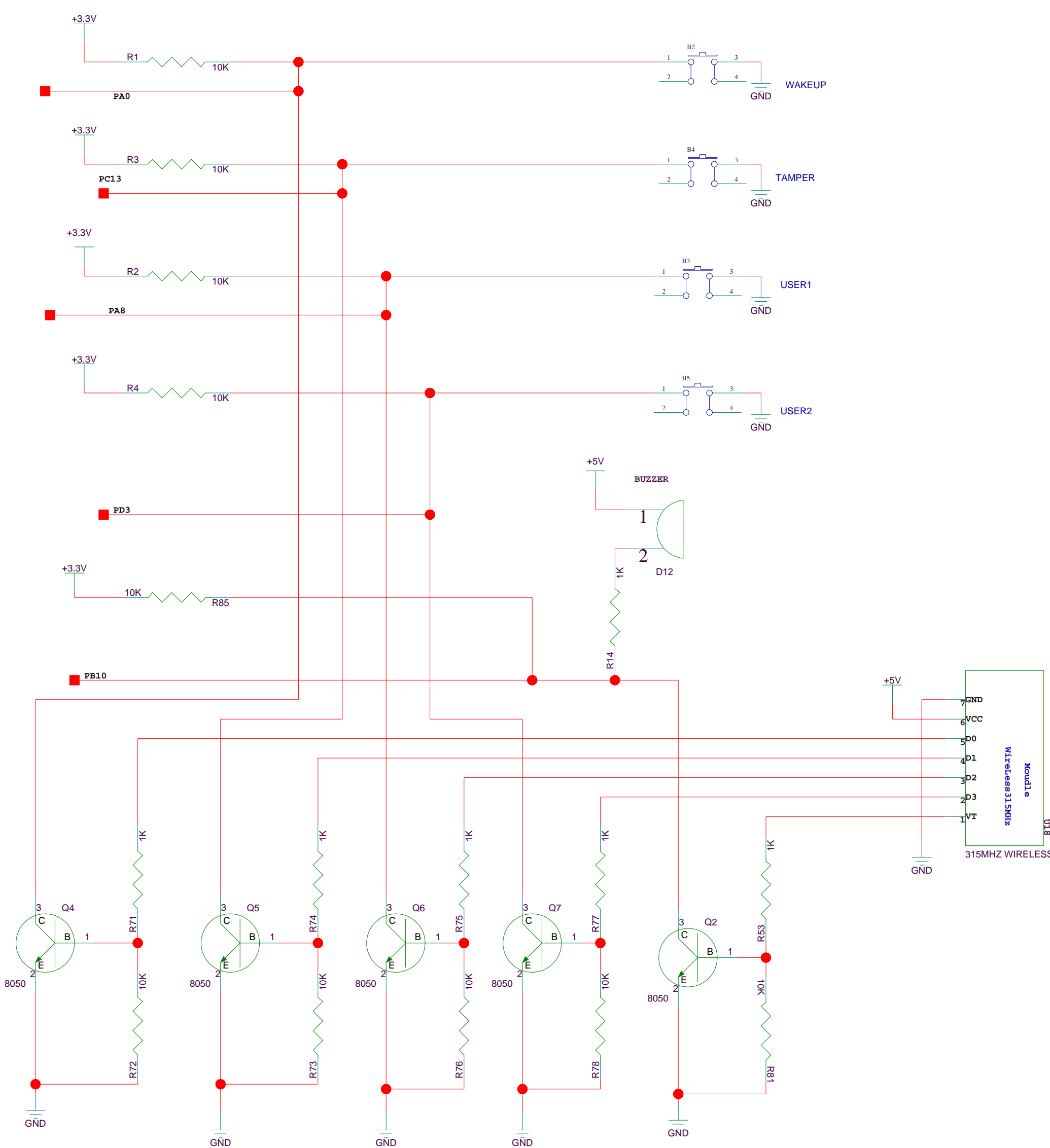
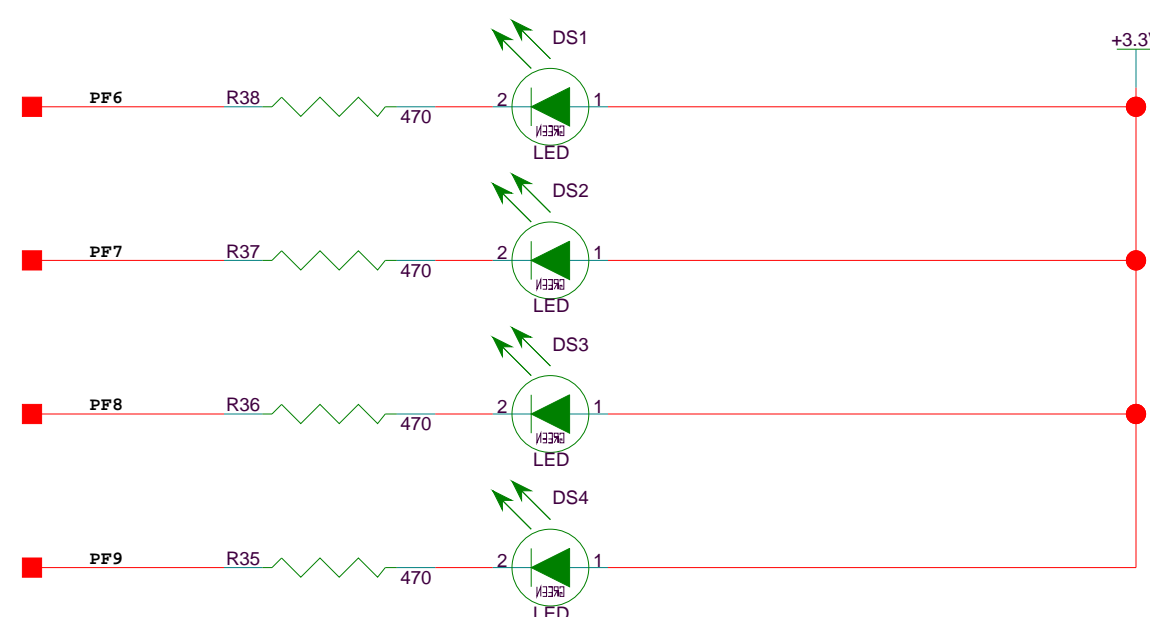
FM



AUDIO DAC



LED



KEY AND 315MHZ WIRELESS MODULE

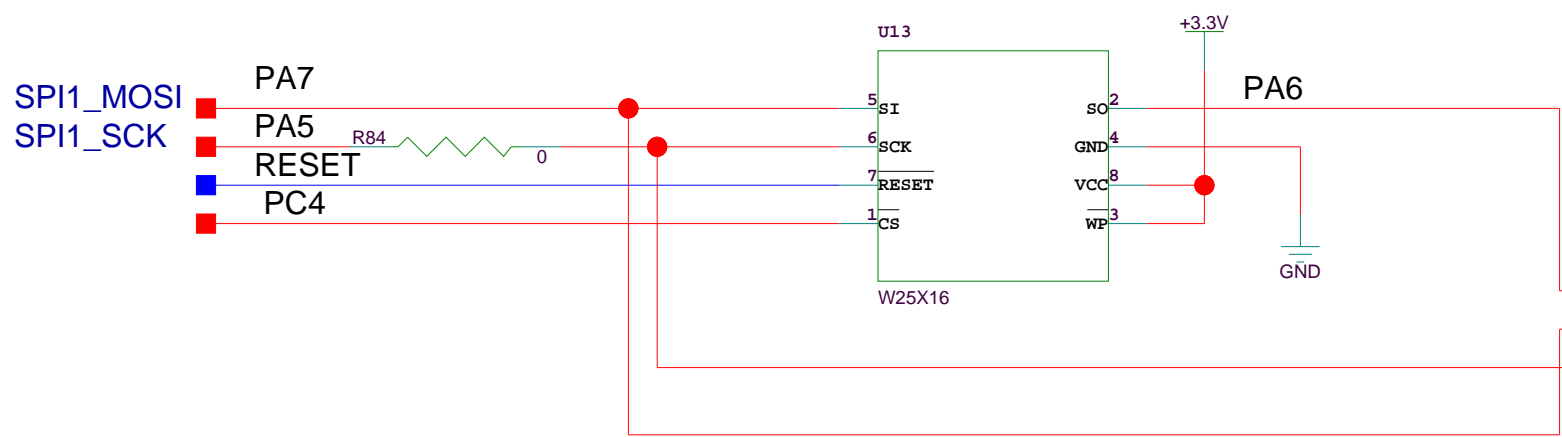
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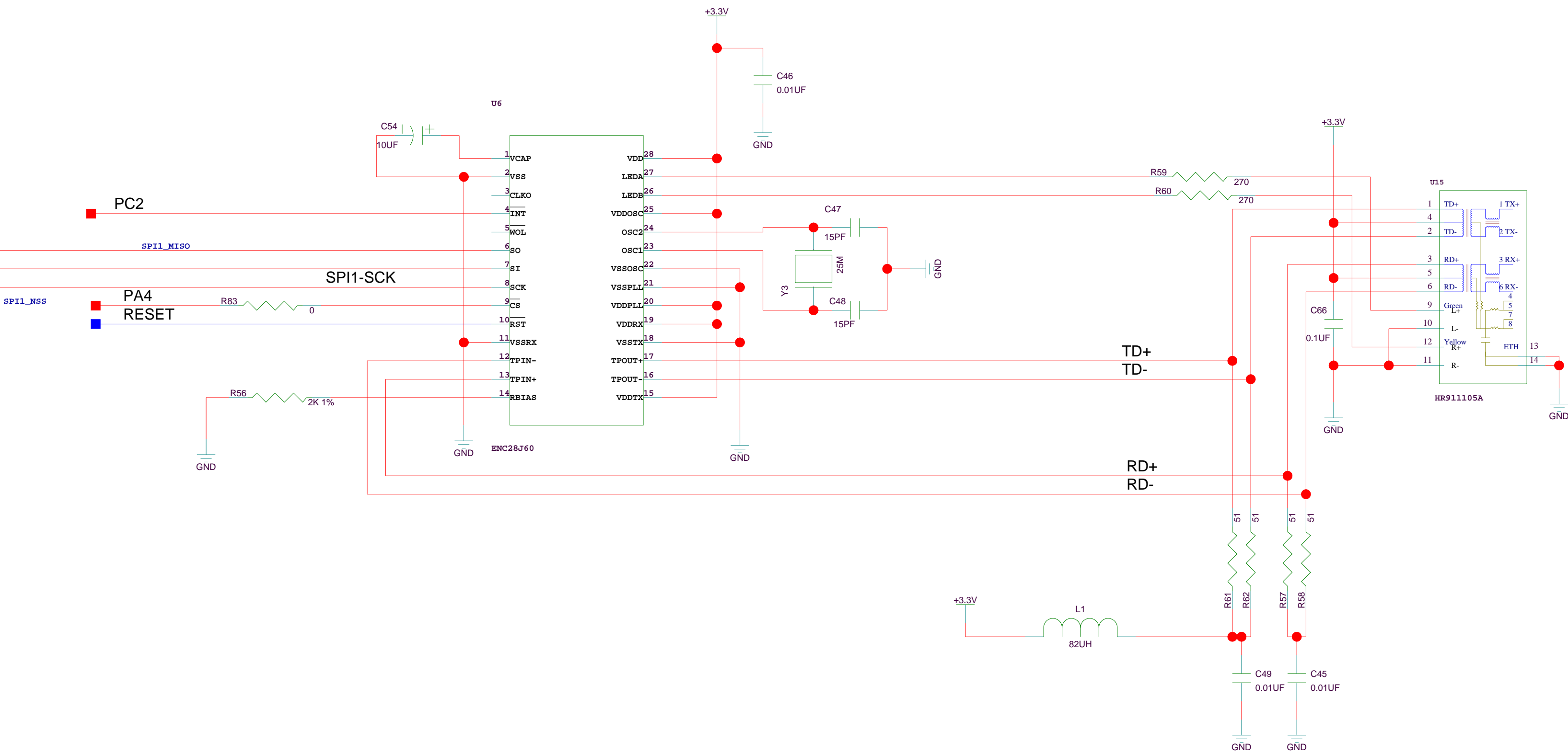
www.armjishu.com

SHEET 1 OF 6 REV V??

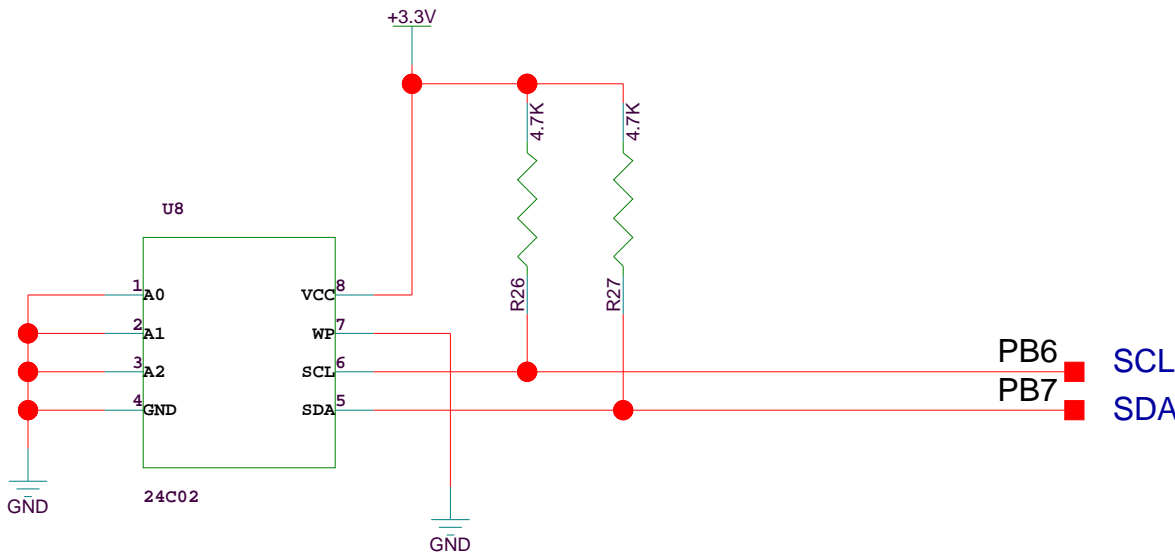
SPI FLASH



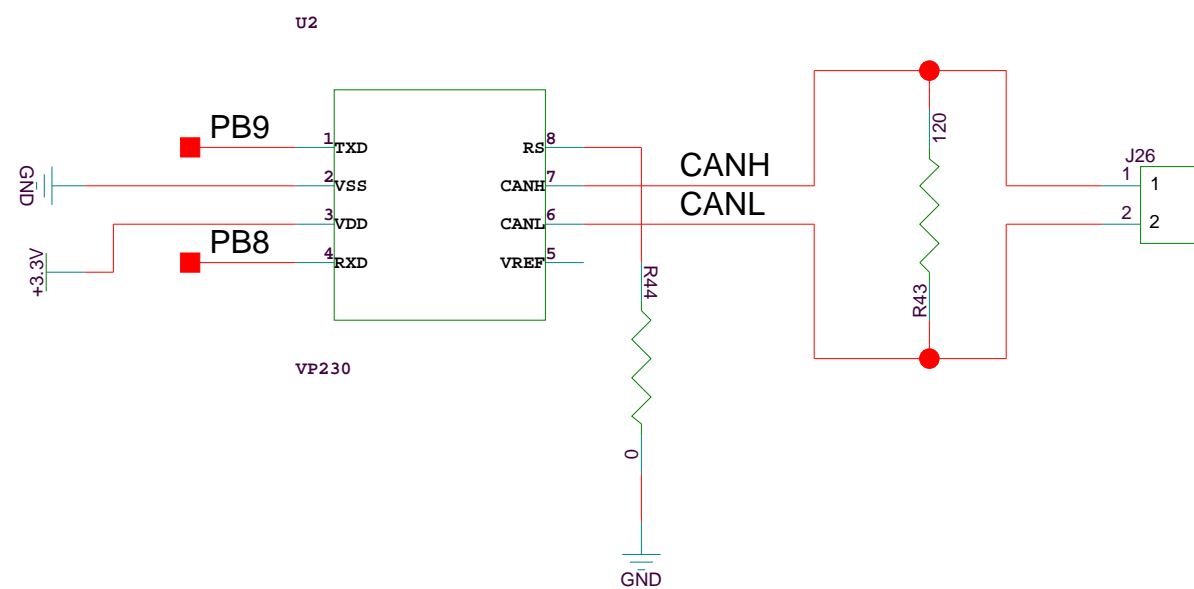
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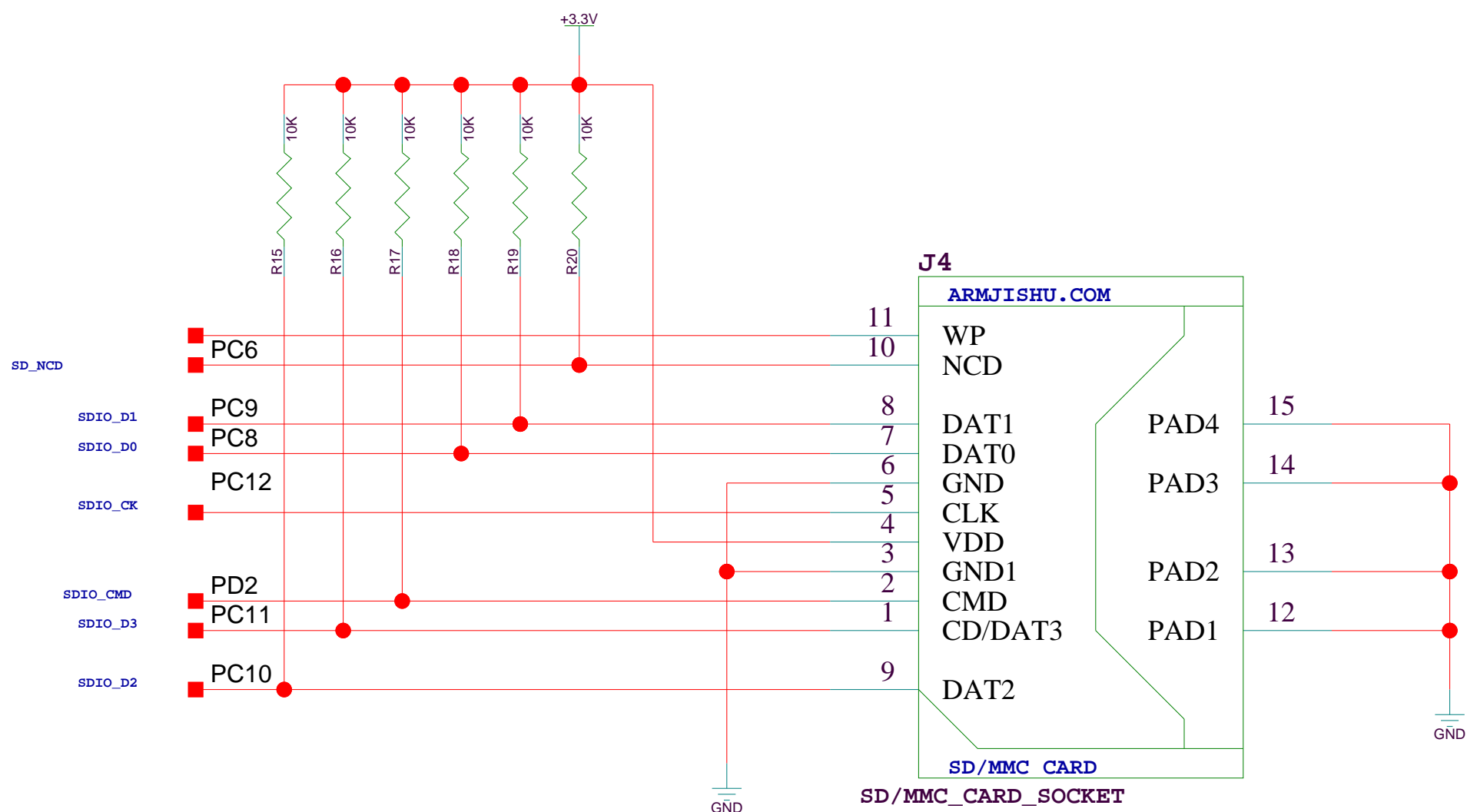
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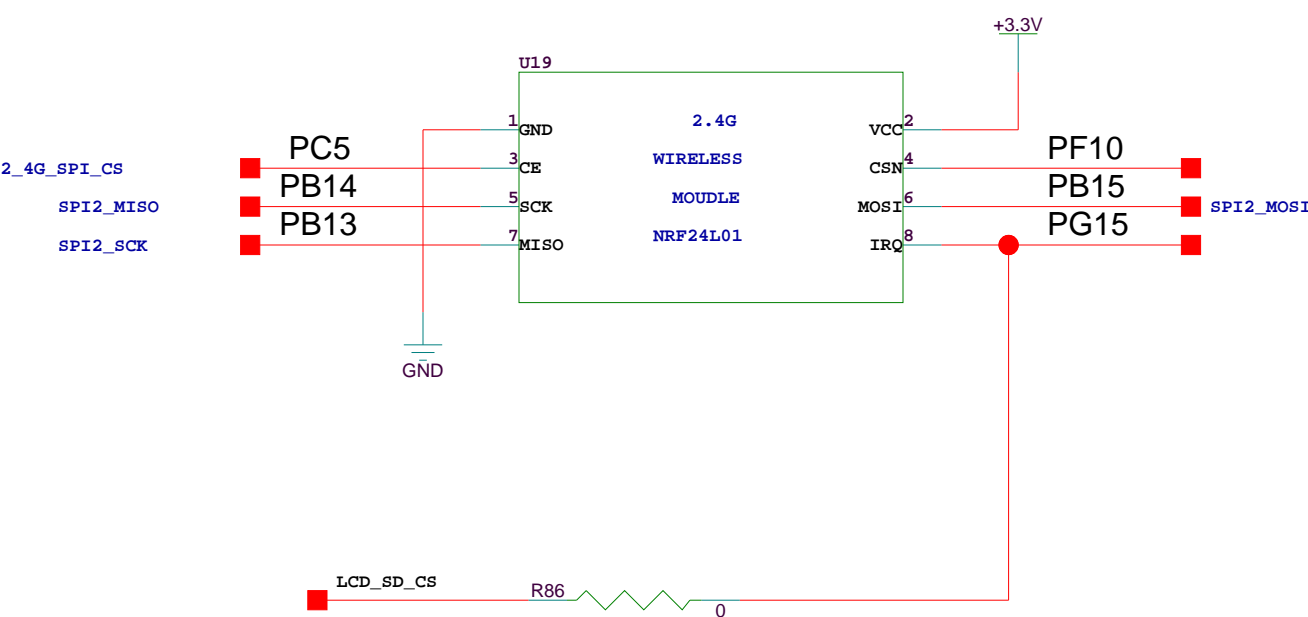
CAN



SD



2.4G WIRELESS MODULE



TITLE

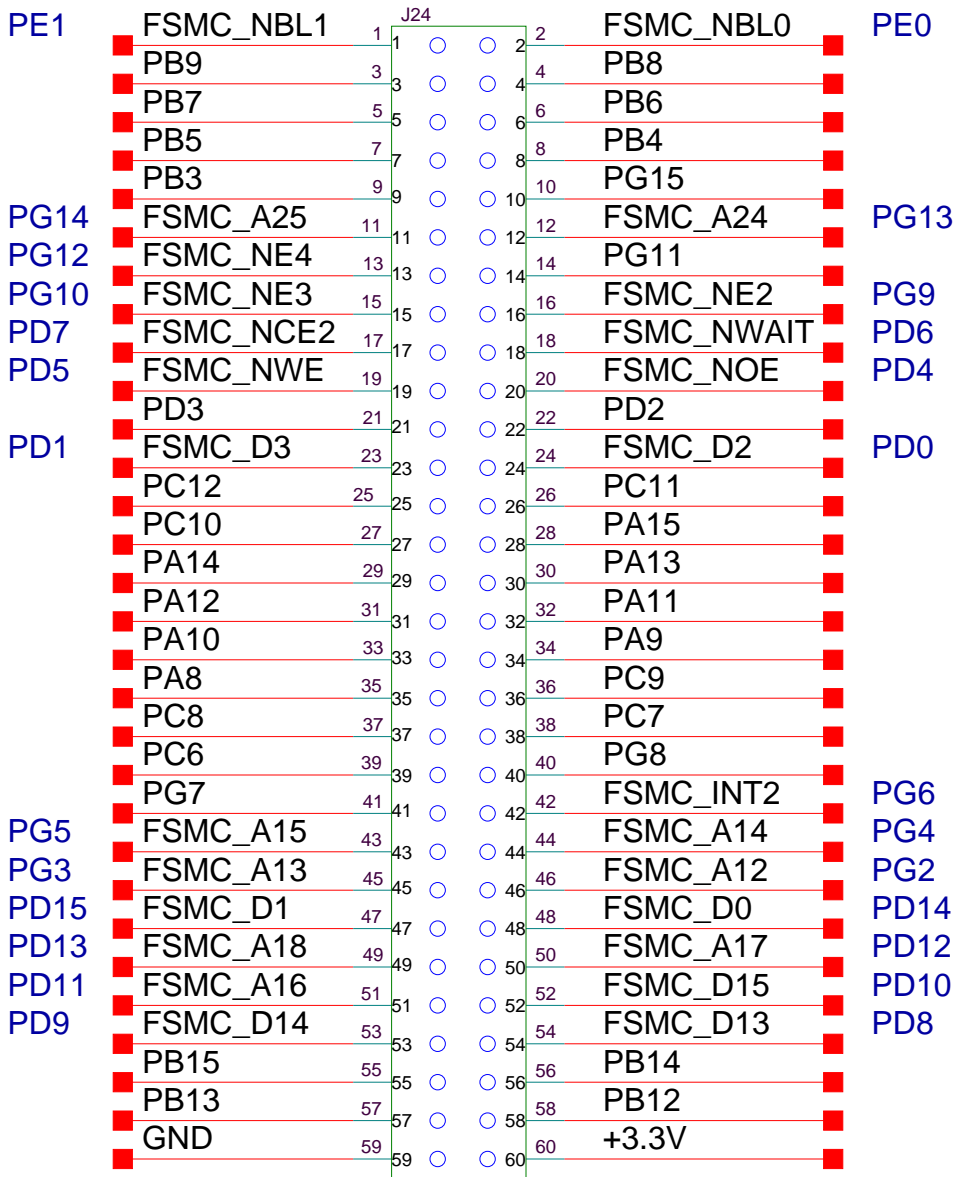
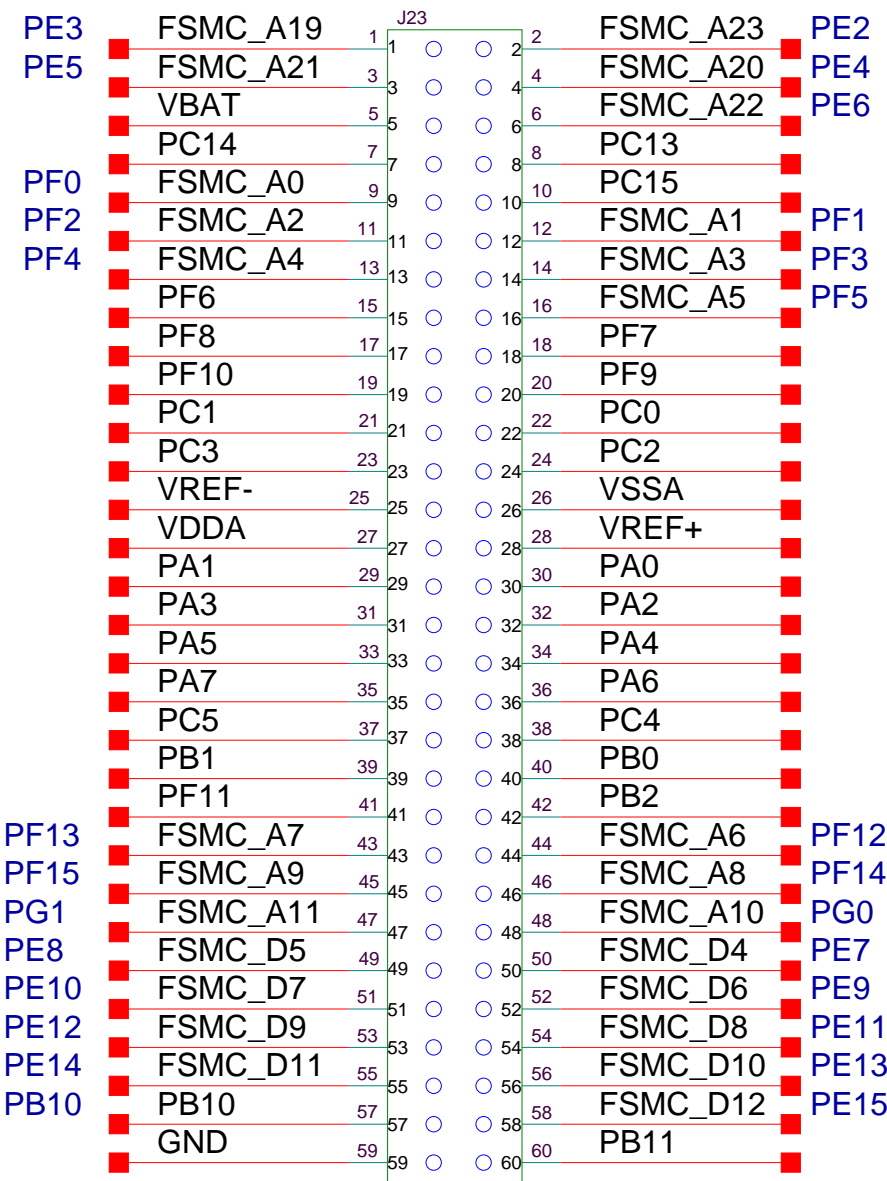
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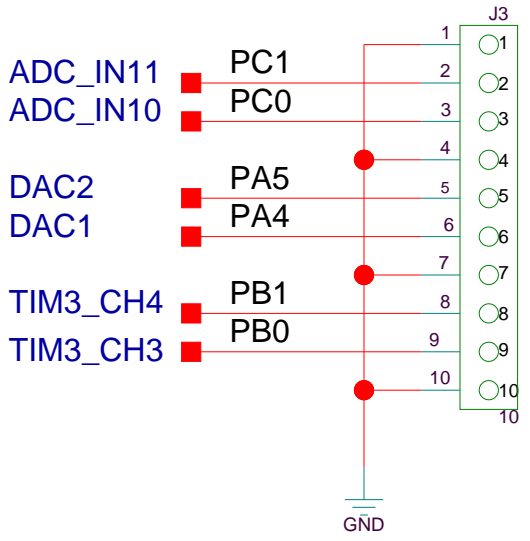
SHEET 1 OF 6

REV V??

EXPANSION INTERFACE



AD/DA



TITLE

PROJECT NAME