

512K x 16 HIGH SPEED ASYNCHRONOUS CMOS STATIC RAM WITH 3.3V SUPPLY

DECEMBER 2005

FEATURES

- High-speed access time:
 - 8, 10, and 12 ns
- CMOS low power operation
- Low stand-by power:
 - Less than 5 mA (typ.) CMOS stand-by
- TTL compatible interface levels
- Single 3.3V power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial and Automotive temperatures available
- Lead-free available

DESCRIPTION

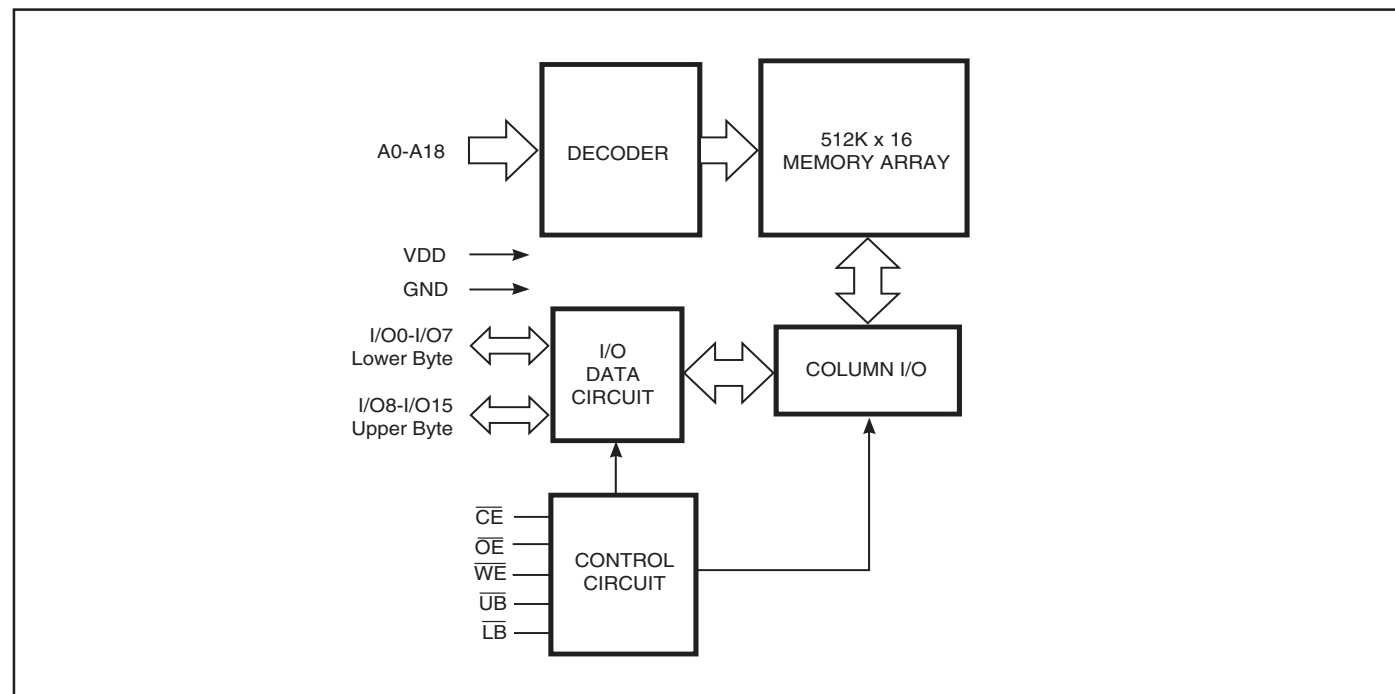
The ISSI IS61/64LV51216 is a high-speed, 8M-bit static RAM organized as 525,288 words by 16 bits. It is fabricated using ISSI's high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When \overline{CE} is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, \overline{CE} and \overline{OE} . The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory. A data byte allows Upper Byte (\overline{UB}) and Lower Byte (\overline{LB}) access.

The IS61/64LV51216 is packaged in the JEDEC standard 44-pin TSOP Type II and 48-pin Mini BGA (9mm x 1 mm).

FUNCTIONAL BLOCK DIAGRAM



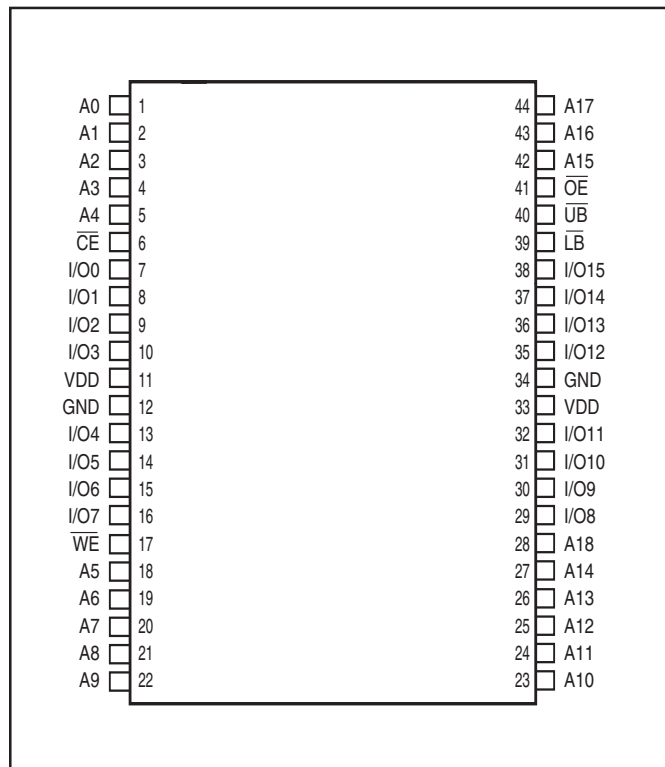
Copyright © 2005 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.

TRUTH TABLE

| Mode | \overline{WE} | \overline{CE} | \overline{OE} | \overline{LB} | \overline{UB} | I/O PIN | | V_{DD} Current |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------|------------|------------------|
| | | | | | | I/O0-I/O7 | I/O8-I/O15 | |
| Not Selected | X | H | X | X | X | High-Z | High-Z | Isb1, Isb2 |
| Output Disabled | H | L | H | X | X | High-Z | High-Z | Icc |
| | X | L | X | H | H | High-Z | High-Z | |
| Read | H | L | L | L | H | DOUT | High-Z | Icc |
| | H | L | L | H | L | High-Z | DOUT | |
| | H | L | L | L | L | DOUT | DOUT | |
| Write | L | L | X | L | H | DIN | High-Z | Icc |
| | L | L | X | H | L | High-Z | DIN | |
| | L | L | X | L | L | DIN | DIN | |

PIN CONFIGURATIONS

44-Pin TSOP (Type II)

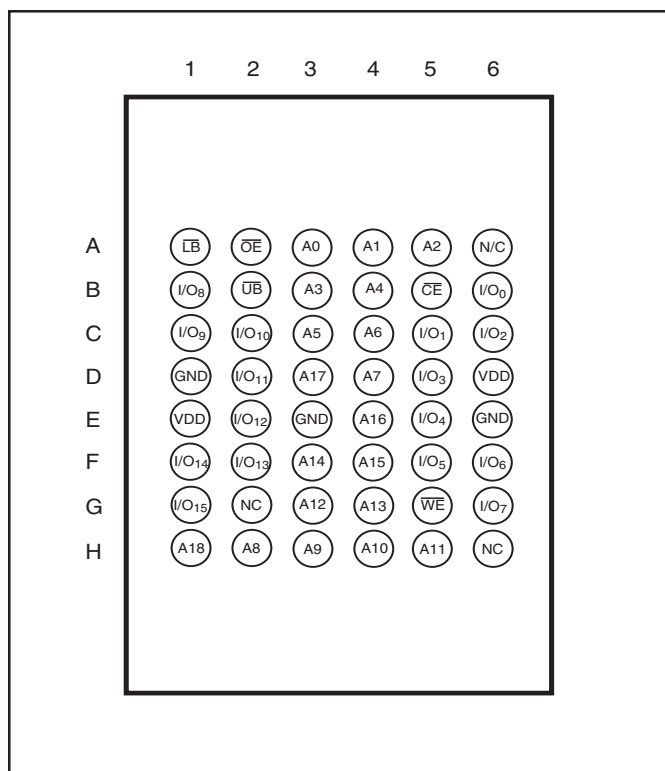


PIN DESCRIPTIONS

| | |
|-----------------|---------------------------------|
| A0-A18 | Address Inputs |
| I/O0-I/O15 | Data Inputs/Outputs |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| \overline{WE} | Write Enable Input |
| \overline{LB} | Lower-byte Control (I/O0-I/O7) |
| \overline{UB} | Upper-byte Control (I/O8-I/O15) |
| NC | No Connection |
| V_{DD} | Power |
| GND | Ground |

PIN CONFIGURATIONS

48-Pin mini BGA (9mmx11mm)



PIN DESCRIPTIONS

| | |
|-----------------|---------------------------------|
| A0-A18 | Address Inputs |
| I/O0-I/O15 | Data Inputs/Outputs |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| \overline{WE} | Write Enable Input |
| \overline{LB} | Lower-byte Control (I/O0-I/O7) |
| \overline{UB} | Upper-byte Control (I/O8-I/O15) |
| NC | No Connection |
| VDD | Power |
| GND | Ground |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|-------------------|--------------------------------------|------------------------------|------|
| V _{TERM} | Terminal Voltage with Respect to GND | -0.5 to V _{DD} +0.5 | V |
| V _{DD} | V _{DD} Related to GND | -0.3 to +4.0 | V |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| P _T | Power Dissipation | 1.0 | W |

Note:

- Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

| Range | Ambient Temperature | V _{DD} |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 3.3V +10%, -5% |
| Industrial | -40°C to +85°C | 3.3V +10%, -5% |
| Automotive | -40°C to +125°C | 3.3V +10%, -5% |

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit | |
|-----------------|----------------------------------|--|-----------------------|-----------------------|---------------|----|
| V _{OH} | Output HIGH Voltage | V _{DD} = Min., I _{OH} = −4.0 mA | 2.4 | — | V | |
| V _{OL} | Output LOW Voltage | V _{DD} = Min., I _{OL} = 8.0 mA | — | 0.4 | V | |
| V _{IH} | Input HIGH Voltage | | 2.2 | V _{DD} + 0.3 | V | |
| V _{IL} | Input LOW Voltage ⁽¹⁾ | | −0.3 | 0.8 | V | |
| I _{LI} | Input Leakage | GND ≤ V _{IN} ≤ V _{DD} | Com. Ind. Auto. | −1 −5 −10 | 1 5 −10 | μA |
| I _{LO} | Output Leakage | GND ≤ V _{OUT} ≤ V _{DD} Outputs Disabled | Com. Ind. Auto. | −1 −5 −10 | 1 5 −10 | μA |

Notes:

1. V_{IL} (min.) = -2.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | | -8 | | -10 | | -12 | | Unit |
|------------------|--|--|-----------------------|------|------------|------|------------|------|------------------|------|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| I _{CC} | V _{DD} Dynamic Operating Supply Current | V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX} | Com. Ind. Auto. | — | 110 120 | — | 100 110 | — | 90 100 120 | mA |
| I _{SB1} | TTL Standby Current (TTL Inputs) | V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = 0 | Com. Ind. Auto. | — | 30 35 | — | 30 35 | — | 30 35 40 | mA |
| I _{SB2} | CMOS Standby Current (CMOS Inputs) | V _{DD} = Max., $\overline{CE} \geq V_{DD} - 0.2V$, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0 | Com. Ind. Auto. | — | 20 25 | — | 20 25 | — | 20 25 30 | mA |

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE⁽¹⁾

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 6 | pF |
| C _{OUT} | Input/Output Capacitance | V _{OUT} = 0V | 8 | pF |

Note:

1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

| Parameter | Unit |
|---|---------------------|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 3 ns |
| Input and Output Timing and Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

AC TEST LOADS

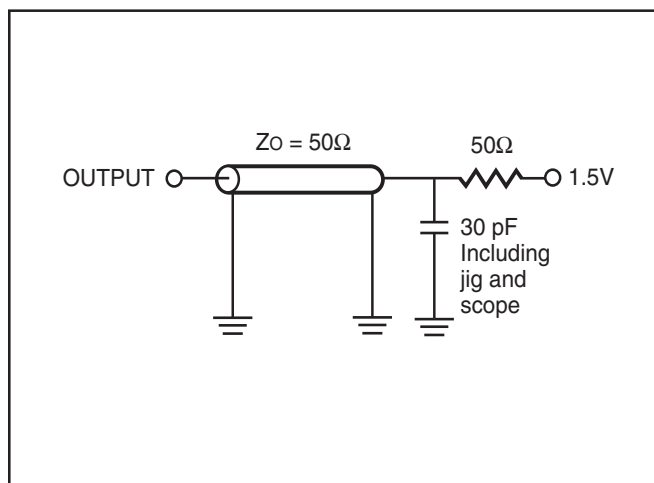


Figure 1

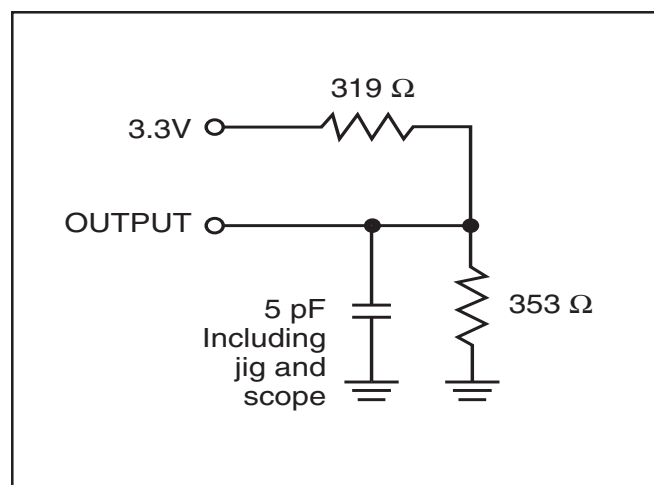


Figure 2

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

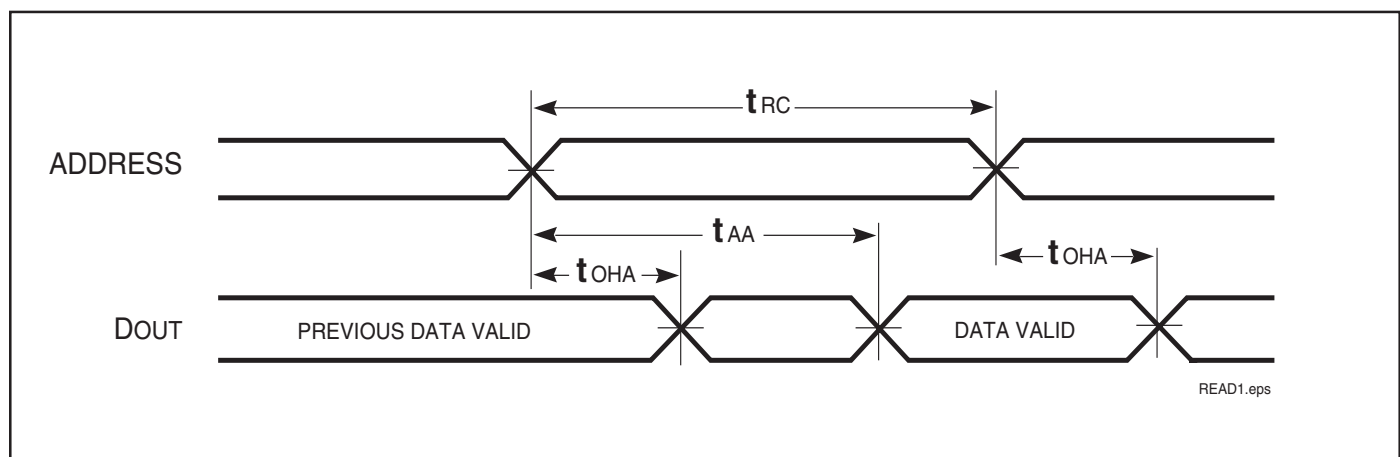
| Symbol | Parameter | -8 | | -10 | | -12 | | Unit |
|----------------------------------|--|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{RC} | Read Cycle Time | 8 | — | 10 | — | 12 | — | ns |
| t _{AA} | Address Access Time | — | 8 | — | 10 | — | 12 | ns |
| t _{OHA} | Output Hold Time | 3 | — | 3 | — | 3 | — | ns |
| t _{ACE} | \overline{CE} Access Time | — | 8 | — | 10 | — | 12 | ns |
| t _{DOE} | \overline{OE} Access Time | — | 3.5 | — | 4 | — | 5 | ns |
| t _{HZOE} ⁽²⁾ | \overline{OE} to High-Z Output | — | 3 | — | 4 | 0 | 5 | ns |
| t _{LZOE} ⁽²⁾ | \overline{OE} to Low-Z Output | 0 | — | 0 | — | 0 | — | ns |
| t _{HZCE} ⁽²⁾ | \overline{CE} to High-Z Output | 0 | 3 | 0 | 4 | 0 | 6 | ns |
| t _{LZCE} ⁽²⁾ | \overline{CE} to Low-Z Output | 3 | — | 3 | — | 3 | — | ns |
| t _{BA} | \overline{LB} , \overline{UB} Access Time | — | 3.5 | — | 4 | — | 5 | ns |
| t _{HZB} ⁽²⁾ | \overline{LB} , \overline{UB} to High-Z Output | 0 | 3 | 0 | 3 | 0 | 4 | ns |
| t _{LZB} ⁽²⁾ | \overline{LB} , \overline{UB} to Low-Z Output | 0 | — | 0 | — | 0 | — | ns |
| t _{PU} | Power Up Time | 0 | — | 0 | — | 0 | — | ns |
| t _{PD} | Power Down Time | — | 8 | — | 10 | — | 12 | ns |

Notes:

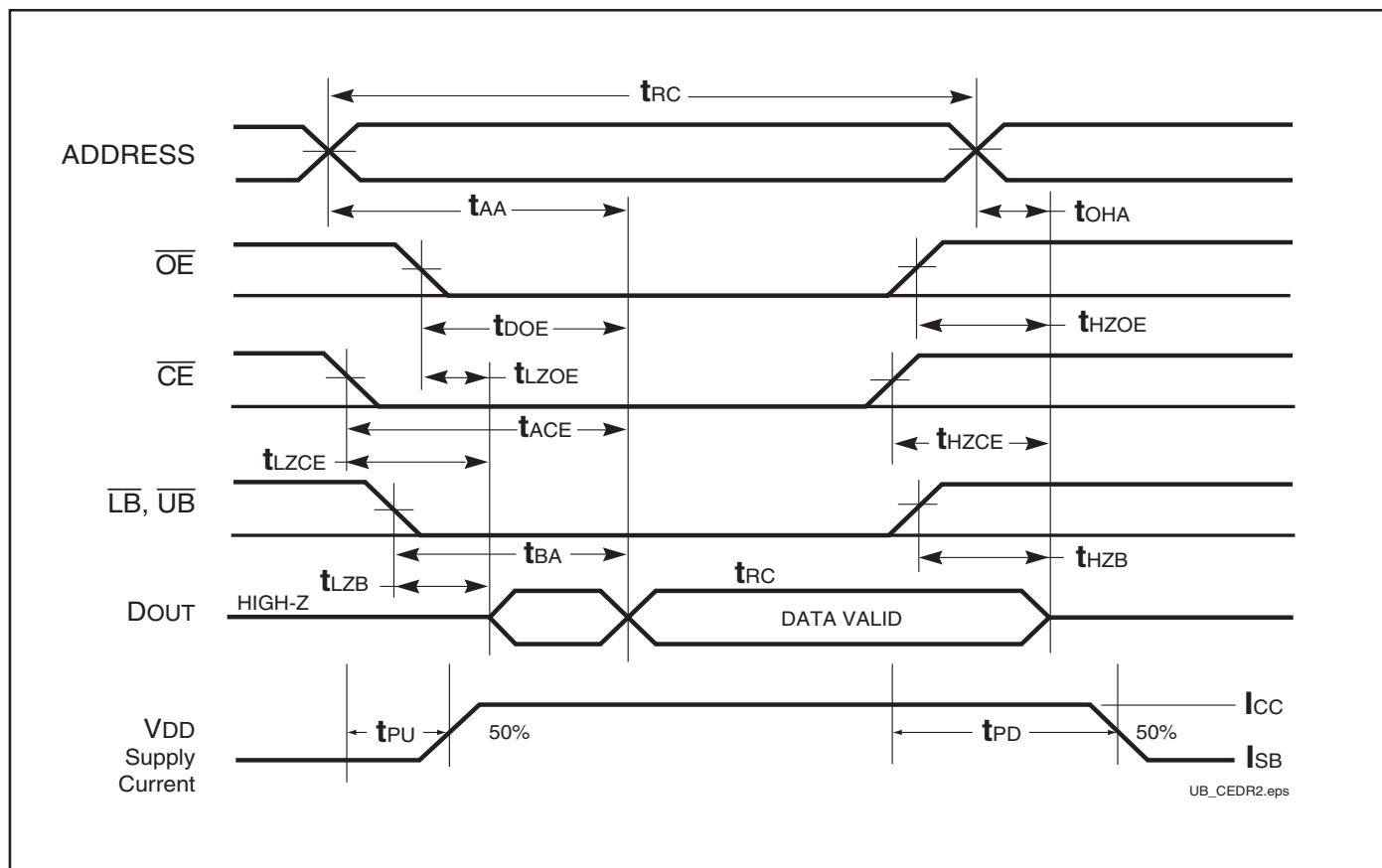
- Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
- Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$, \overline{UB} or $\overline{LB} = V_{IL}$)



READ CYCLE NO. 2^(1,3)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , \overline{CE} , \overline{UB} , or \overline{LB} = V_{IL} .
3. Address is valid prior to or coincident with \overline{CE} LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

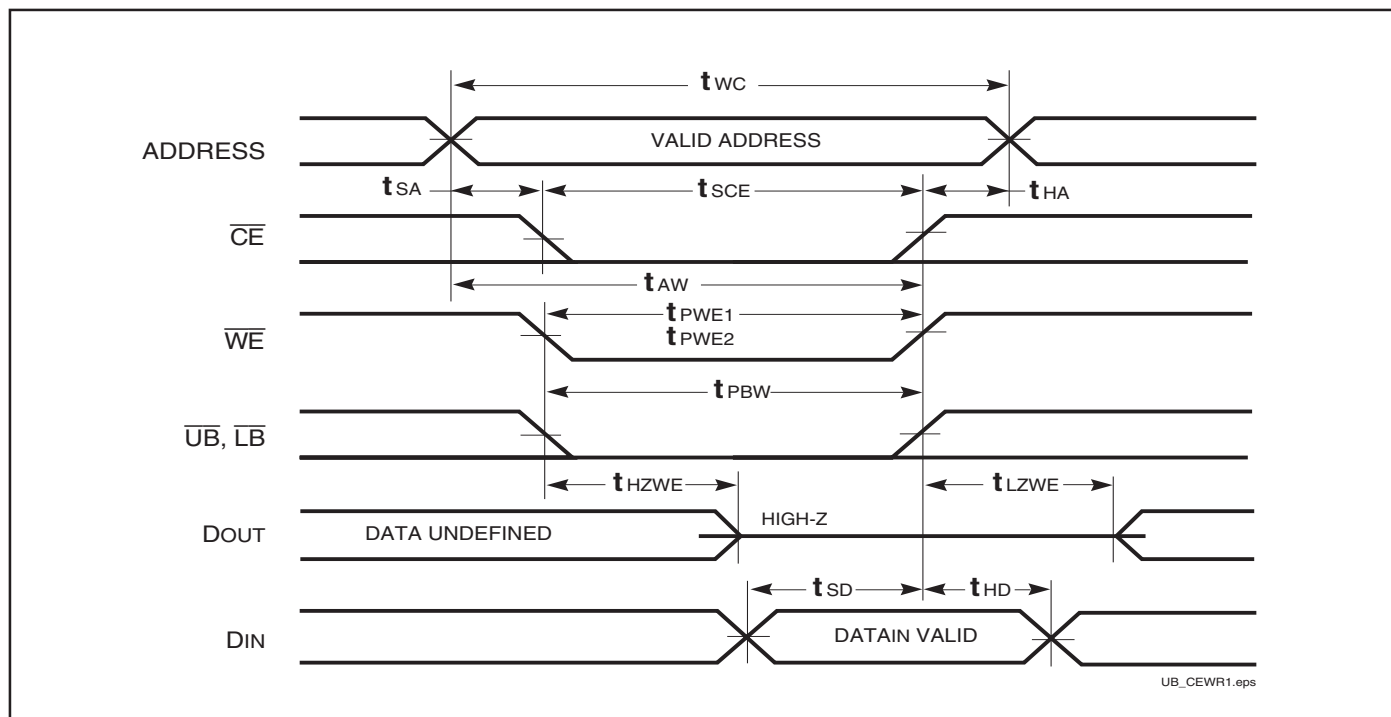
| Symbol | Parameter | -8 | | -10 | | -12 | | Unit |
|----------------------------------|---|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{WC} | Write Cycle Time | 8 | — | 10 | — | 12 | — | ns |
| t _{SCE} | \overline{CE} to Write End | 6.5 | — | 8 | — | 8 | — | ns |
| t _{AW} | Address Setup Time to Write End | 6.5 | — | 8 | — | 8 | — | ns |
| t _{HA} | Address Hold from Write End | 0 | — | 0 | — | 0 | — | ns |
| t _{SA} | Address Setup Time | 0 | — | 0 | — | 0 | — | ns |
| t _{PWB} | \overline{LB} , \overline{UB} Valid to End of Write | 6.5 | — | 8 | — | 8 | — | ns |
| t _{PWE1} | \overline{WE} Pulse Width | 6.5 | — | 8 | — | 8 | — | ns |
| t _{PWE2} | \overline{WE} Pulse Width (\overline{OE} = LOW) | 8.0 | — | 10 | — | 12 | — | ns |
| t _{SD} | Data Setup to Write End | 5 | — | 6 | — | 6 | — | ns |
| t _{HD} | Data Hold from Write End | 0 | — | 0 | — | 0 | — | ns |
| t _{HZWE} ⁽²⁾ | \overline{WE} LOW to High-Z Output | — | 3.5 | — | 5 | — | 6 | ns |
| t _{LZWE} ⁽²⁾ | \overline{WE} HIGH to Low-Z Output | 2 | — | 2 | — | 2 | — | ns |

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{UB} or \overline{LB} , and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development

AC WAVEFORMS

WRITE CYCLE NO. 1 (\overline{CE} Controlled, \overline{OE} is HIGH or LOW) ⁽¹⁾

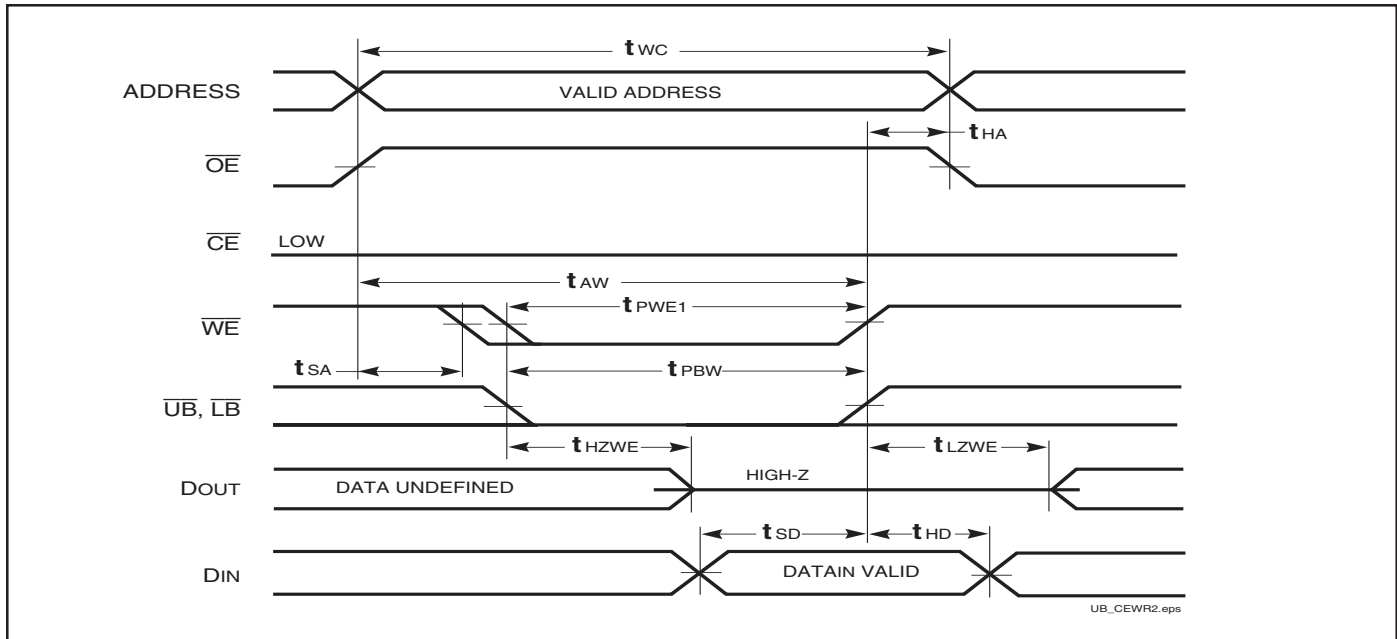


Notes:

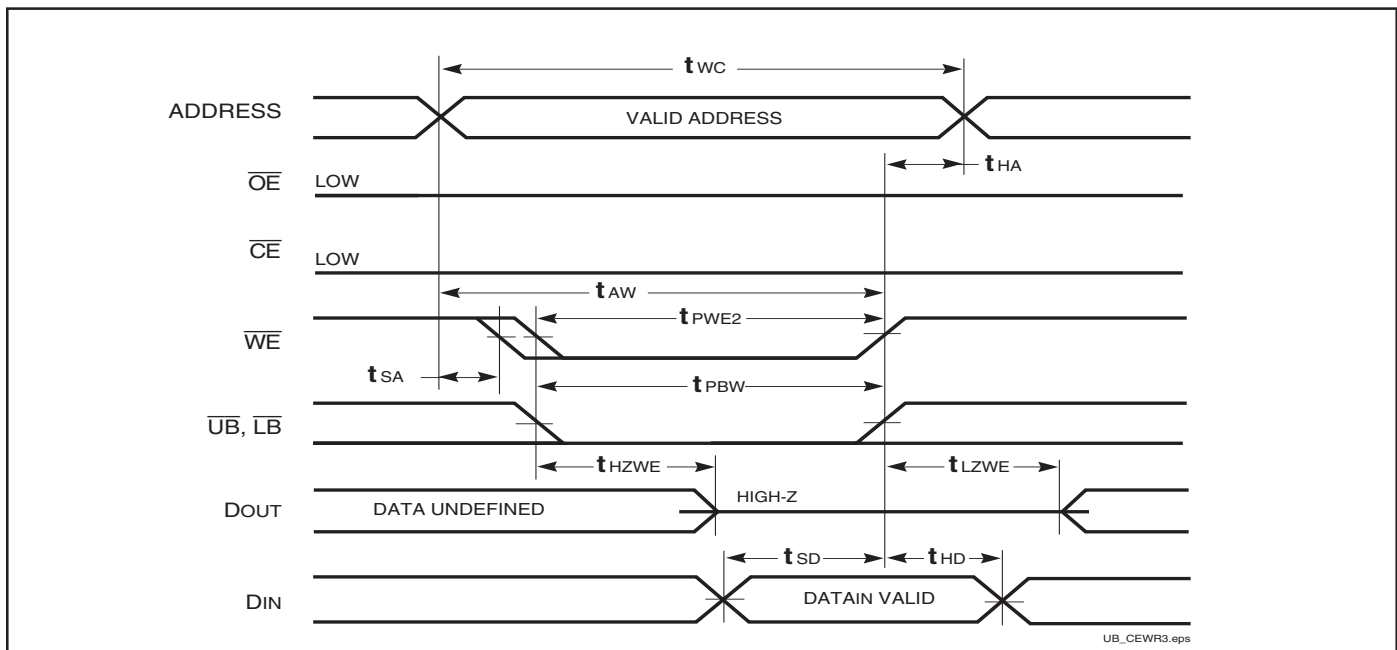
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the \overline{CE} and \overline{WE} inputs and at least one of the \overline{LB} and \overline{UB} inputs being in the LOW state.
2. WRITE = (\overline{CE}) [(\overline{LB}) = (\overline{UB})] (\overline{WE}).

AC WAVEFORMS

WRITE CYCLE NO. 2 (\overline{WE} Controlled. \overline{OE} is HIGH During Write Cycle) ^(1,2)

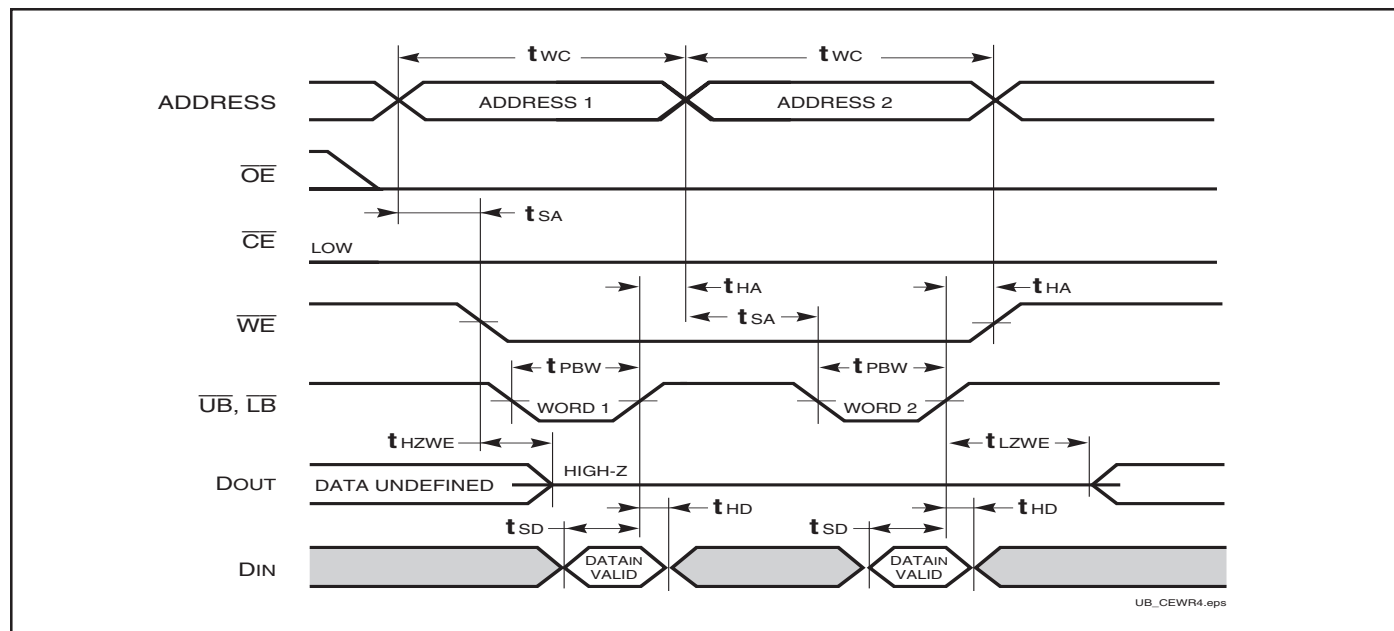


WRITE CYCLE NO. 3 (\overline{WE} Controlled. \overline{OE} is LOW During Write Cycle) ⁽¹⁾



AC WAVEFORMS

WRITE CYCLE NO. 4 ($\overline{\text{LB}}$, $\overline{\text{UB}}$ Controlled, Back-to-Back Write) ^(1,3)



Notes:

1. The internal Write time is defined by the overlap of $\overline{\text{CE}} = \text{LOW}$, $\overline{\text{UB}}$ and/or $\overline{\text{LB}} = \text{LOW}$, and $\overline{\text{WE}} = \text{LOW}$. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The t_{SA} , t_{HA} , t_{SD} , and t_{HD} timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with $\overline{\text{OE}}$ HIGH for a minimum of 4 ns before $\overline{\text{WE}} = \text{LOW}$ to place the I/O in a HIGH-Z state.
3. $\overline{\text{WE}}$ may be held LOW across many address cycles and the $\overline{\text{LB}}$, $\overline{\text{UB}}$ pins can be used to control the Write function.

ORDERING INFORMATION:

Commercial Range: 0°C to +70°C

| Speed (ns) | Order Part No. | Package |
|------------|-----------------|---------------------------|
| 8 | IS61LV51216-8T | TSOP (Type II) |
| | IS61LV51216-8TL | TSOP (Type II), Lead-free |
| | IS61LV51216-8M | Mini BGA (9mm x 11mm) |
| 10 | IS61LV51216-10T | TSOP (Type II) |
| | IS61LV51216-10M | Mini BGA (9mm x 11mm) |
| 12 | IS61LV51216-12T | TSOP (Type II) |

Industrial Range: -40°C to +85°C

| Speed (ns) | Order Part No. | Package |
|------------|-------------------|----------------------------------|
| 8 | IS61LV51216-8TI | TSOP (Type II) |
| | IS61LV51216-8MI | Mini BGA (9mm x 11mm) |
| 10 | IS61LV51216-10TI | TSOP (Type II) |
| | IS61LV51216-10TLI | TSOP (Type II), Lead-free |
| | IS61LV51216-10MI | Mini BGA (9mm x 11mm) |
| | IS61LV51216-10MLI | Mini BGA (9mm x 11mm), Lead-free |
| 12 | IS61LV51216-12TI | TSOP (Type II) |

Automotive Range: -40°C to +125°C

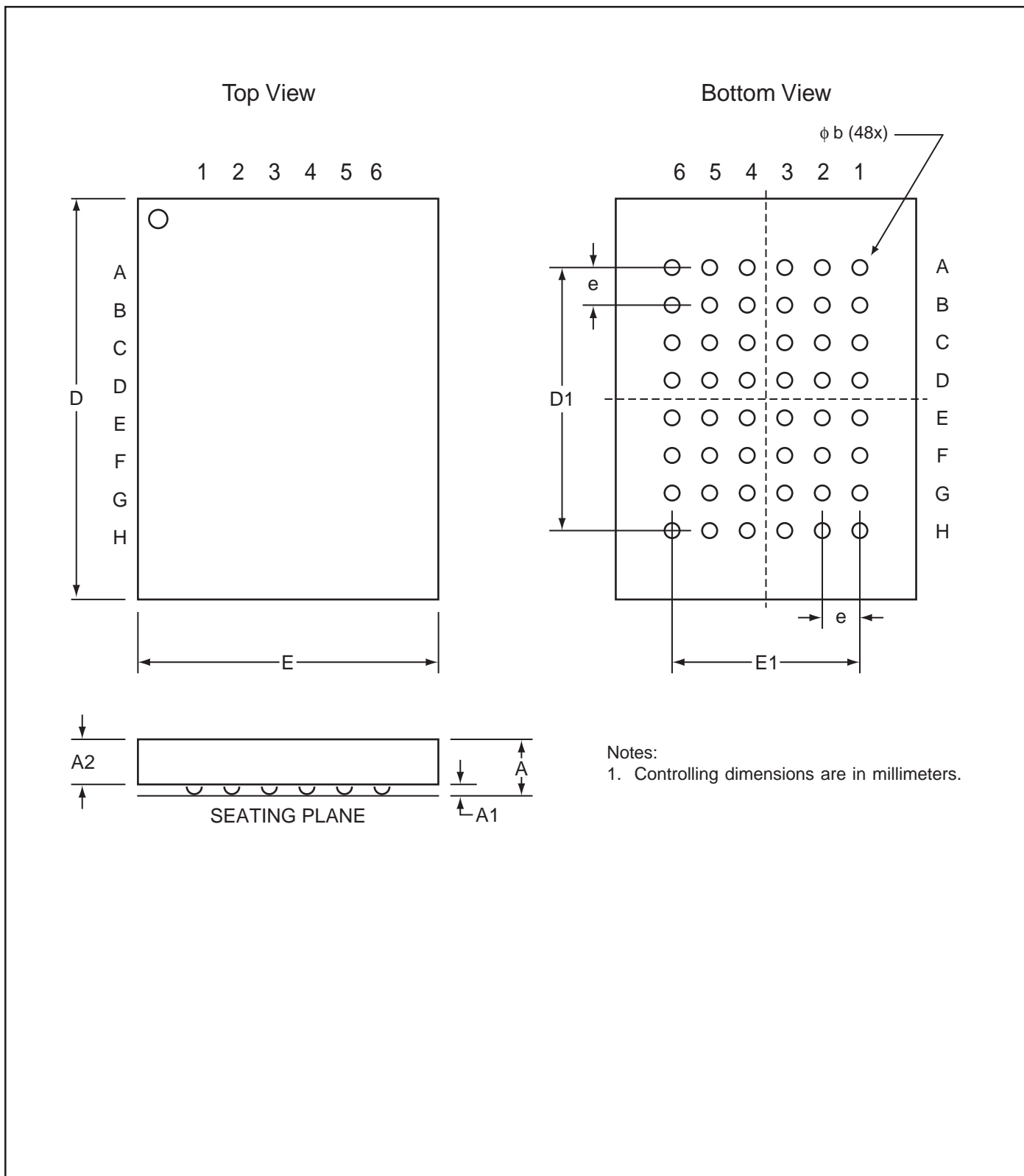
| Speed (ns) | Order Part No. | Package |
|------------|--------------------|---|
| 12 | IS64LV51216-12TA3 | TSOP (Type II) ⁽¹⁾ |
| | IS64LV51216-12TLA3 | TSOP (Type II) ⁽¹⁾ , Lead-free |

Note:

1. Copper Leadframe

PACKAGING INFORMATION

Mini Ball Grid Array Package Code: M (48-pin)



Copyright © 2003 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.

PACKAGING INFORMATION



Mini Ball Grid Array

Package Code: M (48-pin)

mBGA - 6mm x 8mm

| MILLIMETERS | | | | INCHES | | |
|--------------|---------|------|------|----------|-------|-------|
| Sym. | Min. | Typ. | Max. | Min. | Typ. | Max. |
| N0. Leads | 48 | | | | | |
| A | — | — | 1.20 | — | — | 0.047 |
| A1 | 0.25 | — | 0.40 | 0.010 | — | 0.016 |
| A2 | 0.60 | — | — | 0.024 | — | — |
| D | 7.90 | 8.00 | 8.10 | 0.311 | 0.314 | 0.319 |
| D1 | 5.60BSC | | | 0.220BSC | | |
| E | 5.90 | 6.00 | 6.10 | 0.232 | 0.236 | 0.240 |
| E1 | 4.00BSC | | | 0.157BSC | | |
| e | 0.80BSC | | | 0.031BSC | | |
| b | 0.40 | 0.45 | 0.50 | 0.016 | 0.018 | 0.020 |

mBGA - 7.2mm x 8.7mm

| MILLIMETERS | | | | INCHES | | |
|--------------|---------|------|------|----------|-------|-------|
| Sym. | Min. | Typ. | Max. | Min. | Typ. | Max. |
| N0. Leads | 48 | | | | | |
| A | — | — | 1.20 | — | — | 0.047 |
| A1 | 0.24 | — | 0.30 | 0.009 | — | 0.012 |
| A2 | 0.60 | — | — | 0.024 | — | — |
| D | 8.60 | 8.70 | 8.80 | 0.339 | 0.343 | 0.346 |
| D1 | 5.25BSC | | | 0.207BSC | | |
| E | 7.10 | 7.20 | 7.30 | 0.280 | 0.283 | 0.287 |
| E1 | 3.75BSC | | | 0.148BSC | | |
| e | 0.75BSC | | | 0.030BSC | | |
| b | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |

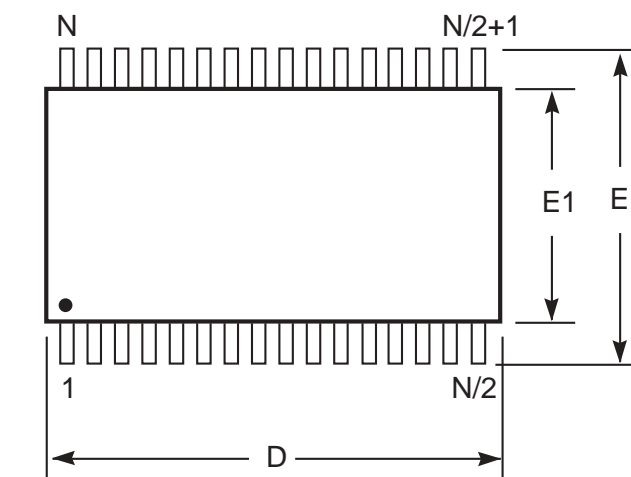
mBGA - 9mm x 11mm

| MILLIMETERS | | | | INCHES | | |
|--------------|---------|-------|-------|----------|-------|-------|
| Sym. | Min. | Typ. | Max. | Min. | Typ. | Max. |
| N0. Leads | 48 | | | | | |
| A | — | — | 1.20 | — | — | 0.047 |
| A1 | 0.24 | — | 0.30 | 0.009 | — | 0.012 |
| A2 | 0.60 | — | — | 0.024 | — | — |
| D | 10.90 | 11.00 | 11.10 | 0.429 | 0.433 | 0.437 |
| D1 | 5.25BSC | | | 0.207BSC | | |
| E | 8.90 | 9.00 | 9.10 | 0.350 | 0.354 | 0.358 |
| E1 | 3.75BSC | | | 0.148BSC | | |
| e | 0.75BSC | | | 0.030BSC | | |
| b | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |

PACKAGING INFORMATION

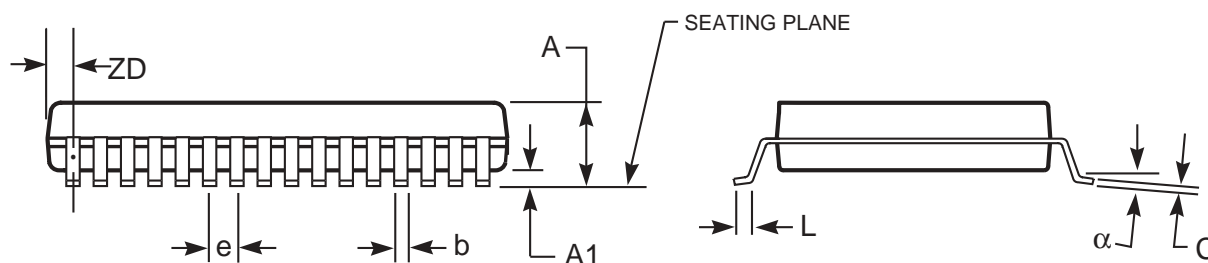
Plastic TSOP

Package Code: T (Type II)



Notes:

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



Plastic TSOP (T - Type II)

| Symbol | Millimeters | | Inches | | Millimeters | | Inches | | Millimeters | | Inches | |
|---------------|-------------|-------|-----------|-------|-------------|-------|-----------|-------|-------------|-------|-----------|-------|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |
| Ref. Std. | | | | | | | | | | | | |
| No. Leads (N) | 32 | | | | 44 | | | | 50 | | | |
| A | — | 1.20 | — | 0.047 | — | 1.20 | — | 0.047 | — | 1.20 | — | 0.047 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 | 0.05 | 0.15 | 0.002 | 0.006 | 0.05 | 0.15 | 0.002 | 0.006 |
| b | 0.30 | 0.52 | 0.012 | 0.020 | 0.30 | 0.45 | 0.012 | 0.018 | 0.30 | 0.45 | 0.012 | 0.018 |
| C | 0.12 | 0.21 | 0.005 | 0.008 | 0.12 | 0.21 | 0.005 | 0.008 | 0.12 | 0.21 | 0.005 | 0.008 |
| D | 20.82 | 21.08 | 0.820 | 0.830 | 18.31 | 18.52 | 0.721 | 0.729 | 20.82 | 21.08 | 0.820 | 0.830 |
| E1 | 10.03 | 10.29 | 0.391 | 0.400 | 10.03 | 10.29 | 0.395 | 0.405 | 10.03 | 10.29 | 0.395 | 0.405 |
| E | 11.56 | 11.96 | 0.451 | 0.466 | 11.56 | 11.96 | 0.455 | 0.471 | 11.56 | 11.96 | 0.455 | 0.471 |
| e | 1.27 BSC | | 0.050 BSC | | 0.80 BSC | | 0.032 BSC | | 0.80 BSC | | 0.031 BSC | |
| L | 0.40 | 0.60 | 0.016 | 0.024 | 0.41 | 0.60 | 0.016 | 0.024 | 0.40 | 0.60 | 0.016 | 0.024 |
| ZD | 0.95 REF | | 0.037 REF | | 0.81 REF | | 0.032 REF | | 0.88 REF | | 0.035 REF | |
| α | 0° | 5° | 0° | 5° | 0° | 5° | 0° | 5° | 0° | 5° | 0° | 5° |

Copyright © 2003 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.