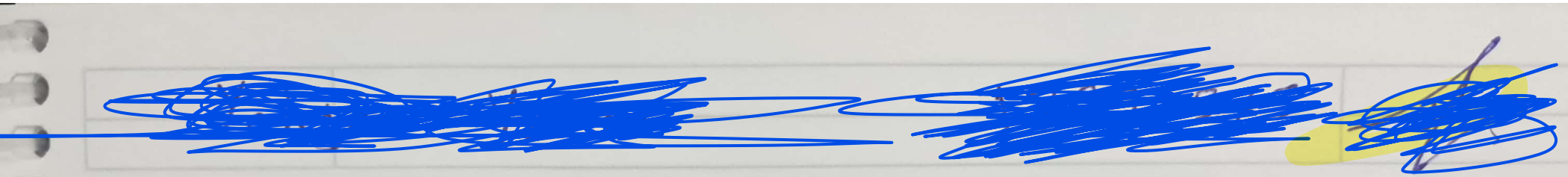

(1) a) main structural components of a computer:

1. central processing Unit
2. Main memory
3. I/O:
4. System interconnection.

b) main structural components of a processor:

1. ALU: Arithmetic and logic Unit
2. Registers
3. Control Unit
4. CPU interconnection.

(2) Pipelining: when processor can work simultaneously on multiple instructions

Branch prediction: when the processor looks ahead in the instructions and predicts which groups of instructions are likely to be processed next

Data flow analysis: the processor analyzes which instructions are dependent on each other's result or data to create an optimized schedule of instructions

Speculative execution: when processor uses the branch prediction and data analysis to speculatively execute instructions ahead of their actual appearance and holding the result in temporary locations

(b) Average CPI $= (1 \times 0.65) + (2 \times 0.15) + (4 \times 0.15) + (8 \times 0.05)$
$= \boxed{1.95}$

$$MIPS = \frac{f}{CPI \times 10^6} = \frac{800 \times 10^6}{1.95 \times 10^6} = \boxed{410}$$

(c)

$$\text{Speed up} = \frac{\text{Time to execute program on a single processor}}{\text{Time to execute program on 4 parallel processor}}$$

$$= \frac{1}{(1-f) + \frac{f}{N}} = \frac{1}{(1-0.4) + \frac{0.4}{4}} = \boxed{1.43}$$

(3) 1. A disabled interrupt simply means that processor will ignore that interrupt and it will remain pending until the processor enable interrupts again. this will cause all interrupts to be executed in sequential order

2. second approach to define priorities for interrupts and to allow higher priority interrupts to cause a lower priority interupts handeler to be interrupted this will result in mixed sequential and nested interrupts,

(4) 1. centralized arbitration: where there is a singl hardware device is responsible to allocating time on the bus, "bus controller or arbiter"

distributed arbitration: where each module contains access control logic and all modules work together to share the bus

(5) Sequential access: where memory is organized into units of data, called records. access must be made in a specific linear sequence.
for example: Tape units

Direct access: where individual blocks or records has a unique address based on physical location. Access made by direct to reach a general vicinity than sequential search foreach final location
for example: Disk Unit

Random access: each addressable location in memory has a unique physically wired-in adressing mechanism

for example: Main memory

Associative: This is a random access type memory with ability to make comparision of desired bit locations within a word for specified match

For example: Cache memories

6 (a) because processor during the course of execution memory references tend to cluster

- that for to reasons ;loops are sub routines and operations on tables and arrays

(b) it increase the speed of processing when hit occurs processor get data from fast memory and there will be no need to wait for slower main memory.

(c) DRAM is simpler and smaller and stores data in as charge in capacitors

SRAM is faster and stores data using traditional flip-flop logic-gate configuration

(d) ~~(0.9 x 0.01) + (0.1 x (0.1) = 0.019~~

$(0.9 \times 0.01) + (0.1 \times (0.1 + 0.01)) = 0.02\ \mu s$

(e) for single-error-correcting :

$2^k - 1 \geq 32 + k$

$k = 6 : 2^6 - 1 \geq 32 + 6$ ✓

for single-error-correction and Double-Error-Detecti

$k = 6 + 1 = 7$

(7) (a) $\frac{512\ K\ byte}{8\ byte} =$ **64 K lines**

(b) for lines $64\ K = 2^6 \times 2^{10} = 2^{16} \Rightarrow$ **16 bits**

main memory $64\ M = 2^6 \times 2^{20} \Rightarrow 2^{26} \Rightarrow$ **26 bits**

for identifiy a word : $8 = 2^3 \Rightarrow$ **3 bits**

tag + 3 + 16 = 26

tag = 7 bits