LAB 3 Report

Name: Hyokwon Chung, Rishi Jarral

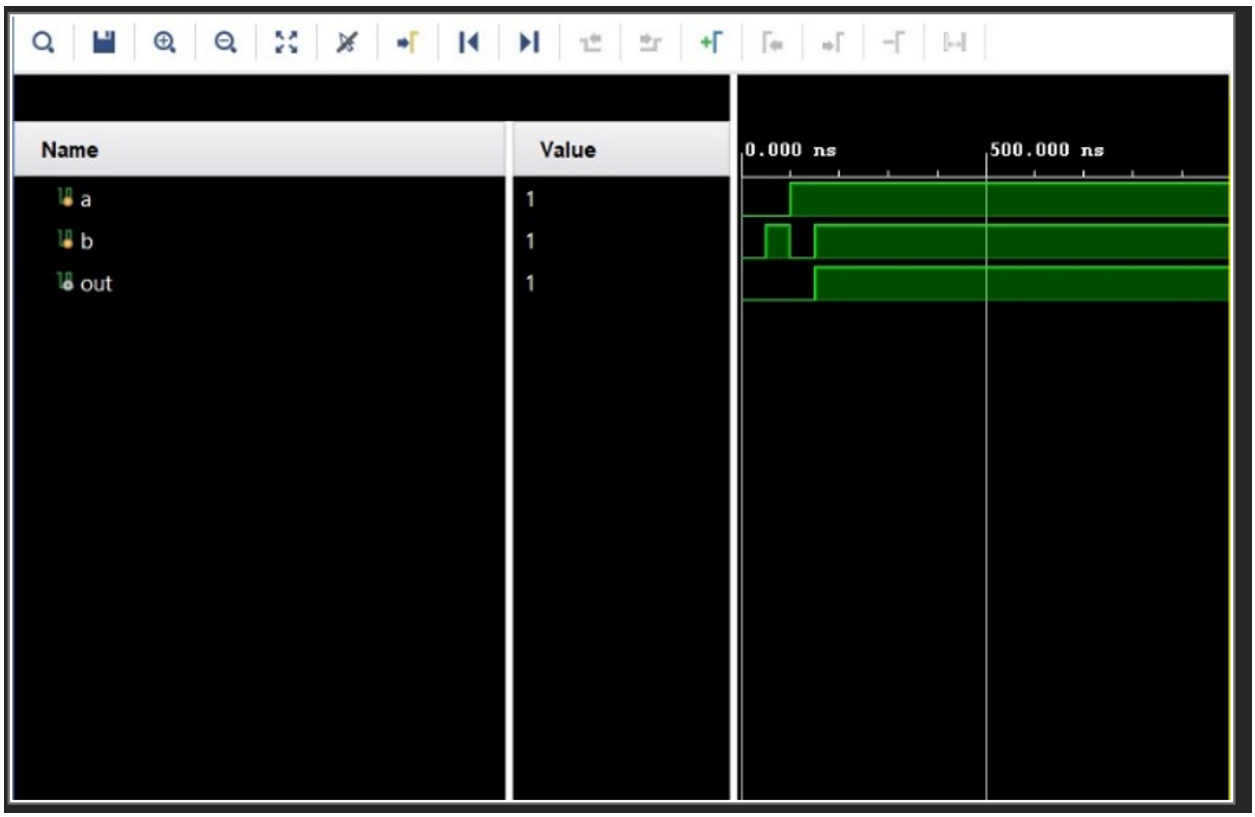
UT EID: hc27426, rsj647

Section: 17540, 17508

Checklist:

Part 1 -

i. Waveform of the structural AND gate (Just the uncommented portion)



ii. Constraint File (Just the uncommented portion)

Switches

iii. set_property PACKAGE_PIN V17 [get_ports {b}]

iv. set_property IOSTANDARD LVCMOS33 [get_ports {b}]

v. set_property PACKAGE_PIN V16 [get_ports {a}]

vi. set_property IOSTANDARD LVCMOS33 [get_ports {a}]

vii.

viii.

ix. ## LEDs

x. set_property PACKAGE_PIN U16 [get_ports {out}]

Part 2 -

iii. Constraint File (Just the uncommented portion)

```
set_property PACKAGE_PIN V17 [get_ports {c}]
set_property IOSTANDARD LVCMOS33 [get_ports {c}]
set_property PACKAGE_PIN V16 [get_ports {b}]
set_property IOSTANDARD LVCMOS33 [get_ports {b}]
set_property PACKAGE_PIN W16 [get_ports {a}]
set_property IOSTANDARD LVCMOS33 [get_ports {a}]
set_property PACKAGE_PIN W17 [get_ports {sw[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sw[3]}]
## LEDs
set_property PACKAGE_PIN U16 [get_ports {d0}]
set_property IOSTANDARD LVCMOS33 [get_ports {d0}]
set_property PACKAGE_PIN E19 [get_ports {d1}]
set_property IOSTANDARD LVCMOS33 [get_ports {d1}]
set_property PACKAGE_PIN U19 [get_ports {d2}]
set_property IOSTANDARD LVCMOS33 [get_ports {d2}]
set_property PACKAGE_PIN V19 [get_ports {d3}]
set_property IOSTANDARD LVCMOS33 [get_ports {d3}]
set_property PACKAGE_PIN W18 [get_ports {d4}]
set_property IOSTANDARD LVCMOS33 [get_ports {d4}]
set_property PACKAGE_PIN U15 [get_ports {d5}]
set_property IOSTANDARD LVCMOS33 [get_ports {d5}]
set_property PACKAGE_PIN U14 [get_ports {d6}]
set_property IOSTANDARD LVCMOS33 [get_ports {d6}]
set_property PACKAGE_PIN V14 [get_ports {d7}]
```

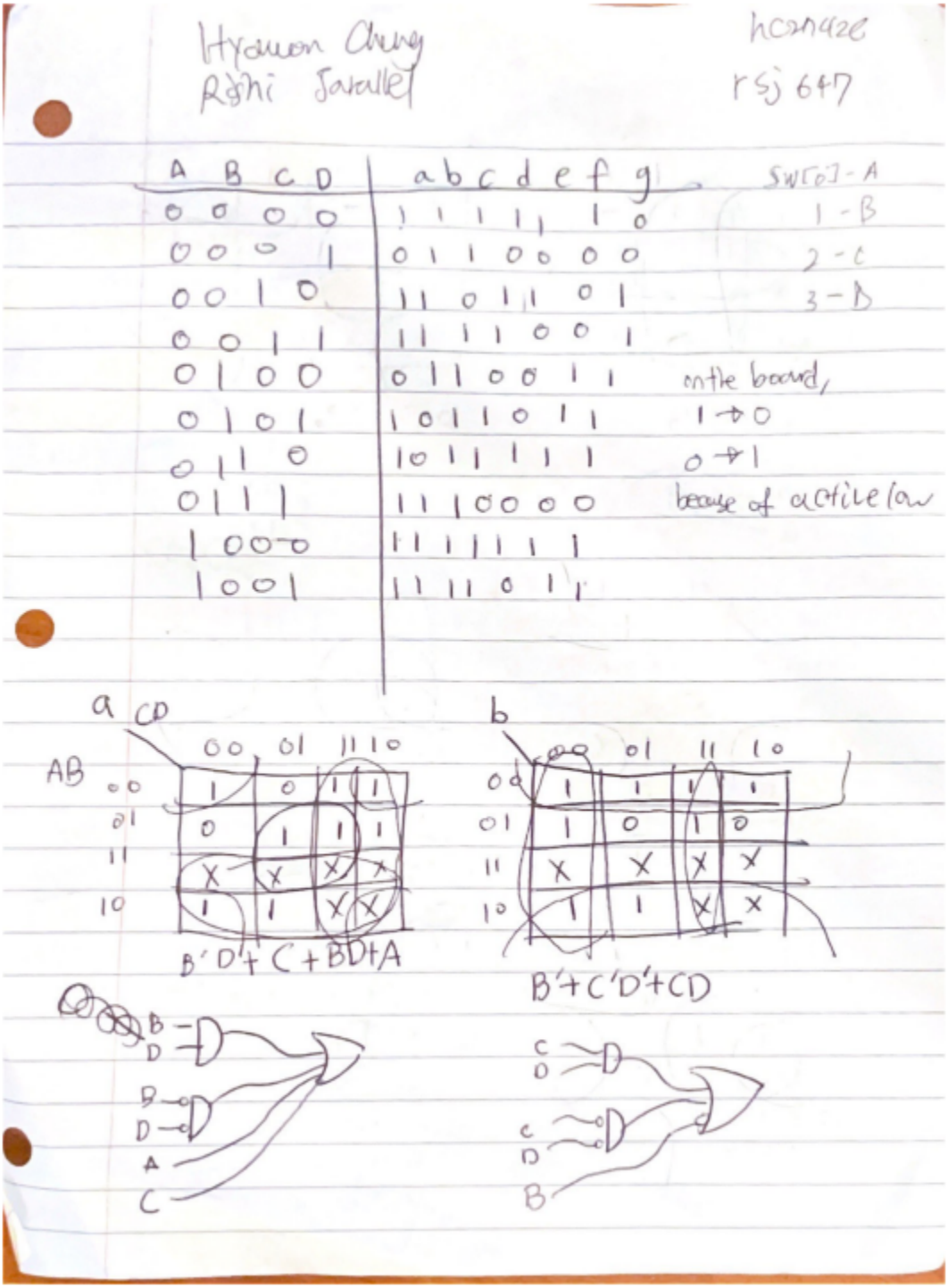
```
set_property IOSTANDARD LVCMOS33 [get_ports {d7}]
```

Part 3 -

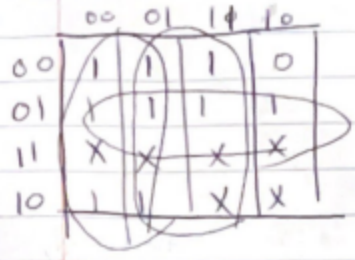
iv. Truth Table of the function
v. K-maps showing minimization of the logic functions (outputs)
vi. Algebraic expression of the minimized logic functions (outputs)
vii. Verilog codes of module and testbench for structural modelling
viii. Simulation waveform for structural modelling
ix. Constraint File (Just the uncommented portion)

Note *The Verilog codes and the uncommented portions of the constraint files should be copied in your lab report and the actual Verilog (.v) and Constraint (.xdc) files need to be zipped and submitted as well on Canvas. You are not allowed to change your Verilog codes after final submission as the TAs may download the submitted codes from Canvas during checkouts. For the truth Table, K-maps minimizations and algebraic expressions, you are free to draw them on paper and then put the pictures in your lab report, but please make sure it is legible for the TAs to grade it properly.*

Part3 IV & V & VI (TT, K-map, Equations)

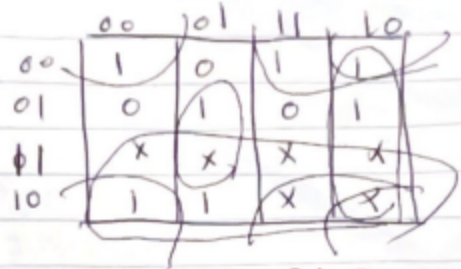


c



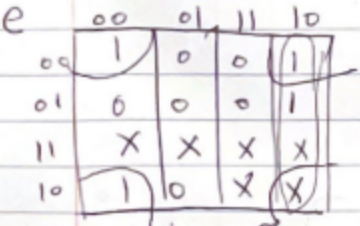
$C'+D+B$

d

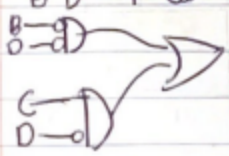


$B'D'+B'C+B'CD$
$+C'D+A$

e

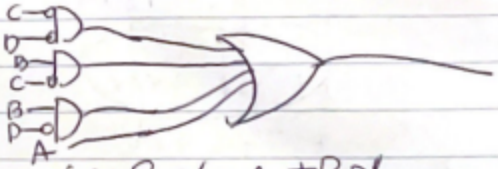


$B'D'+CD$



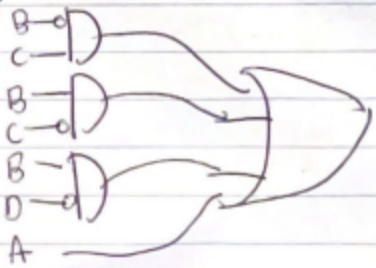
f

$C'D'+BC'+BD'+A$



g

$B'C+BC'+A+BD'$



Part3 - VI Verliog code

```
`timescale 1ns / 1ps



module lcd(
    input [3:0] sw,
    output  AN3, AN2, AN1, AN0,
    output[6:0] seg,
    output dp

    );


   assign AN3 = 1;
  assign  AN2 = 1;
  assign  AN1 = 1;
 assign   AN0 = 0;

assign seg[0]= ((~sw[3])&(~sw[2])&(~sw[1])&sw[0]) | ((~sw[3])&sw[2]&(~sw[1])&(~sw[0]));

assign seg[1]= ((~sw[3])&sw[2]&(~sw[1])&sw[0]) | ((~sw[3])&sw[2]&sw[1]&(~sw[0]));
```

```
assign seg[2]= ((~sw[3])&(~sw[2])&sw[1]&(~sw[0]));

assign seg[3] = ((~sw[3])&(~sw[2])&(~sw[1])&sw[0]) | ((~sw[3])&sw[2]&(~sw[1])&(~sw[0])) | ((~sw[3])&sw[2]&sw[1]&sw[0]);

assign seg[4] = ((~sw[3])&sw[0]) | ((~sw[3])&sw[2]&(~sw[1])) | (~(sw[2])&(~sw[1])&sw[0]);

assign seg[5] = ((~sw[3])&(~sw[2])&sw[0]) | ((~sw[3])&(~sw[2])&sw[1]) | ((~sw[3])&sw[1]&sw[0]);

assign seg[6] = ((~sw[3])&(~sw[2])&(~sw[1]))|((~sw[3])&sw[2]&sw[1]&sw[0]);

assign dp = 1;

endmodule
```

Part3 - VI tb

```
`timescale 1ns / 1ps


module tb_lcd;
    reg [3:0] SW;
    wire [6:0]seg;
    wire AN0;
    wire AN1;
    wire AN2;
    wire AN3;

    lcd uut (
        .sw(SW),
        .seg(seg),
        .AN0(AN0),
        .AN1(AN1),
        .AN2(AN2),
        .AN3(AN3)
    );

    initial begin
    #50;       // initial wait
```

```
// Iterate through all values 0-9

SW[0] = 1'b0;
SW[1] = 1'b0;
SW[2] = 1'b0;
SW[3] = 1'b0;
#50;

SW[0] = 1'b0;
SW[1] = 1'b0;
SW[2] = 1'b0;
SW[3] = 1'b1;
#50;

SW[0] = 1'b0;
SW[1] = 1'b0;
SW[2] = 1'b1;
SW[3] = 1'b0;
#50;

SW[0] = 1'b0;
```

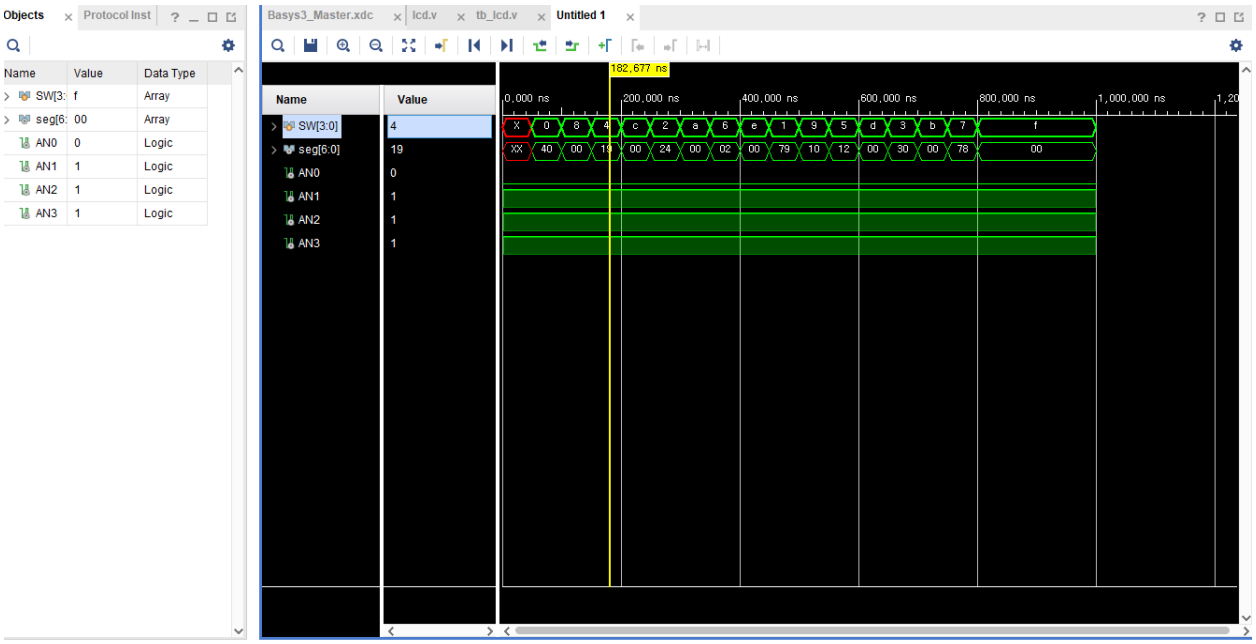
```
SW[1] = 1'b0;
SW[2] = 1'b1;
SW[3] = 1'b1;
#50;
SW[0] = 1'b0;
SW[1] = 1'b1;
SW[2] = 1'b0;
SW[3] = 1'b0;
#50;

SW[0] = 1'b0;
SW[1] = 1'b1;
SW[2] = 1'b0;
SW[3] = 1'b1;
#50;

SW[0] = 1'b0;
SW[1] = 1'b1;
SW[2] = 1'b1;
SW[3] = 1'b0;
#50;
```

```
SW[0] = 1'b0;
SW[1] = 1'b1;
SW[2] = 1'b1;
SW[3] = 1'b1;
#50;

SW[0] = 1'b1;
SW[1] = 1'b0;
SW[2] = 1'b0;
SW[3] = 1'b0;
#50;

SW[0] = 1'b1;
SW[1] = 1'b0;
SW[2] = 1'b0;
SW[3] = 1'b1;
#50;

SW[0] = 1'b1;
SW[1] = 1'b0;
SW[2] = 1'b1;
SW[3] = 1'b0;
```

```
#50;

SW[0] = 1'b1;
SW[1] = 1'b0;
SW[2] = 1'b1;
SW[3] = 1'b1;
#50;
SW[0] = 1'b1;
SW[1] = 1'b1;
SW[2] = 1'b0;
SW[3] = 1'b0;
#50;

SW[0] = 1'b1;
SW[1] = 1'b1;
SW[2] = 1'b0;
SW[3] = 1'b1;
#50;

SW[0] = 1'b1;
SW[1] = 1'b1;
SW[2] = 1'b1;
```

```
    SW[3] = 1'b0;
    #50;

    SW[0] = 1'b1;
    SW[1] = 1'b1;
    SW[2] = 1'b1;
    SW[3] = 1'b1;
    #50;

    end
endmodule
```

Part3 - VII Waveform



Part3 - VIII Constraint file

Clock signal - Uncomment if needed (will be used in future labs)

set_property PACKAGE_PIN W5 [get_ports clk]

set_property IOSTANDARD LVCMOS33 [get_ports clk]

create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]

Switches

set_property PACKAGE_PIN V17 [get_ports {sw[0]}]

set_property IOSTANDARD LVCMOS33 [get_ports {sw[0]}]

set_property PACKAGE_PIN V16 [get_ports {sw[1]}]

set_property IOSTANDARD LVCMOS33 [get_ports {sw[1]}]

set_property PACKAGE_PIN W16 [get_ports {sw[2]}]

set_property IOSTANDARD LVCMOS33 [get_ports {sw[2]}]

set_property PACKAGE_PIN W17 [get_ports {sw[3]}]

set_property IOSTANDARD LVCMOS33 [get_ports {sw[3]}]

#7 segment display

set_property PACKAGE_PIN W7 [get_ports {seg[0]}]

set_property IOSTANDARD LVCMOS33 [get_ports {seg[0]}]

set_property PACKAGE_PIN W6 [get_ports {seg[1]}]

set_property IOSTANDARD LVCMOS33 [get_ports {seg[1]}]

set_property PACKAGE_PIN U8 [get_ports {seg[2]}]

set_property IOSTANDARD LVCMOS33 [get_ports {seg[2]}]

set_property PACKAGE_PIN V8 [get_ports {seg[3]}]

set_property IOSTANDARD LVCMOS33 [get_ports {seg[3]}]

set_property PACKAGE_PIN U5 [get_ports {seg[4]}]

set_property IOSTANDARD LVCMOS33 [get_ports {seg[4]}]

set_property PACKAGE_PIN V5 [get_ports {seg[5]}]

set_property IOSTANDARD LVCMOS33 [get_ports {seg[5]}]

set_property PACKAGE_PIN U7 [get_ports {seg[6]}]

set_property IOSTANDARD LVCMOS33 [get_ports {seg[6]}]

set_property PACKAGE_PIN V7 [get_ports dp]

set_property IOSTANDARD LVCMOS33 [get_ports dp]

set_property PACKAGE_PIN U2 [get_ports {AN0}]

set_property IOSTANDARD LVCMOS33 [get_ports {AN0}]

set_property PACKAGE_PIN U4 [get_ports {AN1}]

set_property IOSTANDARD LVCMOS33 [get_ports {AN1}]

set_property PACKAGE_PIN V4 [get_ports {AN2}]

set_property IOSTANDARD LVCMOS33 [get_ports {AN2}]

set_property PACKAGE_PIN W4 [get_ports AN3]

set_property IOSTANDARD LVCMOS33 [get_ports AN3]