

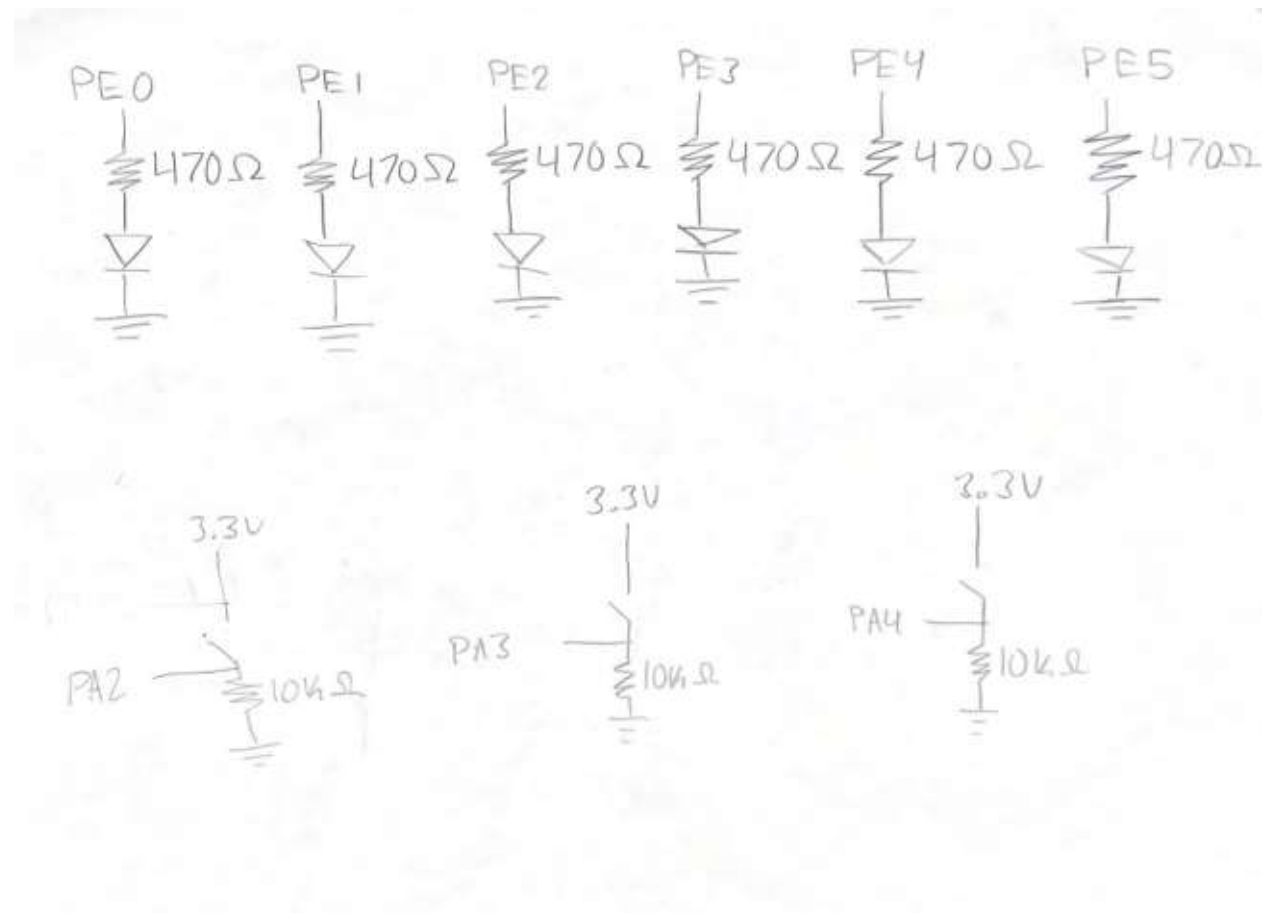
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Valvano

Lab 5 Deliverables

2. Circuit Diagram



3. Logic analyzer and Graded code with EID

Keil v5 EE319KwareFall2022\Lab5_EE319K\Lab5.uvprojx - uVision [Non-Commercial Use License]

File Edit View Project Flash Debug Peripherals Tools SVCS Window Help

Registers

Register	Value
R0	0x0001469
R1	0x200004E8
R2	0x00000000
R3	0x0001459
R4	0x0001D94
R5	0x0001D94
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x200004E8
R14 (LR)	0x000072D
R15 (PC)	0x0001468
xPSR	0x61000000

Logic Analyzer

Setup... Load... Save... Min Time 29.025 us Max Time 14.20923 s Grid 1 s Zoom In Out All Min/Max Auto Undo Update Screen Stop Clear Transition Prev Next Jump to Code Trace Signal Info Show Cycles Amplitude Cursor Timestamps Enable

Core

Thread Privileged MSP 2322 Sec 0.00014512

Command

Running with Code Size Limit: 32K

Load "C:\\Keil_v5\\EE319KwareFall2022\\Lab5_EE319K\\Lab5.axf"

WS 1, 'S

WS 1, 'input

WS 2, 'FSM[S].Next(input)

WS 2, 'input

LA (PORTE & 0x00000001)

LA (PORTE & 0x00000002) >> 1

LA (PORTE & 0x00000004) >> 2

LA (PORTE & 0x00000008) >> 3

LA (PORTE & 0x00000010) >> 4

LA (PORTE & 0x00000020) >> 5

LA (PORTF & 0x00000002) >> 1

LA (PORTF & 0x00000004) >> 2

LA (PORTF & 0x00000008) >> 3

LA (PORTF & 0x00000010) >> 4

LA (PORTA & 0x00000004) >> 2

LA (PORTA & 0x00000008) >> 3

LA (PORTA & 0x00000010) >> 4

LA (PORTA & 0x00000020) >> 5

LA (PORTA & 0x00000040) >> 6

LA (PORTA & 0x00000080) >> 7

LA (PORTA & 0x00000100) >> 8

LA (PORTA & 0x00000200) >> 9

LA (PORTA & 0x00000400) >> 10

LA (PORTA & 0x00000800) >> 11

LA (PORTA & 0x00001000) >> 12

LA (PORTA & 0x00002000) >> 13

LA (PORTA & 0x00004000) >> 14

LA (PORTA & 0x00008000) >> 15

LA (PORTA & 0x00010000) >> 16

LA (PORTA & 0x00020000) >> 17

LA (PORTA & 0x00040000) >> 18

LA (PORTA & 0x00080000) >> 19

LA (PORTA & 0x00100000) >> 20

LA (PORTA & 0x00200000) >> 21

LA (PORTA & 0x00400000) >> 22

LA (PORTA & 0x00800000) >> 23

LA (PORTA & 0x01000000) >> 24

LA (PORTA & 0x02000000) >> 25

LA (PORTA & 0x04000000) >> 26

LA (PORTA & 0x08000000) >> 27

LA (PORTA & 0x10000000) >> 28

LA (PORTA & 0x20000000) >> 29

LA (PORTA & 0x40000000) >> 30

LA (PORTA & 0x80000000) >> 31

LA (PORTA & 0xFFFFFFFF) >> 32

UART #1

Lab 5, Fall 2022 EID1=DND663, EID2=HC27426

Option B2, connect LEDs to PE5-PE0, switches to PA4-2, walk LED PF321

When all inputs true, ... South, Walk, West, South, Walk, West, ...

Activate all three inputs.

Initialization, good, Score=4

Looking for Go South

Go Walk

All stop

Wait Walk

All stop

Wait Walk

All stop

Wait Walk

All stop

Go West

Wait West

All stop

Go South

Found Go South, Score= 11

Looking for Go Walk

Wait South

All stop

Go Walk

Found Go Walk, Score= 18

Looking for Go West

All stop

Wait Walk

All stop

Wait Walk

All stop

Go West

Found Go West, Finished, Score= 25

ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE COVTOFILE DEFINE DIR Display Enter

Call Stack + Locals UART #1 Watch 1 Watch 2 Memory 1

Simulation

t1: 14.6956639 sec

4. FSM Graph

