HYOJONG KIM

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OBJECTIVE

Looking for a **full-time research / software engineering position**.

EDUCATION

Georgia Institute of Technology, Atlanta, Georgia, USA (Expected) *Dec 2019*
Ph.D. in Computer Science (Advisor: Dr. Hyesoon Kim)
Research topic: high-performance computing, memory systems, processing in memory, GPU

Seoul National University, Seoul, South Korea *Aug 2012*
Bachelor of Science in Electrical Engineering and Computer Science
Thesis: Implementation of profiling techniques for process offloading for mobile-cloud-computing (MCC)

RESEARCH/WORK EXPERIENCE

Georgia Institute of Technology, Atlanta, Georgia, USA *Aug 2012 – Present*
Graduate Research Assistant (Advisor: Dr. Hyesoon Kim)
Projects: System modeling of CPU-GPU for 3D memory systems, Performance and Energy modeling of processing-in-memory (PIM) architecture, Virtual address support for PIM architecture

AMD Research, Sunnyvale, California, USA *May 2015 – Aug 2016*
Co-op Engineer (Supervisor: Dr. Nuwan Jayasena)
Project: Virtual address support for PIM architecture

Sandia National Laboratories, Albuquerque, New Mexico, USA *May 2013 – Aug 2013*
Summer Research Intern (Supervisor: Dr. Arun Rodrigues)
Project: SST-MacSim system modeling of CPU-GPU for 3D-stacked memory

Samsung Electronics – *System LSI* *Dec 2011 – Feb 2012*
Undergraduate Intern
Project: Advanced bus system modeling for an application processor

Georgia Institute of Technology, Atlanta, Georgia, USA *May 2011 – Aug 2011*
Undergraduate Research Intern (Supervisor: Dr. Minjang Kim, Dr. Hyesoon Kim)
Project: Case studies for a post-analyzer of data dependence profiler

Vixell Co., Ltd. – *In Fulfillment of Military Service* *Jun 2009 – Dec 2010*
Software Engineer
Project: Electronic toll-collection system development

Citus Co., Ltd. – *In Fulfillment of Military Service* *Nov 2007 – Jun 2009*
Software Engineer
Project: 3D car navigation system development

HONORS/AWARDS

Best paper award at the 1st International Symposium on Memory Systems (MEMSYS) for the paper Understanding Energy Aspect of Processing Near Memory for HPC Workloads, **Hyojong Kim**, Hyesoon Kim, Sudhakar Yalamanchili, and Arun Rodrigues.

Scholarship for the Distinguished Undergraduates *Mar 2005 – Aug 2012*
Korea Foundation of Advanced Studies

PATENTS

Per-page control of physical address space distribution among memory modules. Nuwan S. Jayasena, **Hyojong Kim**, and Hyesoon Kim. US Patent Pub. No. 2018/0246814.

PUBLICATIONS

1. Jie Zhang, Miryeong Kwon, **Hyojong Kim**, Hyesoon Kim, and Myoungsoo Jung. FlashGPU: Placing New Flash Next to GPU Cores, *Design Automation Conference (DAC)*, 2019.
2. Lifeng Nai, Ramyad Hadidi, He Xiao, **Hyojong Kim**, Jaewoong Sim, and Hyesoon Kim. Thermal-Aware Processing-in-memory Instruction Offloading, *Journal of Parallel and Distributed Computing (JPDC)*, 2019.
3. **Hyojong Kim**, Ramyad Hadidi, Lifeng Nai, Hyesoon Kim, Nuwan Jayasena, Yasuko Eckert, Onur Kayiran, and Gabriel Loh. CODA: Enabling Co-location of Computation and Data for Multiple GPU Systems, *ACM Transactions on Architecture and Code Optimization (TACO)*, 2018. **Presented at the HiPEAC (European Network on High Performance and Embedded Architecture and Compilation) conference, 2019**.
4. Prasun Gera, **Hyojong Kim**, Hyesoon Kim, Sunpyo Hong, Vinod George, and Chi-Keung (CK) Luk. Performance Characterisation and Simulation of Intel's Integrated GPU Architecture, *International Symposium on Performance Analysis of Systems and Software (ISPASS)*, 2018
5. Lifeng Nai, Ramyad Hadidi, He Xiao, **Hyojong Kim**, Jaewoong Sim, and Hyesoon Kim. CoolPIM: Thermal-Aware Source Throttling for Efficient PIM Instruction Offloading, *IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, 2018.
6. Ramyad Hadidi, Lifeng Nai, **Hyojong Kim**, and Hyesoon Kim. CAIRO: A Compiler-Assisted Technique for Enabling Instruction-Level Offloading of Processing-In-Memory, *ACM Transactions on Architecture and Code Optimization (TACO)*, 2018.
7. Pranith Kumar, Prasun Gera, **Hyojong Kim**, and Hyesoon Kim. Louvre: Light-weight Ordering Using Versioning for Release Consistency, *arXiv:1710.10746*, 2017.
8. Jen-Cheng Huang, Lifeng Nai, Pranith Kumar, **Hyojong Kim**, and Hyesoon Kim. SimProf: A Sampling Framework for Data Analytic Workloads, *International Parallel & Distributed Processing Symposium (IPDPS)*, 2017.
9. Lifeng Nai, Ramyad Hadidi, Jaewoong Sim, **Hyojong Kim**, Pranith Kumar, and Hyesoon Kim. GraphPIM: Enabling Instruction-Level PIM Offloading in Graph Computing Frameworks, *International Symposium on High Performance Computer Architecture (HPCA)*, 2017.
10. **Hyojong Kim**, Hyesoon Kim, Sudhakar Yalamanchili, and Arun Rodrigues. Understanding Energy Aspect of Processing Near Memory for HPC Workloads, *International Symposium on Memory Systems (MEMSYS)*, 2015. ***Best Paper Award***
11. **Hyojong Kim**, Hongyeol Lim, Dilan Manatunga, Hyesoon Kim, and Gi-Ho Park. Accelerating application start-up with Nonvolatile Memory in Android Systems, *IEEE Micro*, 2015.

12. Chad Kersey, Sudhakar Yalamanchili, **Hyojong Kim**, Nimit Nigania, and Hyesoon Kim. Harmonica: An FPGA-based Data Parallel Soft Core, *International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, 2014.
13. Joo Hwan Lee, Kaushik Patel, Nimit Nigania, **Hyojong Kim**, and Hyesoon Kim. OpenCL Performance Evaluation on Modern Multi Core CPUs, *Parallel and Distributed Processing Symposium Workshops & PhD Forum (IPDPSW)*, 2013.

PROFESSIONAL SERVICES

Conference Reviewer

- International Conference on Supercomputing (ICS) 2015

Journal Reviewer

- IEEE Computer Architecture Letters (CAL) 2019
- IEEE Computer Architecture Letters (CAL) 2018
- IEEE Computer Architecture Letters (CAL) 2017

SKILLS

- **Programming Languages:** C/C++, Python
- **Select Graduate Courses:** High Performance Computer Architecture, Advanced Microarchitecture, Advanced Topics in Memory Systems, Algorithms and Computability

OPEN SOURCE SOFTWARE

- **MacSim: a heterogeneous architecture timing model simulator**
  - Added virtual memory support for x86 and GPU architectures.
  - Modeled Intel GEN GPU architecture in MacSim.
  - Integrated MacSim with SST framework.