AVR1012: XMEGA A Schematic Checklist

Features

- **Power Supplies**
- **Backup battery for XMEGA A3B**
- **Reset circuit**
- **Clocks and crystal oscillators**
- **External bus interface**
- **JTAG and PDI**

1 Introduction

A good hardware design comes from a proper schematic. Since XMEGA™ A devices have a fair number of pins and functions, the schematic for these devices can be large and quite complex.

This application note describes a common checklist which should be used when starting and reviewing the schematics for a XMEGA A design.

8-bit AVR® Microcontrollers

Application Note

Rev. 8278A-AVR-12/09

2 Power Supplies

2.1 Power Supply Connections

Figure 2-1. Power Supply schematic

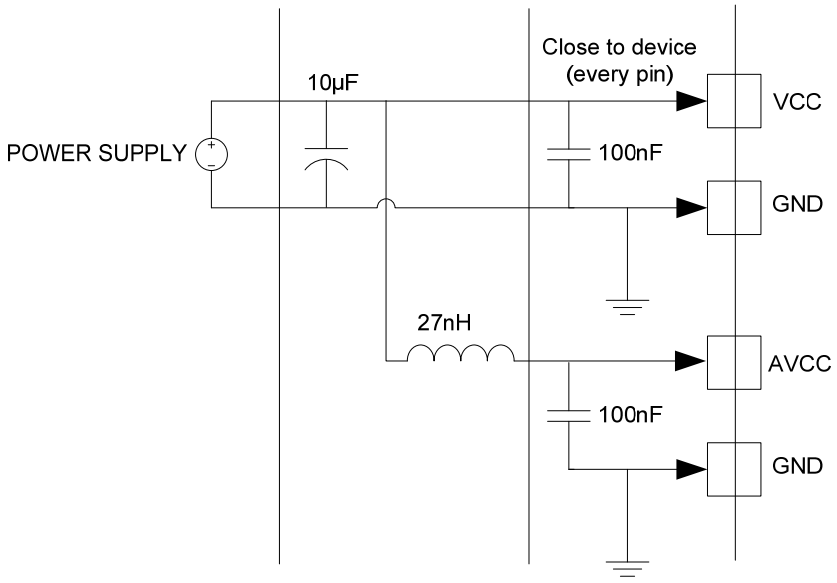


Table 2-1. Power Supply Connections

Signal name	Recommended pin connection	Description
VCC	1.6 V to 3.6 V Decoupling/filtering capacitors 100 nF[1][2] and 10 µF[1]	Digital supply voltage
AVCC	1.6 V to 3.6 V Decoupling/filtering capacitors 100 nF[1][2] and 10 µF[1] Inductor improves power filtering 27nH[1][3]	Analog supply voltage
GND		Ground

1. These values are given only as a typical example.
2. Decoupling capacitor should be placed close to the device for each supply pin pair in the signal group, low ESR caps should be used for better decoupling.
3. The Inductor value is decided by the formula as below $f_{cut} = \frac{1}{2\pi\sqrt{LC}}$

Notes: Assume cut-off frequency $f_{cut} = 3.2MHz$ and $C = 100nF$, so get $L = 27nH$

2.2 Battery Backup Module Connections

This section is only for the application which uses the battery backup function of the XMEGA A3B devices, such as the ATxmega256A3B. Upon main power loss the device will detect this and automatically switch the Battery Backup Module to be powered from the VBAT pin.

Figure 2-2. Battery Backup Module Schematic

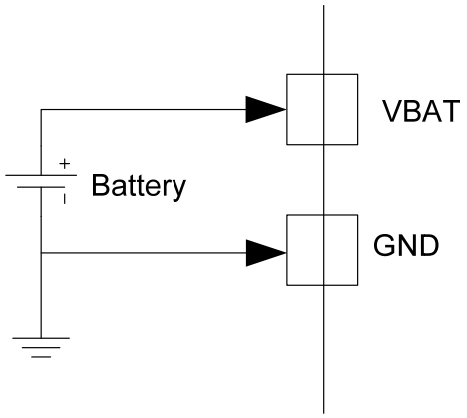


Table 2-2. Battery Backup Module Connections

Signal name	Recommended pin connection	Description
VBAT	1.8 V to 3.6 V	Battery Backup Module supply voltage
GND		Ground

Notes: To run the Real Time Counter a 32.768 kHz crystal oscillator must be connected between the TOSC1 and TOSC2 pins when running from VBAT.

2.3 External Analog Reference Connections

The following schematic checklist is only necessary if the design is using the external analog reference. If the internal reference is used, the circuit is not necessary.

Figure 2-3. External Analog Reference schematic with Two References

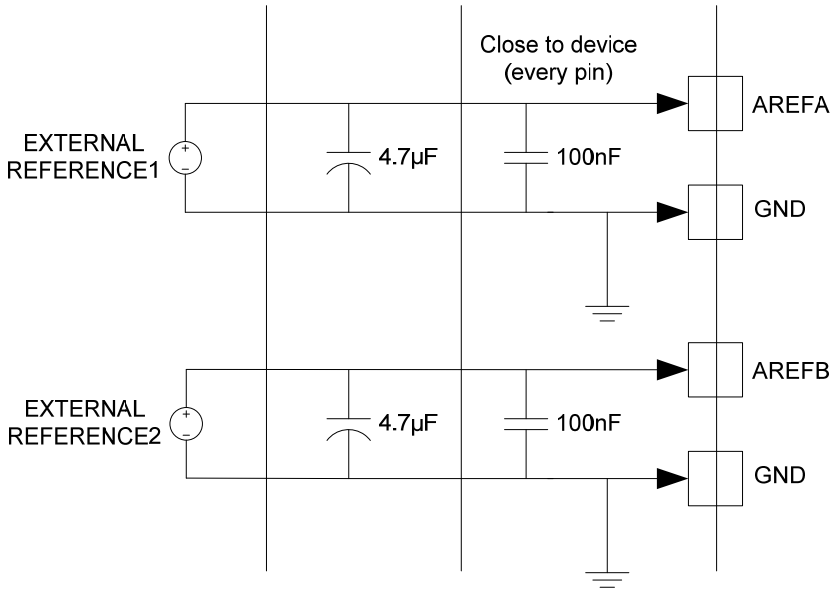


Figure 2-4. External Analog Reference schematic with One Reference

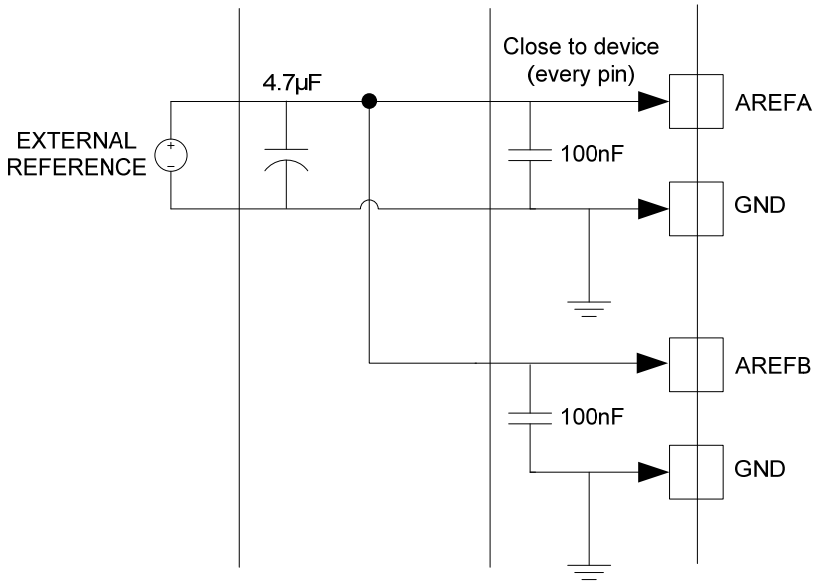


Table 2-3. External Analog Reference Connections

Signal name	Recommended pin connection	Description
AREFA	1.0V to AVCC-0.6V for ADC 1.1V to AVCC-0.6V for DAC Decoupling/filtering capacitors 100 nF[1][2] and 4.7 µF[1]	External reference from AREF pin on PORT A.
AREFB	1.0V to AVCC-0.6V for ADC 1.1V to AVCC-0.6V for DAC Decoupling/filtering capacitors 100 nF[1][2] and 4.7 µF[1]	External reference from AREF pin on PORT B.
GND		Ground

Notes
1. These values are given only as a typical example.
2. Decoupling capacitor should be placed close to the device for each supply pin pair in the signal group.

3 External Reset circuit

The external reset circuit is connected to RESET pin when the external reset function is used. If internal reset is used, the circuit is not necessary. The reset switch also can be removed, if the manual reset is not necessary.

Figure 3-1. External Reset circuit example schematic

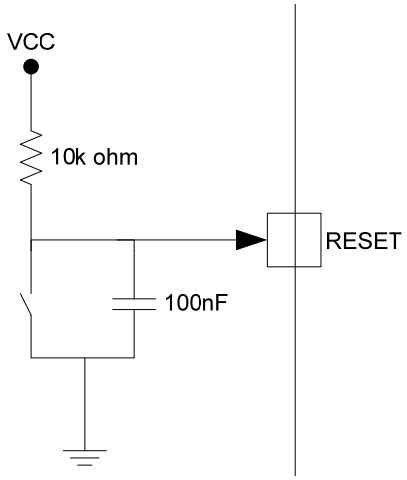


Table 3-1. Reset circuit Connections

Signal name	Recommended pin connection	Description
RESET	Reset low level threshold voltage VCC = 2.7 - 3.6V: Below 0.45*VCC VCC = 1.6 - 2.7V: Below 0.42*VCC	Reset pin
Notes	This pull-up resistor makes sure that reset does not go low unintended. When the PDI programming and debugging is used, the reset line is used as clock. The reset pull-up should be 10k or weaker, or be removed altogether. Any reset capacitors should be removed if PDI programming and debugging is used. Other external reset sources should be disconnected.	

4 Clocks and crystal oscillators

4.1 External clock source

Figure 4-1. External clock source example schematic

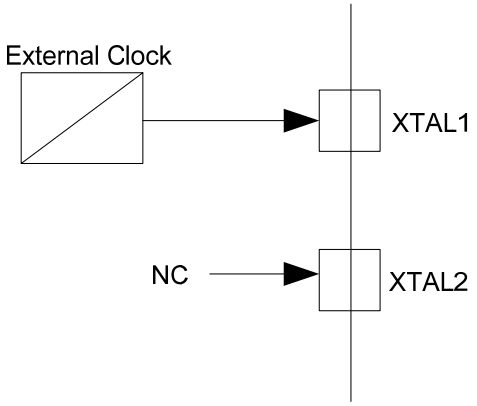


Table 4-1. External clock source Connections

Signal name	Recommended pin connection	Description
XTAL1	XTAL1 is used as input for an external clock signal	Input for inverting Oscillator pin 1
XTAL2	Can be left unconnected or used as GPIO	

4.2 Crystal oscillator

Figure 4-2. Crystal oscillator example schematic

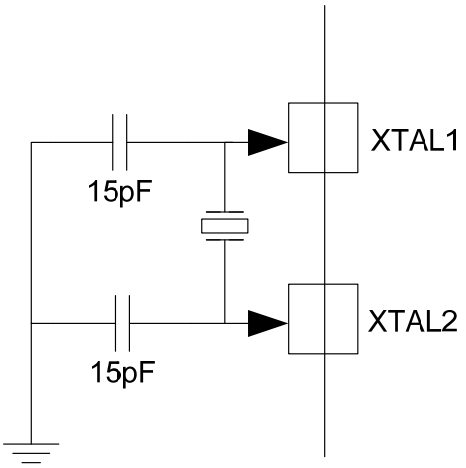


Table 4-2. Crystal oscillator checklist

Signal name	Recommended pin connection	Description
XTAL1	Biasing capacitor 15 pF[1][2]	External crystal between 0.4 MHz to 16 MHz
XTAL2	Biasing capacitor 15 pF[1][2]	

Notes
1. These values are given only as a typical example. Please refer to the crystal datasheet to determine the capacitor value for the crystal used or refer to the application note “AVR1003: Using the XMEGA Clock System”.
2. Decoupling capacitor should be placed close to the device for each supply pin pair in the signal group.

4.3 External Real Time Oscillator

The Low-frequency Crystal Oscillator is optimized for use with a 32.768 kHz watch crystal. When selecting crystals, load capacitance and crystal’s Equivalent Series Resistance, ESR must be taken into consideration. Both values are specified by the crystal vendor.

XMEGA oscillator is optimized for very low power consumption, and thus when selecting crystals, see Table 4-3 for maximum ESR recommendations on 9 pF and 12.5 pF crystals.

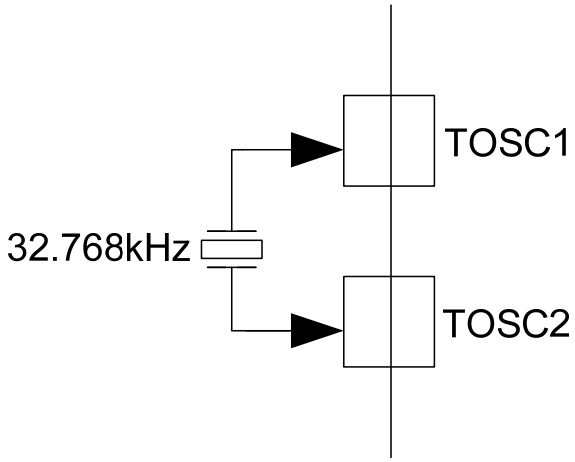
The Low-frequency Crystal Oscillator provides an internal load capacitance of typical 8.0 pF. Crystals with recommended 8.0 pF load capacitance can be without external capacitors as shown in Figure 4-3.

Table 4-3. Maximum ESR Recommendation for 32.768 kHz Watch Crystal

Crystal CL (pF)	Max ESR [kΩ][1]
9.0	65
12.5	30

Note: 1. Maximum ESR is typical value based on characterization

Figure 4-3. External real time oscillator without biasing capacitor



Crystals specifying load capacitance (CL) higher than 8.0 pF, require external capacitors applied as described in Figure 4-4.

To find suitable load capacitance for a 32.768 kHz crysal, please consult the crystal datasheet.

Figure 4-4. External real time oscillator with biasing capacitor

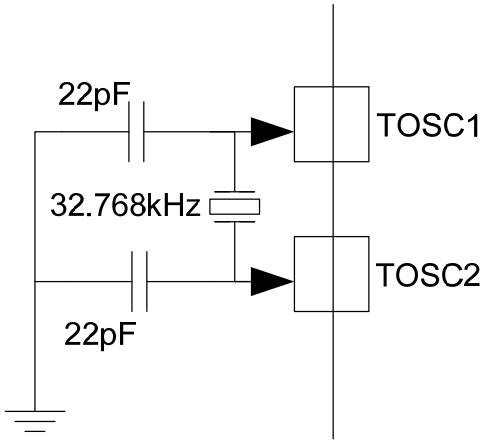


Table 4-4. External real time oscillator checklist

Signal name	Recommended pin connection	Description
TOSC1	Biasing capacitor 22 pF[1][2]	Timer Oscillator pin 1
TOSC2	Biasing capacitor 22 pF[1][2]	Timer Oscillator pin 2

Notes
1. These values are given only as a typical example. Please refer to the crystal datasheet to determine the capacitor value for the crystal used or refer to the application note “AVR1003: Using the XMEGA Clock System”.
2. Decoupling capacitor should be placed close to the device for each supply pin pair in the signal group.

5 External bus interface

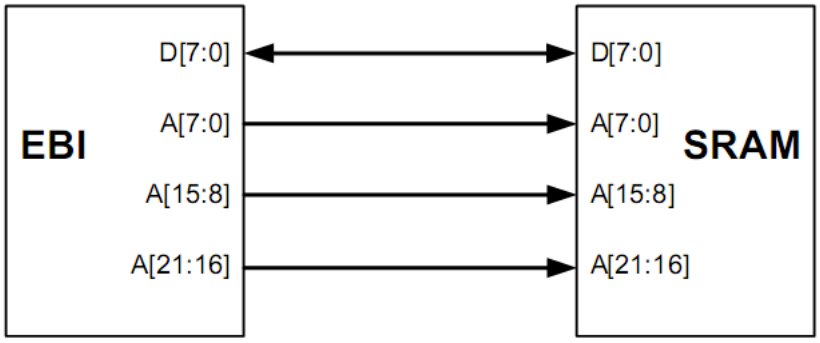
The External Bus Interface (EBI) is the interface for connecting external peripheral and memory to access it through the data memory space.

The EBI can interface external SRAM, SDRAM, and/or peripherals such as LCD displays and other memory mapped devices.

5.1 SRAM Configuration

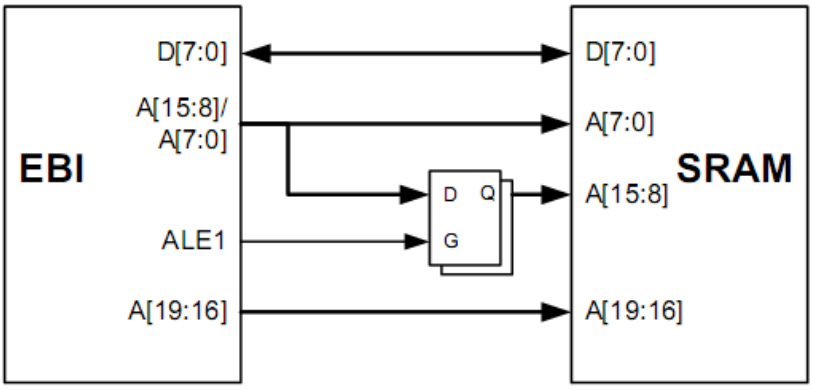
5.1.1 8-bit SRAM No Multiplexing

Figure 5-1. 8-bit SRAM No Multiplexing Connection



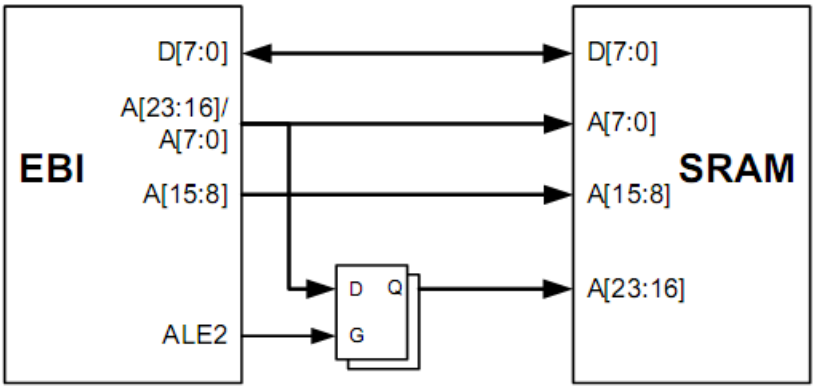
5.1.2 8-bit SRAM Multiplexing Address Byte 0 and 1

Figure 5-2. 8-bit SRAM Multiplexing address byte 0 and 1 Connection



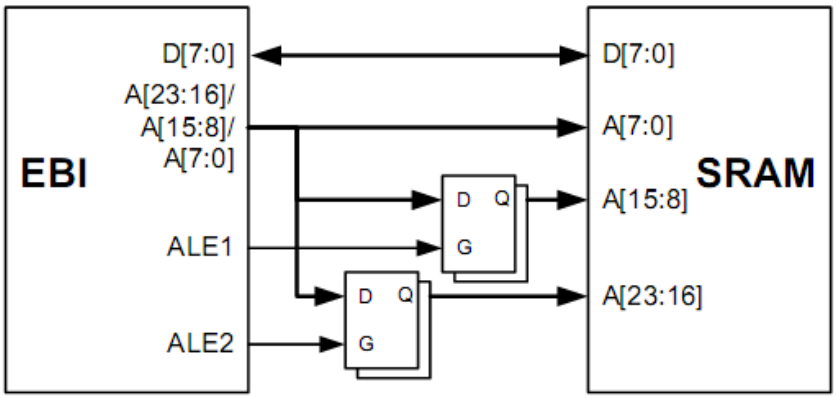
5.1.3 8-bit SRAM Multiplexing Address Byte 0 and 2

Figure 5-3. 8-bit SRAM Multiplexing address byte 0 and 2 Connection



5.1.4 8-bit SRAM Multiplexing Address Byte 0, 1 and 2

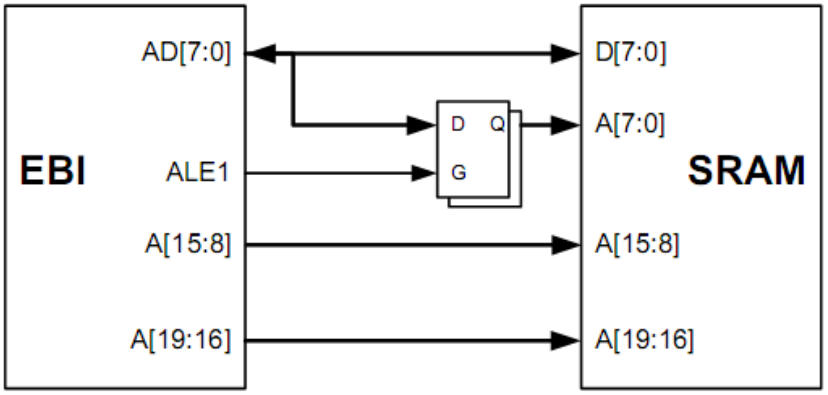
Figure 5-4. 8-bit SRAM Multiplexing address byte 0 ,1 and 2 Connection



5.2 The SRAM Low Pin Count (LPC) configuration

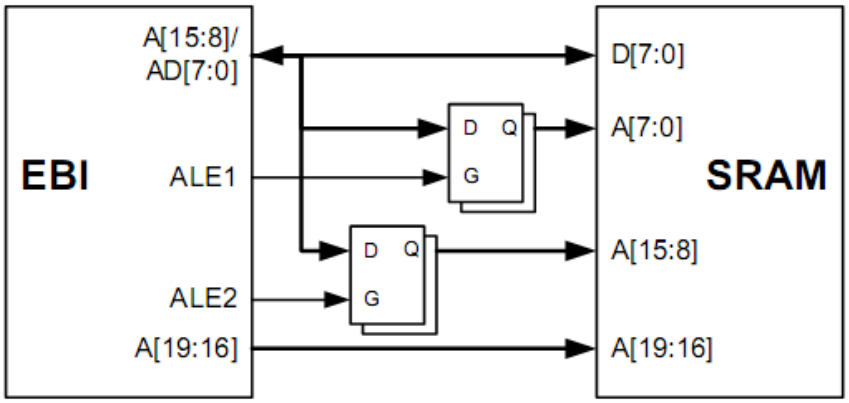
5.2.1 8-bit SRAM Multiplexing Data with Address Byte 0

Figure 5-5. 8-bit SRAM Multiplexing Data with Address Byte 0 Connection



5.2.2 8-bit SRAM Multiplexing Data with Address Byte 0 and 1

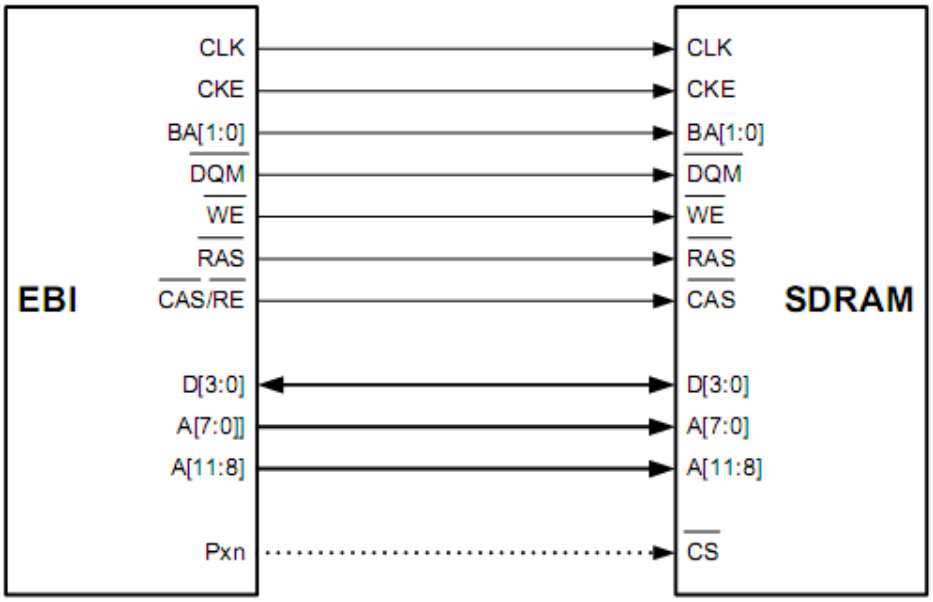
Figure 5-6. 8-bit SRAM Multiplexing Data with Address Byte 0 and 1 Connection



5.3 SDRAM Configuration

5.3.1 4-bit SDRAM 3-Port EBI Configuration

Figure 5-7. 4-bit SDRAM 3-Port EBI Configuration



6 JTAG and PDI ports

6.1 JTAG port interface

Figure 6-1. JTAG port interface example schematic

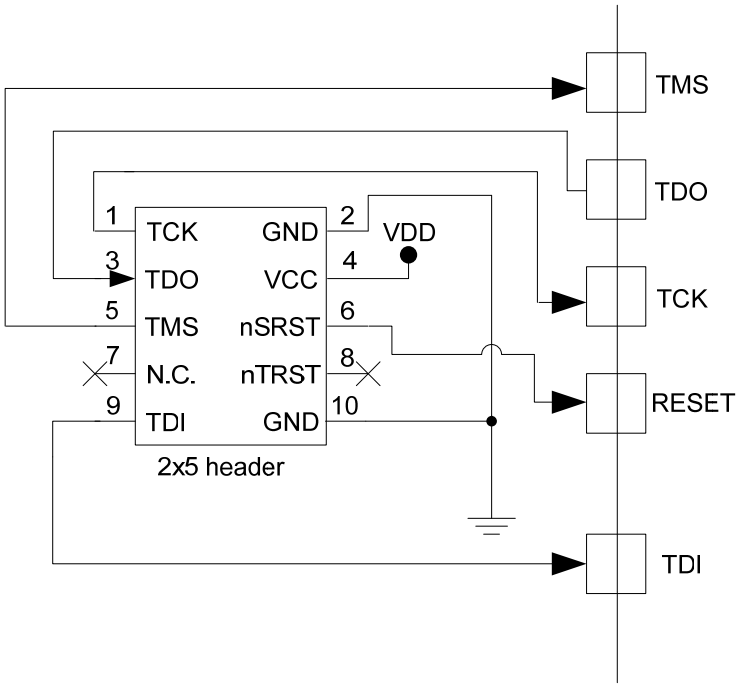


Table 6-1. JTAG port interface checklist

Signal name	Description
TMS	Test mode select, sampled on rising TCK.
TDO	Test data output, driven on falling TCK.
TCK	Test clock, fully asynchronous to system clock frequency.
RESET	Device external reset line.
TDI	Test data input, sampled on rising TCK.

6.2 PDI port interface

Figure 6-2. PDI port interface example schematic

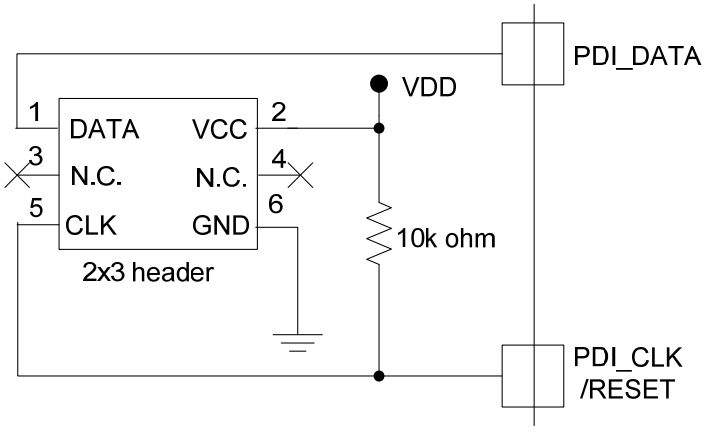


Table 6-2. PDI port interface checklist

Signal name	Recommended pin connection	Description
PDI_CLK	This pull-up resistor makes sure that reset does not go low unintended. When the PDI programming and debugging is used, the reset line is used as clock. The reset pull-up should be 10k or weaker, or be removed altogether. Any reset capacitors should be removed if PDI programming and debugging is used. Other external reset sources should be disconnected.	PDI clock input / Reset pin
PDI_DATA		PDI_DATA: PDI data input/output

7 Suggested reading

7.1 Device datasheet

The device datasheet contains block diagrams of the peripherals and details about implementing firmware for the device. The datasheet is available on http://www.atmel.com/AVR in the Datasheets section.

7.2 Evaluation kit schematic

The evaluation kit ATAVRXPLAIN contains the full schematic for the board; it can be used as a reference design. The schematic is available on http://www.atmel.com/AVR in the Tools & Software section.

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