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9	28.03.2022	<ol style="list-style-type: none"> 1. Write a winspice code to verify the functionality of given bicmos inverter circuit using default model parameters for the transistor. 2. Write a winspice code to verify the functionality of NOR based SR Latch 	
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U19EC046 | DIC LAB 1

AIM

To plot the forward and reverse characteristics of PN Junction Diode for the given Parameters.
Also extract the following parameters :

1. Forward Resistance and Cut-in Voltage from forward characteristics.
2. Reverse resistance from reverse characteristics.
3. Reverse Recovery Time of the Diode (trr).

THEORY

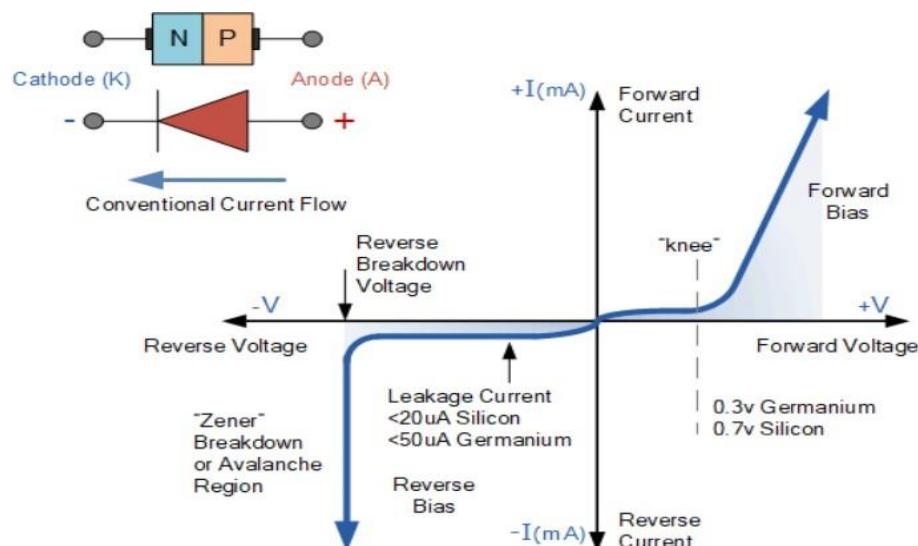
Introduction

A PN Junction Diode is one of the simplest semiconductor devices around, and which has the electrical characteristic of passing current through itself in one direction only. However, unlike a resistor, a diode does not behave linearly with respect to the applied voltage. Instead it has an exponential current-voltage (I-V) relationship and therefore we can not describe its operation by simply using an equation such as Ohm's law.

If a suitable positive voltage (forward bias) is applied between the two ends of the PN junction, it can supply free electrons and holes with the extra energy they require to cross the junction as the width of the depletion layer around the PN junction is decreased.

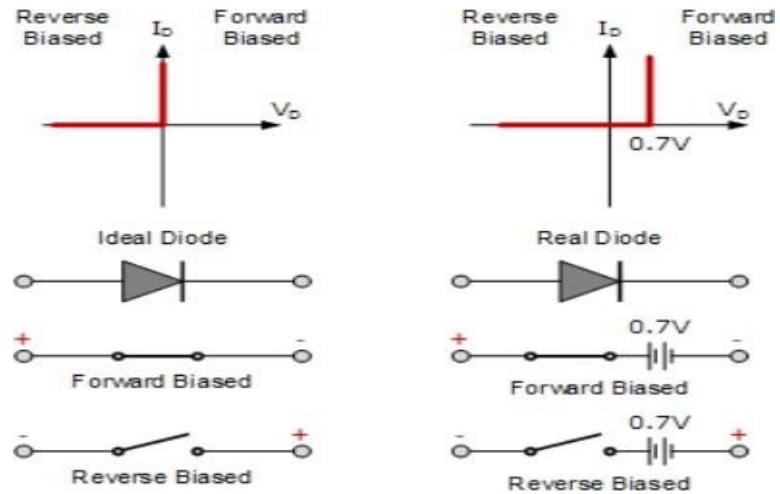
By applying a negative voltage (reverse bias) results in the free charges being pulled away from the junction resulting in the depletion layer width being increased. This has the effect of increasing or decreasing the effective resistance of the junction itself allowing or blocking the flow of current through the diodes pn-junction.

Then the depletion layer widens with an increase in the application of a reverse voltage and narrows with an increase in the application of a forward voltage. This is due to the differences in the electrical properties on the two sides of the PN junction resulting in physical changes taking place. One of the results produces rectification as seen in the PN junction diodes static I-V (current-voltage) characteristics.

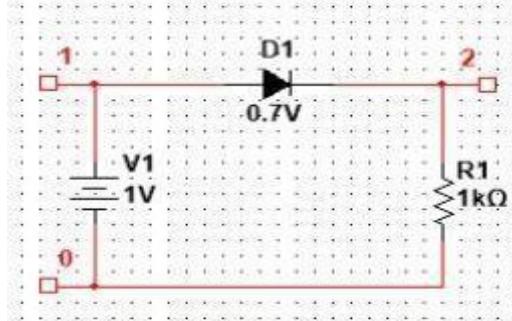


There are two operating regions and three possible "biasing" conditions for the standard Junction Diode and these are:

1. Zero Bias – No external voltage potential is applied to the PN junction diode.
2. Reverse Bias – The voltage potential is connected negative, (-ve) to the P-type material and positive, (+ve) to the N-type material across the diode which has the effect of Increasing the PN junction diode's width.
3. Forward Bias – The voltage potential is connected positive, (+ve) to the P-type material and negative, (-ve) to the N-type material across the diode which has the effect of Decreasing the PN junction diodes width.



Circuit Diagram



SPICE CODE

1. FORWARD CHARACTERISTICS

```
*Diode Forward ch/cs

.Model mod1 D (IS=1E-12 RS=10 CJO=5P TT=10N BV=10)
D1 2 0 mod1

R1 1 2 1k
V1 1 0 dc 1
.dc V1 0 5 0.05
.control
run
* plot v(1)-v(2)
plot -I(V1)
.endc
.end
```

2. REVERSE CHARACTERISTICS

```
* Diode Reverse ch/cs

.Model mod1 D (IS=1E-12 RS=10 CJO=5P TT=10N BV=10)
D1 2 0 mod1

R1 1 2 1k
V1 1 0 dc 1
.dc V1 -5 0 0.05
.control
```

```

run
plot -I(V1)
.endc
.end

```

3. REVERSE RECOVERY TIME

```

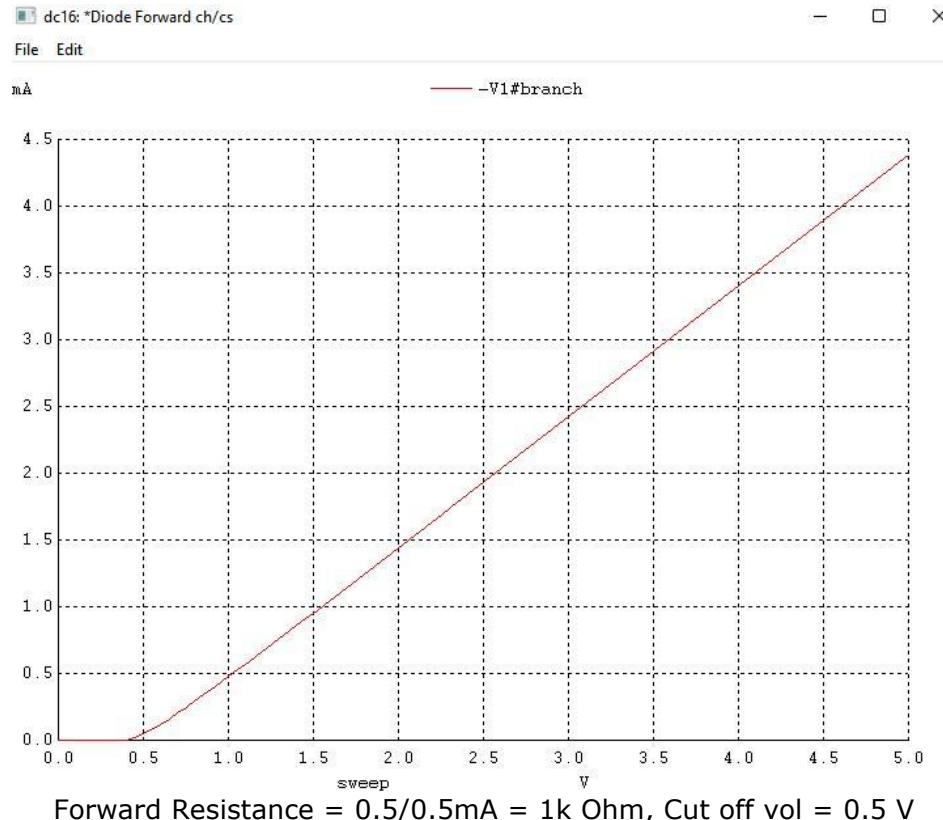
* Reverse recovery time of diode
.MODEL SWITCH D (IS=1E-12 RS=10 CJO=5P TT=10N BV=10)
V1 1 0 pulse (5 -3 10N 0.05N 0.05N 30N 50N)
RS 1 2 1K
D1 2 3 Switch
Vo 3 0 0

.TRAN 1N 50N
.control
run
plot v(1) v(2)
plot i(Vo)
.endc
.end

```

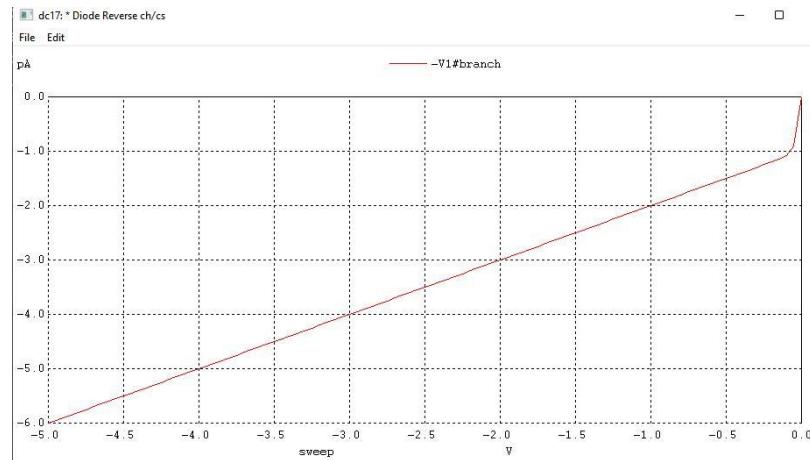
SIMULATION RESULTS AND PRACTICAL CALCULATIONS

1. FORWARD CHARACTERISTICS



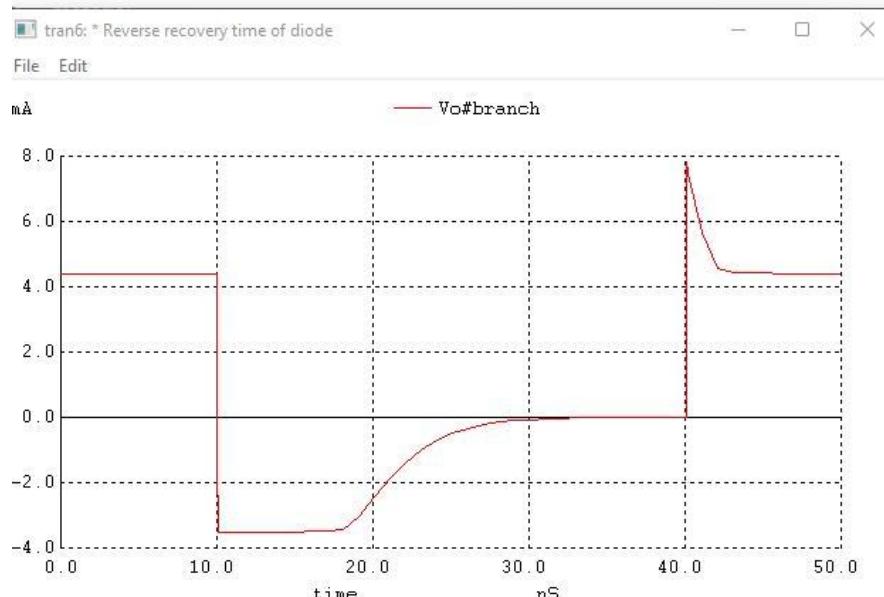
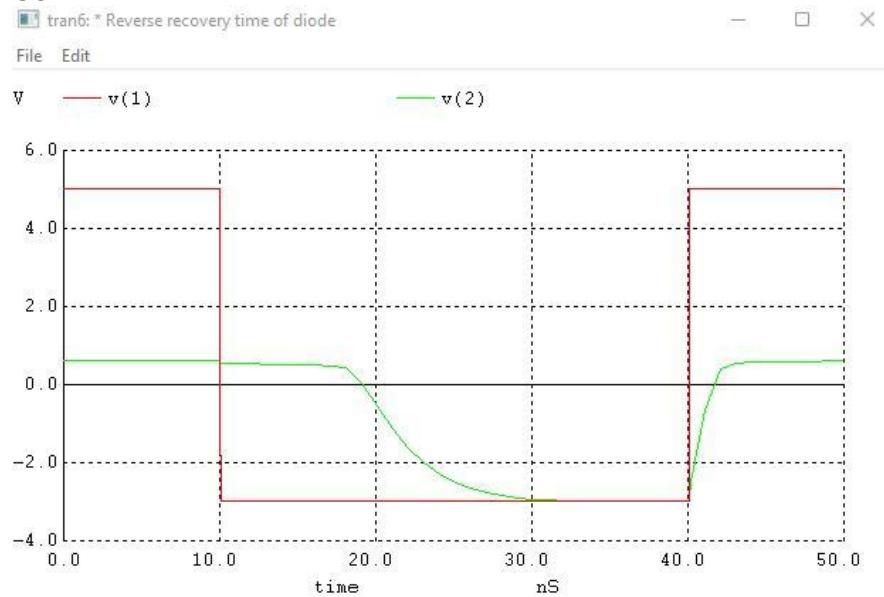
Forward Resistance = $0.5/0.5\text{mA} = 1\text{k Ohm}$, Cut off vol = 0.5 V

2. REVERSE CHARACTERISTICS



$$\text{Reverse resistance} = 1\text{V}/1\text{pA} = 10^6 \text{ M Ohm}$$

3. REVERSE RECOVERY TIME



$$T_{rr} = 8\text{ns}$$

CONCLUSION

In this experiment, we were introduced to Winspice software and developed a netlist to plot forward and reverse characteristics of a p-n junction diode. We also calculated various parameters of diode like forward and reverse resistance, cut-in voltage and Trr.

U19EC046 | DIC LAB 2

AIM

Implement RTL inverter using NPN BJT having $B_f = 20$, $R_b = 10k$ and $R_c = 1k$.

1. Verify its functionality by performing transient analysis.
2. Plot the VTC & Calculate the Noise margin.
3. Find out theoretical and practical fan-out & compare them.

Assignment 1: Repeat above for TTL

THEORY

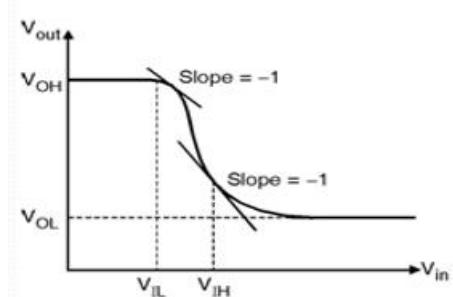
Introduction

RTL Inverter is a circuit used to invert the input signal. It consists of one BJT transistor, Base connected with resistor (R_b), Collector connected with resistor (R_c) and Emitter is grounded. Input Signal is given to Base of transistor through R_b , V_{cc} is connected to R_c and Output is taken at collector terminal.

VOLTAGE TRANSFER CHARACTERISTICS (VTC):

To study the noise margins and the fan-out capability of the RTL inverter, we should know the static behaviour of the circuit output V_{out} when input V_{in} is increased from 0 to V_{cc} . When V_{in} is below the base-emitter cut-in voltage(V_{IL}), collector current is zero and transistor is in the cutoff mode, V_{out} is almost equal to V_{cc} (V_{OH}) (assuming no load is connected at output) and VTC will be constant output for $0 < V_{in} < V_{IL}$.

As V_{in} is increased beyond V_{IL} , the transistor enters active mode. The collector current ($I_c = \beta I_b$) causes a voltage drop in the collector resistor and the collector voltage $V_c = V_{out} = V_{cc} - I_c R_c$ falls. This fall continues until output saturation voltage ($V_{ce} = V_{OL}$) BJT mode changes to saturation and corresponding input voltage is V_{IH} .



NOISE MARGINS:

Noise margin is the ratio by which the signal exceeds the minimum acceptable amount. It is normally measured in decibels. In a digital circuit, the noise margin is the amount by which the signal exceeds the threshold for a proper '0' or '1'.

$$NM_L = V_{IL} - V_{OL}$$

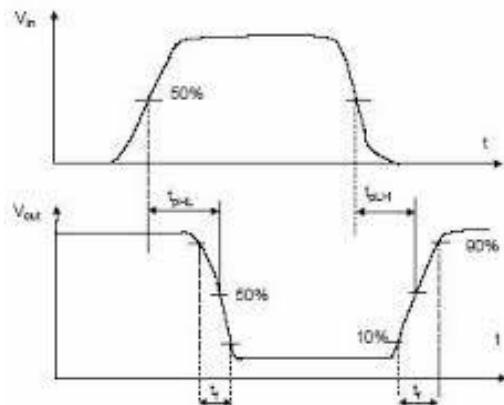
$$NM_H = V_{OH} - V_{IH}$$

In practice, noise margins are the amount of noise, that a logic circuit can withstand. Noise margins are generally defined so that positive values ensure proper operation, and negative margins result in compromised operation, or outright failure.

TRANSIENT RESPONSE:

Transient analysis means analyzing a system in unsteady state. If the variables involved in defining the state of a system does not vary with respect to time, then the system is said to be in steady state.

In Transient Analysis, also called time-domain transient analysis, computes the circuit's response a function of time. This analysis divides the time into segments and calculates the voltage and current levels for each interval.



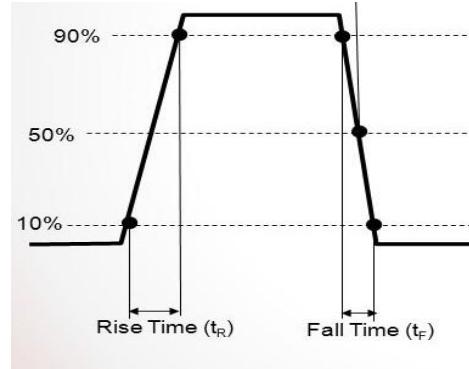
PROPAGATION DELAY:

Propagation delay is a measure of how long it takes for a gate to change state. Ideally, should be as short as possible.

t_{PHL} – the time it takes the output to go from a high to low
 t_{PLH} – the time it takes the output to go from a low to high

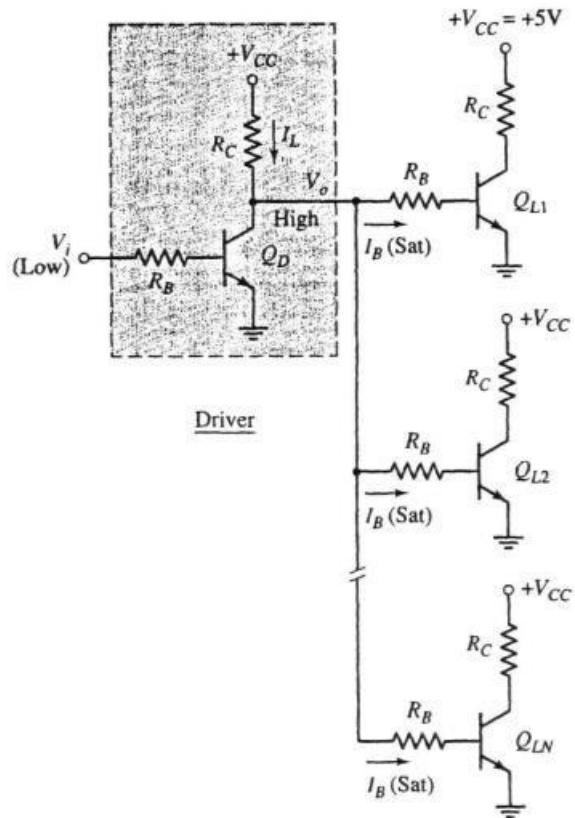
$$\text{Average Propagation Delay Time } (t_p) = \frac{t_{PHL} + t_{PLH}}{2}$$

- ⇒ Rise Time (t_r) = Time from 10% to 90%
- ⇒ Fall Time (t_f) = Time from 90% to 10%



FAN-OUT:

Fan-out of the inverter is the number of identical circuits that the inverter can drive before V_o enters the transition region. When output of RTL inverter (the driver) is at logic low, it can drive practically any number of identical inverters (loads). Since, each load transistor is operating in the cutoff mode, no current is drawn via the collector resistor of the driver, and the output voltage remains at logic low.



For logic high output of the driver as shown in above figure there are N identical inverters connected to output of driver circuit. Since, the saturation base current of each load inverter is supplied by the driver, output voltage V_o drops from its open circuit voltage of V_{CC} . The gate fan-out therefore it is limited by the number of load inverters that can be driven into saturation while maintain satisfactory logic high $V_o \geq$. The number depends on the current gain β of the driver transistor.

From above figure, the sum of the base currents of the load gates, which is the current through the collector resistor of the driver, is given by

$$I_L = N * I_{b(\text{sat})} = N * k * I_{b(\text{EOS})}$$

Where overdrive factor k is defined by

$$k = I_{b(\text{sat})}/I_{b(\text{EOS})}$$

$$I_{b(\text{EOS})} = I_{c(\text{EOS})}/\beta = (V_{cc} - V_{CE(\text{sat})})/\beta R_C$$

$$\begin{aligned} V_o &= V_{cc} - (N * k * I_{b(\text{EOS})} * R_C) \\ &= V_{cc} - (N * k * (V_{cc} - V_{CE(\text{sat})})/\beta) \end{aligned}$$

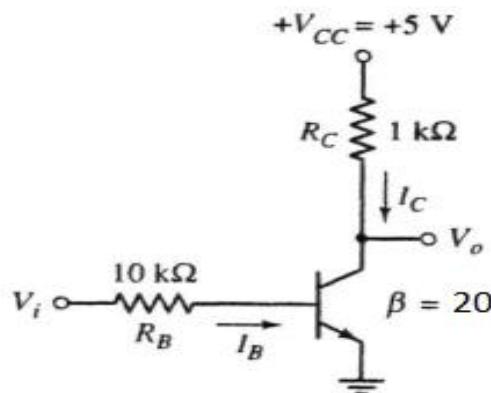
For regeneration of logic levels at the load gates, this voltage V_o must satisfy the input logic high level. Hence

$$V_{cc} - (N * k * (V_{cc} - V_{CE(\text{sat})})/\beta) \geq V_{IH}$$

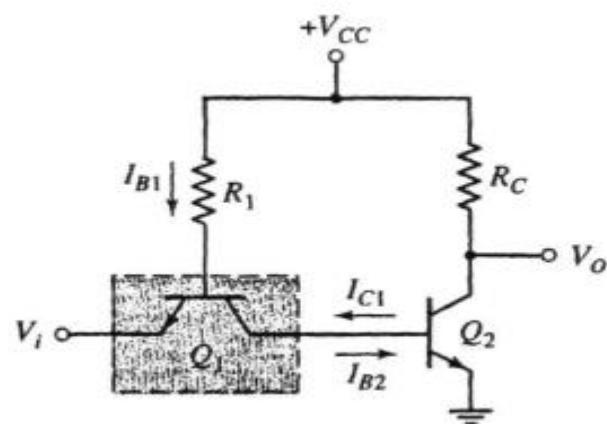
$$N \leq \frac{\beta[V_{cc} - V_{IH}]}{k[V_{cc} - V_{CE(\text{sat})}]}$$

Circuit Diagram

RTL inverter using NPN BJT



TTL inverter using NPN BJT



Working principle

Bipolar transistor switch is the simplest RTL gate. The resistor R_1 in the circuit is used across the base and input terminals. This resistor increases the voltage drop from 0.7 V to 1 V by converting the input voltage into current. The resistance R_b is chosen in such a way that it saturates the transistor and obtains high input resistance.

The collector resistor R_c converts collector current into voltage. The resistance of R_2 is high to saturate the transistor and low to obtain output resistance.

Application

The RTL circuit consists of resistors at inputs and transistors at the output side. Transistors are used as the switching device.

SPICE CODE

4.

```
* U19EC046 Lab 2_2
.model mybjt npn (bf=20)
Q1 2 1 0 mybjt
Rc 2 3 1k
Rb 4 1 10k
Vcc 3 0 5
Vin 4 0 pulse(0 5 1ns 1ns 1ns 20us 40us)
C 3 0 1p

.tran 1ns 80us

.control
run
plot V(2) V(4)
.endc
.end
```

5.

```
* U19EC046 Lab 2
.model mybjt npn (bf=20)
Q1 2 1 0 mybjt
Rc 2 3 1k
Rb 4 1 10k
Vcc 3 0 5
Vin 4 0 0

.dc Vin 0 5 0.05
.control
run
plot V(2) V(4)
.endc
.end
```

6.

```
* RTL Inverter fanout
.model switch NPN (Bf=20)

.subckt Rtl out in vc gnd
Q2 out y gnd switch
Rb1 in y 10k
Rc1 vc out 1k
.ends Rtl
```

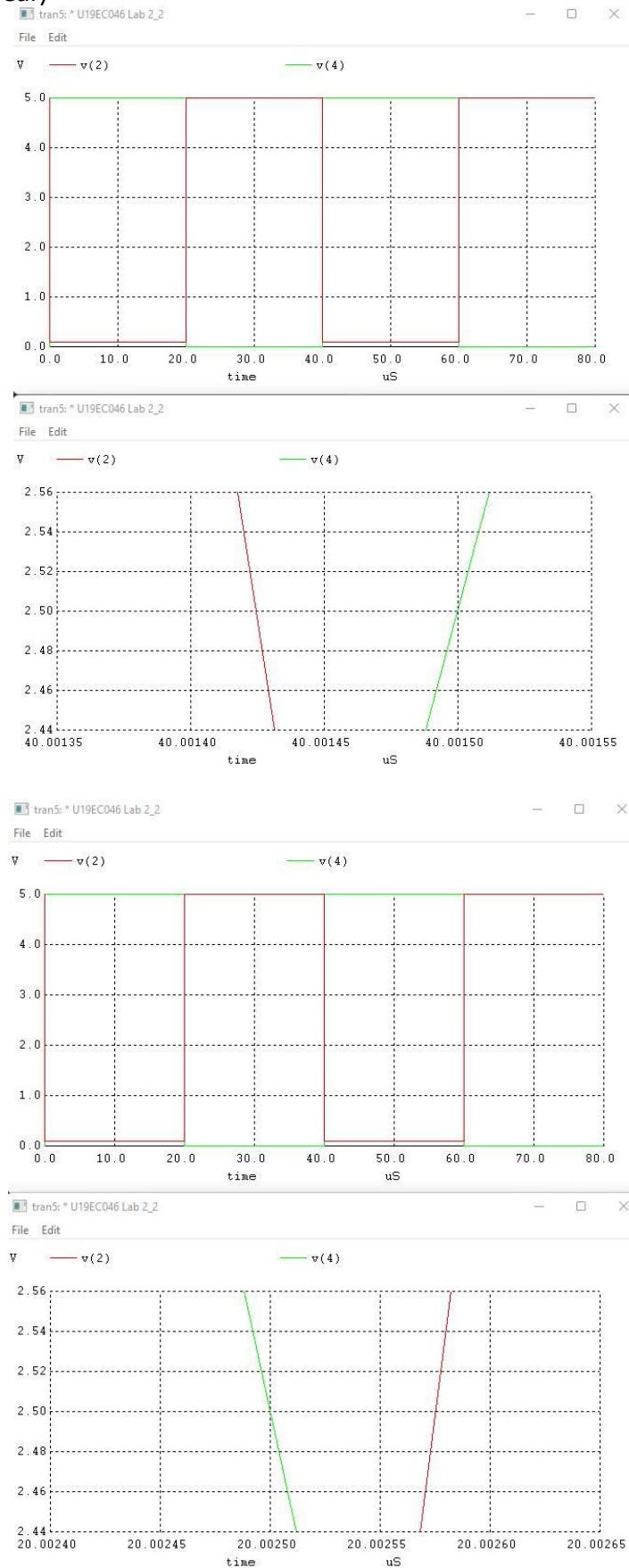
```
Vcc vcc_src 0 5
Vin vin_src 0 5
X_main out_main vin_src vcc_src 0 Rtl

X1 out1 out_main vcc_src 0 Rtl
X2 out2 out_main vcc_src 0 Rtl
X3 out3 out_main vcc_src 0 Rtl
X4 out4 out_main vcc_src 0 Rtl
X5 out5 out_main vcc_src 0 Rtl
X6 out6 out_main vcc_src 0 Rtl
X7 out7 out_main vcc_src 0 Rtl

.dc Vin 0 5 0.05
.control
run
plot V(out_main) V(vin_src)
* plot V(out1)
.endc
.end
```

SIMULATION RESULTS AND PRACTICAL CALCULATIONS

1. Propagation Delay



2. VTC and Noise margin

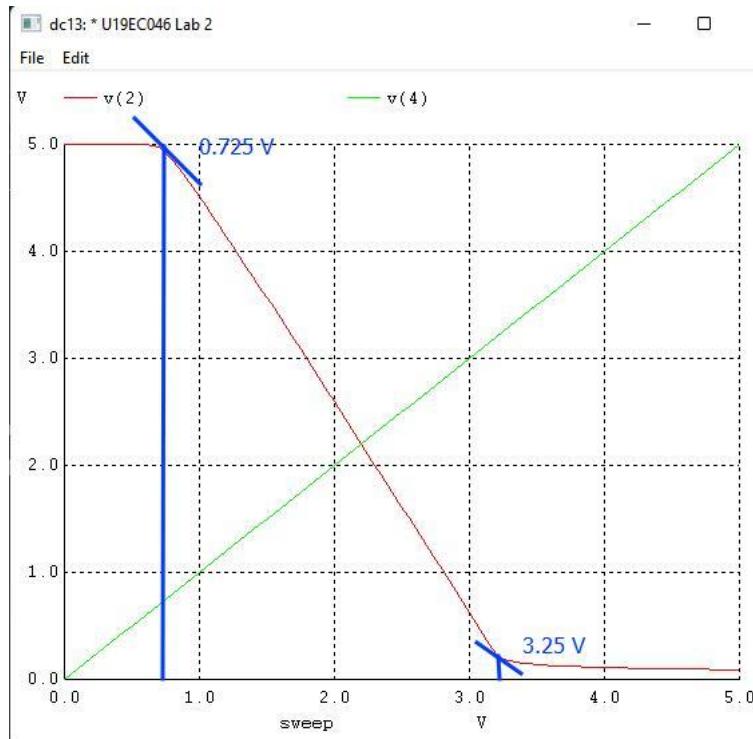


TABLE OF THEORETICAL AND PRACTICAL CALCULATION

RTL inverter transient analysis

$$\text{Propagation delay} = (0.83 + 0.41)/2 = 0.62\text{nS}$$

$$T_r = 2.25\text{nS}$$

$$T_f = 0.98\text{nS}$$

RTL inverter static analysis

$$NML = V_{IL} - V_{OL} = 0.725 - 0.2 = 0.525\text{V}$$

$$NMH = V_{OH} - V_{IH} = 5 - 3.25 = 1.75\text{V}$$

$$NM = \min(NML, NMH) = 0.525\text{V}$$

$$V_{TH} = 2.2\text{V}$$

RTL fanout calculation

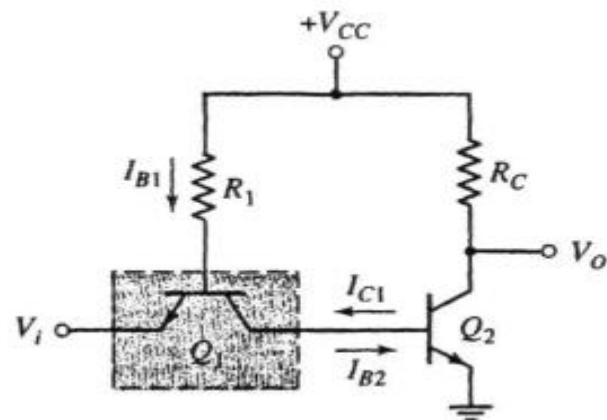
Observation table:

	Theoretical	Practical
Fan-out	7	7

ASSIGNMENT

TTL inverter and its fanout:

Circuit diagram:



TTL inverter Transient analysis:

Spice Code

```
TTL Inverter Transient Analysis U19EC046

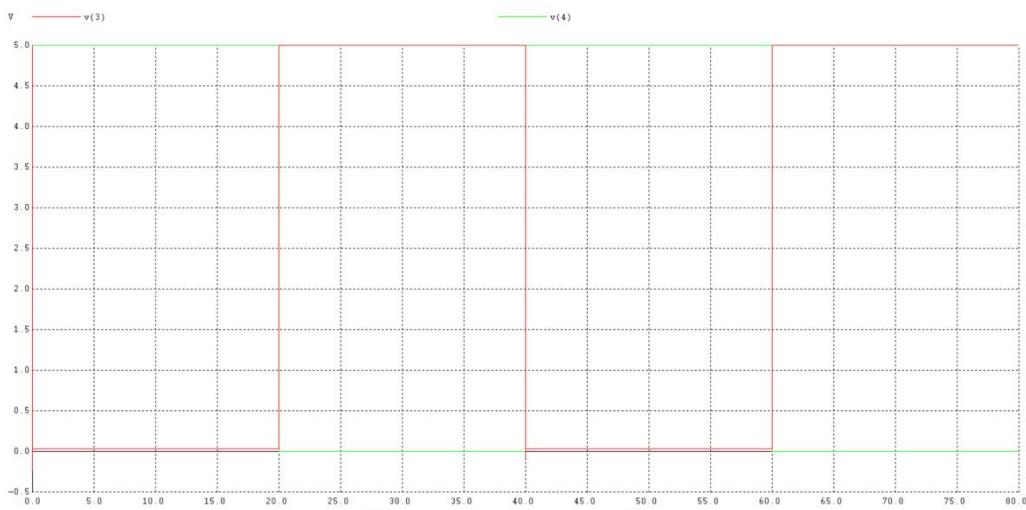
.model switch NPN (Bf=20)

Q1 2 1 4 switch
Q2 3 2 0 switch
R2 5 3 1.6k
R1 5 1 4k
Vcc 5 0 5
Vin 4 0 pulse(0 5 1ns 1ns 1ns 20us 40us)
c 3 0 1p

.tran 1ns 80us

.control
run
plot v(3) v(4)
.endc
.end
```

Simulation plots



TTL inverter static (DC) analysis: Spice Code

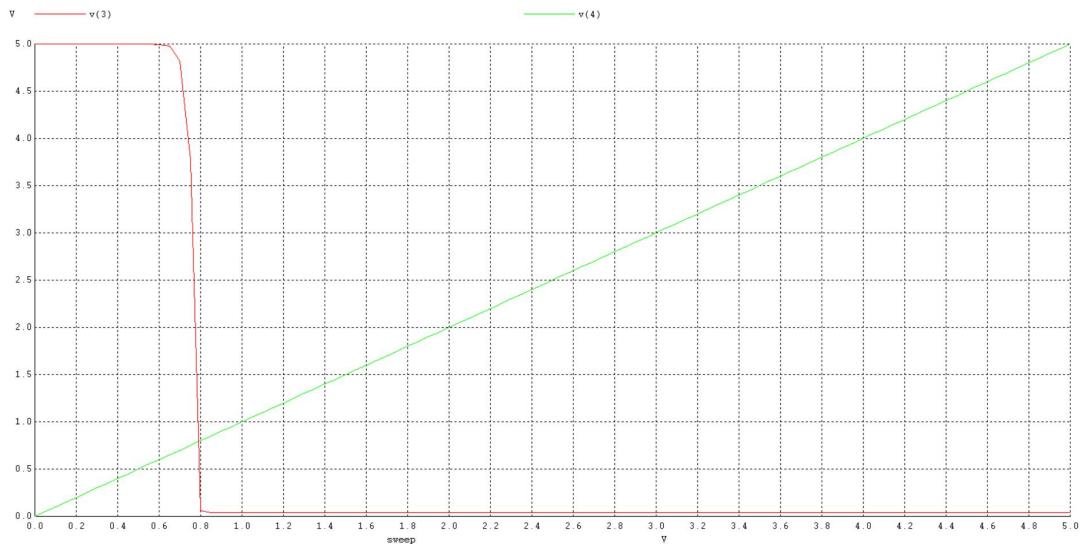
```
*TTL Inverter static(DC) Analysis U19EC046

.model switch NPN (Bf=20)

Q1 2 1 4 switch
Q2 3 2 0 switch
R2 5 3 1.6k
R1 5 1 4k
Vcc 5 0 5
Vin 4 0 dc 5

.dc Vin 0 5 0.05
.control
run
plot v(3) v(4)
.endc
.end
```

Simulation plots



TTL inverter Fan-out:

Spice Code

```
*TTL Inverter fanout U19EC046

.model switch NPN (Bf=20)

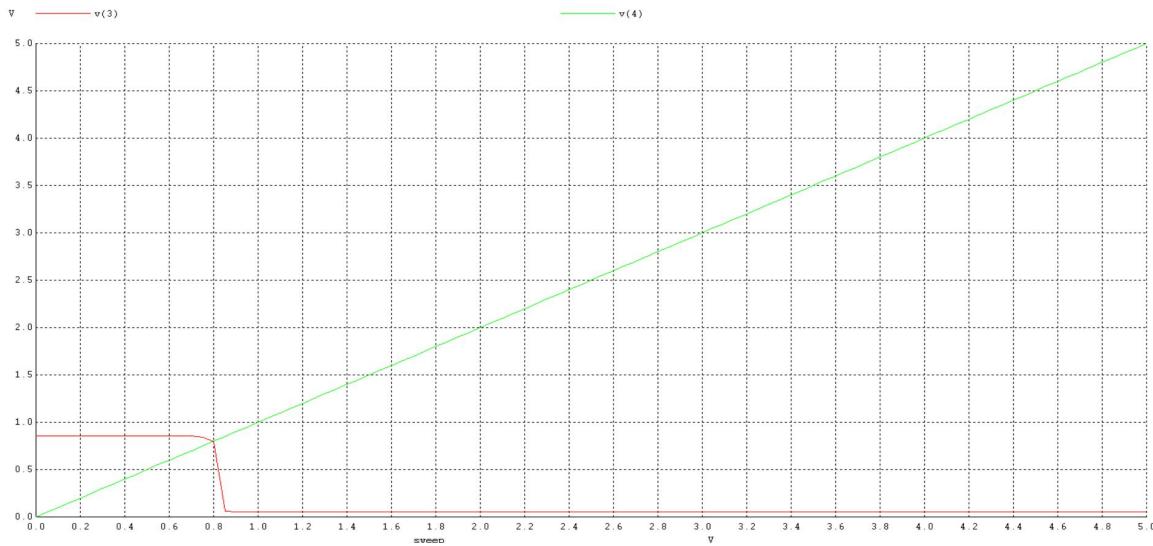
Q1 2 1 4 switch
Q2 3 2 0 switch
R2 5 3 1.6k
R1 5 1 4k
Vcc 5 0 5
Vin 4 0 5

.subckt ttl out in c 0
Q3 out y 0 switch
Q4 y z in switch
R3 out c 1.6k
R4 z c 4k
.ends ttl

x1 out1 3 5 0 ttl
x2 out2 3 5 0 ttl
x3 out3 3 5 0 ttl
x4 out4 3 5 0 ttl

.dc Vin 0 5 0.05
.control
run
plot v(3) v(4)
.endc
.end
```

Simulation plots



Simulation results and practical calculations:

TTL inverter transient analysis

$$\text{Propagation delay} = (1.5 + 0.25)/2 = 0.875\text{nS}$$

$$T_r = 3.5\text{nS}$$

$$T_f = 0.2\text{nS}$$

TTL inverter static analysis

$$NM_L = V_{IL} - V_{OL} = 0.68 - 0.06 = 0.62\text{V}$$

$$NM_H = V_{OH} - V_{IH} = 5 - 0.85 = 4.15\text{V}$$

$$NM = \min(NM_L, NM_H) = 0.62\text{V}$$

$$V_{TH} = 0.79\text{V}$$

TTL fanout calculation

Observation table:

	Theoretical	Practical
Fan-out	X	4

CONCLUSION

In this experiment we have studied about the RTL logic and its characteristic parameters as well as compared the theoretical results with practical results of RTL inverter.

AIM

Implement DTL Inverter using NPN BJT.

1. Plot VTC and Calculate Noise Margin.
2. Verify its functionality by performing transient analysis.
3. Find theoretical and practical Fan Out and compare them.

THEORY

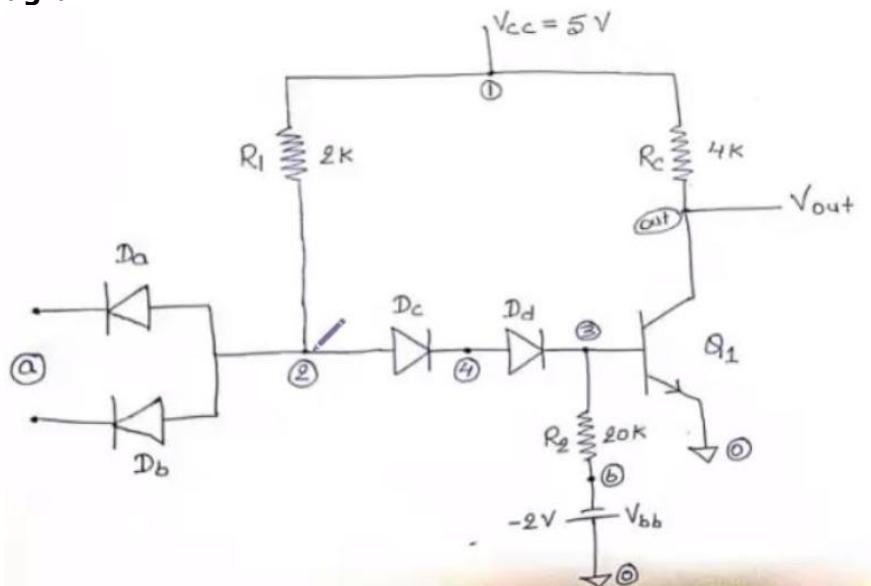
Introduction

Diode-Transistor Logic, or DTL, refers to the technology for designing and fabricating digital circuits wherein logic gates employ both diodes and transistors. DTL offers better noise margins and greater fan-outs than RTL, but suffers from low speed, especially in comparison to TTL.

RTL allows the construction of NOR gates easily, but NAND gates are relatively more difficult to get from RTL. DTL, however, allows the construction of simple NAND gates from a single transistor, with the help of several diodes and resistors.

Below figure shows an example of an 2-input DTL NAND gate. It consists of a single transistor Q configured as an inverter, which is driven by a current that depends on the inputs to the three input diodes D1 and D2.

Circuit Diagram



Working principle

In the NAND gate in Figure 1, the current through diodes DA and DB will only be large enough to drive the transistor into saturation and bring the output voltage V_o to logic '0' if all the input diodes D1-D4 are 'off', which is true when the inputs to all of them are logic '1'. This is because when D1-D4 are not conducting, all the current from V_{cc} through R_1 will go through DA and DB and into the base of the transistor, turning it on and pulling V_o to near ground.

However, if any of the diodes D1 and D2 gets an input voltage of logic '0', it gets forward-biased and starts conducting. This conducting diode 'shunts' almost all the current away from the reverse-biased DA and DB, limiting the transistor base current. This forces the transistor to turn off, bringing up the output voltage V_o to logic '1'.

Application

One advantage of DTL over RTL is its better noise margin. The noise margin of a logic gate for logic level '0', Δ_0 , is defined as the difference between the maximum input voltage that it will recognize as a '0' (V_{il}) and the maximum voltage that may be applied to it as a '0' (V_{oh} of the driving gate connected to it). For logic level '1', the noise margin Δ_1 is the difference between the minimum input voltage that may be applied to it as a '1' (V_{oh} of the driving gate connected to it) and the minimum input voltage that it will recognize as a '1' (V_{ih}).

SPICE CODE

7. VTC and noise margin

```
* modified dtl transfer char
.model mybjt npn bf=20
.model mydiode d

.subckt modifiedDTL in1 in2 vccNode gnd out
    rc vccNode out 2k
    q2 out q2base gnd mybjt
    r3 q2base gnd 5k
    dd q1emitter q2base mydiode
    q1 q1collector q1base q1emitter mybjt
    r2 q1collector q1base 2k
    r1 q1collector vccNode 1.75k
    da q1base in1 mydiode
    db q1base in2 mydiode
.ends dtlckt

*supply
vcc vccNode 0 5
Va in 0 5

*driver gate
Xd in in vccNode 0 out1 modifiedDTL

.dc Va 0.5 5 0.05

.control
run
plot v(in) v(out1)
.endc
.end
```

8. Propogation delay

```
* dtl transfer char
.model q1 npn bf=50
.model d1 d

q11 out 3 0 q1

da 2 a d1
db 2 a d1
dc 2 4 d1
```

```

dd 4 3 d1

r1 1 2 2k
rc 1 out 4k
r2 3 b 20k

vbb b 0 -2
vec 1 0 5
va a 0 pulse(0 5 20ps 10ps 10ps 200ps 550ps)

.tran 20ps 1500ps

.control
run
plot v(a) v(out)
.endc
.end

```

9. Fan Out

```

*DTL NAND FANOUT
.model q1 npn bf=50
.model d1 d

.subckt dtlckt a b c 1 0 out
q1 out 4 0 q1
da 2 a d1
db 2 b d1
dc 2 3 d1
dd 3 4 d1
r1 2 1 2k
rc 1 out 4k
r2 4 c 20k
.ends dtlckt

*supply
vcc 1 0 5
vbb c 0 -2
Va a 0 5

*driver gate
Xd a a c 1 0 out1 dtlckt

*Load gates
XL1 out1 out1 c 1 0 out2 dtlckt
XL2 out1 out1 c 1 0 out3 dtlckt
XL3 out1 out1 c 1 0 out4 dtlckt
XL4 out1 out1 c 1 0 out5 dtlckt
XL5 out1 out1 c 1 0 out6 dtlckt
XL6 out1 out1 c 1 0 out7 dtlckt
XL7 out1 out1 c 1 0 out8 dtlckt
XL8 out1 out1 c 1 0 out9 dtlckt
XL9 out1 out1 c 1 0 out10 dtlckt

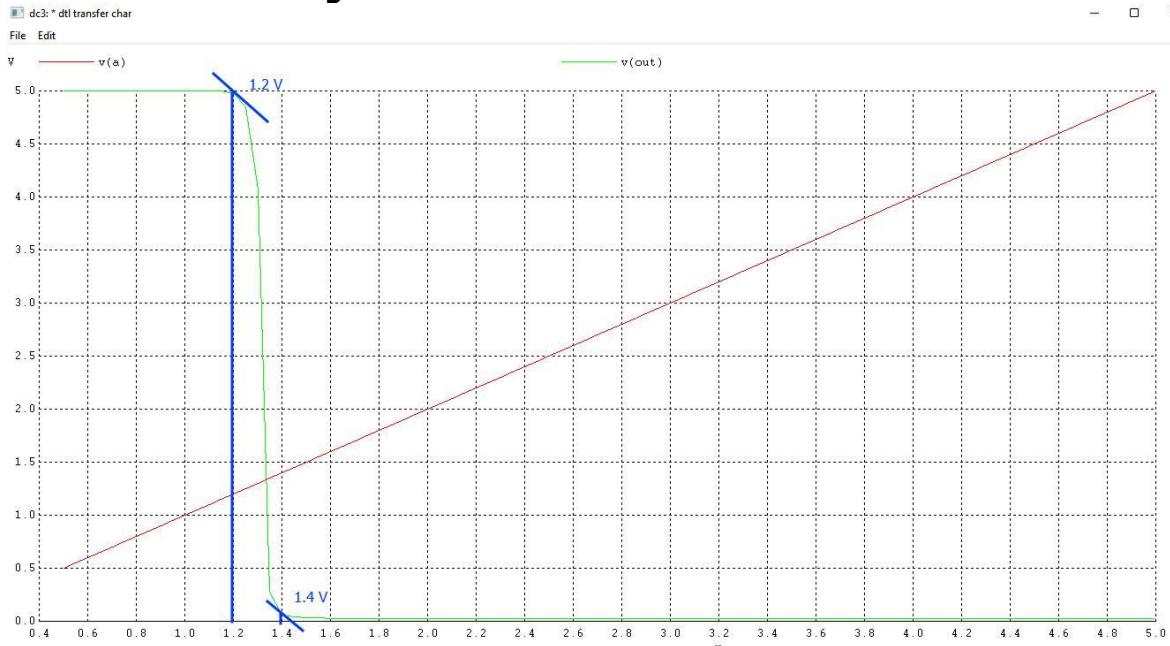
```

```
XL10 out1 out1 c 1 0 out11 dtlckt
XL11 out1 out1 c 1 0 out12 dtlckt
XL12 out1 out1 c 1 0 out13 dtlckt
XL13 out1 out1 c 1 0 out14 dtlckt
XL14 out1 out1 c 1 0 out15 dtlckt
XL15 out1 out1 c 1 0 out16 dtlckt
XL16 out1 out1 c 1 0 out17 dtlckt
XL17 out1 out1 c 1 0 out18 dtlckt
XL18 out1 out1 c 1 0 out19 dtlckt
XL19 out1 out1 c 1 0 out20 dtlckt
XL20 out1 out1 c 1 0 out21 dtlckt
XL21 out1 out1 c 1 0 out22 dtlckt
XL22 out1 out1 c 1 0 out23 dtlckt
XL23 out1 out1 c 1 0 out24 dtlckt
XL24 out1 out1 c 1 0 out25 dtlckt
XL25 out1 out1 c 1 0 out26 dtlckt
XL26 out1 out1 c 1 0 out27 dtlckt
XL27 out1 out1 c 1 0 out28 dtlckt
XL28 out1 out1 c 1 0 out29 dtlckt
XL29 out1 out1 c 1 0 out30 dtlckt
XL30 out1 out1 c 1 0 out31 dtlckt
XL31 out1 out1 c 1 0 out32 dtlckt
XL32 out1 out1 c 1 0 out33 dtlckt
XL33 out1 out1 c 1 0 out34 dtlckt
XL34 out1 out1 c 1 0 out35 dtlckt
XL35 out1 out1 c 1 0 out36 dtlckt
XL36 out1 out1 c 1 0 out37 dtlckt
XL37 out1 out1 c 1 0 out38 dtlckt
XL38 out1 out1 c 1 0 out39 dtlckt
XL39 out1 out1 c 1 0 out40 dtlckt
XL40 out1 out1 c 1 0 out41 dtlckt
XL41 out1 out1 c 1 0 out42 dtlckt
XL42 out1 out1 c 1 0 out43 dtlckt

.dc Va 0.5 5 0.05
.control
run
plot V(out1) V(a)
.endc
.end
```

SIMULATION RESULTS AND PRACTICAL CALCULATIONS

1. VTC and noise margin



$$V_{il} = 1.2 \text{ V}, V_{ih} = 1.4 \text{ V}, V_{oh} = 5\text{V}, V_{ol} = 0.05 \text{ V}$$

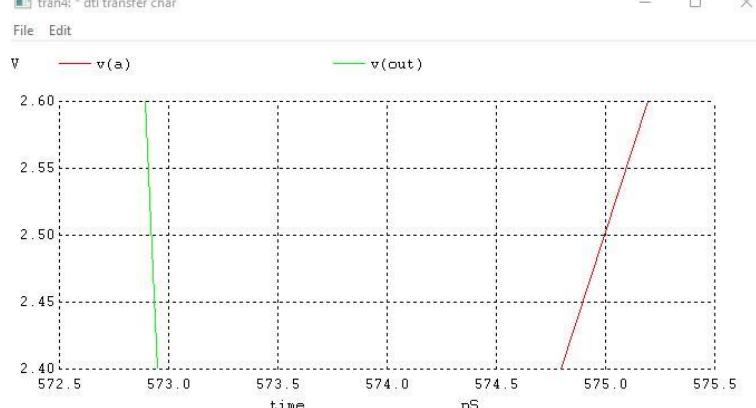
$$NM_H = 5 - 1.4 = 3.6\text{V}$$

$$NM_L = 1.2 - 0.05 = 1.15\text{V}$$

$$NM = \min(NM_H, NM_L) = 1.15\text{V}$$

2. Propagation delay

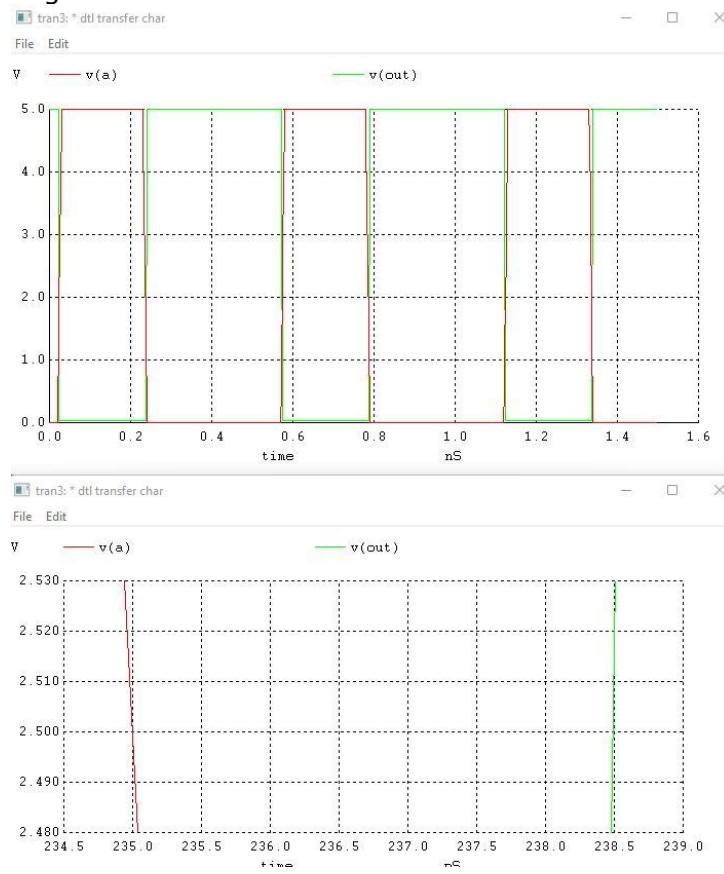
a. High to Low



$$t_1 = 572.8\text{us}, t_2 = 575\text{us}$$

$t_{hl} = 2.2\mu s$

b. Low to High

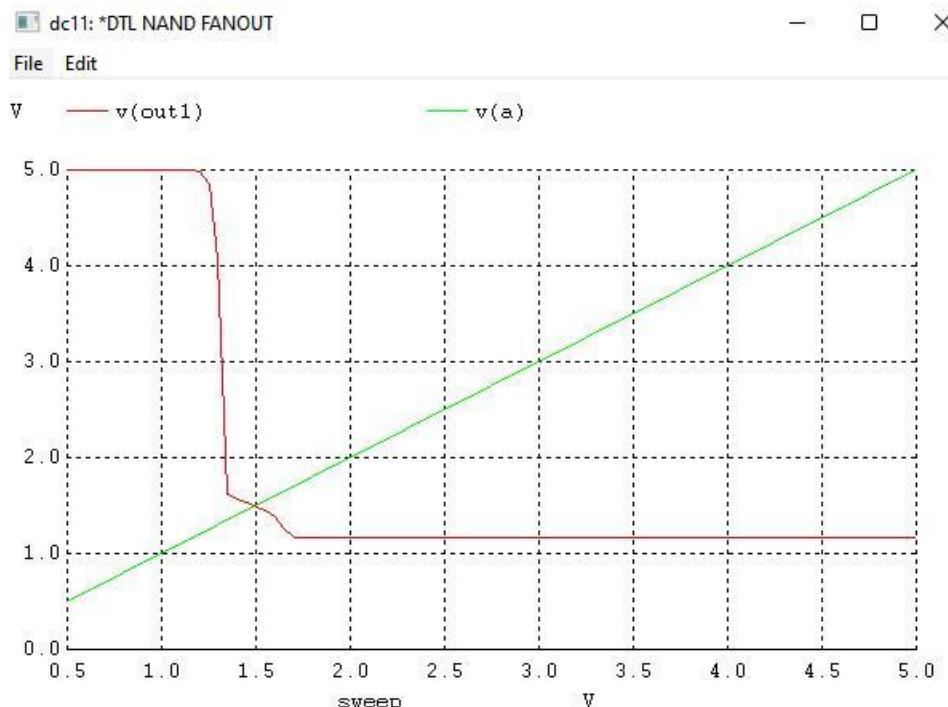


$t_1 = 235\mu s, t_2 = 238.5\mu s$

$t_{hl} = 3.5\mu s$

$$t_{propagation_delay} = \text{avg}(2.2, 3.5) = 2.85\mu s$$

3. Fan Out



Fan Out = 42

CONCLUSION

We implemented DTL inverter using NPN BJT. We plotted VT characteristics of DTL, obtained its noise margin, and verified its functionality by performing transient analysis.

AIM

Implement Modified diode transistor logic (MDTL) using NPN BJT. $B_f = 20$, $R_1 = 1.75k$, $R_2 = 2k$, $R_3 = 5k$ and $R_C = 2k$

1. Verify its functionality as NAND gate and calculate propagation delay.
2. Plot VTC and Calculate Noise Margin.
3. Compare DTL with MDTL with respect to noise margin, fan-out and propagation delay comment about it.

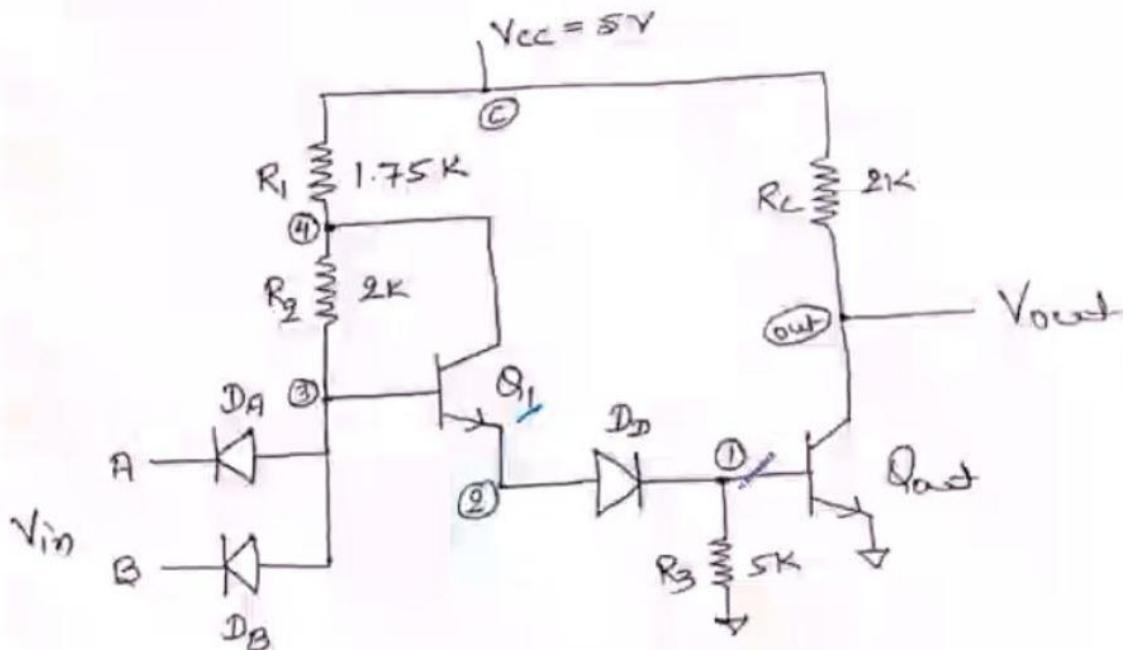
THEORY

Introduction

The diode-transistor logic, also termed as DTL, replaced RTL family because of greater fan-out capability and more noise margin. As its name suggests, DTL circuits mainly consists of diodes and transistors that comprises DTL devices.

Due to number of diodes used in this circuit, the speed of the circuit is significantly low. Hence this family of logic gates is modified to transistor-transistor logic i.e. TTL family.

Circuit Diagram



Working principle

The fan out of IC positive DTL NAND gate may be increased by replacing the diode by a transistor Q_1 as shown in figure 6. Thus, transistor Q_1 while conducting is in its active region and not in saturation. This results from the fact that the current through resistor R_1 (1.75 K-OHMs) is in a direction to reverse bias the collector junction of NPN transistor Q_1 . Further the emitter current of Q_1 provides the base current I_{B2} of Q_{out} . Hence Q_{out} is driven by a much larger base current I_B . Hence, for the same value of h_{FE} , the collector current of Q_{out} is much larger permitting much greater fan out.

Application

It is used in the applications where noise margin, fan Out requirements are high, and Propagation delay is low.

SPICE CODE

10. Propagation Delay

```
* modified dtl propogation delay
.model mybjt npn bf=20
.model mydiode d

.subckt modifiedDTL in1 in2 vccNode gnd out
    rc vccNode out 2k
    q2 out q2base gnd mybjt
    r3 q2base gnd 5k
    dd q1emitter q2base mydiode
    q1 q1collector q1base q1emitter mybjt
    r2 q1collector q1base 2k
    r1 q1collector vccNode 1.75k
    da q1base in1 mydiode
    db q1base in2 mydiode
.ends dtlckt

*supply
vcc vccNode 0 5
va in 0 pulse(0 5 0ps 1ps 1ps 20us 40us)

Xd in in vccNode 0 out1 modifiedDTL
c_load out1 0 1p

.tran 20ns 80us

.control
run
plot v(in) v(out1)
.endc
.end
```

11. VTC and noise margin

```
* modified dtl transfer char
.model mybjt npn bf=20
.model mydiode d

.subckt modifiedDTL in1 in2 vccNode gnd out
    rc vccNode out 2k
    q2 out q2base gnd mybjt
    r3 q2base gnd 5k
    dd q1emitter q2base mydiode
    q1 q1collector q1base q1emitter mybjt
    r2 q1collector q1base 2k
    r1 q1collector vccNode 1.75k
    da q1base in1 mydiode
    db q1base in2 mydiode
.ends dtlckt
```

```

*supply
vcc vccNode 0 5
Va in 0 5

*driver gate
Xd in in vccNode 0 out1 modifiedDTL

.dc Va 0.5 5 0.05

.control
run
plot v(in) v(out1)
.endc
.end

```

12. Fan Out

```

* modified dtl fanout
.model mybjt npn bf=50
.model mydiode d

.subckt modifiedDTL in1 in2 vccNode gnd out
    rc vccNode out 2k
    q2 out q2base gnd mybjt
    r3 q2base gnd 5k
    dd q1emitter q2base mydiode
    q1 q1collector q1base q1emitter mybjt
    r2 q1collector q1base 2k
    r1 q1collector vccNode 1.75k
    da q1base in1 mydiode
    db q1base in2 mydiode
.ends dtlckt

*supply
vcc vccNode 0 5
Va in 0 5

*driver gate
Xd in in vccNode 0 out1 modifiedDTL

*Load gates
XL1 out1 out1 vccNode 0 out2 modifiedDTL
XL2 out1 out1 vccNode 0 out3 modifiedDTL
XL3 out1 out1 vccNode 0 out4 modifiedDTL
XL4 out1 out1 vccNode 0 out5 modifiedDTL
XL5 out1 out1 vccNode 0 out6 modifiedDTL
XL6 out1 out1 vccNode 0 out7 modifiedDTL
XL7 out1 out1 vccNode 0 out8 modifiedDTL
XL8 out1 out1 vccNode 0 out9 modifiedDTL
XL9 out1 out1 vccNode 0 out10 modifiedDTL
XL10 out1 out1 vccNode 0 out11 modifiedDTL
XL11 out1 out1 vccNode 0 out12 modifiedDTL
XL12 out1 out1 vccNode 0 out13 modifiedDTL

```

```
XL13 out1 out1 vccNode 0 out14 modifiedDTL
XL14 out1 out1 vccNode 0 out15 modifiedDTL
XL15 out1 out1 vccNode 0 out16 modifiedDTL
XL16 out1 out1 vccNode 0 out17 modifiedDTL
XL17 out1 out1 vccNode 0 out18 modifiedDTL
XL18 out1 out1 vccNode 0 out19 modifiedDTL
XL19 out1 out1 vccNode 0 out20 modifiedDTL
XL20 out1 out1 vccNode 0 out21 modifiedDTL
XL21 out1 out1 vccNode 0 out22 modifiedDTL
XL22 out1 out1 vccNode 0 out23 modifiedDTL
XL23 out1 out1 vccNode 0 out24 modifiedDTL
XL24 out1 out1 vccNode 0 out25 modifiedDTL
XL25 out1 out1 vccNode 0 out26 modifiedDTL
XL26 out1 out1 vccNode 0 out27 modifiedDTL
XL27 out1 out1 vccNode 0 out28 modifiedDTL
XL28 out1 out1 vccNode 0 out29 modifiedDTL
XL29 out1 out1 vccNode 0 out30 modifiedDTL
XL30 out1 out1 vccNode 0 out31 modifiedDTL
XL31 out1 out1 vccNode 0 out32 modifiedDTL
XL32 out1 out1 vccNode 0 out33 modifiedDTL
XL33 out1 out1 vccNode 0 out34 modifiedDTL
XL34 out1 out1 vccNode 0 out35 modifiedDTL
XL35 out1 out1 vccNode 0 out36 modifiedDTL
XL36 out1 out1 vccNode 0 out37 modifiedDTL
XL37 out1 out1 vccNode 0 out38 modifiedDTL
XL38 out1 out1 vccNode 0 out39 modifiedDTL
XL39 out1 out1 vccNode 0 out40 modifiedDTL
XL40 out1 out1 vccNode 0 out41 modifiedDTL
XL41 out1 out1 vccNode 0 out42 modifiedDTL
XL42 out1 out1 vccNode 0 out43 modifiedDTL
XL43 out1 out1 vccNode 0 out44 modifiedDTL
XL44 out1 out1 vccNode 0 out45 modifiedDTL
XL45 out1 out1 vccNode 0 out46 modifiedDTL
XL46 out1 out1 vccNode 0 out47 modifiedDTL
XL47 out1 out1 vccNode 0 out48 modifiedDTL
XL48 out1 out1 vccNode 0 out49 modifiedDTL
XL49 out1 out1 vccNode 0 out50 modifiedDTL
XL50 out1 out1 vccNode 0 out51 modifiedDTL
XL51 out1 out1 vccNode 0 out52 modifiedDTL
XL52 out1 out1 vccNode 0 out53 modifiedDTL
XL53 out1 out1 vccNode 0 out54 modifiedDTL
XL54 out1 out1 vccNode 0 out55 modifiedDTL
XL55 out1 out1 vccNode 0 out56 modifiedDTL
XL56 out1 out1 vccNode 0 out57 modifiedDTL
XL57 out1 out1 vccNode 0 out58 modifiedDTL
XL58 out1 out1 vccNode 0 out59 modifiedDTL
XL59 out1 out1 vccNode 0 out60 modifiedDTL
XL60 out1 out1 vccNode 0 out61 modifiedDTL
XL61 out1 out1 vccNode 0 out62 modifiedDTL
XL62 out1 out1 vccNode 0 out63 modifiedDTL
XL63 out1 out1 vccNode 0 out64 modifiedDTL
```

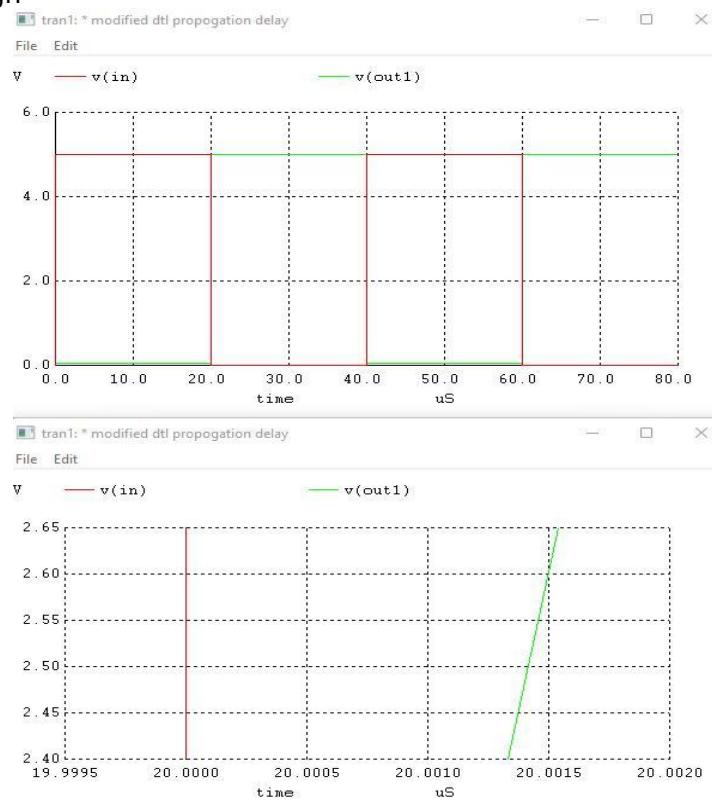
```
XL64 out1 out1 vccNode 0 out65 modifiedDTL
XL65 out1 out1 vccNode 0 out66 modifiedDTL
XL66 out1 out1 vccNode 0 out67 modifiedDTL
XL67 out1 out1 vccNode 0 out68 modifiedDTL
XL68 out1 out1 vccNode 0 out69 modifiedDTL
XL69 out1 out1 vccNode 0 out70 modifiedDTL
XL70 out1 out1 vccNode 0 out71 modifiedDTL
XL71 out1 out1 vccNode 0 out72 modifiedDTL
XL72 out1 out1 vccNode 0 out73 modifiedDTL
XL73 out1 out1 vccNode 0 out74 modifiedDTL
XL74 out1 out1 vccNode 0 out75 modifiedDTL
XL75 out1 out1 vccNode 0 out76 modifiedDTL
XL76 out1 out1 vccNode 0 out77 modifiedDTL
XL77 out1 out1 vccNode 0 out78 modifiedDTL
XL78 out1 out1 vccNode 0 out79 modifiedDTL
XL79 out1 out1 vccNode 0 out80 modifiedDTL
XL80 out1 out1 vccNode 0 out81 modifiedDTL
XL81 out1 out1 vccNode 0 out82 modifiedDTL
XL82 out1 out1 vccNode 0 out83 modifiedDTL
XL83 out1 out1 vccNode 0 out84 modifiedDTL
XL84 out1 out1 vccNode 0 out85 modifiedDTL
XL85 out1 out1 vccNode 0 out86 modifiedDTL
XL86 out1 out1 vccNode 0 out87 modifiedDTL
XL87 out1 out1 vccNode 0 out88 modifiedDTL
XL88 out1 out1 vccNode 0 out89 modifiedDTL

.dc Va 0.5 5 0.05
.control
run
plot V(out1) V(in)
.endc
.end
```

SIMULATION RESULTS AND PRACTICAL CALCULATIONS

1. Propagation Delay

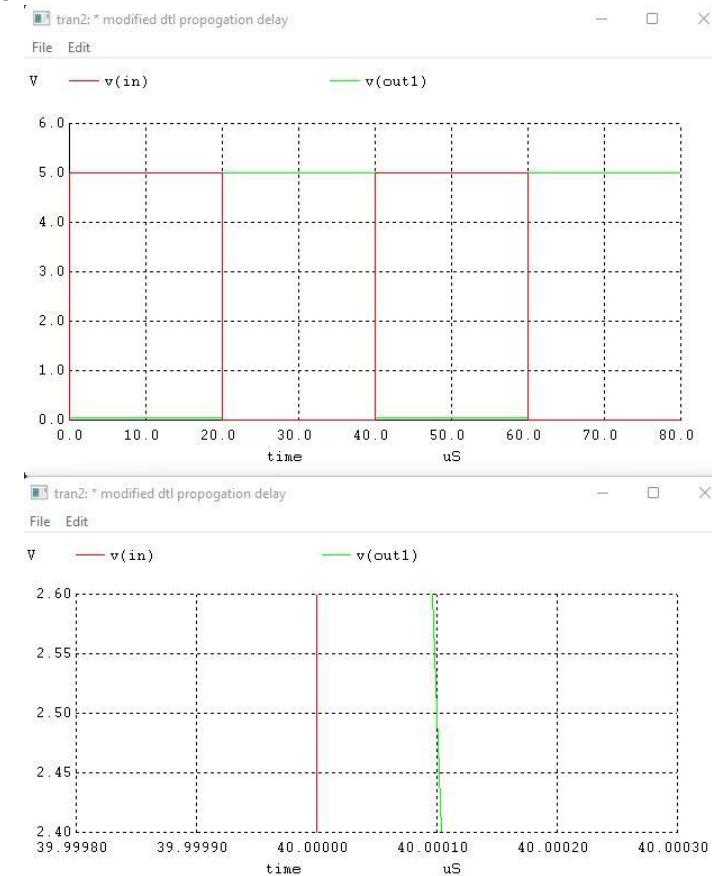
a. Low to High



$$t_1 = 20\text{us}, t_2 = 20.00142\text{us}$$

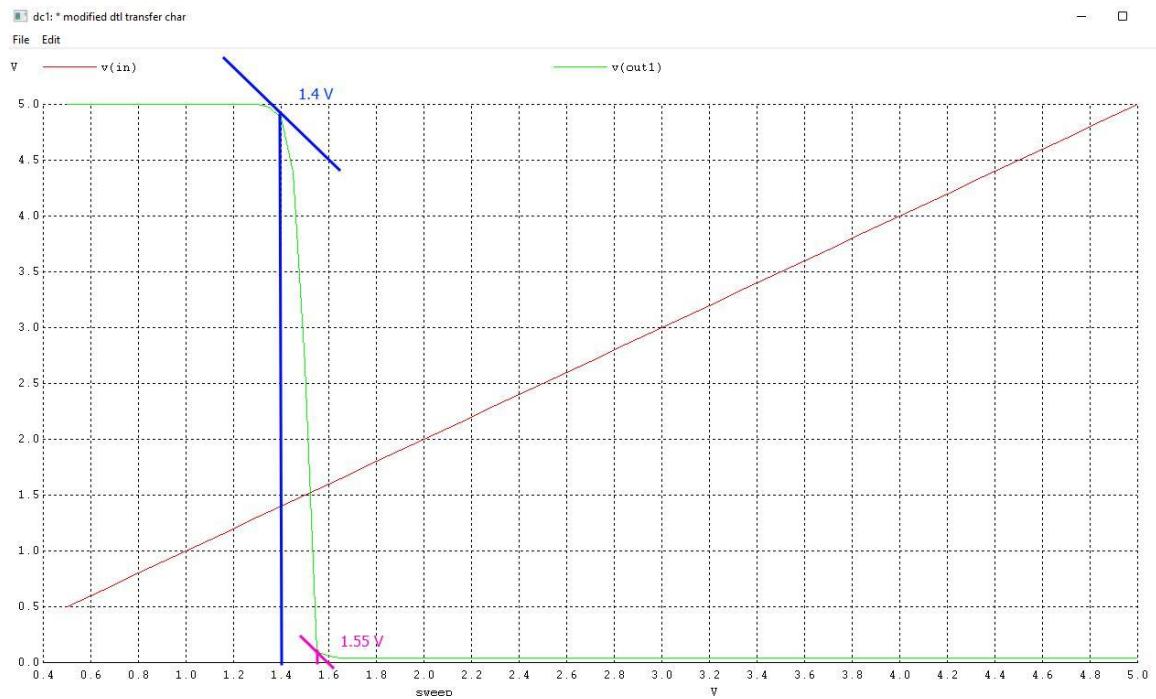
$$t_{lh} = 1.42 \text{ ns}$$

b. High to low



$t_1 = 40\text{us}$, $t_2 = 40.0001\text{us}$
 $t_{hl} = 0.1\text{ns}$
 $t_{propagation_delay} = \text{avg}(1.42, 0.1) = 0.75\text{ns}$

2. VTC and Noise Margin



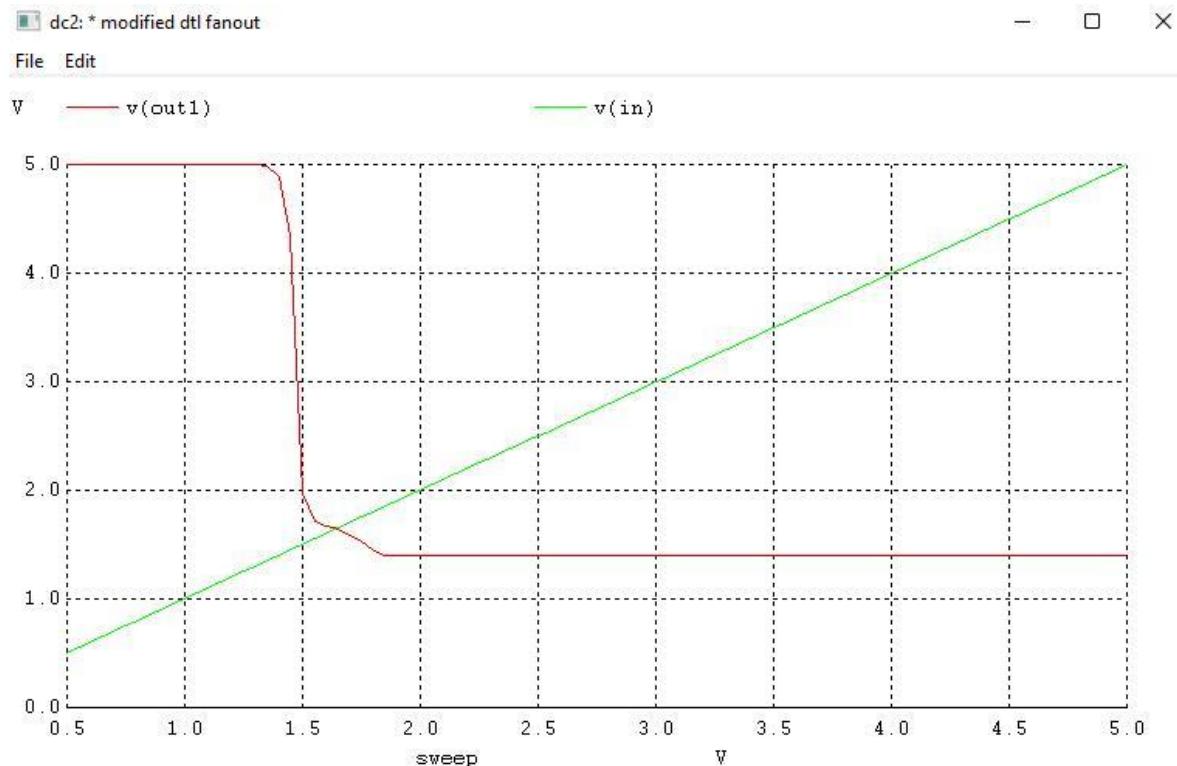
$$V_{oh} = 5\text{V}, V_{ol} = 0.1\text{V}, V_{ih} = 1.55\text{V}, V_{il} = 1.4\text{V}$$

$$NM_H = 5 - 1.55 = 3.45\text{V}$$

$$NM_L = 1.4 - 0.1 = 1.3\text{V}$$

$$NM = \min(NM_H, NM_L) = 1.3\text{V}$$

3. Fan Out



$$\text{Fan Out} = 88 \quad (B_f = 50)$$

Fan Out = 33 (Bf = 20)

COMPARISION OF DTL and MDTL

Parameter	DTL	MDTL
Noise Margin	1.15V	1.3V
Propogation delay	2.85us	0.75ns
Fan out	42	88

CONCLUSION

In this Experiment we have studied and written spice code for Modified diode transistor logic and also calculated its VTC, noise margin and fanout, it was observed that the noise margin of MDTL is increased slightly and the propagartion delaay was reduced by an order of 10^3 and fan out is increased substantially as compared with DTL family.

AIM

Implement TTL inverter using NPN BJT having $B_f = 50$, $R_b = 4k$ and $R_c = 1.6k$.

4. Verify its functionality by performing transient analysis.
5. Plot the VTC & Calculate the Noise margin.
6. Find out theoretical and practical fan-out & compare them.

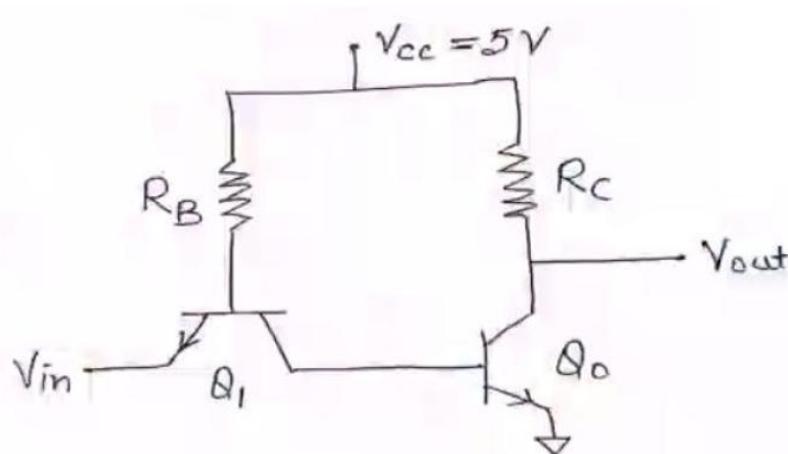
THEORY

Introduction

DTL was able to improve fan-out compared to RTL. However, that was done at the expense of Transient response and Chip area.

A solution for the problem was proposed in the form of a new logic family which utilizes only transistors and resistors. BJTs are smaller than diodes.

Circuit Diagram



Working principle

For V_{in} very low, the base-emitter junction of Q_1 will be forward biased. The base-collector junction will also be forward biased. Therefore, Q_1 will be saturated.

The base-emitter voltage of Q_0 is:

$$V_{BE,0} = V_{CE,1(Sat)} + V_{in}$$

Therefore, Q_0 will be cut-off

Therefore,

$$V_{out} = V_{OH} = V_{cc}$$

As V_{in} is increased, V_B of Q_0 will also increase. Eventually, Q_0 will turn on.

This happens when:

$$V_{in} = V_{IL} = V_{BE,0(FA)} - V_{CE,I(Sat)}$$

As V_{in} is increased even more, Q_0 comes closer to Saturation and eventually saturates.

At that point:

$$V_{out} = V_{OL} = V_{CE,0(Sat)}$$

SPICE CODE

13. Transient Analysis

```
*TTL Inverter Transient Analysis
.model switch NPN (Bf=50)

.subckt ttl out in vcc_power gnd
    Q1 out q1_base gnd switch
    Q2 q1_base q2_base in switch
    Rc out vcc_power 1.6k
    Rb q2_base vcc_power 4k
.ends ttl

xd out input vcc_node 0 ttl

Vcc vcc_node 0 5
Vin input 0 pulse(0 5 1ns 1ns 1ns 20us 40us)

c_load out 0 1p

.tran 1ns 80us

.control
run
plot v(input) v(out)
.endc
.end
```

14. VTC and noise Margin

```
*TTL Inverter Analysis
.model switch NPN (Bf=50)

.subckt ttl out in vcc_power gnd
    Q1 out q1_base gnd switch
    Q2 q1_base q2_base in switch
    Rc out vcc_power 1.6k
    Rb q2_base vcc_power 4k
.ends ttl

xd out input vcc_node 0 ttl

Vcc vcc_node 0 5
Vin input 0 5

c_load out 0 1p

.dc Vin 0 5 0.05

.control
run
plot v(input) v(out)
.endc
```

```
.end
```

15. Fan-out

```
*TTL Inverter Fanout Analysis
.model switch NPN (Bf=50)

.subckt ttl out in vcc_power gnd
    Q1 out q1_base gnd switch
    Q2 q1_base q2_base in switch
    Rc out vcc_power 1.6k
    Rb q2_base vcc_power 4k
.ends ttl

xd out input vcc_node 0 ttl

Vcc vcc_node 0 5
Vin input 0 pulse(0 5 1ns 1ns 1ns 20us 40us)

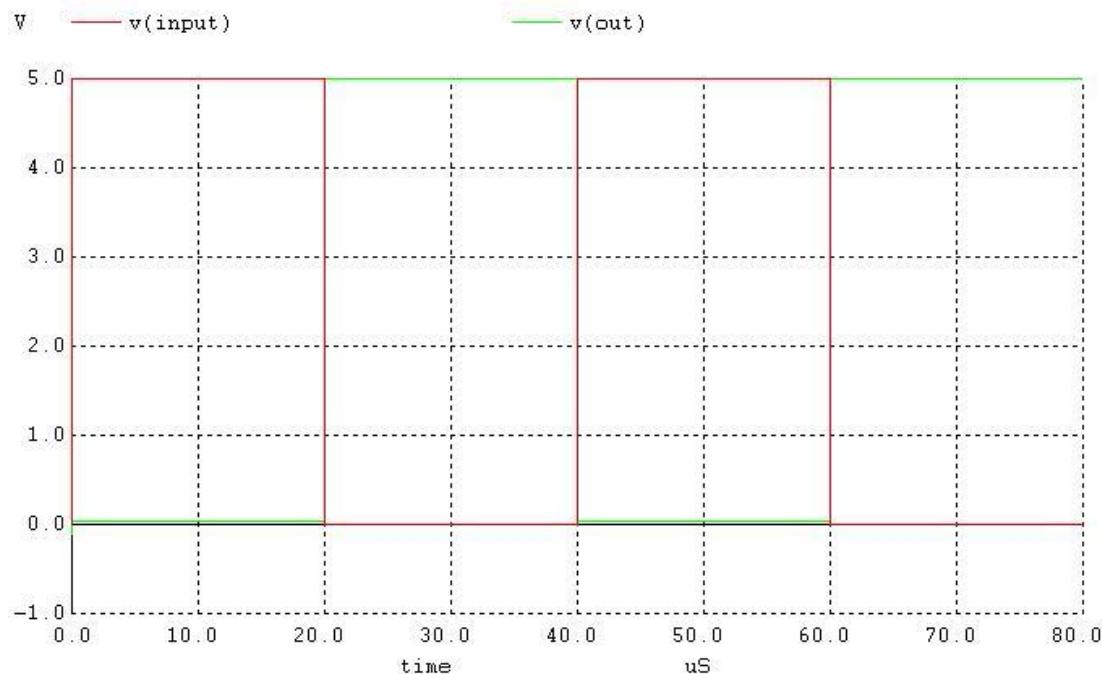
x1 out1 out vcc_node 0 ttl
x2 out2 out vcc_node 0 ttl
x3 out3 out vcc_node 0 ttl
x4 out4 out vcc_node 0 ttl
x5 out5 out vcc_node 0 ttl
x6 out6 out vcc_node 0 ttl
x7 out7 out vcc_node 0 ttl

.dc Vin 0 5 0.001

.control
run
plot v(input) v(out) v(out1)
.endc
.end
```

SIMULATION RESULTS AND PRACTICAL CALCULATIONS

1. Transient Analysis



For Low to High:

$$t_1 = 2.0025\text{us}, t_2 = 2.0039\text{us}$$

$$t_{\text{LH}} = 1.4\text{ns}$$

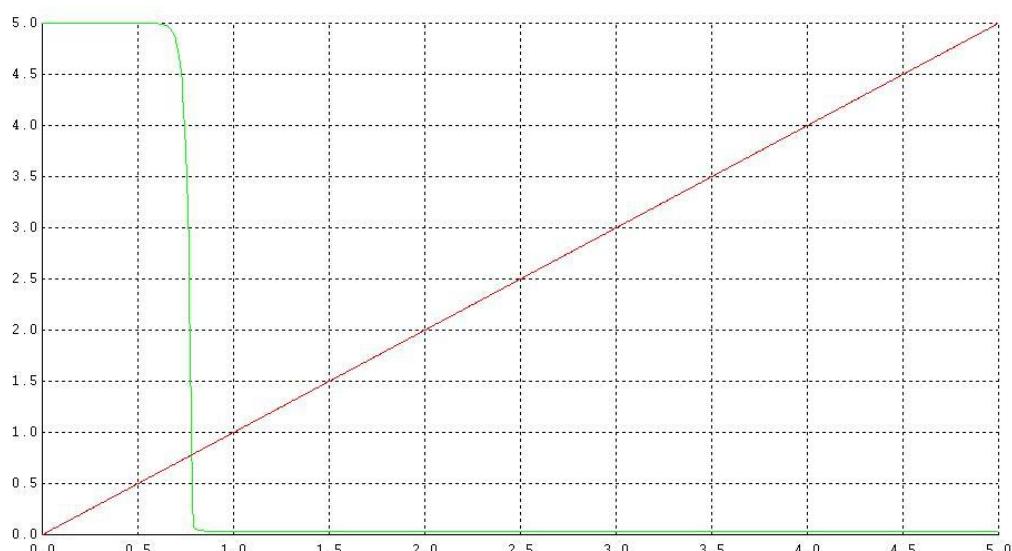
For High to Low

$$t_1 = 40.00125, t_2 = 40.0015$$

$$t_{\text{HL}} = 1.25\text{ns}$$

Propagation Delay = 1.325ns

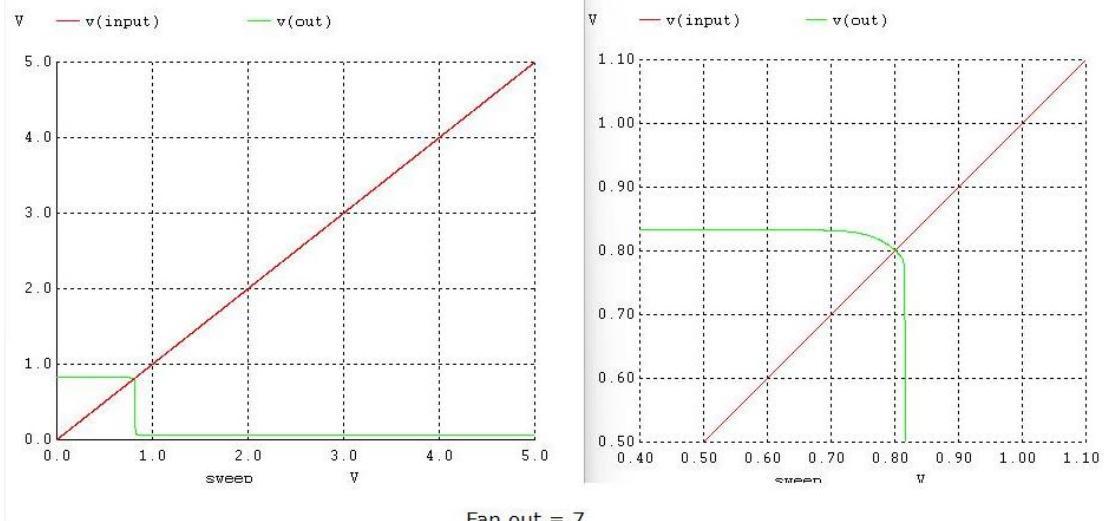
2. VTC and noise Margin



$$V_{ih} = 0.8V, V_{il} = 0.65V, V_{oh} = 5V, V_{ih} = 0.8V$$

$$NM_l = 0.591V, NM_H = 4.2V, NM = 0.591V$$

3. Fan-out



CONCLUSION

In this practical we have implemented spice code TTL inverter and found out its VTC, Noise margin, Propagation delay and fanout. It was observed that the propagation delay of TTL family is lower than DTL

AIM

Aim: To design and verify the performance of given Resistively Loaded NMOS inverter circuit to obtain $V_{OL} = 0.147V$ for the given specifications:

$K_n' = 20\text{pA/V}$, $V_{TO} = 0.8\text{V}$, $V_{DD} = 5\text{V}$, $W/L = 2\mu\text{m}/1\mu\text{m}$.

Find the noise margin of the circuit. Also see the effect of change in R_L on noise margin and comment on it.

THEORY

When the input of the driver transistor is less than threshold voltage V_{TH} ($V_{in} < V_{TH}$), driver transistor is in the cut – off region and does not conduct any current. So, the voltage drop across the load resistor is ZERO and output voltage is equal to the V_{DD} . Now, when the input voltage increases further, driver transistor will start conducting the non-zero current and NMOS goes in saturation region.

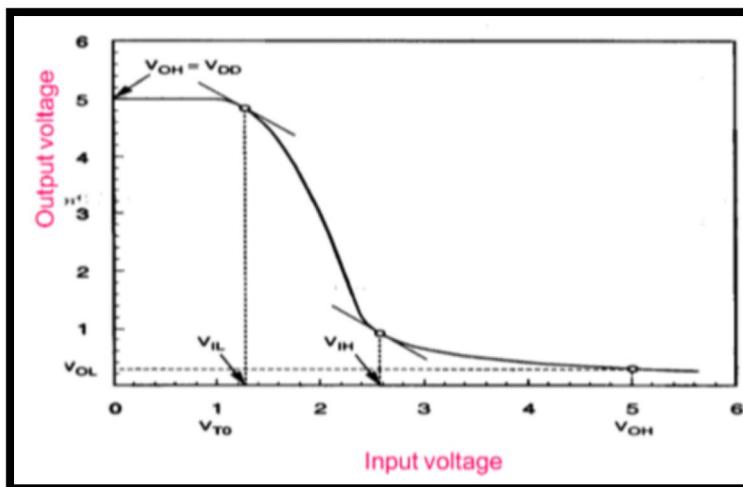
Mathematically,

$$I_D = K_n 2[V_{GS} - V_{TO}]^2 \quad I_D = K_n 2[V_{GS} - V_{TO}]^2$$

Increasing the input voltage further, driver transistor will enter into the linear region and output of the driver transistor decreases.

$$I_D = K_n 2[V_{GS} - V_{TO}]V_{DS} - V_2 \quad I_D = K_n 2[V_{GS} - V_{TO}]V_{DS} - V_{DS2}$$

VTC of the resistive load inverter, shown below, indicates the operating mode of driver transistor and voltage points.



Inverter with N type MOSFET Load

The main advantage of using MOSFET as load device is that the silicon area occupied by the transistor is smaller than the area occupied by the resistive load. Here, MOSFET is active load and inverter with active load gives a better performance than the inverter with resistive load.

Formulas:

- Theoretical formula of V_{OL}

$$V_{OL} = V_{DD} - V_{TO} + \frac{1}{k_n R_L} - \sqrt{\left(V_{DD} - V_{TO} + \frac{1}{k_n R_L} \right)^2 - \frac{2 V_{DD}}{k_n R_L}}$$

- Given parameters
- $V_{OL} = 0.147V$, $k_n' = 20\mu A/V$, $V_{TO} = 0.8V$, $VDD = 5V$, $W/L = 2\mu m/1\mu m$.
Find the R_L from above equation. $RL=200k$
- Using below equation and finding theoretical values of V_{IL} and V_{IH}

$$V_{IL} = V_{TO} + \frac{1}{k_n R_L}$$

$$V_{IH} = V_{TO} + \sqrt{\frac{8}{3} \cdot \frac{V_{DD}}{k_n R_L} - \frac{1}{k_n R_L}}$$

- Model declaration for NMOS transistor is
.model mymos NMOS V_{t0}=0.8 kp=20u
M1 drain gate source substrate mymos w=2um L=2um

Circuit Diagram

Theoretical Calculations

SPICE CODE

16.

```
# NMOS
.model mymos NMOS (Vt0=0.8, Kt=20u)

.subckt mosinverter in vdd_node out gnd
    M1 out in gnd gnd mymos w=2um l=1um
    RL vdd_node out 200k
.ends mosinverter

xd input vdd_node out 0 mosinverter

Vdd vdd_node 0 5
Vin input 0 5

.dc Vin 0 5 0.005

.control
run
plot v(input) v(out)
.endc
.end
```

17.

```
*U19Ec046 Resistively Loaded NMOS Inverter DC Analysis

.model mynmos nmos Vto=0.8 kp=20u

M1 out in 0 0 mynmos w=2u l=1u
R1 1 out 200k
Vdd 1 0 5
Vin in 0 pulse (0 5 1ns 1ns 1ns 20ns 40ns)

.tran 1ns 50ns

.control
run
plot V(in) V(out)
.endc
.end
```

18.

```
# NMOS
.model mymos NMOS (Vt0=0.8, Kt=20u)

.subckt mosinverter in vdd_node out gnd
    M1 out in gnd gnd mymos w=2um l=1um
    RL vdd_node out 100k
.ends mosinverter
```

```

.subckt mosinverter2 in vdd_node out gnd
    M1 out in gnd gnd mymos w=2um l=1um
    RL vdd_node out 200k
.ends mosinverter2

.subckt mosinverter3 in vdd_node out gnd
    M1 out in gnd gnd mymos w=2um l=1um
    RL vdd_node out 300k
.ends mosinverter3

.subckt mosinverter4 in vdd_node out gnd
    M1 out in gnd gnd mymos w=2um l=1um
    RL vdd_node out 400k
.ends mosinverter4

xd input vdd_node out_100k 0 mosinverter
xd1 input vdd_node out_200k 0 mosinverter2
xd2 input vdd_node out_300k 0 mosinverter3
xd3 input vdd_node out_400k 0 mosinverter4

Vdd vdd_node 0 5
Vin input 0 5

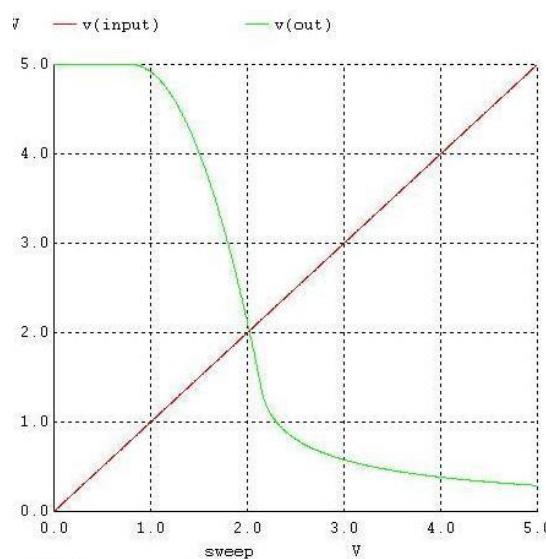
.dc Vin 0 5 0.005

.control
run
plot v(input) v(out_100k) v(out_200k) v(out_300k) v(out_400k)
.endc
.end

```

SIMULATION RESULTS AND PRACTICAL CALCULATIONS

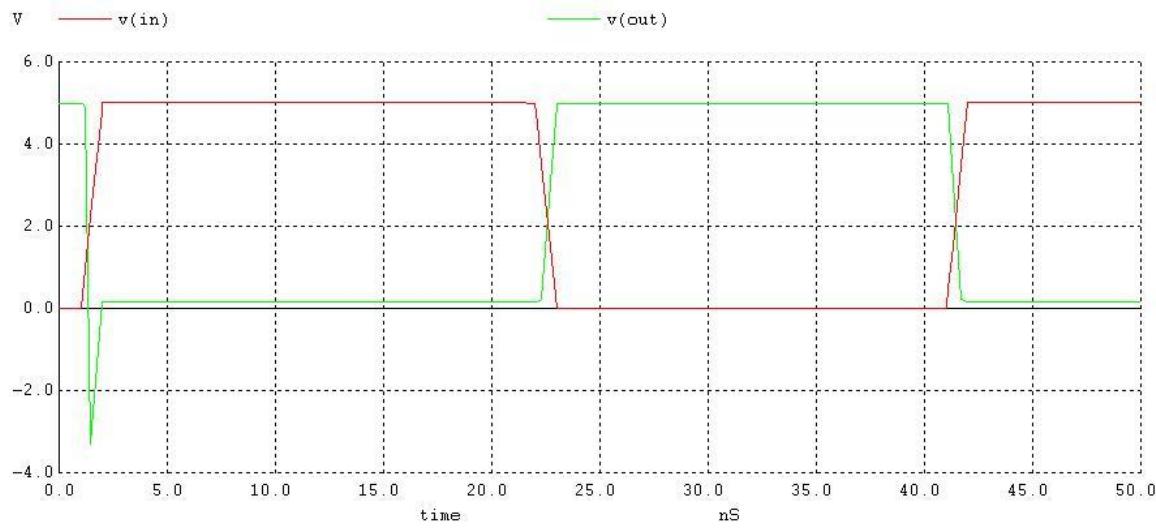
1.



[28-02 14:46] SUTHAR HARSH MUKESHBHAI HARSH

$V_{il} = 1.1V$
 $v_{ih} = 2.4V$
 $v_{oh} = 5V$
 $v_{ol} = 0.3V$
 $V_{TH} = 2V$
 $NM_L = 0.8V$
 $NM_H = 2.6V$
 $NM = 0.8V$

2.

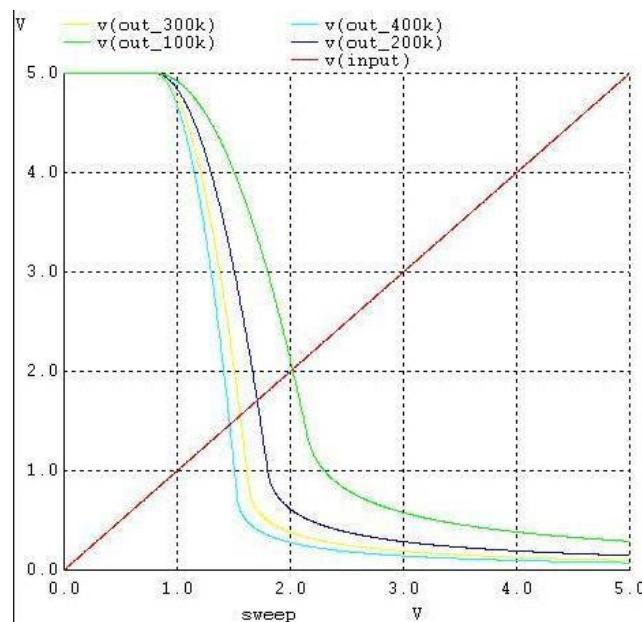


$$t_{PHL} = t_1 - t_2 = (40.0092 - 40.0013) \text{ s} = 7.9 \text{ nS}$$

$$t_{PLH} = t_1' - t_2' = (20.135 - 20.0025) \text{ s} = 132.5 \text{ nS}$$

Propagation delay,
 $= t_{PLH} + t_{PHL} = 132.5 + 7.92 = 140.42 \text{ nS}$
 $T_r = (20.46 - 20.0175) \text{ s} = 442.5 \text{ nS}$
 $T_f = (40.0223 - 40.00312) \text{ s} = 19.18 \text{ nS}$

3.



CONCLUSION

AIM

Design and verify the performance of given saturated loaded NMOS inverter circuit to obtain V_{ih} -2.9, for the given design parameter $V_{DD}=5V$, $K_n'=20\mu A/V^2$, $V_{tl}-0.8V$, $V_{tl}=0.8V$, $(W/L)_{driver}=2\mu m/\mu m$.

- a) Compare the theoretical and practical values of the critical voltages on VTC& find noise margins of the circuit.
- b) observe the effect of change in (W/L) loaded on noise margin &comment on it.
- c) Also compare the results of noise with resistive loaded NMOS inverter for $R_L=200k$

THEORY

Saturated load device. An n-channel enhancement-mode MOSFET with the gate connected to the drain can be used as load device in an NMOS inverter. Since the gate and drain of the transistor are connected, we have $V_{GS}-V_{DS}$ When $V_{GS}-V_{DS} > V_{TN}$, a non zero drain current is induced in the transistor and thus the transistor operates in saturation only.

CIRCUIT

CALCULATIONS

SPICE CODE

19.

```
*saturated load inverter static analysis
.model mymos NMOS (Vt0=0.8 kp=20u)
M1 1 1 out 0 mymos l=1u w=2u
M2 out in 0 0 mymos l=1u w=2u
Vdd 1 0 5V
Vin in 0 5V
.dc Vin 0 5 0.05
.control
run
plot V(out) V(in)
.endc
.end
```

20.

```
*saturated load inverter static analysis
.model mymos NMOS (Vt0=0.8 kp=20u)
M1 d1 d1 out 0 mymos l=1u w=2u
M2 out in 0 0 mymos l=1u w=2u
Vdd1 d1 0 5V
M11 d2 d2 out1 0 mymos l=1u w=4u
M21 out1 in 0 0 mymos l=1u w=2u
Vdd2 d2 0 5V
M12 d3 d3 out2 0 mymos l=1u w=6u
M22 out2 in 0 0 mymos l=1u w=2u
Vdd3 d3 0 5V
M13 d4 d4 out3 0 mymos l=1u w=8u
M23 out3 in 0 0 mymos l=1u w=2u
Vdd4 d4 0 5V
Vin in 0 5V
.dc Vin 0 5 0.05
.control
run
plot V(out) V(out1) V(out2) V(out3) V(in)
.endc
.end
```

21.

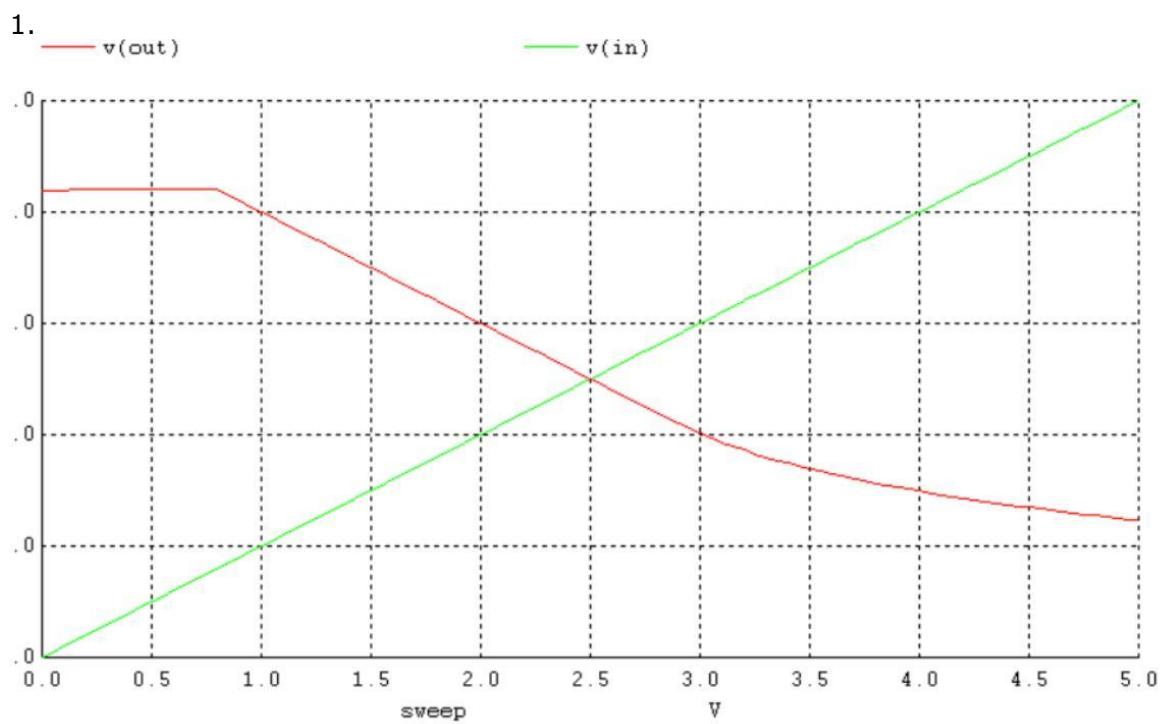
```
*saturated load inverter static analysis
.model mymos NMOS (Vt0=0.8 kp=20u)
M1 d1 d1 out 0 mymos l=1u w=2u
M2 out in 0 0 mymos l=1u w=2u
Vdd1 d1 0 5V
M11 d2 d2 out1 0 mymos l=1u w=4u
M21 out1 in 0 0 mymos l=1u w=2u
Vdd2 d2 0 5V
M12 d3 d3 out2 0 mymos l=1u w=6u
```

```

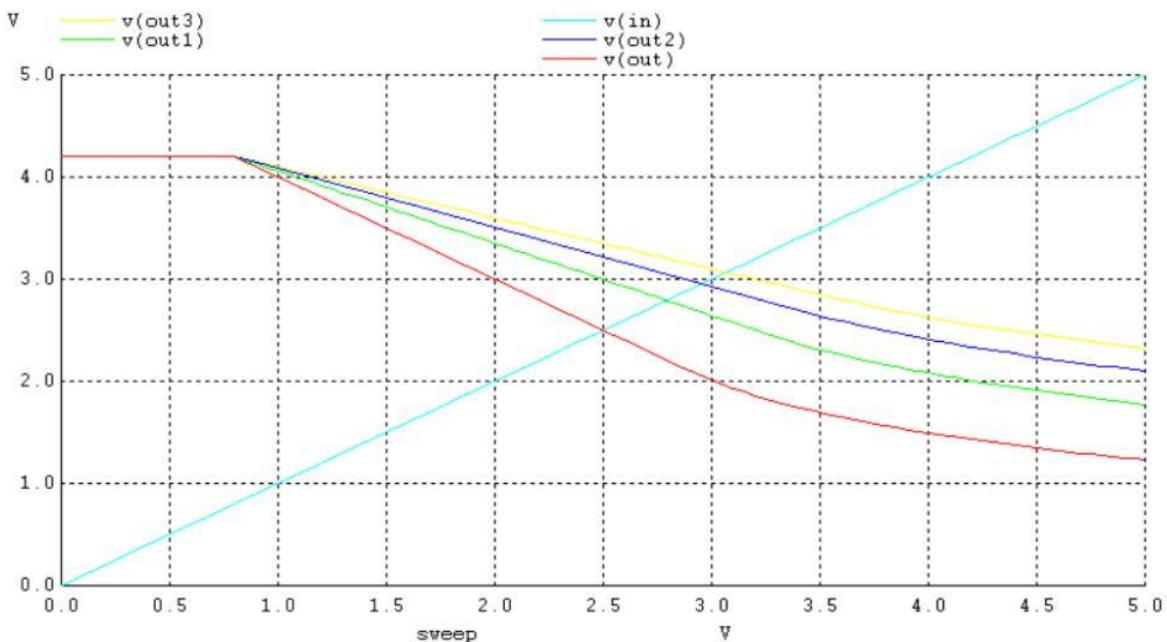
M22 out2 in 0 0 mymos l=1u w=2u
Vdd3 d3 0 5V
M13 d4 d4 out3 0 mymos l=1u w=8u
M23 out3 in 0 0 mymos l=1u w=2u
Vdd4 d4 0 5V
Vin in 0 5V
.dc Vin 0 5 0.05
.control
run
plot V(out) V(out1) V(out2) V(out3) V(in)
.endc
.end

```

SIMULATION RESULTS AND PRACTICAL CALCULATIONS



2.



3.

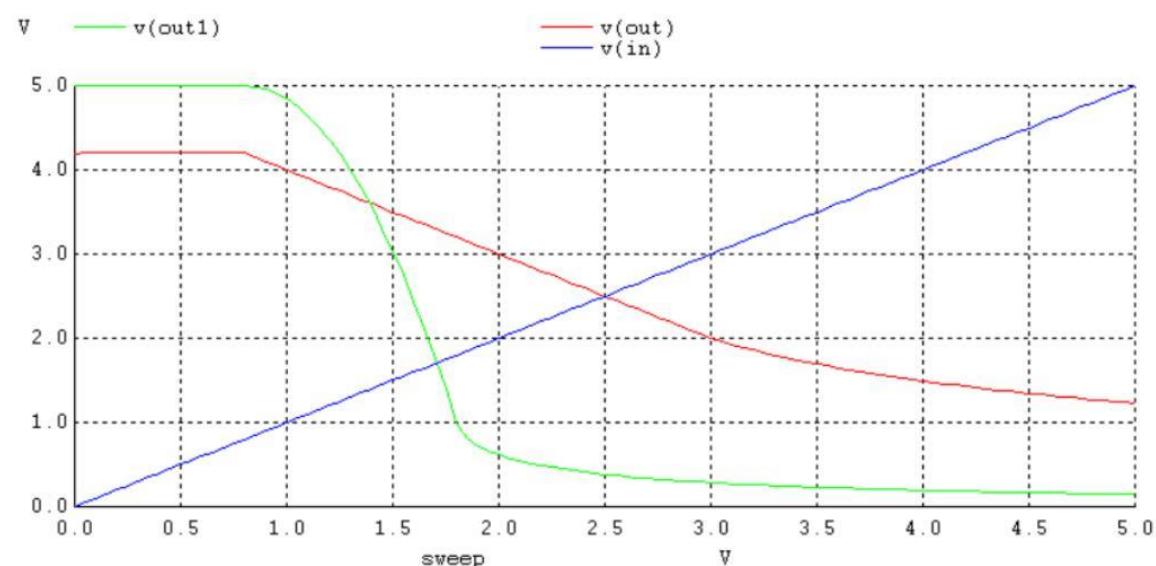


TABLE OF THEORETICAL AND PRACTICAL CALCULATION

Parameters	Theoretical values	Practically Values
VOL	2.1 V	1.23 V
VOH	4.2 V	4.2 V
VIL	0.8 V	0.85 V
VIH	2.9 V	3.2 V
VTH	2.5 V	2.5 V
NML	1.3 V	0.38 V
NMH	1.3 V	1.18 V

Comparison Of Noise Margin of Resistively and Saturated Loaded NMOS inverter.

	NML	NMH
--	------------	------------

Resistively Loaded NMOS	0.802 V	3.12 V
Saturated Loaded NMOS	0.302 V	1.18 V

CONCLUSION

U19EC046 | DIC LAB 8

AIM

Design and verify the performance of given CMOS inverter circuit to obtain switching threshold voltage of 2.2V. Given specifications for the CMOS inverter are:

$$VTN = 0.8V, VTP = -1V, VDD = 5V, Kn' = 20\mu A/V^2, Kp' = 50\mu A/V^2, L_n = L_p = 1\mu m.$$

Compare the theoretical and practical values of critical voltages on VTC and find the noisemargin of the circuit. Observe the following parameters and comment on it.

1. Variation of VDD from 5V to 3.3V on the switching threshold voltage of CMOSinverter.

Variation of Kr at 0.25, 1 and 4 on the switching characteristics.

THEORY

The term CMOS stands for “Complementary Metal Oxide Semiconductor”. CMOS technology is one of the most popular technology in the computer chip design industry and broadly used today to form integrated circuits in numerous and varied applications. Today's computer memories, CPUs and mobile phones make use of this technology due to several key advantages. This technology make use of both p-channel (PMOS) and n- channel (NMOS) semiconductor devices.

The main advantage of CMOS over NMOS and bipolar technology is the much smaller powerdissipation. Unlike NMOS or BIOPOLAR circuits, a complementary MOS circuit has almost no static power dissipation. Power is only dissipated in case the circuit actually switches. VTC Characteristics are more symmetrical in CMOS than NMOS and noise margin offered is muchhigher. This allows integrating more CMOS gates on an IC than in MOS or bipolar technology, resulting in much better performance.

Circuit Diagram

Calculations

SPICE CODE

22.

```
# CMOS
.model mynmos NMOS (Vt0=0.8, Kp=50u)
.model mypmos PMOS (Vt0=-1, Kp=20u)

.subckt cmosinverter in vdd_node out gnd
    MN out in gnd gnd mynmos w=1um l=1um
    MP vdd_node in out vdd_node mypmos w=1.51um l=1um
.ends cmosinverter

Vdd vdd_node 0 5
Vin input 0 5

Xd input vdd_node out 0 cmosinverter

.dc Vin 0 5 0.005 Vdd 3.3 5 1.7

.control
run
plot v(input) v(out)
.endc
.end
```

23.

```
# CMOS
.model mynmos NMOS (Vt0=0.8, Kp=50u)
.model mypmos PMOS (Vt0=-1, Kp=20u)

.subckt cmosinverter in vdd_node out gnd
    MN out in gnd gnd mynmos w=1um l=1um
    MP vdd_node in out vdd_node mypmos w=1.51um l=1um
.ends cmosinverter

Vdd vdd_node 0 5
Vin input 0 pulse(0 5 1ns 1ns 1ns 20us 40us)

Xd input vdd_node out 0 cmosinverter

.tran 1ns 80us

.control
run
plot v(input) v(out)
.endc
.end
```

24.

```
# CMOS
.model mynmos NMOS (Vt0=0.8, Kp=50u)
```

```

.model mypmos PMOS (Vt0=-1, Kp=20u)

.subckt cmosinverter in vdd_node out gnd
    MN out in gnd gnd mynmos w=0.02um l=1um
    MP vdd_node in out vdd_node mypmos w=0.05um l=1um
.ends cmosinverter

.subckt cmosinverter2 in vdd_node out gnd
    MN out in gnd gnd mynmos w=0.02um l=1um
    MP vdd_node in out vdd_node mypmos w=0.2um l=1um
.ends cmosinverter2

.subckt cmosinverter3 in vdd_node out gnd
    MN out in gnd gnd mynmos w=0.08um l=1um
    MP vdd_node in out vdd_node mypmos w=0.05um l=1um
.ends cmosinverter3

Vdd vdd_node 0 5
Vin input 0 5

Xd input vdd_node kr_0_25 0 cmosinverter
Xd2 input vdd_node kr_1 0 cmosinverter2
Xd3 input vdd_node kr_4 0 cmosinverter3

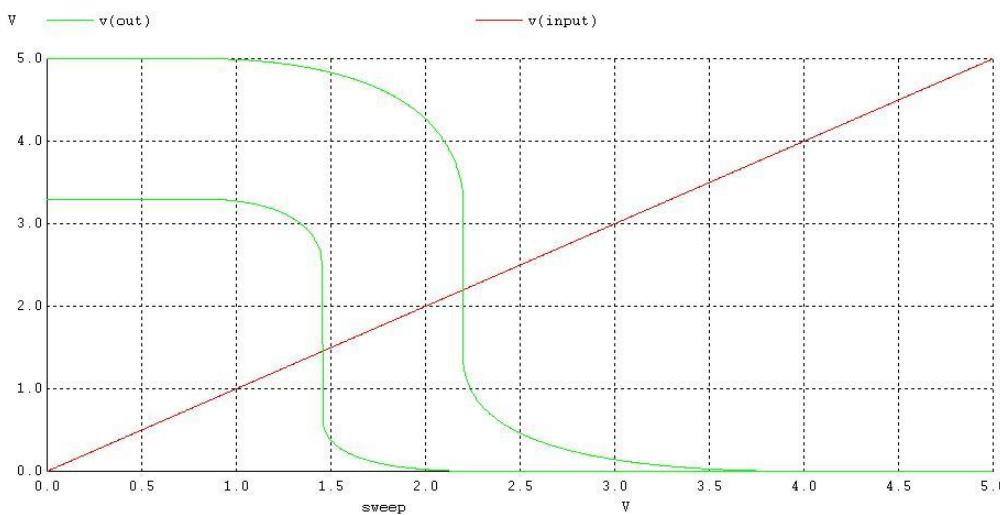
.dc Vin 0 5 0.005

.control
run
plot v(input) v(kr_0_25) v(kr_1) v(kr_4)
.endc
.end

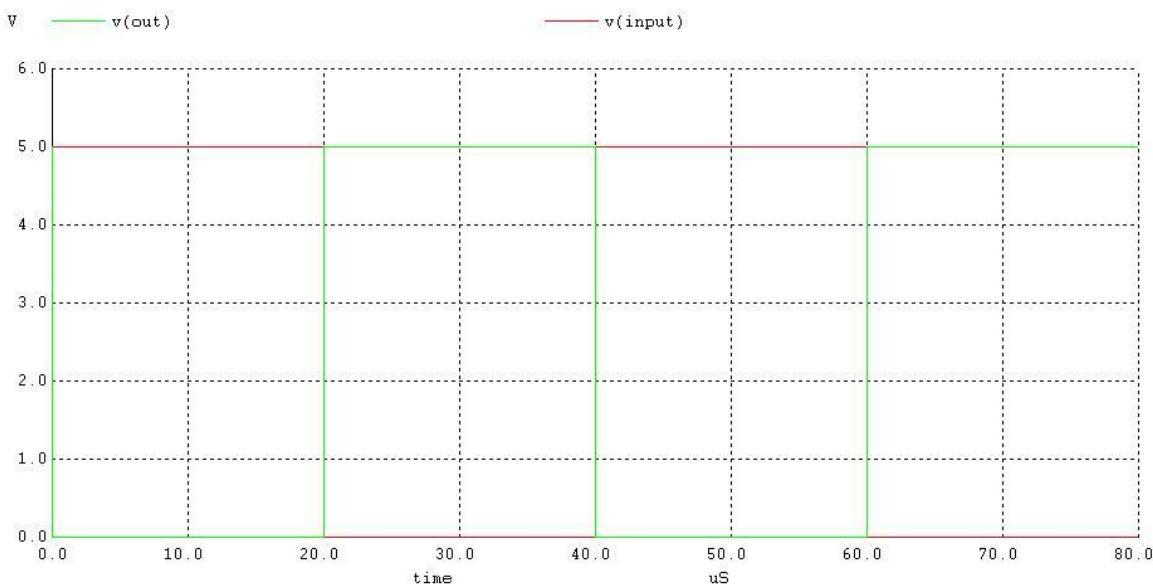
```

SIMULATION RESULTS AND PRACTICAL CALCULATIONS

1.



2.



3.

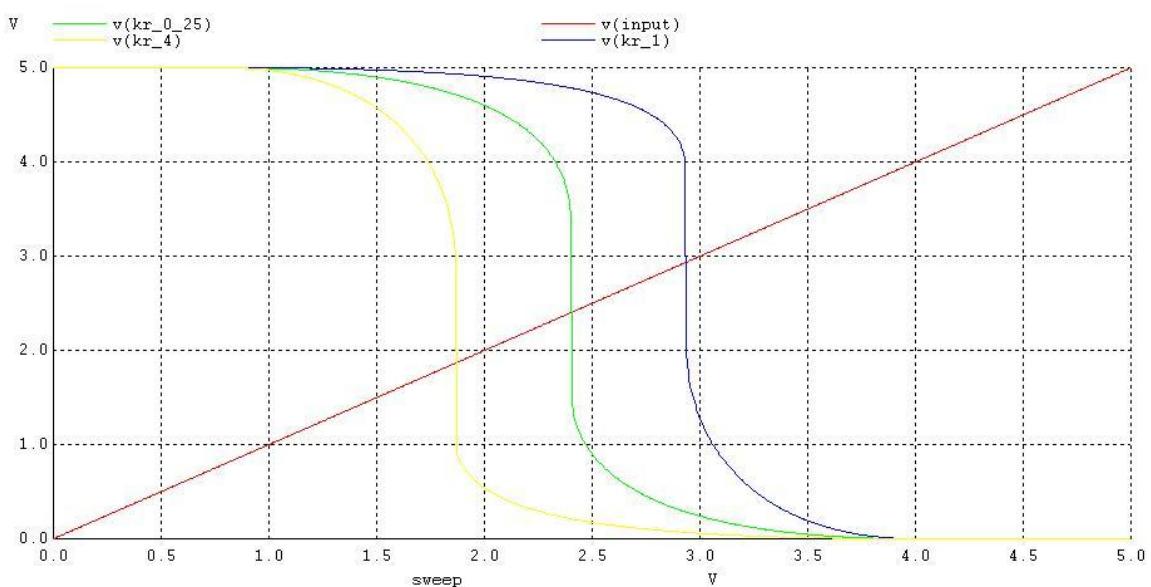


TABLE OF THEORETICAL AND PRACTICAL CALCULATION

Table 1: Noise Margin

Parameters	Theoretical	Practical
V_{OH}	5 V	5 V
V_{OL}	0 V	0 V
V_{IH}		2.20 V
V_{IL}	1.728 V	2.15 V
V_{TH}	2.2 V	2.196 V
Noise Margin High		2.8 V
Noise Margin Low	1.728 V	2.15 V
Noise Margin		2.15 V

Table 2: Effect of VDD variation on VTH

VDD (V)	VTH (V)
5	2.813
4	1.776
3	1.326

Table 3: Effect of kr variation on VTH

kr	VTH (V)
0.25	2.9257
1	2.412
4	1.872

CONCLUSION

AIM

Write a winspice code to verify the functionality of given bimcos inverter circuit using default model parameters for the transistor.

THEORY

Introduction

The history of semiconductor devices starting 1930's when Lienfed and Heil first proposed the mosfet. Bipolar Technology was started in 1980's. CMOS Technology was also started in mid 1980's. Later in 1990 there was a cross over between bipolar and CMOS Technology.

In BiCMOS technology, both the MOS and bipolar device are fabricated on the same chip.

The objective of the BiCMOS is to combine bipolar and CMOS so as to exploit the advantages of both the technologies.

Today BiCMOS has become one of the dominant technologies used for high speed, low power and highly functional VLSI circuits.

The process steps required for both CMOS and bipolar are similar so the BiCMOS process has been enhanced and integrated into the CMOS process without any additional steps.

The primary approach to realize high performance BiCMOS devices is the addition of bipolar process steps to a baseline CMOS process.

The BiCMOS gates could be used as an effective way of speeding up the VLSI circuits. The applications of BiCMOS are vast.

Advantages of bipolar and CMOS circuits can be retained in BiCMOS chips.

- BiCMOS technology enables high performance integrated circuits IC's but increases process complexity..
- CMOS technology offers less power dissipation, smaller noise margins, and high packing density.
- Bipolar technology, on the other hand, ensure high switching and I/O speed and good noise performance. Now we are in 3rd Generation BiCMOS Technology.
- BiCMOS technology accomplishes both improved speed over CMOS and lower power dissipation than bipolar technology.
- The main drawback of BiCMOS technology is the higher costs due to the added process complexity.
- This greater process complexity in BiCMOS results in a cost increase compared to conventional CMOS technology.

Circuit Diagram

SPICE CODE

25.

```
.model q1 npn bf=50
.model mynmos nmos Vto=0.8 Kp=50
.model mypmos pmos Vto=-1 Kp=20

.subckt BI in vdd_node out1 out2 src
M1 out1 in src src mynmos w=1u l=1u
M2 out2 in vdd_node vdd_node mypmos w=1.51u l=1u
.ends BI

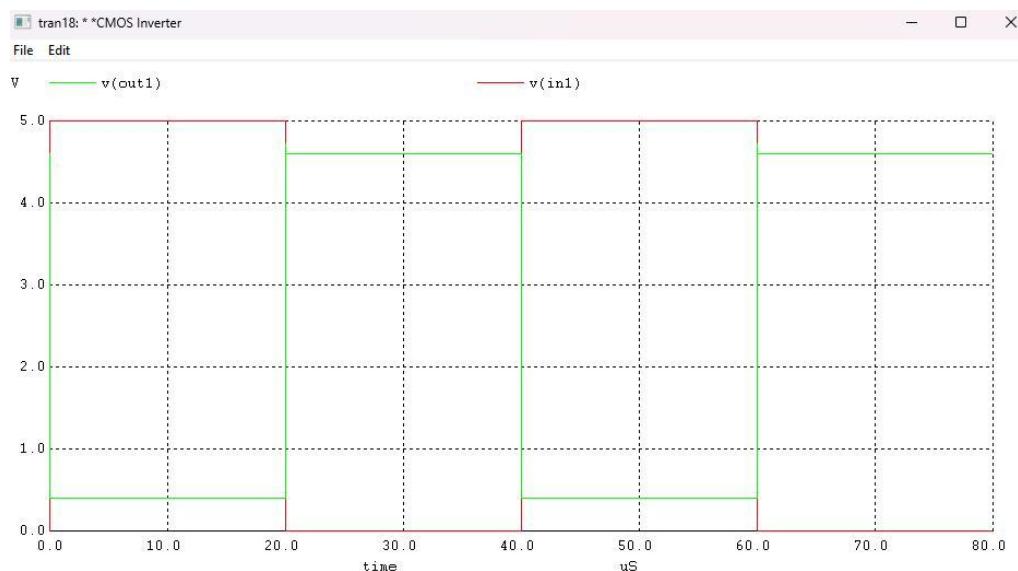
q11 vdd_node out2 out1 q1
q12 out1 src 0 q1
xd1 in1 vdd_node out1 out2 src BI
Vdd vdd_node 0 5

Vin in1 0 pulse(0 5 1ns 1ns 1ns 20us 40us)

.tran 1ns 80us
.control
run
plot v(in1) v(out1)
.endc
.end
```

SIMULATION RESULTS AND PRACTICAL CALCULATIONS

1.



CONCLUSION

AIM

Write a winspice code to verify the functionality of NOR based SR Latch

THEORY

The SR flip-flop, also known as a SR Latch, can be considered as one of the most basic sequential logic circuit possible. This simple flip-flop is basically a one-bit memory bistable device that has two inputs, one which will “SET” the device (meaning the output = “1”), and is labelled S and one which will “RESET” the device (meaning the output = “0”), labelled R.

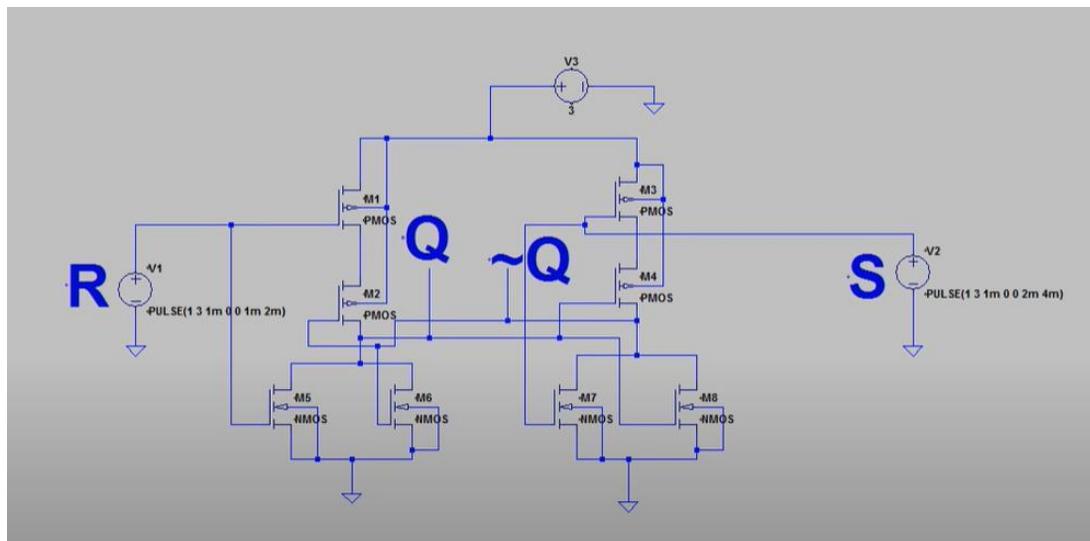
Then the SR description stands for “Set-Reset”. The reset input resets the flip-flop back to its original state with an output Q that will be either at a logic level “1” or logic “0” depending upon this set/reset condition.

A basic NAND gate SR flip-flop circuit provides feedback from both of its outputs back to its opposing inputs and is commonly used in memory circuits to store a single data bit. Then the SR flip-flop actually has three inputs, Set, Reset and its current output Q relating to it's current state or history.

The term “Flip-flop” relates to the actual operation of the device, as it can be “flipped” into one logic Set state or “flopped” back into the opposing logic Reset state.

Circuit Diagram

CIRCUIT DIAGRAM



SPICE CODE

26.

**CMOS Inverter*

```
.model mynmos nmos Vto=0.8 Kp=50
```

```

.model mypmos pmos Vto=-1 Kp=20

Mn1 n_mn1_drain n_mn1_gate 0 0 mynmos w=1u l=1u
Mn2 n_mn1_drain n_mn2_gate 0 0 mynmos w=1u l=1u
Mp1 n_mp1_drain n_mp1_source n_mp1_source mypmos w=1.51u l=1u
Mp2 n_mn1_drain n_mn2_gate n_mp1_drain n_mp1_source mypmos w=1.51u l=1u

Mn3 n_mn2_gate n_mn3_gate 0 0 mynmos w=1u l=1u
Mn4 n_mn2_gate n_mn1_drain 0 0 mynmos w=1u l=1u
Mp3 n_mp3_drain n_mn3_gate n_mp1_source n_mp1_source mypmos w=1.51u l=1u
Mp4 n_mn2_gate n_mn1_drain n_mp3_drain n_mp1_source mypmos w=1.51u l=1u

Vdd n_mp1_source 0 5

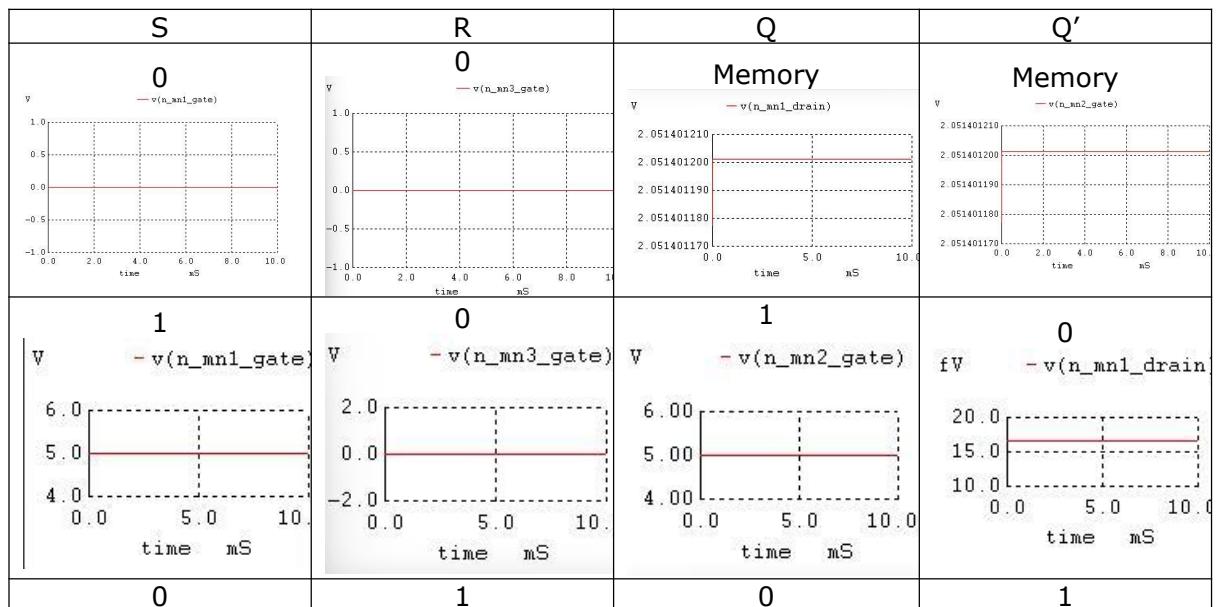
Vin1 n_mn1_gate 0 0
Vin2 n_mn3_gate 0 0

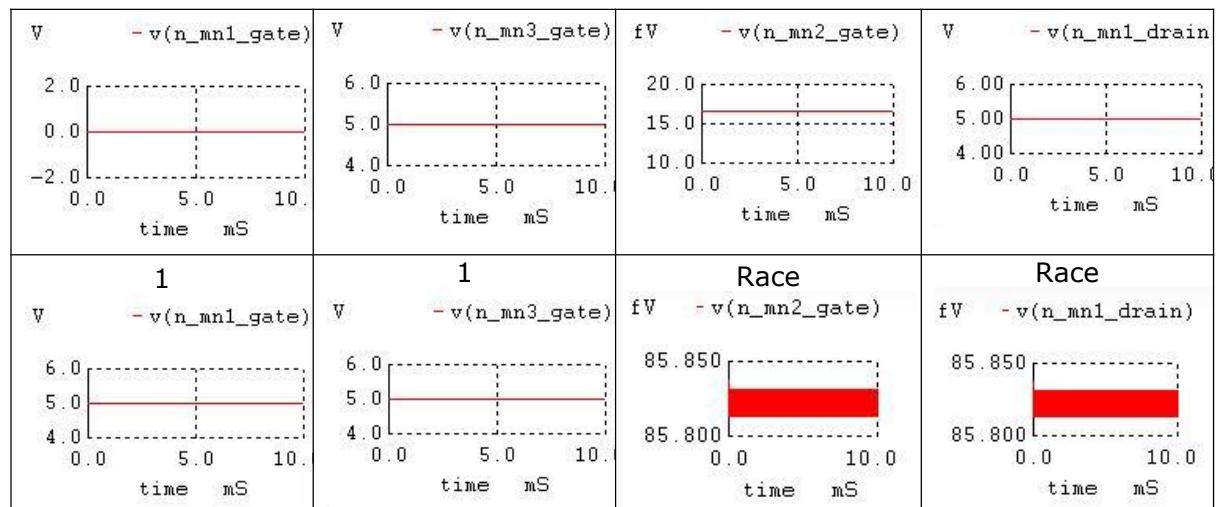
.tran 1us 10ms

.control
run
* plot v(Va)
plot v(n_mn1_gate)
plot v(n_mn3_gate)
plot v(n_mn1_drain)
plot v(n_mn2_gate)
.endc
.end

```

SIMULATION RESULTS





CONCLUSION

AIM

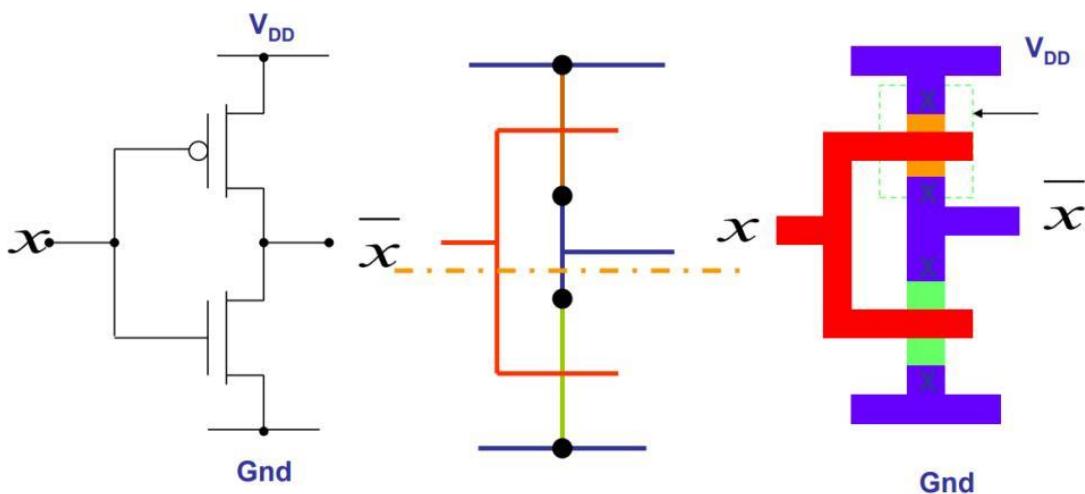
To generate Layout for CMOS inverter circuit and Simulate it for verification.

Software used: DSCH and Microwind Tool

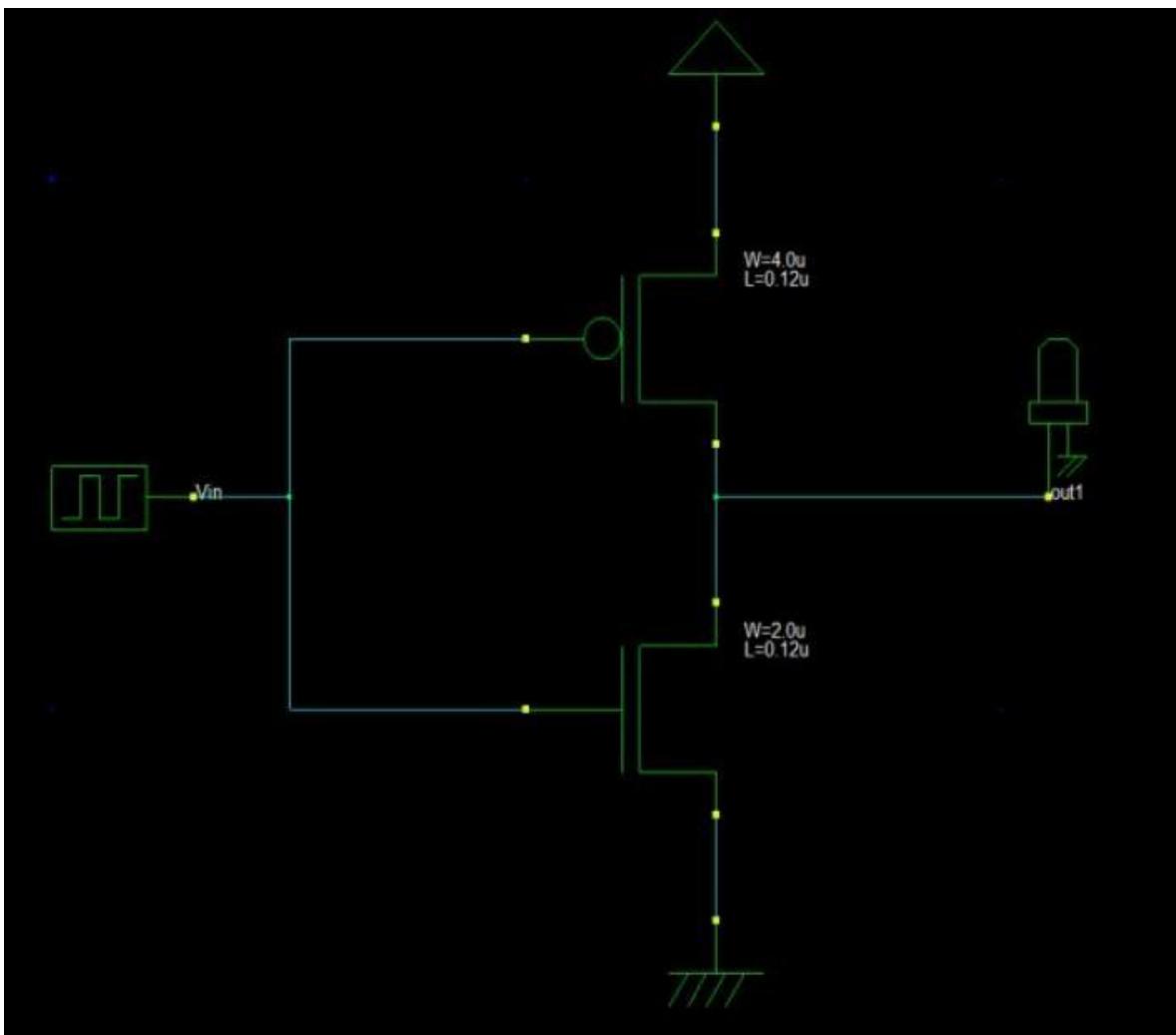
THEORY

The mask layout design of a CMOS inverter will be examined step-by-step. The circuit consists of one nMOS and one pMOS transistor, therefore, one would assume that the layout topology is relatively simple. Yet, we will see that there exist quite a number of different design possibilities even for this very simple circuit.

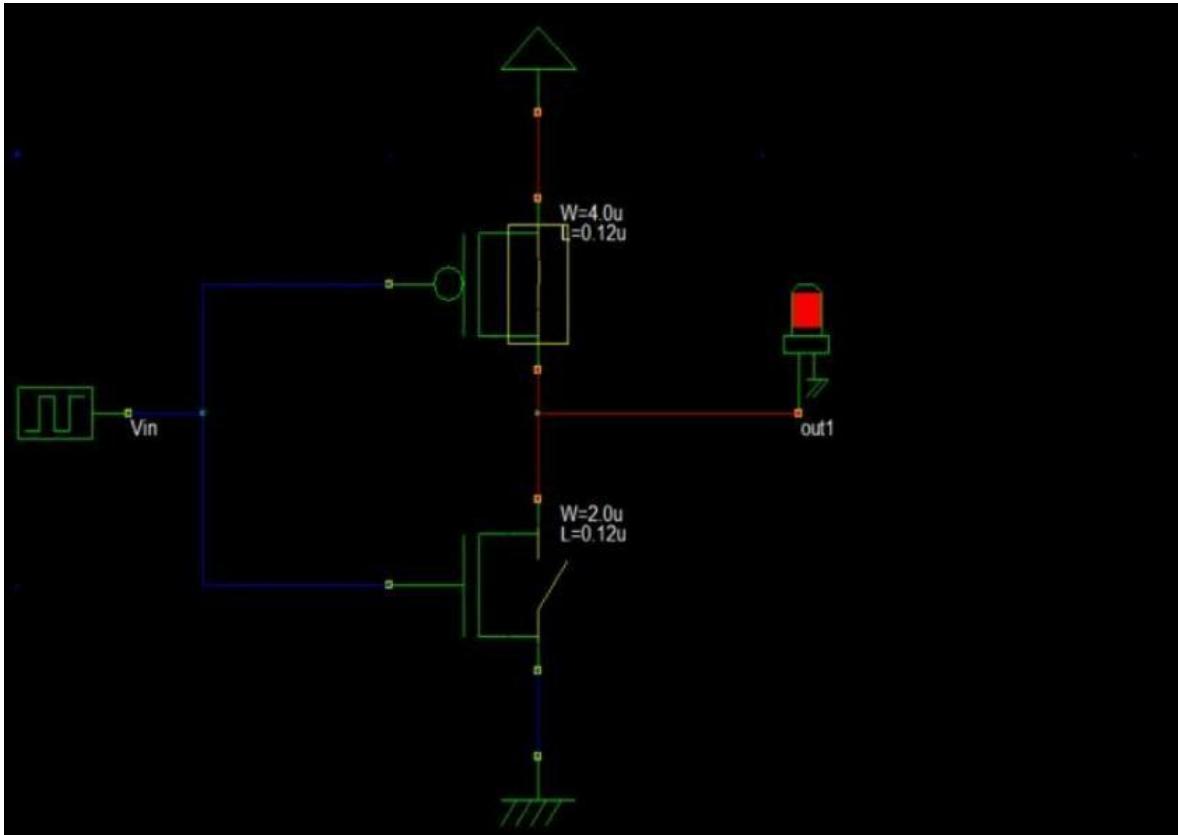
First, we need to create the individual transistors according to the design rules. Assume that we attempt to design the inverter with minimum-size transistors. The width of the active area is then determined by the minimum diffusion contact size (which is necessary for source and drain connections) and the minimum separation from diffusion contact to both active area edges. The width of the polysilicon line over the active area (which is the gate of the transistor) is typically taken as the minimum poly width. Then, the overall length of the active area is simply determined by the following sum: (minimum poly width) + 2 x (minimum poly-to- contact spacing) + 2 x (minimum spacing from contact to active area edge). The pMOS transistor must be placed in an n-well region, and the minimum size of the n- well is dictated by the pMOS active area and the minimum n-well overlap over n+. The distance between the nMOS and the pMOS transistor is determined by the minimum separation between the n+ active area and the n-well. The polysilicon gates of the nMOS and the pMOS transistors are usually aligned. The final step in the mask layout is the local interconnections in metal, for the output node and for the VDD and GND contactsNotice that in order to be biased properly, the n-well region must also have a VDD contact.

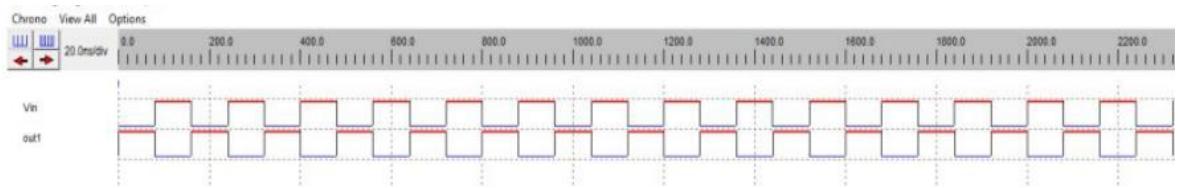


CMOS Invertor in DSCH

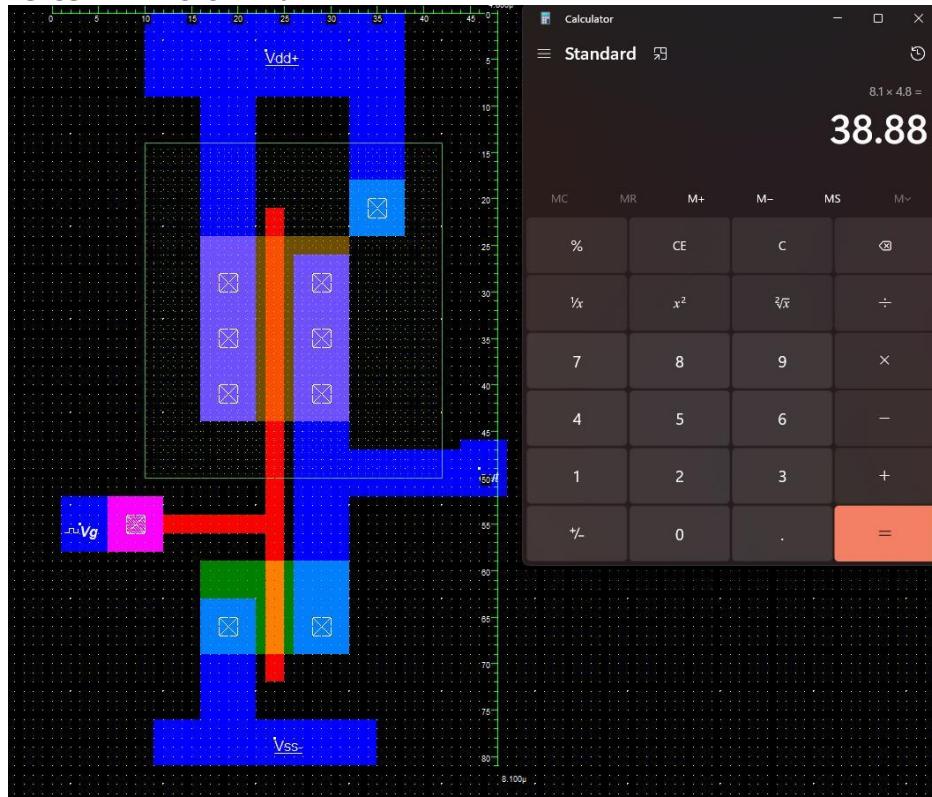


Output

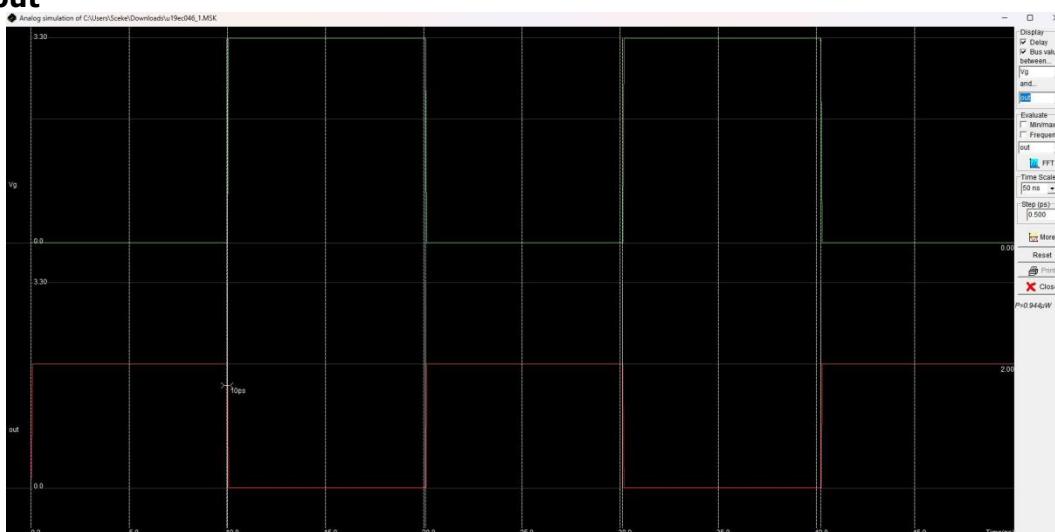




CMOS Inverter in Microwind



Output



CONCLUSION

AIM

To generate Layout for CMOS NAND circuit and Simulate it for verification.

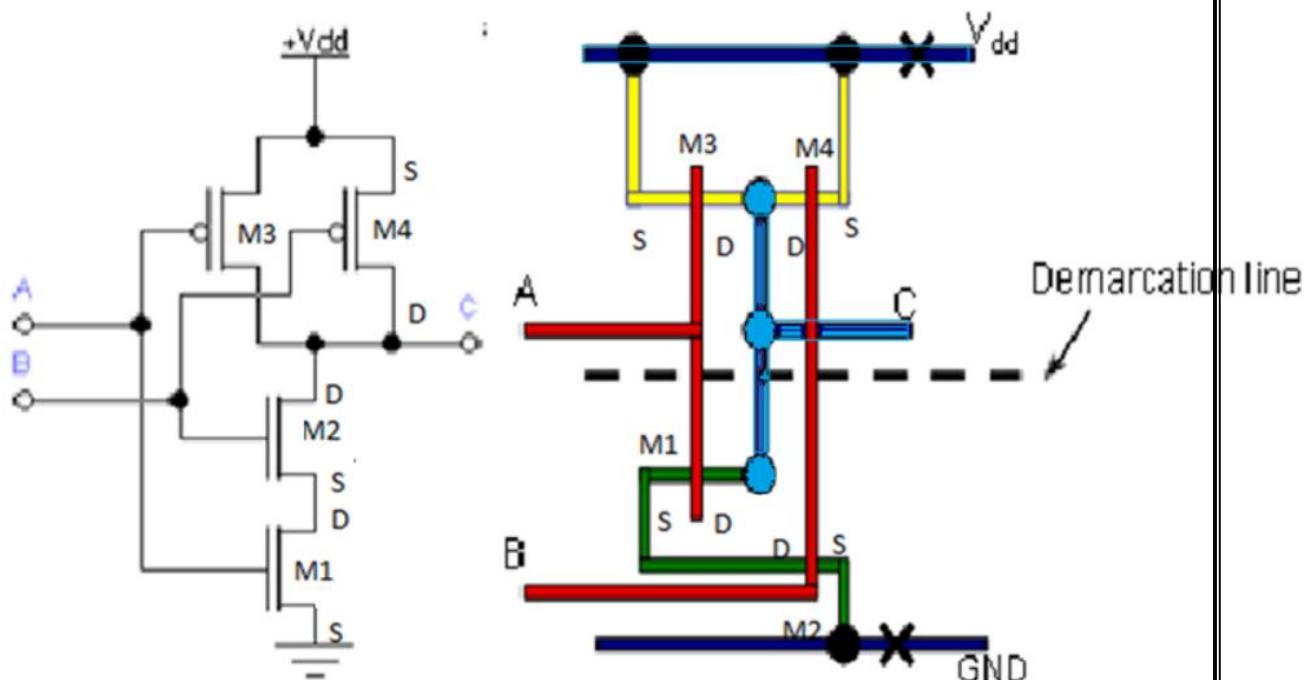
Software used: DSCH and Microwind Tool

THEORY

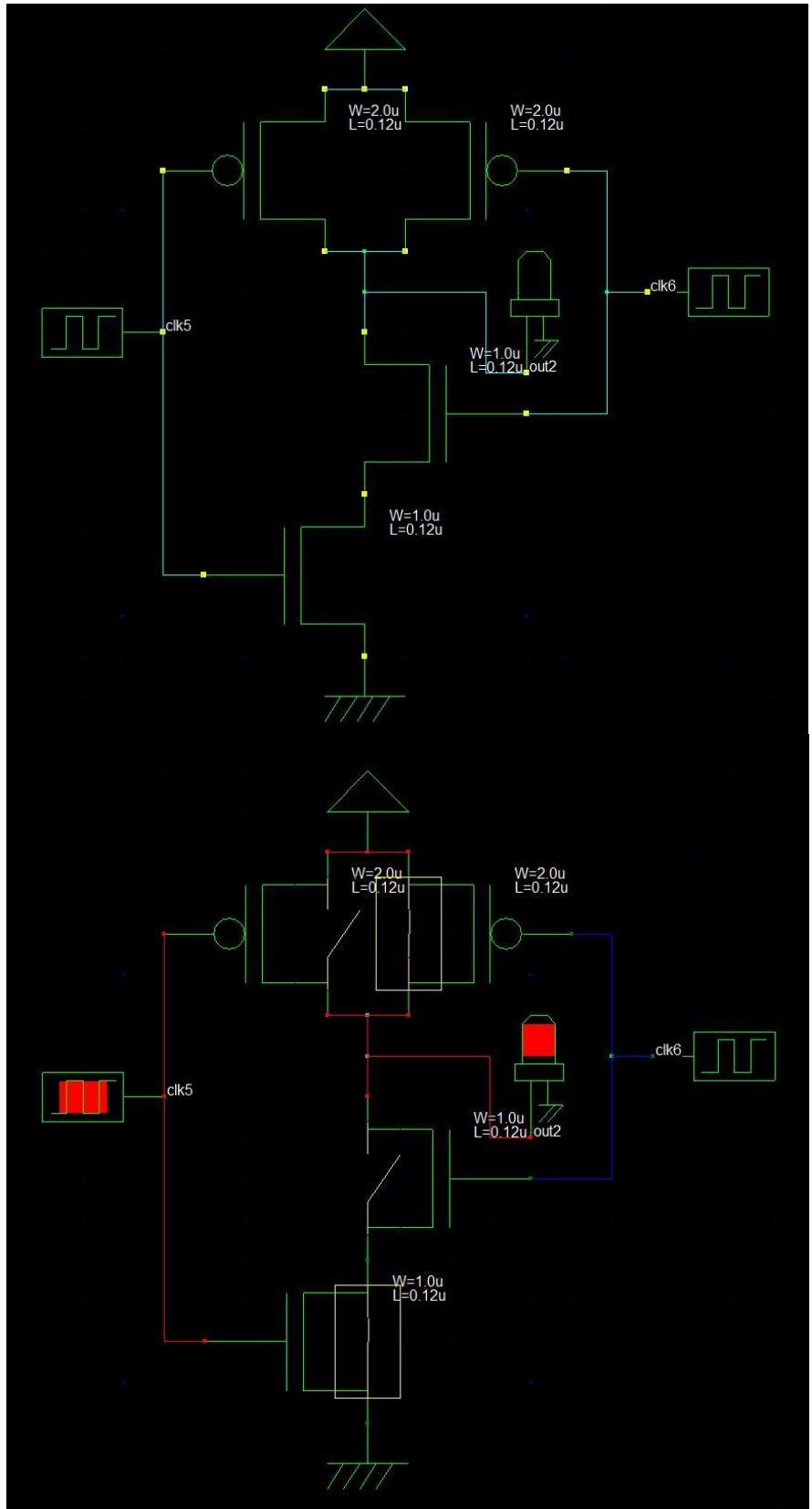
DSCH is software for logic design & based on primitives a hierarchical circuit can be built and simulated & it also includes delay and power consumption evaluation& With the help of this software one can implement digital circuits at its basic gate primitives or at its transistor level. Microwind is a tool for designing and simulating circuits at layout level& The tool features full editing facilities "copy, cut, past, duplicate, move, various views "MOS characteristics6 (2D cross section6 3D process Viewer and an analog simulator.

Truth Table of NAND:

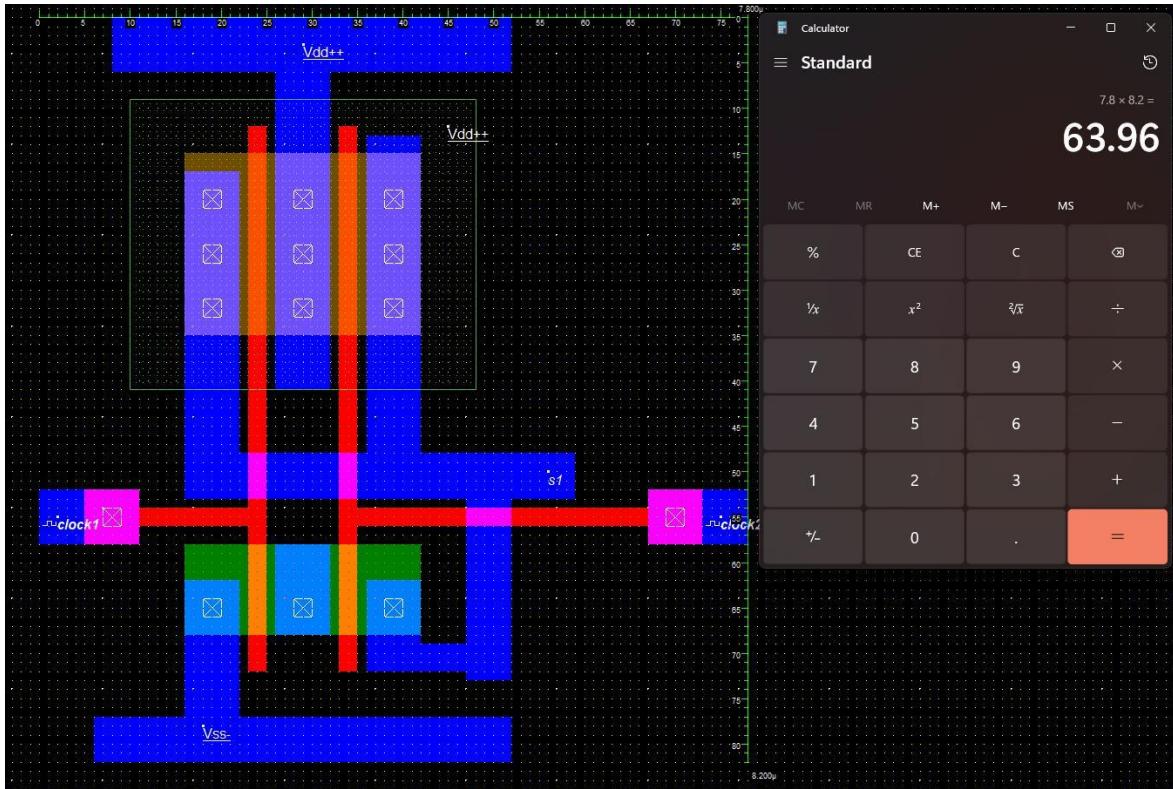
A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0



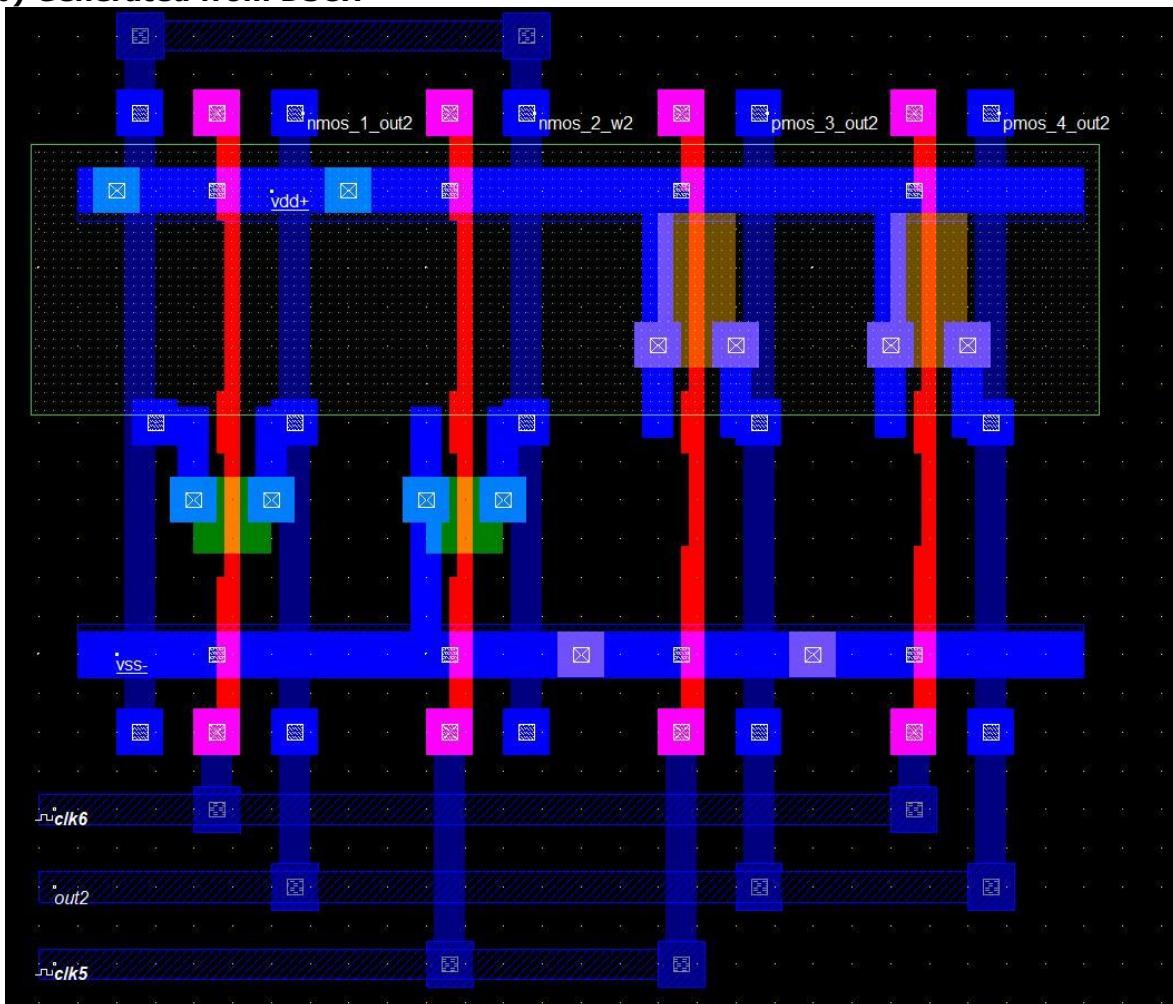
CMOS Invertor in DSCH



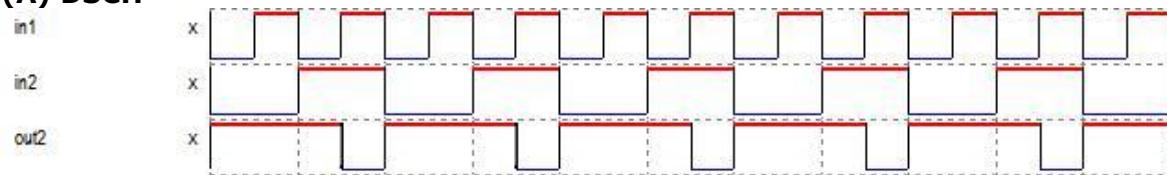
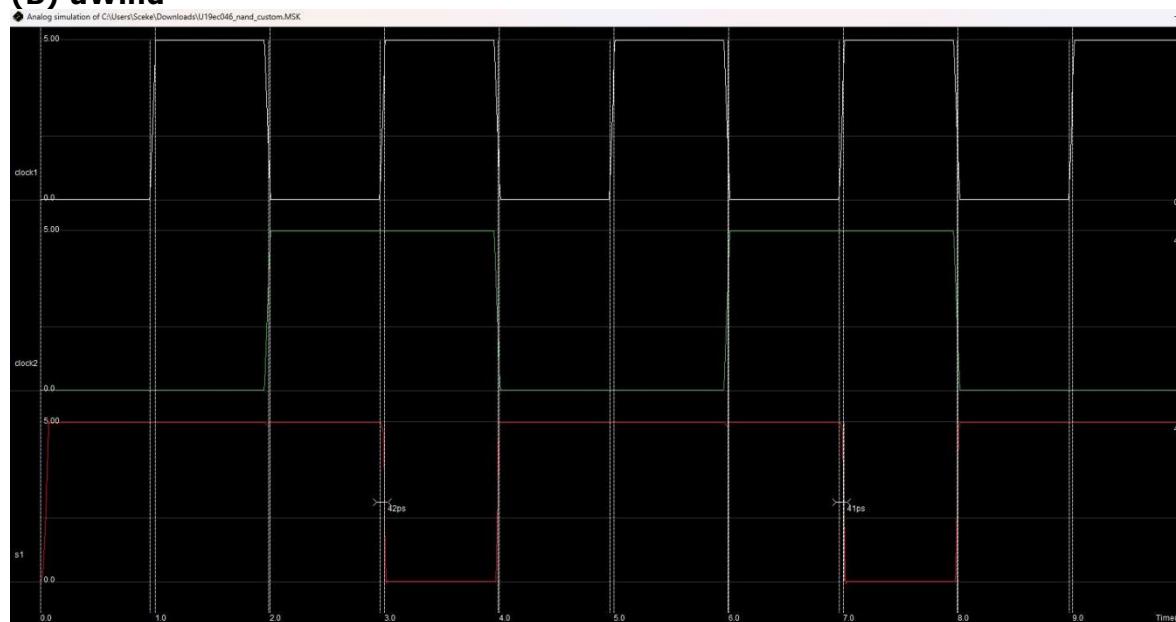
CMOS Inverter in Microwind
(a) Custom



(b) Generated from DSCH



Output

(A) DSCH**(B) uWind****CONCLUSION**

In this practical we have fabricated CMOS nand gate using microwind and verified its functionality. We also learnt about various fabrication rules.

AIM

To generate Layout for CMOS NOR circuit and Simulate it for verification.

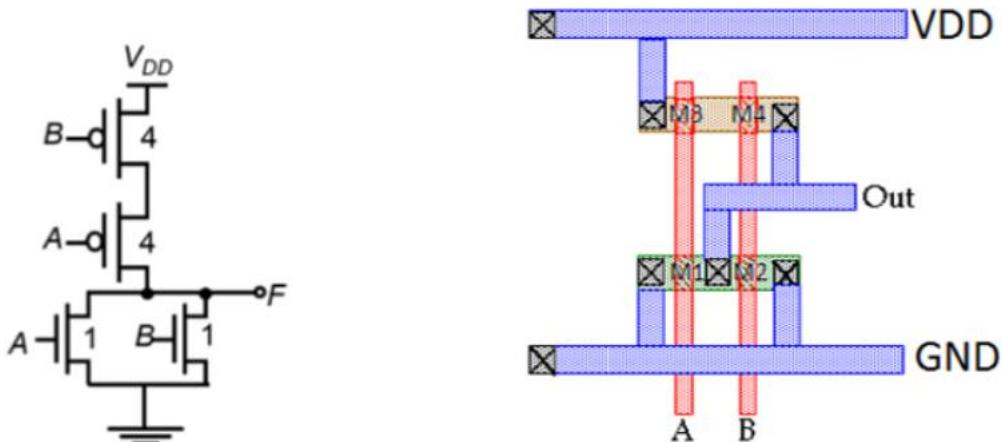
Software used: DSCH and Microwind Tool

THEORY:

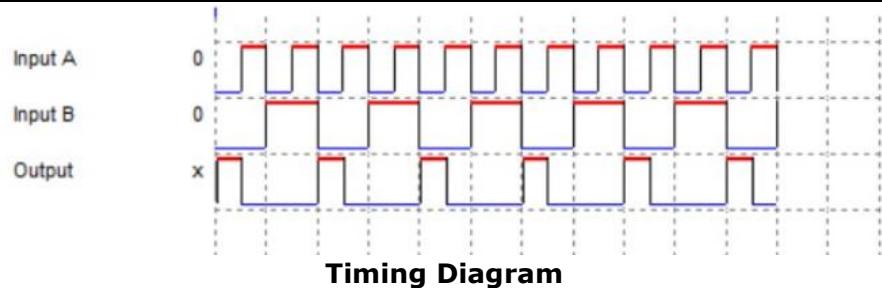
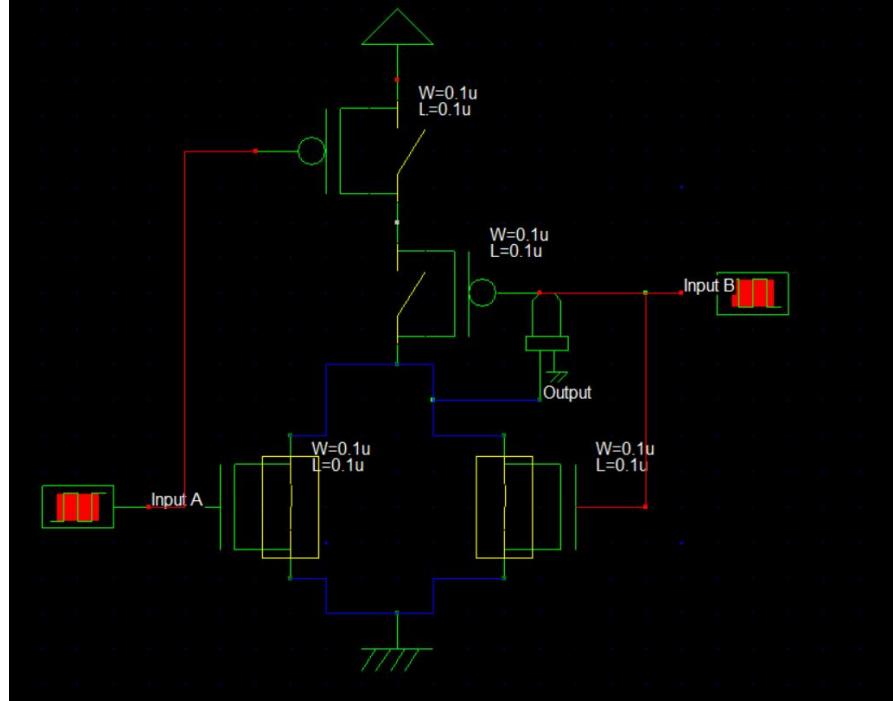
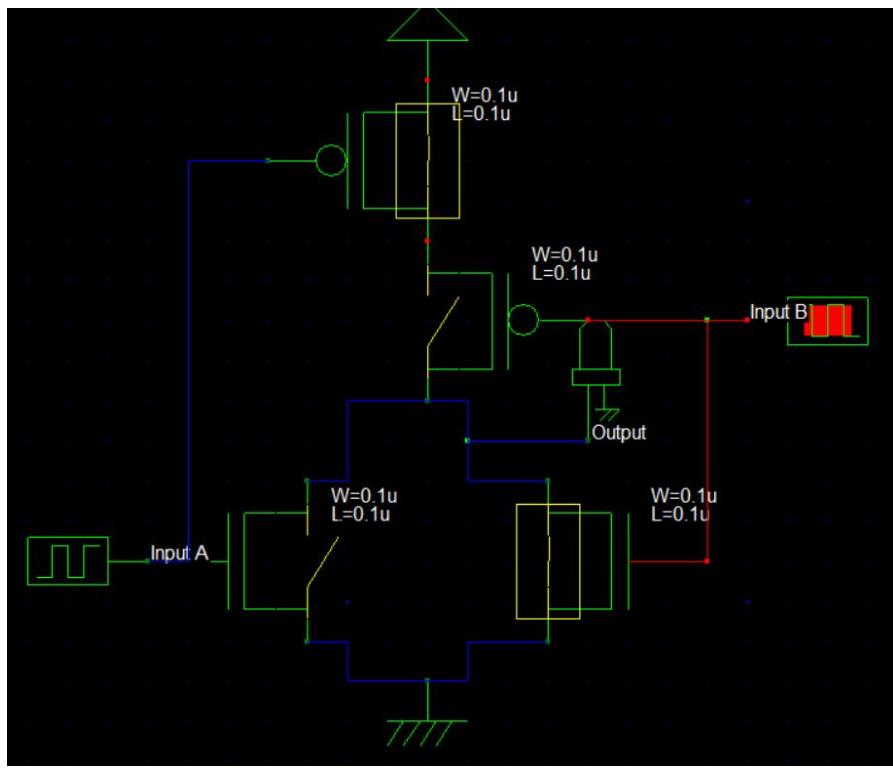
DSCH is software for logic design & based on primitives a hierarchical circuit can be built and simulated & it also includes delay and power consumption evaluation& 7ith the help of this software one can implement digital circuits at its basic gate primitives or at its transistor level. Microwind is a tool for designing and simulating circuits at layout level& The tool features full editing facilities "copy, cut, past, duplicate, move, various views "MOS characteristics6 (2D cross section6 3D process Viewer and an analog simulator. The circuit consists of a parallel-connected n-net and a series-connected complementary p-net. The input voltages VX and VY are applied to the gates of one nMOS and one pMOS transistor. When either one or both inputs are high, i.e., when the n-net creates a conducting path between the output node and the ground, the p-net is cut—off. If both input voltages are low, i.e., the n-net is cut-off, then the p-net creates a conducting path between the output node and the supply voltage.

Truth Table

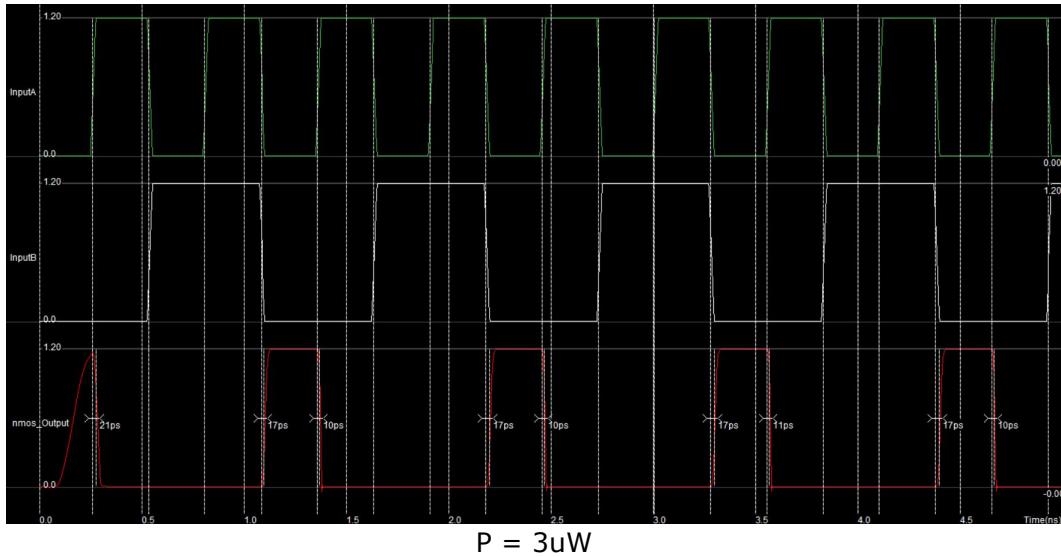
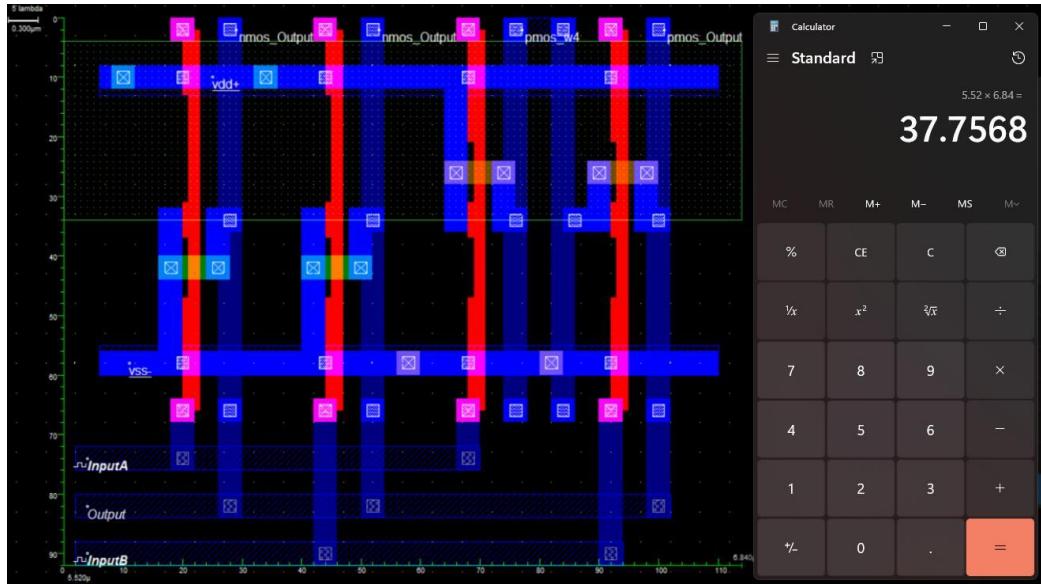
Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



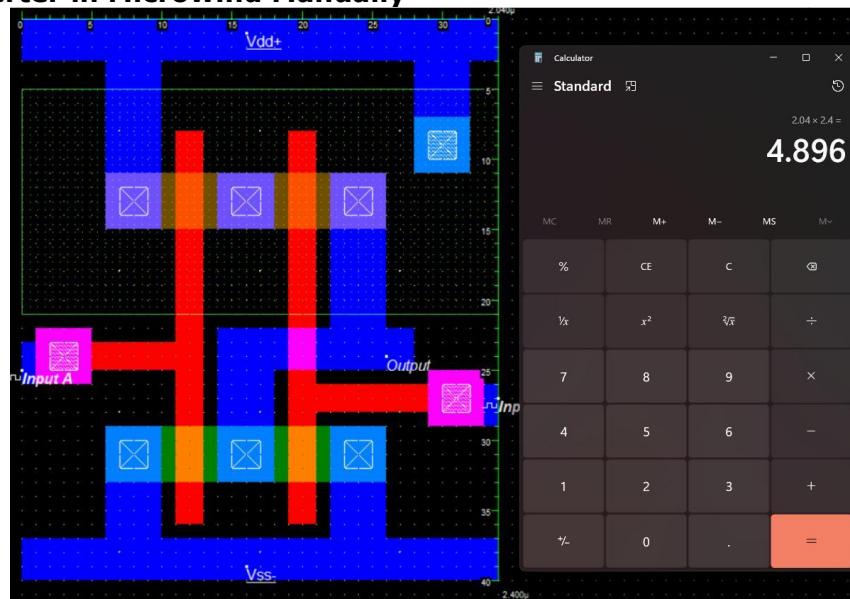
CMOS Invertor in DSCH:

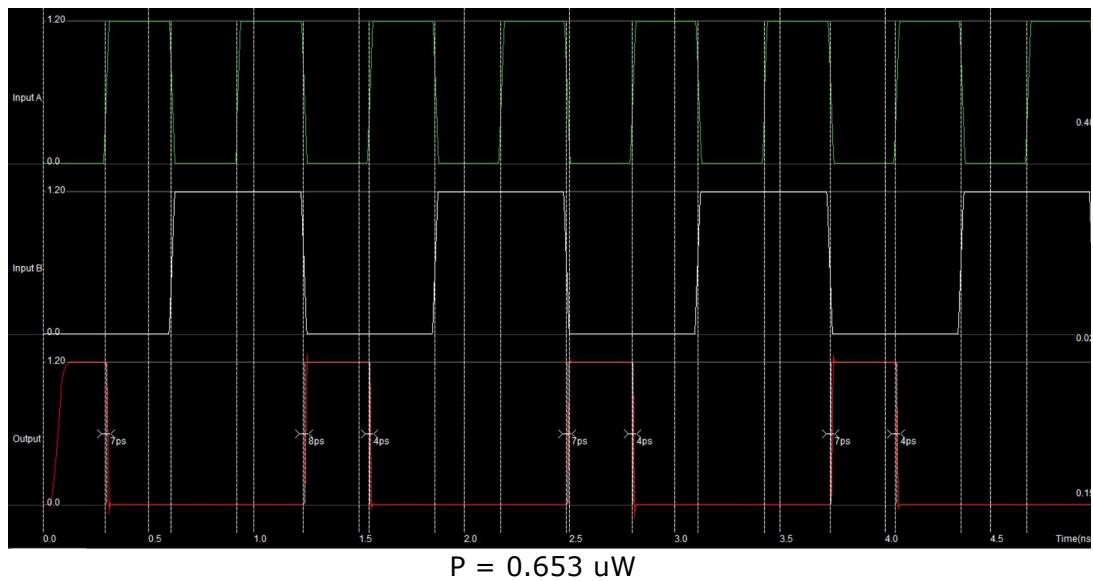


CMOS Inverter in Microwind Using VHDL code



CMOS Inverter in Microwind Manually





$$P = 0.653 \text{ } \mu\text{W}$$

CONCLUSION