**U19EC046 | DIC LAB 10**

**AIM**

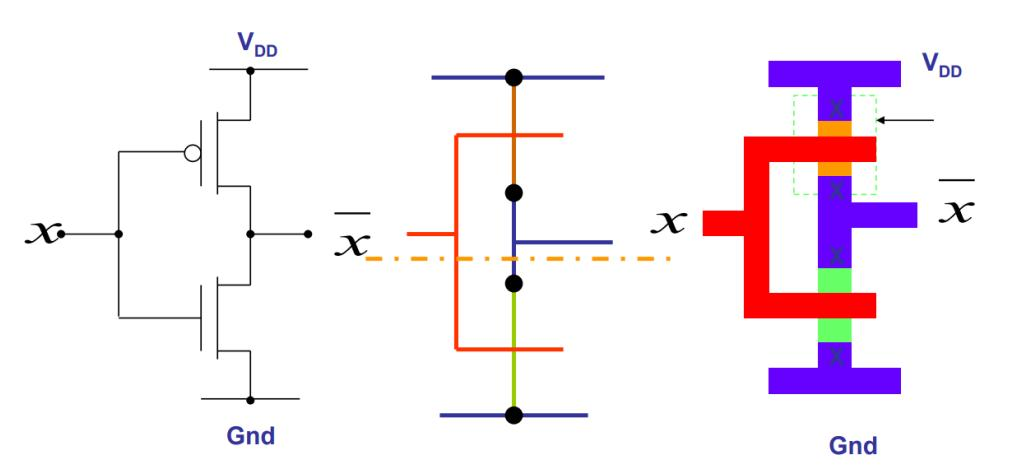
To generate Layout for CMOS inverter circuit and Simulate it for verification.

**Software used:** DSCH and Microwind Tool

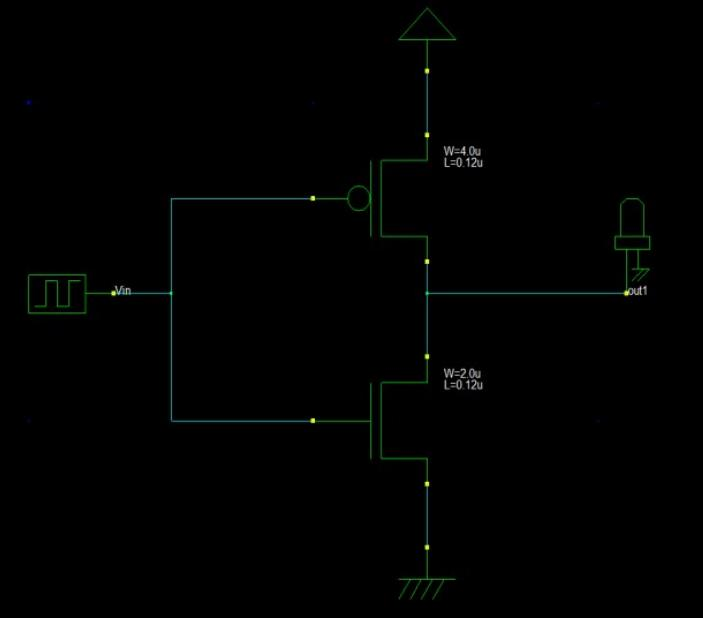
**THEORY**

The mask layout design of a CMOS inverter will be examined step-by-step. The circuit consists of one nMOS and one pMOS transistor, therefore, one would assume that the layout topology is relatively simple. Yet, we will see that there exist quite a number of different design possibilities even for this very simple circuit.

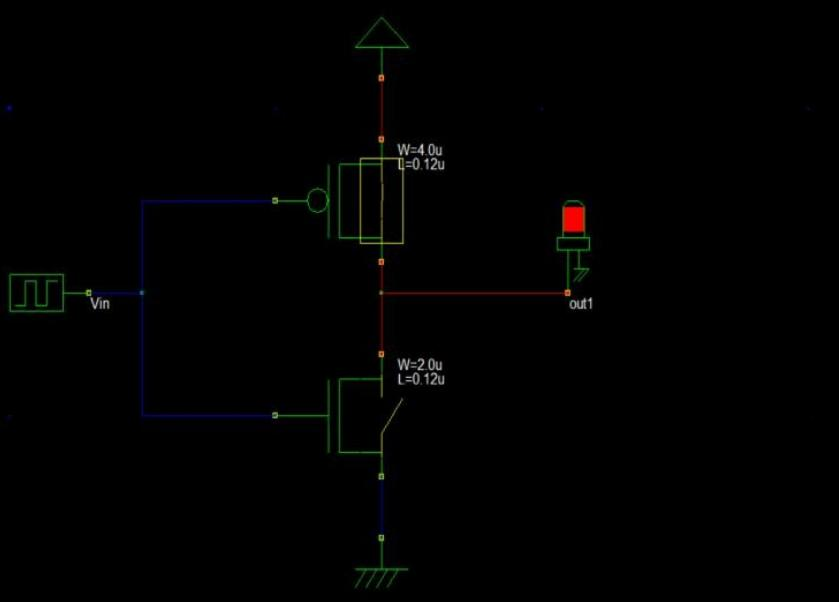
First, we need to create the individual transistors according to the design rules. Assume that we attempt to design the inverter with minimum-size transistors. The width of the active area is then determined by the minimum diffusion contact size (which is necessary for source and drain connections) and the minimum separation from diffusion contact to both active area edges. The width of the polysilicon line over the active area (which is the gate of the transistor) is typically taken as the minimum poly width. Then, the overall length of the active area is simply determined by the following sum: (minimum poly width) + 2 x (minimum poly-to- contact spacing) + 2 x (minimum spacing from contact to active area edge). The pMOS transistor must be placed in an n-well region, and the minimum size of the n- well is dictated by the pMOS active area and the minimum n-well overlap over n+. The distance between the nMOS and the pMOS transistor is determined by the minimum separation between the n+ active area and the n-well. The polysilicon gates of the nMOS and the pMOS transistors are usually aligned. The final step in the mask layout is the local interconnections in metal, for the output node and for the VDD and GND contactsNotice that in order to be biased properly, the n-well region must also have a VDD contact.

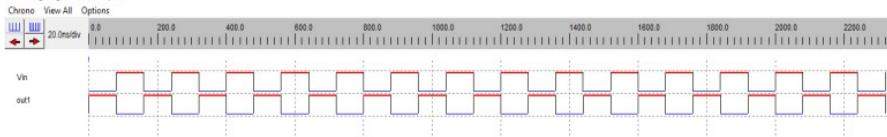


**CMOS Invertor in DSCH**

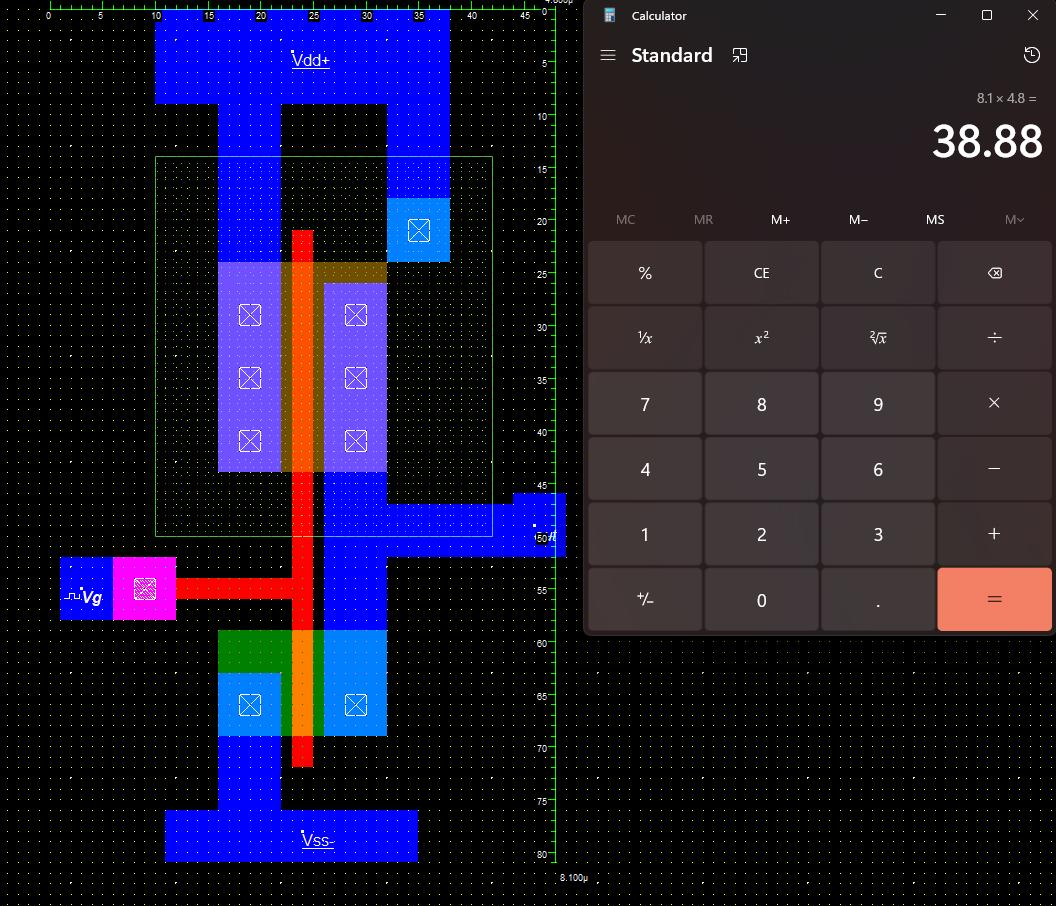


**Output**

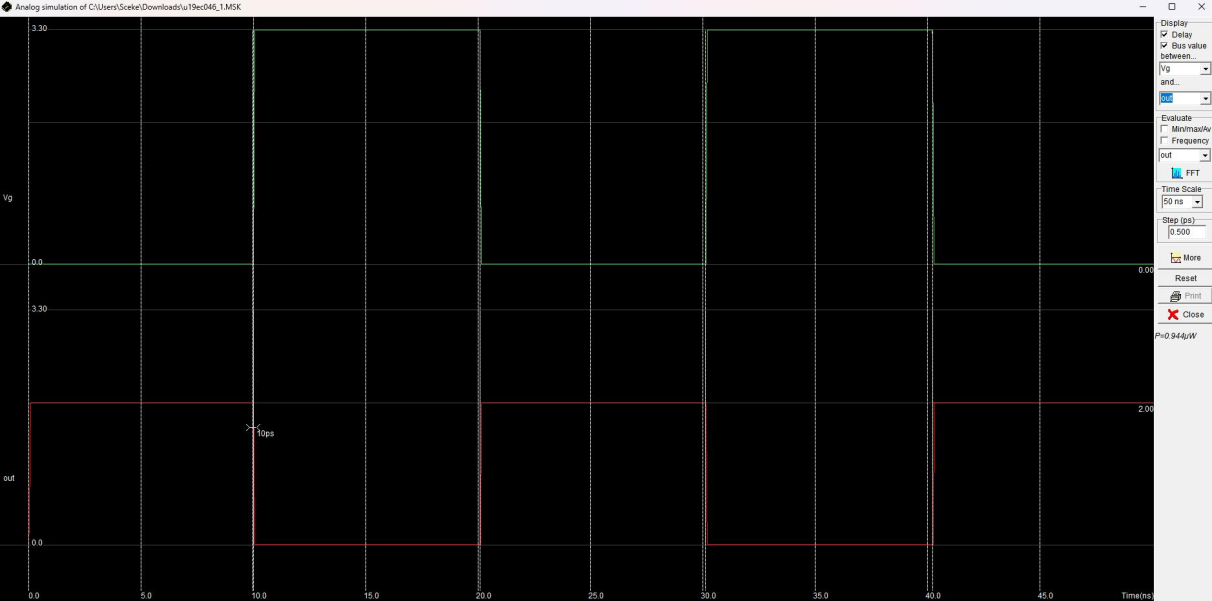




**CMOS Inverter in Microwind**



**Output**



**CONCLUSION**

In this practical we have fabricated CMOS using microwind. We also learnt about various fabrication rules.