**U19EC046 | DIC LAB 12**

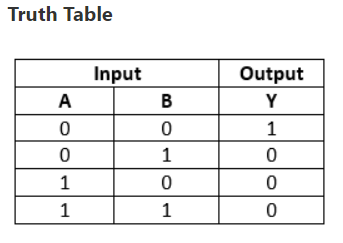
**AIM**

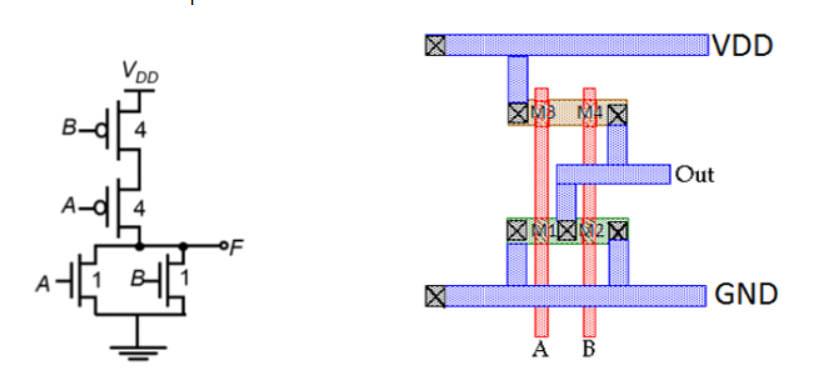
To generate Layout for CMOS NOR circuit and Simulate it for verification.

**Software used:** DSCH and Microwind Tool

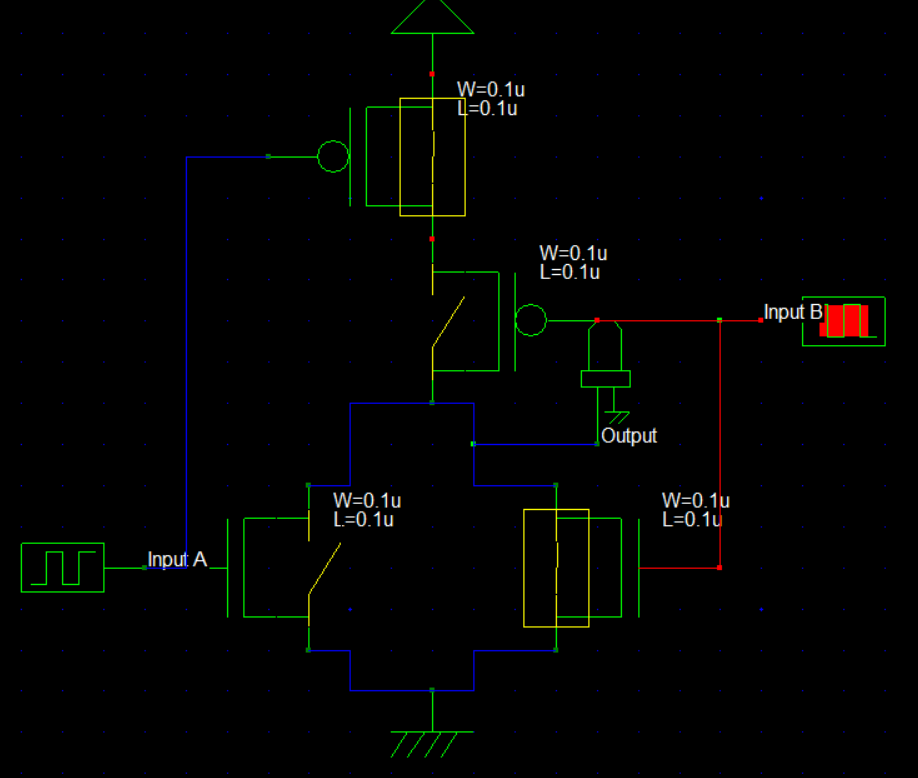
## THEORY:

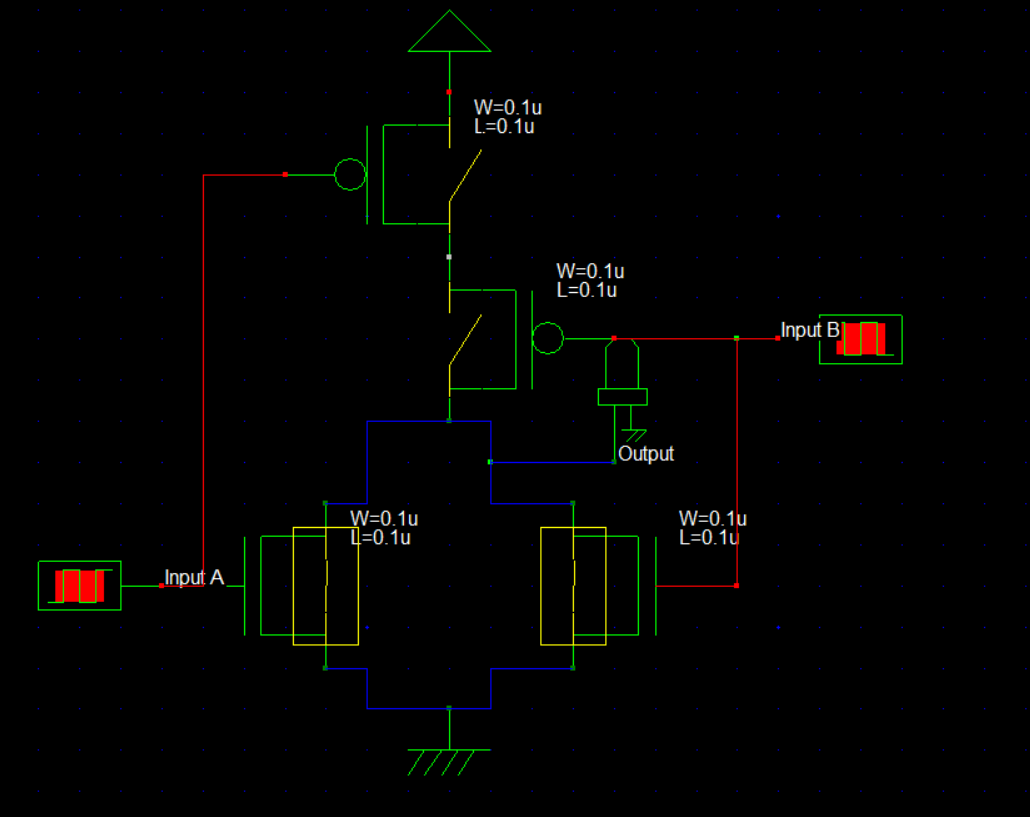
DSCH is software for logic design & based on primitives a hierarchical circuit can be built and simulated & it also includes delay and power consumption evaluation& 7ith the help of this software one can implement digital circuits at its basic gate primitives or at its transistor level. Microwind is a tool for designing and simulating circuits at layout level& The tool features full editing facilities "copy, cut, past, duplicate, move, various views "MOS characteristics6 (2D cross section6 3D process Viewer and an analog simulator. The circuit consists of a parallel-connected n-net and a series-connected complementary p-net. The input voltages VX and VY are applied to the gates of one nMOS and one pMOS transistor. When either one or both inputs are high, i.e., when the n-net creates a conducting path between the output node and the ground, the p-net is cut—off. If both input voltages are low, i.e., the n-net is cut-off, then the p-net creates a conducting path between the output node and the supply voltage.

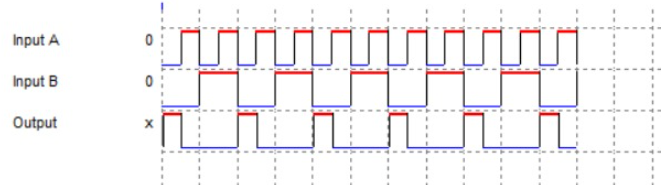




**CMOS Invertor in DSCH:**

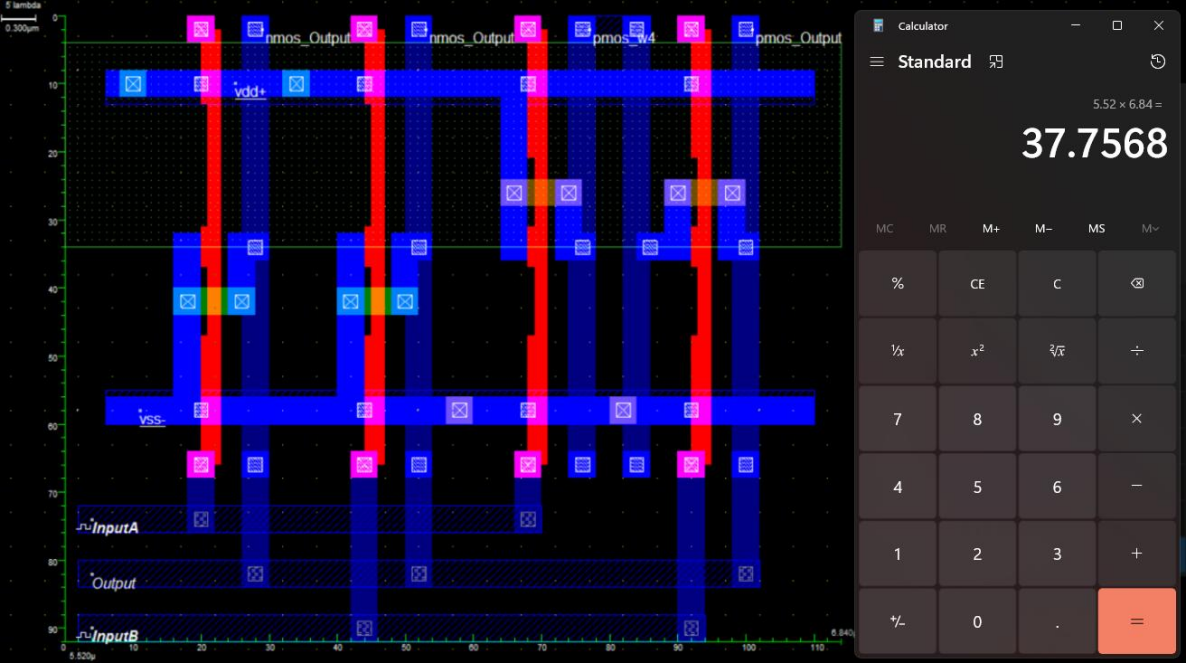
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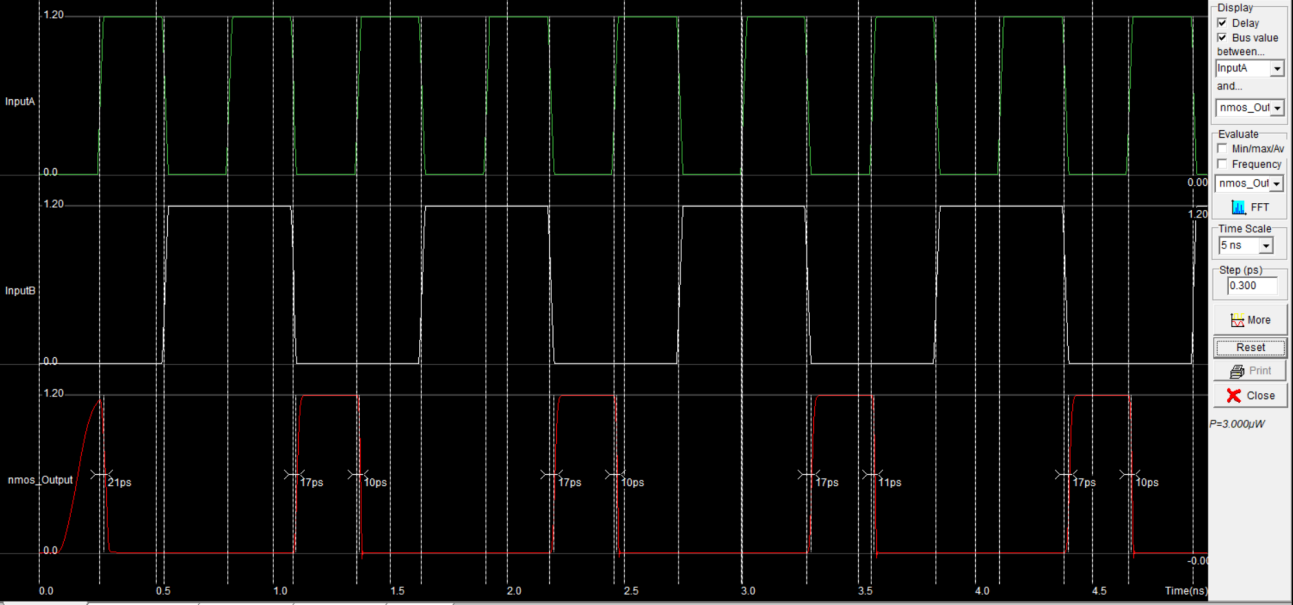
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**Timing Diagram**

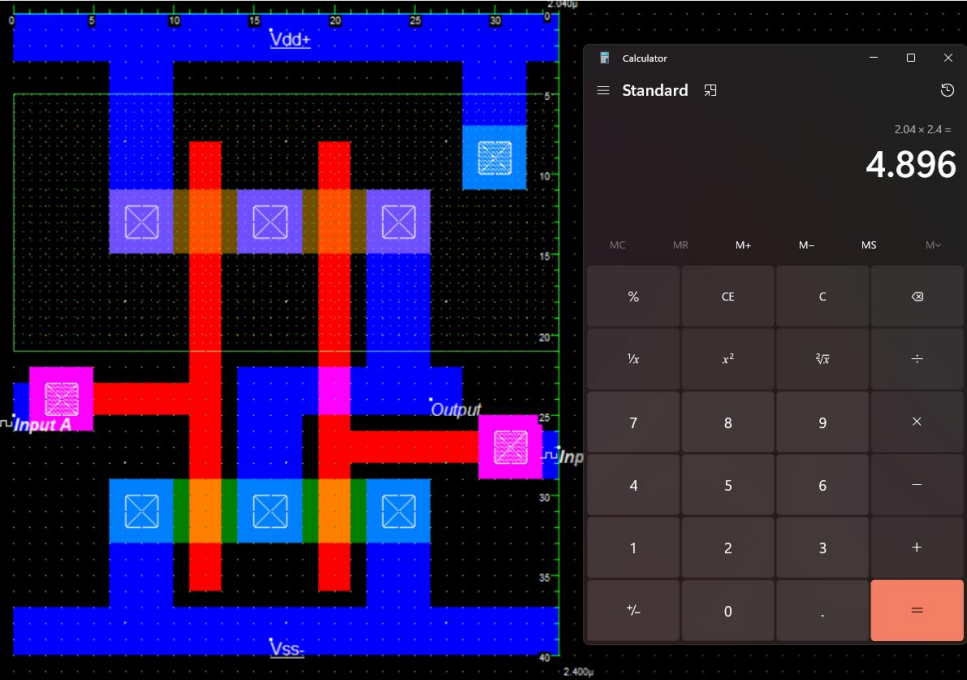
**CMOS Inverter in Microwind Using VHDL code**

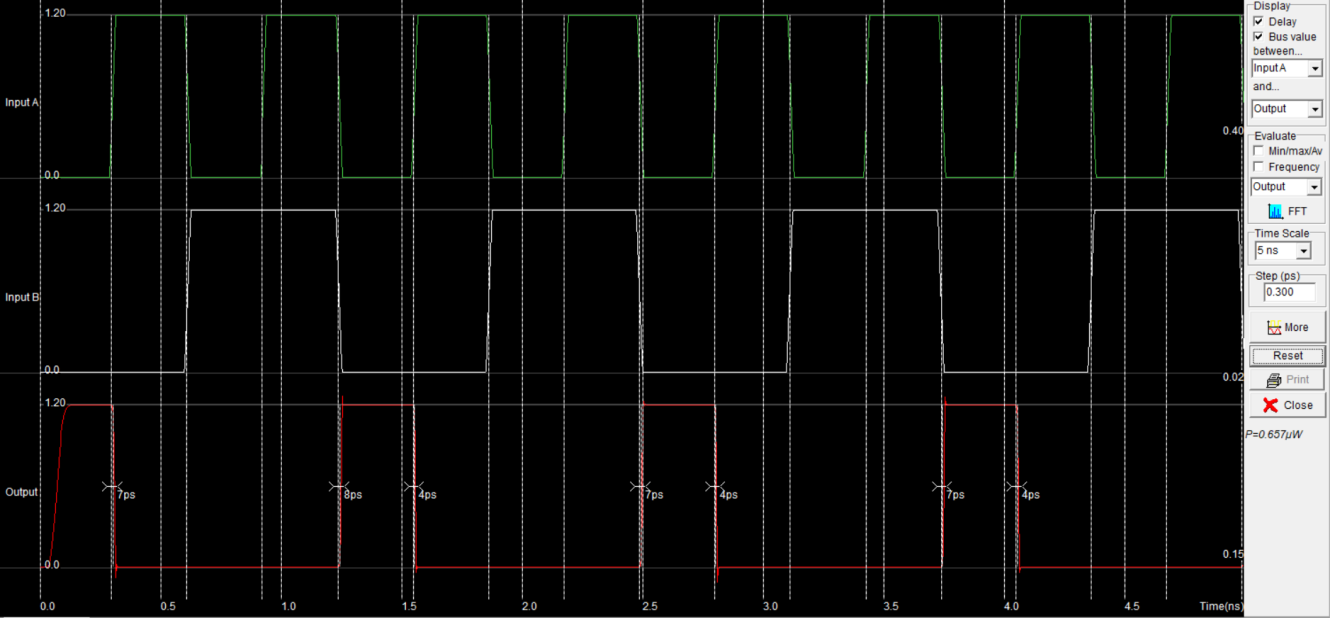


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P = 3uW

**CMOS Inverter in Microwind Manually**



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P = 0.653 uW

**CONCLUSION**

In this practical we have fabricated CMOS nand gate using microwind and verified its functionality. We also learnt about various fabrication rules.