**U19EC046 | DIC LAB 8**

**AIM**

Design and verify the performance of given CMOS inverter circuit to obtain switching threshold voltage of 2.2V. Given specifications for the CMOS inverter are:

VTN = 0.8V, VTP = -1V, VDD = 5V, Kn’ = 20µA/V2, Kp’ = 50µA/V2, Ln = Lp = 1µm.

Compare the theoretical and practical values of critical voltages on VTC and find the noise margin of the circuit. Observe the following parameters and comment on it.

* 1. Variation of VDD from 5V to 3.3V on the switching threshold voltage of CMOS inverter.

Variation of Kr at 0.25, 1 and 4 on the switching characteristics.

**THEORY**

The term CMOS stands for “Complementary Metal Oxide Semiconductor”. CMOS technology is one of the most popular technology in the computer chip design industry and broadly used today to form integrated circuits in numerous and varied applications. Today’s computer memories, CPUs and mobile phones make use of this technology due to several key advantages. This technology make use of both p-channel (PMOS) and n- channel (NMOS) semiconductor devices.

The main advantage of CMOS over NMOS and bipolar technology is the much smaller power dissipation. Unlike NMOS or BIPOLAR circuits, a complementary MOS circuit has almost no static power dissipation. Power is only dissipated in case the circuit actually switches. VTC Characteristics are more symmetrical in CMOS than NMOS and noise margin offered is much higher. This allows integrating more CMOS gates on an IC than in MOS or bipolar technology, resulting in much better performance.

**Circuit Diagram**

**Calculations**

**SPICE CODE**

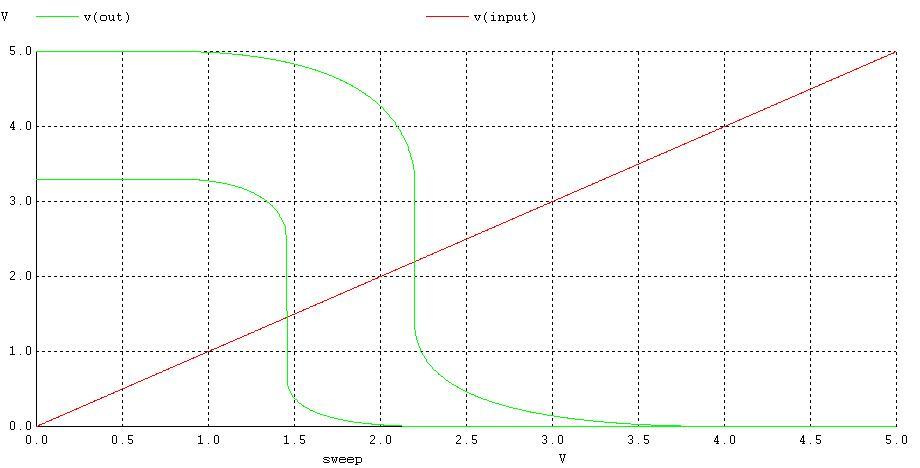
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| --- |
| **# CMOS**  **.model mynmos NMOS (Vt0=0.8, Kp=50u)**  **.model mypmos PMOS (Vt0=-1, Kp=20u)**  **.subckt cmosinverter in vdd\_node out gnd**  **MN out in gnd gnd mynmos w=1um l=1um**  **MP vdd\_node in out vdd\_node mypmos w=1.51um l=1um**  **.ends cmosinverter**  **Vdd vdd\_node 0 5**  **Vin input 0 5**  **Xd input vdd\_node out 0 cmosinverter**  **.dc Vin 0 5 0.005 Vdd 3.3 5 1.7**  **.control**  **run**  **plot v(input) v(out)**  **.endc**  **.end** |

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| **# CMOS**  **.model mynmos NMOS (Vt0=0.8, Kp=50u)**  **.model mypmos PMOS (Vt0=-1, Kp=20u)**  **.subckt cmosinverter in vdd\_node out gnd**  **MN out in gnd gnd mynmos w=1um l=1um**  **MP vdd\_node in out vdd\_node mypmos w=1.51um l=1um**  **.ends cmosinverter**  **Vdd vdd\_node 0 5**  **Vin input 0 pulse(0 5 1ns 1ns 1ns 20us 40us)**  **Xd input vdd\_node out 0 cmosinverter**  **.tran 1ns 80us**  **.control**  **run**  **plot v(input) v(out)**  **.endc**  **.end** |

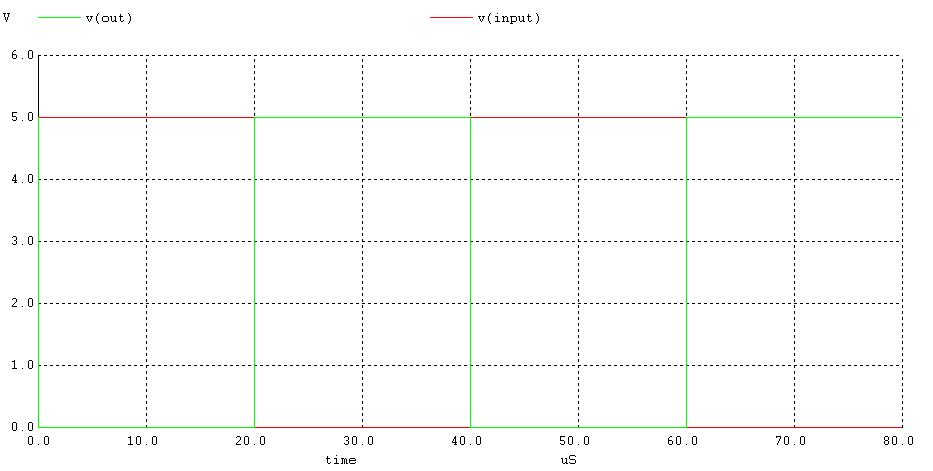
|  |
| --- |
| **# CMOS**  **.model mynmos NMOS (Vt0=0.8, Kp=50u)**  **.model mypmos PMOS (Vt0=-1, Kp=20u)**  **.subckt cmosinverter in vdd\_node out gnd**  **MN out in gnd gnd mynmos w=0.02um l=1um**  **MP vdd\_node in out vdd\_node mypmos w=0.05um l=1um**  **.ends cmosinverter**  **.subckt cmosinverter2 in vdd\_node out gnd**  **MN out in gnd gnd mynmos w=0.02um l=1um**  **MP vdd\_node in out vdd\_node mypmos w=0.2um l=1um**  **.ends cmosinverter2**  **.subckt cmosinverter3 in vdd\_node out gnd**  **MN out in gnd gnd mynmos w=0.08um l=1um**  **MP vdd\_node in out vdd\_node mypmos w=0.05um l=1um**  **.ends cmosinverter3**  **Vdd vdd\_node 0 5**  **Vin input 0 5**  **Xd input vdd\_node kr\_0\_25 0 cmosinverter**  **Xd2 input vdd\_node kr\_1 0 cmosinverter2**  **Xd3 input vdd\_node kr\_4 0 cmosinverter3**  **.dc Vin 0 5 0.005**  **.control**  **run**  **plot v(input) v(kr\_0\_25) v(kr\_1) v(kr\_4)**  **.endc**  **.end** |

**SIMULATION RESULTS AND PRACTICAL CALCULATIONS**

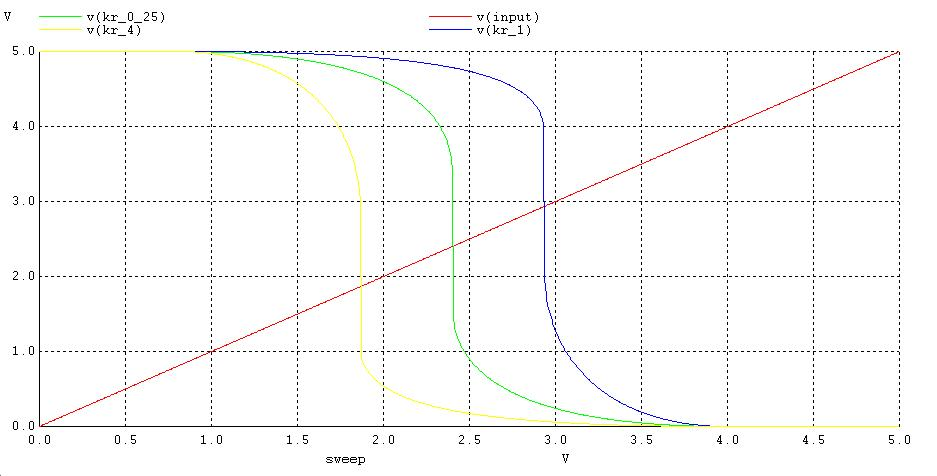
1.



2.



3.



**TABLE OF THEORETICAL AND PRACTICAL CALCULATION**

**Table 1: Noise Margin**

|  |  |  |
| --- | --- | --- |
| **Parameters** | **Theoretical** | **Practical** |
| VOH | 5 V | 5 V |
| VOL | 0 V | 0 V |
| VIH |  | 2.20 V |
| VIL | 1.728 V | 2.15 V |
| VTH | 2.2 V | 2.196 V |
| Noise Margin High |  | 2.8 V |
| Noise Margin Low | 1.728 V | 2.15 V |
| Noise Margin |  | 2.15 V |

#### Table 2: Effect of VDD variation on VTH

|  |  |
| --- | --- |
| **VDD (V)** | **VTH (V)** |
| 5 | 2.813 |
| 4 | 1.776 |
| 3 | 1.326 |

**Table 3: Effect of kr variation on VTH**

|  |  |
| --- | --- |
| **kr** | **VTH (V)** |
| 0.25 | 2.9257 |
| 1 | 2.412 |
| 4 | 1.872 |

**CONCLUSION**