**U19EC046 | DIC LAB 9.1**

**AIM**

Write a winspice code to verify the functionality of given bicmos inverter circuit using default model parameters for the transistor.

**THEORY**

**Introduction**

The history of semiconductor devices starting 1930’s when Lienfed and Heil first proposethe mosfet.Bipolar Technology was started in 1980’s. CMOS Technology was also started in mi1980’s. Later in 1990 there was a cross over between bipolar and CMOS Technology.

In BiCMOS technology, both the MOS and bipolar device are fabricated on the same chip.

The objective of the BiCMOS is to combing bipolar and CMOS so as to exploit the advantages of both the technologies.

Today BiCMOS has become one of the dominant technologies used for high speed, low power and highly functional VLSI circuits.

The process step required for both CMOS and bipolar are similar so the BiCMOS process has been enhanced and integrated into the CMOS process without any additional steps.

The primary approach to realize high performance BiCMOS devices is the addition of bipolar process steps to a baseline CMOS process.

The BiCMOS gates could be used as an effective way of speeding up the VLSI circuits.

The applications of BiCMOS are vast.

Advantages of bipolar and CMOS circuits can be retained in BiCMOS chips.

* BiCMOS technology enables high performance integrated circuits IC’s but increases process complexity..
* CMOS technology offers less power dissipation, smaller noise margins, and high packing density.
* Bipolar technology, on the other hand, ensure high switching and I/O speed and good noise performance. Now we are in 3rd Generation BiCMOS Technology.
* BiCMOS technology accomplishes both improved speed over CMOS and lower power dissipation than bipolar technology.
* The main drawback of BiCMOS technology is the higher costs due to the added process complexity.
* This greater process complexity in BiCMOS results in a cost increase compared to conventional CMOS technology.

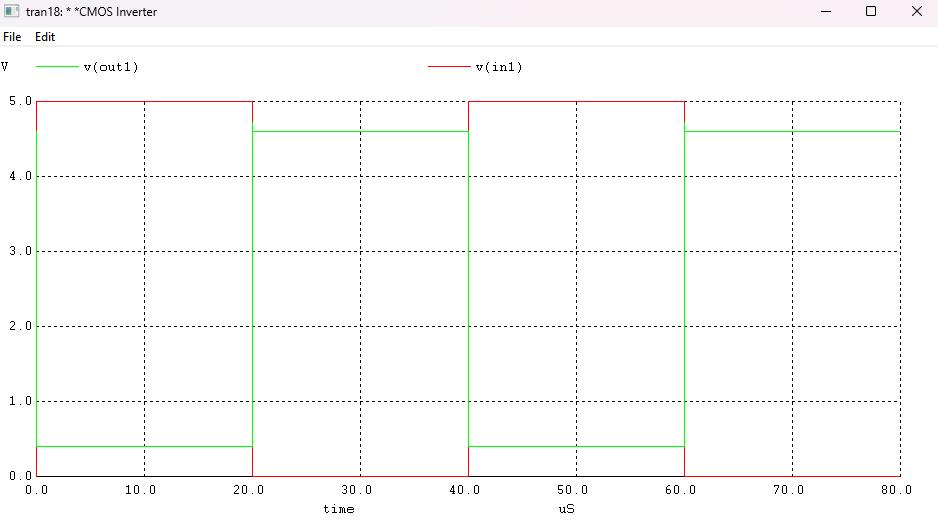
**Circuit Diagram**

**SPICE CODE**

|  |
| --- |
| **.model q1 npn bf=50**  **.model mynmos nmos Vto=0.8 Kp=50**  **.model mypmos pmos Vto=-1 Kp=20**  **.subckt BI in vdd\_node out1 out2 src**  **M1 out1 in src src mynmos w=1u l=1u**  **M2 out2 in vdd\_node vdd\_node mypmos w=1.51u l=1u**  **.ends BI**  **q11 vdd\_node out2 out1 q1**  **q12 out1 src 0 q1**  **xd1 in1 vdd\_node out1 out2 src BI**  **Vdd vdd\_node 0 5**  **Vin in1 0 pulse(0 5 1ns 1ns 1ns 20us 40us)**  **.tran 1ns 80us**  **.control**  **run**  **plot v(in1) v(out1)**  **.endc**  **.end** |

**SIMULATION RESULTS AND PRACTICAL CALCULATIONS**

1.



**CONCLUSION**