**Sardar Vallabhbhai National Institute of Technology Surat**

**Electronics Engineering Department**



**LABORATORY JOURNAL**

**Digital Integrated Circuits**

**(EC-304)**

**Name: Harsh Suthar**

**Roll No. U19EC046**

Sem – VI , Academic Year – 21/22

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CERTIFICATE

This is to Certify that Mr. Harsh Suthar of B.Tech IIIrd E.C, Admission No. U19EC046 has Satisfactorily Completed His course work in Digital Integrated Circuits (EC-**304**) Laboratory during the 6th Semester Session of Academic Year 2021-2022 and the same is submitted on 2022.

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| **Dr. Vivek Garg** |
| **Course Coordinator** |

**Electronics Engineering Department**

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**Sardar Vallabhbhai National Institute of Technology, Surat**

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| **SR. NO** | **DATE** | **AIM** | **SIGN** |
| **1** | 17.01.2022 | To plot the forward and reverse characteristics of PN Junction Diode for the given Parameters. Also extract  the parameters: |  |
| **2** | 24.01.2022 | Implement RTL inverter using NPN BJT having Bf=20, Rb=10k, Rc=1K. |  |
| **3** | 31.01.2022 | Implement DTL NAND Gate using parameters Bf=50, R1=10k, Rc=1K, R2=20k |  |
| **4** | 07.02.2022 | Implement Modified diode transistor logic (MDTL) using NPN BJT. Bf = 50, R1 = 1.75k, R2 = 2k, R3 = 5k and Rc = 2k |  |
| **5** | 14.02.2022 | Implement TTL inverter using NPN BJT having Bf = 50,  Rb = 4kΩ and Rc = 1.6kΩ. |  |
| **6** | 28.02.2022 | To design and verify the performance of given Resistively Loaded NMOS inverter circuit to obtain VOL = 0.147V for the given specifications |  |
| **7** | 14.03.2022 | Design and verify the performance of given saturated loaded NMOS inverter circuit to obtain Vih-2.9, for the given design parameter VDD=5V, Kn’=20ua/v2, Vtl=0.8V,(W/L)driver=2um/1um. |  |
| **8** | 28.03.2022 | Design and verify the performance of given CMOS inverter circuit to obtain switching threshold voltage of 2.2V. Given specifications for the CMOS inverter are: |  |
| **9** | 28.03.2022 | 1. Write a winspice code to verify the functionality of given bicmos inverter circuit using default model parameters for the transistor. 2. Write a winspice code to verify the functionality of NOR based SR Latch |  |
| **10** | 04.04.2022 | To generate Layout for CMOS inverter circuit and Simulate it for verification. |  |
| **11.** | 11.04.2022 | Design the schematic and verify the functionality of NAND circuit for CMOS Technology using Microwind Tool. Also Generate the automatic Layout |  |
| **12.** | 11.04.2022 | Design the schematic and verify the functionality of NOR circuit for CMOS Technology using Microwind Tool. Also Generate the automatic Layout |  |