**U19EC046 | DIC LAB 2**

**AIM**

Implement RTL inverter using NPN BJT having Bf = 20, Rb = 10k and Rc = 1k.

1. Verify its functionality by performing transient analysis.
2. Plot the VTC & Calculate the Noise margin.
3. Find out theoretical and practical fan-out & compare them.

**Assignment 1:** Repeat above for TTL

**THEORY**

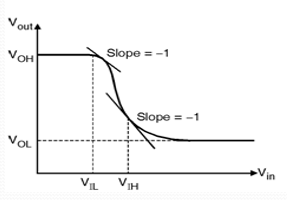
**Introduction**

RTL Inverter is a circuit used to invert the input signal. It consists of one BJT transistor, Base connected with resistor (Rb), Collector connected with resistor (Rc) and Emitter is grounded. Input Signal is given to Base of transistor through Rb, Vcc is connected to Rc and Output is taken at collector terminal.

### VOLTAGE TRANSFER CHARACTERISTICS (VTC):

To study the noise margins and the fan-out capability of the RTL inverter, we should know the static behaviour of the circuit output Vout when input Vin is increased from 0 to Vcc. When Vin is below the base-emitter cut-in voltage(𝑉𝐼𝐿), collector current is zero and transistor is in the cutoff mode, Vout is almost equal to Vcc (𝑉𝑂𝐻) (assuming no load is connected at output) and VTC will be constant output for 0<Vin<𝑉𝐼𝐿.

As Vin is increased beyond 𝑉𝐼𝐿 , the transistor enters active mode. The collector current (Ic = βIb) causes a voltage drop in the collector resistor and the collector voltage Vc = Vout = Vcc - IcRc falls. This fall continues until output saturation voltage (Vce=𝑉𝑂𝐿) BJT mode changes to saturation and corresponding input voltage is 𝑉𝐼𝐻.



### NOISE MARGINS:

Noise margin is the ratio by which the signal exceeds the minimum acceptable amount. It is normally measured in decibels. In a digital circuit, the noise margin is the amount by which the signal exceeds the threshold for a proper '0' or '1'.

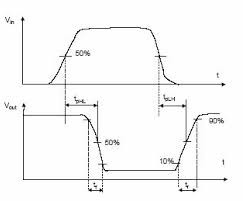
𝑁𝑀𝐿 = 𝑉𝐼𝐿 − 𝑉𝑂𝐿

𝑁𝑀𝐻 = 𝑉𝑂𝐻 − 𝑉𝐼𝐻

In practice, noise margins are the amount of noise, that a logic circuit can withstand. Noise margins are generally defined so that positive values ensure proper operation, and negative margins result in compromised operation, or outright failure.

### TRANSIENT RESPONSE:

Transient analysis means analyzing a system in unsteady state. If the variables involved in defining the state of a system does not vary with respect to time, then the system is said to be in steady state.

In Transient Analysis, also called time-domain transient analysis, computes the circuit's response a function of time. This analysis divides the time into segments and calculates the voltage and current levels for each interval.

### PROPAGATION DELAY:

Propagation delay is a measure of how long it takes for a gate to change state. Ideally, should be as short as possible.

– the time it takes the output to go from a high to low

– the time it takes the output to go from a low to high

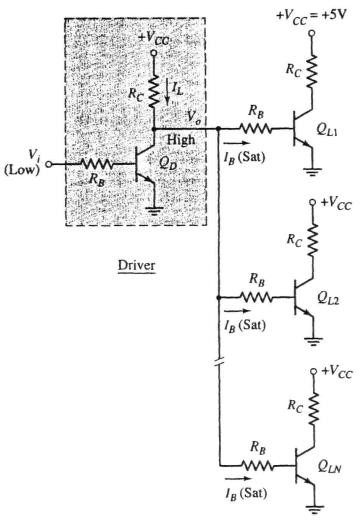
Average Propagation Delay Time

* Rise Time ( = Time from 10% to 90%
* Fall Time ( = Time from 90% to 10%

### Image result for Rise time Fall Time

### FAN-OUT:

Fan-out of the inverter is the number of identical circuits that the inverter can drive before Vo enters the transition region. When output of RTL inverter (the driver) is at logic low, it can drive practically any number of identical inverters (loads). Since, each load transistor is operating in the cutoff mode, no current is drawn via the collector resistor of the driver, and the output voltage remains at logic low.



For logic high output of the driver as shown in above figure there are N identical inverters connected to output of driver circuit. Since, the saturation base current of each load inverter is supplied by the driver, output voltage Vo drops from its open circuit voltage of Vcc. The gate fan-out therefore it is limited by the number of load inverters that can be driven into saturation while maintain satisfactory logic high Vo ≥ 𝑉𝐼𝐻. The number depends on the current gain β of the driver transistor.

From above figure, the sum of the base currents of the load gates, which is the current through the collector resistor of the driver, is given by

= N\*Ib(sat) = N\*k\*Ib(EOS)

Where overdrive factor k is defined by

k=Ib(sat)/Ib(EOS)

Ib(EOS) = Ic(EOS)/β = (Vcc - )/β

Vo = Vcc – (N\*k\*Ib(EOS)\*)

= Vcc – (N\*k\*(Vcc - )/β)

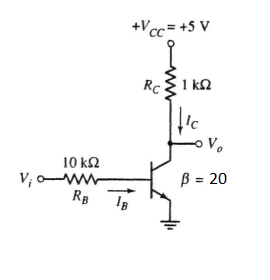
For regeneration of logic levels at the load gates, this voltage Vo must satisfy the input logic high level. Hence

Vcc – (N\*k\*(Vcc - )/β) ≥

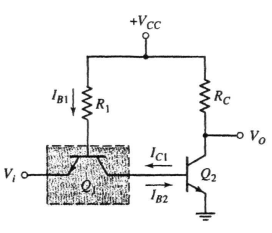
N ≤

**Circuit Diagram**

RTL inverter using NPN BJT



TTL inverter using NPN BJT



**Working principle**

Bipolar transistor switch is the simplest RTL gate. The resistor R1 in the circuit is used across the base and input terminals. This resistor increases the voltage drop from 0.7 V to 1 V by converting the input voltage into current. The resistance Rb is chosen in such a way that it saturates the transistor and obtains high input resistance. The collector resistor Rc converts collector current into voltage. The resistance of R2 is high to saturate the transistor and low to obtain output resistance.

**Application**

The RTL circuit consists of resistors at inputs and transistors at the output side. Transistors are used as the switching device.

**SPICE CODE**

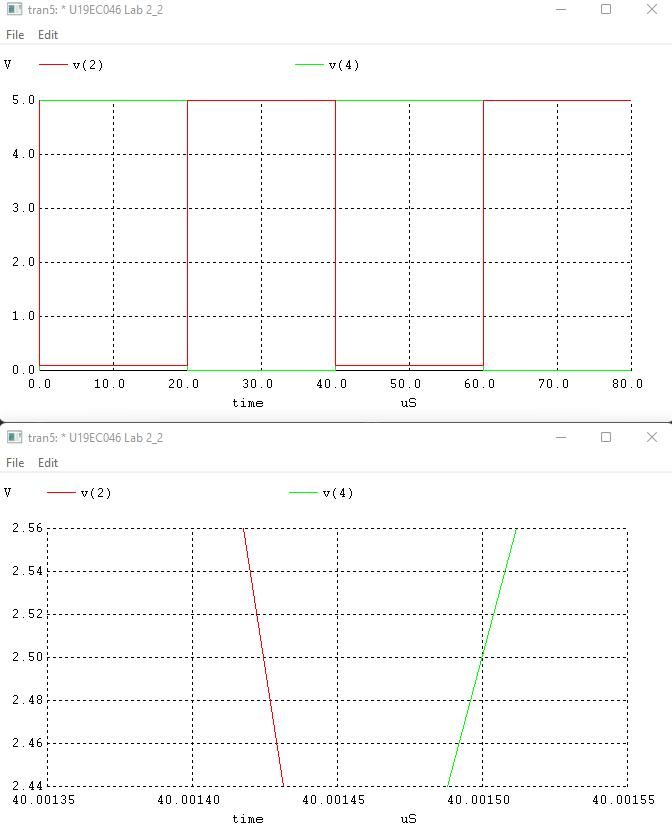
|  |
| --- |
| ***\* U19EC046 Lab 2\_2***  **.model mybjt npn (bf=20)**  **Q1 2 1 0 mybjt**  **Rc 2 3 1k**  **Rb 4 1 10k**  **Vcc 3 0 5**  **Vin 4 0 pulse(0 5 1ns 1ns 1ns 20us 40us)**  **C 3 0 1p**  **.tran 1ns 80us**  **.control**  **run**  **plot V(2) V(4)**  **.endc**  **.end** |

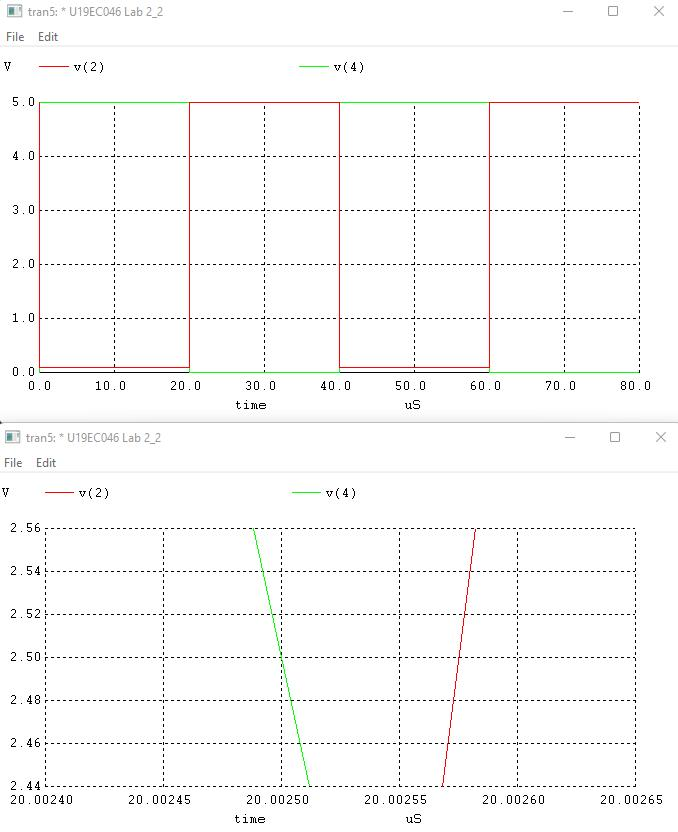
|  |
| --- |
| ***\* U19EC046 Lab 2***  **.model mybjt npn (bf=20)**  **Q1 2 1 0 mybjt**  **Rc 2 3 1k**  **Rb 4 1 10k**  **Vcc 3 0 5**  **Vin 4 0 0**  **.dc Vin 0 5 0.05**  **.control**  **run**  **plot V(2) V(4)**  **.endc**  **.end** |

|  |
| --- |
| ***\* RTL Inverter fanout***  **.model switch NPN (Bf=20)**  **.subckt Rtl out in vc gnd**  **Q2 out y gnd switch**  **Rb1 in y 10k**  **Rc1 vc out 1k**  **.ends Rtl**  **Vcc vcc\_src 0 5**  **Vin vin\_src 0 5**  **X\_main out\_main vin\_src vcc\_src 0 Rtl**  **X1 outl out\_main vcc\_src 0 Rtl**  **X2 out2 out\_main vcc\_src 0 Rtl**  **X3 out3 out\_main vcc\_src 0 Rtl**  **X4 out4 out\_main vcc\_src 0 Rtl**  **X5 out5 out\_main vcc\_src 0 Rtl**  **X6 out6 out\_main vcc\_src 0 Rtl**  **X7 out7 out\_main vcc\_src 0 Rtl**  **.dc Vin 0 5 0.05**  **.control**  **run**  **plot V(out\_main) V(vin\_src)**  ***\* plot V(out1)***  **.endc**  **.end** |

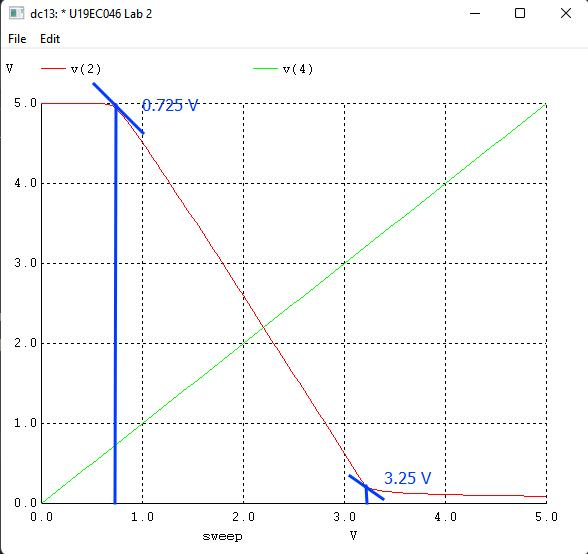
**SIMULATION RESULTS AND PRACTICAL CALCULATIONS**

1. Propagation Dealy





1. VTC and Noise margin



**TABLE OF THEORETICAL AND PRACTICAL CALCULATION**

RTL inverter transient analysis

Propagation delay = (0.83+0.41)/2 = 0.62nS

Tr = 2.25nS

Tf = 0.98nS

RTL inverter static analysis

NML = VIL – VOL = 0.725 – 0.2 = 0.525V

NMH = VOH – VIH = 5 – 3.25 = 1.75V

NM = min(NML , NMH) = 0.525V

VTH = 2.2V

RTL fanout calculation

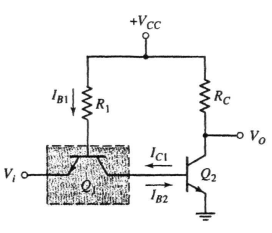
Observation table:

|  |  |  |
| --- | --- | --- |
|  | Theoretical | Practical |
| Fan-out | 7 | 7 |

ASSIGNMENT

**TTL inverter and its fanout:**

Circuit diagram:

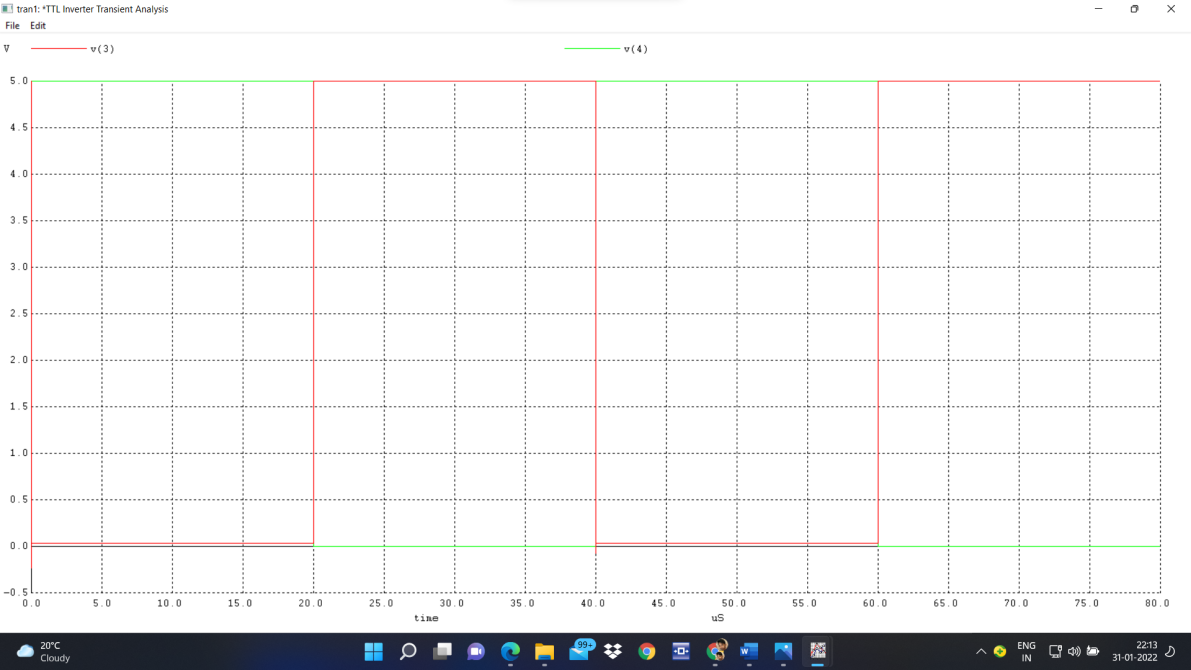


**TTL inverter Transient analysis:**

**Spice Code**

|  |
| --- |
| ***TTL Inverter Transient Analysis U19EC046***  **.model switch NPN (Bf=20)**  **Q1 2 1 4 switch**  **Q2 3 2 0 switch**  **R2 5 3 1.6k**  **R1 5 1 4k**  **Vcc 5 0 5**  **Vin 4 0 pulse(0 5 1ns 1ns 1ns 20us 40us)**  **c 3 0 1p**  **.tran 1ns 80us**  **.control**  **run**  **plot v(3) v(4)**  **.endc**  **.end** |

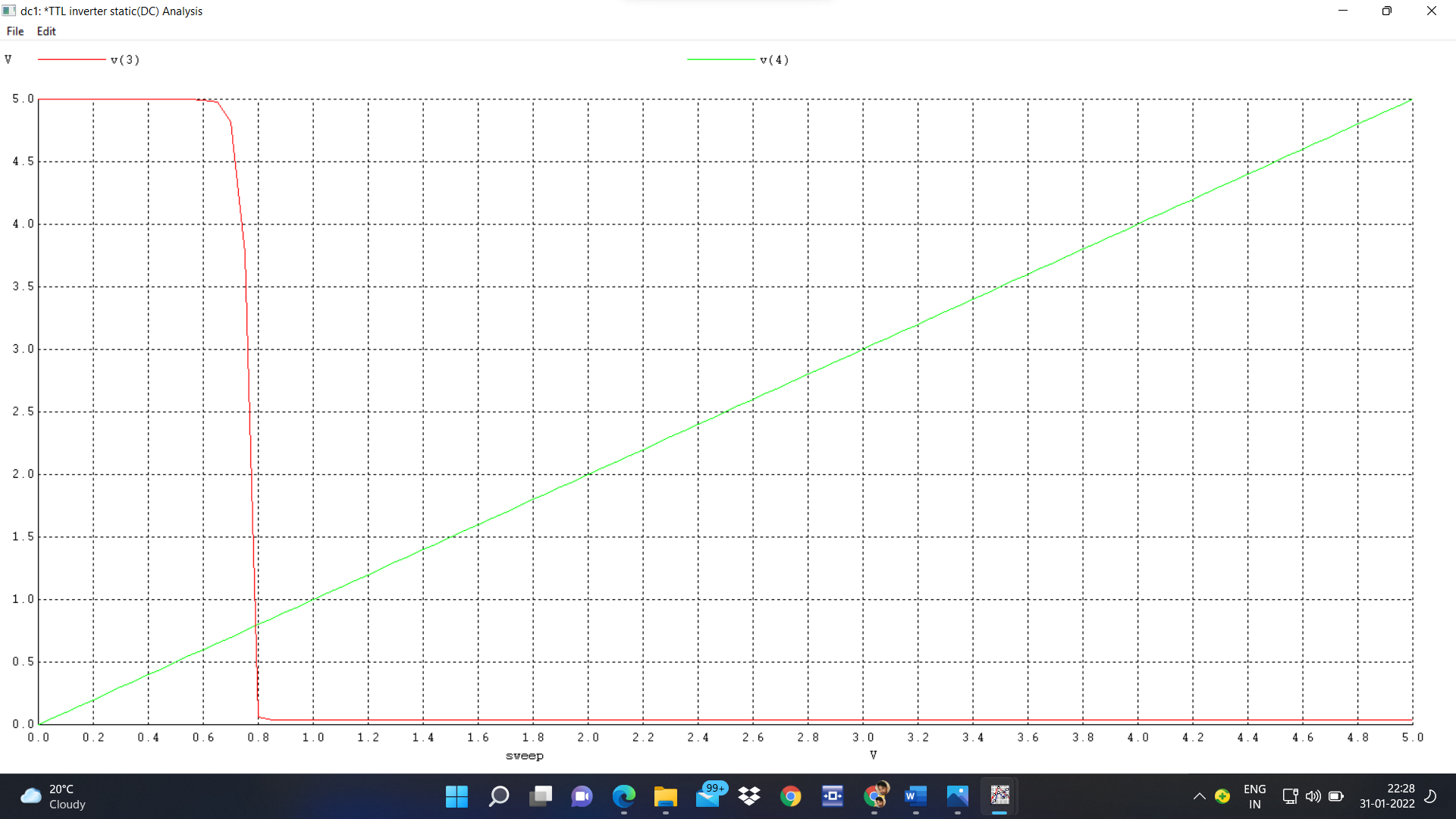
# Simulation plots



# TTL inverter static (DC) analysis: Spice Code

|  |
| --- |
| ***\*TTL Inverter static(DC) Analysis U19EC046***  **.model switch NPN (Bf=20)**  **Q1 2 1 4 switch**  **Q2 3 2 0 switch**  **R2 5 3 1.6k**  **R1 5 1 4k**  **Vcc 5 0 5**  **Vin 4 0 dc 5**  **.dc Vin 0 5 0.05**  **.control**  **run**  **plot v(3) v(4)**  **.endc**  **.end** |

# Simulation plots

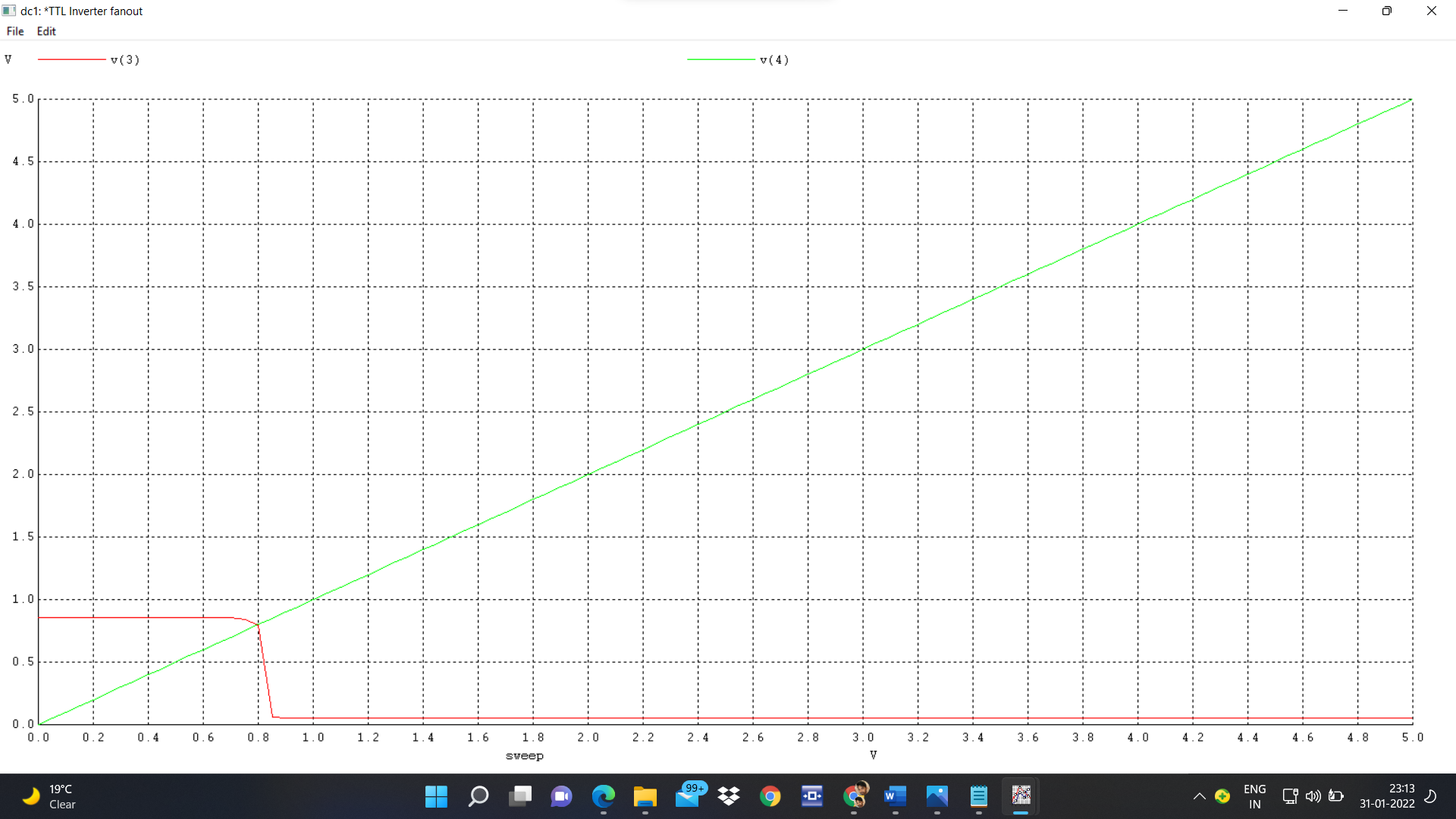


**TTL inverter Fan-out:**

**Spice Code**

|  |
| --- |
| ***\*TTL Inverter fanout U19EC046***  **.model switch NPN (Bf=20)**  **Q1 2 1 4 switch**  **Q2 3 2 0 switch**  **R2 5 3 1.6k**  **R1 5 1 4k**  **Vcc 5 0 5**  **Vin 4 0 5**  **.subckt ttl out in c 0**  **Q3 out y 0 switch**  **Q4 y z in switch**  **R3 out c 1.6k**  **R4 z c 4k**  **.ends ttl**  **x1 out1 3 5 0 ttl**  **x2 out2 3 5 0 ttl**  **x3 out3 3 5 0 ttl**  **x4 out4 3 5 0 ttl**  **.dc Vin 0 5 0.05**  **.control**  **run**  **plot v(3) v(4)**  **.endc**  **.end** |

# Simulation plots



**Simulation results and practical calculations**:

***TTL inverter transient analysis***

Propagation delay = (1.5+0.25)/2 = 0.875nS

Tr = 3.5nS

Tf = 0.2nS

***TTL inverter static analysis***

NML = VIL – VOL = 0.68 – 0.06 = 0.62V

NMH = VOH – VIH = 5 – 0.85 = 4.15V

NM = min(NML , NMH) = 0.62V

VTH = 0.79V

***TTL fanout calculation***

Observation table:

|  |  |  |
| --- | --- | --- |
|  | Theoretical | Practical |
| Fan-out | X | 4 |

**CONCLUSION**

## In this experiment we have studied about the RTL logic and its characteristic parameters as well as compared the theoretical results with practical results of RTL inverter.