**U19EC046 | DIC LAB 3**

**AIM**

Implement DTL Inverter using NPN BJT.

1. Plot VTC and Calculate Noise Margin.
2. Verify its functionality by performing transient analysis.
3. Find theoretical and practical Fan Out and compare them.

**THEORY**

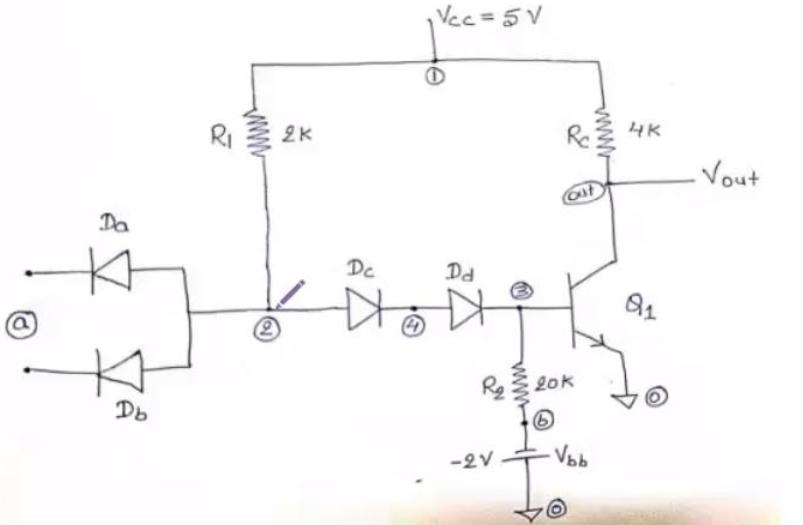
**Introduction**

Diode-Transistor Logic, or DTL, refers to the technology for designing and fabricating digital circuits wherein logic gates employ both diodes and transistors. DTL offers better noise margins and greater fan-outs than RTL, but suffers from low speed, especially in comparison to TTL.

RTL allows the construction of NOR gates easily, but NAND gates are relatively more difficult to get from RTL. DTL, however, allows the construction of simple NAND gates from a single transistor, with the help of several diodes and resistors.

Below figure shows an example of an 2-input DTL NAND gate. It consists of a single transistor Q configured as an inverter, which is driven by a current that depends on the inputs to the three input diodes D1 and D2.

**Circuit Diagram**



**Working principle**

In the NAND gate in Figure 1, the current through diodes DA and DB will only be large enough to drive the transistor into saturation and bring the output voltage Vo to logic '0' if all the input diodes D1 qne D3 are 'off', which is true when the inputs to all of them are logic '1'. This is because when D1-D3 are not conducting, all the current from Vcc through R will go through DA and DB and into the base of the transistor, turning it on and pulling Vo to near ground.

However, if any of the diodes D1 and D2 gets an input voltage of logic '0', it gets forward-biased and starts conducting. This conducting diode 'shunts' almost all the current away from the reverse-biased DA and DB, limiting the transistor base current. This forces the transistor to turn off, bringing up the output voltage Vo to logic '1'.

**Application**

One advantage of DTL over RTL is its better noise margin. The noise margin of a logic gate for logic level '0', Δ0, is defined as the difference between the maximum input voltage that it will recognize as a '0' (Vil) and the maximum voltage that may be applied to it as a '0' (Vol of the driving gate connected to it). For logic level '1', the noise margin Δ1 is the difference between the minimum input voltage that may be applied to it as a '1' (Voh of the driving gate connected to it) and the minimum input voltage that it will recognize as a '1' (Vih).

**SPICE CODE**

1. VTC and noise margin

|  |
| --- |
| ***\* modified dtl transfer char***  **.model mybjt npn bf=20**  **.model mydiode d**  **.subckt modifiedDTL in1 in2 vccNode gnd out**  **rc vccNode out 2k**  **q2 out q2base gnd mybjt**  **r3 q2base gnd 5k**  **dd q1emmiter q2base mydiode**  **q1 q1collector q1base q1emmiter mybjt**  **r2 q1collector q1base 2k**  **r1 q1collector vccNode 1.75k**  **da q1base in1 mydiode**  **db q1base in2 mydiode**  **.ends dtlckt**  ***\*supply***  **vcc vccNode 0 5**  **Va in 0 5**  ***\*driver gate***  **Xd in in vccNode 0 out1 modifiedDTL**  **.dc Va 0.5 5 0.05**  **.control**  **run**  **plot v(in) v(out1)**  **.endc**  **.end** |

1. Propogation delay

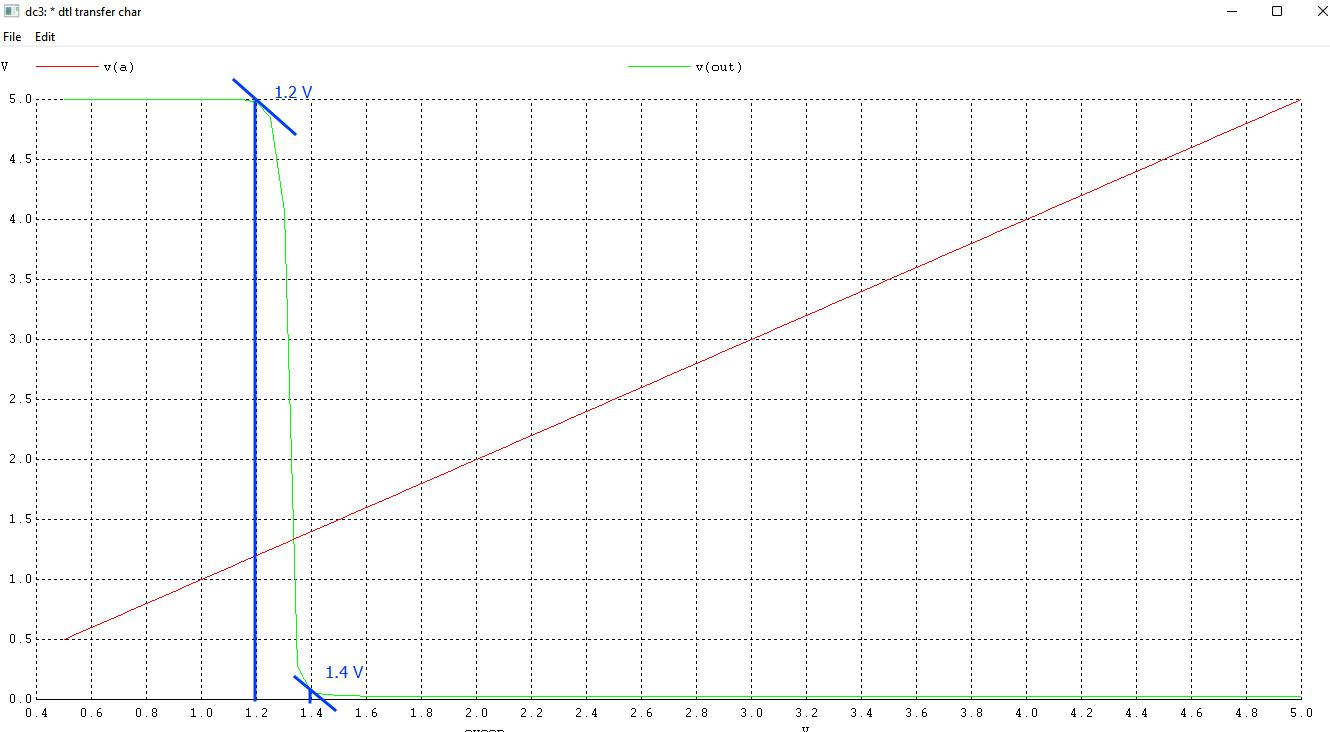
|  |
| --- |
| ***\* dtl transfer char***  **.model q1 npn bf=50**  **.model d1 d**  **q11 out 3 0 q1**  **da 2 a d1**  **db 2 a d1**  **dc 2 4 d1**  **dd 4 3 d1**  **r1 1 2 2k**  **rc 1 out 4k**  **r2 3 b 20k**  **vbb b 0 -2**  **vec 1 0 5**  **va a 0 pulse(0 5 20ps 10ps 10ps 200ps 550ps)**  **.tran 20ps 1500ps**  **.control**  **run**  **plot v(a) v(out)**  **.endc**  **.end** |

1. Fan Out

|  |
| --- |
| ***\*DTL NAND FANOUT***  **.model q1 npn bf=50**  **.model d1 d**  **.subckt dtlckt a b c 1 0 out**  **q1 out 4 0 q1**  **da 2 a d1**  **db 2 b d1**  **dc 2 3 d1**  **dd 3 4 d1**  **r1 2 1 2k**  **rc 1 out 4k**  **r2 4 c 20k**  **.ends dtlckt**  ***\*supply***  **vcc 1 0 5**  **vbb c 0 -2**  **Va a 0 5**  ***\*driver gate***  **Xd a a c 1 0 out1 dtlckt**  ***\*Load gates***  **XL1 out1 out1 c 1 0 out2 dtlckt**  **XL2 out1 out1 c 1 0 out3 dtlckt**  **XL3 out1 out1 c 1 0 out4 dtlckt**  **XL4 out1 out1 c 1 0 out5 dtlckt**  **XL5 out1 out1 c 1 0 out6 dtlckt**  **XL6 out1 out1 c 1 0 out7 dtlckt**  **XL7 out1 out1 c 1 0 out8 dtlckt**  **XL8 out1 out1 c 1 0 out9 dtlckt**  **XL9 out1 out1 c 1 0 out10 dtlckt**  **XL10 out1 out1 c 1 0 out11 dtlckt**  **XL11 out1 out1 c 1 0 out12 dtlckt**  **XL12 out1 out1 c 1 0 out13 dtlckt**  **XL13 out1 out1 c 1 0 out14 dtlckt**  **XL14 out1 out1 c 1 0 out15 dtlckt**  **XL15 out1 out1 c 1 0 out16 dtlckt**  **XL16 out1 out1 c 1 0 out17 dtlckt**  **XL17 out1 out1 c 1 0 out18 dtlckt**  **XL18 out1 out1 c 1 0 out19 dtlckt**  **XL19 out1 out1 c 1 0 out20 dtlckt**  **XL20 out1 out1 c 1 0 out21 dtlckt**  **XL21 out1 out1 c 1 0 out22 dtlckt**  **XL22 out1 out1 c 1 0 out23 dtlckt**  **XL23 out1 out1 c 1 0 out24 dtlckt**  **XL24 out1 out1 c 1 0 out25 dtlckt**  **XL25 out1 out1 c 1 0 out26 dtlckt**  **XL26 out1 out1 c 1 0 out27 dtlckt**  **XL27 out1 out1 c 1 0 out28 dtlckt**  **XL28 out1 out1 c 1 0 out29 dtlckt**  **XL29 out1 out1 c 1 0 out30 dtlckt**  **XL30 out1 out1 c 1 0 out31 dtlckt**  **XL31 out1 out1 c 1 0 out32 dtlckt**  **XL32 out1 out1 c 1 0 out33 dtlckt**  **XL33 out1 out1 c 1 0 out34 dtlckt**  **XL34 out1 out1 c 1 0 out35 dtlckt**  **XL35 out1 out1 c 1 0 out36 dtlckt**  **XL36 out1 out1 c 1 0 out37 dtlckt**  **XL37 out1 out1 c 1 0 out38 dtlckt**  **XL38 out1 out1 c 1 0 out39 dtlckt**  **XL39 out1 out1 c 1 0 out40 dtlckt**  **XL40 out1 out1 c 1 0 out41 dtlckt**  **XL41 out1 out1 c 1 0 out42 dtlckt**  **XL42 out1 out1 c 1 0 out43 dtlckt**  **.dc Va 0.5 5 0.05**  **.control**  **run**  **plot V(out1) V(a)**  **.endc**  **.end** |

**SIMULATION RESULTS AND PRACTICAL CALCULATIONS**

1. **VTC and noise margin**



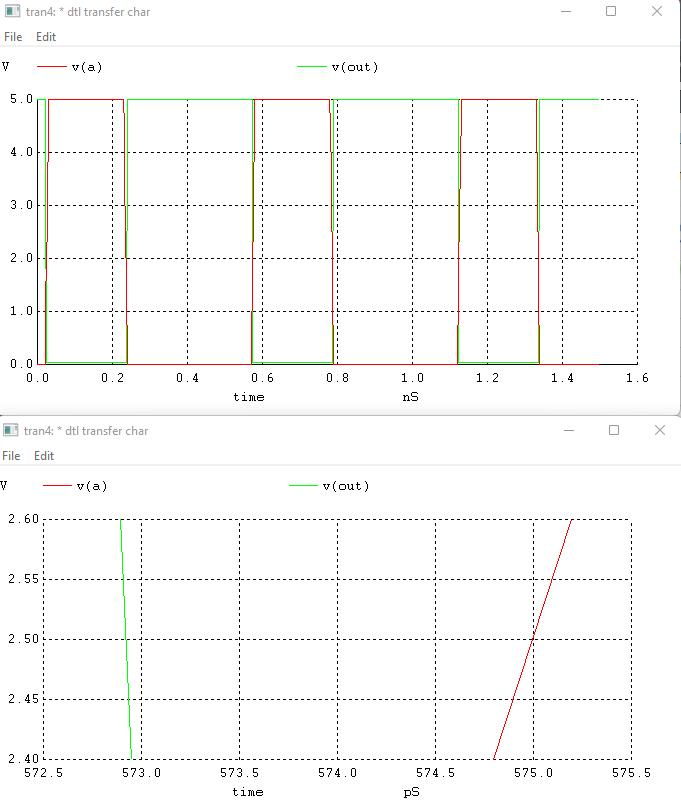
Vil = 1.2 V, Vih = 1.4 V, Voh =5V, Vol = 0.05 V

NM\_H = 5 - 1.4 = 3.6V

NM\_L = 1.2 - 0.05 = 1.15V

NM = min(NM\_H, NM\_L) = 1.15V

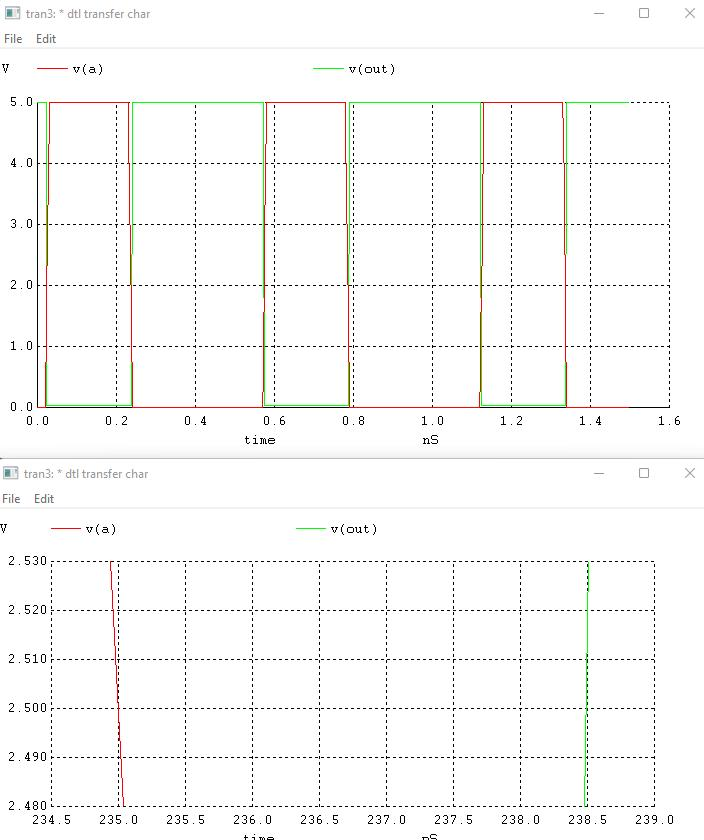
1. **Propogation delay**
2. High to Low



t1 = 572.8us, t2 = 575us

t\_hl = 2.2us

1. Low to High

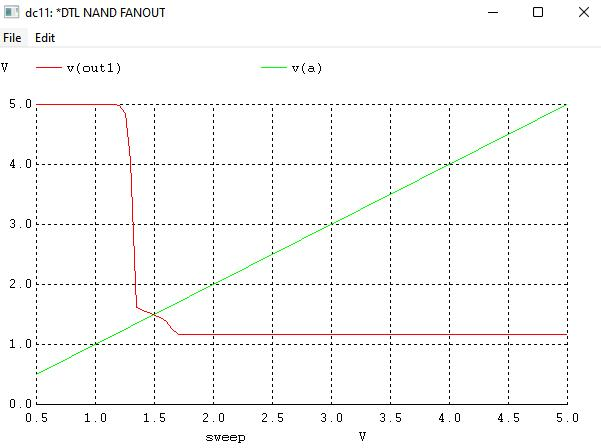


t1 = 235us, t2 = 238.5us

t\_hl = 3.5us

t\_propogation\_delay = avg(2.2, 3.5) = 2.85us

1. **Fan Out**



Fan Out = 42

**CONCLUSION**

We implemented DTL inverter using NPN BJT. We plotted VT characteristics of DTL, obtained its noise margin, and verified its functionality by performing transient analysis.