**U19EC046 | DIC | LAB 4**

**AIM**

Implement Modified diode transister logic (MDTL) using NPN BJT. Bf = 20, R1 = 1.75k, R2 = 2k, R3 = 5k and Rc = 2k

1. Verify its functionality as NAND gate and calculate propagation delay.
2. Plot VTC and Calculate Noise Margin.
3. Compare DTL with MDTL with respect to noise margin, fan-out and propagation delay comment about it.

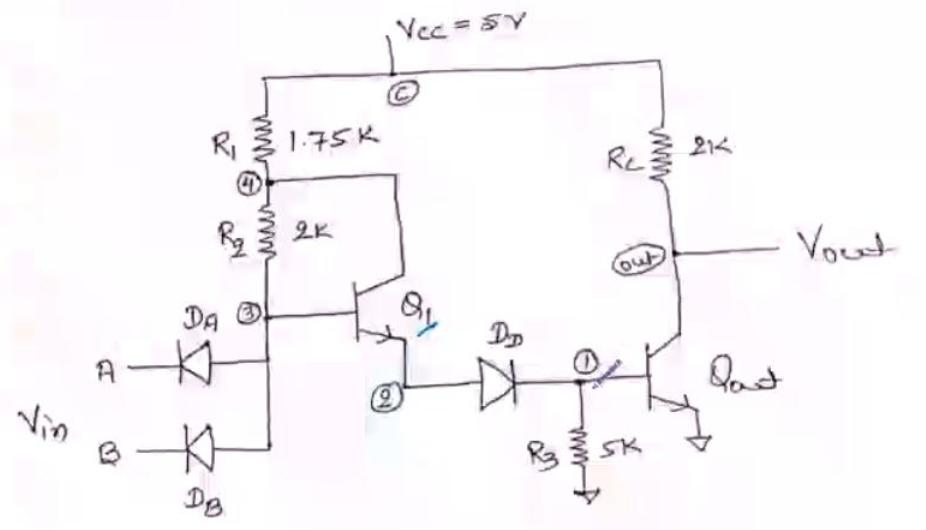
**THEORY**

**Introduction**

The diode-transistor logic, also termed as DTL, replaced RTL family because of greater fan-out capability and more noise margin. As its name suggests, DTL circuits mainly consists of diodes and transistors that comprises DTL devices.

Due to number of diodes used in this circuit, the speed of the circuit is significantly low. Hence this family of logic gates is modified to transistor-transistor logic i.e. TTL family.

**Circuit Diagram**



**Working principle**

The fan out of IC positive DTL NAND gate of may be increased by replacing the diode by a transistor Q1 as shown in figure 6. Thus, transistor Q1 while conducting is in its active region and not in saturation. This results from the fact that the current through resistor R1(1.75 K-OHMs) is in a direction to reverse bias the collector junction of NPN transistor Q1. Further the emitter current of Q1 provides the base current IB2 of Qout. Hence Qout is driven by a much larger base current IB. Hence, for the same value of hFE,the collector current of Qout is much larger permitting much greater fan out.

**Application**

It is used in the applications where noise margin, fan Out requirements are high, and Propagation delay is low.

**SPICE CODE**

1. **Propagation Delay**

|  |
| --- |
| ***\* modified dtl propogation delay***  **.model mybjt npn bf=20**  **.model mydiode d**  **.subckt modifiedDTL in1 in2 vccNode gnd out**  **rc vccNode out 2k**  **q2 out q2base gnd mybjt**  **r3 q2base gnd 5k**  **dd q1emmiter q2base mydiode**  **q1 q1collector q1base q1emmiter mybjt**  **r2 q1collector q1base 2k**  **r1 q1collector vccNode 1.75k**  **da q1base in1 mydiode**  **db q1base in2 mydiode**  **.ends dtlckt**  ***\*supply***  **vcc vccNode 0 5**  **va in 0 pulse(0 5 0ps 1ps 1ps 20us 40us)**  **Xd in in vccNode 0 out1 modifiedDTL**  **c\_load out1 0 1p**  **.tran 20ns 80us**  **.control**  **run**  **plot v(in) v(out1)**  **.endc**  **.end** |

1. **VTC and noise margin**

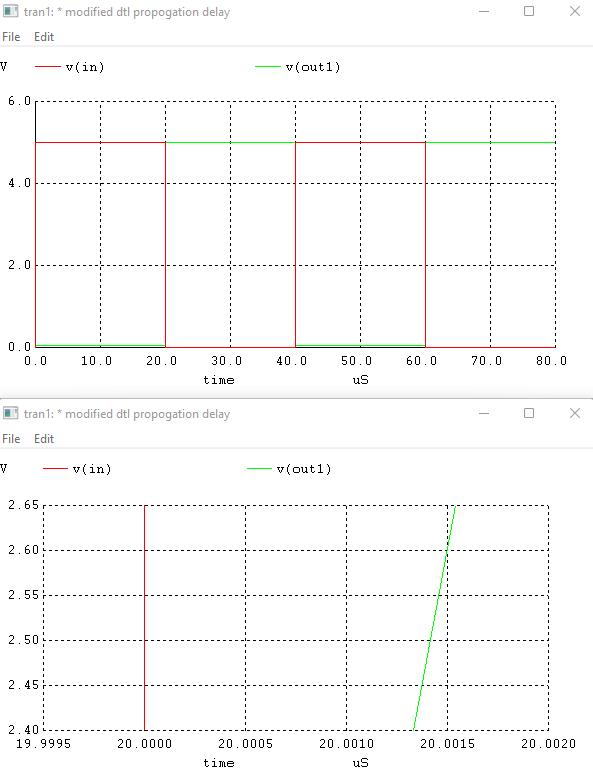
|  |
| --- |
| ***\* modified dtl transfer char***  **.model mybjt npn bf=20**  **.model mydiode d**  **.subckt modifiedDTL in1 in2 vccNode gnd out**  **rc vccNode out 2k**  **q2 out q2base gnd mybjt**  **r3 q2base gnd 5k**  **dd q1emmiter q2base mydiode**  **q1 q1collector q1base q1emmiter mybjt**  **r2 q1collector q1base 2k**  **r1 q1collector vccNode 1.75k**  **da q1base in1 mydiode**  **db q1base in2 mydiode**  **.ends dtlckt**  ***\*supply***  **vcc vccNode 0 5**  **Va in 0 5**  ***\*driver gate***  **Xd in in vccNode 0 out1 modifiedDTL**  **.dc Va 0.5 5 0.05**  **.control**  **run**  **plot v(in) v(out1)**  **.endc**  **.end** |

1. **Fan Out**

|  |
| --- |
| ***\* modified dtl fanout***  **.model mybjt npn bf=50**  **.model mydiode d**  **.subckt modifiedDTL in1 in2 vccNode gnd out**  **rc vccNode out 2k**  **q2 out q2base gnd mybjt**  **r3 q2base gnd 5k**  **dd q1emmiter q2base mydiode**  **q1 q1collector q1base q1emmiter mybjt**  **r2 q1collector q1base 2k**  **r1 q1collector vccNode 1.75k**  **da q1base in1 mydiode**  **db q1base in2 mydiode**  **.ends dtlckt**  ***\*supply***  **vcc vccNode 0 5**  **Va in 0 5**  ***\*driver gate***  **Xd in in vccNode 0 out1 modifiedDTL**  ***\*load gates***  **XL1 out1 out1 vccNode 0 out2 modifiedDTL**  **XL2 out1 out1 vccNode 0 out3 modifiedDTL**  **XL3 out1 out1 vccNode 0 out4 modifiedDTL**  **XL4 out1 out1 vccNode 0 out5 modifiedDTL**  **XL5 out1 out1 vccNode 0 out6 modifiedDTL**  **XL6 out1 out1 vccNode 0 out7 modifiedDTL**  **XL7 out1 out1 vccNode 0 out8 modifiedDTL**  **XL8 out1 out1 vccNode 0 out9 modifiedDTL**  **XL9 out1 out1 vccNode 0 out10 modifiedDTL**  **XL10 out1 out1 vccNode 0 out11 modifiedDTL**  **XL11 out1 out1 vccNode 0 out12 modifiedDTL**  **XL12 out1 out1 vccNode 0 out13 modifiedDTL**  **XL13 out1 out1 vccNode 0 out14 modifiedDTL**  **XL14 out1 out1 vccNode 0 out15 modifiedDTL**  **XL15 out1 out1 vccNode 0 out16 modifiedDTL**  **XL16 out1 out1 vccNode 0 out17 modifiedDTL**  **XL17 out1 out1 vccNode 0 out18 modifiedDTL**  **XL18 out1 out1 vccNode 0 out19 modifiedDTL**  **XL19 out1 out1 vccNode 0 out20 modifiedDTL**  **XL20 out1 out1 vccNode 0 out21 modifiedDTL**  **XL21 out1 out1 vccNode 0 out22 modifiedDTL**  **XL22 out1 out1 vccNode 0 out23 modifiedDTL**  **XL23 out1 out1 vccNode 0 out24 modifiedDTL**  **XL24 out1 out1 vccNode 0 out25 modifiedDTL**  **XL25 out1 out1 vccNode 0 out26 modifiedDTL**  **XL26 out1 out1 vccNode 0 out27 modifiedDTL**  **XL27 out1 out1 vccNode 0 out28 modifiedDTL**  **XL28 out1 out1 vccNode 0 out29 modifiedDTL**  **XL29 out1 out1 vccNode 0 out30 modifiedDTL**  **XL30 out1 out1 vccNode 0 out31 modifiedDTL**  **XL31 out1 out1 vccNode 0 out32 modifiedDTL**  **XL32 out1 out1 vccNode 0 out33 modifiedDTL**  **XL33 out1 out1 vccNode 0 out34 modifiedDTL**  **XL34 out1 out1 vccNode 0 out35 modifiedDTL**  **XL35 out1 out1 vccNode 0 out36 modifiedDTL**  **XL36 out1 out1 vccNode 0 out37 modifiedDTL**  **XL37 out1 out1 vccNode 0 out38 modifiedDTL**  **XL38 out1 out1 vccNode 0 out39 modifiedDTL**  **XL39 out1 out1 vccNode 0 out40 modifiedDTL**  **XL40 out1 out1 vccNode 0 out41 modifiedDTL**  **XL41 out1 out1 vccNode 0 out42 modifiedDTL**  **XL42 out1 out1 vccNode 0 out43 modifiedDTL**  **XL43 out1 out1 vccNode 0 out44 modifiedDTL**  **XL44 out1 out1 vccNode 0 out45 modifiedDTL**  **XL45 out1 out1 vccNode 0 out46 modifiedDTL**  **XL46 out1 out1 vccNode 0 out47 modifiedDTL**  **XL47 out1 out1 vccNode 0 out48 modifiedDTL**  **XL48 out1 out1 vccNode 0 out49 modifiedDTL**  **XL49 out1 out1 vccNode 0 out50 modifiedDTL**  **XL50 out1 out1 vccNode 0 out51 modifiedDTL**  **XL51 out1 out1 vccNode 0 out52 modifiedDTL**  **XL52 out1 out1 vccNode 0 out53 modifiedDTL**  **XL53 out1 out1 vccNode 0 out54 modifiedDTL**  **XL54 out1 out1 vccNode 0 out55 modifiedDTL**  **XL55 out1 out1 vccNode 0 out56 modifiedDTL**  **XL56 out1 out1 vccNode 0 out57 modifiedDTL**  **XL57 out1 out1 vccNode 0 out58 modifiedDTL**  **XL58 out1 out1 vccNode 0 out59 modifiedDTL**  **XL59 out1 out1 vccNode 0 out60 modifiedDTL**  **XL60 out1 out1 vccNode 0 out61 modifiedDTL**  **XL61 out1 out1 vccNode 0 out62 modifiedDTL**  **XL62 out1 out1 vccNode 0 out63 modifiedDTL**  **XL63 out1 out1 vccNode 0 out64 modifiedDTL**  **XL64 out1 out1 vccNode 0 out65 modifiedDTL**  **XL65 out1 out1 vccNode 0 out66 modifiedDTL**  **XL66 out1 out1 vccNode 0 out67 modifiedDTL**  **XL67 out1 out1 vccNode 0 out68 modifiedDTL**  **XL68 out1 out1 vccNode 0 out69 modifiedDTL**  **XL69 out1 out1 vccNode 0 out70 modifiedDTL**  **XL70 out1 out1 vccNode 0 out71 modifiedDTL**  **XL71 out1 out1 vccNode 0 out72 modifiedDTL**  **XL72 out1 out1 vccNode 0 out73 modifiedDTL**  **XL73 out1 out1 vccNode 0 out74 modifiedDTL**  **XL74 out1 out1 vccNode 0 out75 modifiedDTL**  **XL75 out1 out1 vccNode 0 out76 modifiedDTL**  **XL76 out1 out1 vccNode 0 out77 modifiedDTL**  **XL77 out1 out1 vccNode 0 out78 modifiedDTL**  **XL78 out1 out1 vccNode 0 out79 modifiedDTL**  **XL79 out1 out1 vccNode 0 out80 modifiedDTL**  **XL80 out1 out1 vccNode 0 out81 modifiedDTL**  **XL81 out1 out1 vccNode 0 out82 modifiedDTL**  **XL82 out1 out1 vccNode 0 out83 modifiedDTL**  **XL83 out1 out1 vccNode 0 out84 modifiedDTL**  **XL84 out1 out1 vccNode 0 out85 modifiedDTL**  **XL85 out1 out1 vccNode 0 out86 modifiedDTL**  **XL86 out1 out1 vccNode 0 out87 modifiedDTL**  **XL87 out1 out1 vccNode 0 out88 modifiedDTL**  **XL88 out1 out1 vccNode 0 out89 modifiedDTL**  **.dc Va 0.5 5 0.05**  **.control**  **run**  **plot V(out1) V(in)**  **.endc**  **.end** |

**SIMULATION RESULTS AND PRACTICAL CALCULATIONS**

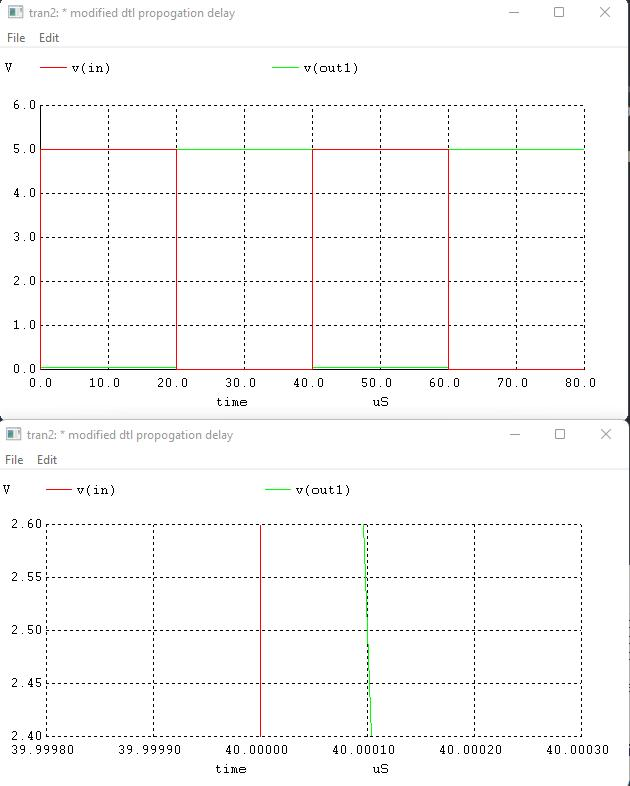
1. **Propagation Delay**
2. Low to High



t1 = 20us, t2 = 20.00142us

t\_lh = 1.42 ns

1. High to low

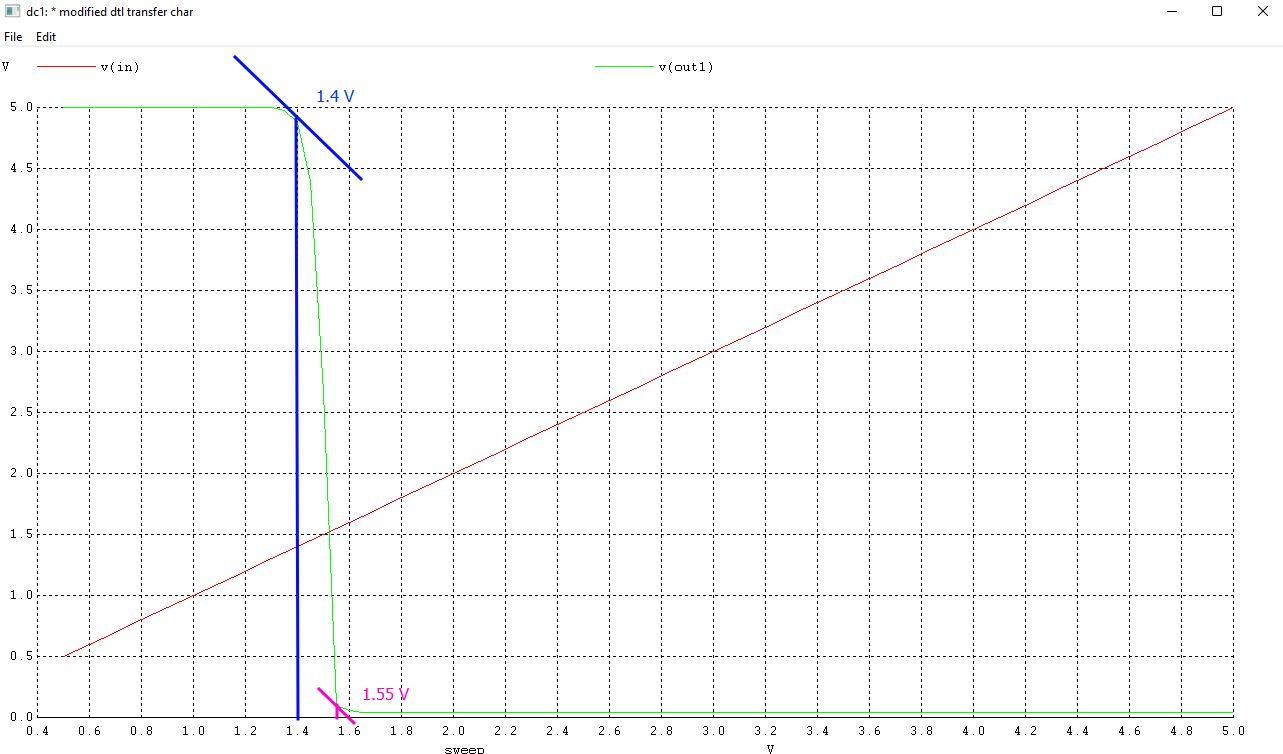


t1 = 40us, t2 = 40.0001us

t\_hl = 0.1ns

t\_propogation\_delay = avg(1.42, 0.1) = 0.75ns

1. **VTC and Noise Margin**



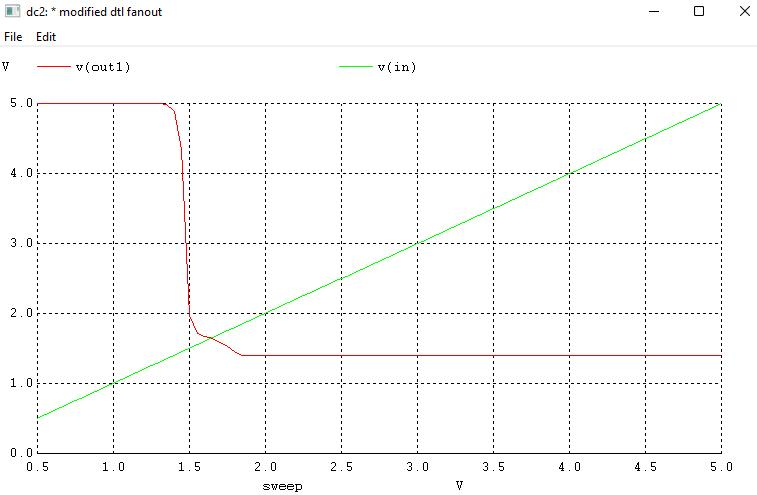
Voh = 5V, Vol = 0.1V, Vih = 1.55V, Vil = 1.4V

NM\_H = 5 - 1.55 = 3.45V

NM\_L = 1.4 - 0.1 = 1.3V

NM = min(NM\_H, NM\_L) = 1.3V

1. **Fan Out**



Fan Out = 88 (Bf = 50)

Fan Out = 33 (Bf = 20)

**COMPARISION OF DTL and MDTL**

|  |  |  |
| --- | --- | --- |
| **Parameter** | **DTL** | **MDTL** |
| Noise Margin | 1.15V | 1.3V |
| Propogation delay | 2.85us | 0.75ns |
| Fan out | 42 | 88 |

**CONCLUSION**

In this Experiment we have studied and written spice code for Modified diode transistor logic and also calculated its VTC, noise margin and fanout, it was observed that the noise margin of MDTL is increased slightly and the propagartion delaay was reduced by an order of 10^3 and fan out is increased substantially as compared with DTL family.