**U19EC046 | DIC LAB 5**

**AIM**

Implement TTL inverter using NPN BJT having Bf = 50, Rb = 4k and Rc = 1.6k.

1. Verify its functionality by performing transient analysis.
2. Plot the VTC & Calculate the Noise margin.
3. Find out theoretical and practical fan-out & compare them.

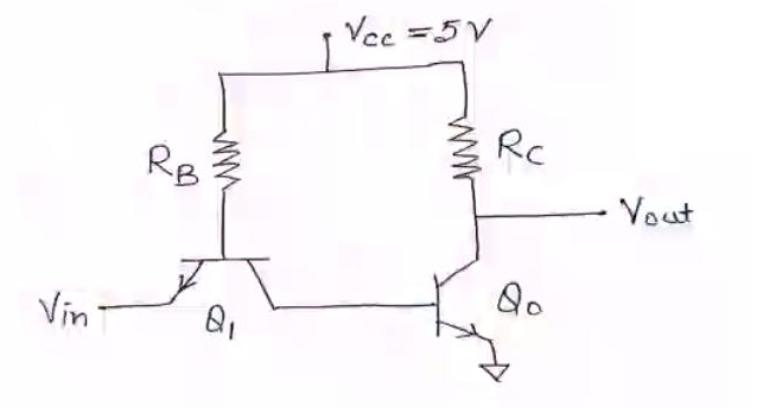
**THEORY**

**Introduction**

DTL was able to improve fan-out compared to RTL. However, that was done at the expense of Transient response and Chip area.

A solution for the problem was proposed in the form of a new logic family which utilizes only transistors and resistors. BJTs are smaller than diodes.

**Circuit Diagram**

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**Working principle**

For Vin very low, the base-emitter junction of Q1 will be forward biased. The base-collector junction will also be forward biased. Therefore, Q1 will be saturated.

The base-emitter voltage of Q0 is:

VBE, 0 = VCE,1(Sat) + Vin

Therefore, Q0 will be cut-off

Therefore,

Vout = VOH = VCC

As Vin is increased, VB of Q0 will also increase. Eventually, Q0 will turn on.

This happens when:

Vin = VIL = VBE,0(FA) – VCE,I(Sat)

As Vin is increased even more, Q0 comes closer to Saturation and eventually saturates.

At that point:

Vout = VOL = VCE,0 (Sat)

**SPICE CODE**

1. Transient Analysis

|  |
| --- |
| ***\*TTL Inverter Transient Analysis***  **.model switch NPN (Bf=50)**  **.subckt ttl out in vcc\_power gnd**  **Q1 out q1\_base gnd switch**  **Q2 q1\_base q2\_base in switch**  **Rc out vcc\_power 1.6k**  **Rb q2\_base vcc\_power 4k**  **.ends ttl**  **xd out input vcc\_node 0 ttl**  **Vcc vcc\_node 0 5**  **Vin input 0 pulse(0 5 1ns 1ns 1ns 20us 40us)**  **c\_load out 0 1p**  **.tran 1ns 80us**  **.control**  **run**  **plot v(input) v(out)**  **.endc**  **.end** |

1. VTC and noise Margin

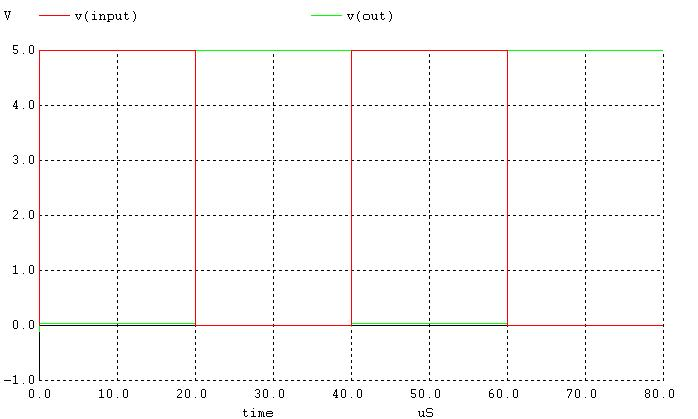
|  |
| --- |
| ***\*TTL Inverter  Analysis***  **.model switch NPN (Bf=50)**  **.subckt ttl out in vcc\_power gnd**  **Q1 out q1\_base gnd switch**  **Q2 q1\_base q2\_base in switch**  **Rc out vcc\_power 1.6k**  **Rb q2\_base vcc\_power 4k**  **.ends ttl**  **xd out input vcc\_node 0 ttl**  **Vcc vcc\_node 0 5**  **Vin input 0 5**  **c\_load out 0 1p**  **.dc Vin 0 5 0.05**  **.control**  **run**  **plot v(input) v(out)**  **.endc**  **.end** |

1. Fan-out

|  |
| --- |
| ***\*TTL Inverter Fanout Analysis***  **.model switch NPN (Bf=50)**  **.subckt ttl out in vcc\_power gnd**  **Q1 out q1\_base gnd switch**  **Q2 q1\_base q2\_base in switch**  **Rc out vcc\_power 1.6k**  **Rb q2\_base vcc\_power 4k**  **.ends ttl**  **xd out input vcc\_node 0 ttl**  **Vcc vcc\_node 0 5**  **Vin input 0 pulse(0 5 1ns 1ns 1ns 20us 40us)**  **x1 out1 out vcc\_node 0 ttl**  **x2 out2 out vcc\_node 0 ttl**  **x3 out3 out vcc\_node 0 ttl**  **x4 out4 out vcc\_node 0 ttl**  **x5 out5 out vcc\_node 0 ttl**  **x6 out6 out vcc\_node 0 ttl**  **x7 out7 out vcc\_node 0 ttl**  **.dc Vin 0 5 0.001**  **.control**  **run**  **plot v(input) v(out) v(out1)**  **.endc**  **.end** |

**SIMULATION RESULTS AND PRACTICAL CALCULATIONS**

1. Transient Analysis



For Low to High:

t1 = 2.0025us, t2 = 2.0039us

tLH = 1.4ns

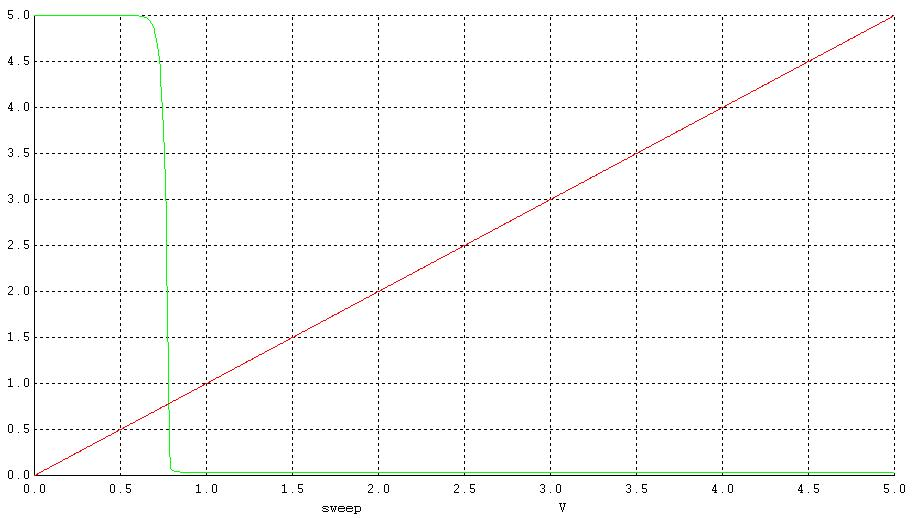
For High to Low

t1 = 40.00125, t2 = 40.0015

tHL = 1.25ns

Propagation Delay = 1.325ns

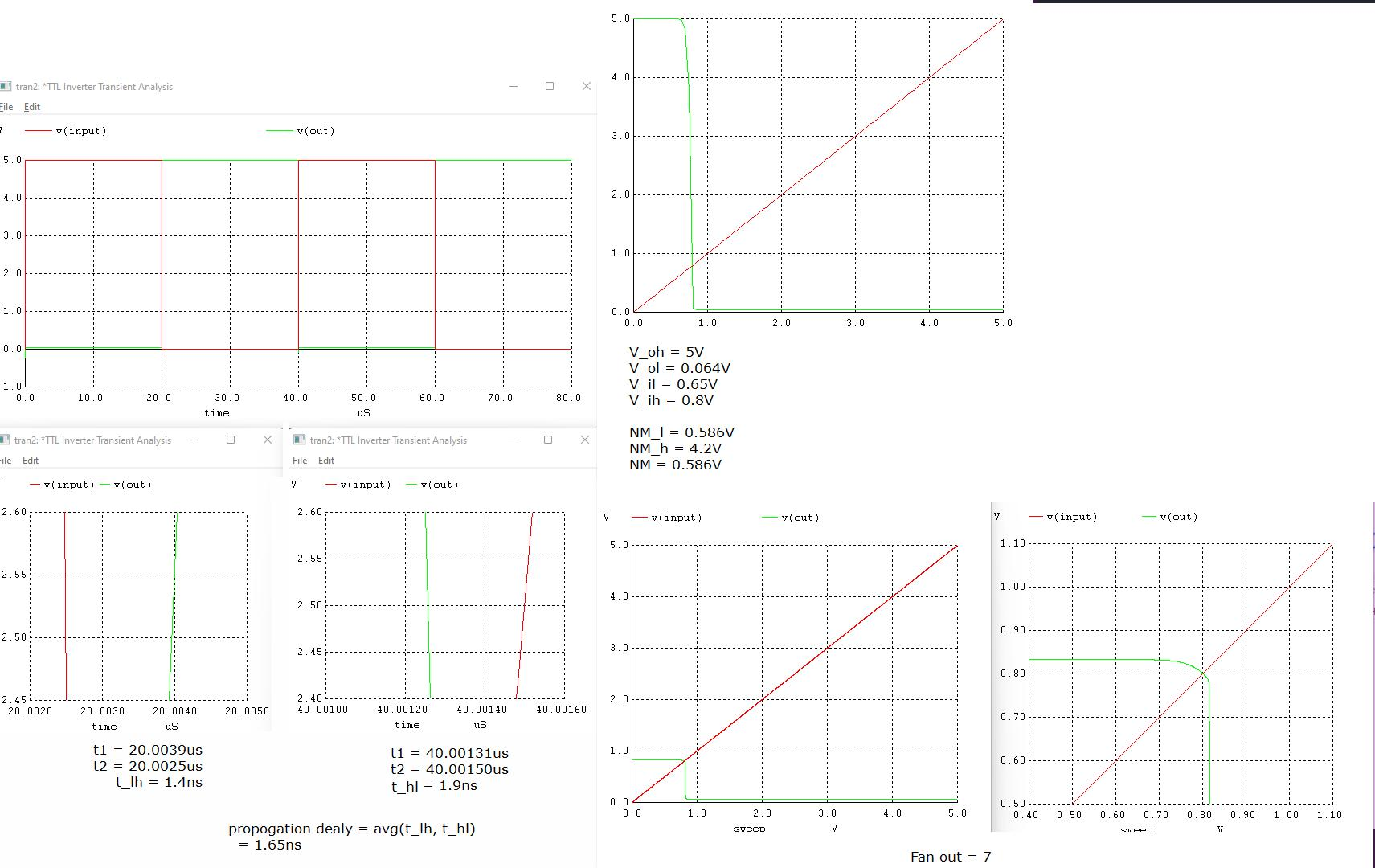
1. VTC and noise Margin



Vih =0.8V, Vil=0.65V, Voh=5V, Vih=0.8V

NML=0.591V, NMH = 4.2V, NM = 0.591V

1. Fan-out



**CONCLUSION**

In this practical we have implemented spice code TTL inverter and found out its VTC, Noise margin, Propagation delay and fanout. it was observed that the propagation delay of TTL family is lower than DTL