**U19EC046 | DIC LAB 6**

**AIM**

Aim: To design and verify the performance of given Resistively Loaded NMOS inverter circuit to obtain VOL = 0.147V for the given specifications:

Kn’= 20pA/V,VTO = 0.8V, VDD = 5V, W/L= 2um/1um.

Find the noise margin of the circuit. Also see the effect of change in RL on noise margin and comment on it.

**THEORY**

When the input of the driver transistor is less than threshold voltage VTH (Vin < VTH), driver transistor is in the cut – off region and does not conduct any current. So, the voltage drop across the load resistor is ZERO and output voltage is equal to the VDD. Now, when the input voltage increases further, driver transistor will start conducting the non-zero current and NMOS goes in saturation region.

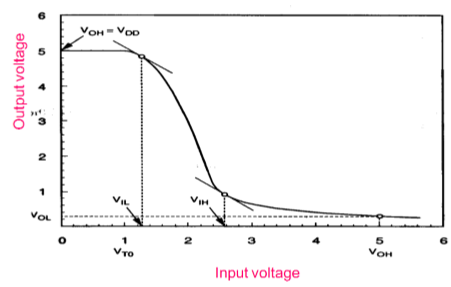
Mathematically,

ID=Kn2[VGS−VTO]2ID=Kn2[VGS−VTO]2

Increasing the input voltage further, driver transistor will enter into the linear region and output of the driver transistor decreases.

ID=Kn22[VGS−VTO]VDS−V2DSID=Kn22[VGS−VTO]VDS−VDS2

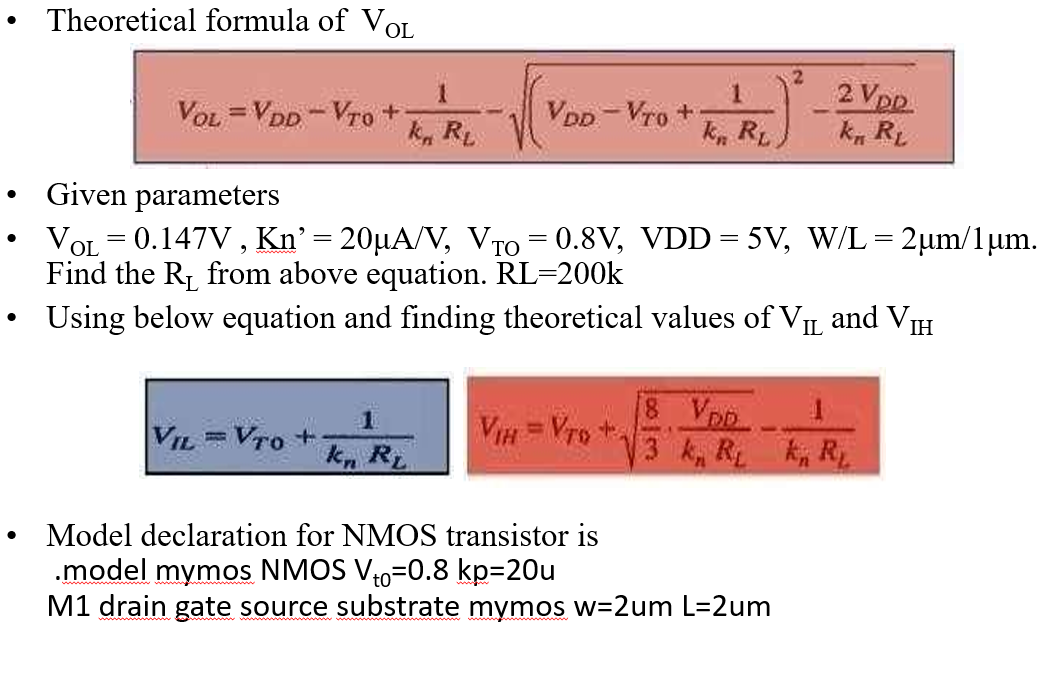
VTC of the resistive load inverter, shown below, indicates the operating mode of driver transistor and voltage points.



## Inverter with N type MOSFET Load

The main advantage of using MOSFET as load device is that the silicon area occupied by the transistor is smaller than the area occupied by the resistive load. Here, MOSFET is active load and inverter with active load gives a better performance than the inverter with resistive load.

**Formulas:**



**Circuit Diagram**

**Theoretical Calculations**

**SPICE CODE**

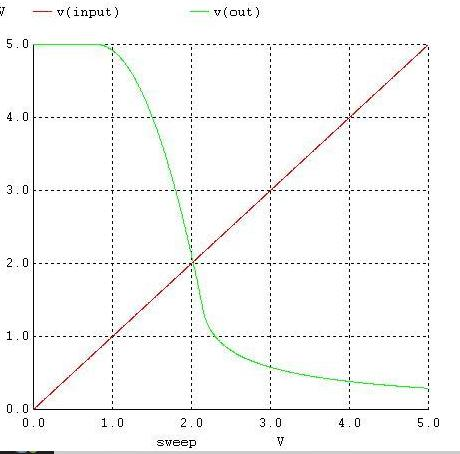
|  |
| --- |
| **# NMOS**  **.model mymos NMOS (Vt0=0.8, Kt=20u)**  **.subckt mosinverter in vdd\_node out gnd**  **M1 out in gnd gnd mymos w=2um l=1um**  **RL vdd\_node out 200k**  **.ends mosinverter**  **xd input vdd\_node out 0 mosinverter**  **Vdd vdd\_node 0 5**  **Vin input 0 5**  **.dc Vin 0 5 0.005**  **.control**  **run**  **plot v(input) v(out)**  **.endc**  **.end** |

|  |
| --- |
| ***\*U19Ec046 Resistively Loaded NMOS Inverter DC Analysis***  **.model mynmos nmos Vto=0.8 kp=20u**  **M1 out in 0 0 mynmos w=2u l=1u**  **Rl 1 out 200k**  **Vdd 1 0 5**  **Vin in 0 pulse (0 5 1ns 1ns 1ns 20ns 40ns)**  **.tran 1ns 50ns**  **.control**  **run**  **plot V(in) V(out)**  **.endc**  **.end** |

|  |
| --- |
| **# NMOS**  **.model mymos NMOS (Vt0=0.8, Kt=20u)**  **.subckt mosinverter in vdd\_node out gnd**  **M1 out in gnd gnd mymos w=2um l=1um**  **RL vdd\_node out 100k**  **.ends mosinverter**  **.subckt mosinverter2 in vdd\_node out gnd**  **M1 out in gnd gnd mymos w=2um l=1um**  **RL vdd\_node out 200k**  **.ends mosinverter2**  **.subckt mosinverter3 in vdd\_node out gnd**  **M1 out in gnd gnd mymos w=2um l=1um**  **RL vdd\_node out 300k**  **.ends mosinverter3**  **.subckt mosinverter4 in vdd\_node out gnd**  **M1 out in gnd gnd mymos w=2um l=1um**  **RL vdd\_node out 400k**  **.ends mosinverter4**  **xd input vdd\_node out\_100k 0 mosinverter**  **xd1 input vdd\_node out\_200k 0 mosinverter2**  **xd2 input vdd\_node out\_300k 0 mosinverter3**  **xd3 input vdd\_node out\_400k 0 mosinverter4**  **Vdd vdd\_node 0 5**  **Vin input 0 5**  **.dc Vin 0 5 0.005**  **.control**  **run**  **plot v(input) v(out\_100k) v(out\_200k) v(out\_300k) v(out\_400k)**  **.endc**  **.end** |

**SIMULATION RESULTS AND PRACTICAL CALCULATIONS**

1.



[28-02 14:46] SUTHAR HARSH MUKESHBHAI HARSH

Vil = 1.1V

vih = 2.4V

voh = 5V

vol = 0.3V

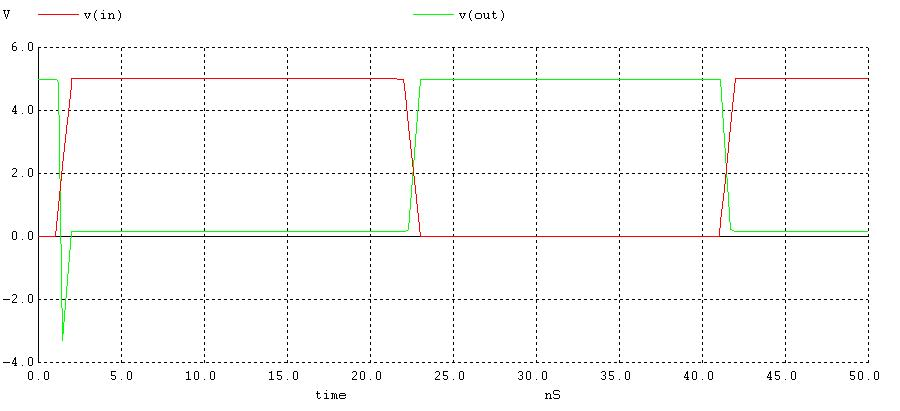
VTH = 2V

NM\_L = 0.8V

NM\_H = 2.6V

NM = 0.8V

2.



tpHL = t1 - t2 = (40.0092-40.0013) s = 7.9 nS

tpLH = t1`- t2` = (20.135-20.0025) s = 132.5 nS

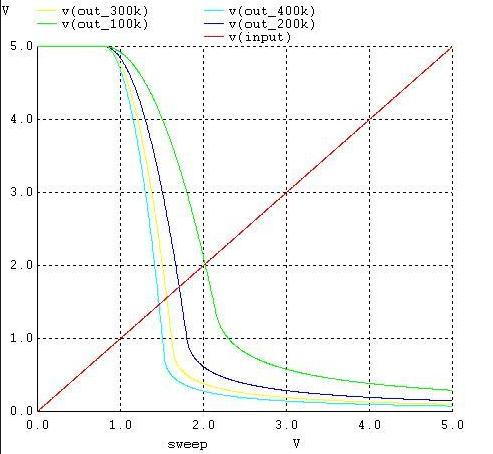
Propagation delay,

= tPLH+tPHL2 = 132.5+7.92 = 70.2 nS

Tr = (20.46-20.0175)s = 442.5 nS

Tf = (40.0223- 40.00312)s = 19.18 nS

3.



**CONCLUSION**