**fU19EC046 | DIC LAB 7**

**AIM**

Design and verify the performance of given saturated loaded NMOS inverter circuit

to obtain Vih-2.9, for the given design parameter VDD=5V, Kn’=20ua/v2, Vtl-0.8V,

Vtl=0.8V,(W/L)driver=2um/lum.

a) Compare the theoretical and practical values of the critical voltages on VTC& find noise margins of the circuit.

b) observe the effect of change in (W/L)loaded on noise margin &comment on it.

c) Also compare the results of noise with resistive loaded NMOS inverter for

RL=200k

**THEORY**

Saturated load device. An n-channel enhancement-mode MOSFET with the gate connected to the drain can be used as load device in an NMOS inverter. Since the gate and drain of the transistor are connected, we have V GS-V DS When V GS-V DS>V TN, a non zero drain current is induced in the transistor and thus the transistor operates in saturation only.

**CIRCUIT**

**CALCULATIONS**

**SPICE CODE**

|  |
| --- |
| \*saturated load inverter static analysis  .model mymos NMOS (Vt0=0.8 kp=20u)  M1 1 1 out 0 mymos l=1u w=2u  M2 out in 0 0 mymos l=1u w=2u  Vdd 1 0 5V  Vin in 0 5V  .dc Vin 0 5 0.05  .control  run  plot V(out) V(in)  .endc  .end |

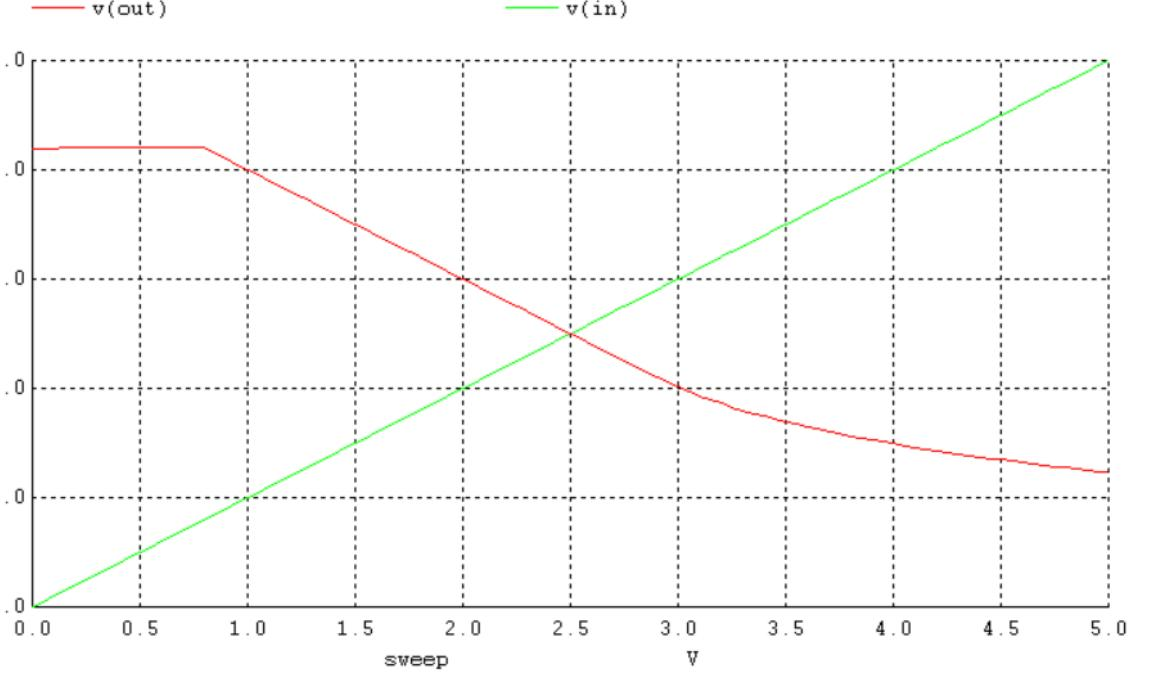
|  |
| --- |
| \*saturated load inverter static analysis  .model mymos NMOS (Vt0=0.8 kp=20u)  M1 d1 d1 out 0 mymos l=1u w=2u  M2 out in 0 0 mymos l=1u w=2u  Vdd1 d1 0 5V  M11 d2 d2 out1 0 mymos l=1u w=4u  M21 out1 in 0 0 mymos l=1u w=2u  Vdd2 d2 0 5V  M12 d3 d3 out2 0 mymos l=1u w=6u  M22 out2 in 0 0 mymos l=1u w=2u  Vdd3 d3 0 5V  M13 d4 d4 out3 0 mymos l=1u w=8u  M23 out3 in 0 0 mymos l=1u w=2u  Vdd4 d4 0 5V  Vin in 0 5V  .dc Vin 0 5 0.05  .control  run  plot V(out) V(out1) V(out2) V(out3) V(in)  .endc  .end |



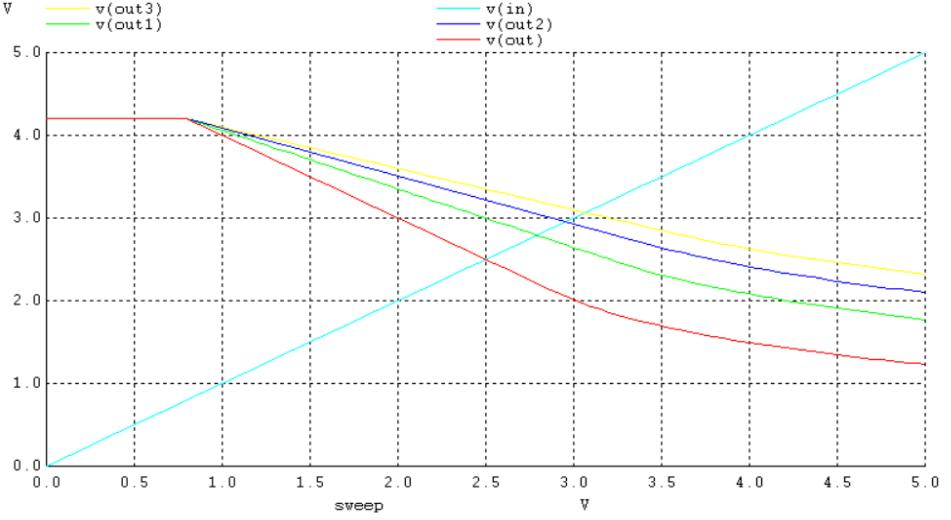
|  |
| --- |
| \*saturated load inverter static analysis  .model mymos NMOS (Vt0=0.8 kp=20u)  M1 d1 d1 out 0 mymos l=1u w=2u  M2 out in 0 0 mymos l=1u w=2u  Vdd1 d1 0 5V  M11 d2 d2 out1 0 mymos l=1u w=4u  M21 out1 in 0 0 mymos l=1u w=2u  Vdd2 d2 0 5V  M12 d3 d3 out2 0 mymos l=1u w=6u  M22 out2 in 0 0 mymos l=1u w=2u  Vdd3 d3 0 5V  M13 d4 d4 out3 0 mymos l=1u w=8u  M23 out3 in 0 0 mymos l=1u w=2u  Vdd4 d4 0 5V  Vin in 0 5V  .dc Vin 0 5 0.05  .control  run  plot V(out) V(out1) V(out2) V(out3) V(in)  .endc  .end |

**SIMULATION RESULTS AND PRACTICAL CALCULATIONS**

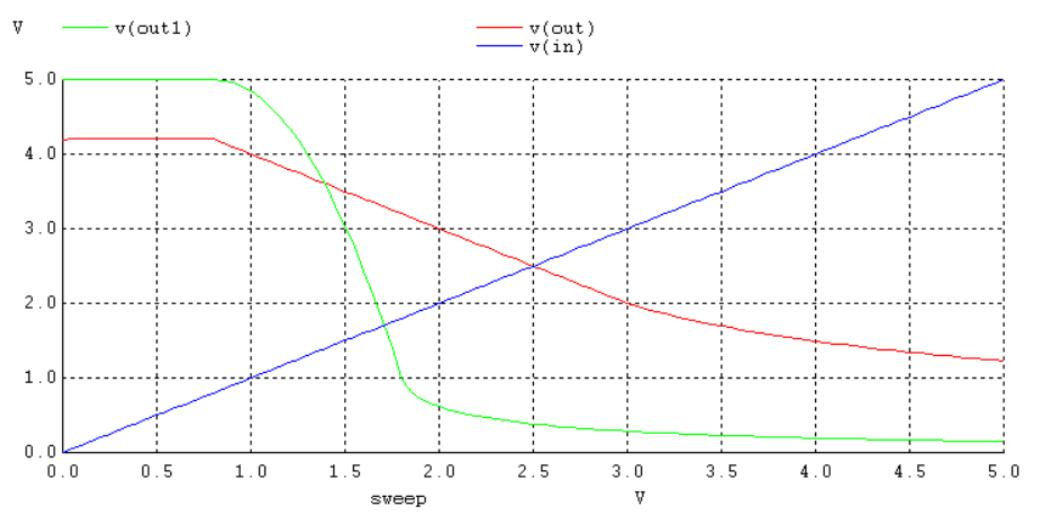
1.



2.



3.



**TABLE OF THEORETICAL AND PRACTICAL CALCULATION**

|  |  |  |
| --- | --- | --- |
| Parameters | Theoretical values | Practically Values |
| VOL | 2.1 V | 1.23 V |
| VOH | 4.2 V | 4.2 V |
| VIL | 0.8 V | 0.85 V |
| VIH | 2.9 V | 3.2 V |
| VTH | 2.5 V | 2.5 V |
| NML | 1.3 V | 0.38 V |
| NMH | 1.3 V | 1.18 V |

Comparison Of Noise Margin of Resistively and Saturated Loaded NMOS inverter.

|  |  |  |
| --- | --- | --- |
|  | **NML** | **NMH** |
| **Resistively Loaded NMOS** | 0.802 V | 3.12 V |
| **Saturated Loaded NMOS** | 0.302 V | 1.18 V |

**CONCLUSION**