**U19EC046 | DIC LAB 9.2**

**AIM**

Write a winspice code to verify the functionality of NOR based SR Latch

**THEORY**

The SR flip-flop, also known as a SR Latch, can be considered as one of the most basic sequential logic circuit possible. This simple flip-flop is basically a one-bit memory bistable device that has two inputs, one which will “SET” the device (meaning the output = “1”), and is labelled S and one which will “RESET” the device (meaning the output = “0”), labelled R.

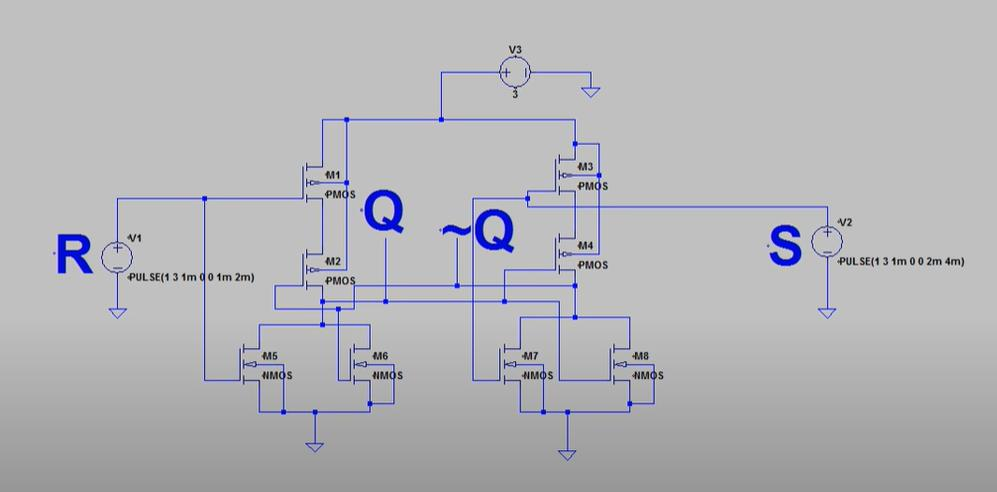
Then the SR description stands for “Set-Reset”. The reset input resets the flip-flop back to its original state with an output Q that will be either at a logic level “1” or logic “0” depending upon this set/reset condition.

A basic NAND gate SR flip-flop circuit provides feedback from both of its outputs back to its opposing inputs and is commonly used in memory circuits to store a single data bit. Then the SR flip-flop actually has three inputs, Set, Reset and its current output Q relating to it’s current state or history.

The term “Flip-flop” relates to the actual operation of the device, as it can be “flipped” into one logic Set state or “flopped” back into the opposing logic Reset state.

Circuit Diagram

**CIRCUIT DIAGRAM**



**SPICE CODE**

|  |
| --- |
| ***\*CMOS Inverter***  **.model mynmos nmos Vto=0.8 Kp=50**  **.model mypmos pmos Vto=-1 Kp=20**  **Mn1 n\_mn1\_drain n\_mn1\_gate 0 0 mynmos w=1u l=1u**  **Mn2 n\_mn1\_drain n\_mn2\_gate 0 0 mynmos w=1u l=1u**  **Mp1 n\_mp1\_drain n\_mn1\_gate n\_mp1\_source n\_mp1\_source mypmos w=1.51u l=1u**  **Mp2 n\_mn1\_drain n\_mn2\_gate n\_mp1\_drain n\_mp1\_source mypmos w=1.51u l=1u**  **Mn3 n\_mn2\_gate n\_mn3\_gate 0 0 mynmos w=1u l=1u**  **Mn4 n\_mn2\_gate n\_mn1\_drain 0 0 mynmos w=1u l=1u**  **Mp3 n\_mp3\_drain n\_mn3\_gate n\_mp1\_source n\_mp1\_source mypmos w=1.51u l=1u**  **Mp4 n\_mn2\_gate n\_mn1\_drain n\_mp3\_drain n\_mp1\_source mypmos w=1.51u l=1u**  **Vdd n\_mp1\_source 0 5**  **Vin1 n\_mn1\_gate 0 0**  **Vin2 n\_mn3\_gate 0 0**  **.tran 1us 10ms**  **.control**  **run**  ***\* plot v(Va)***  **plot v(n\_mn1\_gate)**  **plot v(n\_mn3\_gate)**  **plot v(n\_mn1\_drain)**  **plot v(n\_mn2\_gate)**  **.endc**  **.end** |

**SIMULATION RESULTS**

|  |  |  |  |
| --- | --- | --- | --- |
| S | R | Q | Q’ |
| 0 | 0 | Memory | Memory |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | Race | Race |

**CONCLUSION**