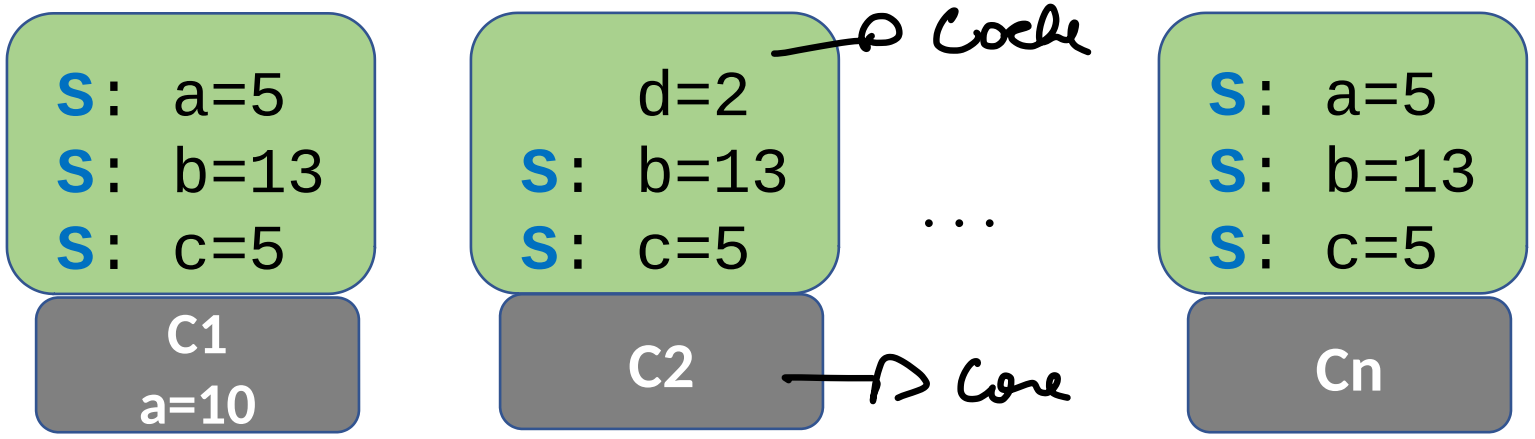
MSI protocols

MSI protocol is a simple cache coherence protocol.
In this protocol, each cache line is labeled with a state:

- **M**: cache block has been modified.
- **S**: other caches may be sharing this block.
- **I**: cache block is invalid

C1 computes new value a=10 in register



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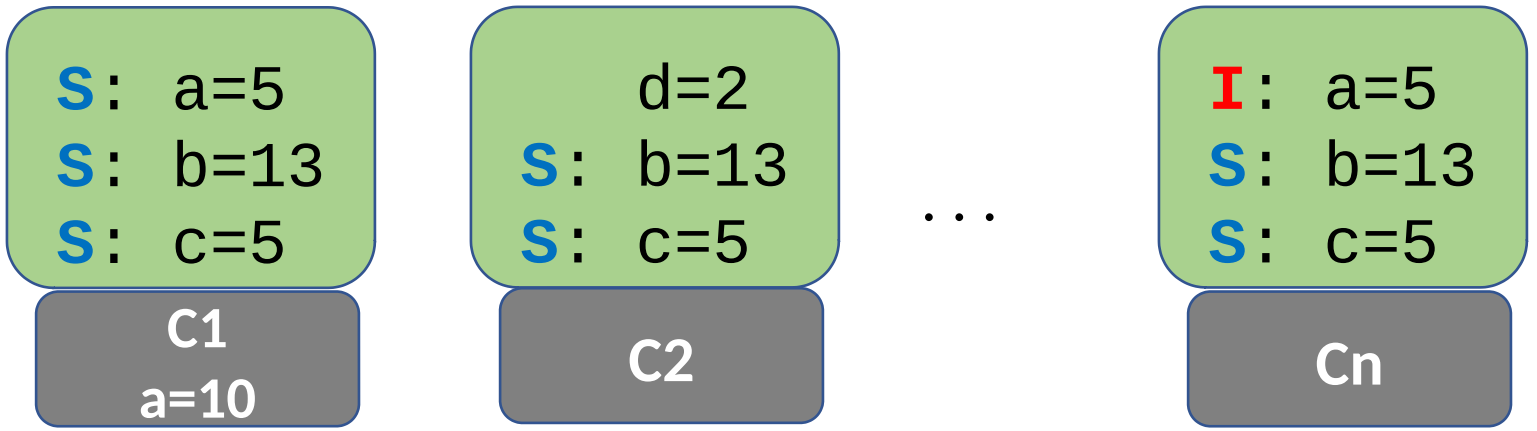
Hardware invalidates all other copies of a



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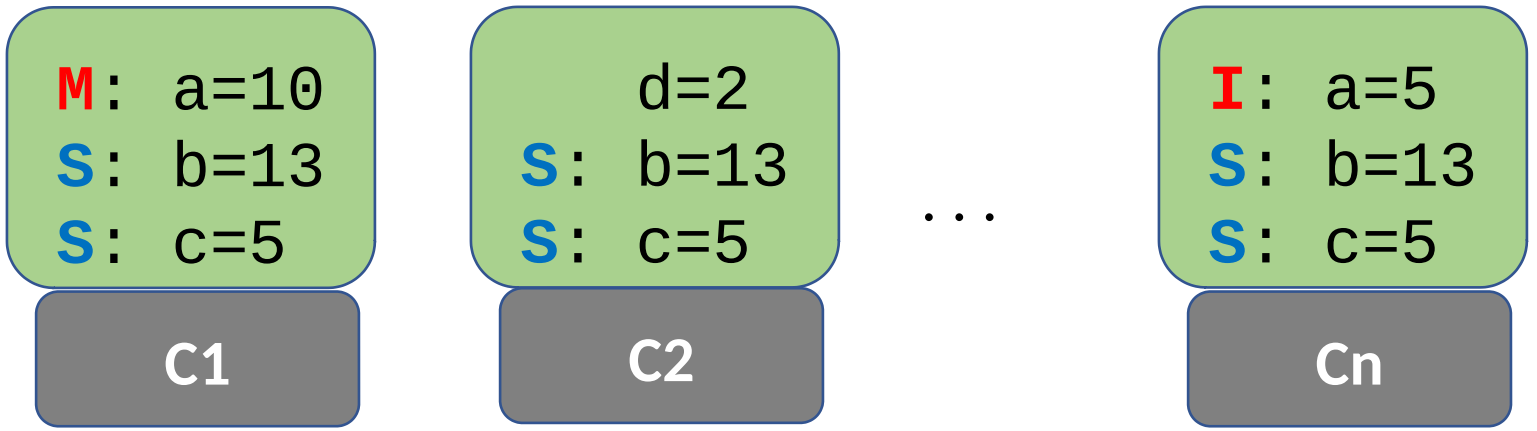
Hardware updates a in cache of C1 and marks it with 'M'



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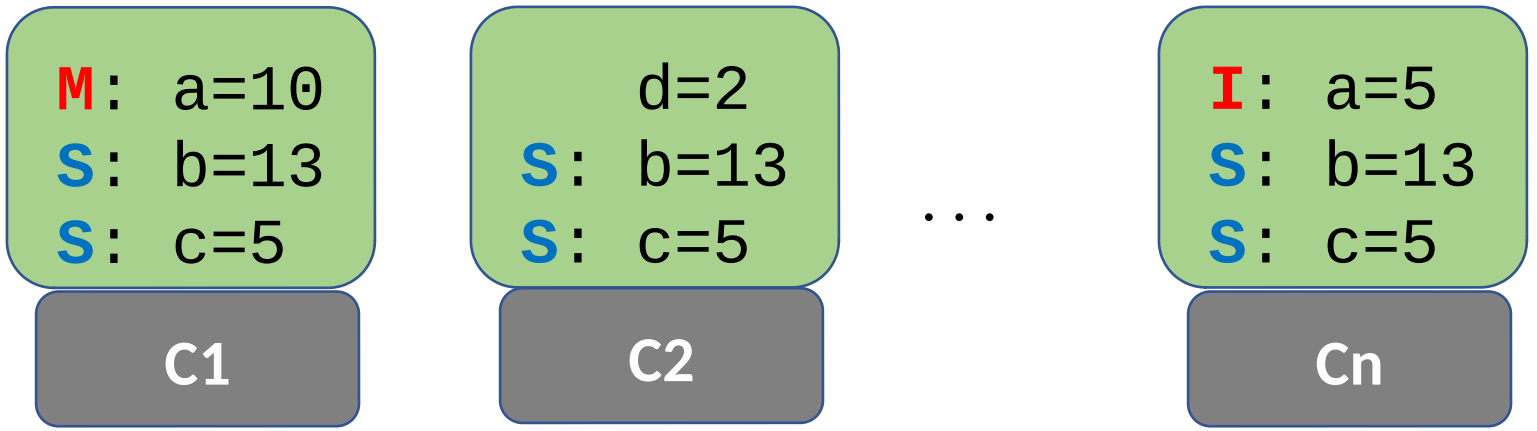
Hardware also updates 'a' in the shared memory



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If Cn wants to load 'a' then 'a' will be brought from the shared memory to the local cache of Cn.