Alarm Clock Implementation using Verilog

Saket Gurjar
International Institute of Information Technology Bangalore
Saket.Gurjar@iiitb.ac.in

***Abstract*—A digital clock with an alarm feature implemented using Verilog is presented in this paper. The clock design can be fully implemented on an FPGA. The module outputs the time in an HH-MM-SS (Hour-Minute-Second) format along with an alarm indicator, which gets set to HIGH when the clock reaches the time set by the user before. A test bench was also made along with the aforementioned. The design was tested on this test bench using Icarus Verilog, and simulated using GTK-Wave.**

I. Introduction

The design is based on a previously developed project [1]. The design consists of a set of inputs and outputs, described in Section II. Section III then talks about the logic through which the inputs are passed, followed by Section IV which discusses the outputs and results obtained.

II. Inputs and Outputs of the Design

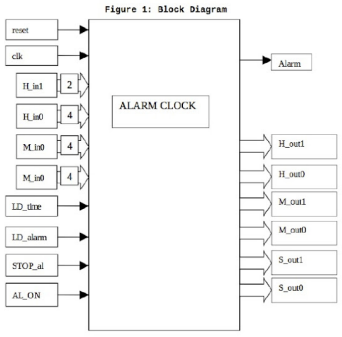

Fig. 1. Pin Layout

A. Inputs

The following input pins were used in the design :

- reset - Active high reset pulse, that sets the current time according to the input time (seconds to 0)and the alarm value to 00.00.00, along with the Alarm output to low. For normal operation, this pin is set to 0.
- clk - A 10Hz input clock. This should be used to generate each real-time second.
- H_{in0}, H_{in1}, M_{in0}, M_{in1} - 4, 2, 4 and 4 bit inputs(respectively), that are used to set the clock time if LD_time is HIGH, set the alarm time if LD_alarm is HIGH.
- LD_time - Active HIGH input which is to set the clock time to the input time when active.
- LD_alarm - Active HIGH input which is to set the alarm time to the input time when active.
- STOP_al - If the Alarm (output) is high, then STOP_al=1 will bring the output back low.
- AL_ON - If high, the alarm is ON

B. Outputs

- Alarm - high if the alarm time equals the current time
- H_{out1}, H_{out0}, M_{out1}, M_{out0}, S_{out1}, S_{out0} - Outputs time in HHMMSS format

III. Alarm Clock Algorithm

Using a 10kHz clock, a one-second clock is generated. This new clock is used to increment the register holding the current times seconds' unit place by 1. After this register reaches 9, the next digit register is incremented and the previous one is reset to 0. After reaching 60 seconds, the seconds are reset to 00 and the minutes' register starts getting incremented. Similarly, the hour registers start getting updated after 60 minutes. An alarm can be set by feeding the alarm time in the time input pins and then setting LD_alarm to HIGH. When the current clock time is equal to the alarm time (if the AL_ON is set to HIGH), the Alarm output pin is set to HIGH. The reset pin when set HIGH, will set the alarm time to 000000, the clock time to the input time, and the alarm output to LOW.

This was tested against a test bench which gave correct outputs for the test cases run against the alarm clock.

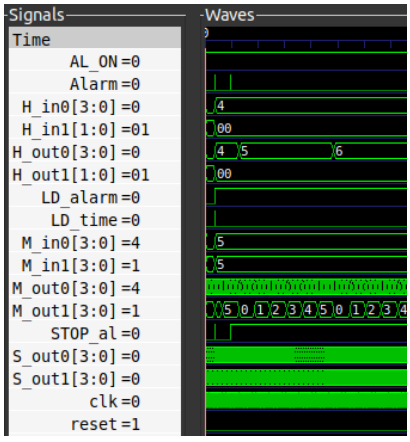

Fig. 2. Results from GTK-Wave

References

[1] Verilog code for Alarm clock on FPGA, fpga4student.com, https://www.fpga4student.com/2016/11/verilog-code-for-alarm-clock-on-fpga.html