Micron & IIITB : Layout automation tool development for Macro Place and Route. Milestone - 1

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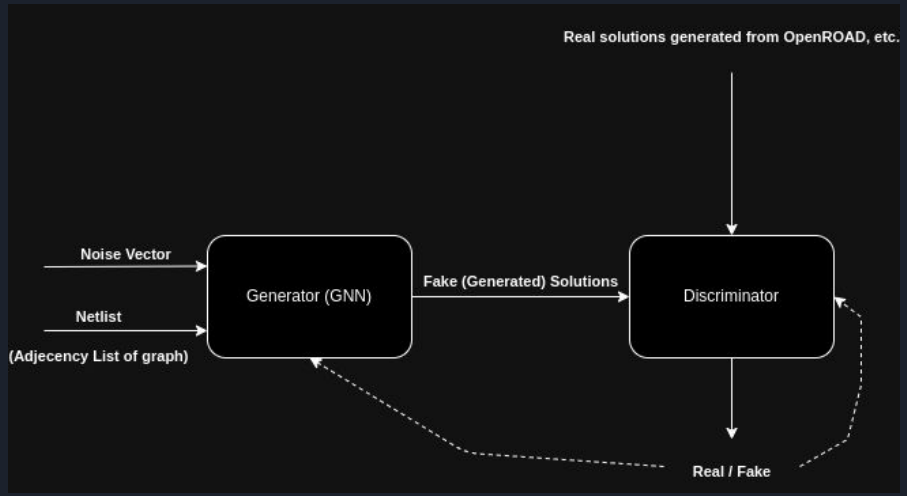
Phase-1 Objectives

- Literature Survey of previous work done regarding usage of ML in Place and Route step.
- Survey of EDA tools to check the degree of customization available in these tools. These include
    - Open Source tools like OpenROAD.
    - Commercial tools like Cadence Innovus.
- These tools will be used for generation of the dataset later.
- Study of current optimization techniques/algorithms used in these tools.
    - Algorithms like MOBO, Pymoo etc.

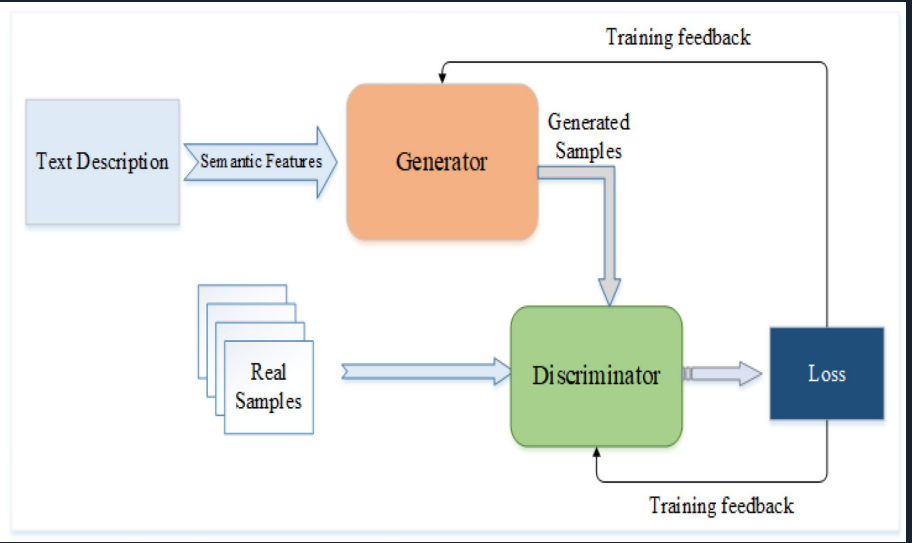
Phase-1 Objectives

- Review of various ML models that could be used in context of this problem.
    - Eg. Graph-based GAN model

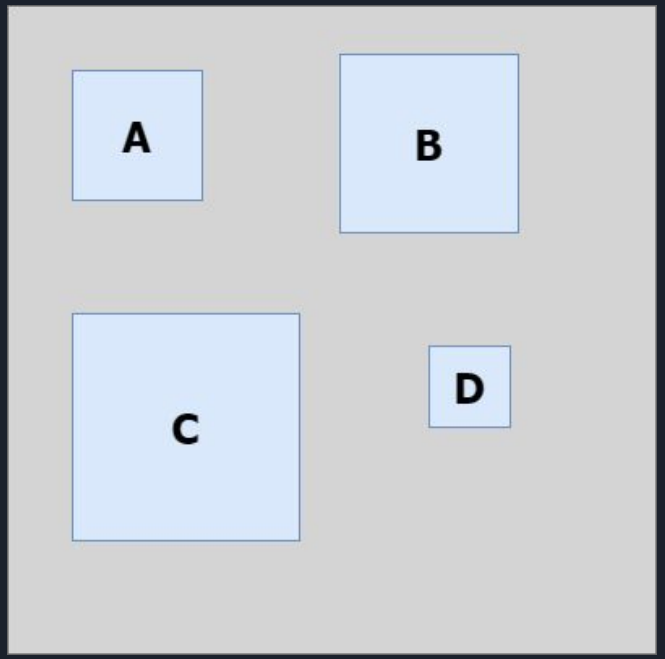


Phase-1 Objectives

- Model Architecture can be made similar to text-to-image models.
- Embedding netlist graph in a vector space instead of embedding text into word-embeddings
- Aim to generate post-routing results instead of an image.



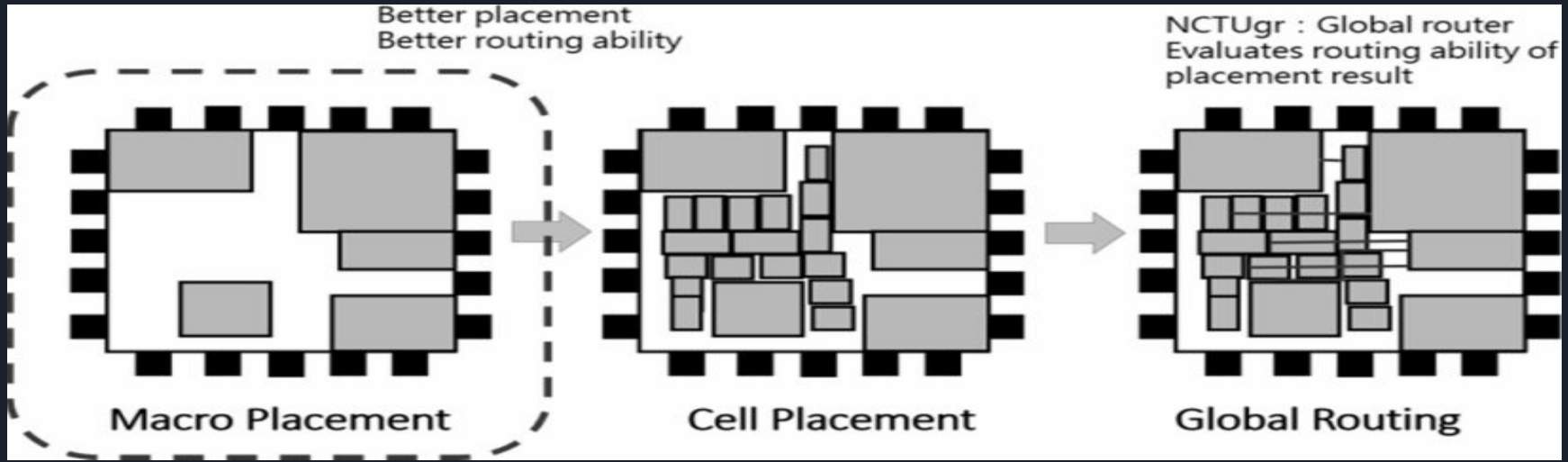
Phase-1 Objectives



- **Dataset Generation:**
  - For a fixed model (netlist), manual changes to the placement by adding noise to the positions of each macro.
  - This can be passed to EDA flows to get hardware performance metrics which can be used as loss parameters.

Queries:-

- Macro placement happens at Floorplan stage of the ASIC flow. So what's the exact motive of the Macro place and route tool.
- Require more inputs regarding the nature of the macro placements like abutted or non-abutted.
- Are we dealing only with the macros or with the standard cells too.



Few References of DEF files

ISPD conference competition - https://drive.google.com/file/d/111_a2kObt3tcjj1IQFXMCNCpQwPyBlZs/view

Few DEF files - https://drive.google.com/drive/folders/1C7fgNoBJZJMs6bE99nA3XHiHNHTtVrJV