International Institute of Information Technology Bangalore

Micron – IIITB Presentation

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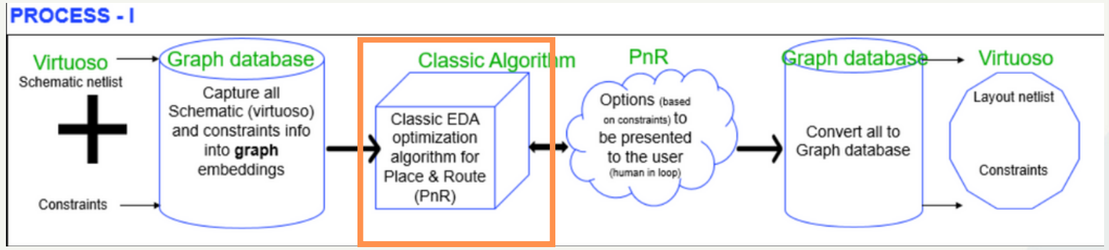
Agenda

- Genetic Algorithm for Placement
- Align Tool

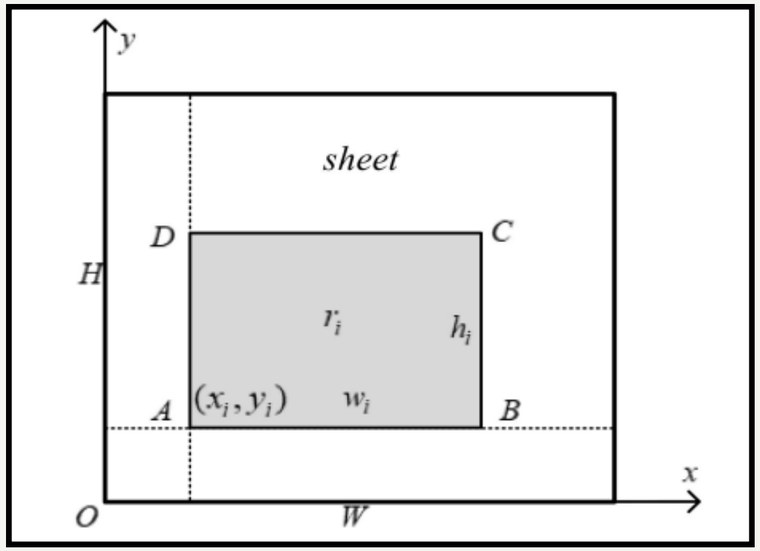
Placement Algorithms



- **Placement Algorithms classified as either :**
  - **Constructive Algorithms:** Each module is placed individually.
  - **Iterative Algorithms:** All modules are placed at once and the positions are improved in every iteration.

Macro Placement using GA

- Problem is similar to 2D-Rectangular Packing Problem, with a difference in the objective functions.
  - Problem definition:
    - Given set of n rectangles and their widths and heights, find out the coordinates of these rectangles such that there is no overlap and a function F is maximised.



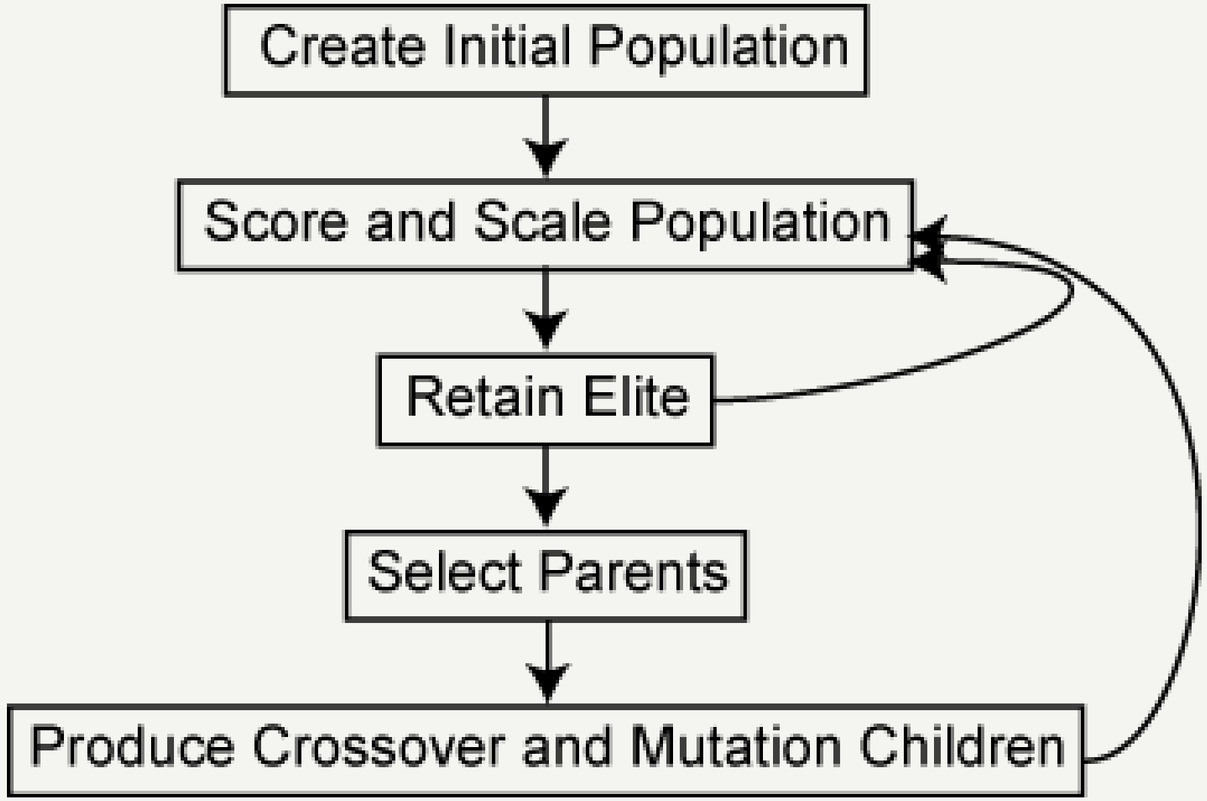
https://www.mdpi.com/2076-3417/11/1/413

Macro Placement using GA

- Function F changes in our case.
  - For now, negative of HPWL taken as F
- Overall objective function is :
  - F(X) = - HPWL(X) - (K * OverlapArea(X))
  - We aim to maximise this function F(X)

https://ieeexplore.ieee.org/document/7033338

Macro Placement using GA

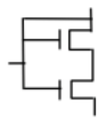
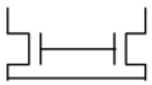
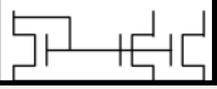


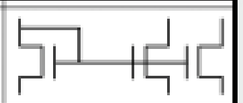
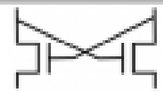
Macro Placement using GA

- Genetic Algorithm defines a population of individuals with a set of genes.
  - X = [x1 , y1 , x2 , y2 , x3 , y3 ,...]
- Genes are randomly initialised, and the population is sorted according to the values of objective function F(X).
- Best k individuals are selected for crossover.
- New individuals have randomly picked genes from one of the best k individuals from previous generation.
- Slight mutation applied to genes at every generation.

Primitive Circuitry

- These circuits will now form the basic macros around which the bigger circuits develop
- Each primitive consists of a small number of transistor or passive units, however, each such unit may consist of multiple replicated structures, such as multi-fin / multi-finger transistors, or resistive/capacitive arrays.

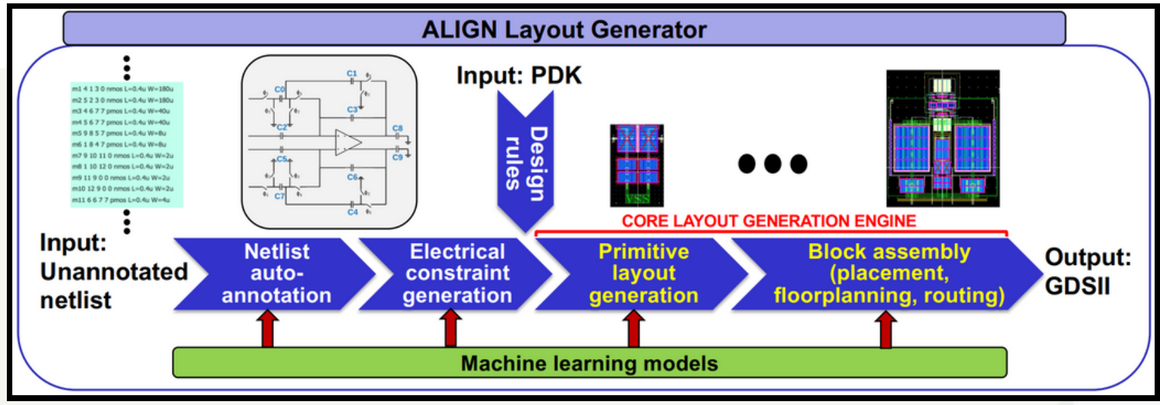
Capacitor array		Voltage reference	
Switch		Level shifter	
Diode-connected load		Current mirror load	
Differential pair		Current mirror bank	

Cross-coupled pair 1		Level shifter bank	
Cross-coupled pair 2		Dummy 1	
Differential load		Dummy 2	
Cascode pair		Decap	

ALIGN tool

- The ALIGN tool rightly suits the problem statement where smaller blocks can be used as macros to build circuitry and follow a hierarchical way of placement and routing.
- The ALIGN Public repository provides 1390 OTA (Operational transconductance amplifiers). These OTA(s) are primarily used in analog signal processing applications, such as filters, oscillators, and voltage-controlled amplifiers.
- Constraints used here talk about Geometric constraints (Related to the placing of MACROs) and the Electric constraints talk about the change in wire properties for longer connections. Hence following the shortest path wherever possible

Constraints Generation



- During the first step, the input spice file is auto-annotated on a hierarchical basis. This is a key step that is used to build the layout of the circuit hierarchically.
- Once the PDKs are added and the netlist is annotated as per ALIGN, the electrical constraints are identified and transformed into Geometric constraints to be implemented during layout.
- These include the maximum permissible wire length, and for the layout, common centroid-based placement.
- The auto-annotation step recognizes known blocks or array structures, it associates geometric requirements with these blocks, such as symmetry, matching, and common-centroid constraints

Compatibilty with current progress

- In the current progress, we were exploring ways of generating spice netlists as inputs to the flow so that dummy MACROs could be added for testing.
- The ALIGN Public dataset provides a wide variety of basic Analog circuits in the same initial format.
- The parser needs to be modified a little so that this forms a bridge between the dataset and the Genetic algorithm described before.

```
.OPTION INGOLD=2 ARTIST=2 PSF=2 MEASOUT=1 PARHIER=LOCAL PROBE=0 M

i4 vdd! id DC=200e-6
c2 voutp 0 357e-15
m17 net16 vinn net24 0 nmos w=27e-9 l=20e-9 nfin=28
m16 net24 id 0 0 nmos w=27e-9 l=20e-9 nfin=10
m15 net27 vinp net24 0 nmos w=27e-9 l=20e-9 nfin=28
m14 id id 0 0 nmos w=27e-9 l=20e-9 nfin=10
m11 vbiasnd vbiasnd 0 0 nmos w=27e-9 l=20e-9 nfin=24
m10 voutp vbiasnd 0 0 nmos w=27e-9 l=20e-9 nfin=24
v3 vdd! 0 DC=0.8
v4 vinn 0 DC=0.7 AC 500e-3
v5 vinp 0 DC=0.7 AC 500e-3 180
m21 net16 net16 vdd! vdd! pmos w=27e-9 l=20e-9 nfin=60
m20 m20stack net16 vdd! vdd! pmos w=27e-9 l=20e-9 nfin=240
m20s vbiasnd net16 m20stack vdd! pmos w=27e-9 l=20e-9 nfin=240
m19 net27 net27 vdd! vdd! pmos w=27e-9 l=20e-9 nfin=60
m18 m18stack net27 vdd! vdd! pmos w=27e-9 l=20e-9 nfin=240
m18s voutp net27 m18stack vdd! pmos w=27e-9 l=20e-9 nfin=240
.END
```

Summary of overall Progress

- A new script was developed for the Genetic Algorithm for the placement of MACROs based on Half Perimeter Wire Length.
- Explored ALIGN tool functionality and circuit databases

Any specific request to Micron

Feedback on current implementation