第四届全国大学生嵌入式芯片与系统设计竞赛

芯片设计赛道

芯片设计验证报告

作品名称（必填）：基于智能计算的图像识别系统

队伍编号（必填）：1377

参赛队名（必填）：chenbochenbochen

日期：2021 年 10 月 7 日

1. 测试点列表

简要说明测试点分解策略

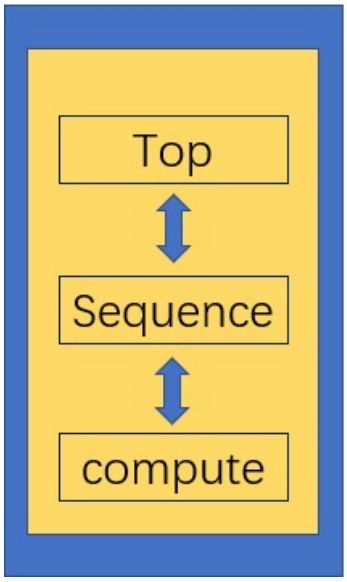
测试点名称	覆盖范围	覆盖方式
功能类: Call LdAdd Excute MACC MACCZ MAX MMAXN MMAXZ MNIST ReLU Store	典型值	coverage
	边界值	coverage
	异常值	directtest
	Cross	coverage
接口类:		
场景类（选填，有可以填）		
性能类（选填，有可以填）		
异常类（选填，有可以填）		

2. 验证方案

主要验证组件

组件名	功能描述
Sequence	发射指令并处理跳转指令
Compute	对数据进行计算处理返回结果
Top	接受外部的 io 指令

验证方案：框图+说明



根据框图简要说明验证方案的流程

首先将 testcase 通过编译汇编指令为 hex 文件，通过对 top_moudule 施加 testbench 后，top 进行状态跳转让 sequence 发射指令至 compute 进行运算，运算成功后将结果写回存储，然后对比行为模型的存储和过程的 trace 即可。

3. 功能覆盖率分析

覆盖率结果（截图）

```
test:
    @cd $(SRC_PATH)/asm && make mlasm;
    @cd $(SRC_PATH)/sim && make mlsim;
    @for subdir in $(SUBDIR); \
        do \
        echo making in $$subdir; \
        cd $$subdir&& $(SRC_PATH)/asm/mlasm -v -o demo.hex -b demo.bin demo.asm  \
        && cp -f -r demo.hex $(SRC_PATH)/Runing \
        && $(SRC_PATH)/sim/mlsim -v -t demo.trace -o demo_out.hex -b demo_out.bin $$subdir/demo.bin \
        && cp -f -r demo_out.hex  $(SRC_PATH)/Runing;\
        cd $(SRC_PATH)/rtl && iverilog -DTRACE  -s testbench -o testbench testbench.v top.v memory.v sequencer.v compute.v; \
        cd $$subdir && rm -f testbench.log \
        && vvp -N $(SRC_PATH)/rtl/testbench>>testbench.log \
        && sed '/^TRACE/ ! d; s/^[^:]*: //;' < testbench.log > testbench.trace \
        && cmp demo.trace testbench.trace\
        && echo ~~~~~~~~~~~~~~~~~~~~~~~~PASS~~~~~~~~~~~~~~~~~~~~~~~~;\
    done
```

```
making in /mnt/c/Users/zhangyang/Desktop/design_2021/accelerator/testcase/Excute
symbol LdAddtestbegin at 144 (0x00090).
symbol LdAddtestend at 172 (0x000ac).
symbol MACCtestbegin at 104 (0x00068).
symbol MACCtestend at 124 (0x0007c).
symbol MMAXtestbegin at 124 (0x0007c).
symbol MMAXtestend at 144 (0x00090).
symbol coeff at 7156 (0x01bf4).
symbol indata at 332 (0x0014c).
symbol middata at 114688 (0x1c000).
symbol outdata at 118784 (0x1d000).
symbol run_32b_multi_10_begin at 292 (0x00124).
symbol run_32b_multi_10_end at 332 (0x0014c).
symbol run_multiply_10time_begin at 172 (0x000ac).
symbol run_multiply_10time_end at 292 (0x00124).
new hex file section at 0x00000.
writing 19300 bytes bin file.
read 19300 bytes from bin file.
load 66978824 16646917 from 332 336 save:acc0:66979894 at 118784
save:acc1:16646903 at 118788
save:acc0:66980964 at 118792
save:acc1:16646889 at 118796
digit:8
simulation finished.
est 1091 cycles, avg 0.234647 ops/cycle, 1.5% utilization
new hex file section at 0x1d000.
writing 128 kB bin file.
~~~~~~~~~~~~~~~~~~~~~~PASS~~~~~~~~~~~~~~~~~~~~~~~~~~
```

```
making in /mnt/c/Users/zhangyang/Desktop/design_2021/accelerator/testcase/LdAdd
symbol LdAdd_test at 152 (0x00098).
symbol LdAdd_test_10 at 108 (0x0006c).
symbol coeff at 7148 (0x01bec).
symbol indata at 324 (0x00144).
symbol middata at 114688 (0x1c000).
symbol outdata at 118784 (0x1d000).
symbol run_32b_multi_10_begin at 284 (0x0011c).
symbol run_32b_multi_10_end at 324 (0x00144).
symbol run_multiply_10time_begin at 164 (0x000a4).
symbol run_multiply_10time_end at 284 (0x0011c).
new hex file section at 0x00000.
writing 18908 bytes bin file.
read 18908 bytes from bin file.
load 66978824 16646917 from 324 328 save:acc0:133957648 at 118784
save:acc1:33293834 at 118788
save:acc0:-117508085 at 118792
save:acc1:116855814 at 118796
save:acc0:337519407 at 118800
save:acc1:941635581 at 118804
save:acc0:-418082528 at 118808
save:acc1:-1902749644 at 118812
digit:0
simulation finished.
est 275 cycles, avg 0.000000 ops/cycle, 0.0% utilization
new hex file section at 0x1d000.
writing 128 kB bin file.
~~~~~~~~~~~~~~~~~~~~~~PASS~~~~~~~~~~~~~~~~~~~~~~~~~~
```

```
making in /mnt/c/Users/zhangyang/Desktop/design_2021/accelerator/testcase/MACC
symbol MACC_test at 176 (0x000b0).
symbol MACC_test_10 at 136 (0x00088).
symbol coeff at 7284 (0x01c74).
symbol indata at 460 (0x001cc).
symbol middata at 114688 (0x1c000).
symbol outdata at 118784 (0x1d000).
symbol run_32b_multi_10_begin at 420 (0x001a4).
symbol run_32b_multi_10_end at 460 (0x001cc).
symbol run_multiply_10time_begin at 300 (0x0012c).
symbol run_multiply_10time_end at 420 (0x001a4).
new hex file section at 0x00000.
writing 19428 bytes bin file.
read 19428 bytes from bin file.
load 9830404 950279 from 0 4 save:acc0:9833060 at 118784
save:acc1:950603 at 118788
save:acc0:9888285 at 118792
save:acc1:967367 at 118796
save:acc0:9956786 at 118800
save:acc1:960957 at 118804
digit:0
simulation finished.
est 2258 cycles, avg 2.834367 ops/cycle, 17.7% utilization
new hex file section at 0x1d000.
writing 128 kB bin file.
~~~~~~~~~~~~~~~~~~~~~~~~PASS~~~~~~~~~~~~~~~~~~~~~~~~~~
```

```
making in /mnt/c/Users/zhangyang/Desktop/design_2021/accelerator/testcase/MACCZ
symbol MACCZ_test at 184 (0x000b8).
symbol MACCZ_test_10 at 140 (0x0008c).
symbol coeff at 7184 (0x01c10).
symbol indata at 360 (0x00168).
symbol middata at 114688 (0x1c000).
symbol outdata at 118784 (0x1d000).
symbol run_32b_multi_10_begin at 320 (0x00140).
symbol run_32b_multi_10_end at 360 (0x00168).
symbol run_multiply_10time_begin at 200 (0x000c8).
symbol run_multiply_10time_end at 320 (0x00140).
new hex file section at 0x00000.
writing 19328 bytes bin file.
read 19328 bytes from bin file.
load 6553604 950279 from 0 4 save:acc0:131 at 118784
save:acc1:-12 at 118788
save:acc0:191 at 118792
save:acc1:-25 at 118796
save:acc0:231 at 118800
save:acc1:169 at 118804
digit:1
simulation finished.
est 1215 cycles, avg 0.684774 ops/cycle, 4.3% utilization
new hex file section at 0x1d000.
writing 128 kB bin file.
~~~~~~~~~~~~~~~~~~~~~~~~PASS~~~~~~~~~~~~~~~~~~~~~~~~~~
```

```
making in /mnt/c/Users/zhangyang/Desktop/design_2021/accelerator/testcase/MAX
symbol Max_test at 152 (0x00098).
symbol Max_test_10 at 108 (0x0006c).
symbol coeff at 7260 (0x01c5c).
symbol indata at 436 (0x001b4).
symbol middata at 114688 (0x1c000).
symbol outdata at 118784 (0x1d000).
symbol run_32b_multi_10_begin at 396 (0x0018c).
symbol run_32b_multi_10_end at 436 (0x001b4).
symbol run_multiply_10time_begin at 276 (0x00114).
symbol run_multiply_10time_end at 396 (0x0018c).
new hex file section at 0x00000.
writing 19020 bytes bin file.
read 19020 bytes from bin file.
load 9043972 950279 from 0 4 save:acc0:9043972 at 114688
save:acc1:950603 at 114692
save:acc0:9043972 at 114696
save:acc1:963915 at 114700
save:acc0:9043972 at 114704
save:acc1:981238 at 114708
digit:0
simulation finished.
est 2468 cycles, avg 3.047002 ops/cycle, 19.0% utilization
new hex file section at 0x1c000.
writing 128 kB bin file.
~~~~~~~~~~~~~~~~~~~~~~~~PASS~~~~~~~~~~~~~~~~~~~~~~~~~~~~
```

```
making in /mnt/c/Users/zhangyang/Desktop/design_2021/accelerator/testcase/MMAXN
symbol Maxn_test at 152 (0x00098).
symbol Maxn_test_10 at 108 (0x0006c).
symbol coeff at 7260 (0x01c5c).
symbol indata at 436 (0x001b4).
symbol middata at 114688 (0x1c000).
symbol outdata at 118784 (0x1d000).
symbol run_32b_multi_10_begin at 396 (0x0018c).
symbol run_32b_multi_10_end at 436 (0x001b4).
symbol run_multiply_10time_begin at 276 (0x00114).
symbol run_multiply_10time_end at 396 (0x0018c).
new hex file section at 0x00000.
writing 19020 bytes bin file.
read 19020 bytes from bin file.
load 9043972 950279 from 0 4 save:acc0:13 at 114688
save:acc1:16 at 114692
save:acc0:13 at 114696
save:acc1:27 at 114700
save:acc0:17 at 114704
save:acc1:659 at 114708
digit:0
simulation finished.
est 2468 cycles, avg 3.047002 ops/cycle, 19.0% utilization
new hex file section at 0x1c000.
writing 128 kB bin file.
~~~~~~~~~~~~~~~~~~~~~~~~PASS~~~~~~~~~~~~~~~~~~~~~~~~~~~~
```

```
making in /mnt/c/Users/zhangyang/Desktop/design_2021/accelerator/testcase/MMAXZ
symbol Maxz_test at 152 (0x00098).
symbol Maxz_test_10 at 108 (0x0006c).
symbol coeff at 7260 (0x01c5c).
symbol indata at 436 (0x001b4).
symbol middata at 114688 (0x1c000).
symbol outdata at 118784 (0x1d000).
symbol run_32b_multi_10_begin at 396 (0x0018c).
symbol run_32b_multi_10_end at 436 (0x001b4).
symbol run_multiply_10time_begin at 276 (0x00114).
symbol run_multiply_10time_end at 396 (0x0018c).
new hex file section at 0x00000.
writing 19020 bytes bin file.
read 19020 bytes from bin file.
load 9043972 950279 from 0 4 save:acc0:13 at 114688
save:acc1:16 at 114692
save:acc0:13 at 114696
save:acc1:27 at 114700
save:acc0:17 at 114704
save:acc1:659 at 114708
digit:0
simulation finished.
est 2468 cycles, avg 3.047002 ops/cycle, 19.0% utilization
new hex file section at 0x1c000.
writing 128 kB bin file.
~~~~~~~~~~~~~~~~~~~~~~~~PASS~~~~~~~~~~~~~~~~~~~~~~~~~~~
```

```
making in /mnt/c/Users/zhangyang/Desktop/design_2021/accelerator/testcase/MNIST
symbol coeff at 2680 (0x00a78).
symbol indata at 1896 (0x00768).
symbol middata at 114688 (0x1c000).
symbol outcoeff at 1736 (0x006c8).
symbol outdata at 118784 (0x1d000).
symbol run_32b_multi_10_begin at 1696 (0x006a0).
symbol run_32b_multi_10_end at 1736 (0x006c8).
symbol run_multiply_10time_begin at 1576 (0x00628).
symbol run_multiply_10time_end at 1696 (0x006a0).
new hex file section at 0x00000.
writing 117272 bytes bin file.
read 117272 bytes from bin file.
load -38459 208226 from 114688 114692 load 75861 26254 from 114696 114700 load 97900 -12628 from 11470
4 114708 load 95592 96909 from 114712 114716 load -44008 6834 from 114720 114724 load 18049 -12793 fro
m 114728 114732 load 44191 46652 from 114736 114740 load 61759 46652 from 114744 114748 load 101 -2783
 from 118784 118788 load 1343 1614 from 118792 118796 load -1989 -593 from 118800 118804 load -3456 44
74 from 118808 118812 load -204 1860 from 118816 118820 digit:7
simulation finished.
est 4913 cycles, avg 2.585793 ops/cycle, 16.2% utilization
new hex file section at 0x1c000.
new hex file section at 0x1d000.
writing 128 kB bin file.
~~~~~~~~~~~~~~~~~~~~~~~~PASS~~~~~~~~~~~~~~~~~~~~~~~~~~~
```

```
making in /mnt/c/Users/zhangyang/Desktop/design_2021/accelerator/testcase/ReLU
symbol ReLU_test1 at 128 (0x00080).
symbol ReLU_test10 at 308 (0x00134).
symbol ReLU_test2 at 148 (0x00094).
symbol ReLU_test3 at 168 (0x000a8).
symbol ReLU_test4 at 188 (0x000bc).
symbol ReLU_test5 at 208 (0x000d0).
symbol ReLU_test6 at 228 (0x000e4).
symbol ReLU_test7 at 248 (0x000f8).
symbol ReLU_test8 at 268 (0x0010c).
symbol ReLU_test9 at 288 (0x00120).
symbol ReLU_test_10 at 84 (0x00054).
symbol coeff at 7312 (0x01c90).
symbol indata at 488 (0x001e8).
symbol middata at 114688 (0x1c000).
symbol outdata at 118784 (0x1d000).
symbol run_32b_multi_10_begin at 448 (0x001c0).
symbol run_32b_multi_10_end at 488 (0x001e8).
symbol run_multiply_10time_begin at 328 (0x00148).
symbol run_multiply_10time_end at 448 (0x001c0).
new hex file section at 0x00000.
writing 19072 bytes bin file.
read 19072 bytes from bin file.
load 66978824 16646917 from 488 492 load -33685768 67110137 from 496 500 load -83953657 100927744 from 504 508 load -133826308 -8447
5901 from 512 516 load -50659068 33880313 from 520 524 load -50134008 -100203003 from 528 532 load 134350848 67434757 from 536 540 l
oad -100990214 67502840 from 544 548 load 150863882 67241994 from 552 556 load 218892037 67700221 from 560 564 load 17234953 1171151
28 from 568 572 load 100727802 184746238 from 576 580 load 84413956 302255109 from 584 588 load -49672696 17106170 from 592 596 load
 134740218 134873860 from 600 604 load -100794361 84146696 from 608 612 load 185140480 -33354493 from 616 620 load -49743610 -101054
472 from 624 628 load -33293051 -151320569 from 632 636 load 67304196 168100342 from 640 644 load -32835318 50526725 from 648 652 lo
ad 117112070 -16517638 from 656 660 load -185666058 202111740 from 664 668 load -33489140 -117704966 from 672 676 load -16582146 836
88456 from 680 684 load -218758662 -286855451 from 688 692 load 605555705 -268698605 from 696 700 load -34080535 133759734 from 704
708 load -134611719 -470615052 from 712 716 load -168694554 152440823 from 720 724 load -353636360 -320083743 from 728 732 load 6691
1988 -117964804 from 736 740 load -101978884 -394506 from 744 748 load -117900551 -321068830 from 752 756 load -304224479 -33816844
from 760 764 load -100727294 134020844 from 768 772 load 84082432 -286003191 from 776 780 load -404429849 -319494422 from 784 788 lo
ad -84412675 -151258622 from 792 796 load 84016631 -16575990 from 800 804 load -117965316 49674749 from 808 812 load 15991800 167761
91 from 816 820 load -218824197 253099266 from 824 828 load 352851980 554833421 from 832 836 load 118295314 252382732 from 840 844 l
oad 116918009 -67634689 from 848 852 load 320277768 437525010 from 856 860 load 841425441 186128678 from 864 868 load 252121103 -165
81634 from 872 876 load -66713603 337645063 from 880 884 load 488314135 690233897 from 888 892 load 151066911 -16252927 from 896 900
 load 133497594 -184222461 from 904 908 load 436799744 404557594 from 912 916 load 353837074 -235403493 from 920 924 load -17105675
-133955588 from 928 932 load 17172734 184943874 from 936 940 load 488508171 236130836 from 944 948 load -34209265 -100992010 from 95
2 956 load -84474635 -83822599 from 960 964 load 234025967 186454536 from 968 972 load 201983748 -83822589 from 976 980 load -172344
35 -84412677 from 984 988 load -16385288 15333625 from 992 996 load 286327552 251529727 from 1000 1004 load 100993795 -66782198 from
 1008 1012 load -50723335 100530688 from 1016 1020 load -185995017 184222198 from 1024 1028 load 235338235 420942101 from 1032 1036
load -83948279 83885570 from 1040 1044 load -117375738 -268897543 from 1048 1052 load 66715115 487657225 from 1056 1060 load 3037660
38 -33619705 from 1064 1068 load 33622013 -16974074 from 1072 1076 load -135332871 -101057546 from 1080 1084 load 437585423 68095252
 from 1088 1092 load -50465267 -83884040 from 1096 1100 load 150796793 -67764986 from 1104 1108 load -34342669 -117311746 from 1112
1116 load -32700926 50856712 from 1120 1124 load 67368950 67369222 from 1128 1132 load -67239171 -235930887 from 1136 1140 load -353
897488 -16252425 from 1144 1148 load -66911996 83822337 from 1152 1156 load -83491323 -196344 from 1160 1164 load -184089090 -135269
385 from 1168 1172 load 17627896 151389958 from 1176 1180 load 261379 151521025 from 1184 1188 load -33815042 -167970306 from 1192 1
196 load -84279809 101317117 from 1200 1204 digit:0
simulation finished.
est 1414 cycles, avg 0.000000 ops/cycle, 0.0% utilization
new hex file section at 0x1d000.
writing 128 kB bin file.
~~~~~~~~~~~~~~~~~~~~~~~~PASS~~~~~~~~~~~~~~~~~~~~~~~~~~~~
```

结果分析（重点分析没有覆盖的部分）

大部分指令在正常执行时都可以覆盖到，未覆盖的部分有以下情况：

Excute 指令：在 LEN 为 0 时会导致计数器的溢出，执行会发生停止

计算指令：在未初始化时累加器会出现未知态，必须使用初始化指令首先进行计算，否则会出现未知态。

Load 指令后的四个周期内目标存储处于亚稳态，无法进行访问，否则会出现未知结果。

Call 指令的最大深度只有 256，超过该深度时，返回后无法执行下一条语句。

4. 代码覆盖率分析

覆盖率结果（截图）

SYNOPSYS

Design Module List

dashboard | hierarchy | modlist | groups | tests | asserts

Expand All | Collapse All

NAME	SCORE	LINE	COND	TOGGLE	FSM	BRANCH
testbench	78.26	87.94		89.71		57.14
sequencer	83.17			83.17		
mem512x64	87.29	100.00		95.21		66.67
mem512x32	89.02	100.00		67.07		100.00
top	94.65	97.12	92.11	95.09		94.29
Compute	95.79	94.82	98.67	94.70		94.97
Sequencer	97.47	100.00	100.00	89.87		100.00
compute	99.74			99.74		
marlann_memory	99.85	100.00		99.69		
spsram8192161782	100.00	100.00	100.00	100.00		100.00
memory_spram	100.00	100.00	100.00	100.00		100.00
Mul8X8	100.00	100.00		100.00		

结果分析（重点分析没有覆盖的部分）

尝试分析没有覆盖部分产生的原因，以及在未来有何策略上的改进

Sequence：

Reset：缺少从 0=>1,因为软件指令不控制 Reset 信号

Addr：程序开始地址，因为 testbench 固定执行地址为 0，所以 addr 的值总是为 0

Smem_addr[0]:每条指令是 32bit 即四字节，Smem_addr[0]是地址的倒数第二位，所以总是为 0

5. 条件覆盖率分析

覆盖率结果（截图）

SYNOPSYS

Design Module List

dashboard | hierarchy | modlist | groups | tests | asserts

Expand All | Collapse All

NAME	SCORE	LINE	COND	TOGGLE	FSM	BRANCH
testbench	78.26	87.94		89.71		57.14
sequencer	83.17			83.17		
mem512x64	87.29	100.00		95.21		66.67
mem512x32	89.02	100.00		67.07		100.00
top	94.65	97.12	92.11	95.09		94.29
Compute	95.79	94.82	98.67	94.70		94.97
Sequencer	97.47	100.00	100.00	89.87		100.00
compute	99.74			99.74		
marlann_memory	99.85	100.00		99.69		
spsram8192161782	100.00	100.00	100.00	100.00		100.00
memory_spram	100.00	100.00	100.00	100.00		100.00
Mul8X8	100.00	100.00		100.00		

结果分析（重点分析没有覆盖的部分）

尝试分析没有覆盖部分产生的原因，以及在未来有何策略上的改进

Top：

```
LINE       183
EXPRESSION (busy_q || seq_busy || comp_busy)
            ---1--    ----2---    ----3----
```

-1-	-2-	-3-	Status
0	0	0	Covered
0	0	1	Not Covered
0	1	0	Covered
1	0	0	Covered

逻辑不发生

```
LINE       95
EXPRESSION ((state_wait == 1'b1) && qmem_done && ((|wstrb)))
            ----------1---------    ----2----    -----3----
```

-1-	-2-	-3-	Status
0	1	1	Not Covered
1	0	1	Covered
1	1	0	Covered
1	1	1	Covered

State_wait：不可能为 0，因为这个信号代表请求

6. 用例激励随机性分析

我们采用 NIST 进行对数据的随机性检验，共包含以下 16 个方面：

1) 频率检验（Frequency Test）
2) 块内频数检验（Frequency Test within a Block）
3) 游程检验（Runs Test）
4) 块内最长游程检验（Test for the Longest Run of Ones in a Block）
5) 二元矩阵秩检验（Binary Matrix Rank Test）
6) 离散傅里叶变换检验（Discrete Fourier Transform (Spectral) Test）
7) 非重叠模块匹配检验（Non-overlapping Template Matching Test）
8) 重叠模块匹配检验（Overlapping Template Matching Test）
9) Maurer 的通用统计检验（Maurer's “Universal Statistical” Test）
10) Lempel-Ziv 压缩检验（Lempel-Ziv Compression Test）
11) 线性复杂度检验（Linear Complexity Test）
12) 序列检验（Serial Test）
13) 近似熵检验（Approximate Entropy Test）
14) 累加和检验（Cumulative Sums (Cusum) Test）
15) 随机游动检验（Random Excursions Test）

16) 随机游动状态频数检验（Random Excursions Variant Test）

检验报告如下:

C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 P-VALUE PROPORTION STATISTICAL TEST

---

1 4 5 1 6 3 0 6 0 4 0.054199 30/30 Frequency

3 2 4 5 2 0 5 4 5 0 0.253551 30/30 BlockFrequency

2 4 5 4 0 1 3 2 6 3 0.350485 30/30 CumulativeSums

0 2 9 1 4 1 8 0 3 2 0.000439 30/30 CumulativeSums

1 4 2 1 0 2 2 7 5 6 0.054199 30/30 Runs

5 1 1 5 4 4 3 1 2 4 0.534146 30/30 LongestRun

2 4 4 7 0 1 1 5 4 2 0.122325 30/30 Rank

16 4 2 2 4 1 0 0 1 0 0.000000 * 24/30 * FFT

3 3 1 6 4 1 3 3 2 4 0.671779 30/30 NonOverlappingTemplate

8 2 1 3 3 3 2 3 1 4 0.213309 29/30 NonOverlappingTemplate

1 1 2 7 1 5 3 5 3 2 0.178278 30/30 NonOverlappingTemplate

7 3 2 4 4 4 1 3 1 1 0.299251 27/30 * NonOverlappingTemplate

3 2 3 2 0 1 4 6 5 4 0.350485 30/30 NonOverlappingTemplate

4 3 2 5 3 2 3 3 3 2 0.976060 30/30 NonOverlappingTemplate

7 1 1 3 0 2 4 4 4 4 0.178278 28/30 NonOverlappingTemplate

7 3 3 3 3 1 1 4 2 3 0.468595 28/30 NonOverlappingTemplate

3 3 3 4 1 1 6 6 2 1 0.299251 29/30 NonOverlappingTemplate

5	2	4	3	1	4	3	3	2	3	0.911413	29/30		NonOverlappingTemplate
4	1	4	3	4	3	2	5	2	2	0.862344	30/30		NonOverlappingTemplate
7	5	1	3	3	2	3	1	2	3	0.350485	29/30		NonOverlappingTemplate
1	3	1	6	3	1	5	4	1	5	0.253551	30/30		NonOverlappingTemplate
8	0	0	6	3	1	7	0	2	3	0.001232	27/30	*	NonOverlappingTemplate
3	2	1	2	4	1	6	8	2	1	0.054199	30/30		NonOverlappingTemplate
6	1	1	1	2	3	4	5	3	4	0.407091	29/30		NonOverlappingTemplate
5	1	6	4	4	2	3	0	3	2	0.350485	28/30		NonOverlappingTemplate
4	1	1	3	3	3	4	4	2	5	0.804337	30/30		NonOverlappingTemplate
5	2	2	2	5	3	3	4	1	3	0.804337	29/30		NonOverlappingTemplate
2	2	6	7	1	1	3	2	4	2	0.178278	30/30		NonOverlappingTemplate
1	2	1	3	6	1	3	4	3	6	0.299251	30/30		NonOverlappingTemplate
6	0	3	2	7	5	3	0	2	2	0.054199	29/30		NonOverlappingTemplate
4	5	3	4	4	4	2	2	2	0	0.671779	27/30	*	NonOverlappingTemplate
0	1	1	1	3	3	6	6	0	9	0.000954	30/30		NonOverlappingTemplate
1	2	6	1	5	6	0	2	1	6	0.035174	30/30		NonOverlappingTemplate
7	5	1	2	2	4	0	3	2	4	0.178278	30/30		NonOverlappingTemplate
3	2	5	3	3	2	4	2	2	4	0.949602	30/30		NonOverlappingTemplate
4	5	3	0	2	1	2	7	4	2	0.178278	30/30		NonOverlappingTemplate
1	2	1	8	5	1	5	2	4	1	0.043745	30/30		NonOverlappingTemplate
4	4	7	3	1	2	5	1	2	1	0.213309	30/30		NonOverlappingTemplate
0	0	2	6	4	3	5	2	1	7	0.035174	30/30		NonOverlappingTemplate

3	3	2	4	3	2	2	4	3	4	0.991468	30/30		NonOverlappingTemplate
3	2	4	3	2	4	4	1	2	5	0.862344	29/30		NonOverlappingTemplate
4	2	1	2	1	8	2	7	2	1	0.022503	29/30		NonOverlappingTemplate
5	3	3	5	5	0	2	2	3	2	0.534146	30/30		NonOverlappingTemplate
0	3	2	1	5	4	3	4	3	5	0.534146	30/30		NonOverlappingTemplate
2	1	3	2	3	3	2	5	3	6	0.671779	30/30		NonOverlappingTemplate
3	3	7	3	5	4	0	0	3	2	0.148094	28/30		NonOverlappingTemplate
5	1	3	2	4	4	3	3	1	4	0.804337	27/30	*	NonOverlappingTemplate
3	3	4	5	2	3	2	2	5	1	0.804337	30/30		NonOverlappingTemplate
5	3	3	0	4	2	1	3	1	8	0.066882	30/30		NonOverlappingTemplate
6	2	2	2	5	3	6	2	2	0	0.213309	30/30		NonOverlappingTemplate
1	1	2	4	4	6	3	6	1	2	0.253551	30/30		NonOverlappingTemplate
1	3	3	6	2	4	3	3	2	3	0.804337	30/30		NonOverlappingTemplate
3	1	2	4	1	7	3	3	2	4	0.407091	29/30		NonOverlappingTemplate
5	3	0	0	1	3	5	5	3	5	0.178278	28/30		NonOverlappingTemplate
2	4	1	4	5	5	2	3	3	1	0.671779	29/30		NonOverlappingTemplate
2	1	2	3	1	2	7	8	2	2	0.035174	30/30		NonOverlappingTemplate
5	2	4	4	3	2	4	2	0	4	0.671779	30/30		NonOverlappingTemplate
1	4	3	5	2	3	5	5	1	1	0.468595	30/30		NonOverlappingTemplate
3	2	7	3	3	3	3	3	2	1	0.602458	30/30		NonOverlappingTemplate
0	4	1	7	3	3	3	4	2	3	0.299251	30/30		NonOverlappingTemplate
1	0	6	1	6	2	7	5	2	0	0.008879	30/30		NonOverlappingTemplate

2 2 3 6 1 2 4 5 3 2 0.602458 30/30 NonOverlappingTemplate

5 4 1 3 2 4 2 4 3 2 0.862344 27/30 * NonOverlappingTemplate

4 0 2 3 4 2 4 4 1 6 0.407091 28/30 NonOverlappingTemplate

10 2 2 4 0 2 2 2 2 4 0.008879 29/30 NonOverlappingTemplate

5 1 3 5 1 3 1 4 3 4 0.602458 29/30 NonOverlappingTemplate

1 3 3 1 3 3 6 5 3 2 0.602458 30/30 NonOverlappingTemplate

1 3 4 3 5 2 4 1 4 3 0.804337 30/30 NonOverlappingTemplate

8 1 1 0 3 3 5 3 2 4 0.066882 29/30 NonOverlappingTemplate

7 6 2 1 1 1 2 2 2 6 0.054199 28/30 NonOverlappingTemplate

5 5 2 4 3 2 1 2 4 2 0.739918 30/30 NonOverlappingTemplate

3 2 3 3 2 5 3 7 1 1 0.350485 30/30 NonOverlappingTemplate

5 2 2 2 0 3 5 3 3 5 0.534146 30/30 NonOverlappingTemplate

1 4 2 2 4 4 4 3 3 3 0.949602 30/30 NonOverlappingTemplate

3 3 2 3 3 3 4 3 0 6 0.671779 30/30 NonOverlappingTemplate

3 0 2 2 4 6 4 4 2 3 0.534146 30/30 NonOverlappingTemplate

2 0 3 2 3 3 2 4 8 3 0.178278 30/30 NonOverlappingTemplate

5 1 4 5 2 3 2 2 3 3 0.804337 30/30 NonOverlappingTemplate

3 3 3 2 1 3 2 3 3 7 0.602458 30/30 NonOverlappingTemplate

4 1 3 2 10 3 1 1 2 3 0.011250 27/30 * NonOverlappingTemplate

4 3 3 0 3 2 1 5 3 6 0.407091 30/30 NonOverlappingTemplate

2 3 3 4 4 3 2 2 5 2 0.949602 30/30 NonOverlappingTemplate

3 3 1 6 4 1 3 3 2 4 0.671779 30/30 NonOverlappingTemplate

3	3	1	1	2	3	3	4	5	5	0.739918	29/30		NonOverlappingTemplate
4	2	1	4	3	4	6	3	3	0	0.468595	30/30		NonOverlappingTemplate
2	2	2	3	0	1	4	2	8	6	0.043745	30/30		NonOverlappingTemplate
3	2	3	3	0	4	4	4	0	7	0.178278	30/30		NonOverlappingTemplate
3	1	1	6	3	3	3	2	5	3	0.602458	30/30		NonOverlappingTemplate
5	5	2	1	0	5	4	2	2	4	0.350485	28/30		NonOverlappingTemplate
2	2	2	3	5	3	4	6	2	1	0.602458	30/30		NonOverlappingTemplate
1	1	7	4	2	1	1	5	5	3	0.122325	30/30		NonOverlappingTemplate
0	4	4	4	5	3	4	3	2	1	0.602458	30/30		NonOverlappingTemplate
4	2	6	4	1	5	2	4	1	1	0.350485	30/30		NonOverlappingTemplate
3	0	3	3	4	1	2	9	1	4	0.028181	29/30		NonOverlappingTemplate
4	3	4	1	3	3	5	3	1	3	0.862344	30/30		NonOverlappingTemplate
5	6	3	3	1	2	6	1	0	3	0.148094	30/30		NonOverlappingTemplate
4	4	3	2	3	4	4	1	2	3	0.949602	30/30		NonOverlappingTemplate
4	4	1	1	2	4	3	6	3	2	0.602458	28/30		NonOverlappingTemplate
2	4	2	4	5	5	2	0	2	4	0.534146	29/30		NonOverlappingTemplate
6	5	4	2	0	1	4	3	5	0	0.122325	29/30		NonOverlappingTemplate
3	4	3	1	0	2	4	4	6	3	0.468595	28/30		NonOverlappingTemplate
6	1	4	2	1	8	2	3	2	1	0.054199	27/30	*	NonOverlappingTemplate
4	2	2	6	2	2	3	1	3	5	0.602458	30/30		NonOverlappingTemplate
1	2	3	5	4	3	4	6	2	0	0.350485	30/30		NonOverlappingTemplate
4	1	1	5	4	6	5	0	2	2	0.178278	30/30		NonOverlappingTemplate

4	6	2	4	4	2	2	2	2	2	0.739918	30/30		NonOverlappingTemplate
2	2	4	4	4	1	8	2	3	0	0.100508	30/30		NonOverlappingTemplate
5	0	5	1	1	2	4	5	4	3	0.299251	30/30		NonOverlappingTemplate
0	2	3	1	4	3	5	6	4	2	0.350485	30/30		NonOverlappingTemplate
5	2	3	3	2	1	3	3	3	5	0.862344	29/30		NonOverlappingTemplate
3	0	2	5	1	5	2	4	1	7	0.100508	27/30	*	NonOverlappingTemplate
5	4	3	2	3	4	0	5	2	2	0.602458	30/30		NonOverlappingTemplate
5	1	1	4	2	2	2	2	5	6	0.350485	30/30		NonOverlappingTemplate
2	3	2	4	4	2	1	2	6	4	0.671779	30/30		NonOverlappingTemplate
7	1	2	3	1	4	4	3	0	5	0.148094	26/30	*	NonOverlappingTemplate
4	2	4	2	2	1	4	4	4	3	0.911413	30/30		NonOverlappingTemplate
1	4	5	3	2	5	1	3	4	2	0.671779	30/30		NonOverlappingTemplate
3	4	3	2	3	6	1	5	2	1	0.534146	30/30		NonOverlappingTemplate
4	1	0	1	6	5	1	5	1	6	0.043745	29/30		NonOverlappingTemplate
3	6	1	1	3	1	4	4	3	4	0.534146	30/30		NonOverlappingTemplate
0	2	3	2	5	4	4	4	1	5	0.468595	30/30		NonOverlappingTemplate
2	4	4	2	4	6	1	3	0	4	0.407091	30/30		NonOverlappingTemplate
0	4	3	2	7	2	7	3	0	2	0.035174	30/30		NonOverlappingTemplate
2	4	3	5	3	5	3	2	2	1	0.804337	29/30		NonOverlappingTemplate
5	3	1	0	4	2	4	4	2	5	0.468595	30/30		NonOverlappingTemplate
0	2	3	4	2	3	3	4	1	8	0.122325	30/30		NonOverlappingTemplate
2	3	1	4	5	2	4	5	2	2	0.739918	28/30		NonOverlappingTemplate

2	7	1	0	5	4	2	4	1	4	0.122325	30/30		NonOverlappingTemplate
0	5	3	3	3	2	3	1	5	5	0.468595	30/30		NonOverlappingTemplate
3	6	1	0	1	5	3	4	4	3	0.299251	30/30		NonOverlappingTemplate
3	5	2	1	4	3	3	3	5	1	0.739918	30/30		NonOverlappingTemplate
4	2	5	3	2	3	3	0	6	2	0.468595	29/30		NonOverlappingTemplate
3	1	2	2	3	4	3	6	3	3	0.804337	30/30		NonOverlappingTemplate
6	2	5	2	5	4	1	1	3	1	0.299251	25/30	*	NonOverlappingTemplate
4	2	1	3	6	2	3	2	4	3	0.739918	29/30		NonOverlappingTemplate
1	3	0	3	8	2	4	5	1	3	0.066882	30/30		NonOverlappingTemplate
1	6	6	1	3	4	2	2	3	2	0.350485	30/30		NonOverlappingTemplate
3	0	3	5	6	2	3	3	4	1	0.407091	30/30		NonOverlappingTemplate
6	3	3	2	4	3	2	2	4	1	0.739918	30/30		NonOverlappingTemplate
9	3	3	4	1	1	2	4	2	1	0.043745	28/30		NonOverlappingTemplate
2	3	1	3	4	3	4	5	3	2	0.911413	29/30		NonOverlappingTemplate
1	3	3	1	5	6	1	6	1	3	0.178278	30/30		NonOverlappingTemplate
5	3	4	1	4	2	3	2	3	3	0.911413	30/30		NonOverlappingTemplate
5	2	3	1	2	5	2	1	5	4	0.534146	30/30		NonOverlappingTemplate
7	1	0	2	3	7	6	1	2	1	0.011250	28/30		NonOverlappingTemplate
3	3	1	3	6	2	6	2	1	3	0.407091	28/30		NonOverlappingTemplate
2	1	5	4	3	3	3	3	4	2	0.911413	30/30		NonOverlappingTemplate
1	8	6	1	4	3	2	2	1	2	0.054199	30/30		NonOverlappingTemplate
8	3	1	0	4	1	2	4	0	7	0.005490	29/30		NonOverlappingTemplate

6 4 0 2 1 4 6 1 3 3 0.178278 29/30 NonOverlappingTemplate

1 5 1 0 2 5 3 5 5 3 0.253551 30/30 NonOverlappingTemplate

1 0 2 1 5 4 2 3 5 7 0.100508 30/30 NonOverlappingTemplate

7 2 1 3 2 4 1 4 4 2 0.350485 29/30 NonOverlappingTemplate

0 0 0 0 5 3 6 7 4 5 0.005490 30/30 NonOverlappingTemplate

2 3 3 2 4 1 4 6 3 2 0.739918 30/30 NonOverlappingTemplate

2 3 3 4 4 3 3 1 5 2 0.911413 30/30 NonOverlappingTemplate

1 0 5 1 0 4 2 6 5 6 0.035174 30/30 OverlappingTemplate

30 0 0 0 0 0 0 0 0 0 0.000000 * 0/30 * Universal

12 2 9 2 2 1 2 0 0 0 0.000000 * 30/30 ApproximateEntropy

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursions

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursions

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursions

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursions

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursions

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursions

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursions

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursions

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursionsVariant

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursionsVariant

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursionsVariant

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursionsVariant

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursionsVariant

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursionsVariant

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursionsVariant

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursionsVariant

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursionsVariant

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursionsVariant

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursionsVariant

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursionsVariant

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursionsVariant

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursionsVariant

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursionsVariant

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursionsVariant

0 0 0 0 0 0 0 0 0 0 ---- ------ RandomExcursionsVariant

3 3 1 2 0 2 2 2 7 8 0.022503 30/30 Serial

4 2 0 2 5 1 2 5 5 4 0.350485 30/30 Serial

6 1 4 3 3 1 1 5 2 4 0.407091 3

0/30 LinearComplexity

7. 验证环境 warning QA

针对验证 log 中的 warning 进行分析，回答是否会影响结果，可以尝试分析原因

Miss braces in $$fflush call :缺少括号，属于代码规范