FIT1047 - Week 3

Central Processing Units

(part 2)

Recap

In the previous lecture we saw

- Basic CPU architecture
- MARIE assembly code
- Combinational circuits (adders, MUXes, decoders)
- ALUs

Overview

- Sequential Circuits
  - flip flops, registers, counters
  - memory
- Control
  - executing a program

Sequential Circuits

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(output depends on sequence of inputs)

Sequences

How can a circuit remember the past?

Sequences

How can a circuit remember the past?

Feed the output back into the input!

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Let's add a switch to control the state.

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Can we implement a toggle?

Sequences

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This is called an SR latch (set-reset-latch).

SR Latch

Truth table:

S	R	Q(t)	Q(t+1)
0	0	0	0
0	1	0	1
1	0	0	0
1	1	forbidden	
0	0	1	1
0	1	1	1
1	0	1	0
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But digital circuits use a single input (bit).

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- One input: the data to be stored
- One output: the data currently stored
- Plus a clock: state only changes on "positive edge"

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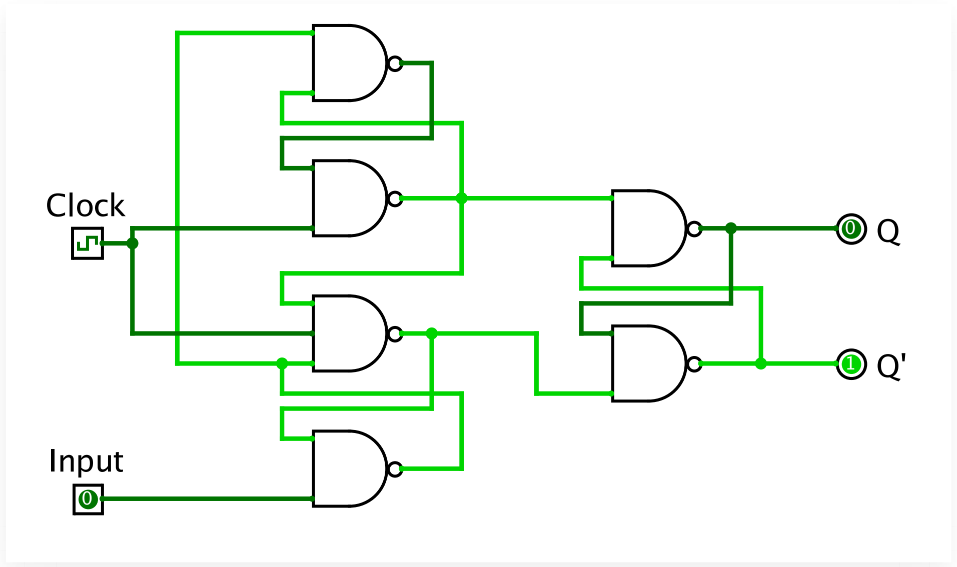

Registers

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- Some special purpose registers
  - PC, IR, MBR, MAR (for MARIE)
- Some general purpose registers
  - AC (MARIE), AH/AL, BH/BL, CH/CL, DH/DL (x86)
- Fixed bit width
  - e.g. 16 bits in MARIE, 16/32 or 64 bits in modern processors

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- Collection of registers

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- Additional input: select register for writing
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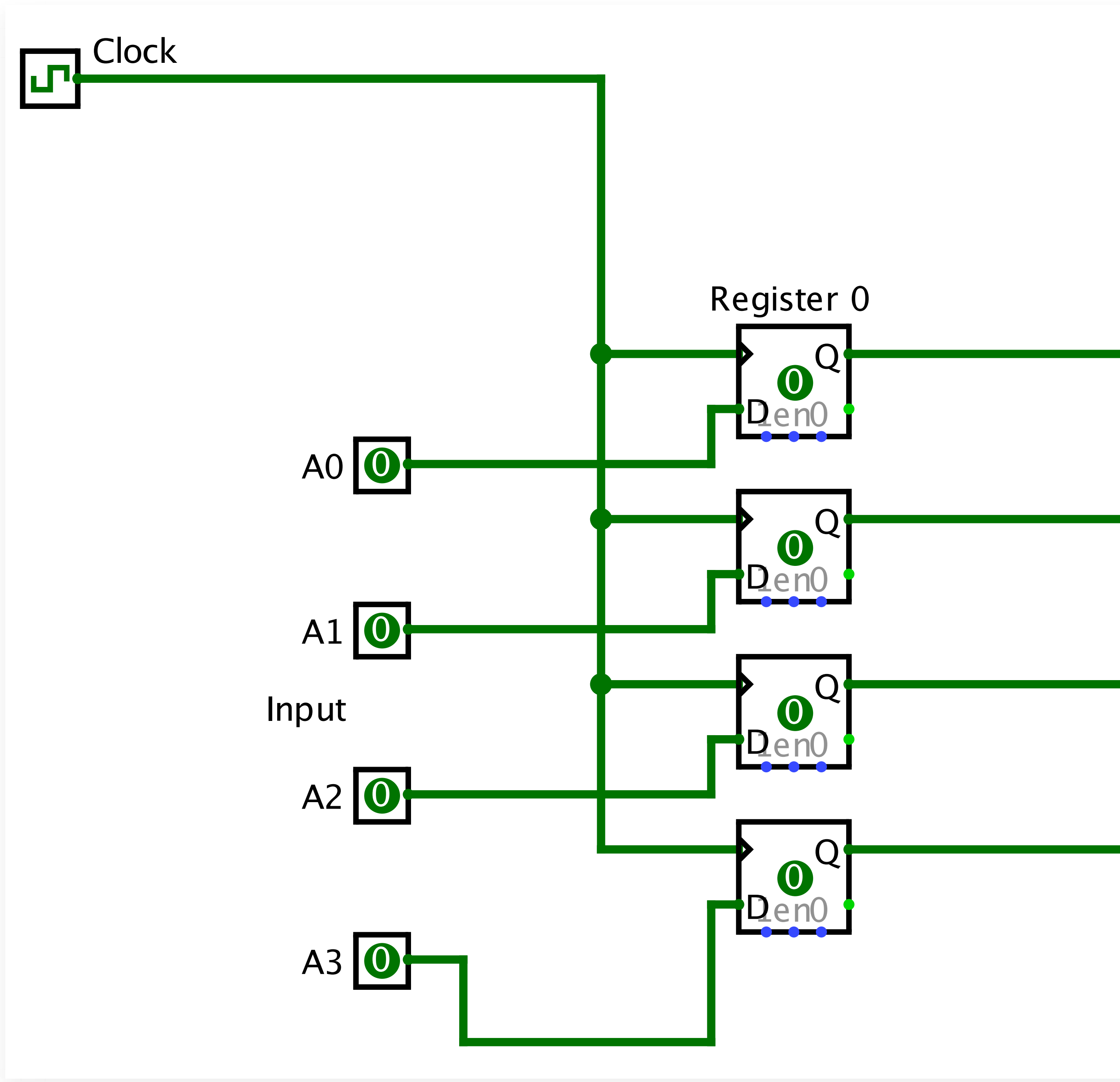

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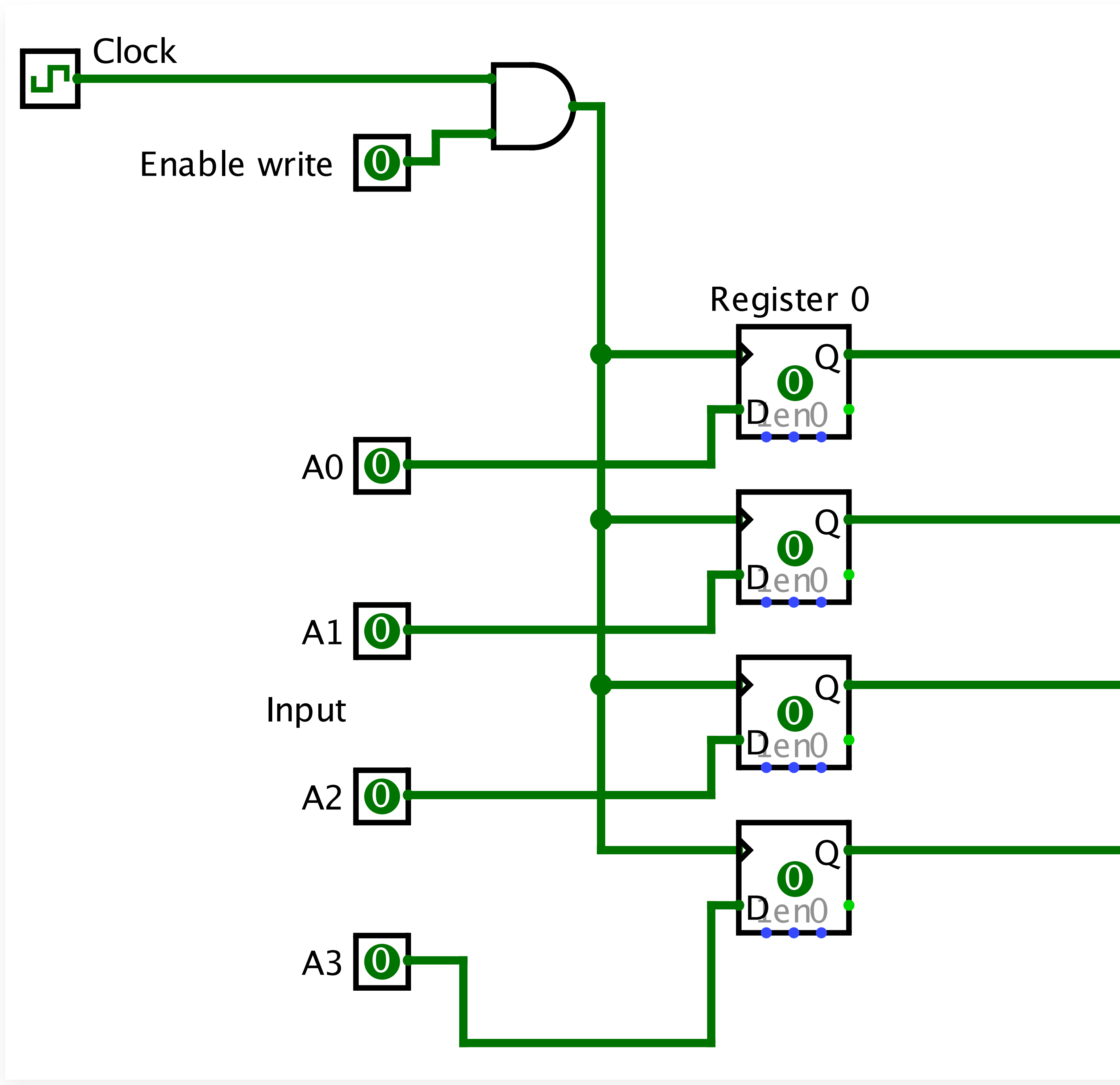

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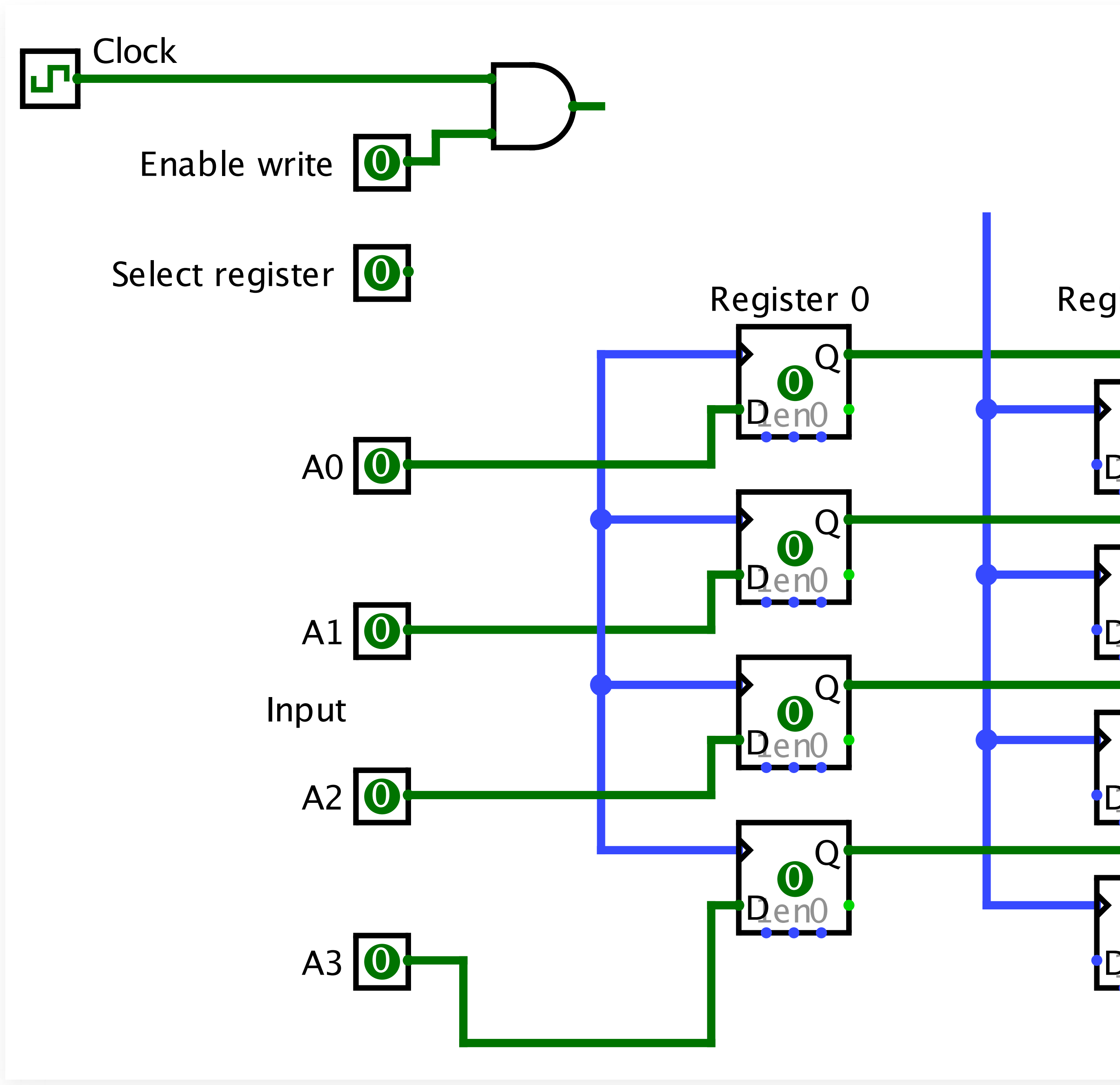

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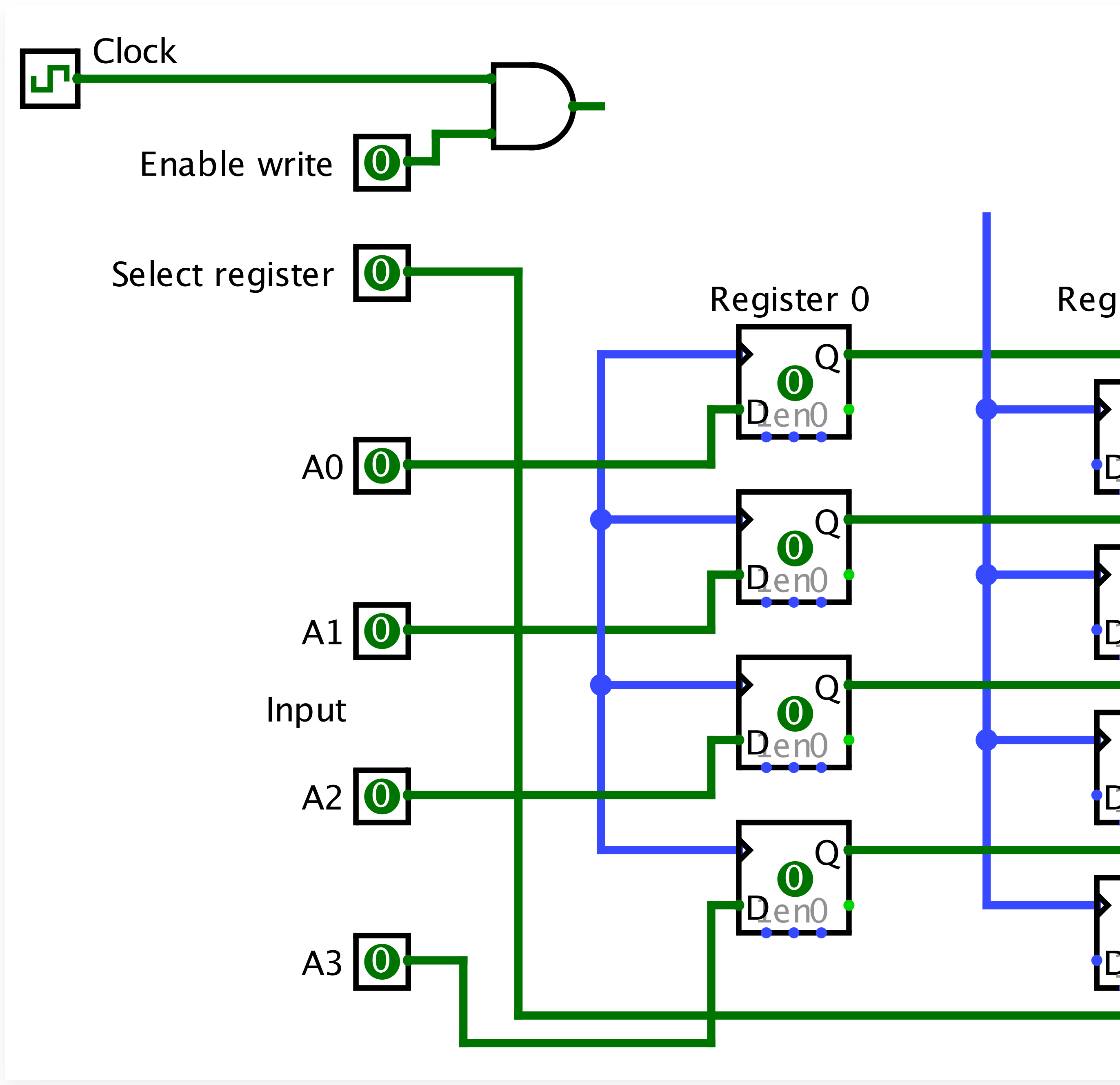

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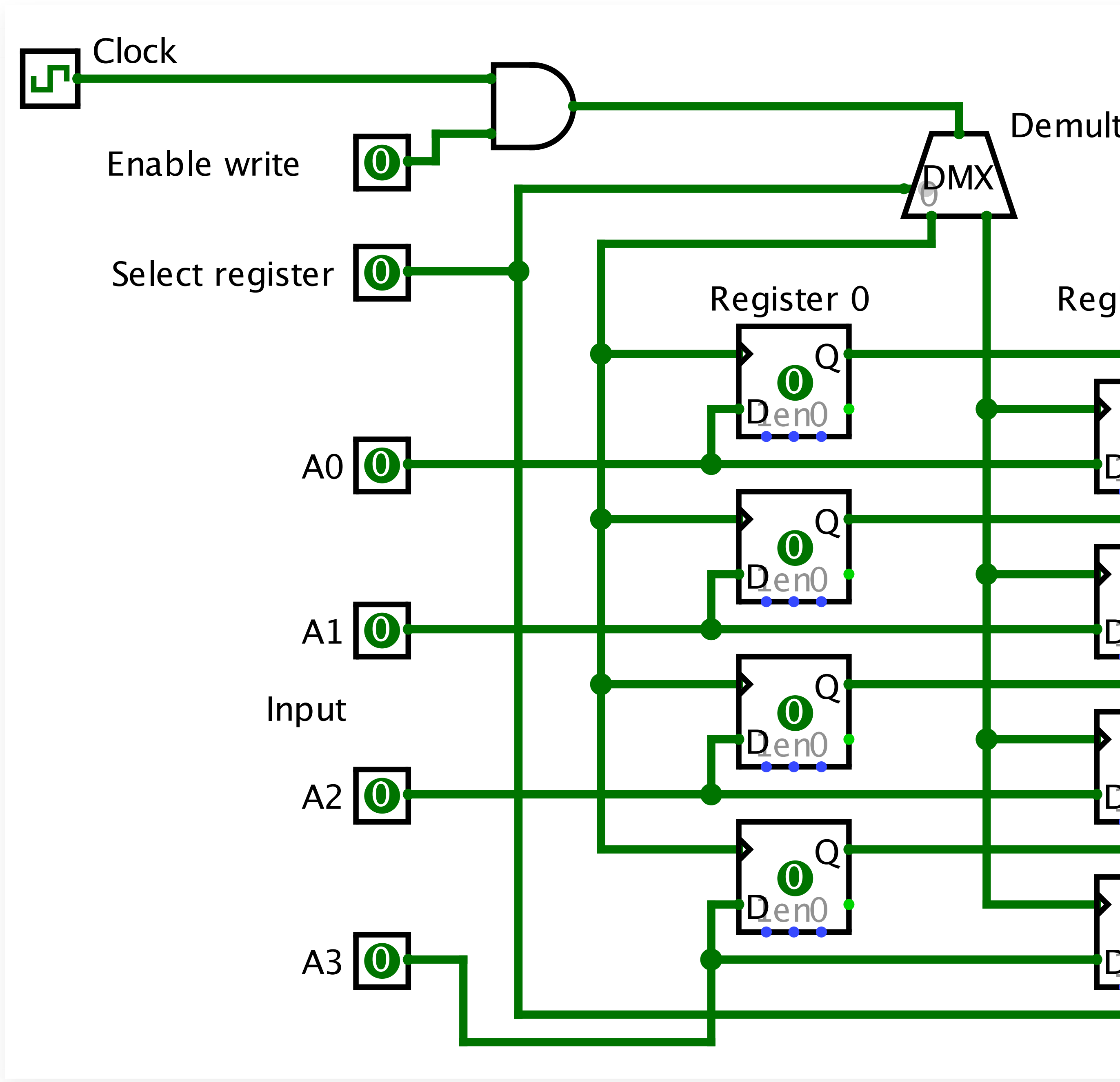

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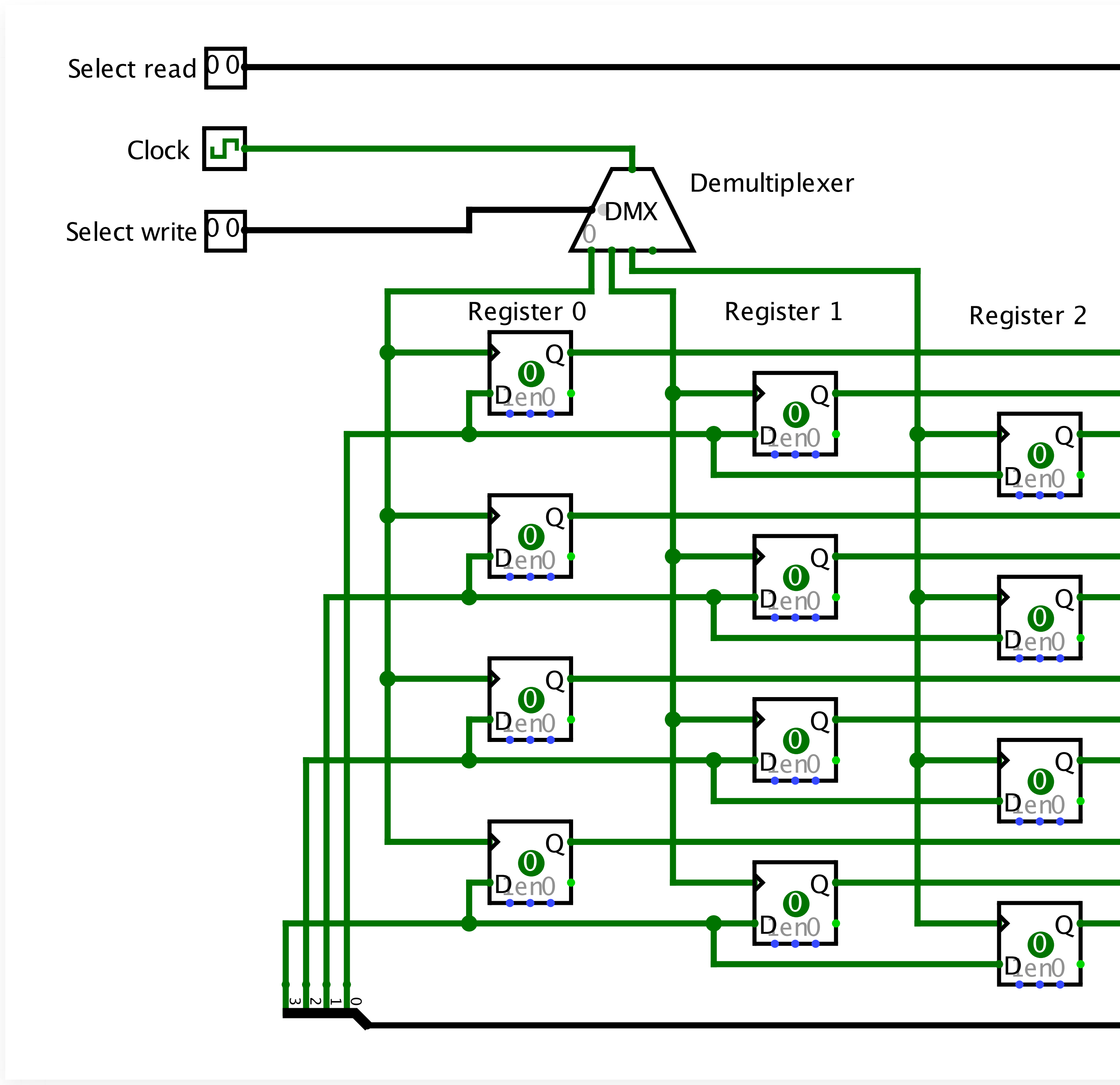

Control

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(the machine)

Control what?

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  - RTL = Register transfer language

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- Implement the RTL code for each instruction
  - RTL = Register transfer language
- Generate control signals for individual circuits
  - opcode for the ALU
  - read/write register number for the register file
  - memory read/write

Timing

Let's take a look at the Add X instruction.

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  - register write control: MAR
- MBR   M[MAR]
  - memory: read (always reads at address MAR)
  - register write control: MBR

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Let's take a look at the Add X instruction.

- MAR   X
  - register read control: IR (X is in IR)
  - register write control: MAR
- MBR   M[MAR]
  - memory: read (always reads at address MAR)
  - register write control: MBR
- AC   AC + MBR
  - ALU opcode: addition (always reads AC and MBR)
  - register write control: AC

Timing

How do we generate that sequence of signals?

Add a cycle counter!

- n outputs T_0 to T_n
- Cycle through these outputs at each clock cycle.
- Has an input C_n to reset to T_0.
- Now we can write RTL using Boolean statements!

Cycle counter

Cycle counter

Control signals

- Register read: $P_2\ P_1\ P_0$
  - Memory=0, MAR=1, PC=2, MBR=3, AC=4, IR=7
- Register write: $P_5\ P_4\ P_3$
- ALU: $A_1\ A_0$
  - Add=1, Subt=2, Clear=3

Add X with signals

MAR X

T_3 P_3 P_2 P_1 P_0

Add X with signals

MAR   X

$T_3 \; P_3 \; P_2 \; P_1 \; P_0$

- read IR ($P_2 = 1, P_1 = 1, P_0 = 1$)

Add X with signals

MAR   X

$T_3 \; P_3 \; P_2 \; P_1 \; P_0$

- read IR ($P_2 = 1, P_1 = 1, P_0 = 1$)
- write MAR ($P_5 = 0, P_4 = 0, P_3 = 1$)

Add X with signals

MAR X

$T_3 \; P_3 \; P_2 \; P_1 \; P_0$

- read IR ($P_2 = 1, P_1 = 1, P_0 = 1$)
- write MAR ($P_5 = 0, P_4 = 0, P_3 = 1$)

Note: T_0, T_1, T_2 are used for the fetch cycle.

Add X with signals

MBR M[MAR]

T_4 P_4 P_3 M_R

Add X with signals

MBR M[MAR]

T_4 P_4 P_3 M_R

- Read memory (always reads at address MAR)

Add X with signals

MBR   M[MAR]

$T_4\ P_4\ P_3\ M_R$

- Read memory (always reads at address MAR)
- write MBR ($P_5 = 0, P_4 = 1, P_3 = 1$)

Add X with signals

AC   AC + MBR

T_5 A_0 P_5 P_1 P_0

Add X with signals

AC   AC + MBR

$T_5 \ A_0 \ P_5 \ P_1 \ P_0$

- ALU: addition ($A_1 = 0, A_0 = 1$)

Add X with signals

AC   AC + MBR

$T_5 \; A_0 \; P_5 \; P_1 \; P_0$

- ALU: addition ($A_1 = 0$, $A_0 = 1$)
- read MBR ($P_2 = 0$, $P_1 = 1$, $P_0 = 1$)

Add X with signals

AC   AC + MBR

$T_5 \; A_0 \; P_5 \; P_1 \; P_0$

- ALU: addition ($A_1 = 0, A_0 = 1$)
- read MBR ($P_2 = 0, P_1 = 1, P_0 = 1$)
- write AC ($P_5 = 1, P_4 = 0, P_3 = 0$)

Add X with signals

AC   AC + MBR

T_6 C_r

Add X with signals

AC   AC + MBR

T_6 C_r

- reset cycle counter

Control circuit (Add X)

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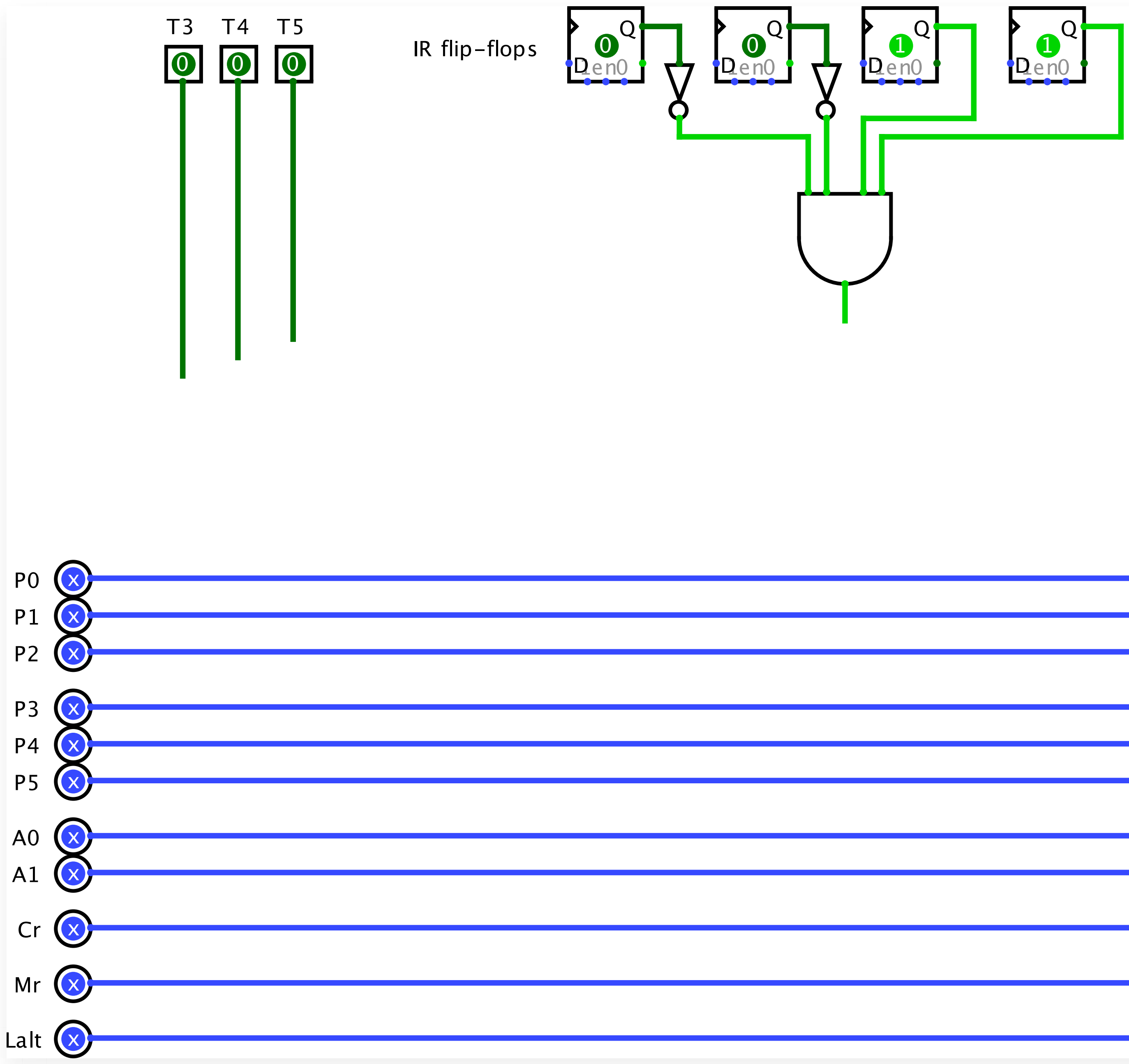
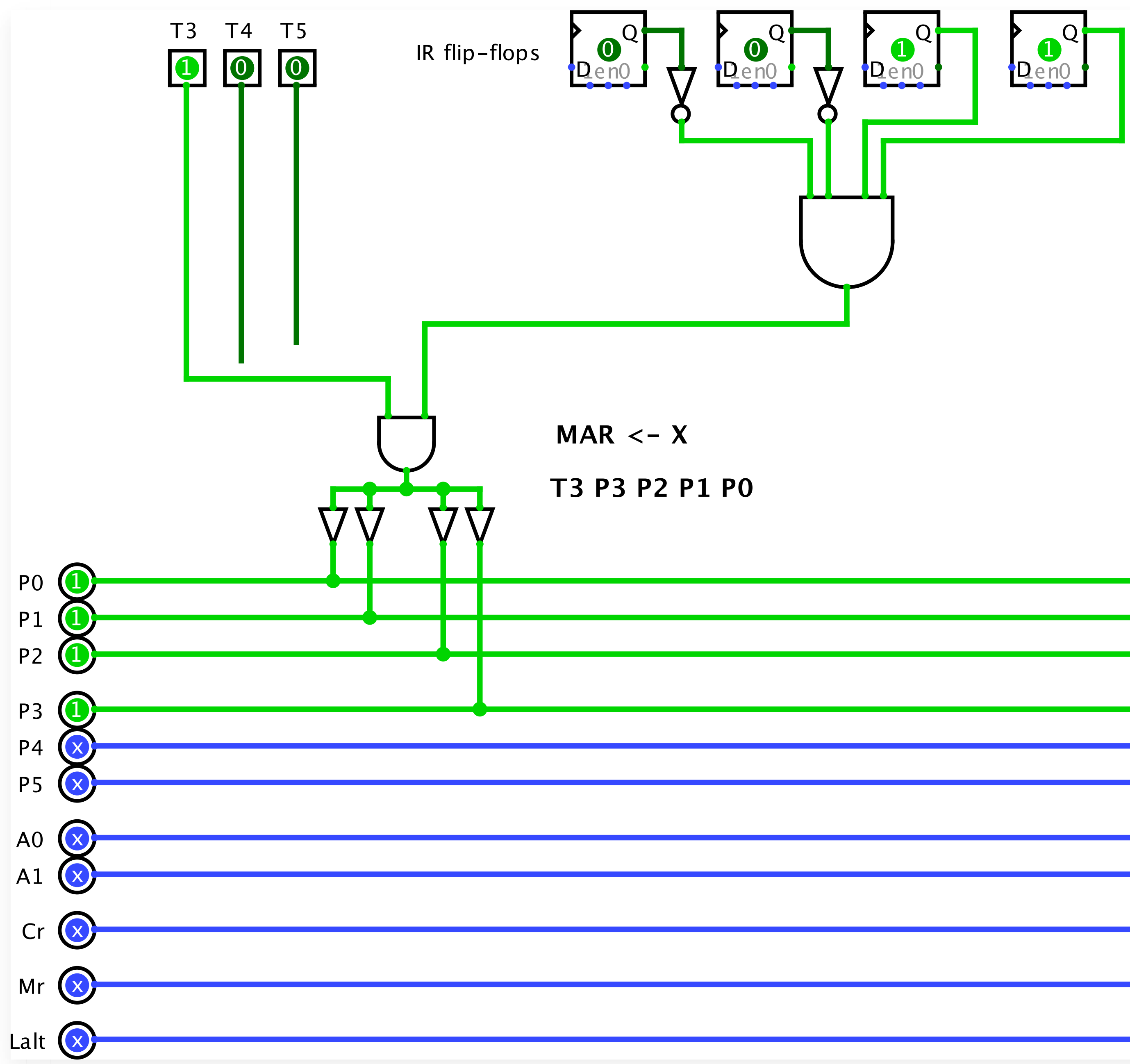


Control circuit (Add X)



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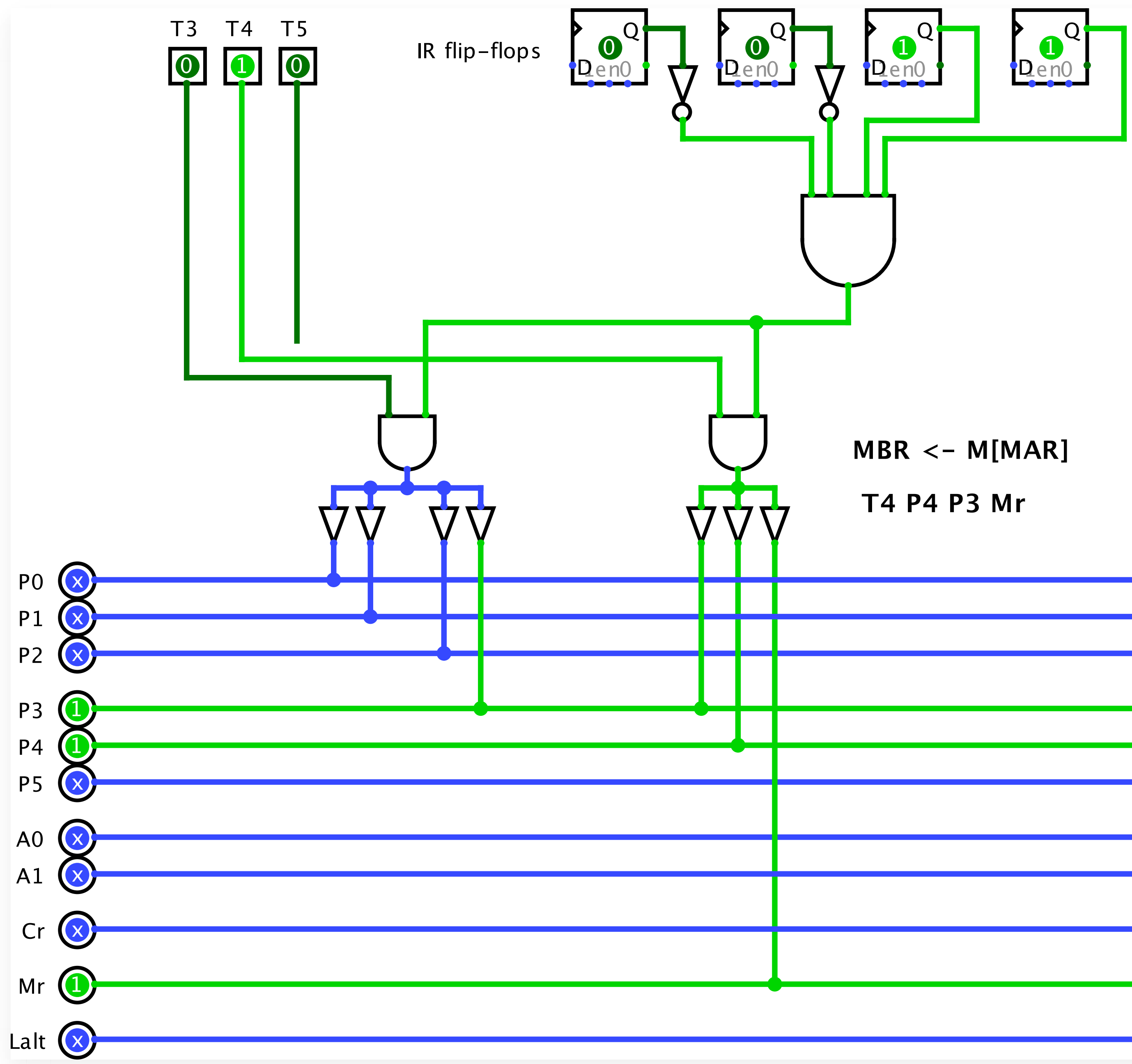

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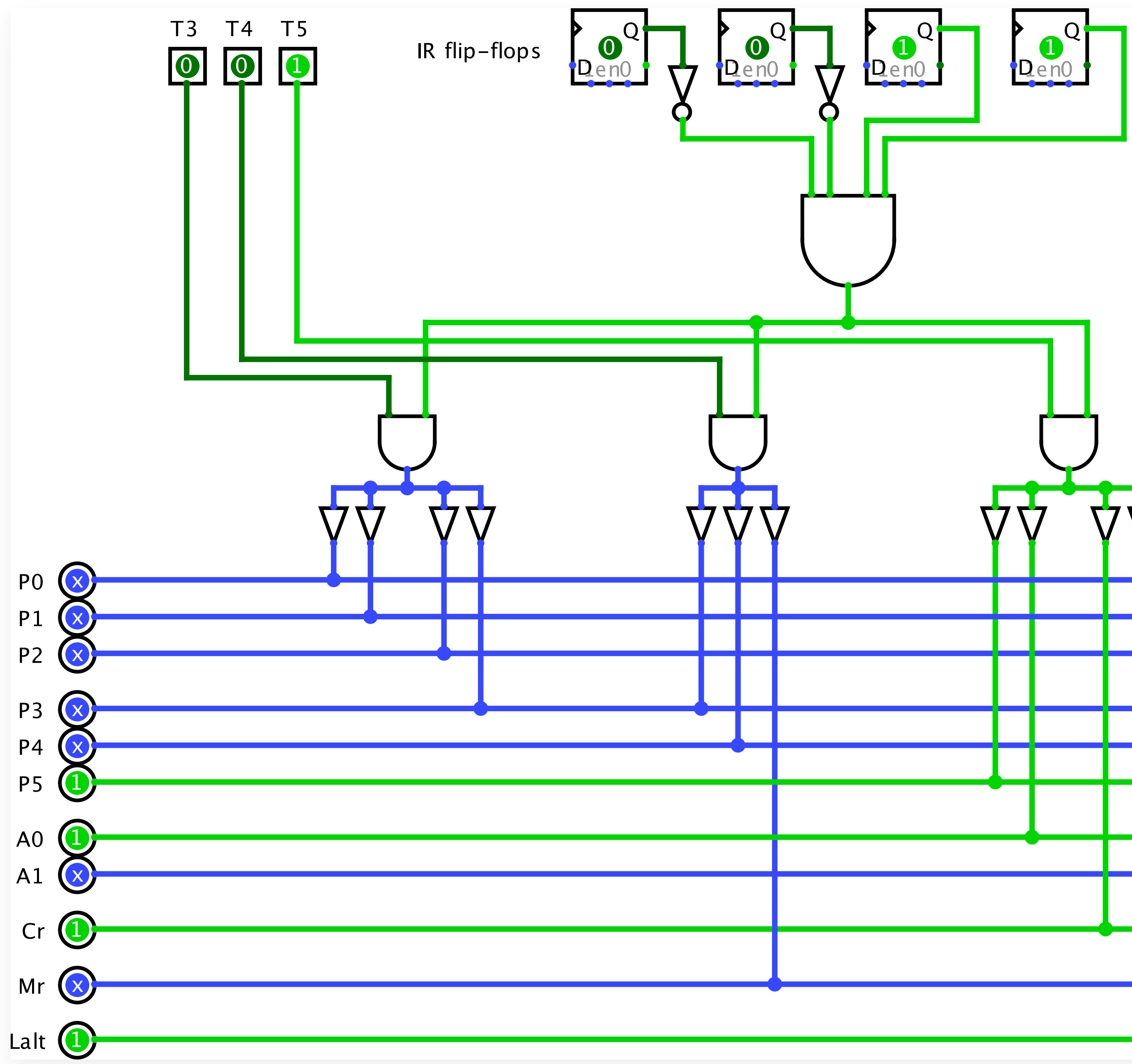

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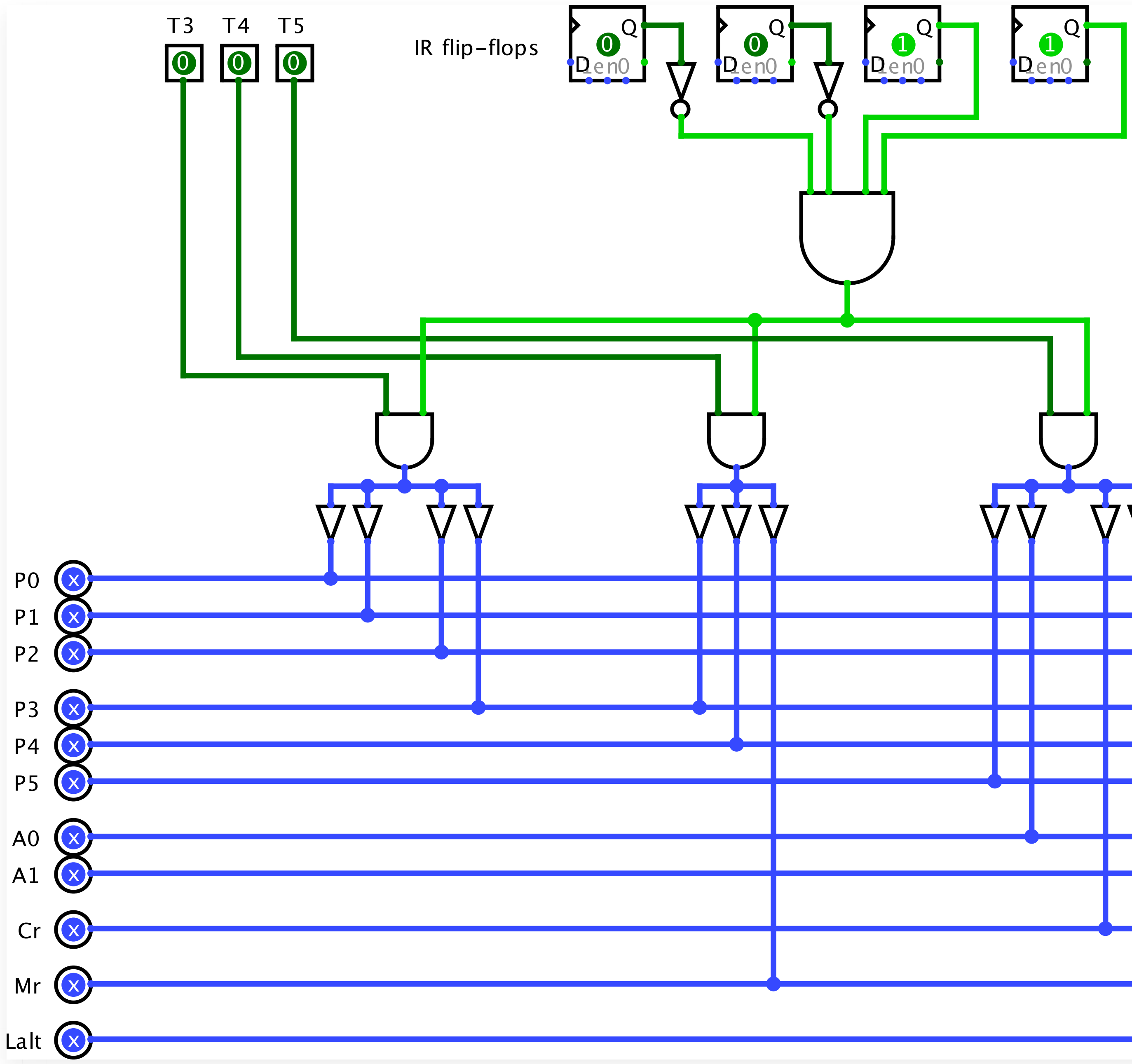

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RTL for each instruction is implemented using gates.

- Very fast!
- But really complicated to design.
- What if we want to add instructions?
- What if we made a mistake?

Microprogrammed Control

Break up instructions into microoperations.

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- One microop per possible RTL instruction
  - Far fewer than instructions!

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- One microop per possible RTL instruction
  - Far fewer than instructions!
- Microops for each instruction stored in memory in the processor
- Execution slightly slower, but
  - Circuits for microops much simpler
  - Microcode can be updated

Putting it all together

MARIE Data Paths

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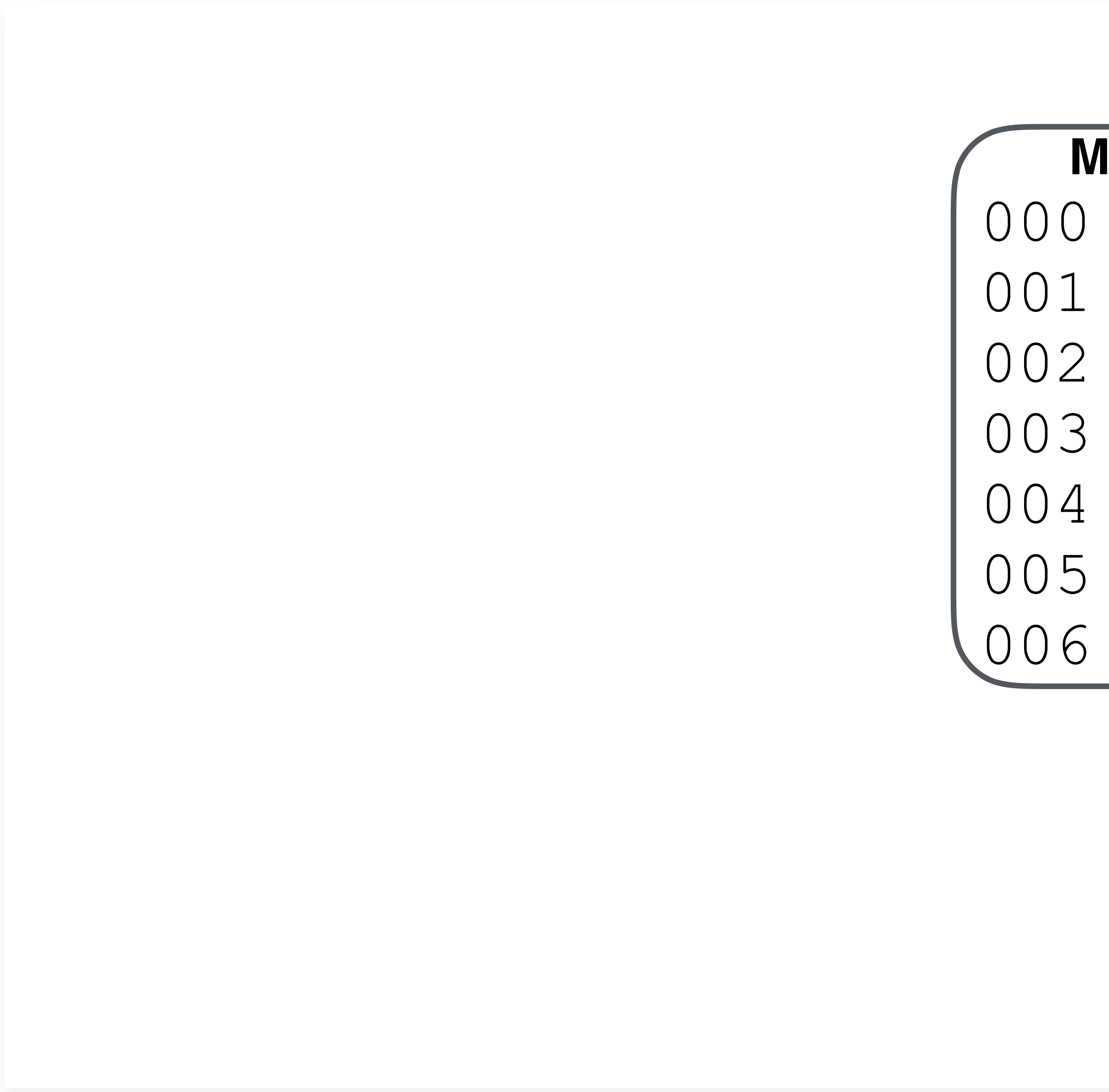

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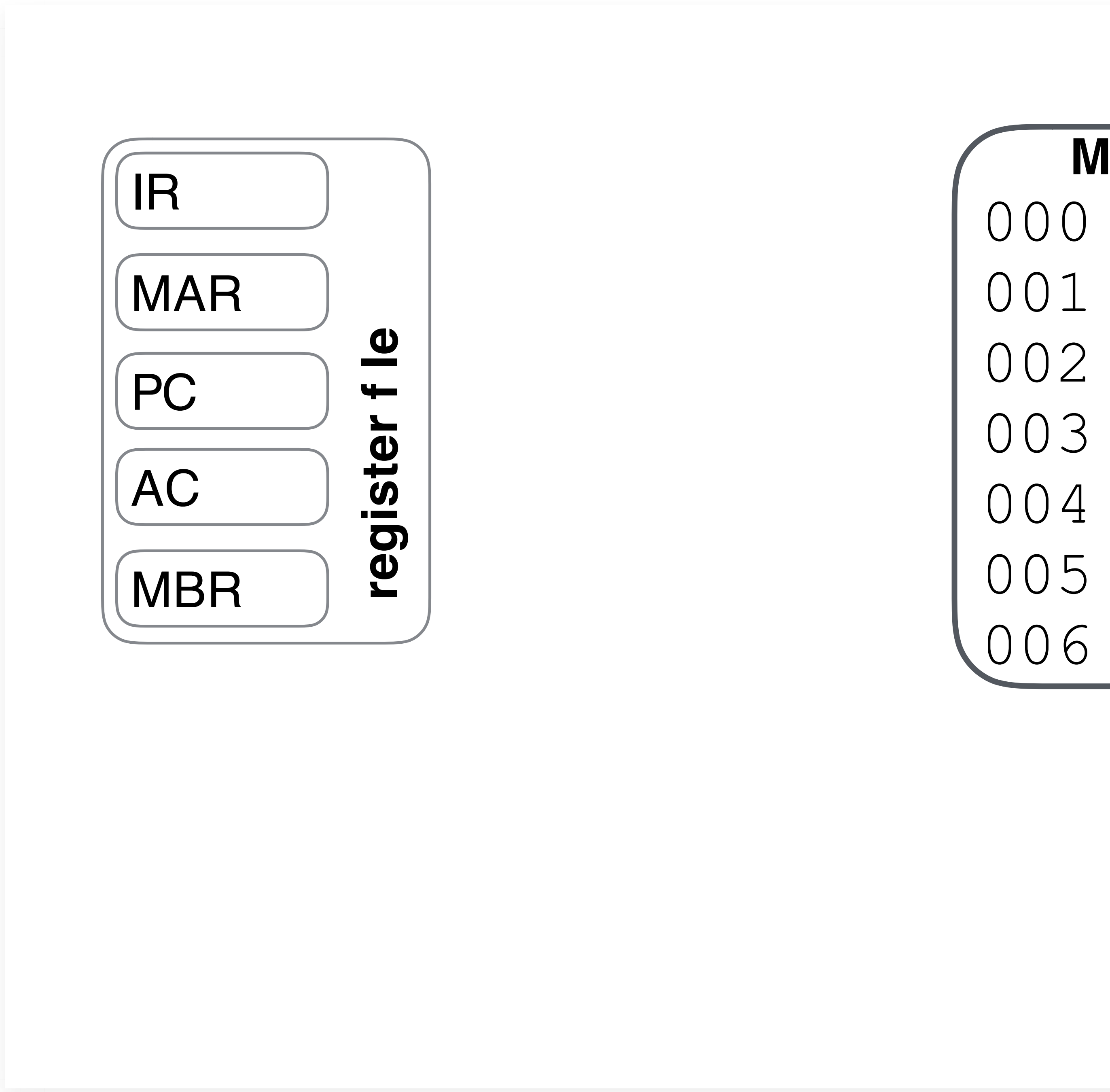

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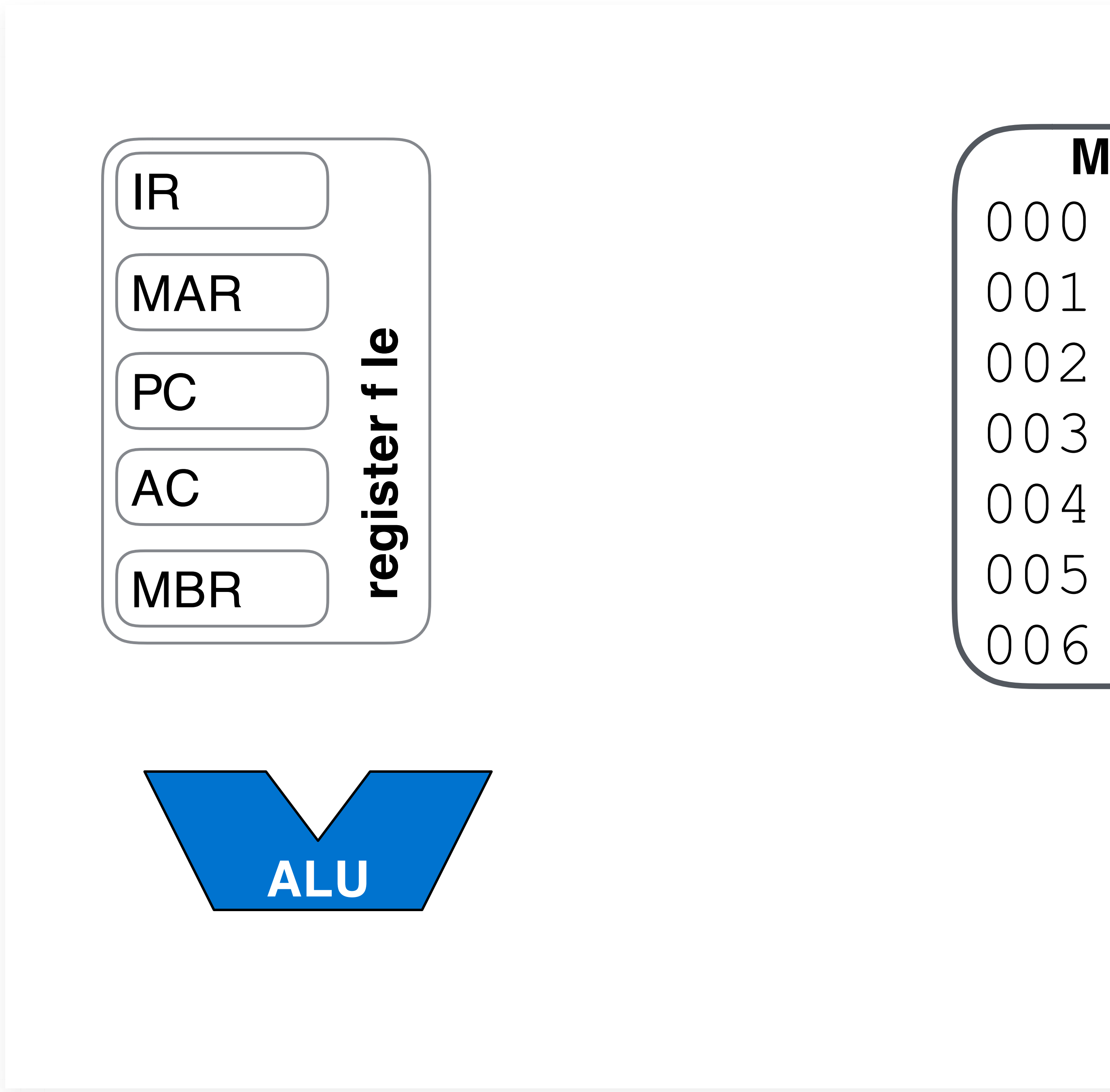

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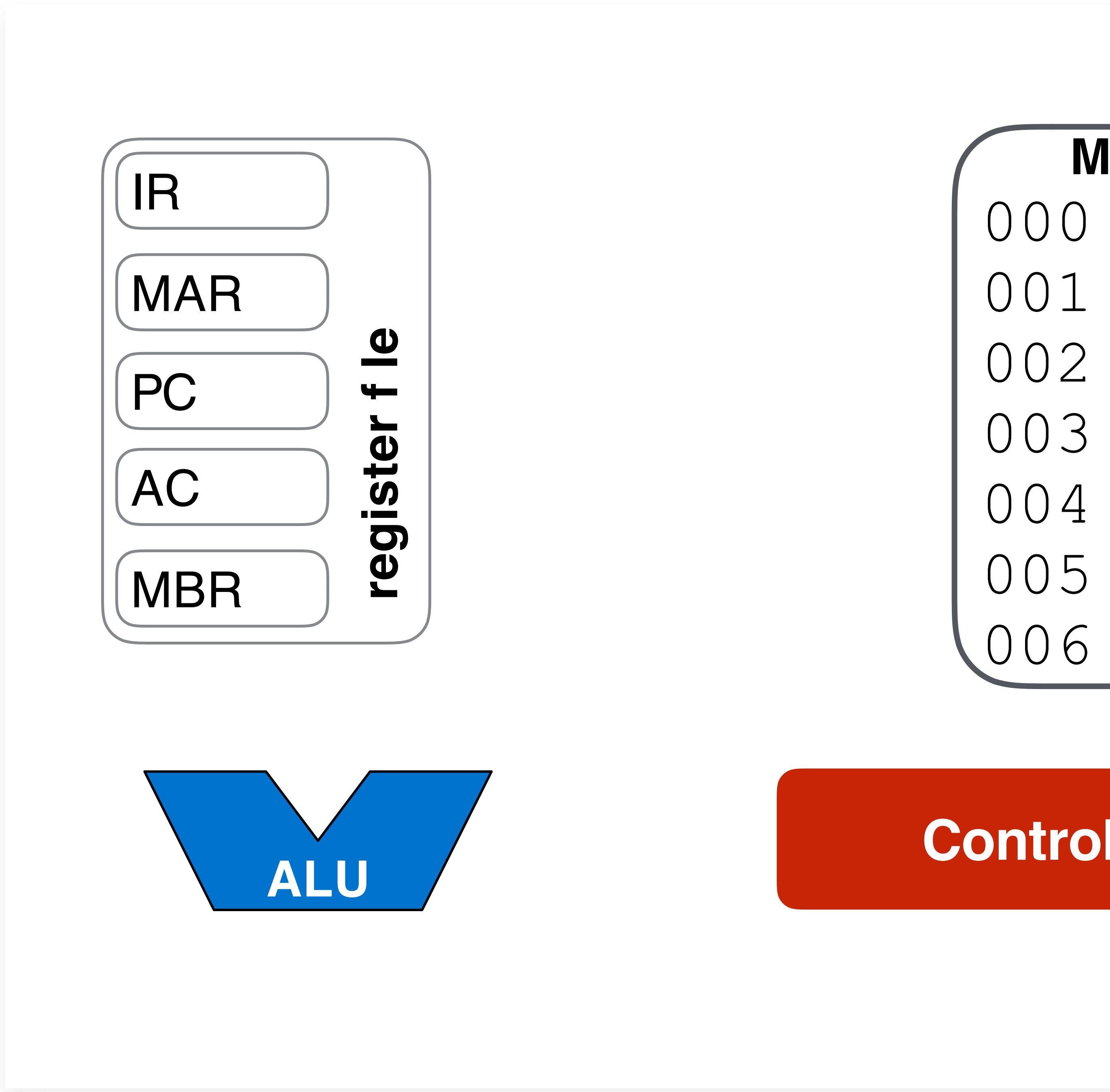

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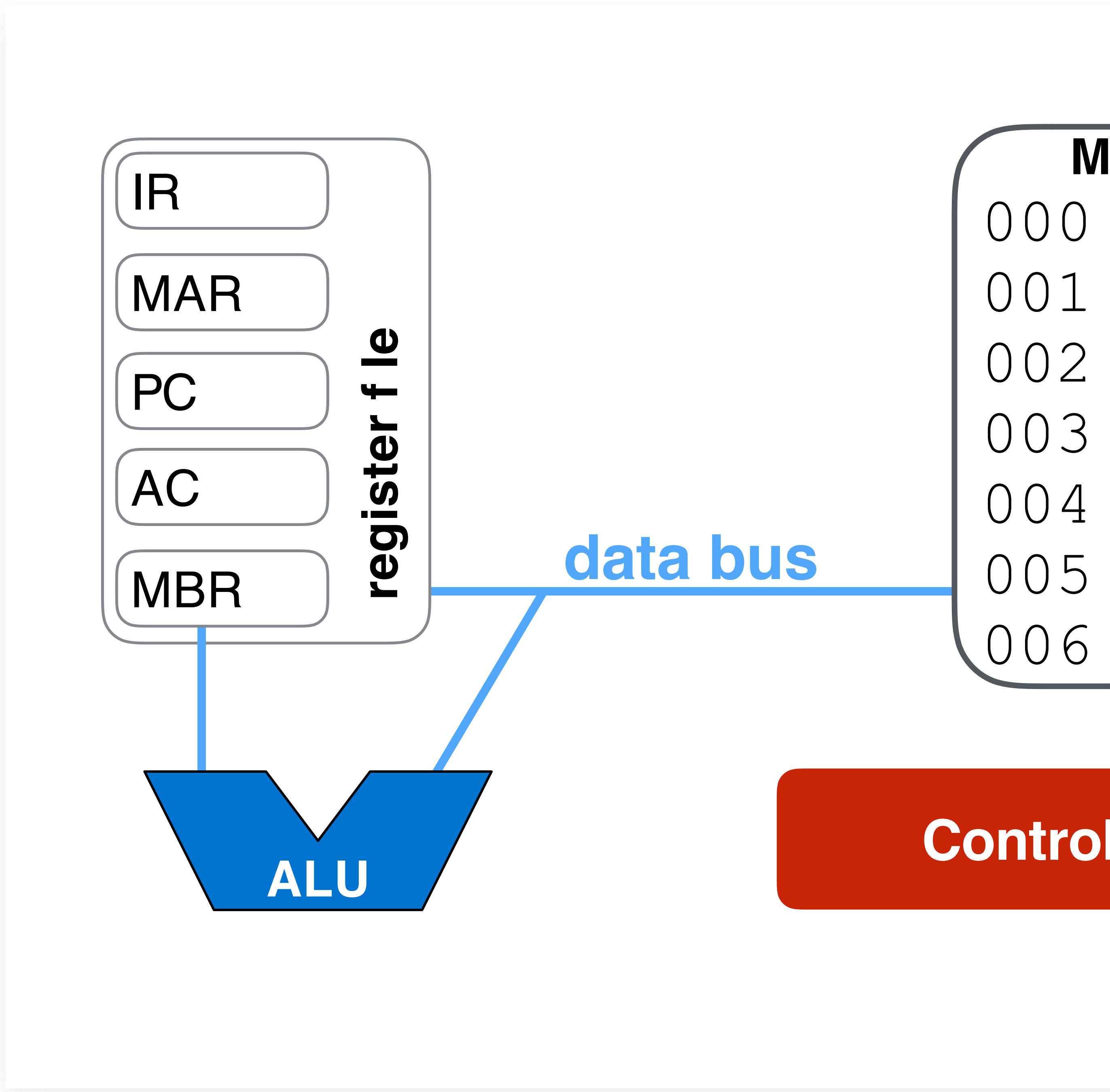

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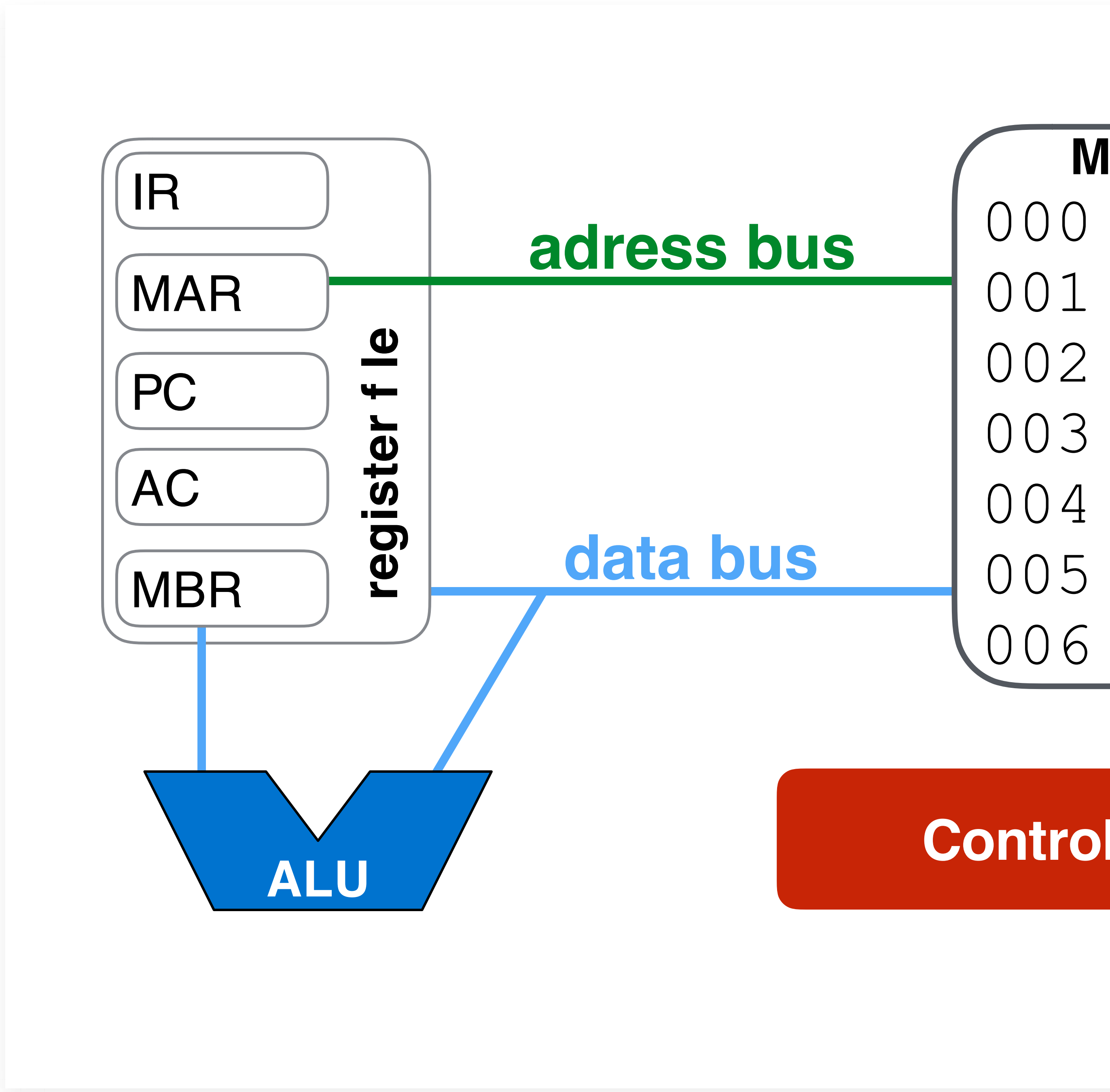

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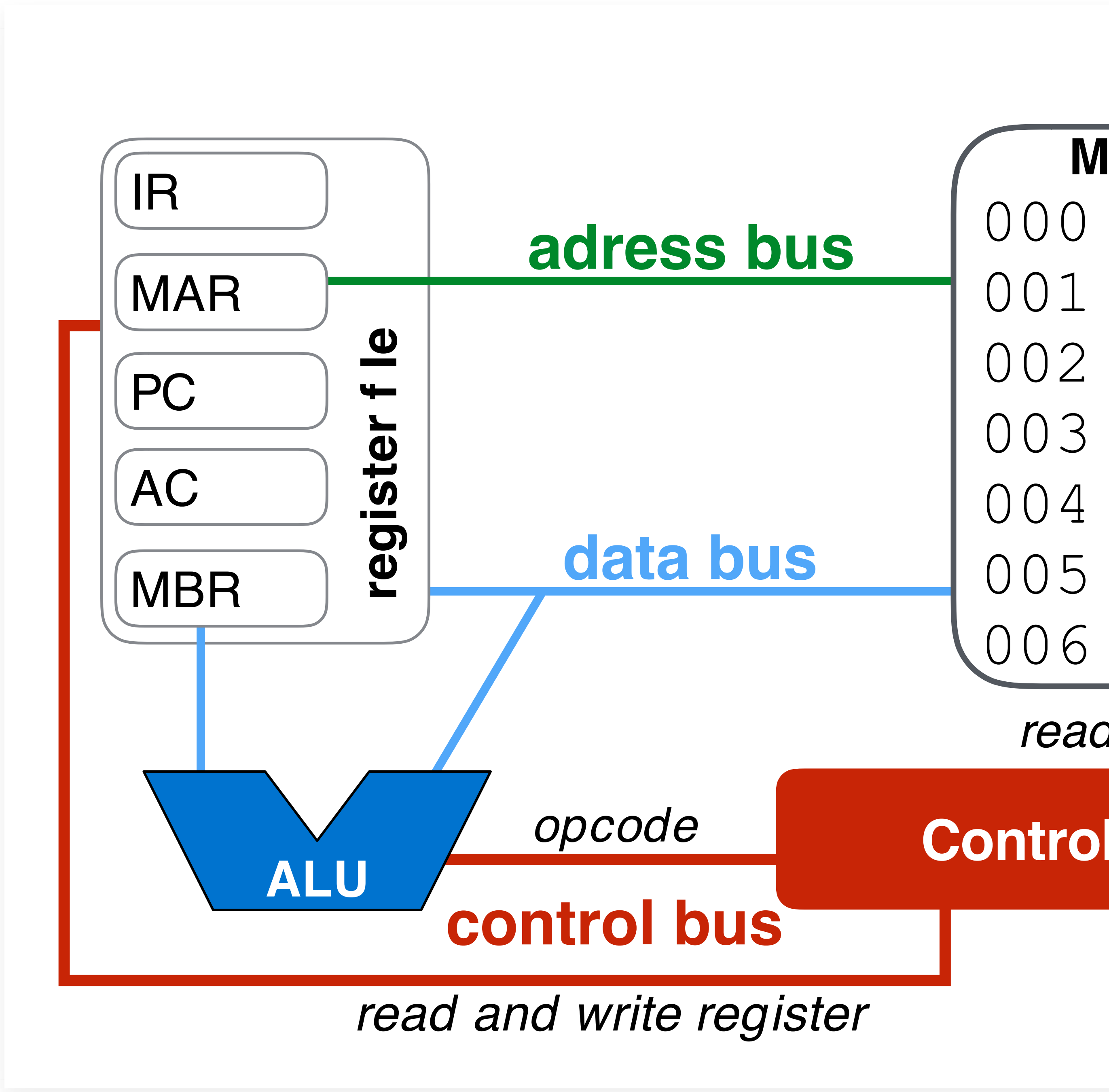

Next lectures