Saturday, April 25, 2015

How to use the interface ?

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1. What is interface file ?

The interface file is “m_if_router_v3.v”. It could be used to interface with the NoC network provided in the blackboard.

2. How to connect it to network and how can I connect my processing element to it ?

The connection diagram is provided in “Connection_and_timing_requirement”. Please follow strictly the way these modules are connected.

3. How to send a packet to the interface ?

The timing relation is given in the same pdf file. Basically, the sending is done by a simple “Req-Ack” fashion. Whenever you send a packet to the interface, you should first set the “i_comm_send_req” as 1’b1 and wait for “o_comm_send_ack” to be 1’b1. If this signal turns 1’b1, you should first set “i_comm_send_req” back to 1’b0. Then you could send the data(32-bit wide flit) via “i_data” cycle by cycle. Meanwhile, “i_data_valid” should be also set as 1’b1 to cover all the data to be sent(i.e., the length of valid “i_data_valid” is the same as valid “i_data”). As long as “o_comm_send_ack” is 1’b0, you should keep “i_comm_send_req” as 1’b1. You could not send any data and should wait until “o_comm_send_ack” turns 1’b1.

Of note, the longest packet should not exceed 16 flits and each flit is 32-bit wide.

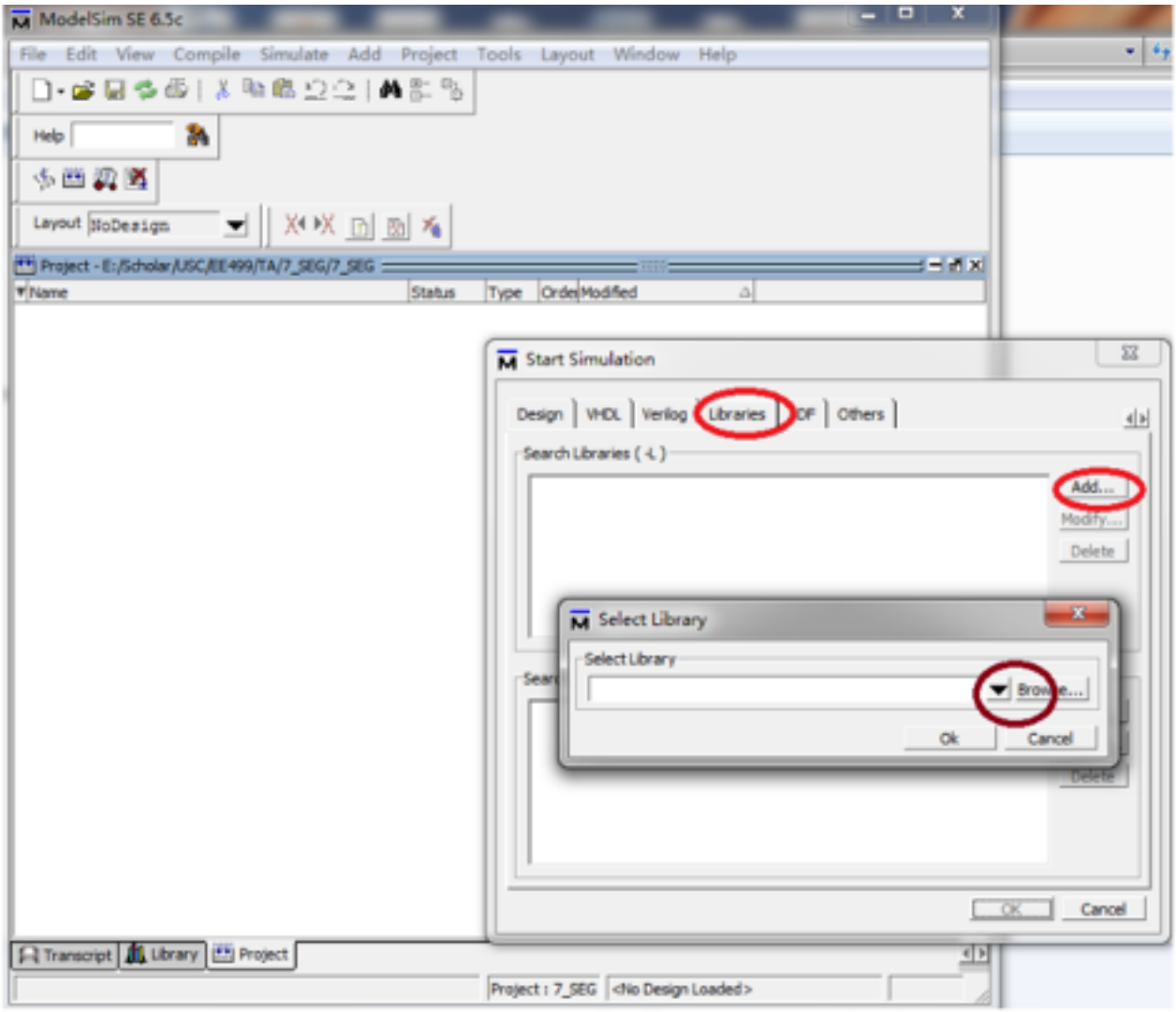
4. How can I get a packet from network ?

You can check the port “recv_ports_X_getFlit”(X is the port ID) and see if its MSB is 1’b1. If so, then the least significant 32 bits are the valid data from the network.

5. How to simulate with the interface provided ?

Since this network interface is using some library from Xilinx. So you need to add some libraries to the Modelsim when you are simulating with it. Here is how you could do it:

- 1. First include the “glbl.v, input_queue_fifo.v, output_queue_fifo.v, vc_fifo.v” as part of your design in the Modelsim
- 2. Press “Start simulation” and add libraries provided(“simprims”,”unisims,”XilinxCoreLib””) as shown below:


ModelSim SE 6.5c
File Edit View Compile Simulate Add Project Tools Layout Window Help
Help
Layout NoDesign
Project - E:/Scholar/USC/EE499/TA/7_SEG/7_SEG
Name Status Type Order Modified
Start Simulation
Design VHDL Verilog Libraries SDF Others
Search Libraries (4)
Add...
Modify...
Delete
Select Library
Select Library
Browse...
Ok
Cancel
OK
Cancel
Transcript Library Project
Project : 7_SEG
<No Design Loaded>