Exercise 6.4 Consider, again, the inverter circuit shown in Figure 6.4. The MOSFET has a threshold voltage $V_T = 2V$. Assume that $V_S = 5V$ and $R_L = 10k$. For this exercise, model the MOSFET using its switch-resistor model. Assume that the on-state resistance of the MOSFET is $R_{ON} = 8k$.

a) Does the inverter satisfy the static discipline which has voltage thresholds given by $V_{OL} = V_{IL} = 1V$ and $V_{OH} = V_{IH} = 4V$? Explain.

b) Does the inverter satisfy the static discipline for the voltage thresholds $V_{OL} = V_{IL} = 2.5V$ and $V_{OH} = V_{IH} = 3V$? Explain.

c) Draw the input versus output voltage transfer curve for the inverter.

d) Is there any value of V_{IL} for which the inverter will satisfy the static discipline? Explain.

e) Now assume that $R_{ON} = 1k$ and repeat parts (a), (b), and (c).

Solution:

a) First find the relevant threshold output and input values for the inverter:

The output high voltage is 5.

The output low voltage is

$$V_S \cdot \frac{R_{ON}}{R_{ON} + R_L} = 5 \cdot \frac{8}{18} = 2.2$$

The lowest input voltage recognized as a logical 1 is

$$V_T = 2V$$

The highest input voltage recognized as a logical 0 is less than $2V$.

With $V_{OL} = V_{IL} = 1V$ and $V_{OH} = V_{IH} = 4V$:

No, the static discipline is not satisfied. A failure case is for an input voltage which is greater than $V_{OH} = 4V$ (i.e., a valid 1). Since this high input voltage is greater than the threshold, the inverter output voltage is 2.2V, which is greater than $V_{OL} = 1V$. But this is not a valid 0. Valid 0 outputs would be outputs that are less than 1V.

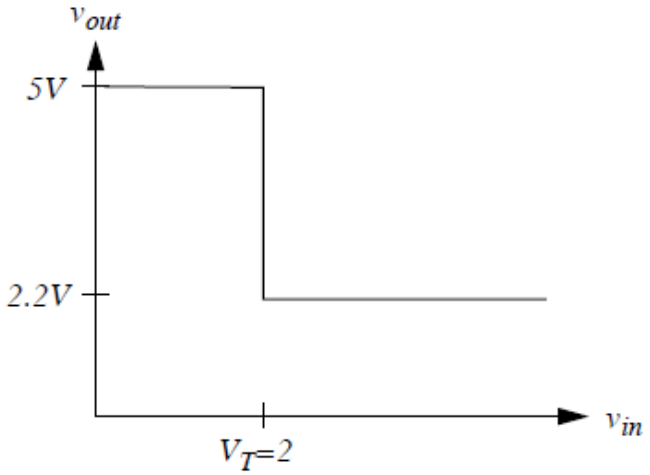

Figure 6.7:

b) With $V_{OL} = V_{IL} = 2.5V$ and $V_{OH} = V_{IH} = 3V$:

No. Now we have a failure case when the input is, say, 2.3V (i.e., a valid 0). But since $2.3 > V_T$, the output will be 2.2V. For a valid inverter the output should have been a valid 1. Thus, this violates the inverter's static discipline.

c) See Figure 6.7 for transfer curve.

d) No. The lowest value the inverter output ever reaches is 2.2V, which is still higher than 2V. Thus the inverter output can never turn the MOSFET in a receiving inverter off. This implies that we will never be able to satisfy the discipline.

e) a) $R_{ON} = 1k$

$$V_{OL} = V_S \cdot (\frac{R_{ON}}{R_{ON} + R_L}) = 5 \cdot \frac{1}{11} = 0.45$$

With $V_{OL} = V_{IL} = 1V$ and $V_{OH} = V_{IH} = 4V$:

Yes, we satisfy the static discipline. For valid 0 input ($< V_{IL}$), then output is always a valid 1 ($> V_{OH}$). For valid 1 input ($> V_{IH}$), the output is always a valid 0 ($< V_{OL}$).

b) With $V_{OL} = V_{IL} = 2.5V$ and $V_{OH} = V_{IH} = 3V$:

No. Counter case is if the input is 2.3V which is $< V_{IL}$ (valid 0), then it will produce an output 0 as well (i.e., $< V_{OL}$).

c) See Figure 6.8 for transfer curve.

ANS:: (a) no (b) no (d) no (e-a) yes (e-b) no

Exercise 6.5 Compute the worst-case power consumed by the inverter shown in Figure 6.4. The MOSFET has a threshold voltage $V_T = 2V$. Assume that $V_S = 5V$ and $R_L = 10k$. Model the MOSFET using its switch-resistor model, and assume that the on-state resistance of the MOSFET is $R_{ON} = 1k$.

Solution:

Power dissipated:

$$\begin{aligned} Power = V_S I &= \frac{V_S^2}{R_L + R_{ON}} \\ &= 5^2 \cdot (\frac{1}{(10+1)10^3}) \\ &= 2.27mW \end{aligned}$$

ANS:: 2.27 mW

Problem 6.1

a) Write a truth table and a boolean equation relating the output Z to A, $\overline{A}$, B, and C, when these are input to the circuit shown in Figure 6.10.

b) Suppose the circuit in Figure 6.10 suffers a manufacturing error which results in a short between the pair of wires depicted in Figure 6.11. Write a truth table and a boolean equation relating the output Z to A, $\overline{A}$, B, and C, for the resulting circuit.

Solution:

A	$\overline{A}$	B	C	Z
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0

A	$\overline{A}$	B	C	Z
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0

ANS:: (a) $Z = \overline{A + B}$ (b) $Z = \overline{A + B + C}$

Problem 6.3 Consider a family of logic gates which operates under the static discipline with the following voltage thresholds: $V_{OL} = 1$ V, $V_{IL} = 1.3$ V, $V_{OH} = 4$ V, and $V_{IH} = 3$ V. Consider the N-input NAND gate design shown in Figure 6.13. In the design $R = 100k$ and R_{ON} for the MOSFETs is given to be $1k$. V_T for the MOSFETs is 1.5V. What is the maximum value of N for which the NAND gate will satisfy the static discipline? What is the maximum power dissipated by the NAND gate for this value of N?

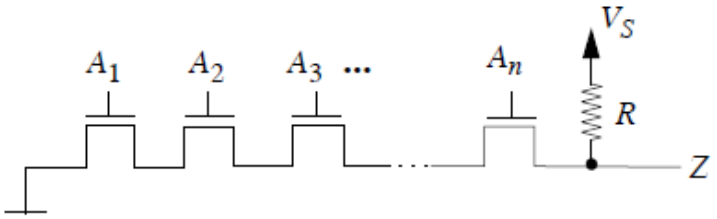

Figure 6.13:

Solution:

Voltage value at Z will equal V_S during a logical 1. During a logical 0, V_S is divided between N R_{ON} and R. Therefore, we require

$V_{Z=0} \leq V_{OL}$

$V_{Z=0} = V_S * \frac{N*R_{ON}}{N*R_{ON}+100k} \leq 1V$

$(V_S - 1)NR_{ON} \leq 100k$

$N \leq \frac{100k}{(V_S-1)R_{ON}}$

Maximum power dissipation when all switches on.

$P_{MAX} = \frac{V_S^2}{100k+NR_{ON}}$

ANS:: $N = \frac{100k}{(V_S-1)R_{ON}}$, $P_{MAX} = \frac{V_S^2}{100k+NR_{ON}}$