Hyunsu Chae

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EDUCATION

The University of Texas at Austin — Doctor of Philosophy in Electrical and Computer Engineering — Expected 05/2025
Advisor: David Z. Pan, since Fall 2021

Coursework Includes: VLSI Physical Design Automation, VLSI, Data Science Lab, Verification of Digital Systems, High-Speed Computer Arithmetic, Dependable Computing, Real-Time Operating Systems, Computer Architecture, Advanced MCU Systems

Sungkyunkwan University (Seoul, Republic of Korea) — Bachelor of Science in Semiconductor Systems Engineering — 03/2013 - 02/2018
Overall GPA: 4.27/4.50 (Second Highest-Ranked Graduate)

PUBLICATION

- Hyunsu Chae, Hao Yu, Sensen Li and David Z. Pan, "PulseRF: Physics-Augmented ML Modeling and Synthesis for High-Frequency RFIC Design," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Newark, NJ, Oct 27-31, 2024 (accepted).
- Hyunsu Chae, Keren Zhu, Bhyrav Mutnury, Zixuan Jiang, Daniel de Araujo, Doug Wallace, Doug Winterberg, Adam Klivans and David Z. Pan, "ISOP-Yield: Yield-Aware Stack-Up Optimization for Advanced Package using Machine Learning," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Incheon, S. Korea, Jan 22-25, 2024.
- Hyunsu Chae, Keren Zhu, Bhyrav Mutnury, Douglas Wallace, Douglas Winterberg, Daniel de Araujo, Jay Reddy, Adam Klivans, and David Z. Pan, "ISOP+: Machine Learning- Assisted Inverse Stack-Up Optimization for Advanced Package Design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Jan. 2024.
- Hyunsu Chae, Bhyrav Mutnury, Douglas Wallace, Douglas Winterberg, Arun Chada, Adam Klivans, and David Z. Pan, "Method of Exploring HVM Process Corner Cases for Loss and Impedance in High Speed Designs," *IEEE Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)*, Milpitas, CA, Oct. 15-18, 2023.
- Hyunsu Chae, Bhyrav Mutnury, Keren Zhu, Douglas Wallace, Douglas Winterberg, Daniel de Araujo, Jay Reddy, Adam Klivans and David Z. Pan, "ISOP: Machine Learning Assisted Inverse Stack-Up Optimization for Advanced Package Design," *IEEE/ACM Design, Automation and Test in Europe (DATE)*, Apr. 17 - Apr. 19, 2023.
- Hyunsu Chae, and Joon-Sung Yang, "Test Cost Reduction for X-Value Elimination by Scan Slice Correlation Analysis," *Proceedings of the 55th Annual Design Automation Conference (DAC)*, No.78, June 2018.

HONORS AND AWARDS

- 2023 Cadence Diversity in Technology Scholarship – Woman in Technology
- 2018 DAC A. Richard Newton Young Student Fellow
- 2013-2018 Samsung Electronics Semiconductor Scholarship for Undergraduate Study

TECHNICAL SKILLS

Programming Python, C/C++, Verilog, System Verilog, VHDL, MATLAB, MIPS assembly
EDA Tools Cadence Tools (Innovus, Virtuoso, JasperGold), Synopsys Tools (Design Compiler, IC Compiler, VCS, HSpice, PrimeTime, DFT Compiler, TetraMAX ATPG), SIS, Modelsim, PSpice, LTSpice

RESEARCH PROJECTS

Inverse Design of RFIC using ML — *UTDA Lab (Professor David Z. Pan)* — 08/2023 – Current

- Leading efforts in the design and optimization of RFIC components in collaboration with Professor Sensen Li's group
- Implementing and experimenting with innovative ML techniques for physics-driven ML modeling and investigating large design space exploration problems for different RFIC design

ML-Assisted Advanced Packaging/Interconnect Optimization — *UTDA Lab (Professor David Z. Pan)* — 01/2022 – 07/2023

- Proposed a fully automated design methodology for advanced packaging interconnect design to optimize signal performance and ensure signal integrity in high-frequency setting
- Leveraging ML techniques for multi-objective and non-convex problems faced in advanced packaging design
- Developed methods for enhancing the robustness of the design by accounting for the manufacturing process design variance and fast and efficient yield analysis technique

Formal/Semi-Formal Verification of Cache Coherency Protocol — *(Professor Jacob Abraham)* 06/2020 – 12/2020

- Explore MESI cache coherency protocol and formal verification methods using SystemVerilog and Cadence JasperGold
- Develop an effective semi-formal verification method for cache coherency checks and experiment with iterative improvements

SKKU: Undergraduate Research Assistant — *Design and Test for Systems Lab (Professor Joon-Sung Yang)* 08/2016 – 07/2018

- Developed method for optimization in scan testing that improved performance by reducing data volume and test time
- Led a team for the Undergraduate Research Program (URP) sponsored by the Korea Foundation for the Advancement of Science and Creativity. Selected as one of the top ten teams in the field and was awarded with research funding

INDUSTRY INTERNSHIP EXPERIENCE

Cadence Design Systems: Cadence MSA R&D team 05/2024 – 08/2024

- Developed inverse design framework for power delivery network using image-to-image ML model and Bayesian optimization
- Utilized Cadence Innovus, Voltus, and PSDL tools to generate various floorplanning and power grid designs for creating a comprehensive ML training dataset
- Designed and adapted UNet and Fourier Neural Operator (FNO) models to predict power grid performance metrics, including the effective resistance of VDD and VSS

Dell Technologies: Signal integrity team 05/2022 – 08/2023

- Developed an ML-assisted inverse optimization framework for high-speed PCB design, which enabled x60 speedup compared to the conventional manual design flow with increased efficiency. This framework can be use by anyone without prior knowledge and customizable for various PCB interconnect design applications
- Investigated and evaluated different ML models and hyper-parameter optimization algorithms for tabular dataset
- Elevated design robustness by creating a method for corner case modeling for PCB interconnect structures

Intel Corporation: Atom CPU FV team 06/2020 – 08/2021

- Developed a formal verification environment to enable reusable validation for a cache eviction protocol
- Evaluated emerging microprocessor designs by discovering bugs using Cadence JasperGold and formal verification techniques

TEACHING EXPERIENCE

UT Austin: Graduate Teaching Assistant — *E E 460R/382M VLSI 1* 08/2019 – 12/2019, 08/2021 – 12/2021

- Led lab sessions on physical design and synthesis based on common industry design practices and CAD tools
- Provided teaching support on topics such as advanced circuit design techniques, timing/power analysis, and RTL system design

UT Austin: Graduate Teaching Assistant — *E E 382M Verification of Digital Systems* 01/2020 – 06/2020

- Led lab sessions covering verification methods such as LEC, UVM and Formal Verification and their industrial tools

UT Austin: Graduate Teaching Assistant — *E E 306 Introduction to Computing* 08/2018 – 12/2018

- Instructed weekly lab sessions on fundamental topics in computer architecture, operating systems, and algorithm design