HYUNSU CHAE

hyunsu.chae@utexas.edu • linkedin.com/in/hyunsu-chae • (737) 218-2349

EDUCATION

The University of Texas at Austin
Doctor of Philosophy in Electrical and Computer Engineering — 08/2018 – Present
Advisor: David Z. Pan

Master of Science in Electrical and Computer Engineering — 08/2018 – Present
Coursework Includes: VLSI Physical Design Automation, VLSI, High Speed Computer Arithmetic, Verification of Digital Systems, Dependable Computing, Real-Time Operating Systems, Data Science Lab, Computer Architecture, Advanced MCU Systems

Sungkyunkwan University (Seoul, Republic of Korea)
Bachelor of Science in Semiconductor Systems Engineering — 03/2013 – 02/2018
Overall GPA: 4.27/4.50 (Second Highest-Ranked Graduate)
Honors: Samsung Electronics Semiconductor Scholarship

PUBLICATION

- Hyunsu Chae, Bhyrav Mutnury, Keren Zhu, Douglas Wallace, Douglas Winterberg, Daniel de Araujo, Jay Reddy, Adam Klivans and David Z. Pan, "ISOP: Machine Learning Assisted Inverse Stack-Up Optimization for Advanced Package Design," *IEEE/ACM Design, Automation and Test in Europe (DATE)*, Apr. 17 - Apr. 19, 2023. (accepted)
- Hyunsu Chae, and Joon-Sung Yang, "Test Cost Reduction for X-Value Elimination by Scan Slice Correlation Analysis," *Proceedings of the 55th Annual Design Automation Conference (DAC)*, No.78, June 2018.

TECHNICAL SKILLS

Programming Python, C, Verilog, System Verilog, VHDL, MATLAB, MIPS assembly
Tools Cadence Tools (JasperGold, Virtuoso), Synopsys Tools (Design Compiler, IC Compiler, VCS, HSpice, PrimeTime, DFT Compiler, TetraMAX ATPG), SIS, Modelsim, PSpice, LTSpice

WORK EXPERIENCE

Dell Technologies: Graduate Intern — 05/2022 – 08/2022
- Developed an ML-assisted automated optimization framework for high-speed PCB design, allowing for faster and more efficient stack-up design process compared to manual design process commonly used in the industry
- Investigated and evaluated different ML models and hyper-parameter optimization algorithms for given application.

Intel Corporation: Graduate Validation Intern — 06/2020 – 08/2021
- Developed a formal verification environment to enable reusable validation for a cache eviction protocol
- Evaluated emerging microprocessor designs by discovering bugs using Cadence JasperGold and formal verification techniques

RESEARCH PROJECTS

Interconnect Technology Optimization – *UT Design Automation Lab (Professor David Z. Pan)* — 01/2022 – Current
- Proposed a fully automated design methodology for advanced packaging stack-up to optimize signal performance by minimizing signal insertion loss and crosstalk for a given target characteristics impedance
- Working on improving hyper-parameter optimization algorithm and extending the work to multi-layer stack-up design to enable the optimization beyond cross-sectional objectives
- Exploring the possibility of extending optimization target to package via design

Formal/Semi-Formal Verification of Cache Coherency Protocol — 06/2020 – 12/2020
- Explore MESI cache coherency protocol and formal verification methods using SystemVerilog and Cadence JasperGold
- Develop an effective semi-formal verification method for cache coherency checks, and experiment with iterative improvements

SKKU: Undergraduate Research Assistant – *Design & Test for Systems Lab (Professor Joon-Sung Yang)* — 08/2016 – 07/2018
- Published research findings in 55th Annual Design Automation Conference
- Developed method for optimization in scan testing that improved performance by reducing data volume and testing time
- Sponsored by the Korea Foundation for the Advancement of Science and Creativity and awarded research support

TEACHING EXPERIENCE

UT Austin: Graduate Teaching Assistant – *E E 460R/382M VLSI 1* — 08/2019 – 12/2019, 08/2021 – 12/2021
- Led lab sessions on physical design, cost analysis, and synthesis, based on common industry design practice using CAD tools
- Provided teaching support on topics such as advanced circuit design techniques, timing/power analysis, and RTL system design

UT Austin: Graduate Teaching Assistant – *E E 382M Verification of Digital Systems* — 01/2020 – 06/2020
- Led lab sessions covering verification methods such as LEC, UVM and Formal Verification and their industrial tools

UT Austin: Graduate Teaching Assistant – *E E 306 Introduction to Computing* — 08/2018 – 12/2018
- Instructed weekly lab sessions on fundamental topics in computer architecture, operating systems, and algorithm design