Rapid MOSFET Contact Resistance Extraction From Circuit Using SPICE-Augmented Machine Learning Without Feature Extraction

Thomas Lu, Varada Kanchi, Kashyap Mehta, Sagar Oza, Tin Ho, and Hiu Yung Wong, *Senior Member, IEEE*

***Abstract*— It is desirable to monitor the degradation of integrated circuits (ICs) or perform their failure analysis through their electrical characteristics [such as the voltage-transfer characteristic (VTC), of an inverter]. Such a method is nondestructive, low-cost, and can be applied to a large number of samples. Machine learning is naturally an excellent tool to perform this task. However, it is very expensive, in terms of time and cost, to generate enough experimental data with well-controlled defects to train a reliable machine. Moreover, IC defect signatures and features are usually embedded in the hyperspace of their electrical characteristics and are difficult to extract. In this article, we propose to use dimensionality reduction to extract the defect signature from the IC electrical characteristics using data generated through simulations. A CMOS inverter is used for demonstration. The drain contact resistances, which can increase due to defect or degradation, of the nMOSFET and pMOSFET in an inverter are extracted using a machine based on autoencoder (AE). The machine is trained using data generated from SPICE simulation. The machine is then tested using experimental data and high accuracy is obtained ($R^2 > 0.9$). In particular, for the first time, through the analysis of the hidden variables, we demonstrate that the machine has effectively extracted the features automatically which obviates the cumbersome feature extraction process.**

***Index Terms*— Autoencoder (AE), CMOS inverter, contact resistance, defects, machine learning, reverse engineering, SPICE simulation.**

I. Introduction

DEFECT identification [1] and reverse engineering [2] are the daily routines in semiconductor manufacturing and fabrication processes. They rely heavily on destructive and expensive, in terms of cost and time, failure analysis (FA) tools such as SEM [3] and TEM [4]. As Moore's law reaching its end [5], fabrication processes become more complicated using emerging 3-D structures, such as FinFET, stacked nanosheet, and complimentary FET [6]–[8], and the demand for rapid FA increases. Moreover, since the parasitic resistance and capacitance start dominating in highly scaled devices in the Design-Technology Cooptimization (DTCO) era [9], the understand and analysis of the parasitic components and their degradation also become more important. Contact resistance is one of the most important parasitic components which needs special attention [10], [11]. Contact resistance control is also important to the success of emerging memories [12].

To meet the increasing demand of FA, it is desirable to find a low-cost and high-throughput methodology to analyze, narrow down, or even pinpoint the defect properties qualitatively (e.g., identify the type of defects) and quantitatively (e.g., identify the contact location and its resistance value). One attractive proposal is to use the electrical characteristics to deduce the defect qualitatively and quantitively.

However, the electrical characteristics of devices (such as the Current–Voltage, I–V, and Capacitance–Voltage, C–V) and circuits [such as the voltage transfer characteristic (VTC) of an inverter or the butterfly curves of an static random access memory (SRAM)] usually are not explicitly correlated with the defect properties. Therefore, machine learning is proposed in [13]–[21] to learn the correlations. To use machine learning successfully, enough training data, i.e., electrical characteristics of devices/circuits with well-controlled defects, is required. This cannot be obtained easily and accurately through the experiment at a low cost. In [13], it is proposed to use Technology Computer-Aided Design (TCAD) to generate I–V curves of p-i-n diodes with various epitaxial thicknesses and doping and a machine is trained to deduce the thicknesses and doping based on the measured I–V. This is called TCAD-augmented machine learning. It is noted that no feature extraction is performed in [13] and this obviates domain expertise and the resources required in feature extractions. However, such an approach can lead to overfitting and cannot be used in experimental data due to the noise in the experimental I–V. Principal component analysis [14], noise technique [15],

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and autoencoder (AE) [16], [17] are proposed to solve the overfitting issue when domain expertise and feature extraction are not used. Among them, AE is the most promising in that it gives similar results as with feature extraction when applied to experimental data [17]. Moreover, it is shown that using the same AE architecture, one can apply to both I–V and C–V of FinFET without the need of performing separate feature extractions for the I–V and C–V curves [18]. It is noted that only [14] and [17] have the results verified with experimental data.

Based on the successful experience in using AE in TCAD-augmented machine learning, in this article, we applied a similar framework to extract the drain contact resistances of the nMOS and pMOS in an inverter based on its VTC. The drain contact resistance can be considered as a result of manufacturing defects [23] or degradation (e.g., due to radiation damage [24]). The training data are generated using SPICE simulation and the result is verified experimentally. This work has four major achievements. First, it shows that the concept of TCAD-augmented machine learning can be extended to other types of simulations (in this case, SPICE) directly. Second, it shows AE-based machine is applicable also to circuit electrical characteristics without the need for architectural change. Third, this is the first time to verify a SPICE-augmented machine learning on a circuit using experimental data. Last, through hidden node analysis, we show that the machine has successfully performed accurate feature extraction automatically. It should also be noted that feature extraction in [17] for TCAD-augmented machine learning is relatively easy. However, in the VTC case, the extraction of features based on VTC is far from trivial.

It is worth noting that there were also efforts in the literature to use TCAD trained data to deduce silicon on insulator (SOI) breakdown voltage (BV) properties [19], nanowire properties [20], and SRAM defects locations [21], [22]. However, feature extractions are used and they have not been verified using experimental data (i.e., the trained machines are tested using unseen TCAD data only).

II. Overview

The idea of this article can be used in the common scenario in a fab as illustrated in Fig. 1. The goal is to use SPICE simulation to rapidly generate circuit electrical characteristics (e.g., VTC of an inverter) with variations of the parameters in interest (e.g., drain contact resistances) to train a machine without feature extraction. Circuit measurements on the wafer level are then fed into the machine to deduce the distribution of the parameters, which is then compared to any existing process wafer maps [e.g., contact hole critical dimension (CD)] for correlations to understand the source of defects. To demonstrate this, inverter and drain contact resistance are the circuit and parameters in interest, respectively. Inverters with various contact resistances are first measured experimentally (Section III). SPICE simulations with contact resistance variations are conducted to generate training data (Section IV) and a machine is trained (Section V) to deduce the contact resistances for any given measured VTC.

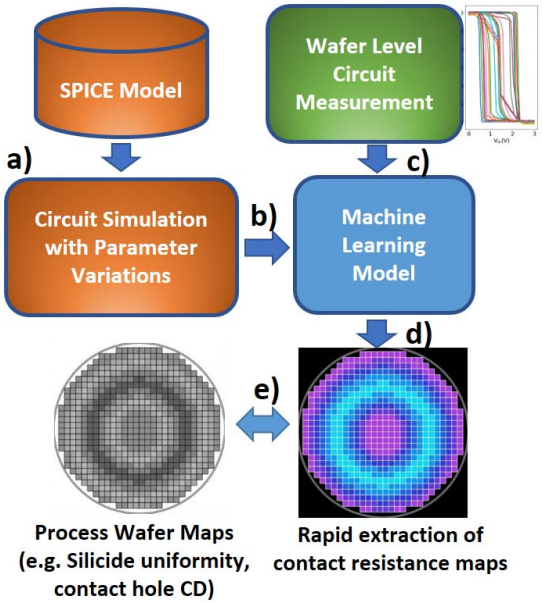

Fig. 1. Overview of the application of this study. (a) SPICE circuit simulations and (b) are performed to generate data to build a machine, without feature extraction. (c) Wafer-level measurement, e.g., VTC of an inverter, are fed into the machine, (d) which can deduce the contact resistances distribution on the wafer level, and (e) can be used to compare to process wafer maps to identify the defect root cause.

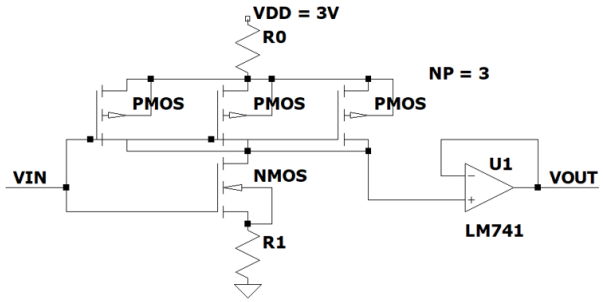

Fig. 2. Schematic circuit of the experiment. NP = 3 case is shown.

III. Experiment Setup

The inverter is constructed using commercial-off-the-self (COTS) pMOS and nMOS in ALD1103 by Advanced Linear Devices, Inc., fabricated using enhanced advanced complementary metal-oxide-semiconductor (ACMOS) silicon gate CMOS process [25]. Discrete resistors with accuracy better than 10% are used to model the *extra* drain contact resistance of pMOS and nMOS due to defect or degradation. They are labeled as R_0 and R_1, respectively. Fig. 2 shows the schematic of the setup. A USB-powered data acquisition module, ADALM2000 by Analog Devices [26] is used for biasing, input sweeping, and data acquisition. Since the input impedance of the sensing channel of ADALM2000 is only 1 MΩ, a unity gain buffer is added at the inverter output. V_{DD} is set to be 3 V.

The pMOS and nMOS are characterized by setting $|V_{GS}| = |V_{DS}| = V_{DD}/2 = 1.5$ V. The drain current, $|I_{DS}|$, is measured and their effective resistance, R_p for pMOS and R_n for nMOS, is found by 1.5 V/$|I_{DS}|$. It is found that $R_p = 2243\ \Omega$ and $R_n = 744\ \Omega$.

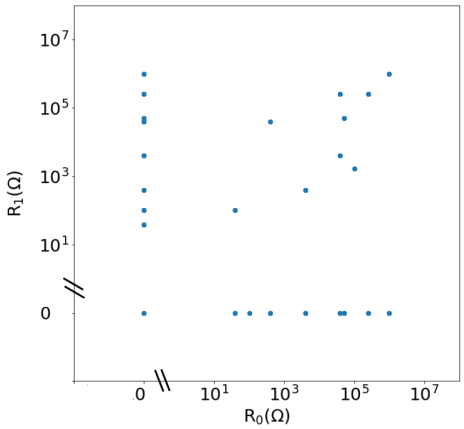

Fig. 3. Distribution of R_0 and R_1 pairs used to construct the inverter circuits for each NP group.

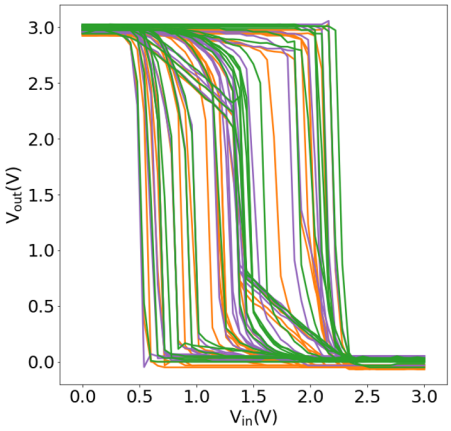

Fig. 4. VTCs of experimental inverter circuits with various R_0 and R_1. Three groups of circuits are identified. Orange: NP = 1. Purple: NP = 2, and Green: NP = 3.

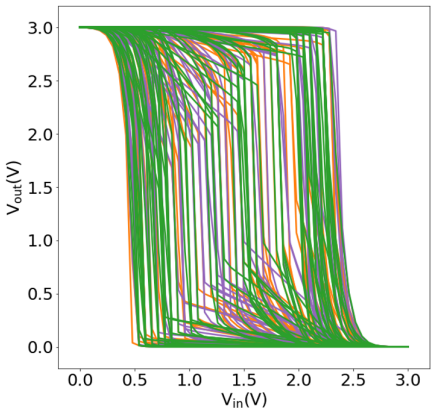

Fig. 5. Simulation VTCs. Three groups of inverter circuits are identified. Orange: NP = 1. Purple: NP = 2, and Green: NP = 3. Only 75 curves from each group are shown for clarity.

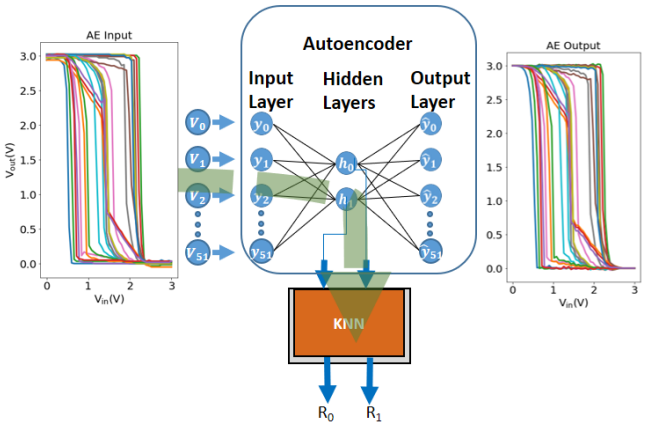

Fig. 6. AE-based machine used in this study. The machine has five hidden layers, each has 80, 50, 2, 50, and 80 nodes, respectively. For clarity, only the middle layer is shown. Each VTC is discretized into 51 points and encoded as two latent variables, h_0 and h_1. The machine is trained such that the output values equal the input values in the AE and h_0 and h_1 are correlated with R_0 and R_1 using KNN with $k = 3$.

Three sets of inverter experiments are then conducted. Each set uses one nMOS and NP pMOS in parallel, where NP = 1, 2, or 3. This represents three different types of inverter circuits. For example, in the set with NP = 3, it has three pMOS connected in parallel to represent an inverter with a stronger pMOS, i.e., the width is tripled. V_{in} is swept from 0 to 3 V and the V_{out} is measured to construct the VTC. Different values of R_0 and R_1, between 0 and 1 MΩ, are used with 0 representing no extra contact resistance. There are 25 circuits in each set of experiments. Fig. 3 shows the distribution of R_0 and R_1 used in the experiments. Fig. 4 shows the measured VTC of the circuits.

IV. Training Data Generation

The SPICE models of the pMOS/nMOS in ALD1103 are not provided by the vendor. To model the pMOS/nMOS in ALD1103, a SPICE LEVEL 3 model is created so that the threshold voltage and R_n and R_p match the experimental values. In any modern integrated circuit (IC) fabrication process, an accurate SPICE model is usually available and thus it is not necessary to perform this extra calibration. However, if it is a new process under development, the SPICE model might not be complete. It is thus important to show that using a primitive SPICE model (such as in our case) to generate simulation data is still useful in simulation augmented machine learning.

About 10 000 VTC curves are simulated using Cadence Specter [27] by varying R_0 and R_1 for each NP value. The resistance values vary from 10 Ω to 10 MΩ logarithmically. Fig. 5 shows 75 randomly selected simulation curves from each NP group.

V. Machine Learning

As shown in Figs. 4 and 5, it is not trivial to extract the features that are associated with R_0 and R_1. One possibility is to extract the V_M (i.e., $V_M = V_{in}|V_{in} = V_{out}$) and slopes of the regions before and after V_M which are affected not only by R_0 and R_1 but also R_n and R_p. As a result, for each set of inverters, one might need to reoptimize the feature extractions. Moreover, for small R_0 and R_1, the VTC is smoother but becomes more piecewise linear when R_0 and R_1 are large. Therefore, feature extractions require a lot of domain expertise

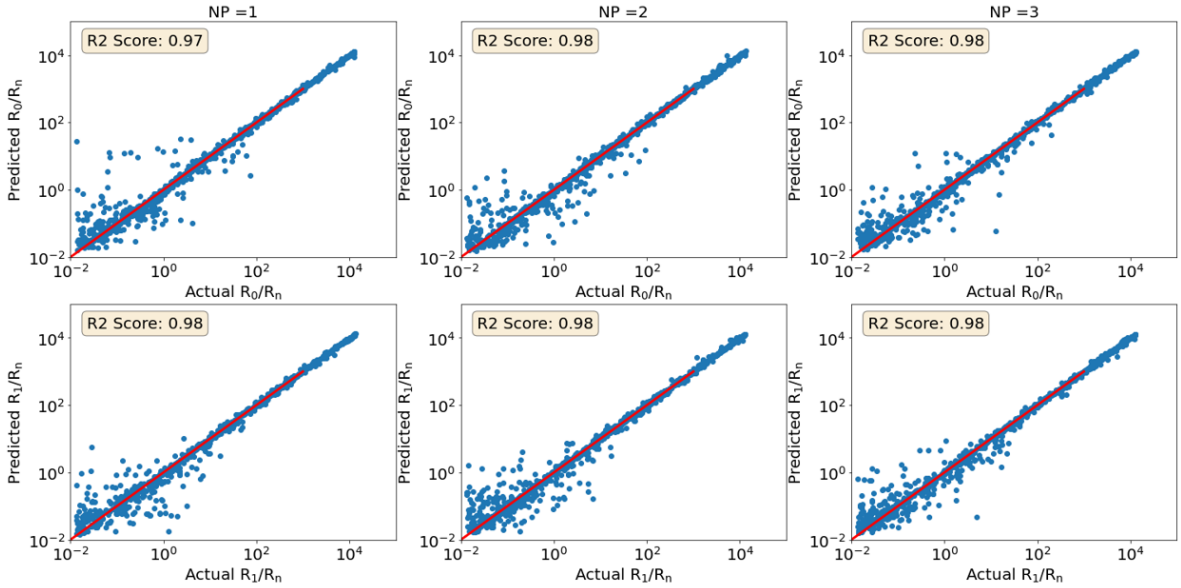

Fig. 7. Validation results of NP = 1, 2, 3 cases. R_0 and R_1 are normalized to R_n.

(knowledge of how the R_0, R_1, R_n, and R_p affect the shape of the VTC).

To obviate the cumbersome feature extraction and reextraction when different inverters are used, an AE-based machine is used in this study. AE [28], [29], a type of manifold learning algorithm, is capable of performing nonlinear dimensionality reduction of hyperspace data into latent variables. The VTC curves are the hyperspace representing the inverter configuration. Since in the simulation and experiment, only R_0 and R_1 are varied in each set of inverters, the VTC can be represented by a set of latent variables with much reduced dimensions. The latent variables can then be correlated with R_0 and R_1.

Fig. 6 shows the algorithm used and for clarity, only the middle hidden layer is shown. Tensorflow platform is used [30]. Each VTC is discretized into 51 points (y_0–y_{50}). An AE with five hidden layers is used. About 90% of the simulation curves are used as the training data and the rest are used for validation. The model is trained to have less than 5×10^{-5} mean-squared error loss by comparing the AE input (y_0–y_{50}) and output ($\hat{y}_0$–$\hat{y}_{50}$). A decaying learning rate scheme is used, in which the learning rate is gradually reduced from 0.001 before 50 epochs to 0.0002 after 1700 epochs. This is found to help avoid local minima in the optimization process. The number of nodes in each hidden layer is 80, 50, 2, 50, and 80, respectively, and node counts are manually adjusted to minimize loss.

The latent variables in the middle layer, h_0 and h_1, are correlated with R_0 and R_1 through the kth nearest neighbors (KNNs) algorithm with $k = 3$. Overfitting is monitored and avoided by tracking the validation loss and evaluating KNN performance once every 50 epochs. No overfitting occurs and 2000 epochs are used in the final model.

Fig. 7 shows that the model performs very well and the coefficients of determination [31], R^2, are very close to 1 for both validation and training (not shown) data.

After the machine is trained, experimental VTCs from Fig. 4 are then fed into the machine to deduce the R_0 and R_1 of the inverters, without any manual feature extraction. Fig. 8 shows that it can predict R_0 and R_1 very well with R^2 larger than 0.9.

VI. Discussion

We demonstrated experimentally that, without feature extraction, using AE, the drain contact resistances in an inverter can be deduced based on measured VTCs. Statistically, it deduces the extra resistance location (at pMOS, i.e., R_0, or at nMOS, i.e., R_1) and extra resistance values very well as shown in Fig. 8. In certain experiments, it can predict the abnormal resistance with values of only a few percentages of R_n well (e.g., R_1 in NP = 2 case in Fig. 8 even when $R_1/R_n < 10\%$), which is impossible in other FA methods. Overall, the AE can predict the trend fairly well even for small resistance (i.e., between $R_1/R_n > 1\%$ and $R_1/R_n < 100\%$) in all cases. This is particularly useful for high throughput wafer map analysis.

Although discrete components are used in the experiment, the transistors are made in a traditional CMOS IC process. Therefore, the experimental circuits constructed represent an IC inverter well. Such an approach also obviates the need to fabricate a test chip which might have a limitation on the number of probe pads. On the other hand, such a setup introduces more noises due to parasitic capacitance and resistance than a fully IC. Since dc measurement is performed, parasitic capacitance has minimal impacts. Parasitic resistance is also negligible as it is much lower than the MOSFET resistance which is further confirmed with the accuracy in the contact resistance prediction result. Such extra noise and nonideality are expected to make it more difficult to apply simulation augmented machine learning to the experimental data than if a fully integrated inverter were used. Since good

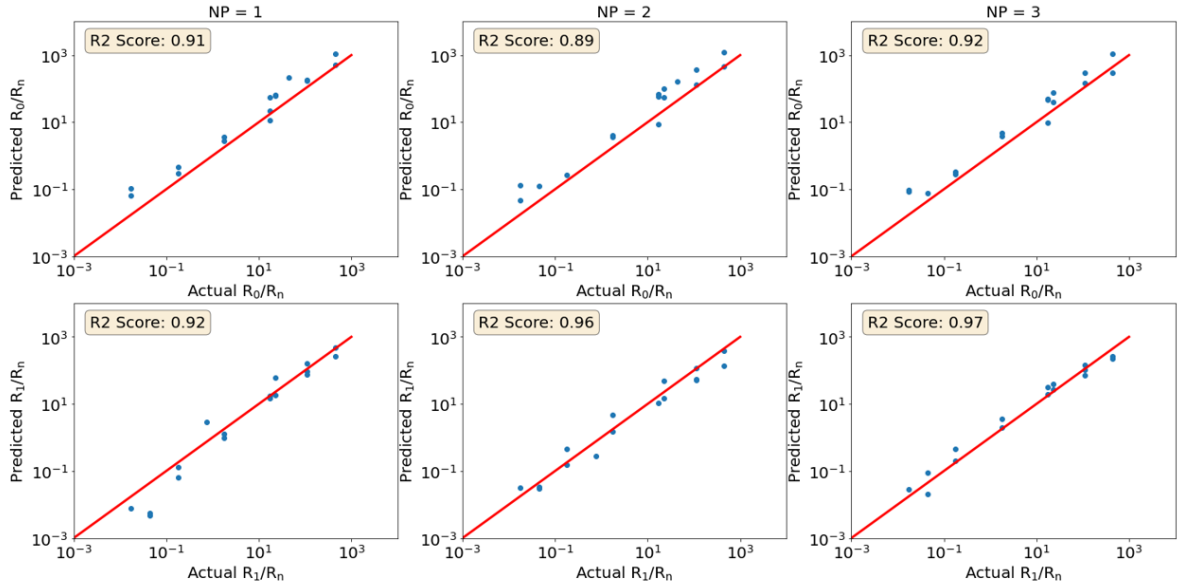

Fig. 8. Prediction of experimental R_0 and R_1. R_0 and R_1 are normalized to R_n.

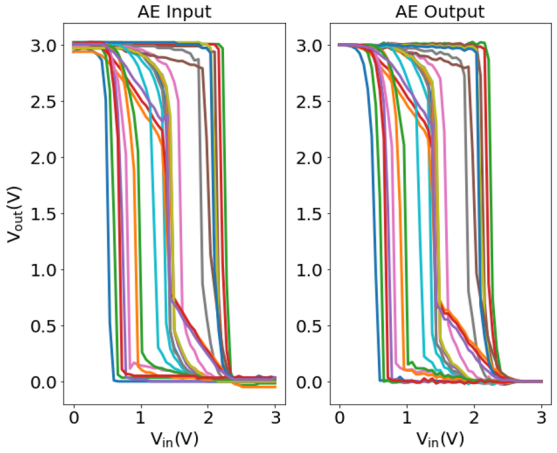

Fig. 9. Experimental VTCs input to the machine (left) and the VTCs output from the machine (right). NP = 3 is used.

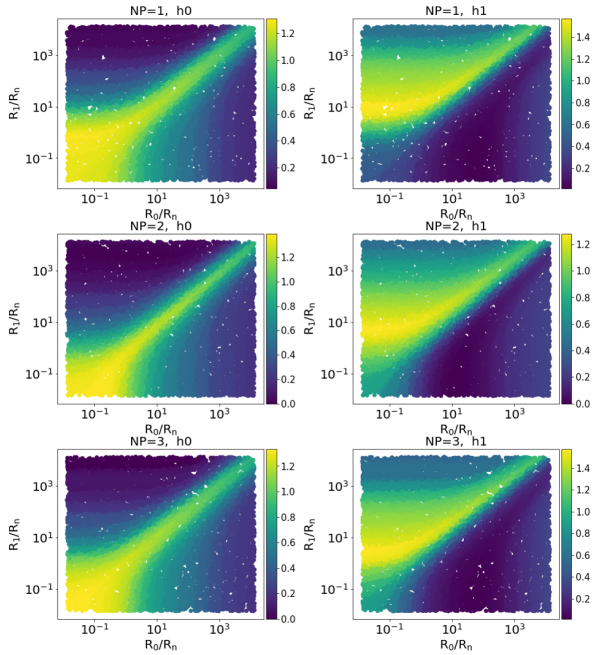

Fig. 10. h_0 and h_1 as the functions of R_0 and R_1 for NP = 1, 2, and 3.

results are obtained with the current experimental setup, it is expected that such a methodology will perform even better on fully ICs. This also shows that the AE can perform well even when unknown variations are present. Of course, if the unknown variations are comparable to the variations been investigated (i.e., R_0 and R_1 in this case), it is expected that the AE will not be able to perform as well. This can be solved by generating another model for the suspected new variations.

To further quantify the ability of the AE on performing accurate feature extraction, Fig. 9 shows the input and output of the AE. It is noted that the AE encodes the 51-D input data (y_0–y_{50}) to a 2-D space spanned by h_0 and h_1, which is then used to reconstruct the original curve as the output ($\hat{y}_0$–$\hat{y}_{50}$). As shown, the output resembles the input very well which means that the AE has successfully automatically extracted two features to represent the VTC.

Figs. 10 and 11 show the relationship between the latent variables and R_0 and R_1 for all three sets of inverters. It can be seen that all three different sets of inverters (NP = 1, 2, and 3), which have different V_M, show the same qualitative and very similar quantitative relationships between the contact resistances and the hidden variables. Therefore, the AE is repeatable in all three cases and has automatically extracted the features that faithfully represent the parameters, i.e., R_0 and R_1, that we are interested in.

The time required to perform 10 000 SPICE simulations for training data generation is less than 3 h with one Specter license and the time required to train the machine

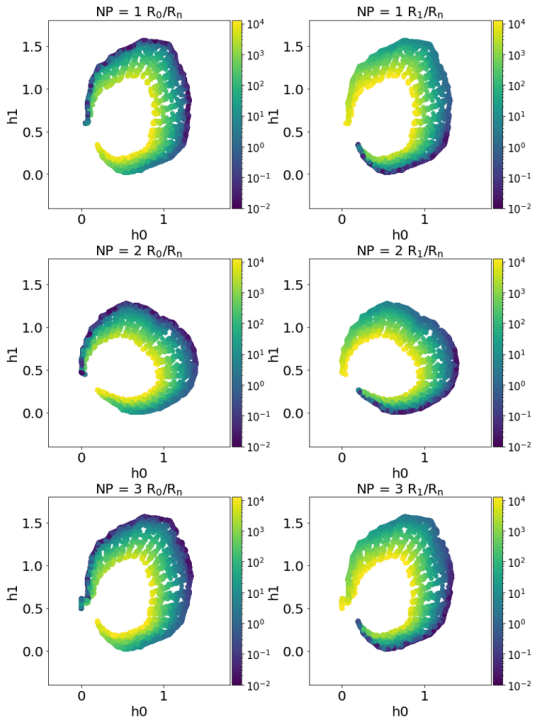

Fig. 11. R_0 and R_1 as the functions of h_0 and h_1 for NP = 1, 2, and 3.

is only 20 min using Intel i7-8705G CPU with eight logical cores. The SPICE simulation time can be further reduced to 16 min if only 1000 curves are used. The R^2 of predicting the experimental data is found to be still better than 0.85 when only 1000 data are used for training. Therefore, this approach is very rapid and can be performed almost on the fly for semiconductor defect debugging and yield enhancement without the need for expensive FA.

In this study, a simple inverter is demonstrated. There might be a possibility that R_0 and R_1 can be extracted using an analytical model if the transistor model is very simple. However, this is usually impossible when a realistic compact model is used. And it is also very difficult to construct analytical models for more complex circuits. Compared to the analytical model, the AE approach is expected to be readily applicable to other circuits with minimal domain expertise.

VII. Conclusion

In this article, we demonstrated a method to deduce the contact resistances of nMOS and pMOS in an inverter based on its VTC using simulation augmented machine learning without the need for feature extraction. An AE-based machine is used, which can reduce the hyperdimensional VTC to a 2-D latent subspace representing the contact resistances. Such a method is validated experimentally and can achieve accuracy with $R^2 > 0.9$. It is clearly shown that the latent subspace has faithfully represented the parameters in interest. Such an approach is not inverter-specific and no feature extraction is required. It is thus expected to be applicable to other circuits. Since circuit simulations are fast, this method is expected to be very useful in improving the defect debugging and yield enhancement processes.

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