Problem B:

Power and Timing Optimization Using Multibit Flip-Flop

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Q&A

Q1. For the given input test cases, only TNS will be provided. Based on our understanding of DEF/LEF, it seems that the slack for each cell will not be explicitly indicated in the input data. Could you confirm whether the input will provide the initial slack for each cell at the initial placement, or is there another way to obtain the slack for each cell?

A1. We will include an SDC file with the input.

Q2. As an extension of the first point, I would like to confirm whether the slack, power, and area information of an individual flip-flop will be included in the flip-flop library, or if the library follows the same format as last year.

A2. We will include an SDC file with the input. User can utilize open source or self-implemented Timer to help parse it.

Q3. In the Evaluation section, it is mentioned that banking & debanking must follow the scan chain rules. Does this imply that the scan chains are predefined at the initial placement, specifying the sequence of cells in each scan chain? If so, when performing optimization, should we consider the order of the scan chain and ensure that banking & debanking operations adhere to its topological order?For example, if the initial placement shows that the topological order of a certain scan chain is flip-flops A → B → C, would it be valid to bank only A and C, or must all flip-flops within the chain be banked together in order?

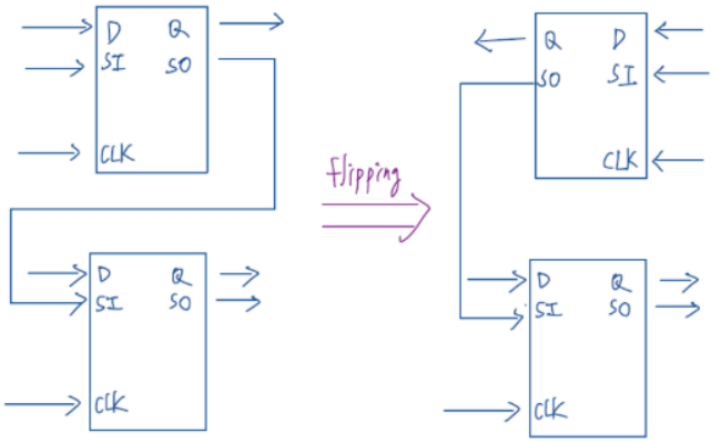
A3. If there is scan def in the def file, contestants should follow. If there is no scan def file, contestants don’t need to follow it.

Q4. Is banking across different scan chains prohibited? Additionally, will every flip-flop necessarily belong to a scan chain? Lastly, does the SI/SO mapping need to be included in the output?

A4. If there's scan def, contestants should follow its connection before and after multibit moves. If there's no scan def, we do not constrain it.

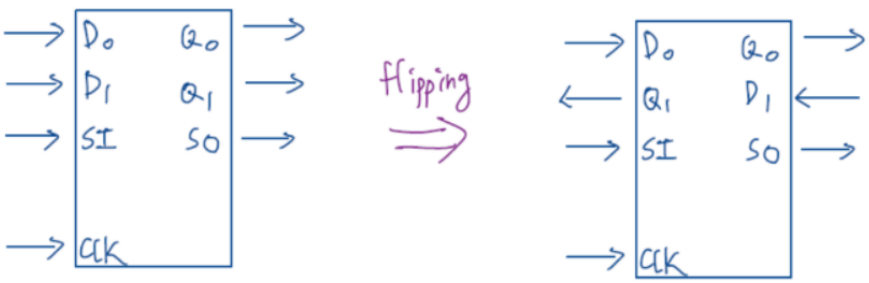
Q5a. Can the pins of the flipflop be flipped as shown in the examples below?

Case 1: flip a single bit FF (the top one)



Case 2: flip all the pins of a MBFF

Case 3: flip the partial pins of a MBFF



A5a. We allow cell flipping as long as cells could be placed legally.

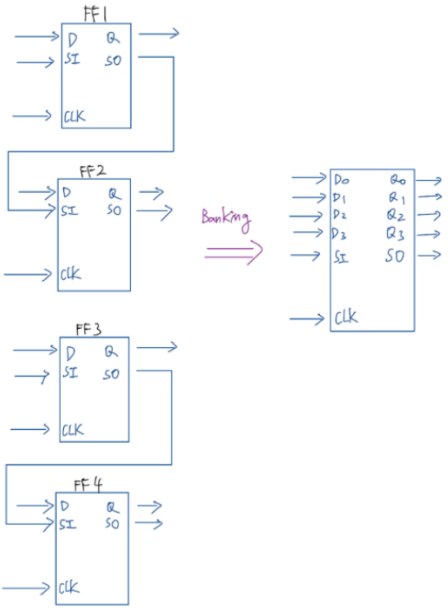
Q5b. Does it mean that the pin locations relative to a flip-flop from the input file can be modified (i.e., the output pin locations can differ from the input) to implement "flipping"?
Or is there an attribute to indicate whether the FF has been flipped in the output file?

A5b. Yes. Please refer to LEF DEF format on how to reflect a flipped cell solution.

Q6. If the scan chain order of the single-bit flip-flops is FF1 → FF2 → FF3 → FF4, does it mean that the mapping must follow the order (i.e. the D pins of FF1,FF2,FF3,FF4 must be mapped to D0,D1,D2,D3 of the MBFF respectively) after banking? Or can the D pins of FF1, FF2, FF3, and FF4 be mapped to D3, D1, D0, and D2, for example?

A6. If there is scan def in the def file, contestants should follow its precedence in their submission results. That is to say, the order precedence should remain the same.
If there is no scan def file, contestants don't need to follow it.

Q7. How should the pins of single-bit FFs be mapped to a MBFF after banking in the case shown below (where the scan chain orders are FF1 → FF2 and FF3 → FF4)? If I map the SI of FF1 to the SI of the MBFF, does that imply the SO of FF4 should be mapped to the SO of the MBFF? Do I understand correctly?



A7. If that's why defined in the scan def, yes. FF1/SI should map to the banked cell's SI and FF4/SO should be mapped to the banked SO.

Q8. According to the updated problem description, it is mentioned that an SDC file will be provided.
However, as far as I understand, the SDC file typically only contains information such as the clock period.
To compute slack values for each path, it seems that additional data would be required — such as path delays derived from cell delays, wire lengths, and setup/hold times of flip-flops.
Could you kindly clarify where or how we are expected to obtain the slack information for each path?

A8. Gate delays, loads, input delays and output delays are being provided for each clock loads. We are providing library information of each cells. Please utilize the given input information to optimize the circuit.

Q9. According to the problem description, "A placement region is divided into several bins, each with a defined utilization rate threshold." However, I could not find the actual threshold value or details on how this constraint should be applied.
Could you please clarify:
What is the specific utilization rate threshold for each bin?
Will this threshold be provided as part of the input for each testcase, or is it a fixed value?
How strictly must this threshold be enforced (e.g., soft vs. hard constraint)?

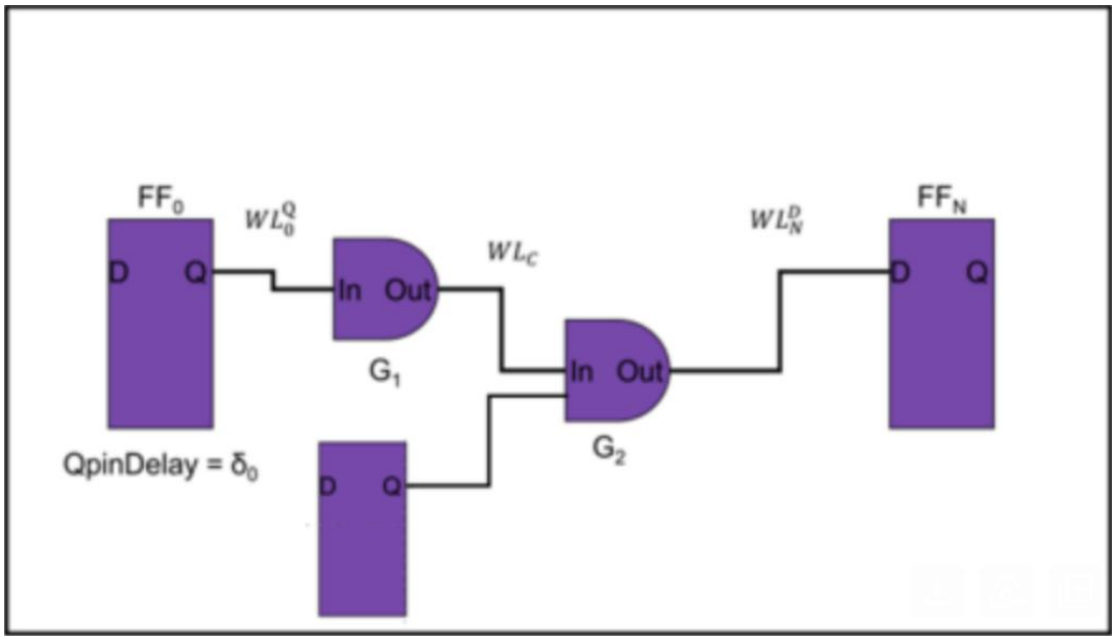
A9. Thank you very much for your inquiry. The utilization rate threshold constraint is not enacted in 2025 ICCAD CAD Contest Problem B. Please refer to the updated Problem Formulation.

Q10. The problem statement says "All instances must be placed on-site and within the die region." However, it is not explicitly stated whether the die region size or placement row/site information will be included as part of the input.
Could you please confirm:
Will the die area and legal placement sites be provided via the LEF/DEF input files?
Is there any additional information about site dimensions or die boundaries we should be aware of?

A10. Yes. The die area and legal placement sties will be provided via the input files. The legality of contestants' submission, along with the cost metrics, would be evaluated with the latest version of Synopsys Fusion Compiler.

Q11.

1. Could you give a formulated definition about the function TNS(), like the relation between TNS() and DisplacementDelay, QpinDelay, TimingSlack.
2. How to calculate the WLq if the Q pin connects to more than one pin?
3. How do we determine the slack when a FF has multiple ancestor FFs? As depicted in the figure.How to know which one is critical path?



4. How will the contest provide the slack-related information? Will it list the slack value of each individual pin, or only provide the overall TNS of the original circuit?

A11. Please refer to the latest Problem Formulation of 2025 ICCAD CAD Contest Problem B.

Q12. Is the organizer considering providing a complete .lib file (such as Nangate45_typ) for contestants to test timing and power consumption using open source tools?

A12. We will provide .lib file format to contestants.

Q13. I would like to clarify a detail regarding the DIEAREA specification in the .def file. According to the LEF/DEF Language Reference Manual (Reference [5]), particularly at the bottom of page 251, an example is provided that illustrates an L-shaped polygon for DIEAREA. However, I would like to confirm whether, in this contest, the DIEAREA is always guaranteed to be a rectangle.
Additionally, if the DIEAREA is always a rectangle, is it guaranteed that the coordinates are always specified using exactly four points, as shown in testcase1?

A13. The DIEAREA would be a shape descriptive by LEF DEF format.

Q14. I would like to ask if there's a file with the information of all kinds of gates and flipflops?

A14. LEF DEF file as well as .lib file will be provided along with updated testcase.

Q15. I just downloaded the testcase. When I start to check the input files, I cannot locate where the Flip-Flop Library Cells are. There is a weight file and a .swp file that correspond to it. There are also a .sdc file and a .def file, which contain the placement results. However, those files have no information regarding the flip-flop library cell. There are also no instructions regarding how the .sdc file name will be sent to the program in the problem instruction on the ICCAD contest webpage, which was updated on May 8.
On the other hand, there are other files in the testcase1.tar too. A Verilog file represents the circuit's topology, and a .tf file contains the technology information. But again, there is no information regarding the cell library.
I would like to know if the provided testcase1 is intended to be like this, or if something is wrong.

A15. LEF DEF file as well as .lib file will be provided along with updated testcase.

Q16. For problem B, lots of folders and files are added in the updated testcase. I would like to inquire whether there's a description file explaining the new-added folder and file in the testcase, inlcuding SNPSHOPT25, SNPSLOPT25, SNPSROPT25, SNPSSLOPT25, and all folders within them.
A16. These are for the .lef and .lib files describing the library of testcase1.

Q17. By the information on spec The contestant's submitted program should be able to execute as follows ./cadb_0000_alpha <inputFile1.txt> <inputFile2.txt> <inputFile3.txt>… <outputName>
I would like to ask the input file include all the files in testcase1 file(.sdc、.v、.tf、.def、testcase1_weight)?

A17. Yes.

Q18. I would like to ask the spec says we have to solve the location of MBFF as a result and we have to submit the def. However, the placement of wire and net information are in the def, should we handle this by ourselves?

A18. Yes.

Q19. I am currently working on Problem B and would like to perform static timing analysis (STA). I would like to use Cadence Tempus for this purpose.
I have tried sourcing the license files with the following commands:

source /project/cad/cad50/cadence/CIC/license.csh
source /project/cad/cad50/synopsys/CIC/license.csh

However, it seems that the tempus (or pt_shell) command is not available in my current environment.

May I kindly ask if Tempus is available on this system, or if there is any recommended way for performing STA under the current setup?

A19. Cadence Tempus would not be used as evaluation metrics for this contest.

Q20. We have also noted that the current file set does not include essential implementation data such as cell width/height, power, and timing information. Should we expect additional files (e.g., .lef, .lib or .ndm, .upf, etc.) to be provided?

A20. .lef and .lib has been sent with the latest release.

Q21. I'd like to confirm the meaning of the program requirements description "./cadb_0000_alpha <inputFile1.txt> <inputFile2.txt> <inputFile3.txt>... <outputName>
inputFile1.txt represents the input syntax data from sections 3.1.1 to 3.1.5.
inputFile2.txt and all subsequent files, up to but not including the last parameter, represent design data in LEF/DEF format."
For the testcase1, I would like to confirm whether inputFile1 refers to testcase1_weight.
Additionally, do inputFile2 through the last input file (excluding the outputName) include not only LEF/DEF files but also other design files such as testcase1.sdc, testcase1.v, testcase1.tf, and *.lib?

A21. The format would be like this:
cadb_0000_alpha testcase1_weight testcase1_lib1.lef testcase1_lib2.lef testcase1_lib1.lib testcase1_lib2.lib testcase1.tf testcase1.v testcase1.def testcase1.sdc outputName
Please note that the number of .lib and .lef may be design-dependent and therefore tangible.

Q22. Can the .lib and .db files under liberty provide relevant format descriptions? Reference only has format descriptions for .sdc and lefdef.

A22. We would encourage contestants to refer to Liberty File Format: What is Library Characterization? – How it Works & Techniques | Synopsys (https://www.synopsys.com/glossary/what-is-library-characterization.html)

Q23. I have tried to use Library Compiler to convert all .lib files in the liberty folder into .db files, and tried to use ICC2 Library Manger to convert all .db files into .ndm files so that ICC2 can read them, but it seems that such conversion on ICC2 Library Manager seems to have errors. Therefore, I would like to ask the organizer if there are some problems with this test case, or is it simply that ICC2 does not support this operation?

A23. We encourage contestants to continue research with our testcase. However, we could not guarantee that every file format that contestants converted this design into would result in success.

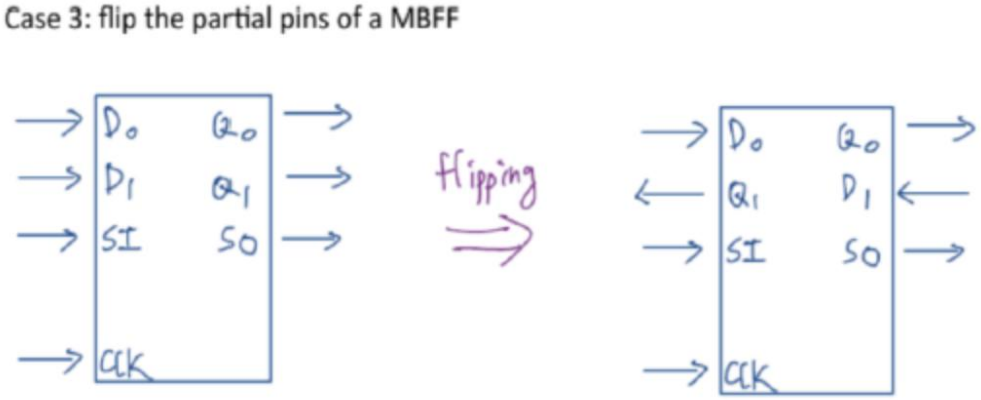
Q24. Is the placement result in the input data guaranteed to be legal? In addition, we noticed that in the currently released testcase1, some non-flip-flop cells are not on-site or overlapping. Is this expected behavior, or could we be misunderstanding the provided data?

A24. We expect contestants could optimize the design regardless of initial legality.

Q25. Will there be any tools provided to check whether our generated output is legal (e.g., specific Fusion Compiler commands or other checkers)?

A25. We are evaluating the content of evaluation tool to be released public. Meanwhile, check_legality from Fusion Compiler could be applied for legality check for now.

Q26. The A5a of the QA response mentioned the possible flipping shown in the attached image. But this doesn't seem possible because DEF LEF format only supports mirroring and rotation. Could you clarify on how what possible cases are possibly present in the testcase?



A26. Please follow LEF/DEF file format where cell flippings are allowed.

Q27. After reviewing the most recent Q&A, I noticed that the response to Q11 lacks sufficient detail. Specifically, A11 refers us to the latest Problem Formulation to address the four sub-questions, but I was unable to locate any relevant information therein. I would like to confirm whether the timing model used for this year's competition is the same as that of ICCAD 2024 Problem B. If that is the case, I kindly ask that this be explicitly stated in either the Q&A or the Problem Formulation.

Otherwise, I respectfully request a thorough explanation of the timing model adopted this year.

A27. 2025 ICCAD CAD Contest Problem B is an extension from 2024 ICCAD CAD Contest Problem B. The similarity is that both aim for power/performance/area optimization. The differences is that instead of using simplified and artificial data format, in 2025 we have adopted standard industrial format for contestants to participate in industrial-scale optimization problem.

Q28. I find it unusual that only the .sdc file has been provided, as it contains constraints primarily used for synthesis. It would be more appropriate to directly provide the initial timing slack of each flip-flop (FF). Based on the current setup, it appears that we are expected to perform timing analysis using EDA tools to obtain this information. However, such pre-processing seems unrelated to the core objectives of this EDA problem, and it would be unreasonable to require participants to run a synthesis tool like Design Compiler simply to retrieve initial slack values. I therefore request that you either clearly explain how to obtain the initial slack using the provided resources or supply the necessary data files directly.

A28. We do not require contestants to run Design Compiler. The SDC file is to help contestants understand the timing information of the current design.

Q29. I would like to raise concerns about the contents of testcase1. It appears that various files, possibly outputs from Design Compiler, have been included without explanation, particularly the .lib files. These files are highly repetitive and collectively occupy approximately 29 GB of storage. It is unclear whether we are expected to parse all of them, or if only a subset is relevant. Clear guidance on how to utilize these files effectively would be greatly appreciated.

A29. As explained in the Problem Formulation, we would like to provide a full industrial format design for contestants to participate in industrial-level optimization problem.
If you are not aware of what liberty file format is, we recommend you to refer to some materials on what liberty file format works: What is Library Characterization? – How it Works & Techniques | Synopsys (https://www.synopsys.com/glossary/what-is-library-characterization.html)

Q30. As stated in problem description 5.1, the score function requires the contestant to optimize both TNS and total Power. Reviewing the provided testcase, we found that related information is only present in either *.lib or *.db files. Although it might be possible for the contestants to attempt a calculation on all the simulation parameters and derive the required information to calculate the score function, such task is clearly outside the bound of the contest.

A30. Please refer to Liberty File Format and LEF/DEF Language Reference. There are several online references that you can review to understand the physical timing analysis of these library settings. Below are some examples that you could refer to:
https://people.eecs.berkeley.edu/~alanmi/publications/other/liberty07_03.pdf
https://www.ispd.cc/contests/18/lefdefref.pdf

For this Problem B contest, applying physical design tool on the testcase is not a requirement to participate in this contest. We have provided the testcase using industrial standard so that contestants could parse and optimize using standard file format. We would encourage contestants to study the Liberty File Format and LEF/DEF Language Reference and utilize the well-formulated testcase information for optimization.