Features

- I^2C communication interface for NT1912.
- Monitor Li-ion / Li-polymer battery.
- Reports Accurate Time-to-Empty in measured load and maximum load.
- Reports Voltage, Current, Temperature and State-of-Charge.
- Built-in 16-bit VFC to Provide High Accuracy. Measurement for Charging and Discharging current with Automatic Offset Cancellation.
- Built in EEPROM for configuration storage.
- Programmable I/O Port.
- Dynamic EDV algorithm support.
- Low Power Operating Modes:
  - Active mode: 160uA (typically)
  - Shelf Sleep mode: 2.0uA (typically)
  - Auto Shelf Sleep mode: 2.0uA (typically)
- Offer a small 3mm × 4mm DFN-10L package

Applications

- Smart Phones
- Digital Cameras
- PDA
- Handheld Devices
- Mini NB

Descriptions

NT1912 is a precise single-cell (1S1P) and multi-cell (1SxP) Li-Ion and Li-Poly battery monitoring ICs applied in handheld and portable products. The IC monitors available battery capacity and reports battery voltage, temperature, current, state-of-charge (SOC) and useful information via communication interface.

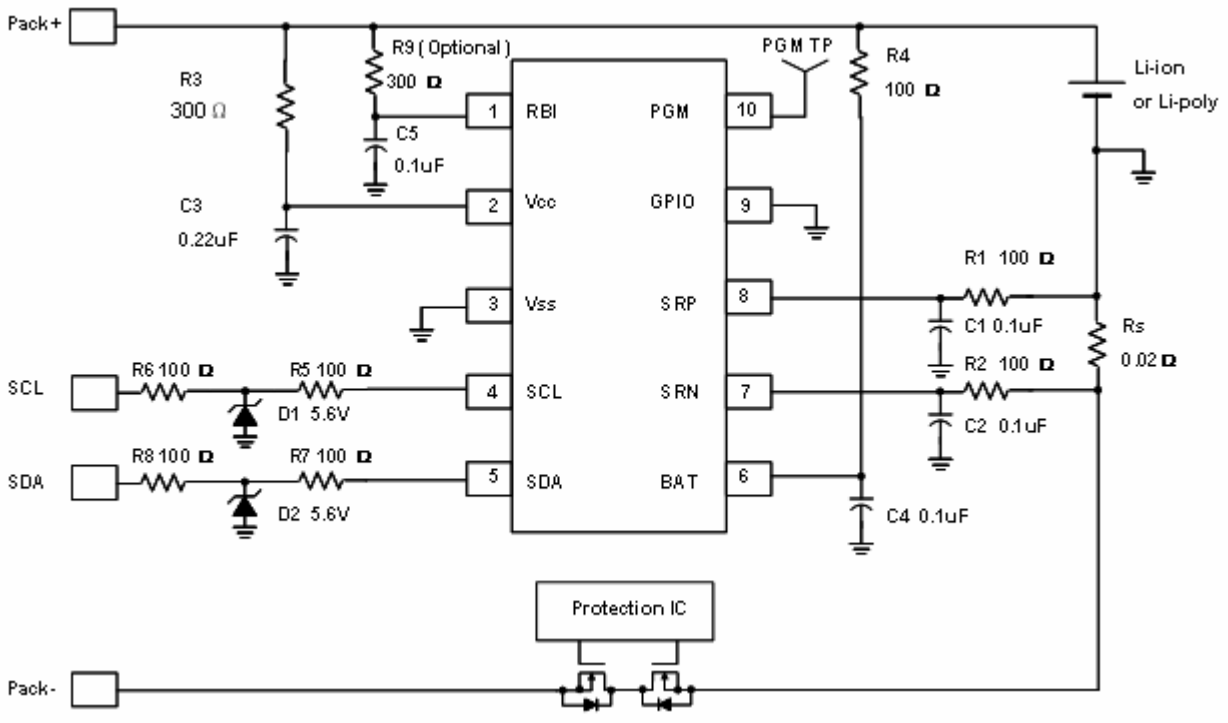
This series ICs monitor a voltage drop across a small sense resistor to determine charge and discharge activity of the battery. Compensations for battery temperature, self-discharge and discharge rate are applied to provide available capacity. The battery capacity is automatically relearned in a discharge cycle from full to empty.

NT1912 can be applied on single-cell (1S1P), multi-cell (1SxP) or multi-cell (2SxP) Li-Ion and Li-Poly battery and communicates with the host system via I^2C serial interface.

NT1912 also can be applied to system side gauge application. The application circuit depends on cooperation between host CPU and NT1912.

Typical Application Circuits

1S1P Typical Application Circuits



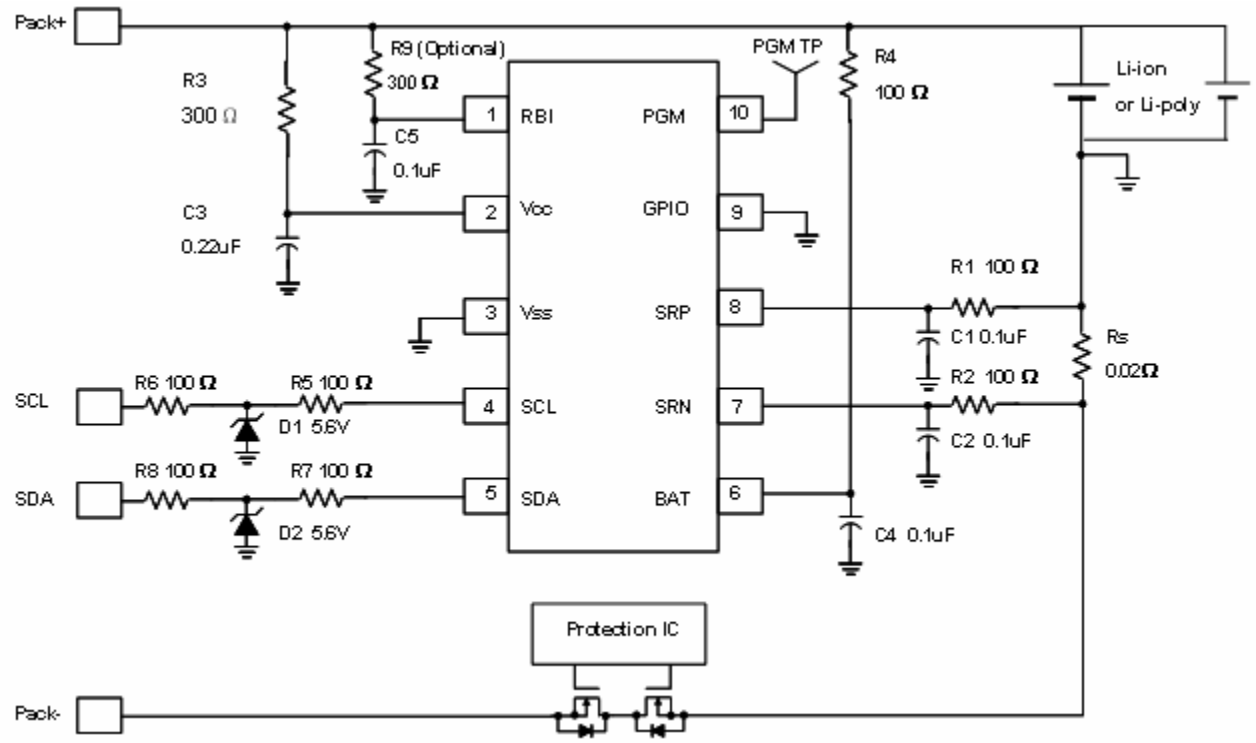
Note:

(1) Please keep PGM pin floating in normal application.

(2) Please apply 6.5V to PGM pin while NT1912 EEPROM is programmed.

(3) Pull-up voltage for SCL/SDA should be higher than 2.94V (Vcc*0.7).

1S2P Typical Application Circuits



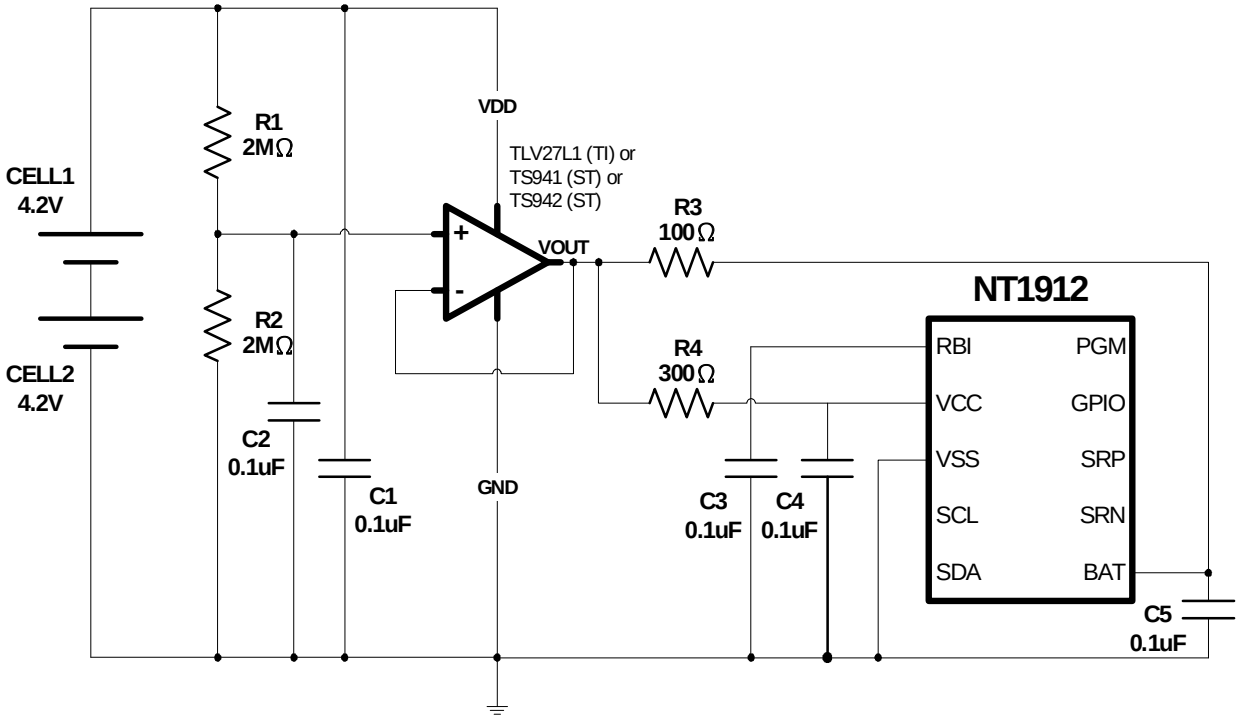
Note:

(1) Please keep PGM pin floating in normal application.

(2) Please apply 6.5V to PGM pin while NT1912 EEPROM is programmed.

(3) Pull-up voltage for SCL/SDA should be higher than 2.94V (Vcc*0.7).

2S1P Typical Application Circuits



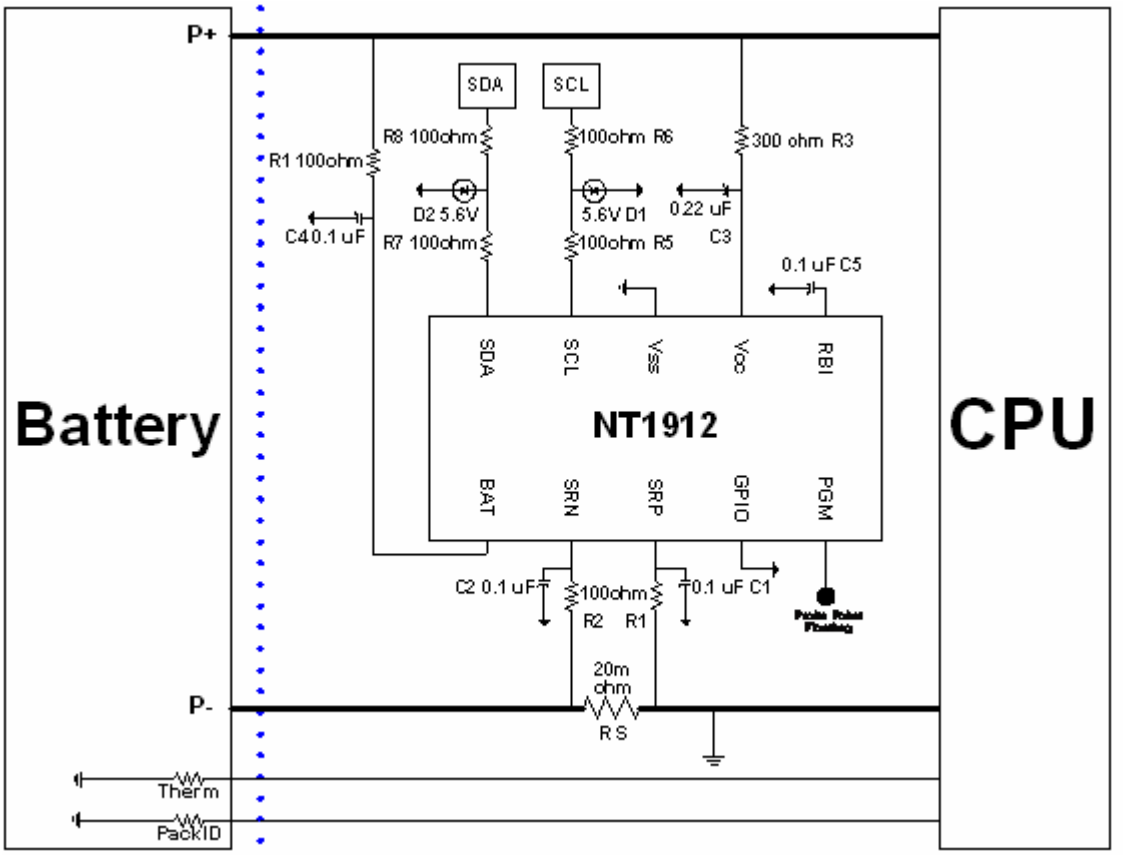
Note:

(1) Please keep PGM pin floating in normal application.

(2) Please apply 6.5V to PGM pin while NT1912 EEPROM is programmed.

(3) Pull-up voltage for SCL/SDA should be higher than 2.94V (Vcc*0.7).

System Side Application Circuit Example



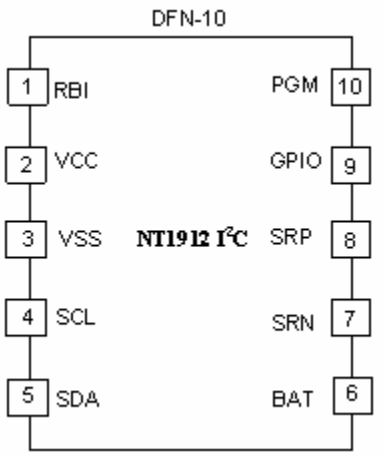
Note:

(1) Please keep PGM pin floating in normal application.

(2) Please apply 6.5V to PGM pin while NT1912 EEPROM is programmed

(3) Pull-up voltage for SCL/SDA should be higher than 2.94V (Vcc*0.7).

Pin Descriptions



DFN-10L (NT1912 I2C)			
Name	**I/O**	**Pin**	**Description**
RBI	I	1	Register back-up input
VCC	I	2	IC supply input
VSS	I	3	Ground input
SCL	I/O	4	Serial clock (I^2C)
SDA	I/O	5	Serial data (I^2C)
BAT	I	6	Battery voltage sense input
SRN	I	7	Current sense input (negative)
SRP	I	8	Current sense input (positive)
GPIO	I/O	9	General-purpose open-drain I/O pin. An external pull-up resistor is required. If no use, tied to Vss.
PGM	I	10	EEPROM program voltage input

Absolute Maximum Ratings

Over operating free-air temperature range unless otherwise noted (1)

Description		Rating	Unit
Supply voltage range, VCC (all with respect to VSS)		-0.3 to 7	V
Input voltage range at SRP, SRN, RBI, and BAT (all with respect to V_{SS})		-0.3 to Vcc+0.3	
Input voltage	SCL, SDA, GPIO (with respect to VSS)	-0.3 to 7	
	PGM (with respect to VSS) during EEPROM programming only	-0.3 to 7	
Output sink current at SCL, SDA, and GPIO		5	mA
Operating free-air temperature range, T_A		0 to 70	°C
Storage temperature range, T_{stg}		-65°C to 150°C	
Junction temperature range, T_J		-40°C to 125°C	
Lead temperature (soldering for 10 seconds)		300	

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability

Recommended Operating Conditions

Description	MIN	TYP	MAX	Units
Supply voltage, V_{CC}	2.8	-	4.2	V
Operating free-air temperature, T_A	0	-	70	°C

Electrical Characteristics

TJ = 0°C to 70°C, TJ = TA, 2.8 V ≤ VCC ≤ 4.2 V

Parameter		Test Conditions	MIN	TYP	MAX	Unit
General						
ICC(ACT)	Active current	VCC > VCC (min)		160	230	uA
ICC(SLP)	Shelf sleep mode current			2	2.5	uA
	RBI current	RBI pin only, VCC < V (POR)			20	nA
VPOR	POR threshold		2.1		2.6	V
	POR hysteresis			70		mV
	SRN, SRP Input impedance		10			MΩ
	BAT Input impedance			1		MΩ
SCL, SDA, and GPIO pin						
VIH	Hi-level input voltage			Vccx0.7		V
VIL	Low-level input voltage			Vccx0.3		
VOL	Low-level output voltage (GPIO)	IOL=1mA			0.4	
VOL	Low-level output voltage (SCL, SDA)	IOL=2mA			0.4	
	Pull down current (SCL, SDA)			16		uA
Voltage Measurement						
Measurement range		VCC = V (BAT)	2.8		4.2	V
Reported voltage resolution				2.7		mV
Voltage error percentage (%)		Vcc = 2.8~4.2V @ 0/25/45 °C	-1		1	%
Voltage update time				1.8		S
Current Measurement						
Measurement range		Rs = 20mΩ	-7		+7	A
Current error percentage (%)		-0.1A~-3.0A & 0.1A~3.0A	-1		1	%
Current error (mA)		0~100mA			±3	mA
Current update time				1.8		S
Temperature Measurement						
Measurement range			0		70	°C
Reported temperature resolution				0.25		°K
Reported temperature accuracy (NOTE1)		0~70 °C @ Vcc = 3.9V	-3		3	°C
Temperature update time				1.8		S
Time Measurement						
fOSC	Internal oscillator frequency accuracy		-5		5	%
EEPROM Programming (Vcc = 3.0~4.2V, 20 °C ≤ T_A ≤ 35 °C)						
VPROG	Programming voltage		6.25	6.5	6.75	V
tPROG	Programming pulse width	VPROG = 6.5V	100			uS
IPROG	EEPROM programming current	VPROG = 6.5V			5	mA

Note1: Self-heating due to output pin loading and sense resistor power dissipation can alter the reading from ambient conditions

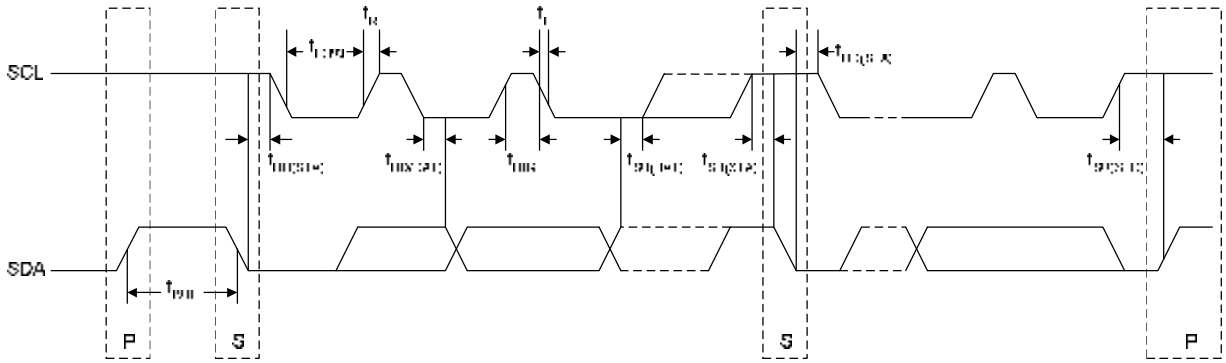
Note2: Need 5.4 seconds to update current when load or charger is applied

Electrical Characteristics (Continued)

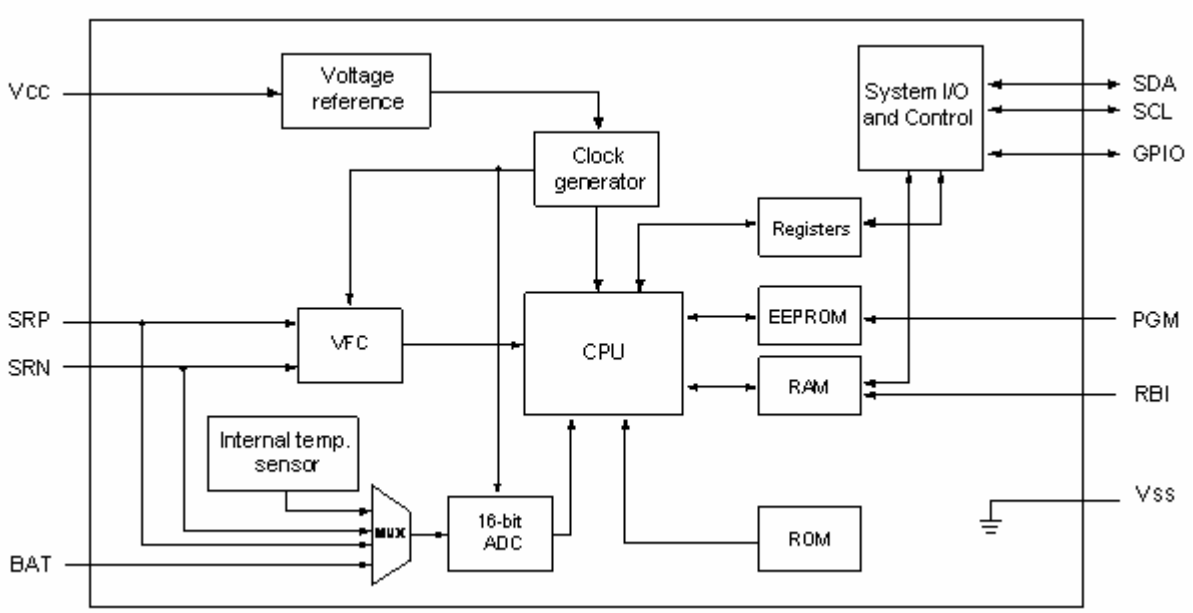
T_J = 0°C to 70°C, T_J = T_A, 2.8 V ≤ VCC ≤ 4.2 V

Parameter		Test Conditions	MIN	TYP	MAX	Unit
Standard Serial I²C Communication Timing (NT1912)						
t_R	SCL/SDA rising time				1	uS
t_F	SCL/SDA falling time				300	nS
t_{HIGH}	SCL for high		4			uS
t_{Low}	SCL for low		4.7			
$t_{SU(STA)}$	Setup time for repeated -start		4.7			
$t_{HD(STA)}$	Start to first falling edge of SCL		4			
$t_{SU(DAT)}$	Setup time for data		250			nS
$t_{HD(DAT)}$	Hold time for data		300			
$t_{SU(STO)}$	Setup time for stop		4			uS
t_{BUF}	Bus free time between sop and start		4.7			
t_{SCL}	Clock frequency				100	KHz
$t_{BUS(ERR)}$	Timeout for bus error			14.2		S

NT1912 (I^2C) Timing Diagram



Functional Diagram



Scope: NT1912

This document is applied to NT1912.

Functional Descriptions

NT1912 determines battery capacity by monitoring the amount of charge or discharge from a Li-Ion or Li-Poly battery. The IC measures charge and discharge current to monitor the battery's low-voltage threshold, compensates for aging, self-discharge, temperature and discharge rate. The resolution of available capacity is reported in 3.57uVh. NT1912 measures the current via a resistor (R_{sense}), shown as typical application circuit, across the negative terminal of the battery and the ground. Differential voltage sense across the current sense resistor improves device performance and leading to an improvement in time-to-empty accuracy. NT1912 also reports Time-to-empty (TTE) in minutes to indicate the remaining time for different situations: average usage time (at-rate and actual load) and longest standby time (standby load). Such meaningful information could be read from the specific registers.

Shown as application circuits, the GPIO pin can be configured as a general-purpose programmable I/O port. An internal pull down resistor on SCL and SDA line ensure that the device detect a logic "0" on the SCL and SDA lines and automatically enter the low power sleep mode when the system power is switched off or the pack is removed. A 100k pull up resistor to VCC can be placed to the SCL and SDA lines to disable this feature.

Measurements

NT1912 uses a precise voltage-to-frequency converter (VFC) for charge and discharge counting and uses analog-to-digital converter (ADC) for battery voltage and temperature measurement. Both VFC and ADC are compensated for offset automatically.

Charge and Discharge Counting

NT1912 uses a voltage-to-frequency converter (VFC) to perform a continuous integration of the voltage waveform across the sense resistor and the integration of the voltage across the sense resistor is the charge added (charging) or removed (discharging) from the battery. Since the VFC integrates the waveform directly, the shape of the current waveform through the sense resistor does not take effect the measurement accuracy. The low-pass filter feeds the sense resistor voltage to the input of SRP and SRN to reduce the signal noise and doesn't have any effect the measurement accuracy, either.

Offset Calibration

NT1912 provides an auto-compensation to eliminate the internal voltage offset error across SRP and SRN for maximum charge measurement accuracy. The offset voltage of the VFC measurement must be low enough to be able to measure small signal levels accurately.

Digital Magnitude Filter (Current Gap)

The digital magnitude filter (DMF) threshold can be set in *EEPROM (DMFSD 0x7A)*. The charge or discharge accumulation is ignored while the sensed voltage (from the sense resistor) is below the DMF threshold. This could be used to set a threshold above the maximum VFC offset estimated from the device and PCB. This ensures the measured capacity change is zero when no charge or discharge current.

Since even a small PCB offset may be accumulated to a big error over a long period. In addition to setting the threshold above the largest offset expected, the DMF should be set below the minimum signal level to be measured. Since the measured signal can only be measured as accurate as the VFC offset

induced from the PCB. The DMF threshold is programmed in *EEPROM (DMFSD 0x7A)* in increments of 5uV. Programming a zero in the DMF value disables the DMF function and no VFC counts are ignored.

Voltage

NT1912 measures and monitors the battery voltage through the BAT pin and reports an offset correction value via the internal registers. This IC also monitors the voltage for the end-of-discharge voltage (EDV) thresholds. The EDV threshold levels are used to determine when the battery has been empty or discharged to 6.25%.

Temperature

NT1912 uses an integrated temperature sensor to monitor the battery pack's temperature. This measurement is reported via the internal registers. The temperature information is used to adjust the compensations of charge, discharge rate and self-discharge capacity.

RBI Input

The register back up input pin, RBI, is used with an external capacitor to provide backup potential to the internal registers when Vcc drops below the power-on-reset voltage V (POR). Vcc is output on RBI to charge the capacitor when Vcc is above V (POR). When Vcc is below V (POR), the capacitor can support the internal registers to retain the Ram data. Ram data could keep as long as the RBI voltage remains above 1.3V.

NT1912 checks the RAM corruption by storing redundant copies of the high bytes of NAC, LMD and low byte of CYCT and specific critical data. After a reset, this IC compares NAC, LMD, CYCT and specific critical data with the redundant copies. If the checks are correct, NAC, LMD, CYCT and CYCL are retained and the CI bit in FLAGS is left unchanged. Otherwise, NAC, CYCT, CYCL are cleared, LMD is initialized from EEPROM, and the CI bit in FLAGS is set to "1". All other RAM is initialized on all resets.

GPIO Pin

The GPIO pin can be used as an input or output. The initial state can be set the value in bit 7 in the *EEPROM (PKCFG 0x7C)* location. The GPIO state can be changed by change bit-7 of Mode at any time. If no used, the GPIO pin should be tied to Vss.

Layout Considerations

The auto-compensating VFC approach effectively cancels the internal offset voltage within this IC but any external offset caused by PCB layout still exists. This makes it critical to pay special attention to the PCB layout. To obtain optimal performance, the decoupling capacitor from Vcc to Vss and the filter capacitors from SRP and SRN to Vss should be placed as closely as possible to NT1912, with short trace runs to both signal and Vss pins. All low-current Vss connections should be kept separate from the high-current discharge path from the battery and should tie into the high current trace at a point directly next to the sense resistor. This should be a trace connection to the edge or inside of the sense resistor connection, so that no part of the Vss interconnections carries any load current and no portion of the high-current PCB trace is included in the effective sense resistor.

The resistor placed at pin Vcc will affect I2C hi-level input voltage because it will induce a voltage drop between Vcc and VPack$^+$. The V_{IH} is defined as 0.7xVcc, i.e. the lower Vcc is, the lower V_{IH}. For example, VPack+ is 4.2V and the resistor is 300 Ohm, and the Vcc will be $4200 - 300 \times 0.16 = 4152mV$. Therefore, I2C hi-level input voltage is $0.7 \times 4152 = 2906mV$. The hi-level input voltage can be lower by increase resistance, but it will also lower Vcc. In some worse cases, it will drop into V_{POR} range.

Capacity Learning and Qualified Discharge

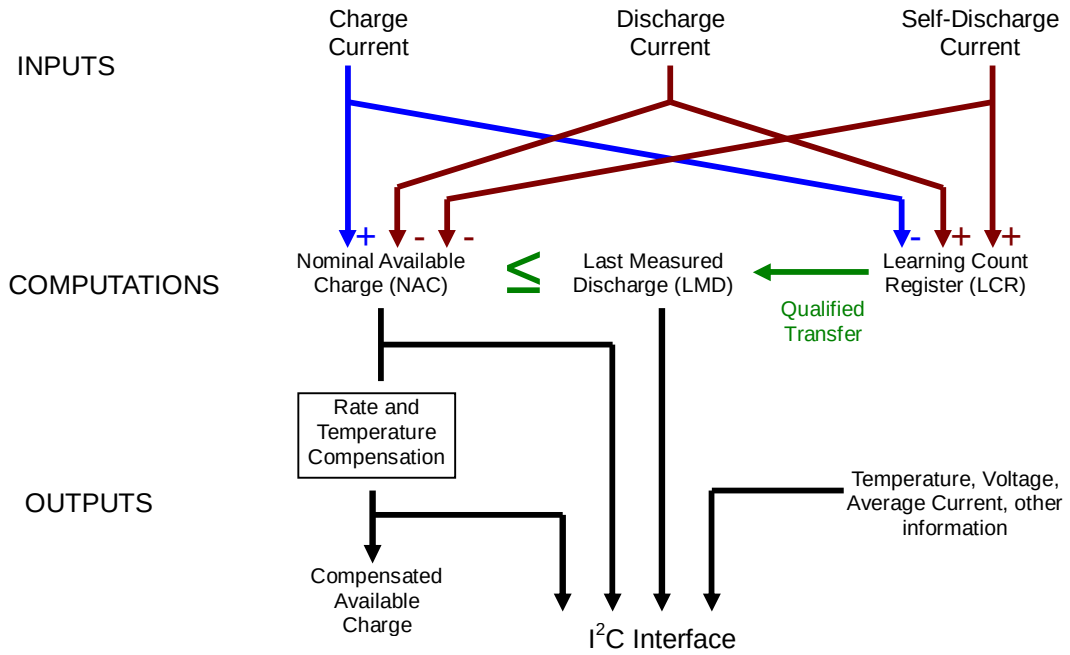


Figure 1. Operation Overview

NT1912 measures the capacity of the battery during actual use conditions and updates the last measured discharge (LMD) register with the latest measured value. Learned LMD is retained unless a full reset occurs. NT1912 would learn a new capacity on each full discharge except for such disqualified discharge. A learning cycle is disqualified by several abnormal conditions (please refer to *Disqualify Conditions*).

The full-charged condition is defined as Nominal Available Capacity (NAC) = Last Measured Discharge (LMD). The EDV1 threshold is defined as the voltage that guarantees at least 6.25% of battery capacity. When full-charged condition occurs, the "Valid Discharge Flag" (VDQ) in FLAGS is set and remains "1" until the learning discharge cycle completes or any of the disqualify conditions occurs.

When the battery is discharged from the full-charged status to the threshold, EDV1, a learning discharge cycle completes. The measured LMD value is determined by measuring the capacity drained from battery on the full-charged condition (NAC=LMD) until battery voltage V ≤ EDV1, plus LMD/16 (6.25%) to account for the capacity remaining below the EDV1 threshold. To prevent premature detection of the EDV thresholds caused by load variations, EDV detection has a adjusted dynamically delay of up to 21.5 seconds with RSOC ≥ 6.25% and 3 seconds with RSOC = 0%. The equation of LMD is shown as follows:

$$LMD_{NEW} = (Capacity\ deliver\ from\ NAC{=}LMD\ to\ V{=}EDV1) + 1/16\ (LMD_{OLD})$$

In a learning cycle with a significant reduction caused by unexpected situations, the new LMD value is restricted to a maximum value learn-down during any single learning discharge of LMD/8 (i.e. 12.5% of LMD). The capacity inaccurate bit (CI) in FLAGS is cleared after a learning cycle. This bit remains cleared unless a full reset occurs or the cycle count (CYCL) reaches a count of 32 since the last learning cycle.

Taper Current and Voltage of Charging Termination

NT1912 detects the charging termination when the charging current is below a threshold (taper current) stored in *EEPROM (TAPER 0x7B)* and the pack voltage is above well-defined voltage threshold determined by the bits of QV1 and QV2 setting in *EEPROM (PKCFG 0x7C)*. When charging termination occurs, the state-of-charge is set to 100%. Otherwise, maximum value of state-of-charge is 99% if charging termination doesn't happen.

Disqualify Conditions:

VDQ is cleared and a capacity learning cycle is disqualified caused by any of the following conditions:

(1). Cold temperature: Temperature $\leq 0^{o}C$ when the EDV1 threshold voltage is reached.

(2). Light load: Average current is less than or equal to double of the initial standby load (AI ≤ 2xISLC) when the EDV1 threshold voltage is reached.

(3). Excessive charging: Cumulative charge > 255 NAC counts during a learning discharge cycle (alternating discharge-charge-discharge before EDV1 is set).

(4). Excessive self-discharge: NAC reduction from self-discharge estimate performed 45 times.

(5). Self-discharge at termination of learning cycle. If self-discharge estimate reduces NAC to be below LMD/16, the VDQ is cleared.

(6). Reset: VDQ is cleared on all resets.

Power Modes

NT1912 has three power modes: active, shelf sleep and low voltage mode. Followings are the descriptions in detailed.

Active Mode

During normal operation, NT1912 works in active mode. An external pull-up resistor between Vcc and SCL, SDA on the IC side of the system can disable the shelf sleep mode function. This pull up resistor value should be small enough to force logic “1” on SCL, SDA even with the loading, internal pull down current and any external ESD protection circuitry.

Shelf Sleep Mode

NT1912 enters the shelf sleep mode when receives the SLEEP command from host and the SDA and SCL lines are pulled low for at least 1.8 seconds, which is adjustable, and the charge or discharge activity is below the digital magnitude filter threshold (DMF). When entering shelf sleep mode, the gas gauge function ceased.

Two internal pull down resistors are built-in NT1912. Therefore, no external pull down resistor is needed. Two 100KΩ pull up resistors are connected between SDA and SCL and Vcc to wake up NT1912 from the shelf sleep mode.

A full reset will be done when leaves shelf sleep mode. If the value of NAC must be retained after wake up, shelf sleep mode is not supposed to be used.

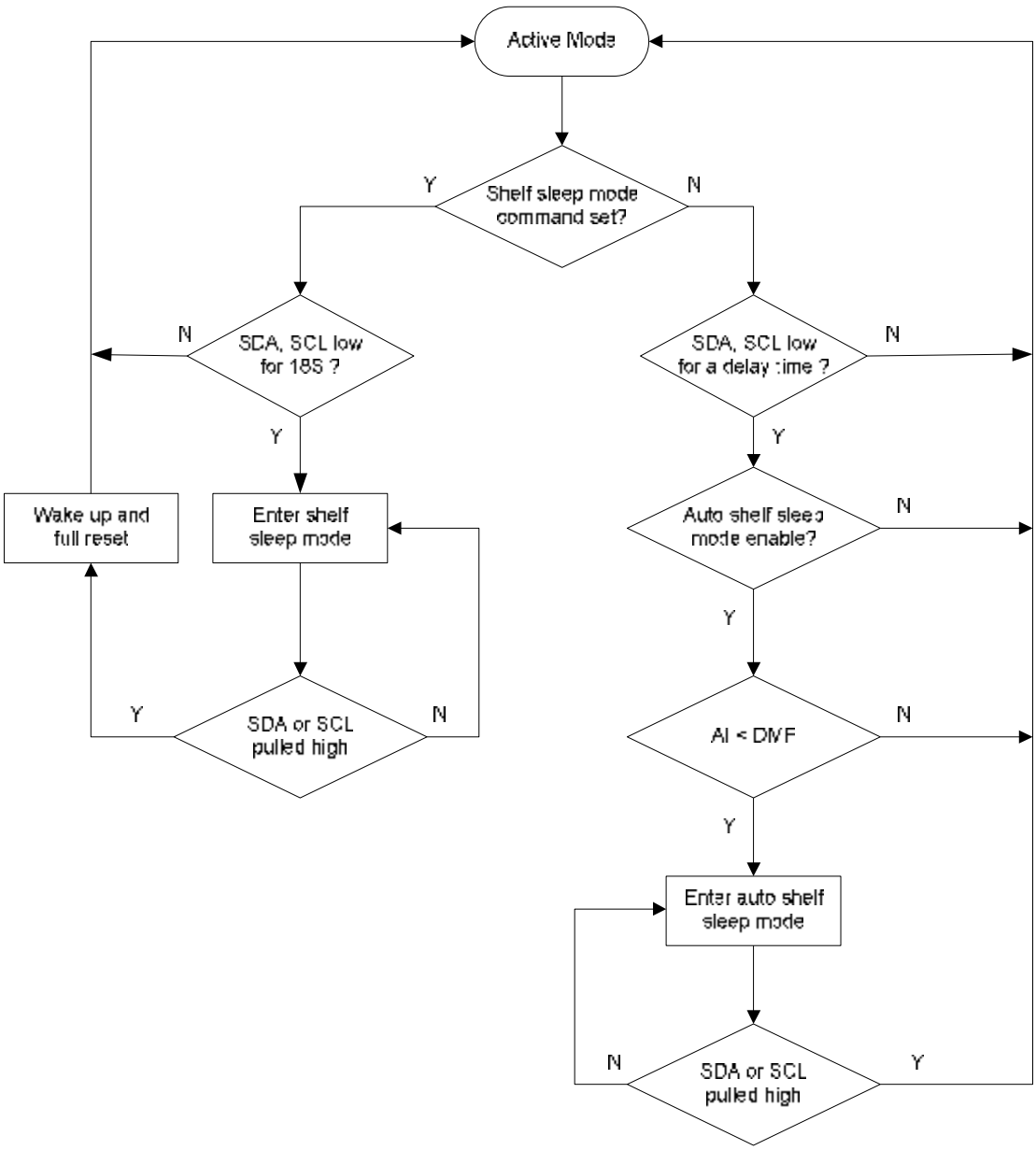
Auto Shelf Sleep Mode

Auto Shelf Sleep Mode can be enable/disable in *EEPROM IF_SEL [1].*

NT1912 enters the auto shelf sleep mode when SDA and SCL lines are pulled low for specific time which can be set (default is around 18 seconds, please see application notes), the charge or discharge current is below the digital magnitude filter threshold (DMF) and auto shelf sleep function is enable. When entering shelf sleep mode, the gas gauge functions stop.

Two internal pull down resistors are built-in NT1912. Therefore, no external pull down resistor is needed. Two 100KΩ pull up resistors are connected between SDA and SCL and Vcc to wake up NT1912 from the shelf sleep mode.

Power modes flow chart



Programming the EEPROM

There are 10 bytes of EEPROM that are used for firmware control and application data (please see the *Register Descriptions* section for more information). Programming the EEPROM should employ a 6.5V pulse on the PGM pin for at least 100uS during pack manufacturing. The programming mode must be enabled prior to writing any values to the EEPROM. The programming mode is enabled by writing to *EE_EN register (0x6E)* with data 0xDD. Once the programming mode is enabled, the desired data can be written to the appropriate address. Figure 2 shows the method for programming all locations. It is not required that addresses 0x76-0x7F be programmed at the same time or in any particular order. The programming method illustrated in Figure 2 that can be used to program any of the bytes as long as the sequence of enable, write, read, apply programming pulse and disable is followed.

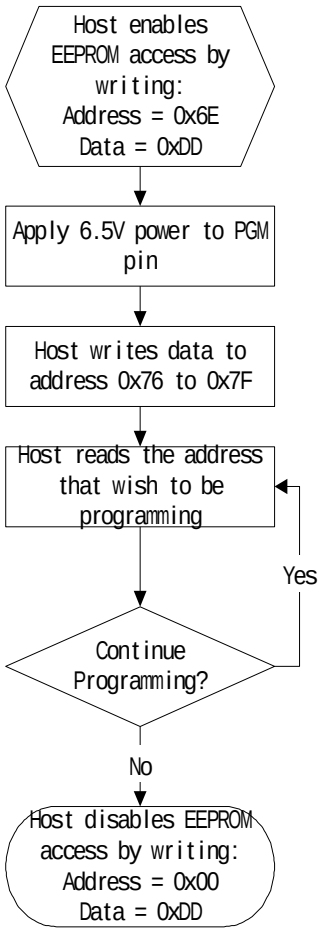


Figure 2. EEPROM access flow chart

Memory Map

The EEPROM registers store permanent user data. The memory map is shown as table below.

Table 1. NT1912 Memory Map

Address	Name	Function	LSB Units	Access
EEPROM Registers				
0x7F	TCOMP	Temperature compensation constants, or ID#1		R/W
0x7E	DCOMP	Discharge rate compensation constants, or ID#2		R/W
0x7D	GAF/DEDV	Initial maximum load current, or ID#3		R/W
0x7C	PKCFG	Pack configuration values		R/W
0x7B	TAPER	Charge termination taper current	228uV	R/W
0x7A	DMFSD	Digital magnitude filter and self-discharge rate constants		R/W
0x79	ISLC/EDVT	Initial standby load current		R/W
0x78	SEDV1	Scaled EDV1 threshold		R/W
0x77	SEDVF	Scaled EDVF threshold		R/W
0x76	ILMD	Initial last measure discharge high byte	914uVh	R/W
RAM Registers				
0x6F-0x75	--	Reserved		R
0x6E	EE_EN	EEPROM program enable		R/W
0x2D-0x6D	--	Reserved		R
0x2C	CSOC	Compensated state-of-charge (SOC)	%	R
0x2B-0x2A	CYCT	Cycle count total high-low byte	Counts	R
0x29-0x28	CYCL	Cycle count since learning cycle high-low byte	Counts	R
0x27-0x26	TTECP	Time-to-empty at constant power high-low byte	Minutes	R
0x25-0x22	RSVD	Reserved		R
0x21-0x20	CEDV	Compensated EDV Threshold high-low byte	mV	R
0x1F-0x1E	RSVD	Reserved		R
0x1D-0x1C	STTE	Standby time-to-empty high-low byte	Minutes	R
0x1B-0x1A	SI	Standby current high-low byte	3.57uV	R
0x19-0x18	TTF	Time-to-full high-low byte	Minutes	R
0x17-0x16	TTE	Time-to-empty high-low byte	Minutes	R
0x15-0x14	AI	Average current high-low byte	3.57uV	R
0x13-0x12	FCAC	Full Compensated Available Capacity high – low Byte	3.57uV	R
0x11-0x10	CAC	Compensated Available Capacity high – low Byte	3.57uV	R
0x0F-0x0E	LMD	Last Measured Discharge high-low byte	3.57uV	R
0x0D-0x0C	NAC	Nominal available capacity high-low byte	3.57uV	R
0x0B	RSOC	Relative state-of-charge	%	R
0x0A	FLAGS	Status flags		R
0x08-0x09	VOLT	Reported voltage high-low byte	MV	R
0x06-0x07	TEMP	Reported temperature high-low byte	0.25 ^{o}K	R
0x04-0x05	ARTTE	At rate time-to-empty high-low byte	Minutes	R
0x02-0x03	AR	At rate high-low byte	3.57uV	R/W
0x01	MODE	Device mode register		R/W
0x00	CTRL	Device control register		R/W

Device Control Register (CTRL) - Address 0x00

The device control register is used to request special operations by host. The highest priority command set in the MODE register is executed when the host writes data 0xA9, 0x56, or 0xc5 (command key) to this register. The CTRL register is cleared when the command is accepted. The host should set appropriate bits in MODE before sending the command key to CTRL.

The commands are changed data for pack-side gauge.

The commands can be used with pack-side gauge if the default EEPROM values in the NT1912 do not match the required values. All of the commands are only changed the Ram data (0x76~0x7F). The Ram data are changed to initial data from EEPROM if there is a full reset or data corruption is detected.

NAME	WNACCI	WRTCYC	WRTLMD	UPDC	UPEDV1	UPDMF	UPCFG	UPCOMP
MODE	0x08	0x02	0x01	0x20	0x10	0x08	0x02	0x01
CTRL	0x56	0x56	0x56	0xC5	0xC5	0xC5	0xC5	0xC5

WNACCI	AR(L/H) **à** NAC.	**WRTLMD**	AR(L/H) **à** LMD.
WRTCYC	AR(L/H) **à** CYCT.	**UPDC**	AR **à** ILMD(ARL) / EDVF(ARH)
UPEDV1	AR **à** SEDV1(ARL) / ISLC/EDVT(ARH)	**UPDMF**	AR **à** DMFSD(ARL) / TAPER(ARH)
UPCFG	AR **à** PKCFG(ARL) / GAF/DEDV(ARH)	**UPCOMP**	AR **à** DCOMP(ARL) / TCOMP(ARH)

WNACCI WNACCI is used to transfer data from the AR registers to NAC. It's identical to the WRTNAC command , but the CI bit in FLAGS is also cleared.

WRTCYC WRTCYC is used to transfer data form the AR registers to CYCT.

WRTLMD WRTLMD is used to transfer data form the AR registers to LMD.

UPDC UPDC is used to simultaneously transfer data form the AR registers to ILMD(ARL) and SEDVF(ARH).

UPEDV1 UPEDV1 is used to simultaneously transfer data form the AR registers to SEDV1(ARL) and ISLC/EDVT(ARH).

UPDMF UPDMF is used to simultaneously transfer data form the AR registers to DMFSD(ARL) and TAPER(ARH).

UPCFG UPCFG is used to simultaneously transfer data form the AR registers to PKCFG(ARL) and GAF/DEDV(ARH).

UPCOMP UPCOMP is used to simultaneously transfer data form the AR registers to DCOMP(ARL) and TCOMP(ARH).

Mode Register (MODE) - Address 0x01

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	GPIEN	GPSTAT	WRTNAC	DONE	PRST	INIT	FRST	Reserved
Priority	**-**	**-**	**1**	**2**	**3**	**Read only**	**4**	**-**

MODE REGISTER	DESCRIPTION
GPIEN	(1) GPIEN sets the state of the GPIO pin. (2) “1” configures the GPIO pin as input. (3) “0” configures the GPIO pin as an open-drain output. (4) This bit is initialized to the value of bit 7 of the PKCFG register in the EEPROM
GPSTAT	(1) GPSTAT sets the state of the open drain output of the GPIO pin (GPIEN = 0). (2) “1” turns off the open drain output. (3) “0” turns the output on. (4) This bit is set when POR and when the GPIO pin is an input (GPIEN=1), this bit returns the logic state of the GPIO pin.
WRTNAC	WRTNAC is used to transfer data from the AR registers to the NAC registers. Other registers are updated as appropriate. This command is useful during the pack manufacture and test to initialize the gauge to match the estimated battery capacity. This bit is cleared on all resets.
DONE	(1) DONE is used to write NAC with LMD. (2) If the host uses a charge termination method that does not allow the monitor to detect the taper current. The host system could use this command when the charging is complete to force update of internal registers to a full battery condition. (3) This bit is cleared on all resets.
PRST	(1) The partial reset (PRST) command requests a full reset except that the NAC, LMD, and the CI bit in FLAGS should not be restored to their initial values. This command is intended for manufacturing use. (2) This bit is cleared on all resets.
INIT	(1) The INIT status bit is set to ‘1’ by this IC when first power-on-reset (POR), a full reset, data Corruption is detected in the internal memory containing EEPROM coefficients. (2) If NAC, LMD, CYCT, or EEPROM-initialized coefficients need to be modified from their original values, the host should first update the values and then clear the INIT bit. The INIT bit is not cleared by the NT1912.
FRST	(1) The full reset (FRST) command requests a full reset. (2) A full reset re-initializes all RAM registers, including the NAC, LMD, and FLAGS registers. This command is intended for manufacturing use. (3) This bit is cleared on all resets.
Reserved	Reserved bit.
Notes	(1) GPIEN & GPSTAT would be performed while MODE is set. (2) For setting WRTNAC, DONE, PRST and FRST, only the highest priority mode set is enabled whenever the CTRL register is written with data 0xA9. (3) All other mode bits and the CTRL register are cleared when the highest priority command is completed.

At Rate Registers (ARL/ARH)–Address 0x02/0x03

The host writes the current value to this register for predictive calculation of time-to-empty. NT1912 uses this value to predict the time-to-empty at any desired current. The current value written into this register pair is always assumed to be a discharge current. The value written to AR should be the predicted voltage across the sense resistor expressed in units of 3.57uV per count.

This register is also used during pack manufacturing to input a nominal available charge (NAC) value to set the NAC registers to the approximate initial pack capacity value.

At Rate Time to Empty Registers (ARTTEL/ARTTEH)–Address 0x04/0x05

Predicted time-to-empty, in minutes, at user entered discharge rate. The discharge current used in the calculation is entered by the host system in the at-rate (AR) registers. The at-rate capacity (ARCAP) value used may be larger or smaller than CACT. It is computed using the same formulas as CACT, except the discharge compensation is computed using AR, instead of average discharge current (AI), for the discharge rate. The equation used to predict at rate time-to-empty is:

$$ARTTE=60 \times (ARCAP/AR)$$

The host system has read only access to this register pair.

Reported Temperature Registers (TEMPL/TEMPH)–Address 0x06/0x07

The TEMPH and the TEMPL registers contain the reported die temperature. The temperature is expressed in units of $0.25^{o}K$ and is updated every 1.8 seconds. The equation to calculate reported pack temperature is:

$$T_{PACK}=0.25 \times (256 \times TEMPH+TEMPL)$$

The host system has read-only access to this register pair.

Reported Battery Voltage Registers (VOLTL/VOLTH)–Address 0x08/0x09

The VOLTH and the VOLTL registers contain the reported battery voltage measured on the BAT pin. Voltage is expressed in mV. Reported voltage can't exceed 5000 mV. The host system has read only access to this register pair. Voltage is updated every 1.8 seconds.

Status Flag Register (FLAGS)–Address 0x0A (Host read only)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	CHGS	NOACT	IMIN	CI	FC	VDQ	EDV1	EDVF

MODE REGISTER	DESCRIPTION
CHGS	(1) CHGS is charge-state flag. (2) "1" indicates a charge current (V_{SRP} > V_{SRN}). (3) "0" indicates a lack of charge activity. (4) This bit should be read when the host system reads the average current register pair to determine the sign of the average current magnitude. (5) This bit is cleared to "0" on all resets.
NOACT	(1) NOACT is no-activity flag. (2) "1" indicates the voltage across RS is less than the digital magnitude filter. (See the *Digital Magnitude Filter* section for more information) (3) This bit is cleared to "0" on all resets.
IMIN	(1) IMIN is Li-ion taper current detection flag. (2) "1" indicates that the charge current has tapered to less than the taper value set in EEPROM and that the battery voltage is greater than or equal to the value selected by the QV0 and QV1 bits in the PKCFG register (see *EEPROM Data Registers* description for more details). (3) This bit is cleared to "0" on all resets.
CI	(1) CI is capacity inaccurate flag. (2) "1" indicates the firmware has not been through a valid learning cycle and is basing all calculations on design values programmed into EEPROM. This bit is also set while at least 32-count increments since the last learning cycle. (3) This bit is set on a full reset and cleared on a LMD learning cycle updated
FC	(1) FC is fully charged flag (2) FC is set when RSOC = 100% (3) FC is cleared when RSOC < 95%
VDQ	(1) VDQ is valid-discharge flag. (2) "1" indicates device met all necessary requirements for a capacity learning discharge cycle. (3) This bit is cleared to "0" on LMD update or disqualified conditions occurred. (4) This bit is cleared to "0" on all resets.
EDV1	(1) EDV1 is end-of-discharge-voltage-1 flag. (2) "1" indicates voltage on the BAT pin is less than or equal to the EDV1 voltage programmed in EEPROM and the battery has less than or equal to 6.25% of LMD capacity remaining. (3) LMD updates immediately if the VDQ bit is set when this bit transitions from 0 to 1. (4) This bit is cleared to "0" on all resets or when charging.
EDVF	(1) EDVF is end-voltage-final flag. (2) "1" indicates battery has discharged fully based on design capacity programmed in EEPROM. (3) EDVF is defined as the empty capacity (0%) threshold. (4) This bit is cleared to "0" on all resets or when charging.

Relative State of Charge (RSOC)–Address 0x0B

RSOC reports the nominal available capacity as a percentage of the last measured discharge (LMD) value. This value is required if end-equipment reports percentage rather than time-to-empty. The equation is:

$$RSOC\ (\%) = 100 \times (NAC/LMD)$$

The host system has read-only access to this register.

Nominal Available Capacity Registers (NACL/NACH)–Address 0x0C/0x0D

NAC is uncompensated available capacity in the battery and it is reported in counts of 3.57uVh. This registers pair (NAC) increments during charge (V_{SRP} > V_{SRN}) and decrements during discharge (V_{SRP} < V_{SRN}). The NAC registers are cleared when the BAT voltage is less than or equal to EDVF while

discharging. The NAC registers are also cleared during reset or power-on-reset (POR) if RAM corruption is detected. Otherwise, the registers are retained after a reset if RAM corruption is not detected. The host system has read only access to this register pair.

Last Measured Discharge Registers (LMDL/LMDH) – Address 0x0E/0x0F

Last measured discharge (LMD) is used as a measured full reference. It is based on the measured discharge capacity of the battery from full to empty. LMD is reported in counts of 3.57uVh. The firmware updates LMD on a valid capacity learning cycle, which is defined as the battery reaching the EDV1 level while the VDQ bit is set. Used with NAC register values to calculate relative state of charge (RSOC). The host system has read only access to this register pair.

Compensate Available Capacity (CACL/CACH)–Address 0x10/0x11

CAC is the available capacity with compensated for discharge rate, temperature, and age. It is reported in counts of 3.57uVh. This register pair follows NAC during discharge by an amount computed from DCOMP (discharge compensation coefficients), TCOMP (temperature compensation coefficients), and GAF/DEDV (gain age compensation coefficients). The CAC is not allowed to increase while discharging, so that if the discharge rate decreases, the NAC may be still decrease but CAC is keep in the same value. Once CAC equals to NAC minus compensated value, it will continue decreasing. CAC equals NAC if the CHGS bit set to “1”. The host system has read-only access to this register pair.

Fully Charged Compensated Available Capacity (FCACL/FCACH) –Address 0x12/0x13

FCAC is the available capacity with compensated for discharge rate, temperature, and age. It is reported in counts of 3.57uVh. This register pair follows LMD during discharge, it will compute by LMD minus DCOMP (discharge compensation coefficients), TCOMP (temperature compensation coefficients), and GAF/DEDV (gain age compensation coefficients). In charge condition, it should be set to LMD. The host system has read only access to this register pair.

Average Current Registers (AIL/AIH) –Address 0x14/0x15

This register pair reports the magnitude of the average current through the sense resistor. The resolution of this register is 3.57uV per count. The current reported is an average over the last 3.6 seconds. The host system has read-only access to this register pair. Use the following equation to convert the value to mA, where Rs is the sense resistor value in milliohms:

$$\text{Average Current} = (256 \times \text{AIH} + \text{AIL}) \times 3.57 / \text{Rs}$$

Time-to-Empty Registers (TTEL/TTEH) –Address 0x16/0x17

This register pair reports calculated time-to-empty at the measured discharge rate. This value is based on the temperature and discharge rate compensated available charge and the average current. The equation to calculate TTE is:

$$\text{TTE} = 60 \times \text{CAC/AI}$$

TTE is reported in minutes. The host system has read-only access to this register pair.

Time-to-Full Registers (TTFL/TTFH) –Address 0x18/0x19

This register pair reports calculated time-to-full at the measured charge rate. The time computed at the average current rate is extended by 50% to estimate the effect of the current taper. TTF is reported in minutes. The equation for TTF is:

$$TTF = 60 \times 1.50 \times (LMD-NAC)/AI$$

Standby Current Registers (SIL/SIH) –Address 0x1A/0x1B

This register pair reports measured standby current through the sense resistor. The standby current is an adaptive measurement. Initially, the register pair reports the standby current programmed in EEPROM and after spending some time in standby, the register pair reports the measured standby current. Each new SI value is computed as follows:

$$SI_{NEW} = (15/16) \times SI_{OLD} + (1/16) \times AI$$

This filter function allows the reported standby current to shift towards the actual measured current with a time constant of approximately 1~2 minutes. The value is reported with a resolution of 3.57uV per bit. Use the following equation to convert the value to mA, where Rs is the sense resistor value in milliohms:

$$\text{Standby Load Current} = (256 \times SIH + SIL) \times (3.57 / Rs)$$

The host system has read-only access to this register pair.

Standby Time-to-Empty Registers (STTEL/STTEH) –Address 0x1C/0x1D

This register pair reports calculated time-to-empty at the measured standby current value. This value is based on the nominal available charge and the standby current. STTE is reported in minutes. STTE is calculated by:

$$STTE = 60 \times NAC / SI$$

The host system has read-only access to this register pair.

Compensated End-of-Discharge Registers (CEDVL/CEDVH) –Address 0x20/0x21

The EDV1 threshold can be compensated for discharge rate and temperature. After EDV1 threshold has computed by compensated values, it will show in these register pairs. The CEDV only updated when discharge. The minimum of EDV1 threshold will be the greater of the computed CEDV threshold and EDVF+ 32mV. CEDV is displayed in million volts. The host system has read-only access to this register pair.

Time-to-Empty at Constant Power Registers (TTECPL/TTECPH) –Address 0x26/0x27

TTECP is the time-to-empty in minutes with a constant power load. TTECP is equal to the TTE constant-current value scaled to reflect a future drop in battery voltage that would cause the load current to increase. The calculation assumes a linear voltage drop down to EDVF.

$$TTECP = TTE \times (VOLT + EDVF) / (2 \times VOLT)$$

The host system has read-only access to this register pair.

Cycle Count Since Learning Cycle Registers (CYCLL/CYCLH) –Address 0x28/0x29

CYCL is the cycle count since the last learning cycle. Each count indicates an increment of CYCT since there was a learning cycle. This register is cleared every time there is a learning cycle. When this count reaches 32, it forces the CI flag in FLAGS to a “1”. The host system has read-only access to this register pair.

Cycle Count Total Registers (CYCTL/CYCTH) –Address 0x2A/0x2B

CYCT is the cycle counts since a full reset. A full reset clears these registers. Each count indicates a cumulative discharge equal to the Design Capacity (256×ILMD). The host system has read-only access to this register pair.

Compensated State-of-Charge (CSOC) –Address 0x2C

CSOC reports the compensated available capacity as a percentage of the last measured discharge value (LMD). The equation is:

$$\text{CSOC (\%)} = 100 \times \text{CAC/LMD}$$

The host system has read-only access to this register pair.

EEPROM Enable Register (EE_EN) –Address 0x6E

Register used to enable host writes to EEPROM data locations (addresses 0x76–0x7F). Host must write data 0xDD to this register to enable EEPROM programming.

EEPROM Data Registers (EE_DATA)–Address 0x76 – 0x7F

These registers will be programmed during pack manufacturing to allow flexibility in the design values of the battery to be monitored. The EEPROM data registers are listed as below Table.

Address	Name	Function	LSB Units	Access
EEPROM Registers				
0x7F	TCOMP	Temperature compensation constants, or ID#1		R/W
0x7E	DCOMP	Discharge rate compensation constants, or ID#2		R/W
0x7D	GAF/DEDV	Initial maximum load current, or ID#3		R/W
0x7C	PKCFG	Pack configuration values		R/W
0x7B	TAPER	Charge termination taper current	228uV	R/W
0x7A	DMFSD	Digital magnitude filter and self-discharge rate constants		R/W
0x79	ISLC/EDVT	Initial standby load current		R/W
0x78	SEDV1	Scaled EDV1 threshold		R/W
0x77	SEDVF	Scaled EDVF threshold		R/W
0x76	ILMD	Initial last measure discharge high byte	914uVh	R/W

Initial Last Measured Discharge High Byte (ILMD) – Address 0x76

This register contains the scaled design capacity of the battery to be monitored. The equation to calculate the initial LMD is:

$$ILMD = \frac{DesignCapacity(mAh) \times R_S(m\Omega)}{(256 \times 3.57uVh)}$$

Where the R_S is the value of the sense resistor used in the system. This value is used as the high byte for the initial LMD values. The initial low byte value is “0”.

Scaled EDVF Threshold (SEDVF) – Address 0x77

This register contains the scaled value of the threshold for zero battery capacity. To calculate the value to program, use the following equation:

$$SEDVF = \frac{DesignEDVF(mV)}{8} - 256$$

Scaled EDV1 Threshold (SEDV1) – Address 0x78

This register contains the scaled value of the voltage when the battery has 6.25% remaining capacity. When the battery reaches this threshold during a valid discharge, the device learns the full battery capacity, including the remaining 6.25%. To calculate the value to program, use the following equation:

$$SEDV1 = \frac{DesignEDV1(mV)}{8} - 256$$

Initial Standby Load Current and EDV1 Temperature compensation (ISLC/EDVT) – Address 0x79

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	ISLC[3]	ISLC [2]	ISLC [1]	ISLC [0]	EDVT [3]	EDVT [2]	EDVT [1]	EDVT [0]

The high nibble in this register contains the scaled end-equipment design standby current. A capacity learning cycle is disqualified if average current is less than or equal to two times the initial standby load when the EDV1 threshold voltage is reached. The equation for programming this value is:

$$ISLC = \frac{DesignStandbyCurrent(mA)\ x\ Rs(m\Omega)}{57.1}$$

Where the R_S is the value of the sense resistor used in the system.

The low nibble in this register contains the EDV1 temperature compensation (EDVT) coefficient. The temperature compensation is impedance-based so the resulting compensation is proportional to load current. EDVT is programmed to increase the EDV1 rate compensation (programmed in the DEDV coefficient) by 0.78% per count for each degree than temperature is below the Toff threshold programmed in TCOMP. See the GAF/DEDV section for the complete EDV1 compensation equation.

Digital Magnitude Filter and Self-Discharge (DMF/SD)–Address 0x7A

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	DMF[3]	DMF[2]	DMF[1]	DMF[0]	SD[3]	SD[2]	SD[1]	SD[0]

MODE REGISTER	DESCRIPTION
DMF[3]	(1) Sets the digital magnitude filter (DMF) threshold. (See *Digital Magnitude Filter* section for more information). The equation for programming this value as (2):
DMF[2]	
DMF[1]	(2) $DMF[3:0] = \frac{DesignThreshold}{5}(uV)$
DMF[0]	
SD[3]	(1) Set the self-discharge rate %/day at 25°C. NAC is reduced with an estimated self-discharge correction to adjust the expected self-discharge of the battery. This estimation is only performed when the battery is not being charged. The rate programmed in EEPROM for DMFSD determines the self-discharge when 20°C ≤ Temperature ≤ 30°C.
SD[2]	(2) Self-discharge estimation is doubled when temperature increased 10°C.
SD[1]	(3) Maximum value of self-discharge is 16 times of the programmed rate for temperature ≥ 60°C. (4) Self-discharge estimation is halved when temperature decreased 10°C. (5) Minimum value of self-discharge is 1/4 of the programmed rate for temperature < 0°C.
SD[0]	(6) $SD[3:0] = \frac{1.61}{DesignSD}(\%/day)$

Taper Current (TAPER) - Address 0x7B

This register contains the enable bit for the capacity aging estimation and the scaled end-equipment design charge taper current. This value, in addition to battery voltage, is used to determine when the battery has reached a full charge state. The equation for programming this value is:

$$TAPER[6:0] = \frac{I_{TAPER}(mA) \times R_S(m\Omega)}{228(uV)}$$

Where R_S is the value of the sense resistor used in the system.

TAPER[7] is used to enable the aging function of the LMD. If this bit is enabled, LMD will be reduced by LMD/1024 that every time the CYCL increments by 2 and a cumulative NAC self-discharge reduction of 1.56% has been done without charging the battery to full. If TAPER[7] is set to 0, the LMD aging function will be disabled.

Pack Configuration (PKCFG) - Address 0x7C

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	GPIEN	QV1	QV2	RG1	RG2	RG3	DCFIX	TCFIX

MODE REGISTER	DESCRIPTION
GPIEN	(1) Allow pack manufacturer to set the state of the GPIO pin on initial power on. (2) "0" indicates the GPIEN bit is cleared on reset and GPIO pin acts as a high impedance output. (3) "1" indicates the GPIEN bit is set on rest and GPIO pin acts as an input. (4) The state of the GPIO pin can be read from the GPSTAT bit in MODE register.
QV1	The two bits set the end voltage of charge termination. Terminating voltage is set as Table 2
QV2	
RG1	The three bits set the initial RSOC value after FRST. Please refer to AN12 for RSOC setting.
RG2	
RG3	
DCFIX	(1) DCFIX is fixed discharge compensation. (2) "0" indicates use normal discharge rate compensation (DCOMP register). (3) "1" indicates the device assumes a fixed value of 0x6C for DCOMP, that is, set a discharge rate compensation gain of 5.08% with a compensation threshold of C/2. (4) "1" also indicates free the EEPROM location of 0x7E for use as a programmable ID byte.
TCFIX	(1) TCFIX is fixed temperature compensation. (2) "0" indicates use normal temperature compensation (TCOMP register). (3) "1" indicates the device assumes a fixed value of 0x46 for TCOMP, which will increase DCGN by 25% per °C below 12°C. (4) "1" also indicates free the EEPROM location of 0x7F for use as a programmable ID byte.

Table 2. Charge Termination Voltage Settings

QV1	QV2	Voltage (mV)
0	0	3968
0	1	4016
1	0	4064
1	1	4112

Gain Age Factor and EDV1 Discharge Rate Compensation (GAF/DEDV) - Address 0x7D

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	GAF [1]	GAF [0]	DEDV [5]	DEDV [4]	DEDV [3]	DEDV [2]	DEDV [1]	DEDV [0]

The two most significant bits in address 0x7d set the gain factor (GAF). This Factor adjusts the discharge rate compensation with age. The GAF will cause a linear increase in the discharge rate and temperature compensation with cycle count. GAF=3 will cause DCGN to increase by same amount as a drop in temperature of 16 °C below the Toff threshold programmed in TCOMP when CYCT = 85 . Lower value of GAF will require proportionally more cycle counts to reach the same level of compensation reduction. The equation for the aged discharge compensation gain (ADCGN) is :

$$ADCGN = DCGN\left(1 + TCGN \frac{CYCT}{16}\right) \frac{GAF}{32}$$

TCGN is the temperature compensation gain programmed in TCOMP. See the section on DCOMP for the complete discharge rate compensation equation. There will be no aging of the discharge compensation if GAF=0 . The recommended value for GAF if battery aging data is not available is GAF=2.

The six significant bits (DEDV [5:0]) in address 0x7d set the EDV1 discharge rate compensation gain. The EDV1 threshold is impedance-based and will be reduced from the no-load EDV1 threshold programmed in SEDV1 as a function of load current. The EDV1 threshold is reduced linearly with AI at a rate of 8mV per C-rate for each DEDV count. The DEDV rate compensation is also increased at cold temperature as described in the section on ISLC / EDVT. The actual EDV1 threshold used will be the greater of CEDV or EDVF +32mV. The equation for the EDV1 threshold compensation is as below:

$$CEDV = \mathrm{EDV1} - 8\mathrm{mV} * \mathrm{DEDV} * (\frac{AI}{DC}),\ when\ T \geq Toff$$

$$CEDV = EDV1 - 8mV * DEDV * (\frac{AI}{DC}) * [1 + EDVT * \frac{(Toff\ -\ T)}{128}],\ when\ T < Toff$$

Discharge Rate Compensation Coefficients (DCOMP) - Address 0x7E

This register is used to set the basic discharge compensation coefficients. These basic discharge gain coefficients DCGN, is increased at cold temperature and with age to achieve a combined impedance-based discharge rate, temperature, and age compensation of available capacity. This compensation determines the reduction in CAC from NAC and the reduction in FCAC from LMD.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	DCGN[4]	DCGN[3]	DCGN[2]	DCGN[1]	DCGN[0]	DCOFF[2]	DCOFF[1]	DCOFF[0]

MODE REGISTER	DESCRIPTION
DCGN[4]	Discharge rate compensation gain coefficient sets the slope of the capacity compensation with discharge current. These slope can be set in increments of 0.39% (DCGN / 256).
DCGN[3]	
DCGN[2]	
DCGN[1]	
DCGN[0]	
DCOFF[2]	The discharge compensation offset coefficient sets the capacity offset threshold. There is no capacity compensation reduction if the compensation falls below this threshold. The discharge compensation threshold is set in multiples of C/8.The threshold is set as Table 3. (A 1C-rate current is the current that equals the design capacity.)
DCOFF[1]	
DCOFF[0]	

Table 3. Discharge Rate Compensation Thresholds

DCOFF[2:0]	DCOFF Threshold
0	0
1	(DCGN / 256) * 1C / 8
2	(DCGN / 256) * 2C / 8
3	(DCGN / 256) * 3C / 8
4	(DCGN / 256) * 4C / 8
5	(DCGN / 256) * 5C / 8
6	(DCGN / 256) * 6C / 8
7	(DCGN / 256) * 7C / 8

The discharge compensation capacity reduction (DCMP) is function of discharge rate, temperature, and age (cycle count). There is no compensation if the DSGN factor increased for age and temperature times AI is less than the DCOFF threshold (DCMP≧0). The following is the combined equation for the DCMP reduction：

$$TCMP = 1 + \frac{TCGN}{32} * (Toff - T) \text{ , when } T < Toff$$
$$TCMP = 1 \text{ , when } T \geq Toff$$

$$ACMP = 1 + (\frac{TCGN}{32}) x (\frac{CYCT}{16}) xGAF$$
$$DCMP = (AI * \frac{DCGN * ACMP * TCMP}{256}) - (\frac{DCOFF * DC * DCGN}{8 * 256})$$

If PKCFG [1]=1, the device assumes a fixed value of 0x6C for DCOMP, giving a discharge rate compensation gain of 5.08% with a compensation threshold of C/2. This frees the EEPROM location of 0x7E for a user-defined identification byte.

Temperature Compensation Coefficients (TCOMP) – Address 0x7F

This register is used to set the compensation coefficients for temperature. These coefficients are used to scale the aged discharge rate compensation for improved accuracy of predicted available capacity ate at cold temperature.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	TCGN[4]	TCGN[3]	TCGN[2]	TCGN[1]	TCGN[0]	TOFF[2]	TOFF[1]	TOFF[0]

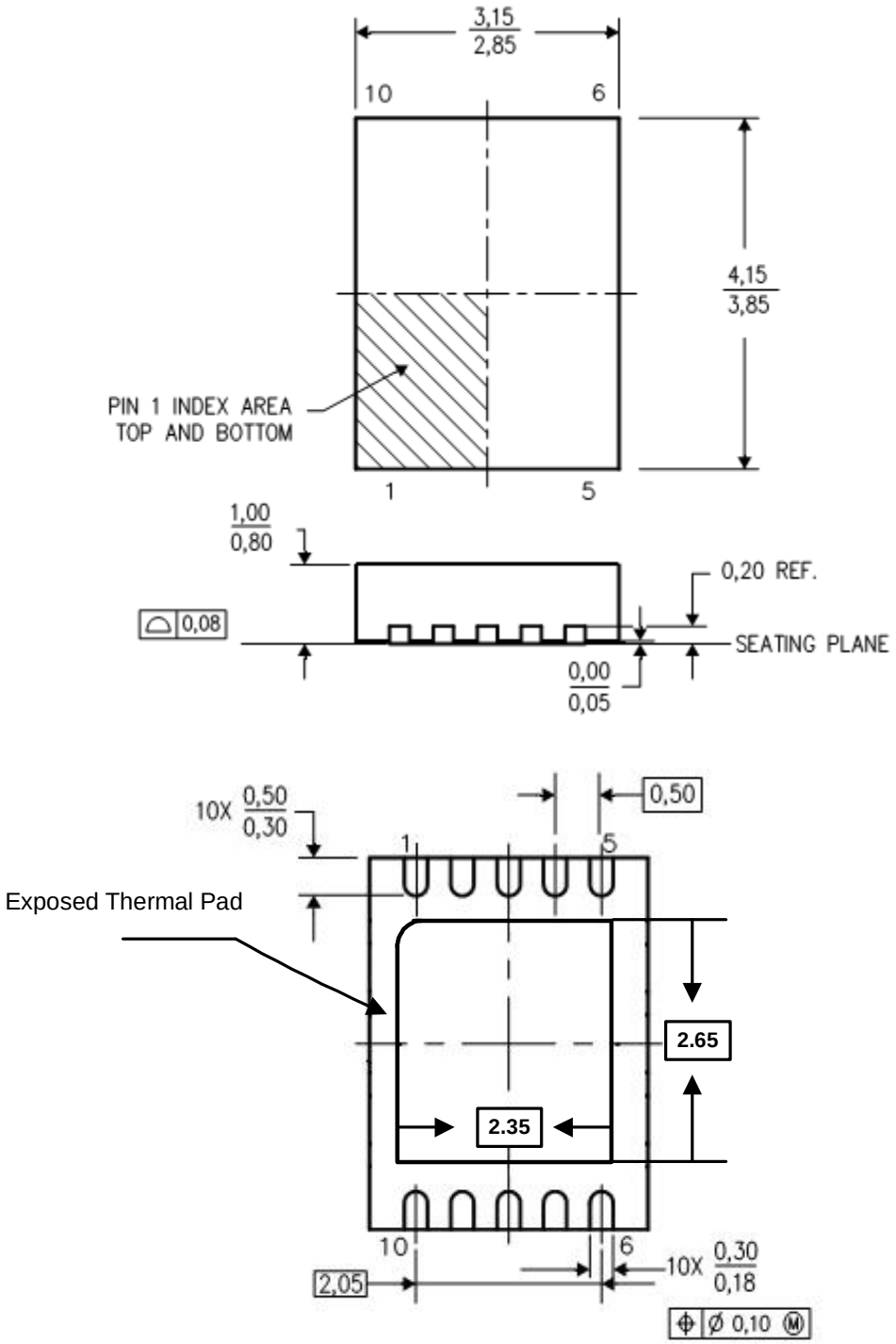
MODE REGISTER	DESCRIPTION
TCGN[4]	The temperature compensation gain coefficient is used to scale DCGN when temperature drops below the Toff threshold. TCGN will increase the ACMP value in increments of 3.125% (TCGN/32) for each degree that temperature is below the Toff threshold.
TCGN[3]	
TCGN[2]	
TCGN[1]	
TCGN[0]	
TOFF[2]	Temperature compensation offset threshold sets the temperature above which there is no temperature compensation applied to DCGN. The threshold is also used as the threshold for application of cold temperature if EDV1 (see GAF/EDVT section) and the threshold to allow the NAC = LMD capacity adjustment to be made at MIN detection (see functional description section). The Toff threshold in degree Celsius is equal to 2* Toff.
TOFF[1]	
TOFF[0]	

If PKCFG[0]=1, the device assumes a fixed value of 0x46 for TCOMP. This will increase the DCGN factor by 25% per degree Toff of 12°C. This frees the EEPROM location of 0x7F for use as a programmable identification byte.

Package Information (DFN-10L)

第一行(字元最多爲 6 碼): 第 1~2 碼 => 固定碼 NT(Neotec 縮寫)
第 3~6 碼 => 品名

第二行爲 Date Code: 第 1 碼 => 代表月份, 爲大寫英文字母 A~L
第 2 碼 => 代表週別, 以數字 1~5 表示
第 3 碼 => 代表當年西元年份的尾數
第 4~5 碼 => 代表流水號



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice

C. The package thermal pad must be soldered to the PCB for thermal and mechanical performance