

AOD403
P-Channel Enhancement Mode Field Effect Transistor

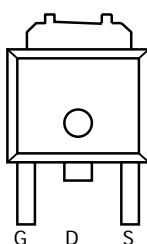
General Description

The AOD403 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and low gate resistance. With the excellent thermal resistance of the DPAK package, this device is well suited for high current load applications. *Standard Product AOD403 is Pb-free (meets ROHS & Sony 259 specifications). AOD403L is a Green Product ordering option. AOD403 and AOD403L are electrically identical.*

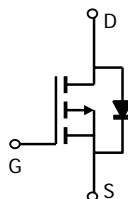
Features

V_{DS} (V) = -30V
 I_D = -85A (V_{GS} = -20V)
 $R_{DS(ON)} < 6m\Omega$ (V_{GS} = -20V)
 $R_{DS(ON)} < 7.6m\Omega$ (V_{GS} = -10V)

TO-252
D-PAK



Top View
Drain Connected
to Tab


Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current ^{B,G}	I_D	$T_A=25^\circ\text{C}$ ^G	A
		$T_A=100^\circ\text{C}$ ^B	
Pulsed Drain Current	I_{DM}	-200	A
Avalanche Current ^C	I_{AR}	-30	A
Repetitive avalanche energy $L=0.1\text{mH}$ ^C	E_{AR}	120	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	W
		$T_C=100^\circ\text{C}$	
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	13	20	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		39	50	$^\circ\text{C/W}$
Maximum Junction-to-Case ^C	$R_{\theta JL}$	0.56	1.5	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24V, V _{GS} =0V T _J =55°C		-0.01	-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±25V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.5	-2.6	-3.5	V
I _{D(ON)}	On state drain current	V _{GS} =-10V, V _{DS} =-5V	-60			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-20V, I _D =-20A T _J =125°C		5.1 7.1	6 8.5	mΩ
		V _{GS} =-10V, I _D =-20A		6.3	7.6	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-20A		44		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.72	-1	V
I _S	Maximum Body-Diode Continuous Current				-104	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz		4360	5300	pF
C _{oss}	Output Capacitance			1050		pF
C _{rss}	Reverse Transfer Capacitance			762		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		2.5	3	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =-10V, V _{DS} =-15V, I _D =-20A		93.2	120	nC
Q _{gs}	Gate Source Charge			18		nC
Q _{gd}	Gate Drain Charge			29.2		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-15V, R _L =0.75Ω, R _{GEN} =3Ω		18	25	ns
t _r	Turn-On Rise Time			30	45	ns
t _{D(off)}	Turn-Off DelayTime			51	75	ns
t _f	Turn-Off Fall Time			35	50	ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-20A, dI/dt=100A/μs		39.5	48	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-20A, dI/dt=100A/μs		30.8	37	nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on steady-state R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB or heatsink allows it.

B: The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

C: Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C.

D: The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

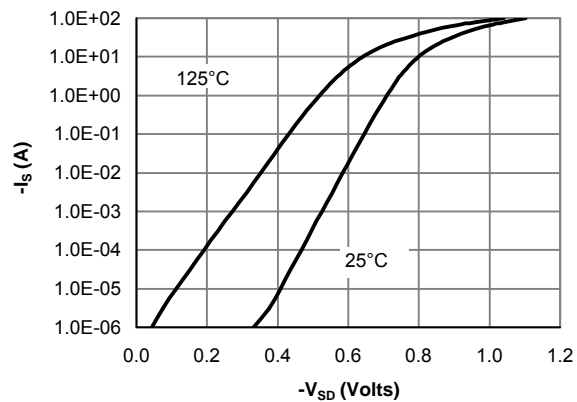
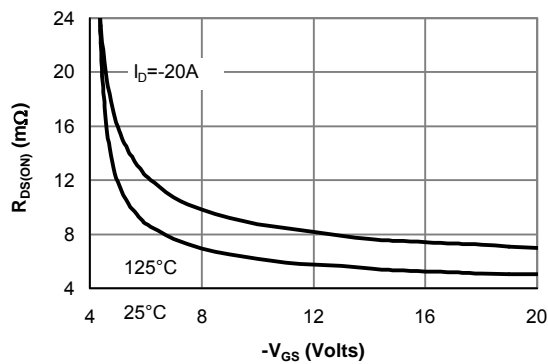
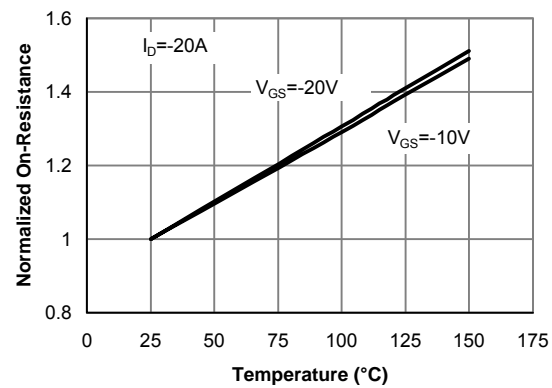
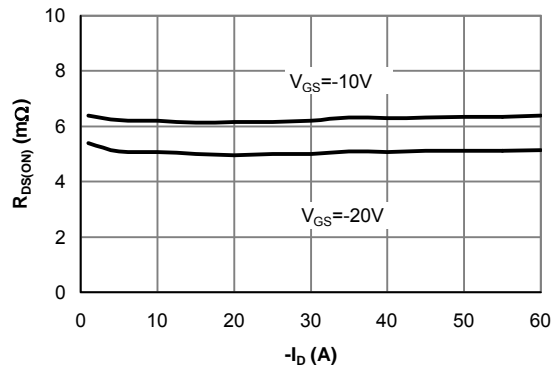
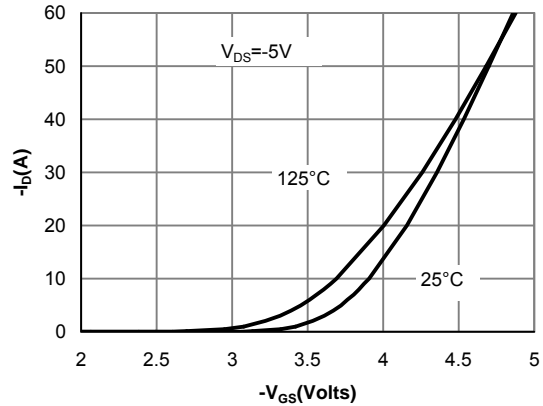
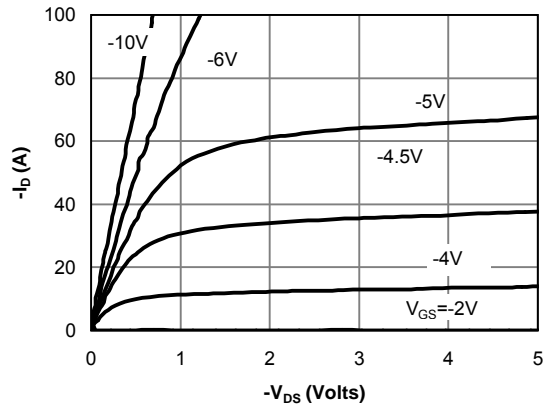
F: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

G: The maximum current rating is limited by the package current capability.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



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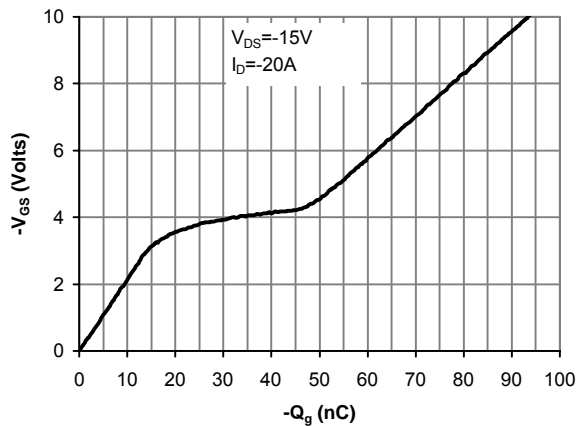


Figure 7: Gate-Charge Characteristics

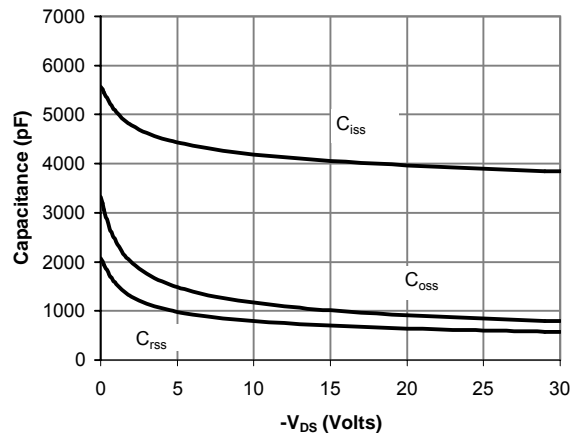


Figure 8: Capacitance Characteristics

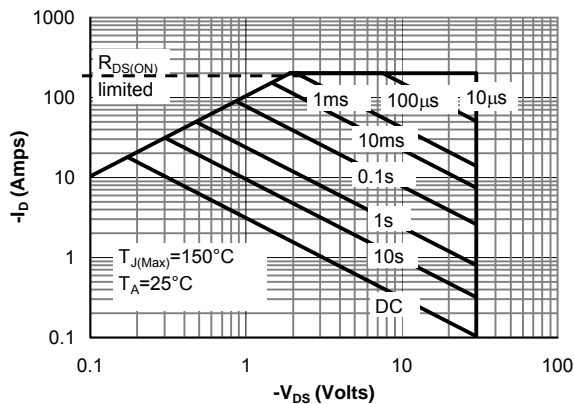


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

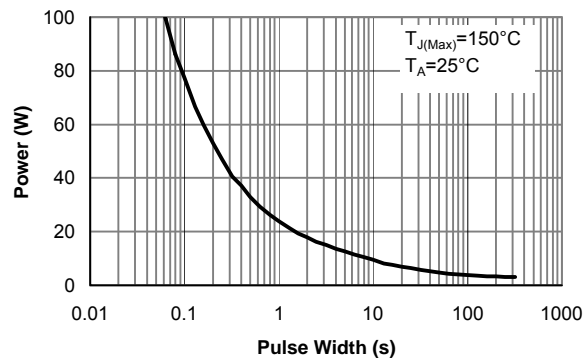


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

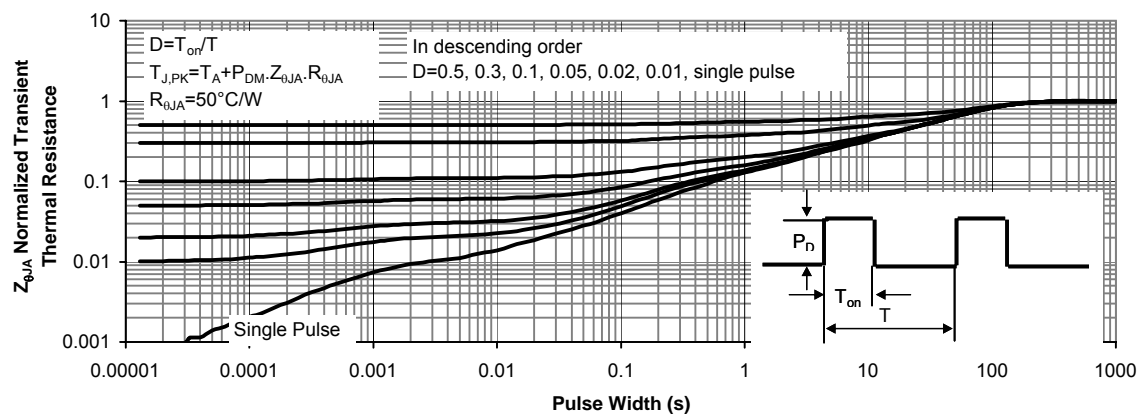


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)