3A Charger Interface, Wide Input Sensorless CC/CV Synchronous-Rectified Buck Converter for QC2.0

General Description

The uP9602 is certified by Qualcomm® and UL for QC2.0. The uP9602 is a high-efficiency synchronous-rectified buck converter with an internal power switch. With internal low RDS(ON) switches, the high-efficiency buck converter is capable of delivering up to 3A output current for charger interface and a wide input voltage range from 8V to 29V. It operates in either CV (Constant Output Voltage) mode or CC (Constant Output Current) mode and provides a current limitation function. The uP9602 has a constant output voltage 5.1V/9V/12V for Quick Charge 2.0 (QC2.0) that is detected from D+ and D- line and automatically detects whether a connected Powered Device (PD) is Quick Charge 2.0 capable before enabling output voltage adjustment. If a PD not compliant to Quick Charge 2.0 is detected, the uP9602 disables output voltage adjustment to ensure safe operation with legacy 5.1V only USB PDs.

Other features for the buck converter include internal soft-start, adjustable external CC (Constant Output Current) limit setting, built-in fixed line-compensation, short circuit protection, VIN/VOUT over voltage protection, and over temperature protection. It is available in a space saving PSOP-8L package.

Ordering Information

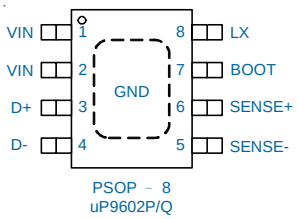
Order Number	Package Type	Top Marking
uP9602PSW8	PSOP-8L	uP9602P
uP9602QSW8	PSOP-8L	uP9602Q

Note:

(1) Please check the sample/production availability with uPI representatives.

(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration



PSOP – 8
uP9602P/Q

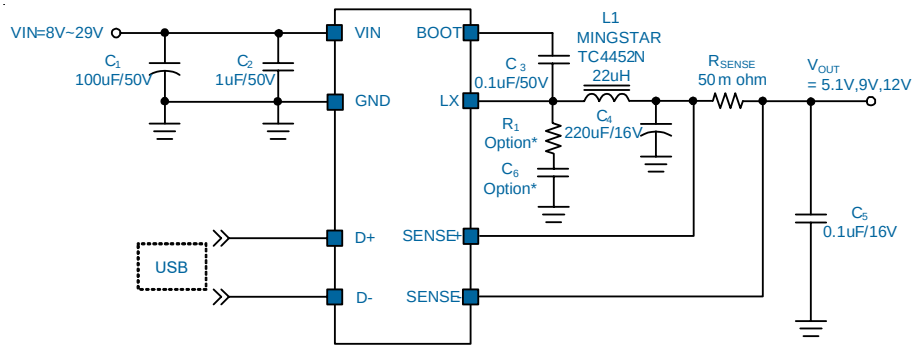
Features

- **Certification: uP9602 is certified by Qualcomm® and UL. Please refer to the information below for verification:**
  - **UL Certificate No. 4786937378-2**
  - **http://www.qualcomm.com/documents/quick-charge-device-list**
- **Wide Input Voltage Range : 8V to 29V**
- **Input Voltage Absolute Maximum Rating: 36V**
- **Up to 3A Output Current**
- **CV/CC Mode Control (Constant Voltage and Constant Current)**
- **Internal QC2.0 Function**
- **Internal USB2.0 and BC1.2**
- **Output Constant Voltage: 5.1V/9V/12V**
- **Output Voltage Accuracy: ±1.5%**
- **Fixed 135kHz Frequency Operation**
- **Up to 95% Conversion Efficiency**
- **Internal Soft Start: 10ms**
- **Fixed Cable Compensation Voltage**
- **Adjustable External CC (Constant Output Current) Limit Setting: Default = 2.6A**
- **CC (Constant Output Current) Limit Accurarcy:±3%**
- **Short Circuit Protection**
- **VIN/VOUT Over Voltage Protection and Over Temperature Protections**
- **PSOP-8L Package**
- **RoHS Compliant and Halogen Free**

Applications

- **PDA Like Device Car Chargers**
- **Portable Charging Devices**

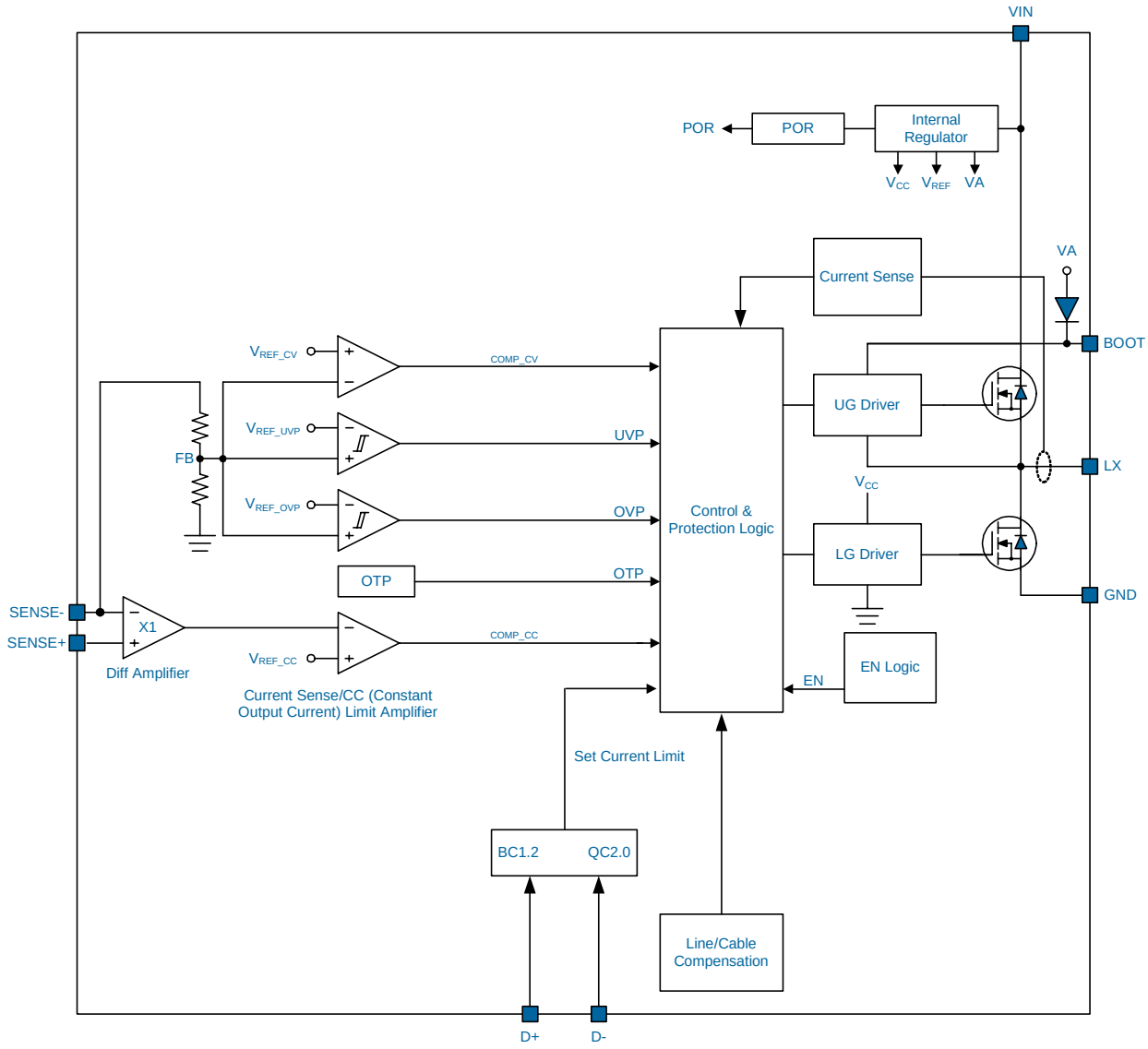
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1,2	VIN	**Power Supply Input**. Input voltage that supplies current to the output voltage and powers the internal control circuit. Bypass the input voltage with a minimum 1uFx1 X5R or X7R ceramic capacitor.
3	D+	**USB Port D+ Input Connection.** USB D+ data line input**.**
4	D-	**USB Port D- Input Connection.** USB D- data line input.
5	SENSE-	**The Current Sense Input (-) Pin.** Adjustable line and cable compensation voltage.
6	SENSE+	**The Current Sense Input (+) Pin.** Adjustable line and cable compensation voltage.
7	BOOT	**Bootstrap Supply for the Floating Upper Gate Driver.** Connect the bootstrap capacitor C BOOT between BOOT pin and the LX pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Typical value for C BOOT is 0.1uF or greater. Ensure that C BOOT is placed near the IC.
8	LX	**Internal Switches Output.** Connect this pin to the output inductor.
Exposed Pad (GND)		**Ground.** Ground of the buck converter. The exposed pad is the main path for heat convection and should be well-soldered to the PCB for best thermal performance.

Functional Block Diagram



Functional Description

CV/CC Mode Control

The uP9602 provides CV/CC function. It operates in either CV (Constant Output Voltage) mode or CC (Constant Output Current) mode. The function provides a current limitation function and adjusts external current limit setting (Default=2.6A). In the CV mode, the output voltage is controlled within ±1.5%. In the CC mode, the output current variation is less than ±3% of the nominal value which can be set up to 3A by the current sensing resistor.
When Output current increase until it reaches the CC limit set by the R_{SENSE} resistor. At this point, the device will transition from regulating output voltage to regulating output current, and the output voltage will drop with increasing load.

The CC (Constant Output Current) limit is set at 2.6A by default with an external resistance R_{SENSE} = 50mΩ, When the (SENSE1+) - (SENSE1-) voltage gets higher than 130mV and reaches the current limit, the driver is turned off. The CC (Constant Output Current) limit is set according to the following equation:

$$\text{CC (Constant Output Current) Limit} = \frac{130\text{mV}}{R_{SENSE}}$$

Output Cable Resistance Compensation

In charger applications, the large load will cause voltage drop in the output cable. The uP9602 has a built-in cable compensation function. When the load increases, the cable compensator will increase an adjustable regulation of the error amplifier that can make the output voltage constant. Use the curve and table to adjust internal the reference voltage values for fixed USB cable compensation by outside resistance R_{SENSE} = 50mΩ (default), as shown in Figure 1 and Table 1.The fixed cable compensation is calculated as follows:

$$V_{COMP} = I_{LOAD} \times R_{COMP}$$

R_{COMP}(mΩ)	60
I_{LOAD}(mA)	Fixed USB Cable Compensation Voltage (mV)
0	0
500	0
1000	60
1500	90
2000	120
2500	150
3000	180

Table 1 USB Cable Compensation Application Table

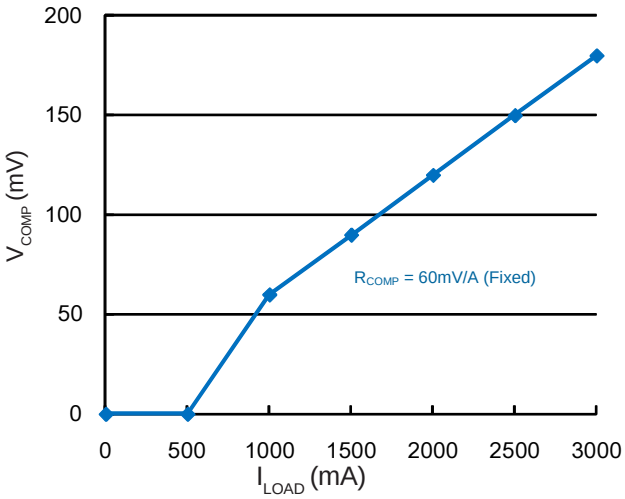


Figure 1 USB Cable Compensation at a Fixed Resistor Divider Value

Current Limit Protection

The uP9602 continuously monitors the inductor current, when the inductor current is higher than current limit threshold, the current limit function activates and forces the upper switch turning off to limit inductor current cycle by cycle.

Output Short Circuit Protection

The uP9602 provides output short circuit protection function. Once the output loader short-circuits, the SCP will be triggered then always hiccup, the hiccup cycle time is set by an internal counter. When the SCP condition is removed or disappears, the converter will resume normal operation and the hiccup status will terminate.

Output Over Voltage Protection

The uP9602 provides output over voltage protection. Once the output voltage (measured the at SENSE- pin) gets higher than OVP threshold, the OVP will be triggered to shut down the converter. When the OVP condition disappears, the converter will resume normal operation and resume the normal state automatically.

Over Temperature Protection

The OTP is triggered and shuts down the uP9602 if the junction temperature is higher than 150°C The OTP is a non-latch type protection. The uP9602 automatically initiates another soft start cycle if the junction temperature drops below 130°C.

Functional Description

Quick Charge 2.0 High Voltage Dedicated Charging Port (HVDCP)Specifications

The HVDCP specification details a simple method for a downstream device to request a higher voltage from the upstream AC/DC adapter while maintaining USB battery Charging 1.2 compatibility and allowing compatibility with other specifications that use the USB ID pin or communicate on USB VBUS. There is Class A of HVDCP upstream devices, class A must be capable of outputting 5.1V at the beginning, and then 9V or 12V. These voltages are based on the capabilities of the downstream device. The downstream device will request an output voltage for the HVDCP.

Quick Charge 2.0 Interface

The uP9602 supports the full output voltage range of Quick Charge 2.0 Class A (5.1V, 9V, or 12V), but does not support Class B (5.1V, 9V, 12V, or 20V). It automatically detects either Quick Charge 2.0 capable powered devices (PD) or legacy PDs compliant with the USB Battery Charging Specification 1.2 and only enables output voltage adjustment accordingly.

The uP9602 with D+ and D- short-circuited the normall handshake between the AC-DC adapter and powered devices (PD) as described in the USB Battery Charging Specification 1.2 can commence. After uP9602 starts monitoring the voltage level at D+. If D+ continuously stays above 0.325 V for at least 1.25 seconds and will enter Quick Charge 2.0 operation mode. If the voltage at D+ drops any time below 0.325 V resets the 1.25 seconds timer and stays in USB Battery Charging Specification 1.2 compatibility mode with a default output voltage of 5.1V.

Once uP9602 has entered Quick Charge 2.0 operation mode, a 19.53 kΩ pull-down resistor is connected to D-. As soon as the voltage at D- has dropped low (<0.325 V) for at least 1 ms starts accepting requests for different AC-DC adapter output voltages by means of applied voltage levels at data lines D+ and D- through the powered device. Table 2 is HVDCP fourth detection voltage and status.

Portable Device		HVDCP		
D+	D-	Output Voltage	Output Current	Current Limit
0.6V	GND	5.1V	2.4A	Default 2.6A±3%
0.6V	0.6V	12V	2.0A	Default 2.6A±3%
3.3V	0.6V	9V	2.0A	Default 2.6A±3%
0.6V	3.3V	Reserved		

Table 2 HVDCP Fourth Detection Voltage And Status

Note: GND is not forced by the portable device. The portable device shall go High-Z and the HVDCP pulls D- low through Rdm_dwn. This is to prevent misdetection when current flowing through GND causes the GND in the portable device to be at a higher voltage relative to HVDCP GND. Care should be taken in the portable device as this can result in a negative relative voltage on D- as seen by the portable device.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VIN ---------- -0.3V to +36V
SW Voltage to GND ---------- -0.3V to + (VIN + -0.3V)
D+/D- Pin Voltage ---------- -0.3V to +6.0V
SENSE+/SENSE- Pin Voltage ---------- -0.3V to +14V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
D+/D-/Sense- Pin
HBM (Human Body Mode) ---------- 4kV
MM (Machine Mode) ---------- 400V
Other Pins
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
PSOP - 8L θ_{JA} ---------- 47°C/W
PSOP - 8L θ_{JC} ---------- 17.9°C/W
Power Dissipation, P_D @ T_A = 25°C
PSOP - 8L ---------- 2.13W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{IN} ---------- +8V to 29V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(V_{IN} = 12V, T_A =25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input Voltage						
Input Voltage Range	V_{IN}		8	--	29	V
VIN POR Threshold		VIN Rising	--	7.50	--	V
		VIN Falling	--	7	--	V
Input OVP Threshold	V_{IN_OVP}	V_{IN_OVP} Rising	29.3	--	--	V
		V_{IN_OVP} Falling	29	--	--	V
Supply Input Current						
Input Quiescent Current	I_Q	No switching	--	1	1.50	mA
Power Switches						
Hi-Side Switch On Resistance	$R_{DS(ON)}$		--	100	--	mΩ
Low-Side Switch On Resistance	$R_{DS(ON)}$		--	100	--	mΩ
Oscillation Frequency	f_{OSC}		--	135	--	kHz
Maximum Duty Cycle	D_{MAX}		95	97	98	%
Output Voltage						
Output Voltage Accuracy	ΔV_{OUT}	V_{IN} = 12V, V_{OUT} = 5.1V	-1.50	--	+1.50	%
		V_{IN} = 12V, V_{OUT} = 9V	-1.50	--	+1.50	%
		V_{IN} = 24V, V_{OUT} = 12V	-1.50	--	+1.50	%
Soft Start						
Soft Start Time	T_{SS}		--	10	--	ms
Current Sense Amplifier						
Voltage Difference Between SENSE+ and SENSE- at CC Mode Operation	ΔV_{SEN}	V_{OUT} = 5.1V	126.1	130	133.9	mV
Protection						
CC (Constant Output Current) Limit	I_{OUT}	R_{SENSE} = 50mΩ, V_{OUT} = 5.1V	2.53	2.60	2.67	A
		R_{SENSE} = 43.33mΩ, V_{OUT} = 5.1V	2.91	3	3.09	A
Output Voltage needs to collapse threshold	V_{OUT}	Into CC (Constant Output Current) Limit	--	1.50	--	V
Output Over Voltage Protection	V_{OVP}	V_{OUT} = 5.1V, measured at V_{SENSE-}	--	10	--	%
		V_{OUT} = 9V, measured at V_{SENSE-}	--	10	--	%
		V_{OUT} = 12V, V_{IN} = 24V measured at V_{SENSE-}	--	10	--	%
Thermal Shutdown Temprature	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	T_{SDHYS}		--	20	--	°C

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
High Voltage Dedicated Charging Port (D+/D-)						
Data Detect Voltage	V_{DAT_REF}		0.25	0.325	0.40	V
Output Voltagte Selection Reference	V_{SEL_REF}	2.0V Reference for Selection HVDCP Voltage	1.80	2	2.20	V
Current Limit for HVDCP at Any Output Voltage	I_{HVDCP_MIN}	All HVDCP's must output this current at minimum	500	--	--	mA
D- Low Glitch Filter Time	$T_{GLITCHP\_DM\_LOW}$	After D+/- A are open and Rdm_dwn is asserted, how long should HVDCP expect D- to stay low before being pulled high.	1	--	--	ms
D- High Glitch Filter Time	$T_{GLITCHP\_DM\_HIGH}$	After D+/- A are open and Rdm_dwn is asserted, how long after a portable device sees D- go low, before it makes first voltage request and pulls D-high.	40	--	--	ms
D+ High Glitch Filter Time	$T_{GLITCHP\_BC\_Done}$	After BC1.2 Detection is complete, HVDCP	1	--	1.50	s
Output Voltage Glitch Filter Time	$T_{GLITCHP\_V\_CHANGE}$	Glitch filter after D+/- toggle before HVDCP attempts to change output voltage	20	40	60	ms
Unplug Vbus Discharge	T_{V_UNPLUG}	Time for Vbus to discharge to 5.1V in HVDCP on unplug	--	--	500	ms
D+/D- HVDCP Short Time	$T_{D+\_D-\_SHORT}$	Time for D+/D- to short on HVDCP	--	10	20	ms
D+D- Capacitance	C_{DCP_PWR}	Equivalent capacitance on D+ and D- to GND	--	--	1	nF
Data Line Leakage	R_{DAT_LKG}		300	--	1500	kΩ
D- Pull Down Resistance	R_{D-_DWN}		14.25	19.53	24.80	kΩ
BC 1.2 DCP Mode (Short Mode)						
D+ to D- Resistance During DCP Mode	R_{DCP_DAT}	For uP9602P/Q only	--	20	40	Ω
D+ Output Voltage	$V_{DP\_1.2V+}$	VIN = 12V, for uP9602P only	1.12	1.20	1.28	V
D- Output Voltage	$V_{DM\_1.2V+}$	VIN = 12V, for uP9602P only	1.12	1.20	1.28	V
D+ Output Impedance	$R_{DP\_1.2V}$	ID+ = -5uA, for uP9602P only	80	102	130	kΩ
D- Output Impedance	$V_{DM\_1.2V+}$	ID- = -5uA, for uP9602P only	80	102	130	kΩ
Divider Mode (2.7V/2.7V) for uP9602P only						
D+ Output Voltage	$V_{D+\_2.7V}$	VIN = 12V	2.57	2.70	2.84	V
D+ Output Voltage	$V_{D-\_2.7V}$	VIN = 12V	2.57	2.70	2.84	V
D+ Output Impedance	$R_{D+\_2.7V}$	ID+ = -5uA	--	36	--	kΩ
D+ Output Impedance	$R_{D-\_2.7V}$	ID- = -5uA	--	36	--	kΩ

Typical Operation Characteristics

This page is intentionally left blank and will be updated when data is available.

Output Inductor Selection

Output inductor selection is usually based on the considerations of inductance, rated current value, size requirements and DC resistance (DCR).

The inductance is chosen based on the desired ripple current. Large value inductors result in lower ripple currents and small value inductors result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in the equation below. A reasonable starting point for setting ripple current is ΔI_L = 900mA (30% of 3000mA).

$$\Delta I_L = \frac{1}{f_{OSC} \times L_{OUT}} \times V_{OUT} (1 - \frac{V_{OUT}}{V_{IN}})$$

Maximum current ratings of the inductor are generally specified in two methods: permissible DC current and saturation current. Permissible DC current is the allowable DC current that causes 40ºC temperature raise. The saturation current is the allowable current that causes 10% inductance loss. Make sure that the inductor will not saturate over the operation conditions including temperature range, input voltage range, and maximum output current. If possible, choose an inductor with rated current higher than 5A so that it will not saturate even under current limit condition.

The size requirements refer to the area and height requirement for a particular design. For better efficiency, choose a low DC resistance inductor. DCR is usually inversely proportional to size.

Different core materials and shapes will change the size, current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends on the price vs. size requirements and any radiated field/EMI requirements.

Input Capacitor Selection

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 22uF. The best choice is he ceramic type and low ESR electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. In the case of the electrolytic types, they can be further away if a small parallel 1uF ceramic capacitor is placed right close to the IC. A 100uF elecrolytic capacitor and 1uF ceramic capacitor are recommended and placed close to VIN and GND pins, with the shortest traces possible.

Output Capacitor Selection

The ESR of the output capacitor determines the output ripple voltage and the initial voltage drop following a high slew rate load transient edge. The output ripple voltage can be calculated as:

$$\Delta V_{OUT} = \Delta I_C \times (ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}})$$

Where f_{OSC} = operating frequency, C_{OUT} = output capacitance and $\Delta I_C = \Delta I_L$ = ripple current in the inductor. The ceramic capacitor with low ESR value provides the low output ripple and low size profile.

In the case of electrolytic capacitors, the ripple is dominated by R_{ESR} multiplied by the ripple current. Connect a 220uF electrolytic capacitor at output SENSE+ terminal for good performance and low output ripple and place output capacitor5s as close as possible to the device.

In the case of ceramic output capacitors, R_{ESR} is very small and does not contribute to the output ripple. Connect a 0.1uF ceramic capacitor at output SENSE- terminal for good performance and place output capacitors as close as possible to the device.

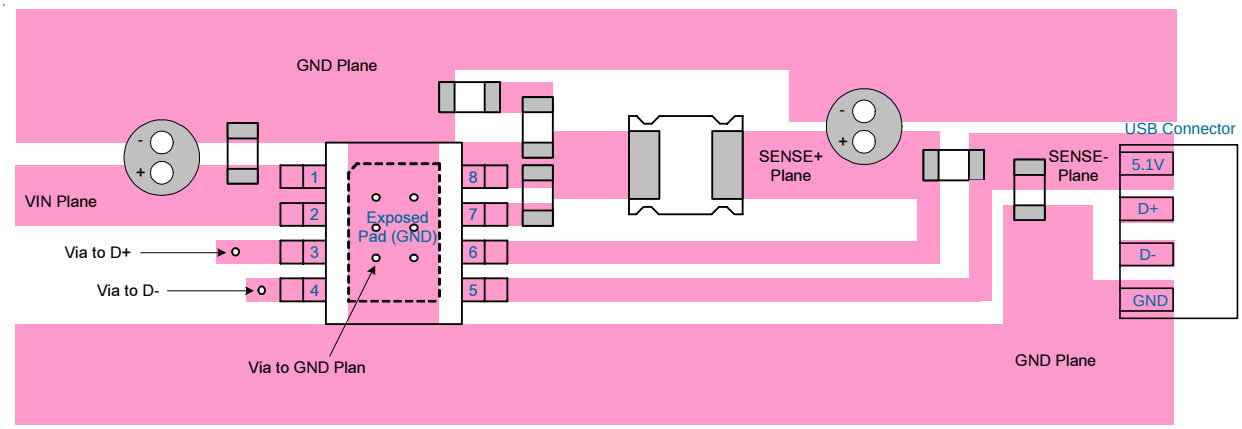
PCB Layout Consideration

The PCB layout is an important step to maintain the high performance of the uP9602. High switching frequencies and relatively large peak currents make the PCB layout a very important part of all high frequency switching power supply design. Both the high current and the fast switching nodes demand full attention to the PCB layout to save the robustness of the uP9602 through the PCB layout. Improper layout might show the symptoms of poor load or lineregulation, radiate excessive noise at ground or input, output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. Follow the PCB layout guidelines for optiomal performances of uP9602.

Application Information

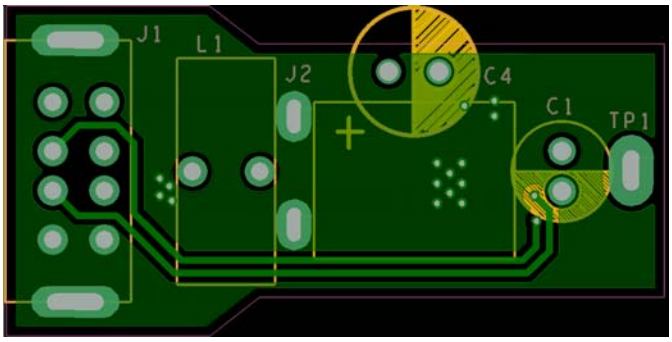
Layout Guidelines:

- Arrange the power components to reduce the AC loop size consisting of C_{IN}, VIN (Pin 1, 2) and LX (Pin 8)
- The input decoupling ceramic capacitor 1uF must be placed closest to the VIN (Pin 1, 2) and Exposed Pad GND plane through vias or a short and wide path.
- Return SENSE+ (PIN 6) to signal GND pin, and connect the signal GND to power GND at a single point for best noise immunity. Connect exposed pad to power ground copper area with copper and vias.
- Apply copper plane to Exposed Pad GND for best heat dissipation and noise immunity. The exposed pad is the main path for heat convection and should be well-soldered to the PCB for best thermal performance.
- Use a short trace connecting the bootstrap capacitor C_{BOOT} to BOOT (Pin 7) and LX (Pin 8) to form a bootstrap circuit.
- Use a short trace connecting R-C to LX (Pin 8) and Exposed Pad GND Plane to form a Snubber Circuit.
- The LX (Pin 6) pad is the noise node switching from VIN (Pin 1, 2) to GND. LX node copper area should be minimized to reduce EMI and should be isolated from the rest of circuit for good EMI and low noise operation.

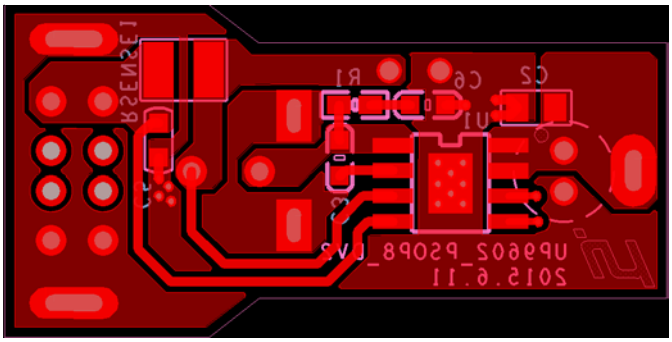


uP9602P/Q

PCB Layout Examples:



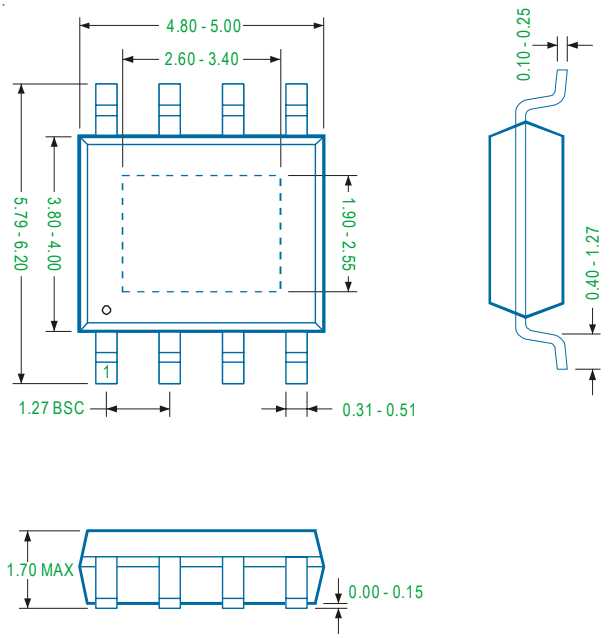
Top View



Bottom View

Package Information

PSOP - 8L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Important Notice

uPI and its subsidiaries reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

uPI products are sold subject to the taerms and conditions of sale supplied at the time of order acknowledgment. However, no responsibility is assumed by uPI or its subsidiaries for its use or application of any product or circuit; nor for any infringements of patents or other rights of third parties which may result from its use or application, including but not limited to any consequential or incidental damages. No uPI components are designed, intended or authorized for use in military, aerospace, automotive applications nor in systems for surgical implantation or life-sustaining. No license is granted by implication or otherwise under any patent or patent rights of uPI or its subsidiaries.

uPI Semiconductor Corp.
Headquarter
9F.,No.5, Taiyuan 1st St. Zhubei City,
Hsinchu Taiwan, R.O.C.
TEL : 886.3.560.1666 FAX : 886.3.560.1888

Sales Branch Office
12F-5, No. 408, Ruiguang Rd. Neihu District,
Taipei Taiwan, R.O.C.
TEL : 886.2.8751.2062 FAX : 886.2.8751.5064