

**BATTERY PROTECTION IC (FOR A 2-SERIAL-CELL PACK)****S-8232 Series**

The 8232 is a series of lithium-ion rechargeable battery protection ICs incorporating high-accuracy voltage detection circuits and delay circuits.

The S-8232 is suitable for a 2-serial-cell lithium-ion battery pack.

## ■ Features

- (1) Internal high-accuracy voltage detection circuit
  - Overcharge detection voltage 3.90 V  $\pm$  25 mV to 4.60 V  $\pm$  25 mV  
5 mV- step
  - Overcharge release voltage 3.60 V  $\pm$  50 mV to 4.60 V  $\pm$  50 mV  
5 mV- step

(The Overcharge release voltage can be selected within the range where a difference from Overcharge detection voltage is 0 to 0.3 V)
  - Overdischarge detection voltage 1.70 V  $\pm$  80 mV to 2.60 V  $\pm$  80 mV  
50 mV- step
  - Overdischarge release voltage 1.70 V  $\pm$  100 mV to 3.80 V  $\pm$  100 mV  
50 mV - step

(The Overdischarge release voltage can be selected within the range where a difference from Overdischarge detection voltage is 0 to 1.2 V)
  - Overcurrent detection voltage 1 0.07 V  $\pm$  20 mV to 0.30 V  $\pm$  20 mV  
5 mV-step
- (2) High input-voltage device (absolute maximum rating: 18 V)
- (3) Wide operating voltage range: 2.0 V to 16 V
- (4) The delay time for every detection can be set via an external capacitor.  
Each delay time for Overcharge detection, Overdischarge detection, Overcurrent detection are "Proportion of hundred to ten to one."
- (5) Two overcurrent detection levels (protection for short-circuiting)
- (6) Internal auxiliary over voltage detection circuit (Fail safe for over voltage)
- (7) Internal charge circuit for 0 V battery (Unavailable is option)
- (8) Low current consumption
  - Operation 7.5  $\mu$ A typ. 14.2  $\mu$ A max (–40 to +85 °C)
  - Power-down mode 0.2 nA typ. 0.1  $\mu$ A max (–40 to +85 °C)
- (9) TSSOP package (8-pin) 6.4 mm $\times$ 3.1 mm

## ■ Applications

Lithium-ion rechargeable battery packs

## ■ Package

8-PinTSSOP (PKG code:FT008-A)

■ Selection Guide (01 .Nov ,2001)

Table1

Model/Item	Overcharge detection voltage <sup>1,2</sup> ( $V_{CU1,2}$ )	Overcharge release voltage <sup>1,2</sup> ( $V_{CD1,2}$ )	Overdischarge detection voltage <sup>1,2</sup> ( $V_{DD1,2}$ )	Overdischarge release voltage <sup>1,2</sup> ( $V_{DU1,2}$ )	Overcurrent detection voltage <sup>1</sup> ( $V_{IOV1}$ )	Overcharge detection delay time ( $t_{CU}$ ) C3=0.22 $\mu$ F	0 V battery charging function
S-8232AAFT	4.25V $\pm$ 25mV	4.05 $\pm$ 50mV	2.40V $\pm$ 80mV	3.00V $\pm$ 100mV	0.150V $\pm$ 20mV	1.0 s	Available
S-8232ABFT	4.35V $\pm$ 25mV	4.15 $\pm$ 50mV	2.30V $\pm$ 80mV	3.00V $\pm$ 100mV	0.300V $\pm$ 20mV	1.0 s	Available
S-8232ACFT	4.35V $\pm$ 25mV	4.15 $\pm$ 50mV	2.30V $\pm$ 80mV	3.00V $\pm$ 100mV	0.300V $\pm$ 20mV	1.0 s	Unavailable
S-8232AEFT	4.35V $\pm$ 25mV	4.28 $\pm$ 50mV	2.15V $\pm$ 80mV	2.80V $\pm$ 100mV	0.100V $\pm$ 20mV	1.0 s	Available
S-8232AFFT	4.25V $\pm$ 25mV	4.05 $\pm$ 50mV	2.30V $\pm$ 80mV	2.70V $\pm$ 100mV	0.300V $\pm$ 20mV	1.0 s	Available
S-8232AGFT	4.25V $\pm$ 25mV	4.05 $\pm$ 50mV	2.20V $\pm$ 80mV	2.40V $\pm$ 100mV	0.200V $\pm$ 20mV	1.0 s	Available
S-8232AHFT	4.25V $\pm$ 25mV	4.05 $\pm$ 50mV	2.20V $\pm$ 80mV	2.40V $\pm$ 100mV	0.300V $\pm$ 20mV	1.0 s	Available
S-8232AIFT	4.325V $\pm$ 25mV	4.325V $\pm$ 25mV <sup>1),2)</sup>	2.40V $\pm$ 80mV	3.00V $\pm$ 100mV	0.300V $\pm$ 20mV	1.0 s	Unavailable
S-8232AJFT	4.25V $\pm$ 25mV	4.05 $\pm$ 50mV	2.40V $\pm$ 80mV	3.00V $\pm$ 100mV	0.150V $\pm$ 20mV	1.0 s	Unavailable
S-8232AKFT	4.20V $\pm$ 25mV	4.00 $\pm$ 50mV	2.30V $\pm$ 80mV	2.90V $\pm$ 100mV	0.200V $\pm$ 20mV	1.0 s	Available
S-8232ALFT	4.30V $\pm$ 25mV	4.05 $\pm$ 50mV	2.00V $\pm$ 80mV	3.00V $\pm$ 100mV	0.200V $\pm$ 20mV	1.0 s	Available
S-8232AMFT	4.19V $\pm$ 25mV	4.19 V $\pm$ 25mV <sup>1)</sup>	2.00V $\pm$ 80mV	3.00V $\pm$ 100mV	0.190V $\pm$ 20mV	1.0 s	Available
S-8232ANFT	4.325V $\pm$ 25mV	4.325V $\pm$ 25mV <sup>1),3)</sup>	2.40V $\pm$ 80mV	3.00V $\pm$ 100mV	0.300V $\pm$ 20mV	1.0 s	Unavailable
S-8232AOFT	4.30V $\pm$ 25mV	4.05 $\pm$ 50mV	2.00V $\pm$ 80mV	3.00V $\pm$ 100mV	0.230V $\pm$ 20mV	1.0 s	Available
S-8232APFT	4.28V $\pm$ 25mV	4.05 $\pm$ 50mV	2.30V $\pm$ 80mV	2.90V $\pm$ 100mV	0.100V $\pm$ 20mV	1.0 s	Unavailable
S-8232ARFT	4.325V $\pm$ 25mV	4.325V $\pm$ 25mV <sup>1),3)</sup>	2.00V $\pm$ 80mV	2.50V $\pm$ 100mV	0.300V $\pm$ 20mV	1.0 s	Unavailable
S-8232ASFT <sup>4)</sup>	4.295V $\pm$ 25mV	4.20 $\pm$ 50mV <sup>3)</sup>	2.30V $\pm$ 80mV	3.00V $\pm$ 100mV	0.300V $\pm$ 20mV	1.0 s	Unavailable
S-8232ATFT	4.125V $\pm$ 25mV	4.125 $\pm$ 25mV <sup>1)</sup>	2.00V $\pm$ 80mV	3.00V $\pm$ 100mV	0.190V $\pm$ 20mV	1.0 s	Available
S-8232AUFT	4.30V $\pm$ 25mV	4.10 $\pm$ 50mV	2.40V $\pm$ 80mV	3.00V $\pm$ 100mV	0.200V $\pm$ 20mV	1.0 s	Unavailable
S-8232AVFT	4.30V $\pm$ 25mV	4.05V $\pm$ 50mV	2.00V $\pm$ 80mV	3.00V $\pm$ 100mV	0.300V $\pm$ 20mV	1.0 s	Available
S-8232AWFT	4.35V $\pm$ 25mV	4.15V $\pm$ 50mV	2.30V $\pm$ 80mV	3.00V $\pm$ 100mV	0.150V $\pm$ 20mV	1.0 s	Unavailable
S-8232AXFT	4.325V $\pm$ 25mV	4.200V $\pm$ 50mV	2.30V $\pm$ 80mV	3.00V $\pm$ 100mV	0.20V $\pm$ 20mV	1.0 s	Unavailable
S-8232AYFT	4.30V $\pm$ 25mV	4.05V $\pm$ 50mV	2.00V $\pm$ 80mV	2.00V $\pm$ 80mV	0.20V $\pm$ 20mV	1.0 s	Available
S-8232AZFT	4.30V $\pm$ 25mV	4.05V $\pm$ 50mV	2.30V $\pm$ 80mV	2.30V $\pm$ 80mV	0.20V $\pm$ 20mV	1.0 s	Available
S-8232NAFT	4.325V $\pm$ 25mV	4.325V $\pm$ 25mV <sup>1)</sup>	2.40V $\pm$ 80mV	3.00V $\pm$ 100mV	0.15V $\pm$ 20mV	1.0 s	Unavailable

- 1): No overcharge detection/release hysteresis  
2): The magnification of final overcharge is 1.11; other is 1.25.  
3): No final overcharging function  
4): Refer to the Description of Operation (\*3).

Change in the detection voltage is available. Please contact SII sales office.

The overdischarge detection voltage can be selected within the range from 1.7 to 3.0 V.

When the overdischarge detection voltage is higher than 2.6 V, the overcharge detection voltage and the overcharge release voltage are limited as table 2.

Table 2

Overdischarge detection voltage <sup>1,2</sup> ( $V_{DD1,2}$ )	Overcharge detection voltage <sup>1,2</sup> ( $V_{CU1,2}$ )	Voltage difference between overcharge detection voltage and overcharge release voltage ( $V_{CU1,2} - V_{CD1,2}$ )
1.70 to 2.60 V	3.90 to 4.60 V	0 to 0.30 V
1.70 to 2.80 V	3.90 to 4.60 V	0 to 0.20 V
1.70 to 3.00 V	3.90 to 4.50 V	0 to 0.10 V

## ■ Block Diagram

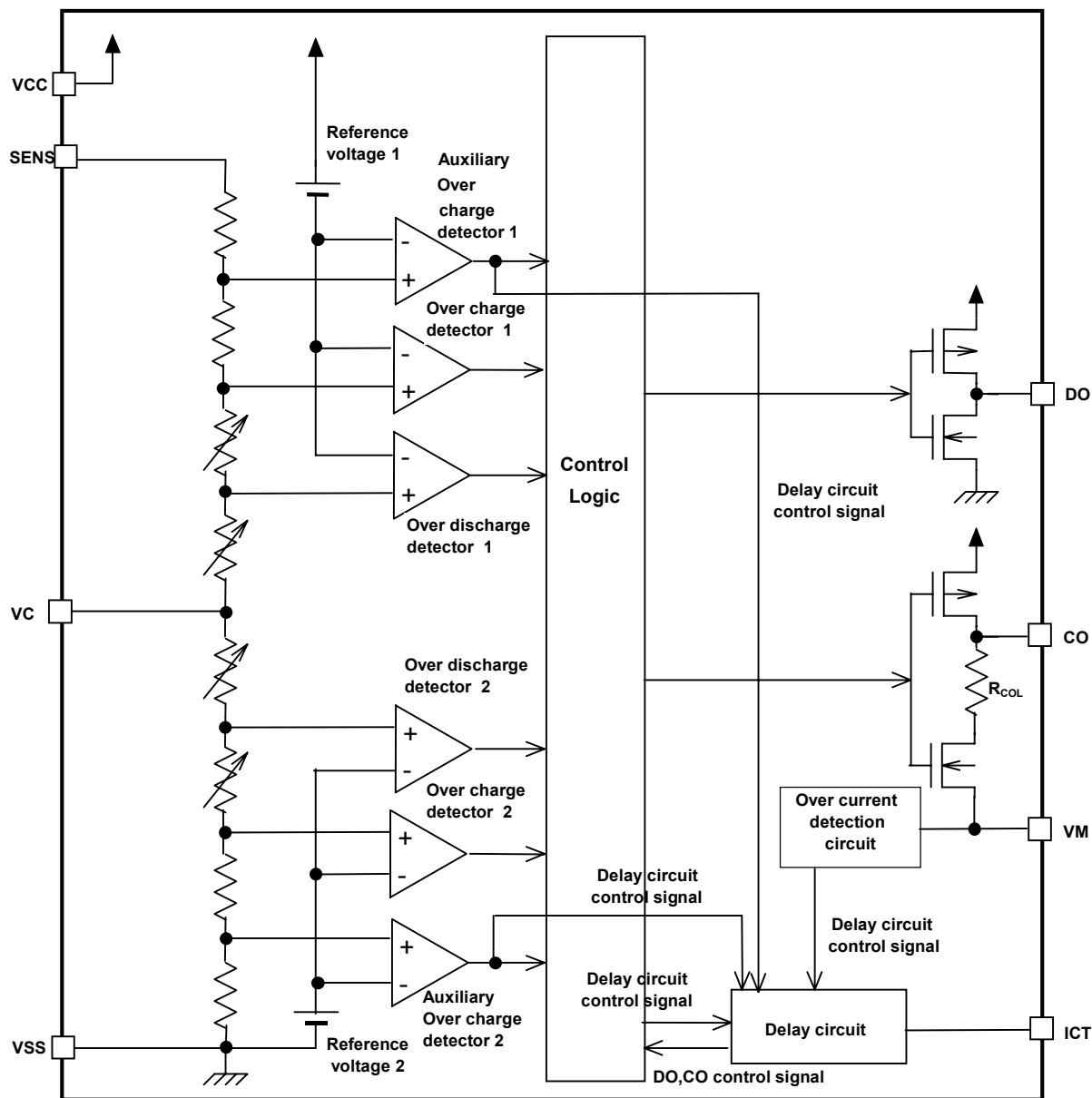
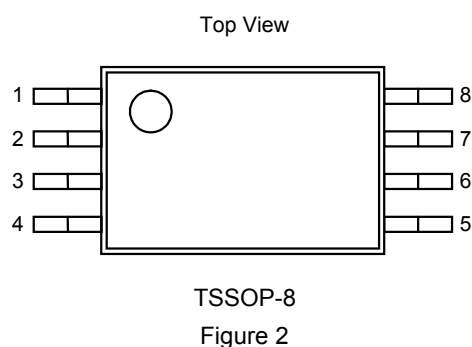


Figure 1

Output impedance when CO terminal output 'L' is higher than DO terminal.  $R_{COL}$  resistor is connected with CO terminal. Please refer 'Electric Characteristics'.

## ■ Pin Assignment



## ■ Pin Description

Table 3

No.	Name	Description
1	SENS	Detection pin for voltage between SENS and VC (Detection for overcharge and overdischarge)
2	DO	FET gate connection pin for discharge control (CMOS output)
3	CO	FET gate connection pin for charge control (CMOS output)
4	VM	Detection pin for voltage between VM and VSS (Overcurrent detection pin)
5	VSS	Negative power input pin
6	ICT	Capacitor connection pin for detection delay
7	VC	Middle voltage input pin
8	VCC	Positive power input pin

## ■ Absolute Maximum Ratings

Table 4

Ta = 25°C

Item	Symbol	Applied Pins	Rating	Unit
Input voltage between VCC and VSS	V <sub>DS</sub>	VCC	V <sub>SS</sub> -0.3 to V <sub>SS</sub> +18	V
SENS Input terminal voltage	V <sub>SENS</sub>	SENS	V <sub>SS</sub> -0.3 to V <sub>CC</sub> +0.3	V
ICT Input terminal voltage	V <sub>ICT</sub>	ICT	V <sub>SS</sub> -0.3 to V <sub>CC</sub> +0.3	V
VM Input terminal voltage	V <sub>VM</sub>	VM	V <sub>CC</sub> -18 to V <sub>CC</sub> +0.3	V
DO output terminal voltage	V <sub>DO</sub>	DO	V <sub>SS</sub> -0.3 to V <sub>CC</sub> +0.3	V
CO output terminal voltage	V <sub>CO</sub>	CO	V <sub>VM</sub> -0.3 to V <sub>CC</sub> +0.3	V
Power dissipation	P <sub>D</sub>		300	mW
Operating temperature range	T <sub>opr</sub>		-40 to +85	°C
Storage temperature range	T <sub>stg</sub>		-40 to +125	°C

## ■ Electrical Characteristics

Table 5

Unless otherwise noted, Ta = 25°C

Item	Symbol	Condition	Circuit	Notice	Min.	Typ.	Max.	Unit
<b>Detection voltage</b>								
Overcharge detection voltage 1,2	V <sub>CU1,2</sub>	1,2	1	Between 3.90 and 4.60	V <sub>CU1,2</sub> −0.025	V <sub>CU1,2</sub>	V <sub>CU1,2</sub> +0.025	V
Auxiliary overcharge detection voltage 1,2 <sup>(4)</sup> V <sub>CUaux1,2</sub> = V <sub>CU1,2</sub> × 1.25 or V <sub>CUaux1,2</sub> = V <sub>CU1,2</sub> × 1.11	V <sub>CUaux1,2</sub>	1,2	1	V <sub>CU1,2</sub> × 1.25	V <sub>CU1,2</sub> × 1.21	V <sub>CU1,2</sub> × 1.25	V <sub>CU1,2</sub> × 1.29	V
	V <sub>CUaux1,2</sub>	1,2	1	V <sub>CU1,2</sub> × 1.11	V <sub>CU1,2</sub> × 1.07	V <sub>CU1,2</sub> × 1.11	V <sub>CU1,2</sub> × 1.15	V
Overcharge release voltage 1,2	V <sub>CD1,2</sub>	1,2	1	Between 3.60 and 4.60	V <sub>CD1,2</sub> −0.050	V <sub>CD1,2</sub>	V <sub>CD1,2</sub> +0.050	V
Overdischarge detection voltage 1,2	V <sub>DD1,2</sub>	1,2	1	Between 1.70 and 2.60	V <sub>DD1,2</sub> −0.080	V <sub>DD1,2</sub>	V <sub>DD1,2</sub> +0.080	V
Overdischarge release voltage 1,2	V <sub>DU1,2</sub>	1,2	1	Between 1.70 and 3.80	V <sub>DU1,2</sub> −0.100	V <sub>DU1,2</sub>	V <sub>DU1,2</sub> +0.100	V
Overcurrent detection voltage 1	V <sub>IOV1</sub>	3	1	Between 0.07 to 0.30	V <sub>IOV1</sub> − 0.020	V <sub>IOV1</sub>	V <sub>IOV1</sub> + 0.020	V
Overcurrent detection voltage 2	V <sub>IOV2</sub>	3	1	V <sub>CC</sub> Reference	−1.57	−1.20	−0.83	V
Temperature coefficient 1 for detection voltage <sup>(1)</sup>	T <sub>COE1</sub>			Ta = −40 to 85°C	−0.6	0	0.6	mV/°C
Temperature coefficient 2 for detection voltage <sup>(2)</sup>	T <sub>COE2</sub>			Ta = −40 to 85°C	−0.24	−0.05	0	mV/°C
<b>Delay time (C3=0.22 μF)</b>								
Overcharge detection delay time 1,2	t <sub>CU1,2</sub>	8,9	5	1.0 s	0.73	1.00	1.35	s
Overdischarge detection delay time 1,2	t <sub>DD1,2</sub>	8,9	5	0.1 s	68	100	138	ms
Overcurrent detection delay time 1	t <sub>IOV1</sub>	10	5	0.01 s	6.7	10	13.9	ms
<b>Input voltage</b>								
Input voltage between VCC and VSS	V <sub>DS</sub>			Absolute maximum rating	−0.3	−	18	
<b>Operating voltage</b>								
Operating voltage between VCC and VSS <sup>(3)</sup>	V <sub>DSOP</sub>				2.0	−	16	V
<b>Current consumption</b>								
Current consumption during normal operation	I <sub>OPE</sub>	4	2	V1=V2=3.6 V	2.1	7.5	12.7	μA
Current consumption at power down	I <sub>PDN</sub>	4	2	V1=V2=1.5 V	0	0.0002	0.04	μA
<b>Output voltage</b>								
DO"H" voltage	V <sub>DO(H)</sub>	6	3	I <sub>out</sub> =10 μA	V <sub>CC</sub> −0.05	V <sub>CC</sub> −0.003	V <sub>CC</sub>	V
DO"L" voltage	V <sub>DO(L)</sub>	6	3	I <sub>out</sub> =10 μA	V <sub>SS</sub>	V <sub>SS</sub> +0.003	V <sub>SS</sub> +0.05	V
CO"H" voltage	V <sub>CO(H)</sub>	7	4	I <sub>out</sub> =10 μA	V <sub>CC</sub> −0.15	V <sub>CC</sub> −0.019	V <sub>CC</sub>	V
<b>CO pin internal resistance</b>								
Resistance between VSS and CO	R <sub>COL</sub>	7	4	V <sub>CO</sub> −V <sub>SS</sub> =9.4 V	0.29	0.6	1.44	MΩ
<b>Internal resistance</b>								
Resistance between VCC and VM	R <sub>vcm</sub>	5	2	V <sub>CC</sub> −V <sub>VM</sub> =0.5 V	105	240	575	kΩ
Resistance between VSS and VM	R <sub>vsm</sub>	5	2	V <sub>VM</sub> −V <sub>SS</sub> =1.1 V	511	597	977	kΩ
<b>0 V battery charging function</b>								
0 V charge starting voltage	V <sub>0CHA</sub>	11	6	0 V battery charging Available	0.38	0.75	1.12	V
0 V charge inhibiting voltage 1,2	V <sub>0INH1,2</sub>	12,13	6	0 V battery charging Unavailable	0.32	0.88	1.44	V

- (1) Temperature coefficient 1 for detection voltage should be applied to overcharge detection voltage, overcharge release voltage, overdischarge detection voltage, and overdischarge release voltage.
- (2) Temperature coefficient 2 for detection voltage should be applied to overcurrent detection voltage.
- (3) The DO and CO pin logic are established at the operating voltage.
- (4) Auxiliary overcharge detection voltage is equal to the overcharge detection voltage times 1.11 for the products without overcharge hysteresis, and times 1.25 for other products.

Table 6

Unless otherwise noted, Ta = -20 to +70°C

Item	Symbol	Condition	Circuit	Notice	Min.	Typ.	Max.	Unit
<b>Detection voltage</b>								
Overcharge detection voltage 1,2	V <sub>CU1,2</sub>	1,2	1	Between 3.90 and 4.60	V <sub>CU1,2</sub> -0.055	V <sub>CU1,2</sub>	V <sub>CU1,2</sub> +0.045	V
Auxiliary overcharge detection voltage 1,2 <sup>(4)</sup> V <sub>CUaux1,2</sub> = V <sub>CU1,2</sub> ×1.25 or V <sub>CUaux1,2</sub> = V <sub>CU1,2</sub> ×1.11	V <sub>CUaux1,2</sub>	1,2	1	V <sub>CU1,2</sub> ×1.25	V <sub>CU1,2</sub> ×1.19	V <sub>CU1,2</sub> ×1.25	V <sub>CU1,2</sub> ×1.31	V
	V <sub>CUaux1,2</sub>	1,2	1	V <sub>CU1,2</sub> ×1.11	V <sub>CU1,2</sub> ×1.05	V <sub>CU1,2</sub> ×1.11	V <sub>CU1,2</sub> ×1.17	V
Overcharge release voltage 1,2	V <sub>CD1,2</sub>	1,2	1	Between 3.60 and 4.60	V <sub>CD1,2</sub> -0.080	V <sub>CD1,2</sub>	V <sub>CD1,2</sub> +0.070	V
Overdischarge detection voltage 1,2	V <sub>DD1,2</sub>	1,2	1	Between 1.70 and 2.60	V <sub>DD1,2</sub> -0.110	V <sub>DD1,2</sub>	V <sub>DD1,2</sub> +0.100	V
Overdischarge release voltage 1,2	V <sub>DU1,2</sub>	1,2	1	Between 1.70 and 3.80	V <sub>DU1,2</sub> -0.130	V <sub>DU1,2</sub>	V <sub>DU1,2</sub> +0.120	V
Overcurrent detection voltage 1	V <sub>IOV1</sub>	3	1	Between 0.07 to 0.30	V <sub>IOV1</sub> -0.033	V <sub>IOV1</sub>	V <sub>IOV1</sub> +0.033	V
Overcurrent detection voltage 2	V <sub>IOV2</sub>	3	1	V <sub>CC</sub> Reference	-1.70	-1.20	-0.71	V
Temperature coefficient 1 for detection voltage <sup>(1)</sup>	T <sub>COE1</sub>			Ta=-40 to 85°C	-0.6	0	0.6	mV/°C
Temperature coefficient 2 for detection voltage <sup>(2)</sup>	T <sub>COE2</sub>			Ta=-40 to 85°C	-0.24	-0.05	0	mV/°C
<b>Delay time (C3=0.22 μF)</b>								
Overcharge detection delay time1,2	t <sub>CU1,2</sub>	8,9	5	1.0 s	0.55	1.00	2.06	s
Overdischarge detection delay time 1,2	t <sub>DD1,2</sub>	8,9	5	0.1 s	67	100	141	ms
Overcurrent detection delay time1	t <sub>IOV1</sub>	10	5	0.01 s	6.3	10	14.7	ms
<b>Input voltage</b>								
Input voltage between VCC and VSS	V <sub>DS</sub>			Absolute maximum rating	-0.3	-	18	
<b>Operating voltage</b>								
Operating voltage between VCC and VSS <sup>(3)</sup>	V <sub>DSOP</sub>				2.0	-	16	V
<b>Current consumption</b>								
Current consumption during normal operation	I <sub>OPE</sub>	4	2	V1=V2=3.6 V	1.8	7.5	14.2	μA
Current consumption at power down	I <sub>PDN</sub>	4	2	V1=V2=1.5 V	0	0.0002	0.10	μA
<b>Output voltage</b>								
DO"H"voltage	V <sub>DO(H)</sub>	6	3	I <sub>out</sub> =10 μA	V <sub>CC</sub> -0.14	V <sub>CC</sub> -0.003	V <sub>CC</sub>	V
DO"L"voltage	V <sub>DO(L)</sub>	6	3	I <sub>out</sub> =10 μA	V <sub>SS</sub>	V <sub>SS</sub> +0.003	V <sub>SS</sub> +0.14	V
CO"H"voltage	V <sub>CO(H)</sub>	7	4	I <sub>out</sub> =10 μA	V <sub>CC</sub> -0.24	V <sub>CC</sub> -0.019	V <sub>CC</sub>	V
<b>CO pin internal resistance</b>								
Resistance between VSS and CO	R <sub>COL</sub>	7	4	V <sub>CO</sub> -V <sub>SS</sub> =9.4 V	0.22	0.6	2.20	MΩ
<b>Internal resistance</b>								
Resistance between VCC and VM	R <sub>vcm</sub>	5	2	V <sub>CC</sub> -V <sub>VM</sub> =0.5 V	79	240	878	kΩ
Resistance between VSS and VM	R <sub>vsm</sub>	5	2	V <sub>VM</sub> -V <sub>SS</sub> =1.1 V	387	597	1491	kΩ
<b>0 V battery charging function</b>								
0 V charge starting voltage	V <sub>0CHA</sub>	11	6	0 V battery charging Available	0.26	0.75	1.25	V
0 V charge inhibiting voltage 1,2	V <sub>0INH1,2</sub>	12,13	6	0 V battery charging Unavailable	0.20	0.88	1.57	V

- (1) Temperature coefficient 1 for detection voltage should be applied to overcharge detection voltage, overcharge release voltage, overdischarge detection voltage, and overdischarge release voltage.
- (2) Temperature coefficient 2 for detection voltage should be applied to overcurrent detection voltage.
- (3) The DO and CO pin logic are established at the operating voltage.
- (4) Auxiliary overcharge detection voltage is equal to the overcharge detection voltage times 1.11 for the products without overcharge hysteresis, and times 1.25 for other products.

Table 7

Unless otherwise noted, Ta = -40 to +85°C

Item	Symbol	Condition	Circuit	Notice	Min.	Typ.	Max.	Unit
<b>Detection voltage</b>								
Overcharge detection voltage 1,2	V <sub>CU1,2</sub>	1,2	1	Between 3.90 and 4.60	V <sub>CU1,2</sub> -0.055	V <sub>CU1,2</sub>	V <sub>CU1,2</sub> +0.045	V
Auxiliary overcharge detection voltage 1,2 <sup>(4)</sup> V <sub>CUaux1,2</sub> = V <sub>CU1,2</sub> × 1.25 or V <sub>CUaux1,2</sub> = V <sub>CU1,2</sub> × 1.11	V <sub>CUaux1,2</sub>	1,2	1	V <sub>CU1,2</sub> × 1.25	V <sub>CU1,2</sub> × 1.19	V <sub>CU1,2</sub> × 1.25	V <sub>CU1,2</sub> × 1.31	V
	V <sub>CUaux1,2</sub>	1,2	1	V <sub>CU1,2</sub> × 1.11	V <sub>CU1,2</sub> × 1.05	V <sub>CU1,2</sub> × 1.11	V <sub>CU1,2</sub> × 1.17	V
Overcharge release voltage 1,2	V <sub>CD1,2</sub>	1,2	1	Between 3.60 and 4.60	V <sub>CD1,2</sub> -0.080	V <sub>CD1,2</sub>	V <sub>CD1,2</sub> +0.070	V
Overdischarge detection voltage 1,2	V <sub>DD1,2</sub>	1,2	1	Between 1.70 and 2.60	V <sub>DD1,2</sub> -0.110	V <sub>DD1,2</sub>	V <sub>DD1,2</sub> +0.100	V
Overdischarge release voltage 1,2	V <sub>DU1,2</sub>	1,2	1	Between 1.70 and 3.80	V <sub>DU1,2</sub> -0.130	V <sub>DU1,2</sub>	V <sub>DU1,2</sub> +0.120	V
Overcurrent detection voltage 1	V <sub>IOV1</sub>	3	1	Between 0.07 to 0.30	V <sub>IOV1</sub> - 0.033	V <sub>IOV1</sub>	V <sub>IOV1</sub> + 0.033	V
Overcurrent detection voltage 2	V <sub>IOV2</sub>	3	1	V <sub>CC</sub> Reference	-1.70	-1.20	-0.71	V
Temperature coefficient 1 for detection voltage <sup>(1)</sup>	T <sub>COE1</sub>			Ta = -40 to 85°C	-0.6	0	0.6	mV/°C
Temperature coefficient 2 for detection voltage <sup>(2)</sup>	T <sub>COE2</sub>			Ta = -40 to 85°C	-0.24	-0.05	0	mV/°C
<b>Delay time (C3=0.22 μF)</b>								
Overcharge detection delay time 1,2	t <sub>CU1,2</sub>	8,9	5	1.0 s	0.55	1.00	2.06	s
Overdischarge detection delay time 1,2	t <sub>DD1,2</sub>	8,9	5	0.1 s	67	100	141	ms
Overcurrent detection delay time 1	t <sub>IOV1</sub>	10	5	0.01 s	6.3	10	14.7	ms
<b>Input voltage</b>								
Input voltage between VCC and VSS	V <sub>DS</sub>			Absolute maximum rating	-0.3	-	18	
<b>Operating voltage</b>								
Operating voltage between VCC and VSS <sup>(3)</sup>	V <sub>DSOP</sub>				2.0	-	16	V
<b>Current consumption</b>								
Current consumption during normal operation	I <sub>OPE</sub>	4	2	V1=V2=3.6 V	1.8	7.5	14.2	μA
Current consumption at power down	I <sub>PDN</sub>	4	2	V1=V2=1.5 V	0	0.0002	0.10	μA
<b>Output voltage</b>								
DO"H" voltage	V <sub>DO(H)</sub>	6	3	I <sub>out</sub> =10 μA	V <sub>CC</sub> -0.17	V <sub>CC</sub> -0.003	V <sub>CC</sub>	V
DO"L" voltage	V <sub>DO(L)</sub>	6	3	I <sub>out</sub> =10 μA	V <sub>SS</sub>	V <sub>SS</sub> +0.003	V <sub>SS</sub> +0.17	V
CO"H" voltage	V <sub>CO(H)</sub>	7	4	I <sub>out</sub> =10 μA	V <sub>CC</sub> -0.27	V <sub>CC</sub> -0.019	V <sub>CC</sub>	V
<b>CO pin internal resistance</b>								
Resistance between VSS and CO	R <sub>COL</sub>	7	4	V <sub>CO</sub> -V <sub>SS</sub> =9.4 V	0.22	0.6	2.20	MΩ
<b>Internal resistance</b>								
Resistance between VCC and VM	R <sub>VCM</sub>	5	2	V <sub>CC</sub> -V <sub>VM</sub> =0.5 V	79	240	878	kΩ
Resistance between VSS and VM	R <sub>VSM</sub>	5	2	V <sub>VM</sub> -V <sub>SS</sub> =1.1 V	387	597	1491	kΩ
<b>0 V battery charging function</b>								
0 V charge starting voltage	V <sub>0CHA</sub>	11	6	0 V battery charging Available	0.26	0.75	1.25	V
0 V charge inhibiting voltage 1,2	V <sub>0INH1,2</sub>	12,13	6	0 V battery charging Unavailable	0.20	0.88	1.57	V

- (1) Temperature coefficient 1 for detection voltage should be applied to overcharge detection voltage, overcharge release voltage, overdischarge detection voltage, and overdischarge release voltage.
- (2) Temperature coefficient 2 for detection voltage should be applied to overcurrent detection voltage.
- (3) The DO and CO pin logic are established at the operating voltage.
- (4) Auxiliary overcharge detection voltage is equal to the overcharge detection voltage times 1.11 for the products without overcharge hysteresis, and times 1.25 for other products.

## ■ Measurement Circuits

### (1) Measurement 1 Measurement circuit 1

Set  $S1=OFF$ ,  $V1=V2=3.6\text{ V}$ , and  $V3=0\text{ V}$  under normal condition. Increase  $V1$  from  $3.6\text{ V}$  gradually. The  $V1$  voltage when  $CO = 'L'$  is overcharge detection voltage 1 ( $V_{CU1}$ ). Decrease  $V1$  gradually. The  $V1$  voltage when  $CO = 'H'$  is overcharge release voltage 1 ( $V_{CD1}$ ). Further decrease  $V1$ . The  $V1$  voltage when  $DO = 'L'$  is overdischarge voltage 1 ( $V_{DD1}$ ). Increase  $V1$  gradually. The  $V1$  voltage when  $DO = 'H'$  is overdischarge release voltage 1 ( $V_{DU1}$ ). Set  $S1=ON$ , and  $V1=V2=3.6\text{ V}$  and  $V3=0\text{ V}$  under normal condition. Increase  $V1$  from  $3.6\text{ V}$  gradually. The  $V1$  voltage when  $CO = 'L'$  is auxiliary overcharge detection voltage 1 ( $V_{CUaux1}$ ).

### (2) Measurement 2 Measurement circuit 1

Set  $S1=OFF$ ,  $V1=V2=3.6\text{ V}$ , and  $V3=0\text{ V}$  under normal condition. Increase  $V2$  from  $3.6\text{ V}$  gradually. The  $V2$  voltage when  $CO = 'L'$  is overcharge detection voltage 2 ( $V_{CU2}$ ). Decrease  $V2$  gradually. The  $V2$  voltage when  $CO = 'H'$  is overcharge release voltage 2 ( $V_{CD2}$ ). Further decrease  $V2$ . The  $V2$  voltage when  $DO = 'L'$  is overdischarge voltage 2 ( $V_{DD2}$ ). Increase  $V2$  gradually. The  $V2$  voltage when  $DO = 'H'$  is overdischarge release voltage 2 ( $V_{DU2}$ ). Set  $S1=ON$ , and  $V1=V2=3.6\text{ V}$  and  $V3=0\text{ V}$  under normal condition. Increase  $V2$  from  $3.6\text{ V}$  gradually. The  $V2$  voltage when  $CO = 'L'$  is auxiliary overcharge detection voltage 2 ( $V_{CUaux2}$ ).

### (3) Measurement 3 Measurement circuit 1

Set  $S1=OFF$ ,  $V1=V2=3.6\text{ V}$ , and  $V3=0\text{ V}$  under normal condition. Increase  $V3$  from  $0\text{ V}$  gradually. The  $V3$  voltage when  $DO = 'L'$  is overcurrent detection voltage 1 ( $V_{IOV1}$ ). Set  $S1=ON$ ,  $V1=V2=3.6\text{ V}$ ,  $V3=0$  under normal condition. Increase  $V3$  from  $0\text{ V}$  gradually. (The voltage change rate  $< 1.0\text{V/ms}$ ) ( $V1+V2-V3$ ) voltage when  $DO = 'L'$  is overcurrent detection voltage 2 ( $V_{IOV2}$ ).

### (4) Measurement 4 Measurement circuit 2

Set  $S1=ON$ ,  $V1=V2=3.6\text{ V}$ , and  $V3=0\text{ V}$  under normal condition and measure current consumption. Current consumption  $I1$  is the normal condition current consumption ( $I_{OPE}$ ). Set  $S1=OFF$ ,  $V1=V2=1.5\text{ V}$  under overdischarge condition and measure current consumption. Current consumption  $I1$  is the power-down current consumption ( $I_{PDN}$ ).

### (5) Measurement 5 Measurement circuit 2

Set  $S1=ON$ ,  $V1=V2=V3=1.5\text{ V}$ , and  $V3=2.5\text{ V}$  under overdischarge condition.  $(V1+V2-V3)/I2$  is the internal resistance between  $VCC$  and  $VM$  ( $R_{vcm}$ ).

Set  $S1=ON$ ,  $V1=V2=3.5\text{ V}$ , and  $V3=1.1\text{ V}$  under overcurrent condition.  $V3/I2$  is the internal resistance between  $VSS$  and  $VM$  ( $R_{vsm}$ ).

### (6) Measurement 6 Measurement circuit 3

Set  $S1=ON$ ,  $S2=OFF$ ,  $V1=V2=3.6\text{ V}$ , and  $V3=0\text{ V}$  under normal condition. Increase  $V4$  from  $0\text{ V}$  gradually. The  $V4$  voltage when  $I1 = 10\text{ }\mu\text{A}$  is  $DO'H'$  voltage ( $V_{DO(H)}$ ).

Set  $S1=OFF$ ,  $S2=ON$ ,  $V1=V2=3.6\text{ V}$ , and  $V3=0.5\text{ V}$  under overcurrent condition. Increase  $V5$  from  $0\text{ V}$  gradually. The  $V5$  voltage when  $I2 = 10\text{ }\mu\text{A}$  is the  $DO'L'$  voltage ( $V_{DO(L)}$ ).

### (7) Measurement 7 Measurement circuit 4

Set  $S1=ON$ ,  $S2=OFF$ ,  $V1=V2=3.6\text{ V}$  and  $V3=0\text{ V}$  under normal condition. Increase  $V4$  from  $0\text{ V}$  gradually. The  $V4$  voltage when  $I1 = 10\text{ }\mu\text{A}$  is the  $CO'H'$  voltage ( $V_{CO(H)}$ ).

Set  $S1=OFF$   $S2=ON$ ,  $V1=V2=4.7$ ,  $V3=0\text{ V}$ , and  $V4=9.4\text{ V}$  under over voltage condition.  $(V5)/I2$  is the  $CO$  pin internal resistance ( $R_{COL}$ ).

### (8) Measurement 8 Measurement circuit 5

Set  $V1=V2=3.6\text{ V}$ , and  $V3=0\text{ V}$  under normal condition. Increase  $V1$  from ( $V_{CU1}-0.2\text{ V}$ ) to ( $V_{CU1}+0.2\text{ V}$ ) immediately (within  $10\text{ }\mu\text{s}$ ). The time after  $V1$  becomes ( $V_{CU1}+0.2\text{ V}$ ) until  $CO$  goes 'L' is the overcharge detection delay time 1 ( $t_{CU1}$ ).



Set  $V1=V2=3.5\text{ V}$ , and  $V3=0\text{ V}$  under normal condition. Decrease  $V1$  from  $(V_{DD1}+0.2\text{ V})$  to  $(V_{DD1}-0.2\text{ V})$  immediately (within  $10\text{ }\mu\text{s}$ ). The time after  $V1$  becomes  $(V_{DD1}-0.2\text{ V})$  until  $DO$  goes 'L' is the overdischarge detection delay time 1 ( $t_{DD1}$ ).

#### (9) Measurement 9 Measurement circuit 5

Set  $V1=V2=3.6\text{ V}$ , and  $V3=0\text{ V}$  under normal condition. Increase  $V2$  from  $(V_{CU2}-0.2\text{ V})$  to  $(V_{CU2}+0.2\text{ V})$  immediately (within  $10\text{ }\mu\text{s}$ ). The time after  $V2$  becomes  $(V_{CU2}+0.2\text{ V})$  until  $CO$  goes 'L' is the overcharge detection delay time 2 ( $t_{CU2}$ ).

Set  $V1=V2=3.6\text{ V}$ , and  $V3=0\text{ V}$  under normal condition. Decrease  $V2$  from  $(V_{DD2}+0.2\text{ V})$  to  $(V_{DD2}-0.2\text{ V})$  immediately (within  $10\text{ }\mu\text{s}$ ). The time after  $V2$  becomes  $(V_{DD2}-0.2\text{ V})$  until  $DO$  goes 'L' is the overdischarge detection delay time 2 ( $t_{DD2}$ ).

#### (10) Measurement 10 Measurement circuit 5

Set  $V1=V2=3.6\text{ V}$ , and  $V3=0\text{ V}$  under normal condition. Increase  $V3$  from  $0\text{ V}$  to  $0.5\text{ V}$  immediately (within  $10\text{ }\mu\text{s}$ ). The time after  $V3$  becomes  $0.5\text{ V}$  until  $DO$  goes 'L' is the overcurrent detection delay time 1 ( $t_{OV1}$ ).

#### (11) Measurement 11 Measurement circuit 6

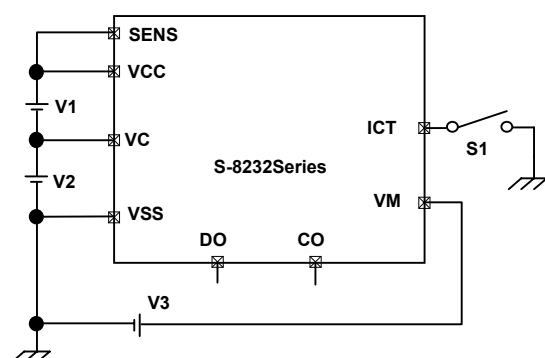
Set  $V1=V2=0\text{ V}$ , and  $V3=2\text{ V}$ , and decrease  $V3$  gradually. The  $V3$  voltage when  $CO = 'L'$  ( $V_{CC} - 0.3\text{ V}$  or lower) is the  $0\text{ V}$  charge starting voltage ( $V_{0CHA}$ ).

#### (12) Measurement 12 Measurement circuit 6

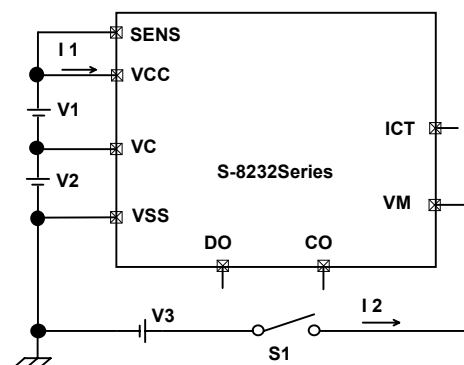
Set  $V1=0\text{ V}$ ,  $V2=3.6\text{ V}$ , and  $V3=12\text{ V}$ , and increase  $V1$  gradually. The  $V1$  voltage when  $CO = 'H'$  ( $V_{VM} + 0.3\text{ V}$  or higher) is the  $0\text{ V}$  charge inhibiting voltage 1 ( $V_{0INH1}$ ).

#### (13) Measurement 13 Measurement circuit 6

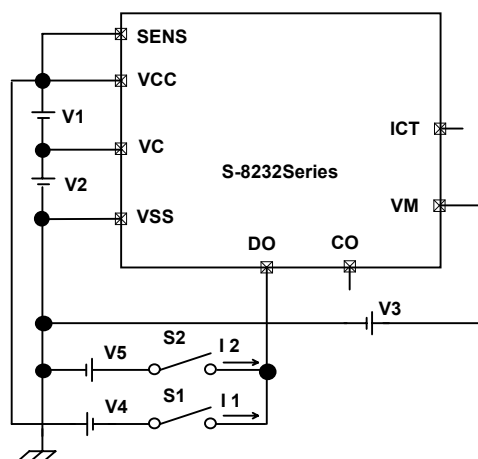
Set  $V1=3.6\text{ V}$ ,  $V2=0\text{ V}$ , and  $V3=12\text{ V}$ , and increase  $V2$  gradually. The  $V2$  voltage when  $CO = 'H'$  ( $V_{VM} + 0.3\text{ V}$  or higher) is the  $0\text{ V}$  charge inhibiting voltage 2 ( $V_{0INH2}$ ).



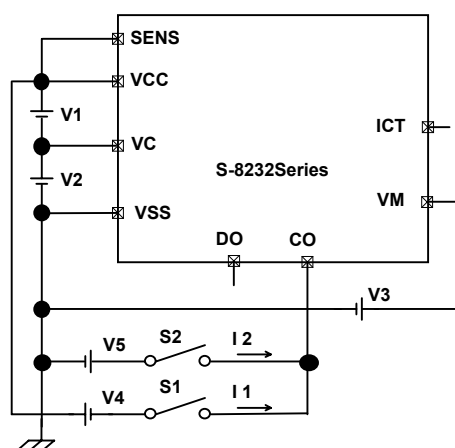
Measurement circuit 1



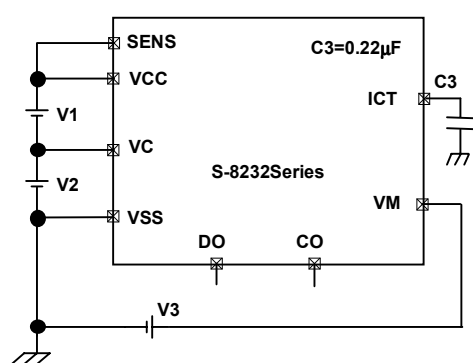
Measurement circuit 2



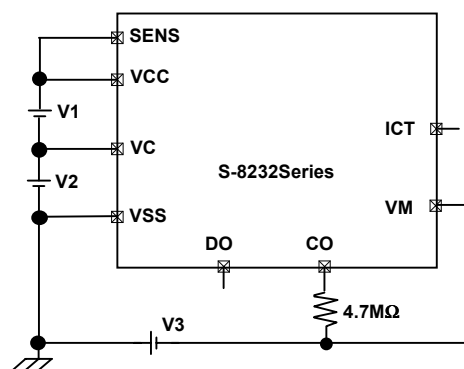
Measurement circuit 3



Measurement circuit 4



Measurement circuit 5



Measurement circuit 6

## ■ Description of Operation

### Normal condition <sup>(1), (3)</sup>

This IC monitors the voltages of the two serially connected batteries and the discharge current to control charging and discharging. When the voltages of two batteries are in the range from the overdischarge detection voltage ( $V_{DD1,2}$ ) to the overcharge detection voltage ( $V_{CU1,2}$ ), and the current flowing through the batteries becomes equal or lower than a specified value (the VM terminal voltage is equal or lower than overcurrent detection voltage 1), the charging and discharging FETs are turned on. In this condition, charging and discharging can be carried out freely. This condition is called normal condition. In this condition, the VM and VSS terminals are shorted by the  $R_{vsm}$  resistor.

### Overcurrent condition

When the discharging current becomes equal to or higher than a specified value (the VM terminal voltage is equal to or higher than the overcurrent detection voltage) during discharging under normal condition and it continues for the overcurrent detection delay time ( $t_{IOV}$ ) or longer, the discharging FET is turned off to stop discharging. This condition is called overcurrent condition. The VM and VSS terminals are shorted by the  $R_{vsm}$  resistor at this time. The charging FET is also turned off. When the discharging FET is off and a load is connected, the VM terminal voltage equals the  $V_{CC}$  potential.

The overcurrent condition returns to the normal condition when the load is released and the impedance between the EB– and EB+ terminals (see Figure 6 for a connection example) is 200 MΩ or higher. When the load is released, the VM terminal, which is shorted to the VSS terminal with the  $R_{vsm}$  resistor, goes back to the  $V_{SS}$  potential. The IC detects that the VM terminal potential returns to overcurrent detection voltage 1 ( $V_{IOV1}$ ) or lower and returns to the normal condition.

### Overcharge condition

Following two cases are detected as overcharge conditions:

- 1) If one of the battery voltages becomes higher than the overcharge detection voltage ( $V_{CU1,2}$ ) during charging under normal condition and it continues for the overcharge detection delay time ( $t_{CU1,2}$ ) or longer, the charging FET turns off to stop charging.
- 2) If one of the battery voltages becomes higher than the auxiliary overcharge detection voltage ( $V_{CUaux1,2}$ ) the charging FET turns off immediately to stop charging.

The VM and VSS terminals are shorted by the  $R_{vsm}$  resistor under the overcharge condition.

The auxiliary overcharge detection voltages ( $V_{CUaux1,2}$ ) are correlated with the overcharge detection voltages ( $V_{CU1,2}$ ) and are defined by following equations:

$$V_{CUaux1,2} [V] = 1.25 \times V_{CU1,2} [V]$$

or for no overcharge hysteresis type ( $V_{CU1,2} = V_{CD1,2}$ )

$$V_{CUaux1,2} [V] = 1.11 \times V_{CU1,2} [V]$$

The overcharge condition is released in two cases:

- 1) The battery voltage which exceeded the overcharge detection voltage ( $V_{CU1,2}$ ) falls below the overcharge release voltage ( $V_{CD1,2}$ ), the charging FET turns on and the normal condition returns.
- 2) If the battery voltage which exceeded the overcharge detection voltage ( $V_{CU1,2}$ ) is equal or higher than the overcharge release voltage ( $V_{CD1,2}$ ), but the charger is removed, a load is placed, and discharging starts, the charging FET turns on and the normal condition returns.

The release mechanism is as follows: the discharge current flows through an internal parasitic diode of the charging FET immediately after a load is installed and discharging starts, and the VM terminal voltage decreases by about 0.6 V from the VSS terminal voltage momentarily. The IC detects this voltage (overcurrent detection voltage 1 or higher), releases the overcharge condition and returns to the normal condition.

### Overdischarge condition

If any one of the battery voltages falls below the overdischarge detection voltage ( $V_{DD1,2}$ ) during discharging under normal condition and it continues for the overdischarge detection delay time ( $t_{DD1,2}$ ) or longer, the discharging FET turns off and discharging stops. This condition is called the overdischarge condition. When the discharging FET turns off, the VM terminal voltage becomes equal to the  $V_{CC}$  voltage and the IC's current consumption falls below the power-down current consumption ( $I_{PDN}$ ). This condition is called the power-down condition. The VM and VCC terminals are shorted by the  $R_{vcm}$  resistor under the overdischarge and power-down conditions.

The power-down condition is canceled when the charger is connected and the voltage between VM and VCC is overcurrent detection voltage 2 or higher. When all the battery voltages becomes equal to or higher than the overdischarge release voltage ( $V_{DU1,2}$ ) in this condition, the overdischarge condition changes to the normal condition.

### Delay circuits

The overcharge detection delay time ( $t_{CU1,2}$ ), the overdischarge detection delay time ( $t_{DD1,2}$ ), and the overcurrent detection delay time 1 ( $t_{IOV1}$ ) change with an external capacitor (C3). Since one capacitor determine each delay time, delay times are correlated by the following ratio:

$$\text{Overcharge delay time : Overdischarge delay time : Overcurrent delay time} = 100 : 10 : 1$$

The delay times are calculated by the following equations: ( $T_a = -40$  to  $+85^\circ\text{C}$ )

Overcharge detection delay time	Min.,	Typ.,	Max.
$t_{CU}[s]$	=Delay factor ( 2.500,	4.545,	9.364 ) $\times C3 [\mu F]$
Overdischarge detection delay time			
$t_{DD}[s]$	=Delay factor ( 0.3045,	0.4545,	0.6409 ) $\times C3 [\mu F]$
Overcurrent detection delay time			
$t_{IOV1}[s]$	=Delay factor ( 0.02864,	0.04545,	0.06682 ) $\times C3 [\mu F]$

Note: The delay time for overcurrent detection 2 is fixed by an internal circuit. The delay time cannot be changed via an external capacitor.

### 0 V battery charging function <sup>(2)</sup>

This function is used to recharge both of two serially-connected batteries after they self-discharge to 0 V. When the 0 V charging start voltage ( $V_{0CHA}$ ) or higher is applied to between VM and VCC by connecting the charger, the charging FET gate is fixed to  $V_{CC}$  potential. When the voltage between the gate sources of the charging FET becomes equal to or higher than the turn-on voltage by the charger voltage, the charging FET turns on to start charging. At this time, the discharging FET turns off and the charging current flows through the internal parasitic diode in the discharging FET. If all the battery voltages become equal to or higher than the overdischarge release voltage ( $V_{DU1,2}$ ), the normal condition returns.

### 0 V battery charge inhibiting function <sup>(2)</sup>

This function is used for inhibiting charging when either of the connected batteries goes 0 V due to its self-discharge. When the voltage of either of the connected batteries goes below 0 V charge inhibit voltage 1 and 2 ( $V_{\text{OINH1, 2}}$ ), the charging FET gate is fixed to "EB –" to inhibit charging. Charging is possible only when the voltage of both connected batteries goes 0 V charge inhibit voltage 1 and 2 ( $V_{\text{OINH1, 2}}$ ) or more.

Note that charging may be possible when the total voltage of both connected batteries is less than the minimum value ( $V_{\text{DSOPmin}}$ ) of the operating voltage between VCC-VSS even if the voltage of either of the connected batteries is 0 V charge inhibit voltage 1 and 2 ( $V_{\text{OINH1, 2}}$ ) or less. Charging is prohibited when the total voltage of both connected batteries reaches the minimum value ( $V_{\text{DSOPmin}}$ ) of the operating voltage between VCC-VSS.

When using this optional function, a resistor of 4.7 M $\Omega$  is needed between the gate and the source of the charging control FET (refer to Figure 6).

#### (1)

When initially connecting batteries, the IC may fail to enter the normal condition (discharging ready state). If so, once set the VM pin to VSS voltage (short pins VM and VSS or connect a charger).

#### (2)

Some lithium ion batteries are not recommended to be recharged after having been completely discharged. Please contact the battery manufacturer when you decide to select a 0 V battery charging function.

#### (3)

The products indicated with 4) in the Selection Guide (model name/item) are set to "overcharge detection/release hysteresis," "no final overcharge function," and "0 V battery charge inhibiting function." The following phenomena may be found, but there is no problem for practical use.

The product is an overcurrent condition due to overload connection when the battery voltage is overcharge release voltage ( $V_{\text{CD1, 2}}$ ) or more and overcharge detection voltage ( $V_{\text{CU1, 2}}$ ) or less. Usually, the IC returns to its normal condition when overload is removed under this condition. However, the charging FET may be turned OFF when overload is removed under this condition, leading to an overcharge condition. If so, attach load to start discharge. The charging FET is turned ON to return to the normal condition. Refer to "Overcharge condition" of description Section.

## ■ Operation Timing Charts

### 1. Overcharge detection

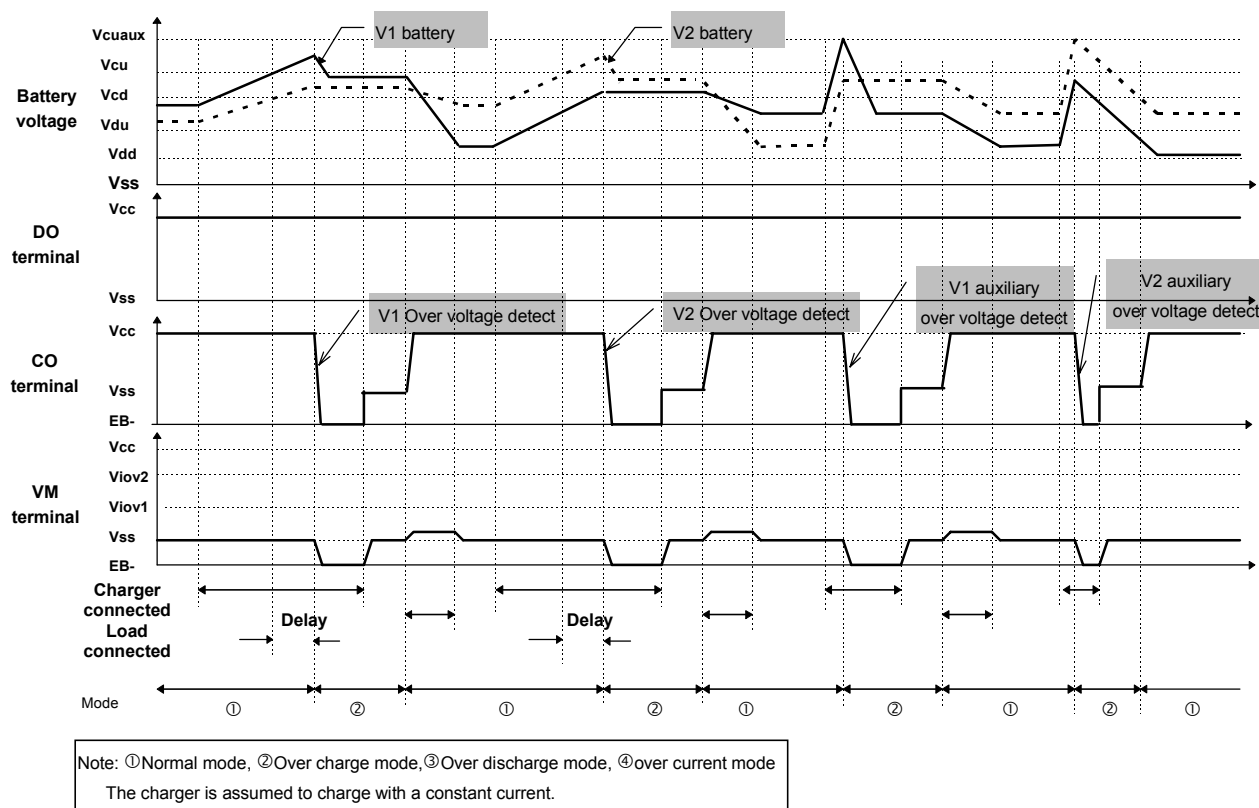


Figure 3

### 2. Overdischarge detection

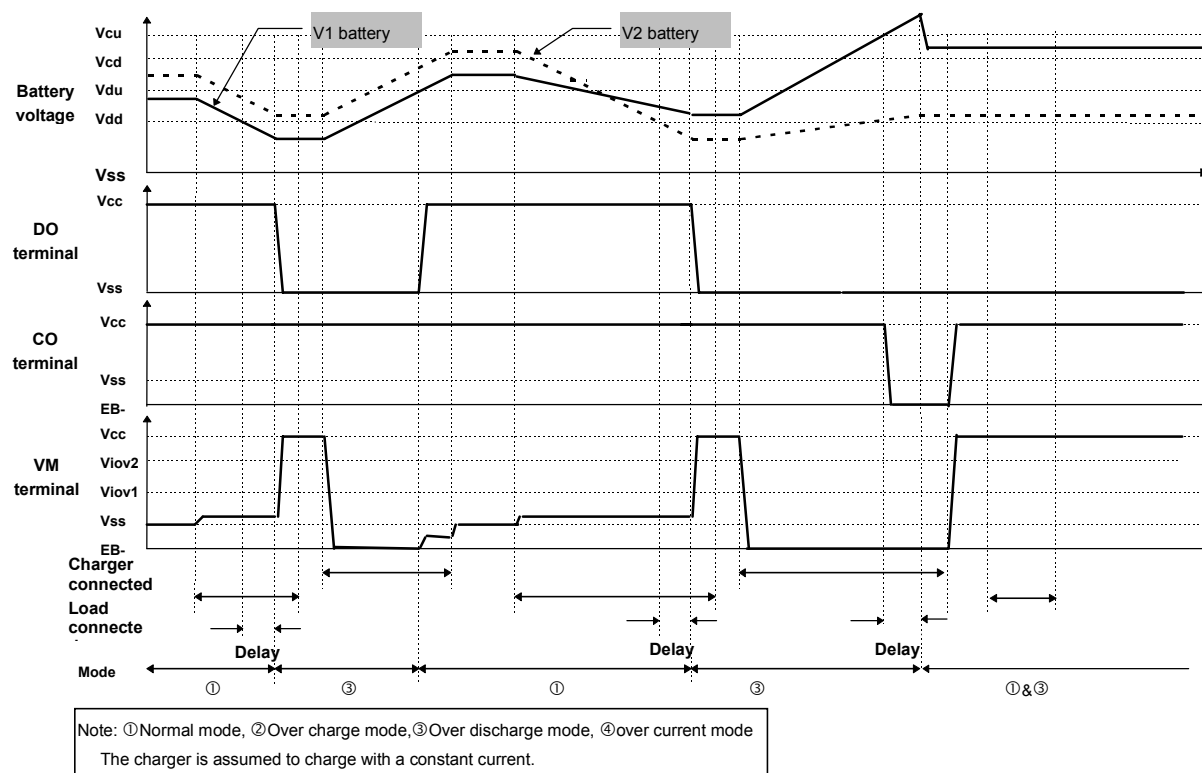


Figure 4

3. Overcurrent detection

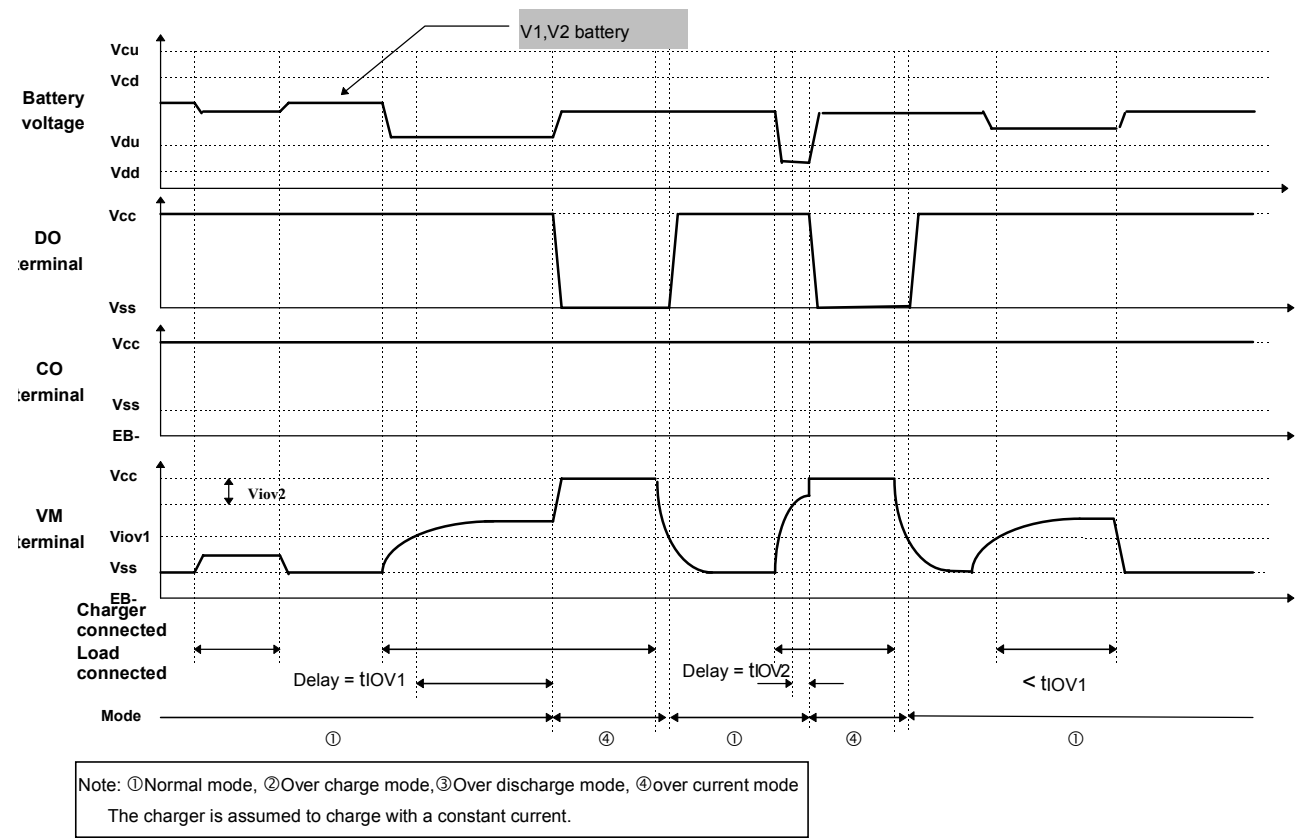


Figure 5

## ■ Battery Protection IC Connection Example

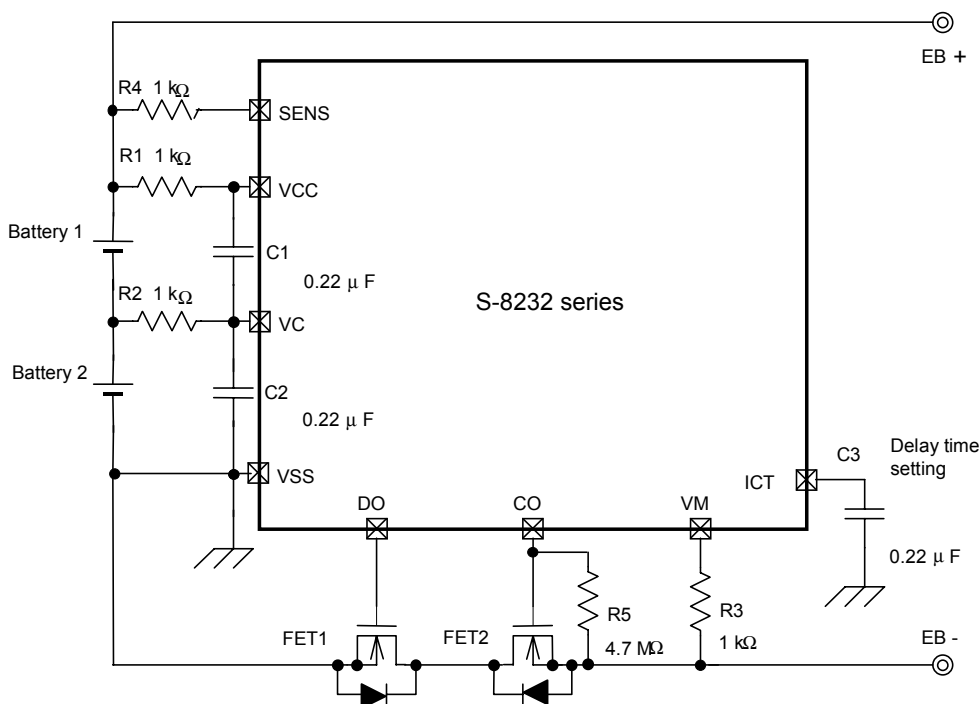


Figure 6

Table 8 Constant

Symbol	Parts	Purpose	Recom- mended	min.	max.	Remarks
<b>FET1</b>	Nch MOSFET	Charge control	-----	-----	-----	-----
<b>FET2</b>	Nch MOSFET	Discharge control	-----	-----	-----	-----
<b>R1</b>	Chip resistor	ESD protection	1 kΩ	300 Ω	1 kΩ	
<b>C1</b>	Chip capacitor	Filter	0.22 μF	0 μF	1 μF	
<b>R2</b>	Chip resistor	ESD protection	1 kΩ	300 Ω	1 kΩ	
<b>C2</b>	Chip capacitor	Filter	0.22 μF	0 μF	1 μF	
<b>R4</b>	Chip resistor	ESD protection	1 kΩ	=R1 min.	=R1 max.	1) Same value as R1 and R2
<b>C3</b>	Chip capacitor	Delay time setting	0.22 μF	0 μF	1 μF	2) Attention should be paid to leak current of C3.
<b>R3</b>	Chip resistor	Protection for charger reverse connection	1 kΩ	300 Ω	5 kΩ	3) Discharge can't be stopped at less than 300 Ω when a charger is reverse-connected.
<b>R5</b>	Chip resistor	0 V battery charging inhibition	(4.7 MΩ)	(1 MΩ)	(10MΩ)	4) R5 should be added when the product has 0 V battery charge inhibition. Lower resistance increases current consumption.

- 1)  $R4 = R1$  is required. Overcharge detection voltage increases by  $R4$ . For example 10 kΩ ( $R4$ ) increases overcharge detection voltage by 20 mV.
- 2) The overcharge detection delay time ( $t_{CU}$ ), the overdischarge detection delay time ( $t_{CD}$ ), and the over current detection delay time ( $t_{IOV}$ ) change with the external capacitor  $C3$ . See the electrical characteristics.
- 3) When the resistor  $R3$  is set less than 300 Ω and a charger is reverse-connected, current which exceeds the power dissipation of the package will flow and the IC may break. But excessive  $R3$  causes increase of overcurrent detection voltage 1 ( $V_{IOV1}$ ).  $V_{IOV1}$  changes to  $V_{IOV1} = (R3 + R_{VSM}) / R_{VSM} \times V_{IOV1}$ . For example 50 kΩ resistor ( $R3$ ) increases overcurrent detection voltage 1 ( $V_{IOV1}$ ) from 0.100 V to 0.113 V.
- 4) A 4.7 MΩ resistor is needed for  $R5$  to inhibit 0 V battery charging. Current consumption increases when the  $R5$  resistance increases.  $R5$  should be connected when the product has 0 V battery charging inhibition.

### Note:

The above connection diagram and constants do not guarantee proper operations. Evaluate your actual application and set constants properly.

## ■ Precautions

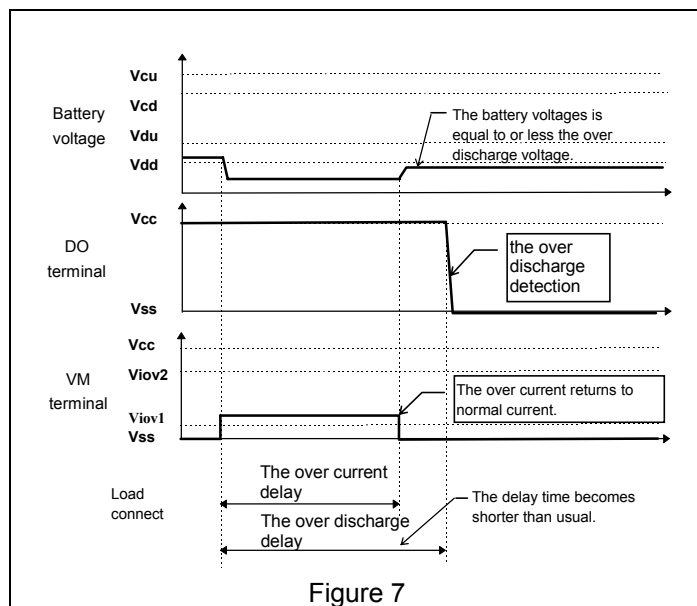
- (1) After the overcurrent detection delay, if the battery voltages is equals the overdischarge detection voltage ( $V_{DD1,2}$ ) or lower, the overdischarge detection delay time becomes shorter than 10ms (min.).  
It occurs because capacitor C3 sets all of delay times. (Refer fig.7)

### [ Cause ]

It occurs because capacitor C3 sets all of delay times. When overcurrent detection is released until  $t_{IOV1}$ , the capacitor C3 is charged by S-8232. If all battery voltage is lower than  $V_{DD1,2}$  at that time, charging goes on. So delay time is shorter then typical.

### [ Conclusion ]

This phenomenon occurs when all battery voltage is nearly equal to the overdischarge voltage ( $V_{DD1,2}$ ) after overcurrent detected. It means that the battery capacity is small and those must be charged in the future. Even if the state changes to overdischarge condition, the battery package capacity is same as typical.



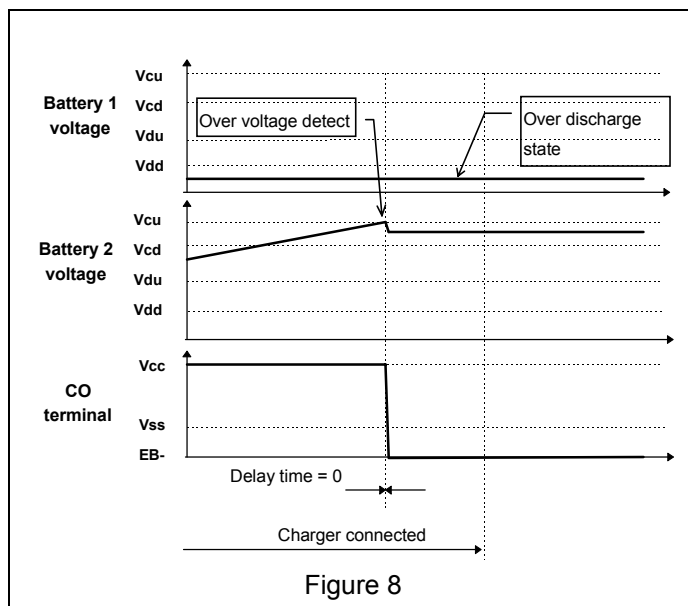
- (2) When one of the battery voltages is overdischarge detection voltage( $V_{DD1,2}$ ) or lower and the other one becomes higher than the overcharge detection voltage( $V_{CU1,2}$ ), the IC detects the overcharge without the overcharge detection delay time( $t_{CU}$ ). (Refer fig.8)

### [ Cause ]

It is same as the overdischarge detection under the overcurrent condition. It occurs because capacitor C3 sets all of delay times.

### [ Conclusion ]

This phenomenon occurs when one battery voltage is lower than overdischarge voltage ( $V_{DD1,2}$ ) and batteries are charged by charger. Under this situation voltage difference between two batteries is unusual. Without delay time is better than long delay time for battery pack safety.(Refer fig.8)



- (3) After the overcurrent detection, the load was connected for a long time, even if one of the battery voltage became lower than overdischarge detection voltage ( $V_{DD1,2}$ ), the IC can't detects the overdischarge as long as the load is connected. Therefor the IC's current consumption at the one of the battery voltage is lower than the overdischarge detection voltage is same as normal condition current consumption ( $I_{OPE}$ ). (Refer fig.9)

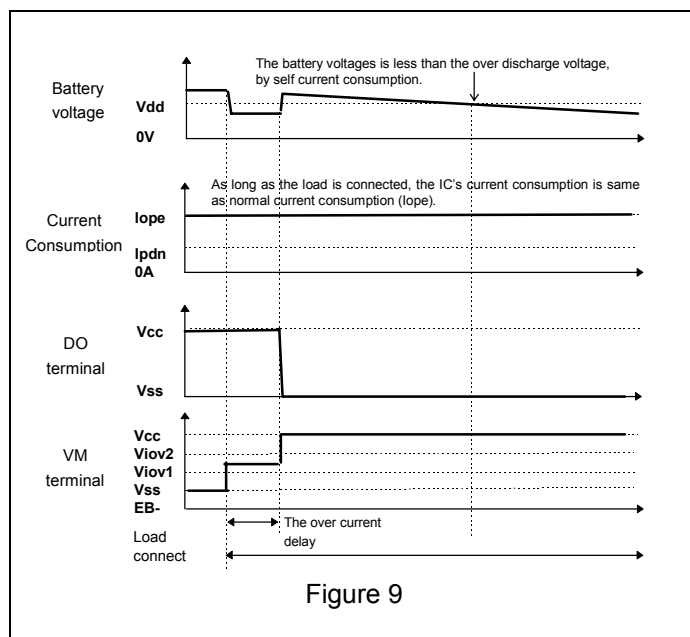


## [ Cause ]

The reason is as follows. If the overcurrent detection and overdischarge detection occur at same time, the overcurrent detection takes precedence the overdischarge detection. As long as the IC detects overcurrent, the IC can't detect overdischarge.

## [ Conclusion ]

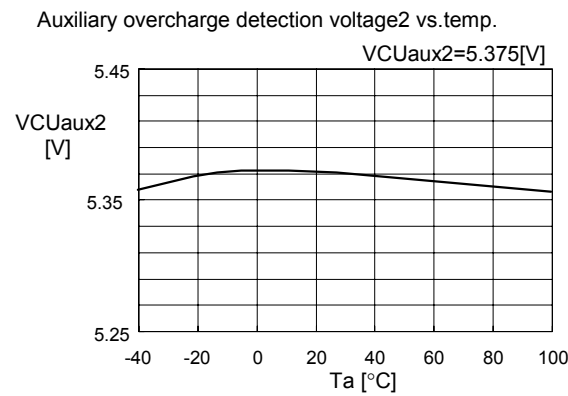
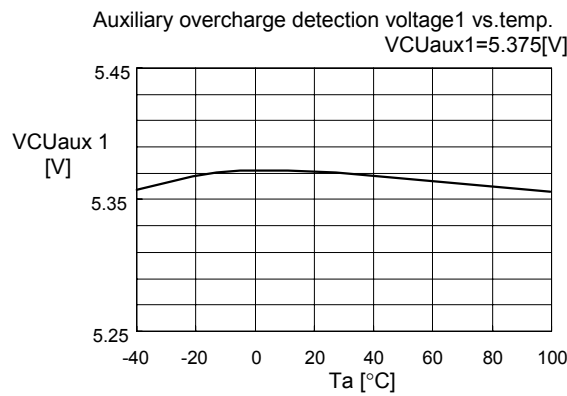
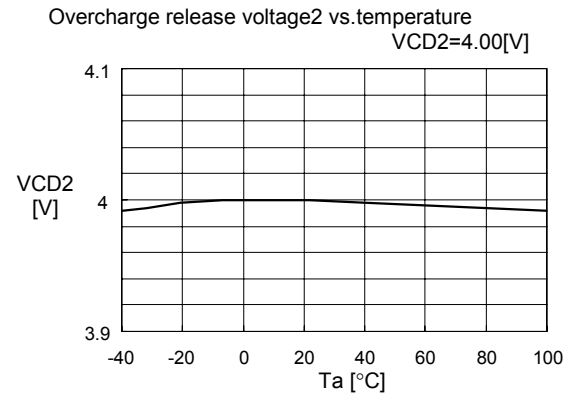
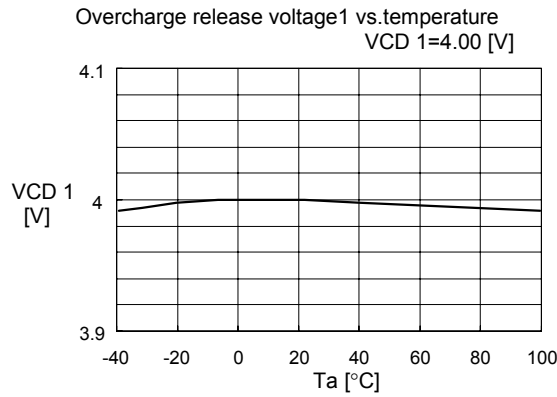
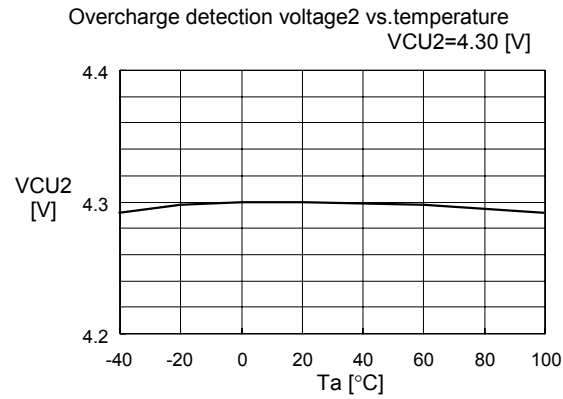
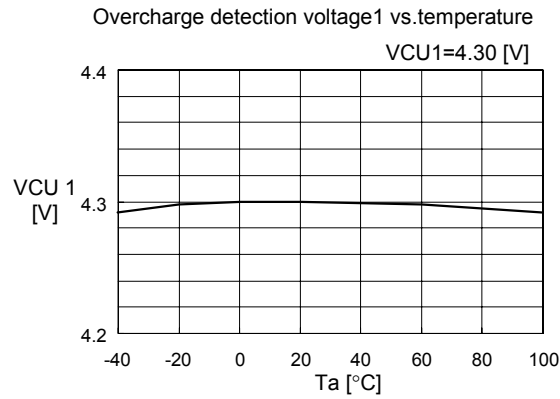
If the load is taken off at least one time, the overcurrent is released and the overdischarge detection works. Unless keeping the IC(S-8232) with load for a long time, the reduction of battery voltage will be neglected, because of the IC's(S-8232) current consumption(typ.  $7.5\ \mu\text{A}$ ) is small.

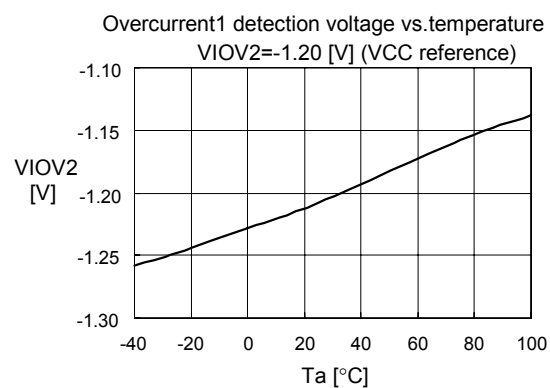
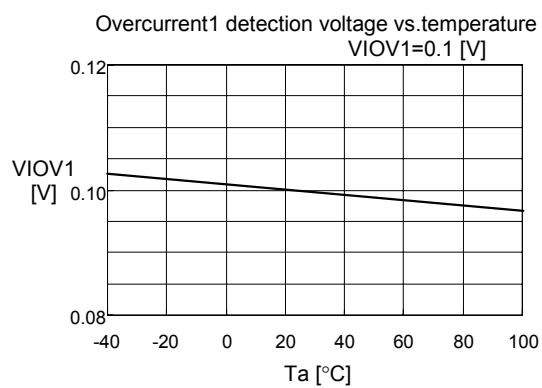
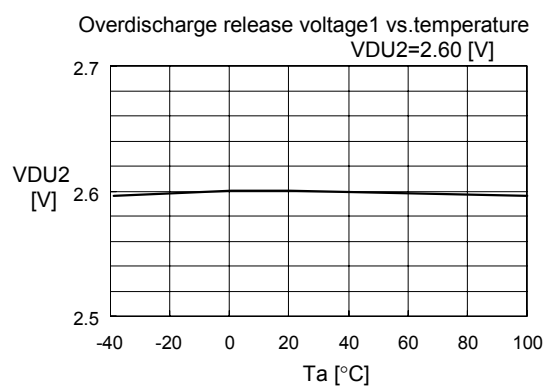
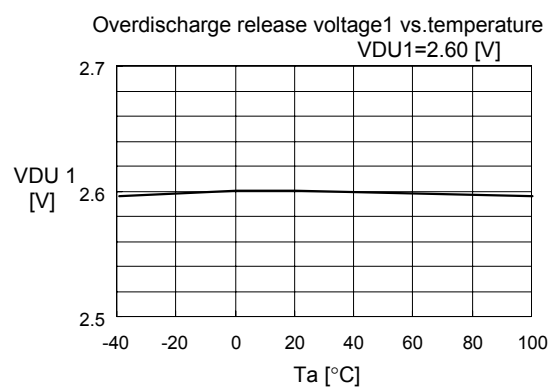
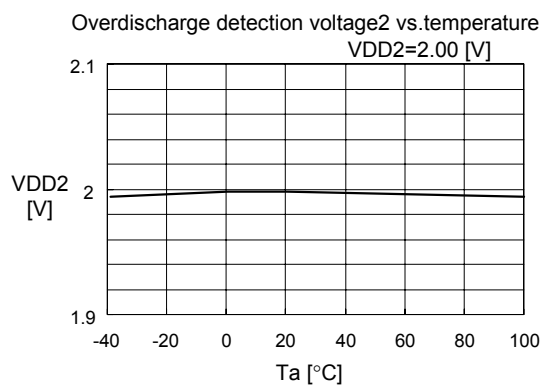
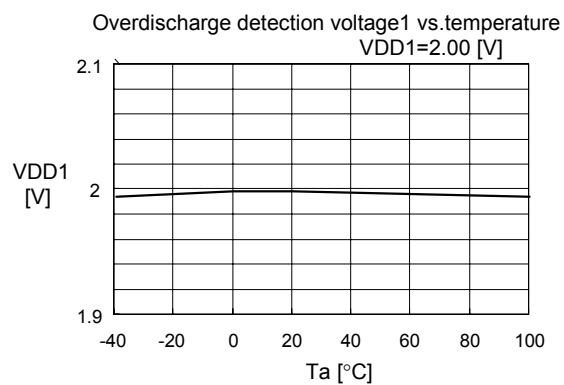


- (4) Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

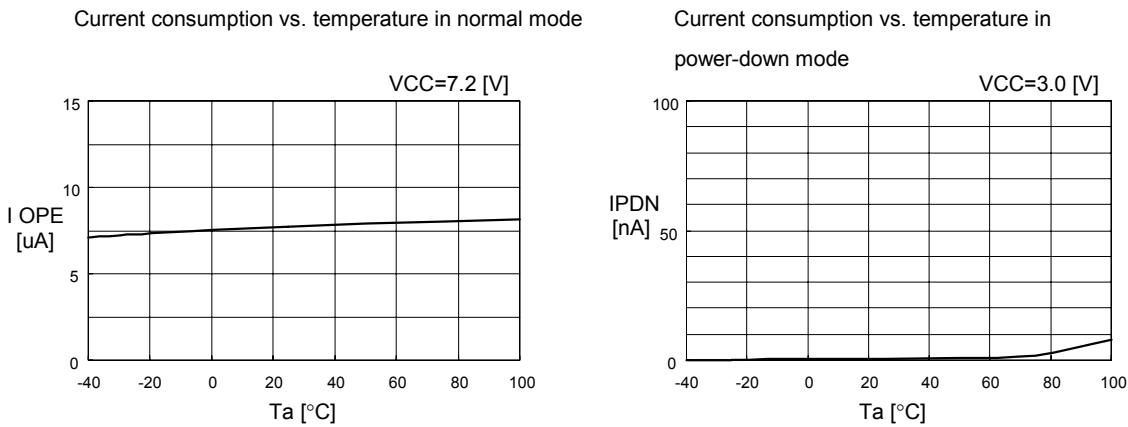
■ Characteristics(typical characteristics)

1. Detection voltage temperature characteristics

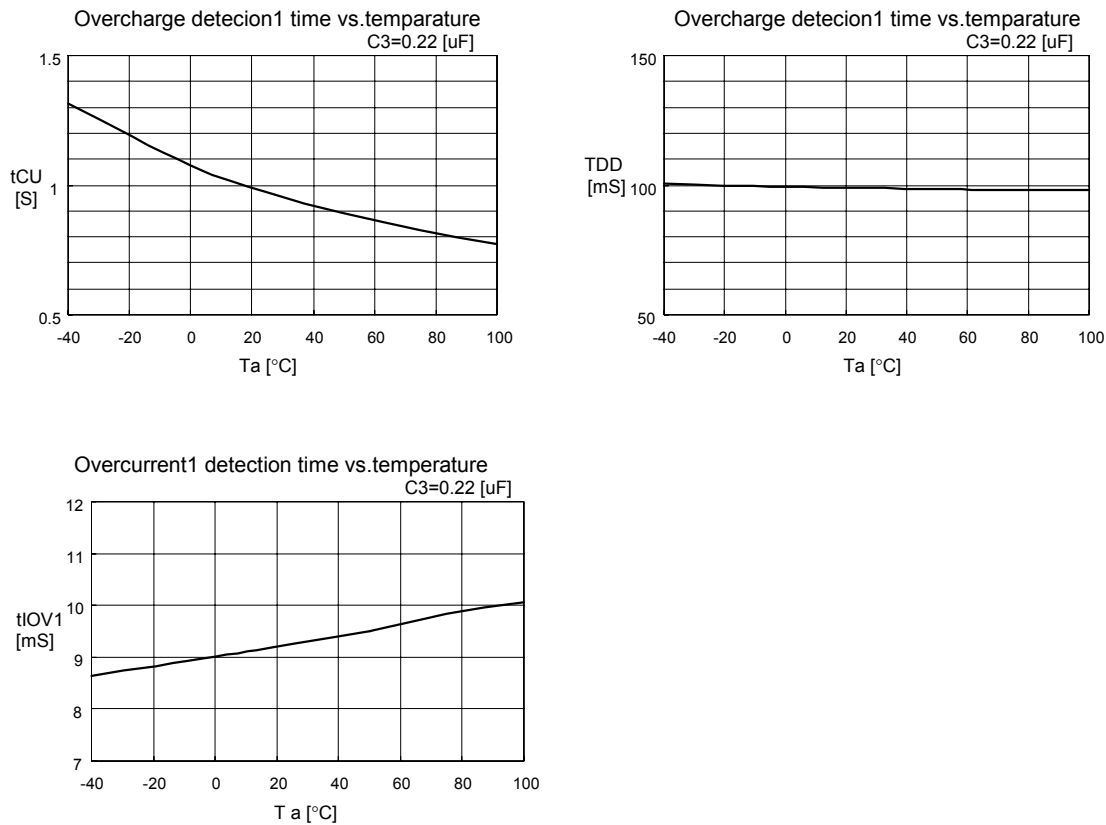




2.Current consumption temperature characteristics

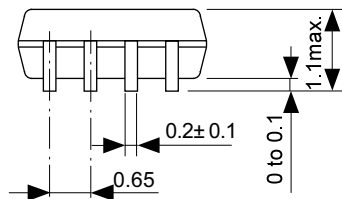
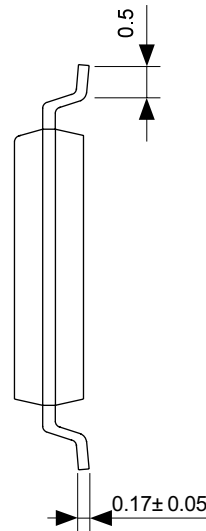
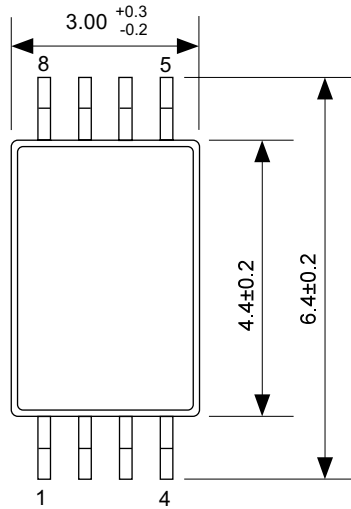


3. Delay time temperature characteristics



●Dimensions

Unit:mm

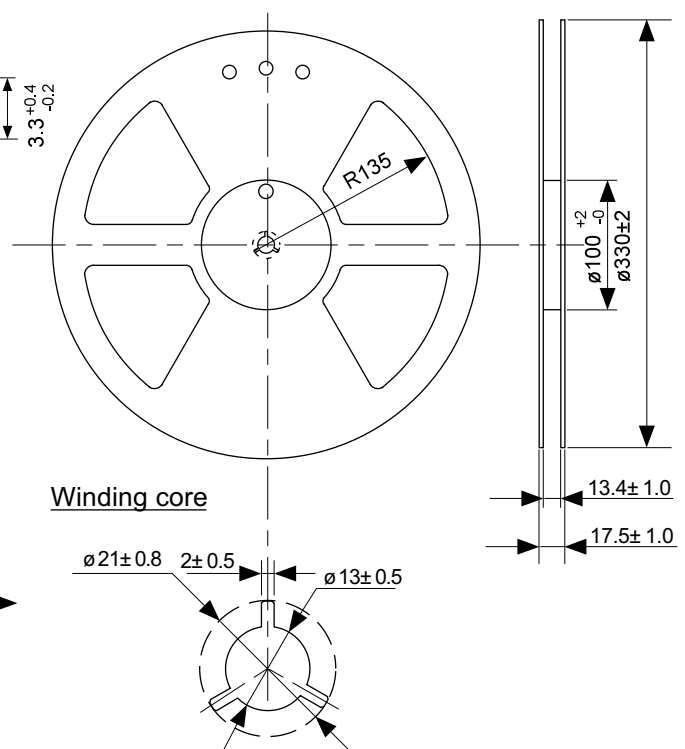
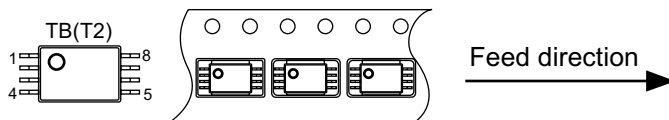
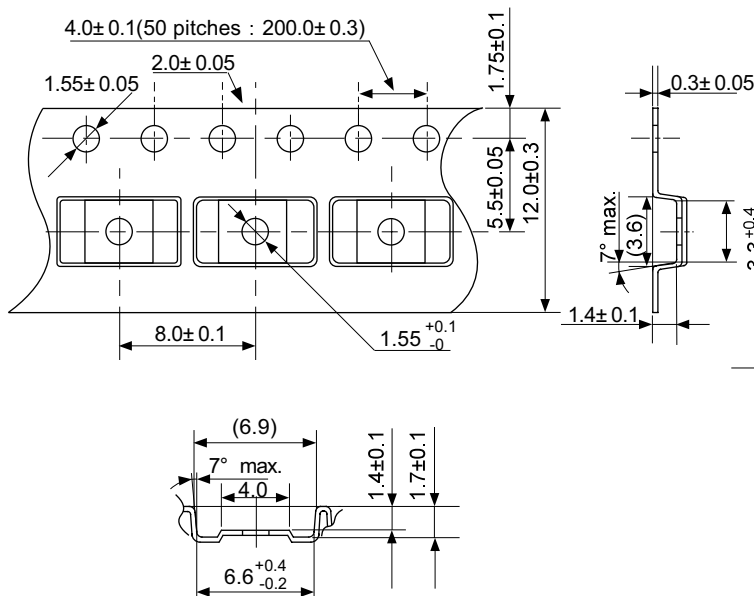


No. : FT008-A-P-SD-1.0

●Taping Specifications

●Reel Specifications

1 reel holds 3000 ICs.



No. : FT008-A-C-SD-3.0

No. : FT008-A-R-SD-3.0

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