

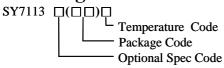
Application Note:SY7113

Low Noise High Efficiency 1MHz, 3A Step Up Regulator with Accurate Output Current Limit Preliminary Specification

General Description

SY7113 develops a current mode control step up regulator with DC current limit. The device integrates a low $R_{DS(0N)}$ switch to minimize the conduction loss. Low output voltage ripple and small external inductor and capacitor size are achieved with 1MHz switching frequency.

Ordering Information



Temperature Range: -40° C to 85° C

Ordering Number	Package type	Note
SY7113ABC	SOT23-6	3 A

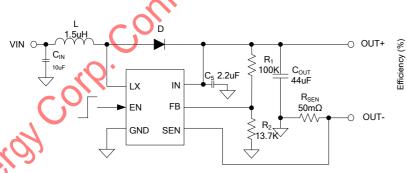
Features

- Input range: 2-6V
- 1MHz switching frequency
- Low $R_{DS(ON)}$ internal switch: 120 m Ω
- Internal softstart limits the inrush current
- Input UVLO
- Over temperature protection
- Minimum on time: 100ns typical
- Minimum off time: 100ns typical
- RoHS Compliant and Halogen Free
- Compact package: SOT23-6

Targeted Applications

- Handheld devices
- Backup Battery
- Notebook
- High Power AP

Typical Application



Efficiency vs. Load Current

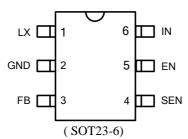
96
92
88
80
76
V_{IN}-4-2V,V_{OUI}-5V
72
1 10 100 1000
Load Current (mA)

Fig. 1 Schematic Diagram

Fig. 2 Efficiency vs Load Current



Pinout (top view)



Top Mark: NM xyz (device code: NM, x=year code, y=week code, z= lot number code)

Pin Name	Pin Number	Pin Description		
LX	1	Inductor node. Connect an inductor from power input to LX pin.		
GND 2 Ground pin				
FB	3 Feedback pin. Connect to the center of resistor voltage divider to program			
		output voltage: V _{OUT} =0.6V*(R1/R2+1)		
SEN	4	Current Sense Pin. Connect current sense resistor Rsen to program the output		
		current limit: I _{LMT} =50mV/Rsen.		
EN	5	Enable control. Pull high to turn on the IC. Do not float.		
IN	6	IC power supply input pin. Decouple this pin to GND pin with 1μF ceramic cap.		

Absolute Maximum Ratings (Note 1)	
IX IN FN	
FB, SEN	
Power Dissipation, PD @ TA = 25°C SOT23-6,	0.6W
Package Thermal Resistance (Note 2)	
θ JA	
θ JC	130°C/W
Junction Temperature Range	
Lead Temperature (Soldering, 10 sec.)	
Storage Temperature Range	
Recommended Operating Conditions (Note 3)	
LX, IN, EN	2V to 6V
FB, SEN	
Junction Temperature Range	
Ambient Temperature Range	



Electrical Characteristics

 $(V_{IN} = 3.3V, V_{OUT} = 5V, I_{OUT} = 100mA, TA = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Input Voltage Range	V_{IN}		2		6	V
Quiescent Current	I_Q	FB=0.66V		120		μA
Low Side Main FET RON	R _{DS(ON)}			120		mΩ
Main FET Current Limit	I_{LIM}		3	\circ		A
Switching Frequency	F_{SW}			1		MHz
Feedback Reference Voltage	V_{REF}		0.588	0.6	0.612	V
Current Sense Limit	V_{SEN}	$V_{FB}=600 \text{mV}$		50		mV
		V_{FB} <600mV	,	50+0.2*(600		mV
			$-\mathbf{C}$	$-1000*V_{FB}$)		
IN UVLO rising threshold	$V_{IN,UVLO}$. 0		1.9	V
UVLO hysteresis	V_{HYS}			0.1		V
Minimum On Time	T _{ON_MIN}	& C) •	100		nS
Minimum Off Time	T _{OFF_MIN}	7		100		nS
Thermal Shutdown	T_{SD}	00		150		°C
Temperature		(0)				

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

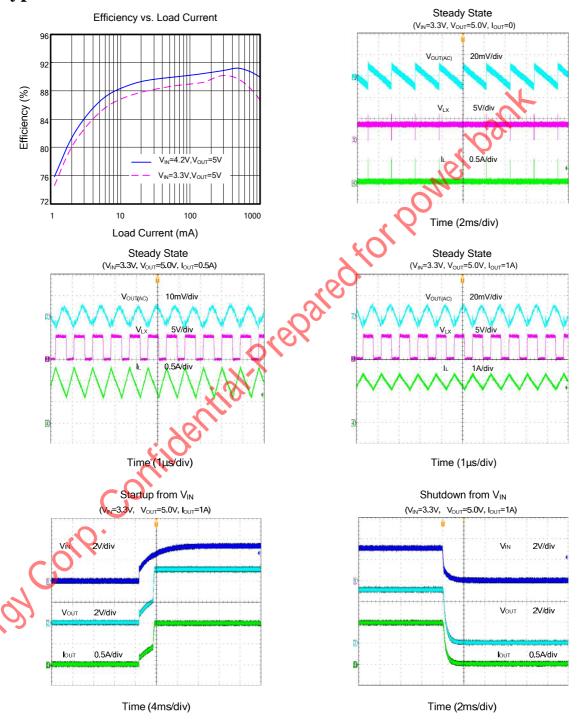
Note 2: θ JA is measured in the natural convection at TA = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of DFN3x3-10 packages is the case position for θ JC measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

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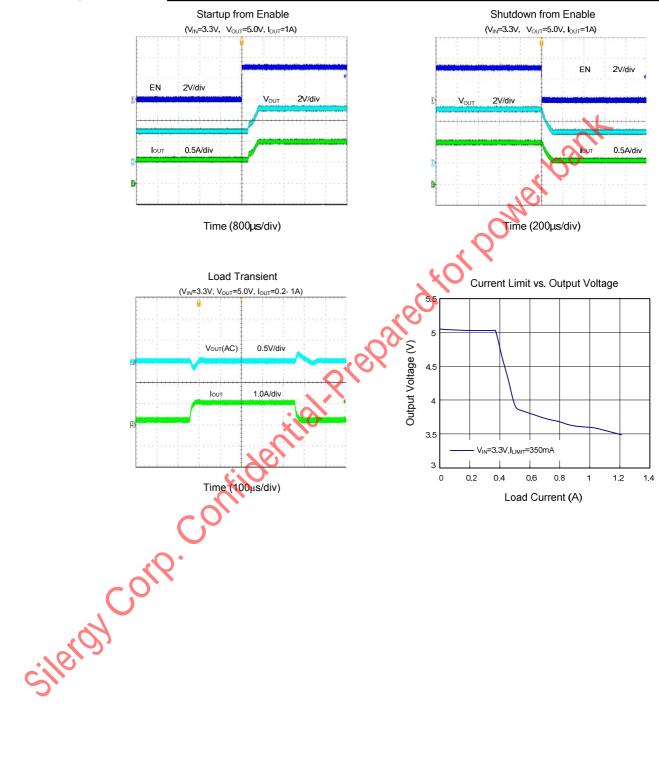


Typical Performance Characteristics











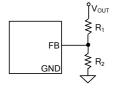
Applications Information

Because of the high integration in SY7113, the application circuit based on this regulator IC is rather simple. Only input capacitor $C_{\rm IN}$, output capacitor $C_{\rm OUT}$, inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications.

Feedback resistor divider R1 and R2

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_1 and R_2 . A value between 10k and 1M is recommended for both resistors. If R_1 =200k is chosen, then R_2 can be calculated to be:

$$R_2 = \frac{0.6R_1}{V_{\text{OUT}} - 0.6}(\Omega)$$



Input capacitor CIN

The ripple current through input capacitor is calculated as:

$$I_{\text{CIN_RMS}} = \frac{V_{\text{IN}} \cdot (V_{\text{OUT}} - V_{\text{IN}})}{2\sqrt{3} \cdot L \cdot F_{\text{SW}} \cdot V_{\text{OUT}}} (A)$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the VDD and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and VDD/GND pins. In this case a 10uF low ESR ceramic capacitor is recommended.

Output capacitor Cour

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into account when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 10V rating and more than two 22uF capacitors.

Boost inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \left(\frac{V_{\text{IN}}}{V_{\text{OUT}}}\right)^2 \frac{(V_{\text{OUT}} - V_{\text{IN}})}{F_{\text{SW}} \times I_{\text{OUT_MAX}} \times 40\%} (H)$$

where F_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

SY7113 regulator IC is less sensitive to the ripple current variations. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

 The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.

$$I_{SAT_MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT_MAX} + \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10m Ω to achieve a good overall efficiency.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During the shut down mode, the SY7113 shut down current drops to lower than 10µA. Driving the EN pin high (>1.5V) will turn on the IC again.

Rectifier Diode Selection

Schottky diode is a good choice for high efficiency operation because of its low forward voltage drop and fast reverse recovery. The maximum current rating of the diode must be higher than maximum input current. And the average current rating of the diode must be higher than the output current.

Output Current Limit

The output current limit level is programmed by the resistor $R_{\text{SEN}}(\text{show as figure 1})$:

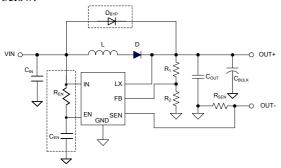
$$I_{O_Limit} = 50 \text{mV/R}_{SEN}$$





Applications with Large Bulk Capacitance

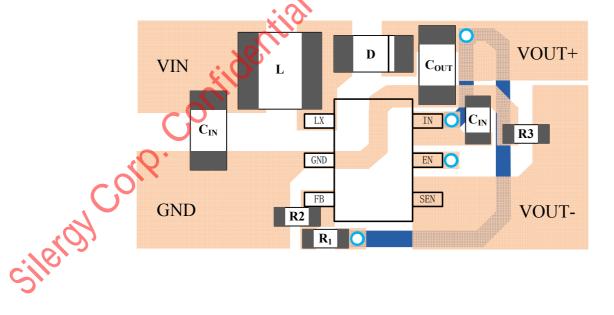
In applications with large bulk capacitance on the output, a very high inrush current can be seen flow through the inductor during power on. To avoid this inrush current flow into the IC and cause any unexpected damage, a Zener diode connected from power input to the output or an RC delay circuit added on EN pin of the IC can be used. Refer to the circuit below.



Layout Design

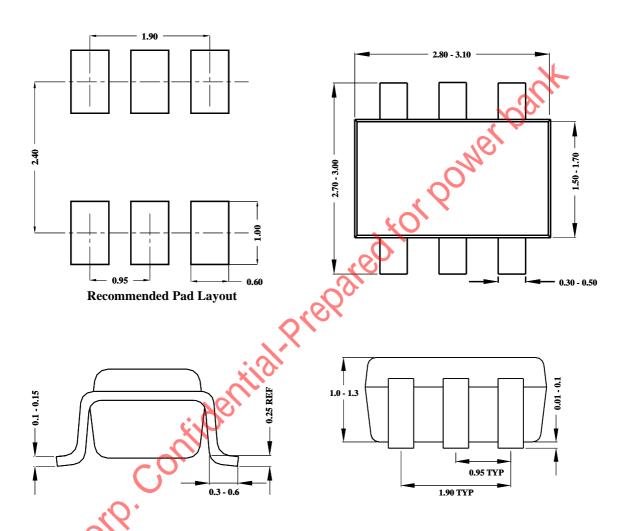
The layout design of SY7113 regulator is highly simplified. To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: $C_{\rm IN}$, L, R_1 and R_2 .

- 1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve a better thermal performance and noise immunity. If the board space allowed, a designated ground plane layer is highly recommended.
- 2) $C_{\rm IN}$ must be close to VDD and GND pins. The loop area formed by $C_{\rm OUT}$, LX and GND pins must be minimized.
- 3) The PCB copper area associated with LX pin must be minimized to improve the noise immunity.
- 4) The components R_1 and R_2 , and the trace connecting to the FB pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to FB pin.
- 5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the VDD pin is connected directly to a power source such as a Li-lon battery, it is desirable to add a pull down $1M\Omega$ resistor across the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.





SOT23-6 Package outline & PCB layout design



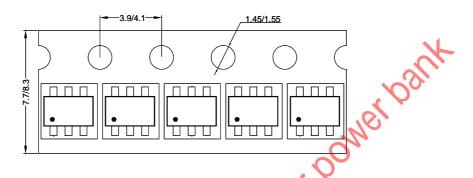
Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.



Taping & Reel Specification

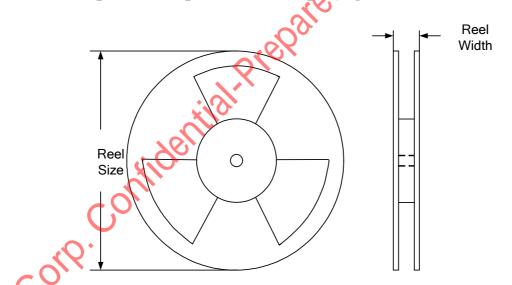
1. Taping orientation

SOT23-6



Feeding direction

2. Carrier Tape & Reel specification for packages



-	Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
2	SOT23-6	8	4	7''	8.4	280	160	3000

3. Others: NA