SAMSUNG ELECTRONICS

KS57C2408/2416
4-Bit CMOS Microcontroller

Data Sheet

DESCRIPTION

The KS57C2408/2416 single-chip 4-bit microcontroller is fabricated using an advanced CMOS process. With an up-to-12-digit LCD direct-drive capability, 8-bit x 6-channel A/D converter, and versatile 8-bit and 16-bit timer/counters, the KS57C2408/2416 offers an excellent design solution for a wide range of LCD related applications.

FEATURES

Memory

- 512 × 4-bit RAM
- 8192 × 8-bit ROM (KS57C2408),
  16,384 x 8-bit ROM (KS57C2416)

Oscillation Sources

- Crystal, ceramic, RC (main)
- Crystal for subsystem clock
- Main system clock frequency: 4.19 MHz (typical)
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider (4, 8, 64)

Two Power-Down Modes

- Idle (only CPU clock stops)
- Stop (system clock stops)

Interrupts

- Five internal vectored interrupts
- Three external vectored interrupts
- Two quasi-interrupts

50 I/O Pins

- 10 input pins
- 12 output pins
- 20 configurable I/O pins
- Eight n-channel open-drain pins

8-Bit Basic Timer

- Four interval timer functions

8-Bit Timer/Counter

- Programmable 8-bit timer
- External event counter
- Arbitrary clock output
- External clock signal divider
- Serial I/O clock generator

16-Bit Timer/Counter

- Programmable 16-bit timer
- External event counter
- Arbitrary clock output
- External clock signal divider

Watch Timer

- Four frequency outputs for buzzer sound

LCD Controller/Driver

- Maximum 12-digit LCD direct-drive capability
- Display modes: static, 1/2 duty (1/2 bias), 1/3 duty (1/2 or 1/3 bias), 1/4 duty (1/3 bias)

A/D Converter

- Six analog input channels
- 19.09-µs conversion speed at 4.19 MHz
- 8-bit conversion resolution

8-Bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable
- Internal/external clock source

Instruction Execution Times

- 0.95 µs, 1.91 µs, 15.3 µs at 4.19 MHz (main)
- 122 µs at 32.768 kHz (subsystem)

Operating Temperature Range

- – 40 °C to 85 °C

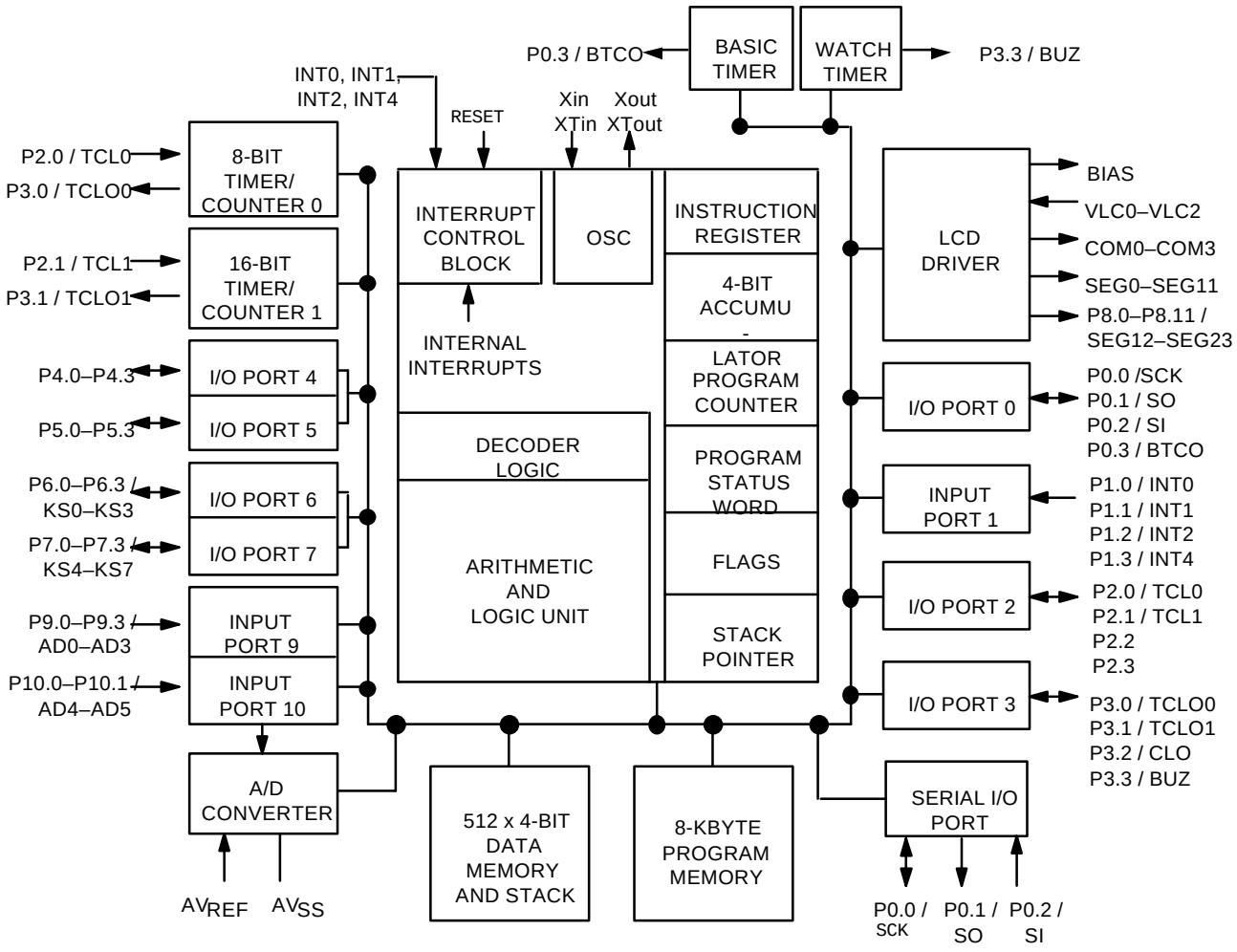
Operating Voltage Range

- 2.7 V to 6.0 V

Package Type

- 80-pin QFP

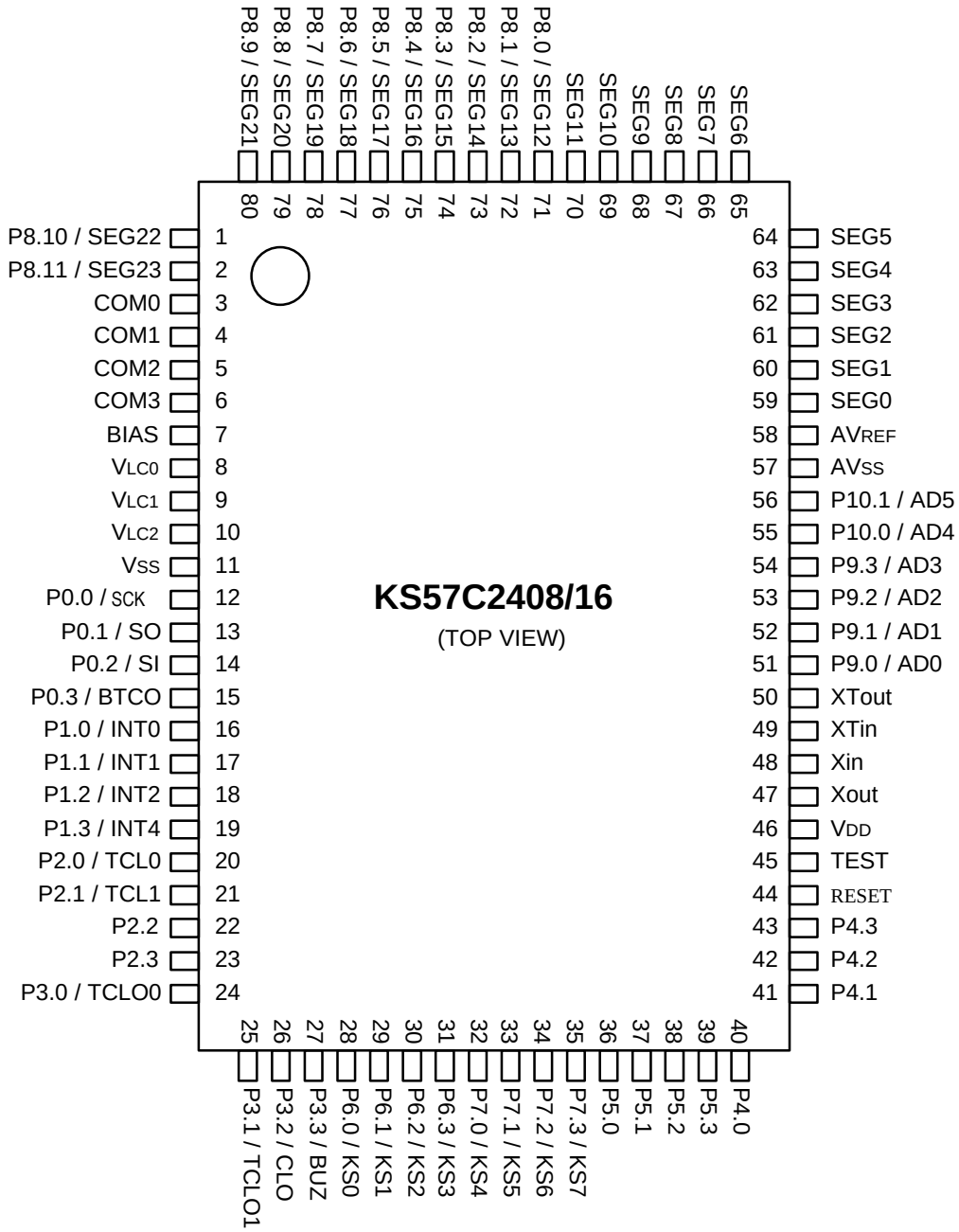
BLOCK DIAGRAM



NOTE: The KS57C2416 has a 16-Kbyte program memory.

SAMSUNG ELECTRONICS

PIN ASSIGNMENTS



PIN DESCRIPTIONS

Pin Names	Pin Type	Description	Number (80-QFP)	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is supported. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable	12 13 14 15	SCK SO SI BTCO
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test is supported. 3-bit pull-up resistors are software assignable to pins P1.0, P1.1, and P1.2 only.	16 17 18 19	INT0 INT1 INT2 INT4
P2.0 P2.1 P2.2 P2.3	I/O	Same as port 0.	20 21 22 23	TCL0 TCL1
P3.0 P3.1 P3.2 P3.3	I/O	Same as port 0.	24 25 26 27	TCLO0 TCLO1 CLO BUZ
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O ports. Configurable as n-channel open-drain pins for up to 9-volt loads. 1-bit, 4-bit, and 8-bit read/write and test is supported. Ports 4 and 5 can be paired to support 8-bit data transfer. Pull-up resistors are assignable to individual pins by mask option.	40–43 36–39	– –
P6.0–P6.3 P7.0–P7.3	I/O	4-bit I/O ports. Port 6 pins are individually software configurable as input or output; 1-bit, 4-bit read/write and test is supported. 4-bit pull-up resistors are software assignable. Ports 6 and 7 can be paired to enable 8-bit data transfer.	28–31 32–35	KS0–KS3 KS4–KS7
P8.0–P8.11	O	Output port for 1-bit data (as CMOS driver only)	71–80, 1–2	SEG12– SEG23
P9.0–P9.3 P10.0–P10.1	I	Input ports for 1-bit or 4-bit data. 1-bit and 4-bit read and test is supported.	51–56	AD0–AD3 AD4–AD5
CLO	I/O	CPU clock output	26	P3.2
BUZ	I/O	2-, 4-, 8-, or 16-kHz frequency output for buzzer sound (4.19-MHz main clock or 32.768-kHz subsystem clock)	27	P3.3
X_{IN}, X_{OUT}	—	Crystal, ceramic, or RC oscillator signal for main system clock (For external clock input, use X_{IN} and input X_{IN}'s reverse phase to X_{OUT}.)	48, 47	–
XT_{IN}, XT_{OUT}	—	Crystal oscillator signal for subsystem clock (For external clock input, use XT_{IN} and input XT_{IN}'s reverse phase to XT_{OUT}.)	49, 50	–

PIN DESCRIPTIONS (Continued)

Pin Names	Pin Type	Description	Number (80-QFP)	Share Pin
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable. Only INT0 is synchronized with the system clock.	16–17	P1.0, P1.1
INT2	I	Quasi-interrupt with detection of rising signal edges	18	P1.2
INT4	I	External interrupt with detection of rising or falling signal edges	19	P1.3
KS0–KS7	I/O	Quasi-interrupt input with falling edge detection	28–35	P6.0–P7.3
TCL0	I/O	External clock input for timer/counter 0	20	P2.0
TCL1	I/O	External clock input for timer/counter 1	21	P2.1
TCLO0	I/O	Timer/counter 0 clock output	24	P3.0
TCLO1	I/O	Timer/counter 1 clock output	25	P3.1
COM0–COM3	O	LCD common signal output	3–6	–
SEG0–SEG11	O	LCD segment output	59–70	–
SEG12–SEG23	O	1-bit LCD segment data output	71–80, 1–2	P8.0–P8.11
BIAS	—	LCD power control	7	–
V_{LC0}–V_{LC2}	—	LCD power supply; voltage dividing resistors are assignable by mask option	8–10	–
AD0–AD5	I	A/D converter analog input channels	51–56	P9.0–P9.3 P10.0–P10.1
AV_{SS}	—	A/D converter ground	57	–
AV_{REF}	—	A/D converter analog reference voltage	58	–
SCK	I/O	Serial I/O interface clock signal	12	P0.0
SO	I/O	Serial data output	13	P0.1
SI	I/O	Serial data input	14	P0.2
BTCO	I/O	Basic interval timer clock output	15	P0.3
RESET	I	RESET signal	44	–
V_{DD}	—	Main power supply	46	–
V_{SS}	—	Ground	11	–
TEST	—	Test signal input (must be connected to V_{SS})	45	–

NOTE: Pull-up resistors for ports 0, 2, 3, 6, and 7 are automatically disabled if they are configured to output mode.

FUNCTION OVERVIEW

SAM4 CPU

All KS57-series microcontrollers have the advanced SAM4 CPU core. The SAM4 CPU can directly address up to 32 K bytes of program memory.

The arithmetic logic unit (ALU) performs 4-bit addition, subtraction, logical, and shift-and-rotate operations in one instruction cycle. Most 8-bit arithmetic and logical operations execute in two cycles.

CPU REGISTERS

Program Counter

For the KS57C2408, a 13-bit program counter (PC) stores addresses for instruction fetch during program execution. The KS57C2416 has a 14-bit PC. Usually, the PC is incremented by the number of bytes of the instruction being fetched. An exception is the 1-byte instruction REF, which is used to reference instructions stored in a look-up table in the ROM.

Stack Pointer

An 8-bit stack pointer (SP) stores addresses for stack operations. The stack area is located in the general-purpose data memory bank 0. The SP is read or written by 8-bit instructions. SP.0 must always be logic zero.

PROGRAM MEMORY

In its standard configuration, the ROM is divided into four functional areas:

— 16-byte area for vector addresses

— 96-byte instruction reference area

— 16-byte and 8,064-byte areas for general-purpose program memory(KS57C2408)

— 16-byte and 16,256-byte areas for general–purpose program memory (KS57C2416)

The REF instruction references 2 × 1-byte and 2-byte instructions stored in locations 0020H–007FH. The REF instruction can also reference three-byte instructions such as JP or CALL.

So that a REF instrcution can reference these instructions, JP or CALL must be shortened to a 2-byte format. To do this, JP or CALL is written to the reference area with the format TJP or TCALL instead of the normal instruction name.

DATA MEMORY

Overview

Data memory is organized into five areas:

— 32 × 4-bit working register area

— 224 × 4-bit general-purpose area in bank 0

— 232 × 4-bit general-purpose area in bank 1.

— 24 × 4-bit area for LCD data.

— 128 × 4-bit area in bank 15 for memory-mapped I/O addresses

Data Memory Addressing Modes

The enable memory bank (EMB) flag controls the addressing mode for data memory banks 0, 1, or 15. .

When the EMB flag is logic zero, restricted area can be accessed. When the EMB flag is set to logic one, any of the three data memory banks can be accessed according to the current SMB value.

LCD Data Register Area Bit values for LCD segment data are stored in data memory bank 1. Register locatins not used to store LCD data can be assigned to general–purpose use.

CONTROL REGISTERS

Select Bank (SB) Register

Two 4-bit registers store address values used to access specific memory and register banks: the select memory bank register, SMB, and the select register bank register, SRB.

The 'SMB n' instruction selects a data memory bank (0, 1, or 15) and stores the upper four bits of the 12-bit data memory address in the SMB register. To select register bank 0, 1, 2, or 3, and store the address data in the SRB, you use the instruction 'SRB n'.

The instructions "PUSH SB" and "POP SB" move SRB and SMB values to and from the stack for interrupts and subroutines.

INTERRUPTS

Interrupt requests can be generated internally by on-chip processes (INTB, INTT0, INTT1, INTAD, and INTS) or externally by peripheral devices (INT0, INT1, and INT4). There are two quasi-interrupts: INT2 and INTW. The following components support interrupt processing:

— Interrupt enable flags
— Interrupt request flags
— Interrupt priority registers
— Power-down release circuit

POWER-DOWN

To reduce power consumption, there are two power-down modes: Idle and Stop. The IDLE instruction initiates Idle mode; the STOP instruction initiates Stop mode.

In Idle mode, the CPU clock stops while peripherals continue to operate normally. In Stop mode, system clock oscillation stops, halting all operations except for a few basic peripheral functions. A power-down can be released by a RESET or by an interrupt.

RESET

When RESET is input during normal operation or a power-down mode, a RESET operation starts and the CPU enters Idle mode. When the oscillation stabilization time interval (31.3 ms at 4.19 MHz) has elapsed, normal CPU operation resumes.

LCD DRIVER/CONTROLLER

The KS57C2408/2416 can directly drive an up-to-12-digit (96-segment) LCD panel. The LCD function block has the following component:

— RAM area for storing display data
— 24 segment output pins (SEG0–SEG23)
— Four common output pins (COM0–COM3)
— Three operating power supply pins (V_{LC0}–V_{LC2})
— BIAS pin for the driver and bias voltage

Frame frequency, LCD clock, duty and bias, and segment pins used for display output are controlled by bit settings in the 8-bit mode reigster, LMOD.

The 4-bit LCD control register, LCON, is used to turn the LCD display on and off, and to control current supplied to the dividing resistors.

TIMERS and TIMER/COUNTERS

The timer function block has four main components: an 8-bit basic timer, an 8-bit timer/counter, a 16-bit timer/counter, and a watch timer.

The 8-bit basic timer generates interrupt requests at precise intervals, based on the selected internal clock frequency.

The 8-bit and 16-bit timer/counters are used for counting events, modifying internal clock frequencies, and dividing external clock signals. The 8-bit timer/counter can generate a clock signal (SCK) for the serial I/O interface.

The watch timer consists of an 8-bit watch timer mode register, and a frequency divider circuit. Its functions include real-time and watch-time measurement, and clock generation for buzzer frequency output.

SERIAL I/O INTERFACE

The serial I/O interface supports the transmission or reception of 8-bit serial data with an external device. The serial interface has the following functional components:

— 8-bit mode register
— Clock selector circuit
— 8-bit buffer register
— 3-bit serial clock counter

D.C. ELECTRICAL CHARACTERISTICS

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	All input pins except as specified for V_{IH2}–V_{IH4}	0.7 V_{DD}	–	V_{DD}	V
	V_{IH2}	Ports 0–2, 6, 7, 9, 10, and RESET	0.8 V_{DD}		V_{DD}	
	V_{IH3}	Ports 4 and 5 with pull-ups assigned	0.7 V_{DD}		V_{DD}	
		Ports 4 and 5 open-drain	0.7 V_{DD}		9	
	V_{IH4}	X_{IN}, X_{OUT}, and XT_{IN}	V_{DD} – 0.5		V_{DD}	
Input Low Voltage	V_{IL1}	Ports 3–5	–	–	0.3 V_{DD}	V
	V_{IL2}	Ports 0–2, 6, 7, 9, 10, and RESET			0.2 V_{DD}	
	V_{IL3}	X_{IN}, X_{OUT}, and XT_{IN}			0.4	
Output High Voltage	V_{OH1}	V_{DD} = 4.5 V to 6.0 V I_{OH} = – 1 mA Ports 0, 2, 3, 6, 7, and BIAS	V_{DD} – 1.0	–	–	V
		I_{OH} = – 100 µA	V_{DD} – 0.5			
	V_{OH2}	V_{DD} = 4.5 V to 6.0 V I_{OH} = – 100 µA; port 8 only	V_{DD} – 2.0			
		I_{OH} = – 30 µA	V_{DD} – 1.0			
Output Low Voltage	V_{OL1}	V_{DD} = 4.5 V to 6.0 V I_{OL} = 15 mA, ports 4 and 5 only	–	0.4	2	V
		I_{OL} = 1.6 mA Ports 0, 2, 3, 6, and 7 only		–	0.4	
		I_{OL} = 400 µA Ports 0, 2, 3, 6, and 7 only			0.2	
	V_{OL2}	V_{DD} = 4.5 V to 6.0 V I_{OL} = 100 µA; port 8 only			1	
		I_{OL} = 50 µA			1	
Input High Leakage Current	I_{LIH1}	V_{IN} = V_{DD} All input pins except ports 4 and 5, X_{IN}, X_{OUT}, and XT_{IN}	–	–	3	µA
	I_{LIH2}	V_{IN} = V_{DD} X_{IN}, X_{OUT}, and XT_{IN}			20	
	I_{LIH3}	V_{IN} = 9 V Ports 4 and 5 are open-drain			20	
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0 V; All input pins except X_{IN}, X_{OUT}, XT_{IN}, and RESET	–	–	– 3	µA

	I_{LIL2}	V_{IN} = 0 V; X_{IN}, X_{OUT}, and XT_{IN}			– 20	

D.C. ELECTRICAL CHARACTERISTICS (Continued)

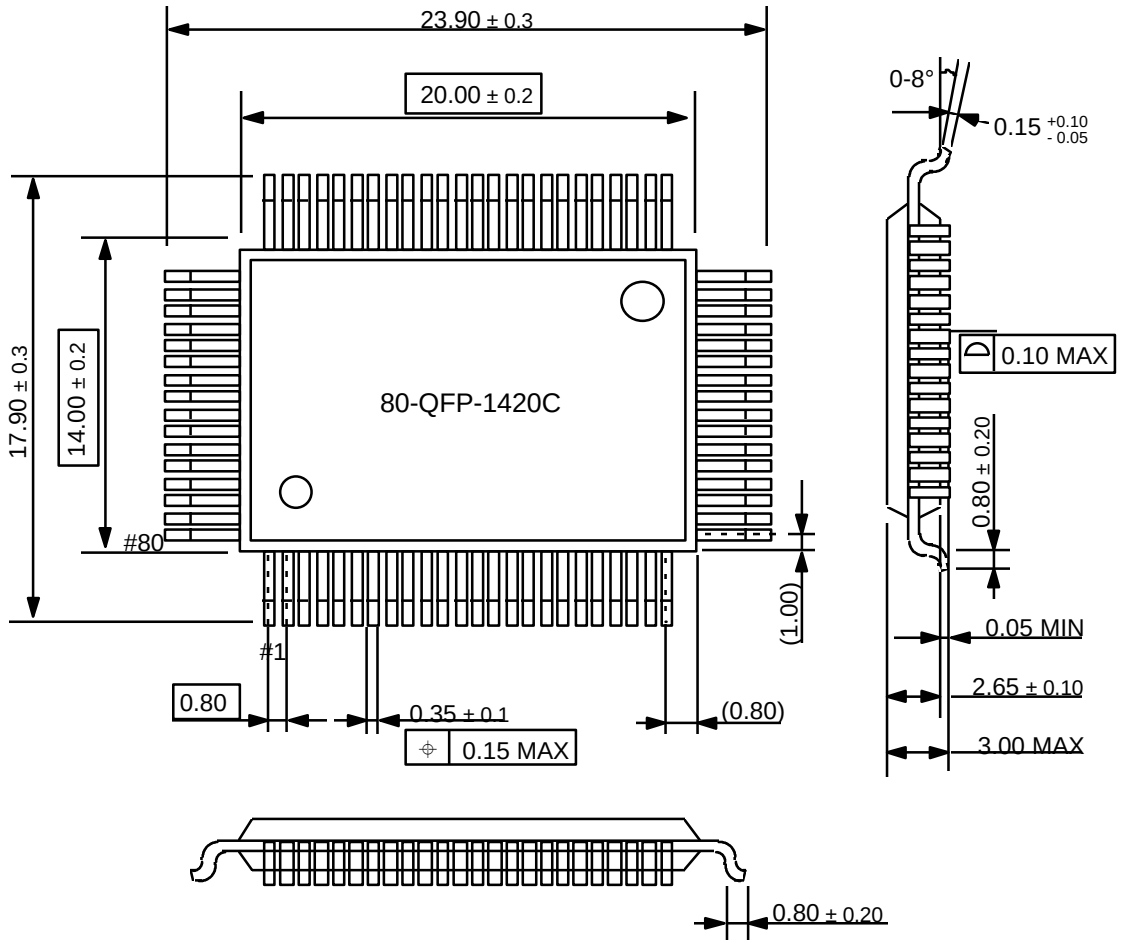
(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output High Leakage Current	I_{LOH1}	$V_{OUT} = V_{DD}$ All output pins except for ports 4 and 5	–	–	3	µA
	I_{LOH2}	Ports 4 and 5 are open-drain; V_{OUT} = 9 V			20	
Output Low Leakage Current	I_{LOL}	V_{OUT} = 0 V			– 3	
Pull-up Resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 5 V ± 10 % Ports 0, 1 (not P1.3), 2, 3, 6, and 7	15	40	80	K½
		V_{DD} = 3 V ± 10 %	30	–	200	
	R_{L2}	$V_{OUT} = V_{DD}$ – 2 V; V_{DD} = 5 V ± 10 % Ports 4 and 5 only	15	40	70	
		V_{DD} = 3 V ± 10 %	10	–	60	
	R_{L3}	V_{IN} = 0 V; V_{DD} = 5 V ± 10 %; RESET	100	230	400	
		V_{DD} = 3 V ± 10 %	200	490	800	
LCD Voltage Dividing Resistor	R_{LCD}		50	100	140	K½
COM Output Impedance	R_{COM}	V_{DD} = 5 V ± 10 %	–	3	6	K½
		V_{DD} = 3 V ± 10 %		10	15	
SEG Output Impedance	R_{SEG}	V_{DD} = 5 V ± 10 %	–	3	20	K½
		V_{DD} = 3 V ± 10 %		10	60	
Supply Current(1)	I_{DD1} (2)	V_{DD} = 5 V ± 10 % (3); C1 = C2 = 22 pF 4.19-MHz crystal oscillator; normal mode	–	2.5	8	mA
		V_{DD} = 3 V ± 10 % (3)		0.62	1.2	
	I_{DD2} (2)	V_{DD} = 5 V ± 10 %; C1 = C2 = 22 pF 4.19-MHz crystal oscillator; Idle mode	–	1.2	1.8	
		V_{DD} = 3 V ± 10 %		0.58	1.0	
	I_{DD3} (4)	V_{DD} = 3 V ± 10 %; 32-kHz crystal oscillator		30	90	µA
	I_{DD4} (4)	Idle mode; V_{DD} = 3 V ± 10 % 32-kHz crystal oscillator		5	15	
	I_{DD5}	Stop mode; XT_{in} = 0 V; V_{DD} = 5 V ± 10 %		0.5	5	
		V_{DD} = 3 V ± 10 %		0.1	3	

NOTES:
1. Supply Current (I_{DD1} to I_{DD5}) does not include current drawn through internal pull-ups or LCD voltage dividing resistors.
2. Data includes power consumption for subsystem clock oscillation.

3. For high-speed controller operation, set PCON to 0011B; for low-speed operation, set it to 0000B.
4. When SCMOD is 1001B, main system clock oscillation stops and the subsystem clock is used.

PACKAGE DIMENSIONS



NOTE: Dimensions are in millimeters.

SAMSUNG ELECTRONICS