# Miscellaneous Design Issues

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- **Vcc regulator issues**
  - **Voltage follower design uses NFET (2N7002, BSS138, etc.). Vcc = Vref - Vgs(off) and will vary widely with component tolerance and temperature. Does NOT provide precision regulation of Vcc.**
    - **REF pin performs like a low-current zener**
    - **Vref = 6.0uV +/- 0.3V @ 5uA and 25C**
      - TC = -12mV/ºC
      - Rz = 140k
    - **Bias resistor and NFET must be chosen to insure Vcc remains in operational range over battery voltage and temperature extremes**
    - **Typical performance will have up to 0.5V drop in Vcc at 60C and 0.2V increase at 1C**
      - Product testing at 25C should guard band test Vcc to 3.5V at minimum battery voltage to insure meeting 3.0V minimum Vcc at 60C.
      - Product testing at 25C should guard band test Vcc to 6.3V at maximum battery voltage (when charging) to insure meeting 6.5V maximum Vcc at 0C
    - **Most designs should avoid external capacitor on REF pin**

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- Vcc regulator issues (cont'd)
  - Voltage regulator design uses N-channel JFET (SST113, etc.) Vcc is precision regulated by gauge and essentially independent of external component parameters
    - Vgs(off) must be less than Vcc at lowest possible current drain (sleep)
    - 0.001ufd cap on REG is recommended value
- Vout (EEPROM power) issues
  - Vout function only applies power to EEPROM when required
    - Reduced power drain during normal operation
  - No capacitor is recommended on Vout
    - Capacitor will rob charge from Vcc when Vout is switched on and could cause unintended device reset when Vout is powered
    - Current draw of EEPROM may pull Vcc back into POR during power up of gauge. Immediate loss of Vout to EEPROM forces reset of EEPROM communications

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- RBI issues
  - Must have series diode from first cell tap of Lithium battery
    - If cell voltage is less than Vcc, then charging current could flow into first cell if diode were not present
    - Not required if battery is only single cell battery
  - Must have series resistor (10Meg) in series with first cell tap
    - If cell voltage is greater than Vcc, the IC could draw all Vcc current from cell tap and unbalance the battery
      - Vcc and RBI are connected by FET that is on if Vcc > POR threshold
    - If Vcc drops, current through 10Meg will force voltage at RBI pin to drop below POR and disconnect all internal load except RAM
  - If unused, tie RBI to Vcc
  - Cap only on RBI is useful to support RAM power through short transients
    - Must have some means to determine whether RAM power is lost and RAM data has been corrupted

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- RBI issues
  - RBI function comparison
    - bq2050, bq2013h, bq2014h, bq2050h, bq2052, bq2913
      - Firmware does RAM corruption check after reset and does not reload original LMD and clear NAC if no corruption is detected
    - Bq2060
      - Firmware does RAM corruption check after reset and does not reload any RAM from EEPROM if no corruption is detected
    - bq2060A anc bq2063
      - Firmware does RAM corruption check after reset and does not set: RemainingCapacity=0, MaxError=100%, or Relearn_Flag=1 if no corruption is detected. All other RAM is reloaded from EEPROM
    - Battery Monitors (bq2018, bq2023, and bq26220)
      - All RAM is maintained by RBI. There is no hardware check for corruption. Data integrity determination is host responsibility
      - bq2018 -- all memory backed up
      - bq2023 -- all counters and 1 page of memory backed up
      - bq26220 -- all counters backed up, RAM is refreshed from flash on POR

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- **Sense resistor location**
  - **Normal location is between Vss of gauge and Bat-**
    - **Best location to maintain highest communication signal-to-noise ratio**
    - **Required location for single-ended VFC measurements (except bq2011)**
    - **Accuracy of gauges like bq2010 series and bq2040 too poor for voltage drop of sense resistor to be large issue**
    - **bq2060 measures Vsr and corrects battery voltage reading for Vsr drop**
    - **bq29311 AFE does not include Vsr in cell measurements sent to bq2083**
  - **Alternate location is between Vss of gauge and Pack-**
    - **bq2011 does this to allow larger voltage drop across sense resistor during discharge without issue of forward biasing ESD protection diode on SR pin**
      - Can't use DQ communication if large signal allowed
    - **bq2063 Vss must tie to Seiko S-8243 Vss**
      - Cannot have Vcc modulated by Vsr
      - S-8243 makes lowest cell voltage measurement with respect to Vss
    - **bq26200 uses single-ended voltage measurement**
      - Differential VFC input allows flexible Rsr location
      - Low Vsr drop insufficient to cause HDQ communication issue

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- VFC inputs
  - Recommended 100k and 0.1ufd filter on each input
    - Low-pass filtering reduces high-frequency noise and does not change the average value of the integrated waveform
    - High impedance reduces risk of damage to the SR inputs from ESD or momentary shorts of the battery
    - Place SR bypass caps as close as possible to the gauge, with short leads to both SR inputs and Vss
  - Tie VFC input sense leads to inside of sense resistor at point where etch is not carrying high current
    - “Kelvin” type connection
    - Adds least etch resistance in series with the sense resistor
- Coulomb counter inputs (bq2083)
  - Recommended 100 ohms and shunt 0.1ufd cap on each input plus 0.1ufd differential cap
    - Place the 3 caps as close to SR input pins as possible
    - Optimal layout can achieve 1uV offset difference to calibrated offset measured internally to IC.
      - Data flash board offset value allows setting external offset correction

# Miscellaneous design issues



- Sense resistor temperature coefficient
  - Not much concern with lower accuracy gauges
  - Noticeable current drift after high current application if poor temperature coefficient used
    - Especially evident with high accuracy of bq2063 and bq2083 current reporting
      - Recommendation is +/-75ppm/ºC
- Keep high-current and low-current grounds separate
  - ESD improvement
  - Measurement accuracy improvement
    - Lower VFC offset
  - Tie grounds together at same point as sense lead connection to sense resistor.
    - Vss connection is reference for single-ended VFC measurements as well as single-ended current measurement by the bq2060 and bq2063.