SLUS429B– FEBRUARY 2000 – REVISED NOVEMBER 2002

LITHIUM-ION AND LITHIUM-POLYMER BATTERY PROTECTOR

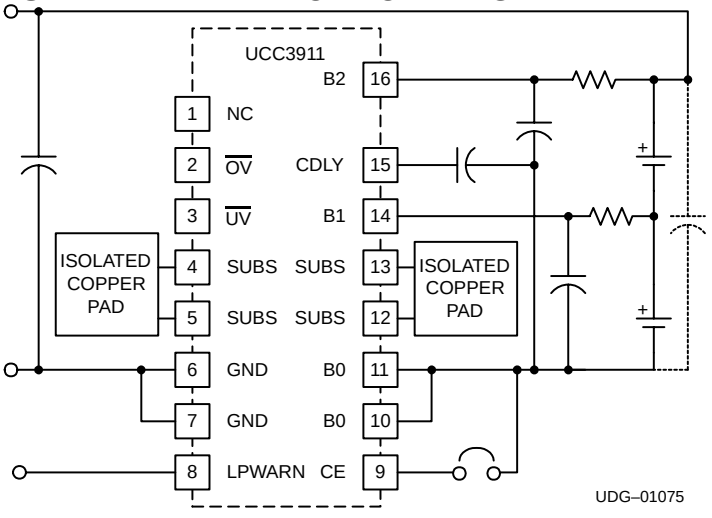
FEATURES

- **Protects Sensitive Lithium-Ion and Lithium-Polymer Cells from Overcharging and Overdischarging**
- **Used for Two-Cell Battery Packs**
- **No External FETs Required**
- **Provides Protection Against Battery Pack Output Short Circuit**
- **Extremely Low Power Drain on Batteries of About 20 μA**
- **Low Internal FET Switch Voltage Drop**
- **User Controllable Delay for Tripping Short Circuit Current Protector**
- **3-A Current Capacity**

APPLICATIONS

- **PDA, Camcorder, Digital Camera, Private Mobile Radio**

SIMPLIFIED APPLICATION DIAGRAM



DESCRIPTION

The UCC3911 is a two-cell lithium-ion (Li-Ion) and lithium-polymer (Li-Pol) battery pack protector device that incorporates an on-chip series FET switch thus reducing manufacturing costs and increasing reliability. The device's primary function is to protect both Li-Ion and Li-Pol cells in a two-cell battery pack from being either overcharged (overvoltage) or overdischarged (undervoltage). It employs a precision bandgap voltage reference that is used to detect when either cell is approaching an overvoltage or undervoltage state. When on-board logic detects either condition, the series FET switch opens to protect the cells.

A negative feedback loop controls the FET switch when the battery pack is in either the overvoltage or undervoltage state. In the overvoltage state the action of the feedback loop is to allow only discharge current to pass through the FET switch. In the undervoltage state, only charging current is allowed to flow. The operational amplifier that drives the loop is powered only when in one of these two states. In the undervoltage state the chip enters sleep mode until it senses that the pack is being charged.

The FET switch is driven by a charge pump when the battery pack is in a normally charged state to achieve the lowest possible $R_{DS(on)}$. In this state the negative feedback loop's operational amplifier is powered down to conserve battery power. Short circuit protection for the battery pack is provided and has a nominal delay of 100 μs before tripping. An external capacitor may be connected between CDLY and B0 to increase this delay time to allow longer overcurrent transients.

A chip enable (CE) pin is provided that when held low, inhibits normal operation of the device to facilitate assembly of the battery pack.

description (continued)

The UCC3911 is specified for operation over the temperature range of –20°C to 70°C, the typical operating and storage temperature range of Li-Ion and Li-Pol batteries.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)‡§

Maximum input voltage (B2, GND) . . . . . 14 V
Minimum input voltage (B0, GND) . . . . . –9 V
Maximum charge current (B0, GND) . . . . . 3.3 A
Minimum discharge current (B0, GND) . . . . . 3.3 A
Operating junction temperature range, T_J . . . . . –55°C to 150°C
Storage temperature range T_{stg} . . . . . –65°C to 150°C
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

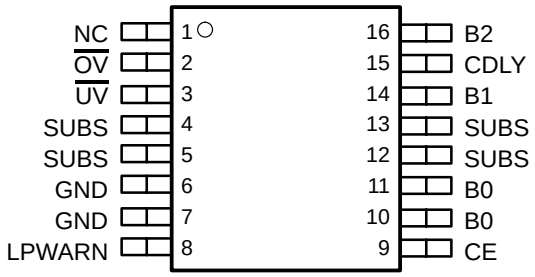
§ All voltages are with respect to ground. Currents are positive into and negative out of the specified terminals.

AVAILABLE OPTIONS

T_A	PACKAGES	OVERVOLTAGE THRESHOLD		
	SOIC–16 (D)	MIN	TYP	MAX
–20°C to 70 °C	UCC3911DP–1	4.15	4.20	4.25
	UCC3911DP–2	4.20	4.25	4.30
	UCC3911DP–3	4.25	4.30	4.35
	UCC3911DP–4	4.30	4.35	4.40

† The DP package is available taped and reeled. Add TR suffix to device type (e.g. UCC3911DPTR–1) to order quantities of 3000 devices per reel.

DP PACKAGE
(TOP VIEW)



electrical characteristics –20°C < T_A = 70°C, all voltages are referenced to B0, V_{B2} = 7.2 V, T_A = T_J (unless otherwise noted)

state transition threshold

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{OV}	Overvoltage threshold	UCC3911–1		4.15	4.20	4.25	V
V_{OVR}	Overvoltage threshold recovery	UCC3911–1		3.60	3.70	3.80	V
V_{OV}	Overvoltage threshold	UCC3911–2		4.20	4.25	4.30	V
V_{OVR}	Overvoltage threshold recovery	UCC3911–2		3.65	3.75	3.85	V
V_{OV}	Overvoltage threshold	UCC3911–3		4.25	4.30	4.35	V
V_{OVR}	Overvoltage threshold recovery	UCC3911–3		3.70	3.80	3.90	V
V_{OV}	Overvoltage threshold	UCC3911–4		4.30	4.35	4.40	V
V_{OVR}	Overvoltage threshold recovery	UCC3911–4		3.75	3.85	3.95	V
V_{UV}	Undervoltage threshold			2.42	2.50	2.58	V
V_{UVR}	Undervoltage threshold recovery			2.90	3.00	3.10	V

B0-to-GND switch

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{B0} to V_{GND}	(Normal) I_{GND} = 2 A	–320	–160		mV
V_{B0} to V_{GND}	(Normal) I_{GND} = –2 A		160	320	mV
V_{B0} to V_{GND}	(Overcharge) I_{GND} = 1 mA	–300	–150		mV
V_{B0} to V_{GND}	(Overcharge) I_{GND} = 2 A	–500	–250		mV
V_{B0} to V_{GND}	(Undercharge) I_{GND} = –1 mA		150	300	mV
V_{B0} to V_{GND}	(Undercharge) I_{GND} = –2 A		250	500	mV
I_{GND}	(Overcharge) V_{GND} = –5 V	–5			µA
I_{GND}	(Undercharge) V_{GND} = 5 V		0	30	µA

input bias current

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{B2}	Nominal		18	25	µA
I_{B2}	In sleep mode		3.5		µA
I_{B1}		–1	0	1	µA

short circuit protection

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{SC}	Current threshold		3.5	5.25	7	A
t_{DLY}	Delay time	CDLY = OPEN, See Note 1		100		µs

timing delays

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$F_{INTERNAL}$	Internal clock frequency	See Note 2		7.5		kHz
t_{DLY} – $\overline{OV}$	Delay time to register overcharge		0.6	2.0	5.0	ms
t_{DLY} – $\overline{UV}$	Delay time to register undercharge		0.3	1.0	3.5	ms

electrical characteristics –20°C < T_A = 70°C, all voltages are referenced to B0, V_{B2} = 7.2 V, T_A = T_J (unless otherwise noted) (continued)

drives

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{B2}–V_{HIGH}	$\overline{OV}$ and $\overline{UV}$ output	I_{PIN} = –100 μA		0.15	0.89	V
V_{LOW}		I_{PIN} = 100 μA		0.05	0.75	
V_{B2}–V_{HIGH}	LPWARN output	I_{LPWARN} = –0.1 mA		0.05	0.75	V
V_{LOW}		I_{LPWARN} = 0.1 mA		0.04	0.75	

other thresholds

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CE}	Chip enable threshold voltage	V_{B2} = 8.5 V	5	6	7	V
		V_{B2} = 5 V, See Note 3	2.05	2.45	4.05	
T_{SD}	Thermal shutdown	See Note 1		165		°C

NOTE: 1. Ensured by design. Not production tested.
NOTE: 2. Tested at functional probe only.
NOTE: 3. V_{B2} is the voltage at the B2 pin relative to the B0 pin.

Terminal Functions

TERMINAL NAME	TERMINAL PACKAGE DP	I/O	DESCRIPTION
B0	10, 11	I	Connects to the negative teminal of the lower cell in the battery pack.
B1	14	I	Connects to the junction of the positive terminal of the lower cell and the negative terminal of the upper cell in the battery pack.
B2	16	I	Connects to the positive terminal of the upper cell in the battery pack. This pin also connects to the positive of the two terminals that are presented to the user of the battery pack.
CDLY	15	I	Delay control pin for the short circuit protection feature.
CE	9	O	Chip enable. The internal FET is disabled when CE is connected to B0. With the CE pin connected to B0, the supply current drain is only about 4 μA.
GND	6,7	–	The second of two terminals that are presented to the user of the battery pack. The internal FET switch connects this terminal to the B0 terminal to give the battery pack user appropriate access to the batteries. In an overcharged state, current is allowed to flow only into this terminal. Similarly, in an over-discharged state, current is allowed to flow only out of this terminal.
LPWARN	8	O	This active–high signal is the low Power Warning. The voltage on this pin goes high (to B2 potential) as soon as either of the battery's cells voltage falls below 3.0 V. Once the UV state is entered, this output goes back to low.
$\overline{OV}$	2	O	This active–low signal indicates the state of the state machine's $\overline{OV}$ bit. When low, it indicates that one or both cells are overvoltage. Further charging is inhibited by the opening of the FET switch. The output buffer for this pin is sized to drive a very light load.
SUBS	4,5,12,13	I	The substrate connections connect these points to a heat sink which is electrically isolated from all other device pins.
$\overline{UV}$	3	O	This active–low signal indicates the state of the state machine's undervoltage bit. When low, it indicates that one or both cells are under voltage. Further discharging is inhibited by the opening of the FET switch.

detailed pin descriptions

CDLY: Delay control pin for the short circuit protection feature. A capacitor connected between this pin and the B0 pin lengthens the time delay from when an overcurrent situation is detected to when the protection circuitry is activated. This control will be useful for those applications where high-peak load currents may momentarily exceed the protection circuit's threshold current and interruption of the battery current is undesirable. The nominal delay time is internally set at 100 μs. The equation for determining this delay is:

$$t_{DLY}(\mu s) = 25 + (25 + \text{CDLY (pF)}) \times 0.4 \times V_{B2} \quad (1)$$

To recover from an overcurrent *shutdown* the load must be removed momentarily from the pack.

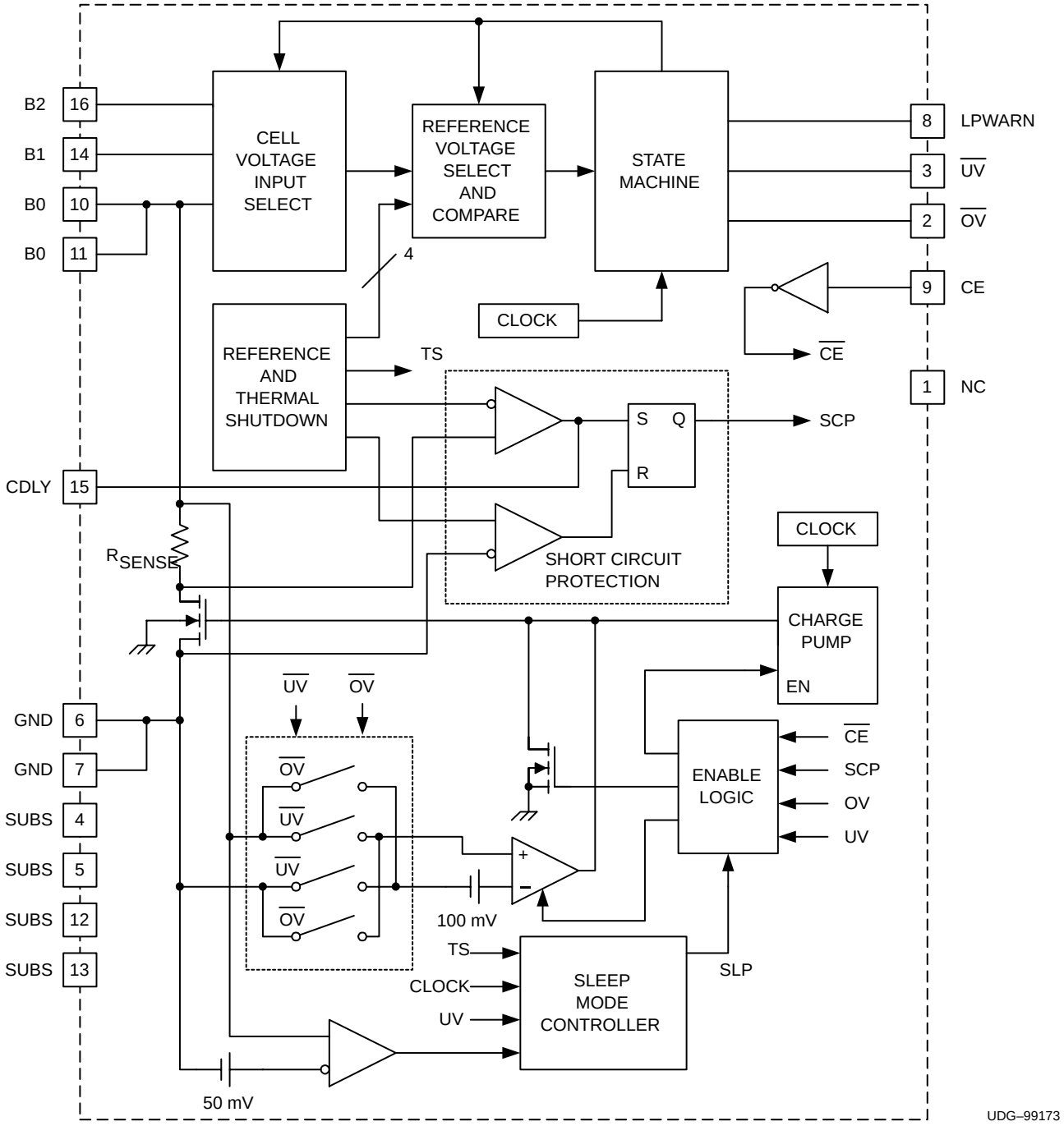
CE: While the chip enable signal is held low, the internal FET is held off. CE is pulled high by a 2-μA current source. This function was included to facilitate construction of the battery pack. The last step in the electrical assembly of the pack is to cut a link grounding B0. With the CE pin connected to B0, the supply current drain is only about 4 μA.

GND: The second of the two terminals that are presented to the user of the battery pack. The internal FET switch connects this terminal to the B0 terminal to give the battery pack user appropriate access to the cells. In an overvoltage state, current is allowed to flow only into this terminal. Similarly, in an undervoltage state, current is allowed to flow only out of this terminal.

$\overline{\text{OV}}$: This active-low signal indicates the state of the state machine's overvoltage bit. When low, it indicates that one or both cells are overvoltage. Further charging is inhibited by the opening of the FET switch. The output buffer for this pin is sized to drive a very light load.

$\overline{\text{UV}}$: This active-low signal indicates the state of the state machine's undervoltage bit. When low, it indicates that one or both cells are undervoltage. Further discharging is inhibited by the opening of the FET switch. The chip enters the *sleep* mode when $\overline{\text{UV}}$ goes low and waits in this state until the device detects that the battery pack has been placed in a charging circuit. The output buffer for this pin is sized to drive a very light load.

functional block diagram



APPLICATION INFORMATION

Figure 1 shows a typical application for the UCC3911 Li-Ion and Li-Pol battery protector. All of the functions required to protect two series cells from overvoltage and undervoltage conditions, as well as provide short circuit protection for the complete battery pack, are included in a single chip. An internal state machine controls an internal power FET which allows either bi-directional or uni-directional battery current. An optional time delay capacitor can be included to slow the reaction time of the short circuit protection circuitry if desired.

While the device is capable of providing overload and over/undervoltage protection of both cells with virtually no external parts, the demands of true short circuit protection require some passive external components.

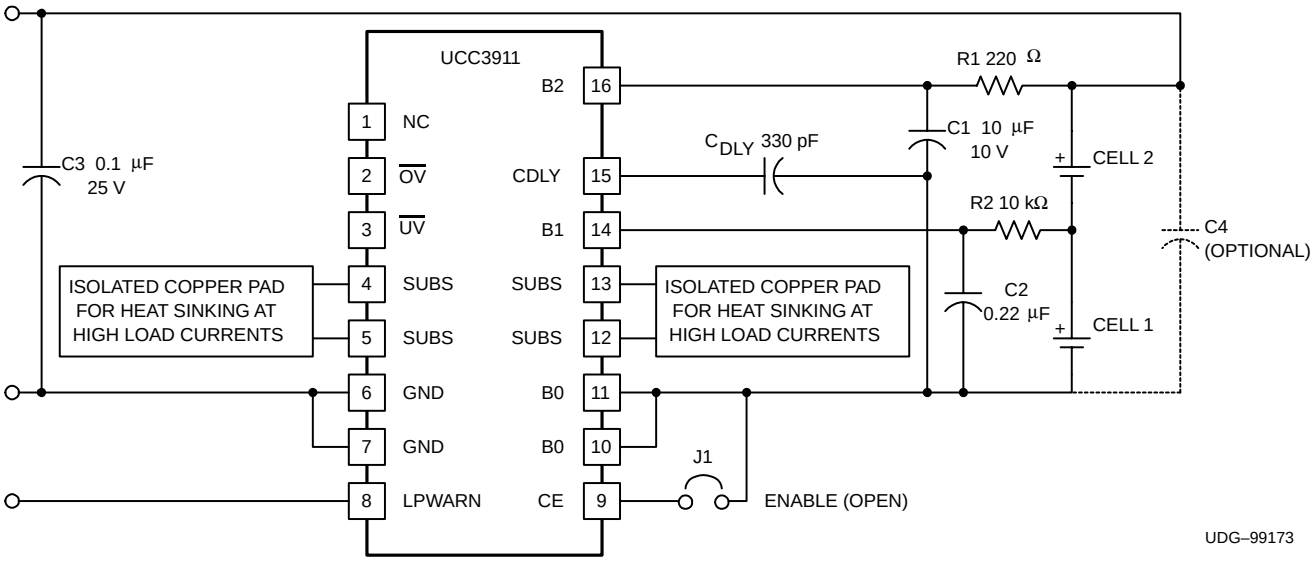


Figure 1. Application Circuit Including Components for Short-Circuit Protection

state machine operation

The internal state machine constantly monitors the two cells for both overvoltage and undervoltage conditions. Figure 2 shows a state diagram which describes the operation of the protection circuitry for the UCC3911–2 version. In the normal mode, both the external overvoltage and undervoltage status bits are held high and full battery current is allowed through the internal power FET in either the charge or discharge direction.

If the voltage across one or both cells exceeds the overvoltage (V_{OV}) threshold, the external overvoltage signal goes low, and further charge current is not allowed. An internal feedback loop controls the power FET to allow only discharge current, allowing for battery recovery. The state machine will not reenter normal mode until the voltage across both cells decays to less than the overvoltage recovery (V_{OVR}) threshold. This feature is important to prevent circuit oscillation due to battery ESR when the circuitry transitions between states.

If the voltage across one or both battery cells falls below 3 V, the LPWARN signal goes high indicating a low power condition. This signal can be used to signal the user that the battery pack is in need of charge.

If the voltage across one or both cells falls below 2.5 V, the $\overline{UV}$ signal goes low, and the feedback loop allows only charge current. The LPWARN signal goes low and the UCC3911 enters sleep mode which consumes only 3 µA, limiting self discharge to a minimum. The circuit remains in this state until the voltage across both cells exceeds 3 V. The battery pack can still be charged, unless the sum of the two cells voltages falls below 3.7 V, which is the minimum guaranteed operating voltage for the device.

APPLICATION INFORMATION

If the battery cells become so poorly matched that the voltage across one cell exceeds 4.25 V and the voltage across the other cell falls below 2.5 V, the power FET does not pass either charge or discharge current, and both the $\overline{OV}$ and $\overline{UV}$ signals will be set low.

The normal high current path for battery current is through the B0 (10, 11) and GND (6, 7) pins of the UCC3911. The GND pins are intended to be connected to system ground for either the charger or the load. The SUBS pins (4, 5, 12, 13) are internally connected to the substrate of the UCC3911, which is internally referenced to B0 or GND depending on the direction of pack current. If high battery currents are anticipated, the SUBS pins can be thermally connected to a heat sink to control the device temperature. However, this heat sink must be electrically isolated from all other device pins including ground. This is a critically important point, as heat sinking to the system ground is not possible.

The CE pin is used to initialize the state of the battery pack during assembly. Holding this pin low forces the state machine to hold the FET off. The last step in the assembly process would be to cut the trace between this pin and B0 which allows the internal pull up to start the state machine. While CE is low, the device's current consumption is approximately 4 μA. This is a useful feature for battery packs that may experience a long period of storage while waiting to be sold.

The *one cell over and one cell under* state (see Figure 2) is entered whenever one cell is overcharged and the other cell is simultaneously overdischarged. When in this state, the series FET switch is turned off inhibiting both charging and discharging of the battery pack. If the battery pack ever gets into this condition, it should be discarded.

short-circuit protection

The demands of true short-circuit protection require that careful attention be paid to the selection of a few external components.

In the application circuit shown in Figure 1, C3 protects the battery pack output terminals from inductive kick when the pack current is shut off due to an overcurrent or overvoltage/undervoltage condition. (It also increases the ESD protection level.)

To prevent a momentary cell voltage drop, caused by large capacitive loads, from causing an erroneous undervoltage shutdown, an RC filter is required in series with the two battery sense inputs, B1 and B2. The resistors (R1 and R2) are sized to have a negligible impact on voltage sensing accuracy. The capacitors (C1 and C2) should be sized to provide a time constant longer than the overcurrent delay time. In the example of Figure 1, they are sized for a nominal 2.2 ms time constant. They do not need to be low ESR style capacitors, as they see no ripple current. A larger resistor value and smaller capacitor value can be used on the B1 input due to the extremely low input current on this pin.

The overcurrent delay capacitor, CDLY, sets the time delay, after the overcurrent threshold is exceeded, before turning off the UCC3911's internal FET. If no capacitor is used, the nominal delay is 100 μs. To charge large capacitive loads without tripping the overcurrent circuit, a small capacitor (typically less than 1000 pF) is used to extend the delay time. The approximate delay time is given below and shown graphically in Figure 3.

$$t_{DLY}(\mu s) = 25 + (25 + CDLY(pF)) \times 0.4 \times V_{B2} \quad (2)$$

APPLICATION INFORMATION

UCC3911–2 STATE DIAGRAM

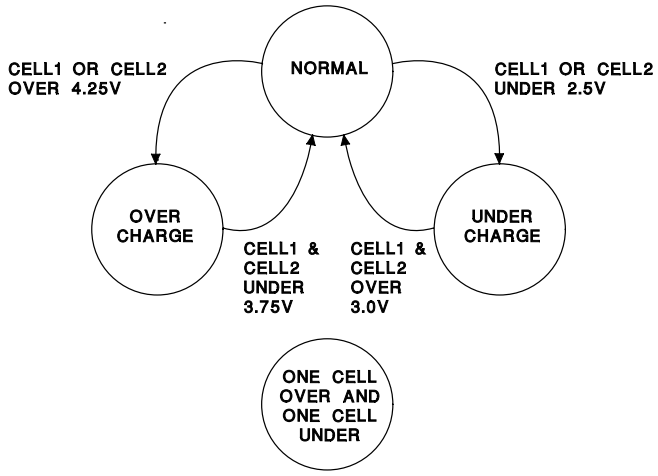


Figure 2

NOMINAL OVERCURRENT DELAY TIME
vs
DELAY CAPACITANCE AND B2 VOLTAGE

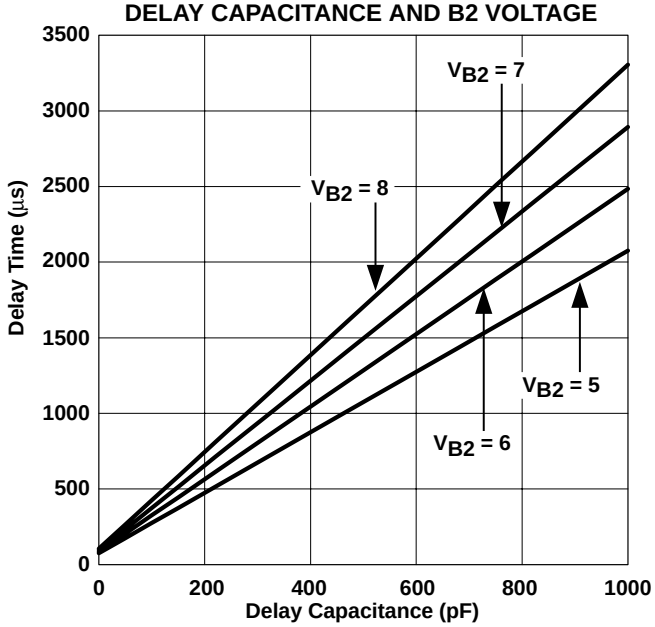


Figure 3

The amount of time required will be a function of the load capacitance, battery voltage, and the total circuit impedance, including the internal resistance of the cells, the UCC3911's on resistance, and the load capacitor ESR. The required delay time can be calculated from:

$$t = -R \times C \times \ln\left(\frac{I \times R}{V}\right) \quad (3)$$

In this equation, R is the total circuit resistance, C is the capacitor being charged, I is the overcurrent trip current (5.25 A nominal), and V is the battery voltage. Using the minimum trip current of 3.5 A and the maximum battery voltage of 8.4 V, the worst case maximum delay time required is defined as:

$$t_{MAX}(\mu s) = -R \times C(\mu F) \times \ln\left(\frac{R}{2.4}\right) \quad (4)$$

In the example of Figure 1, CDLY, C1 and C2 are sized to drive a 1500-µF load capacitor.

If large capacitive loads (or other loads with surge currents above the overcurrent trip threshold) are not being applied to the pack terminals, the overcurrent delay time can be short. In this case, it may be possible to eliminate CDLY, as well as R2 and C2 altogether (replacing R2 with a short). In addition, the time constant of R1 and C1 can be made much shorter. R1 and C2 are still necessary, however, to assure proper operation under short circuit conditions. It is important to maintain a minimum R1/C1 time constant of 100 µs. (For example, R1 and C1 could be reduced to 100 Ω and 1 µF.)

Capacitor C4 is recommended, in case the wires connecting to the top and bottom of the cell stack are more than an inch long (not likely in a small battery pack). In this case, a 10-µF, low ESR capacitor is recommended to prevent excessive overshoot at turn-off due to wiring inductance.

PACKAGING INFORMATION

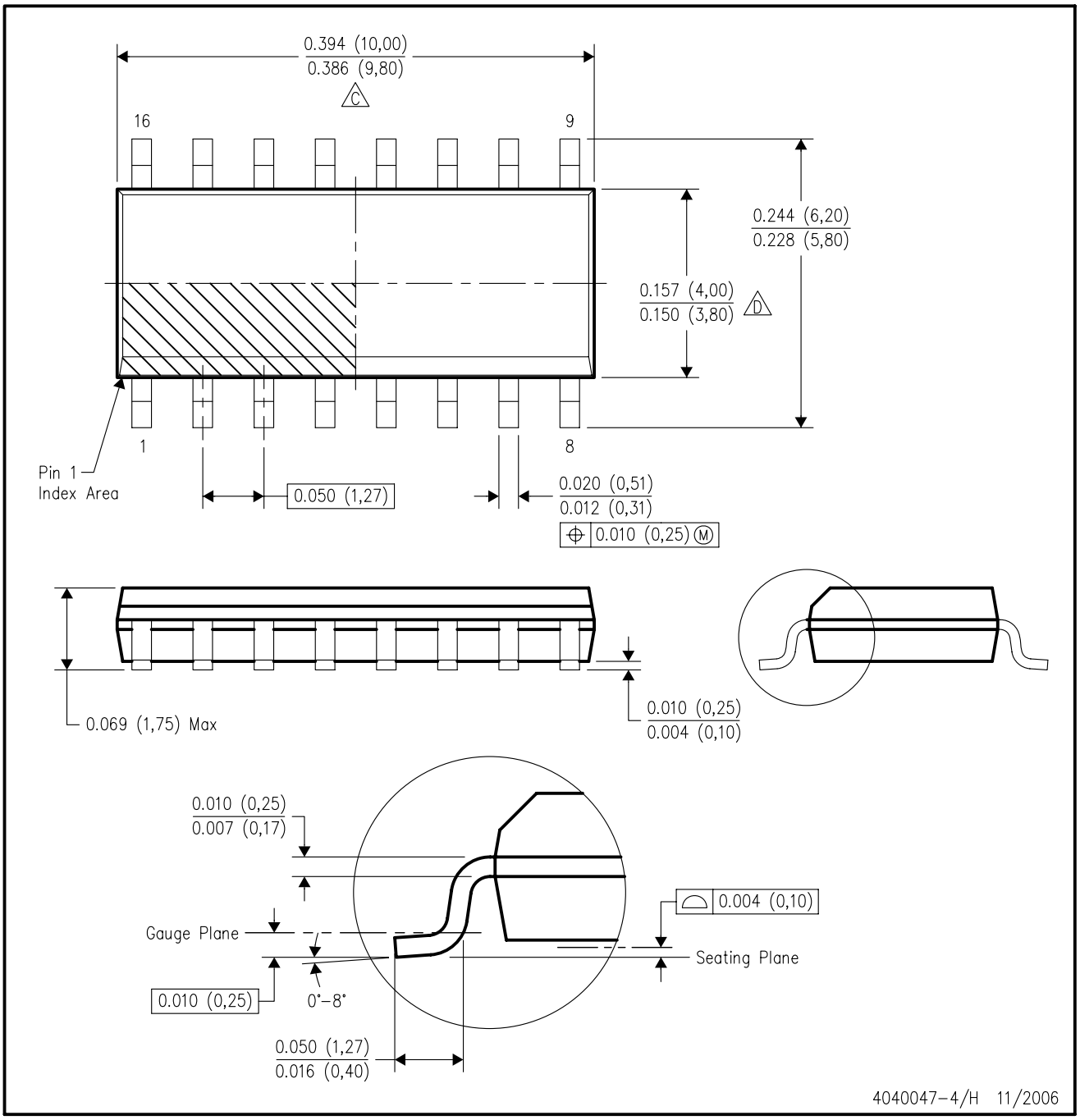
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCC3911DP-1	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU EPD1	Level-2-260C-1 YEAR
UCC3911DP-1G4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU EPD1	Level-2-260C-1 YEAR
UCC3911DP-2	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
UCC3911DP-2G4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
UCC3911DP-3	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
UCC3911DP-3G4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
UCC3911DP-4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
UCC3911DP-4G4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR
UCC3911DPTR-2G4	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

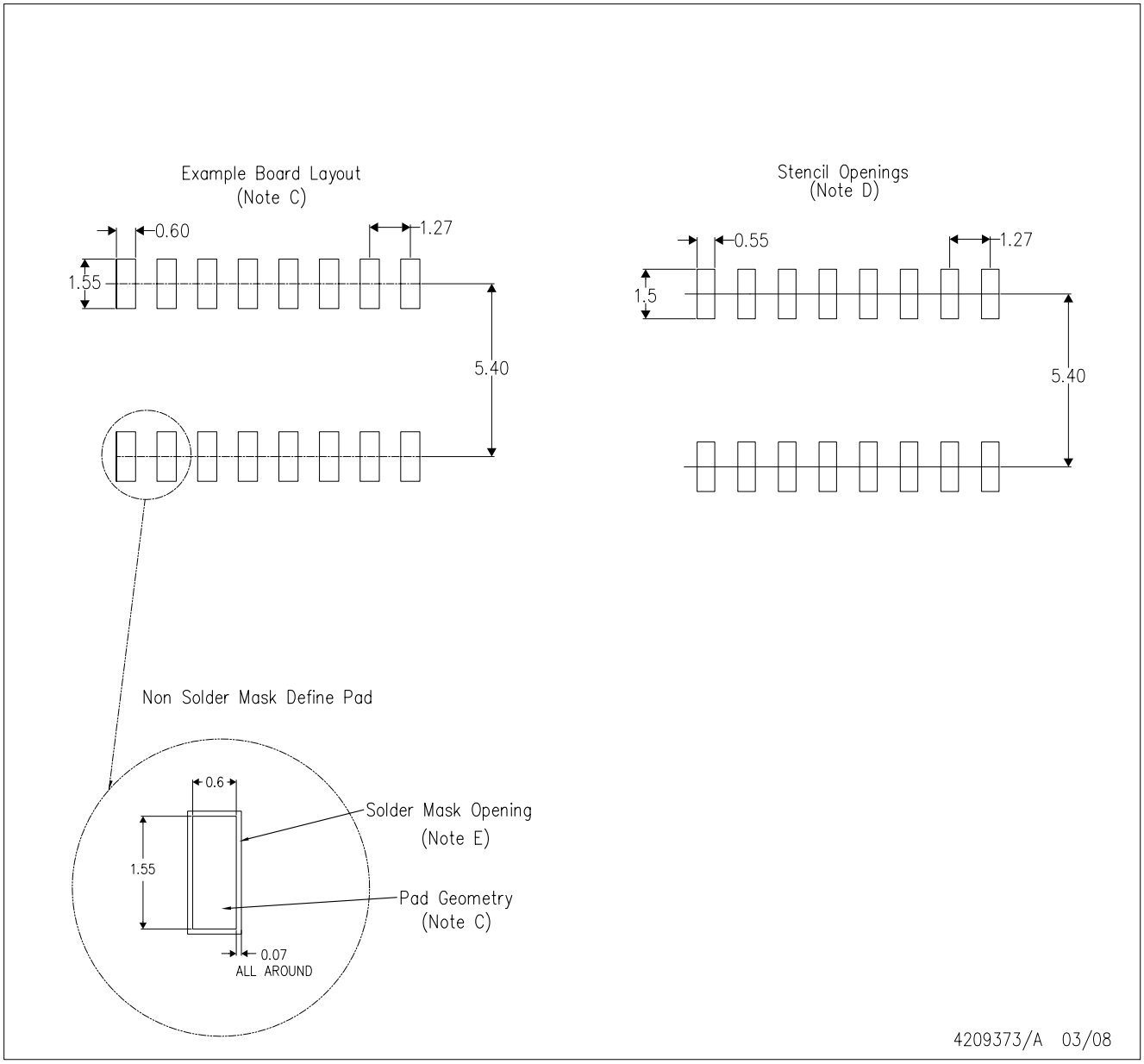
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

D(R–PDSO–G16)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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