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Battery Pack Protection and Monitor IC

FEATURES

- **Supports 6-12 Series Li-ion Battery Cells including Cobalt, Manganese, Phosphate Cells and Fuel cells**
- **Supply Voltage Range from 9.0V to 60V**
- **Multi-channel ADC for voltage and temperature measurement**
  - 12 channels for cell voltage measurement (12 bits).
  - 1 channel for internal temperature measurement (12 bits)
  - 2 channels for external temperature measurement(12 bits)
- **Built-in Protections include:**
  - Over voltage (OV)
  - Under voltage (UV)
  - Cell voltage unbalance (UB)
  - Over current (OC)
  - Short circuit (SC)
  - Over temperature (OT)
  - Under temperature (UT)
  - Over Voltage Permanent Fail (OVPF) (over voltage secondary protection)
- **Embedded 64X16 Bits EEPROM supports (**EEPROM write/erase life cycle is about 100000 times at ambient temperature 25 ^{o}C) **programmable settings of various protection thresholds/timers and protection release thresholds/timers**
- **Supports Internal Bleeding for Cell balance**
- **Supports separate charge and discharge loop**
- **Integrated 3.3V, 10V voltage regulator**
- **Integrated MOSFET driver**
- **Supports SMBus serial Interface**
- **ALERTN (low pulse unmasked interrupt) output support**
- **Low power consumption**
  Full Power Mode < 500uA
  Sleep Mode < 30uA

APPLICATIONS

- **Electric Bicycle**
- **Electric Motorcycle**
- **Power Tools**
- **UPS backup battery**
- **Fuel Cell applications**

GENERAL DESCRIPTION

OZ8940 is a highly integrated battery pack protection and monitor IC for managing Li-Ion or Li-polymer pack in electric bicycle, electric motorcycle, power tools, and UPS applications. It supports 6-12 series Li-Ion battery pack or Li-polymer or Fuel cells battery pack applications.

With integrated multi-channel 12-bit ADC, OZ8940 works constantly to monitor each cell's voltage, and the pack temperature to provide over-voltage, under-voltage, cell voltage unbalance, over-current, short circuit, over-temperature and under-temperature safety protection. Working with embedded FET driver circuits, the protection circuits will independently shut off the FETs when the battery cells are experiencing extreme stress. When cell voltage is higher than the pre-set maximum rating voltage OVPF, OZ8940 can automatically assert the Permanent Fail (PF) signal to blow an external fuse to cut off the power line or to signal an alarm to user. All of the protection thresholds and their related delay time are programmable in EEPROM for different battery types and different applications.

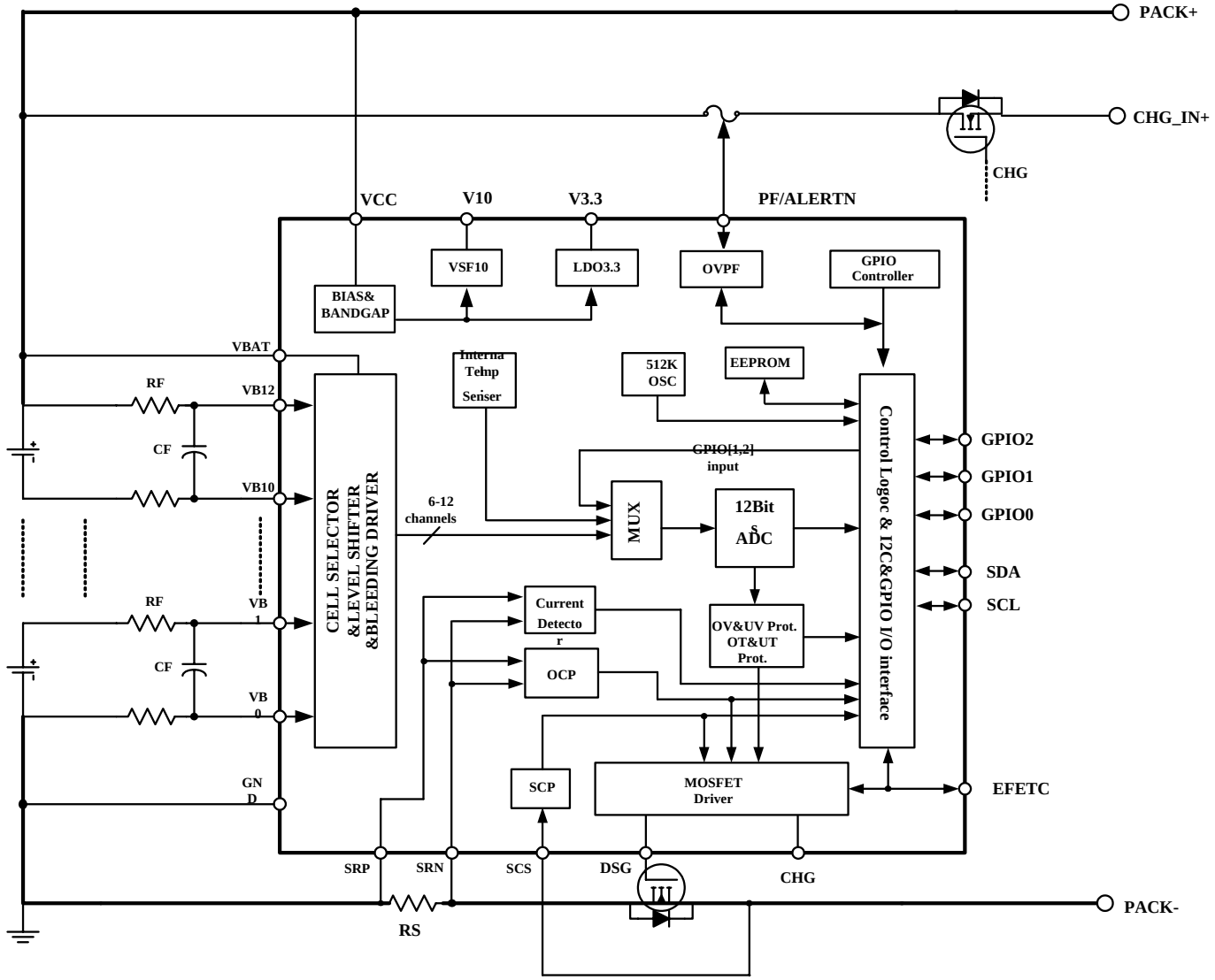
"Balance on Demand (BOD)" technology has been embedded in the OZ8940 to support internal bleeding for cell voltage balance during charge state or idle state (no charge and discharge); BOD technology can achieve longer life cycle for the battery pack.

OZ8940 can work with external uP or MCU to implement more featured function.

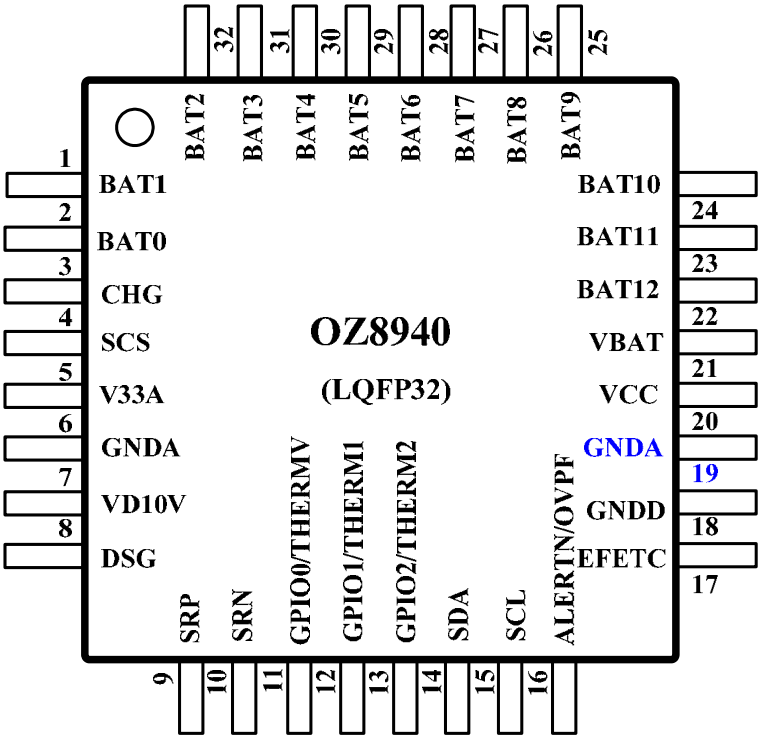
ORDERING INFORMATION

Part Number	Temp Range	Package
OZ8940TN	-40^{o}C to 85^{o}C	LQFP32L

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

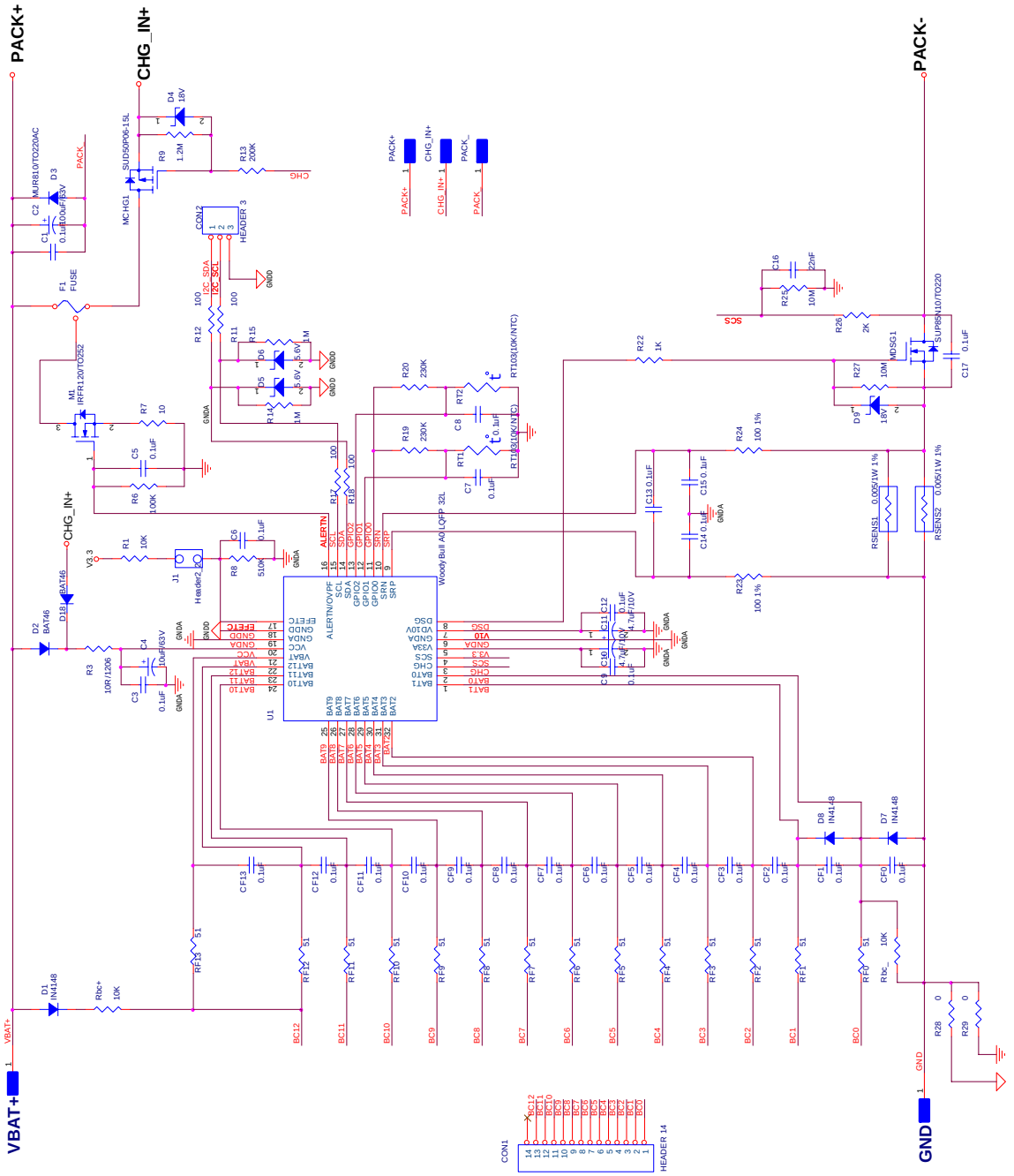
Name	Pin No	I/O	Description
BAT1	1	I	Cell1 positive input
BAT0	2	I	Cell1 negative input
CHG	3	O	Charge MOSFET control, Sink 10uA current at CHG FET ON, high impedance at CHG FET OFF.
SCS	4	I	Short circuit external automatic release input/ and detection SC event in full power mode and sleep mode, the threshold is about 1V.
V33A	5	Power	3.3V power supply. Maximum supply is 30mA in full power mode, maximum supply is about 100uA in sleep mode.
GNDA	6	Ground	Analog ground
VD10V	7	Power	10V power supply for MOSFET driver. Maximum supply is 10mA in full power mode and sleep mode.
DSG	8	O	Discharge MOSFET control. Push-pull structure, drive to high level 10V to turn on DSG FET, drive to low level 0V to turn off DSG FET.
SRP	9	I	Current sense resistor positive terminal
SRN	10	I	Current sense resistor negative terminal
GPIO0/THERMV	11	I/O	General Purpose Input/Output Pin OR External thermal sensor driver voltage (3.3V)

Name	Pin No	I/O	Description
GPIO1/THERM1	12	I/O	General Purpose Input/Output Pin OR External thermal sensor input 1
GPIO2/THERM2	13	I/O	General Purpose Input/Output Pin OR External thermal sensor input 2
SDA	14	I/O	SMBUS data input
SCL	15	I/O	SMBUS clock input
ALERTN/OVPF	16	O	Alert output to uP (active low) / Over Voltage Permanent failure output. Active high
EFETC	17	I/O	External FET control signal, can be configured to input or output
GNDD	18	Ground	Digital ground
GNDA	19	Ground	Analog ground
VCC	20	Power	Chip Power supply
VBAT	21	Power	Internal level shifter power supply
BAT12	22	I	Cell12 positive input
BAT11	23	I	Cell11 positive input
BAT10	24	I	Cell10 positive input
BAT9	25	I	Cell9 positive input
BAT8	26	I	Cell8 positive input
BAT7	27	I	Cell7 positive input
BAT6	28	I	Cell6 positive input
BAT5	29	I	Cell5 positive input
BAT4	30	I	Cell4 positive input
BAT3	31	I	Cell3 positive input
BAT2	32	I	Cell2 positive input

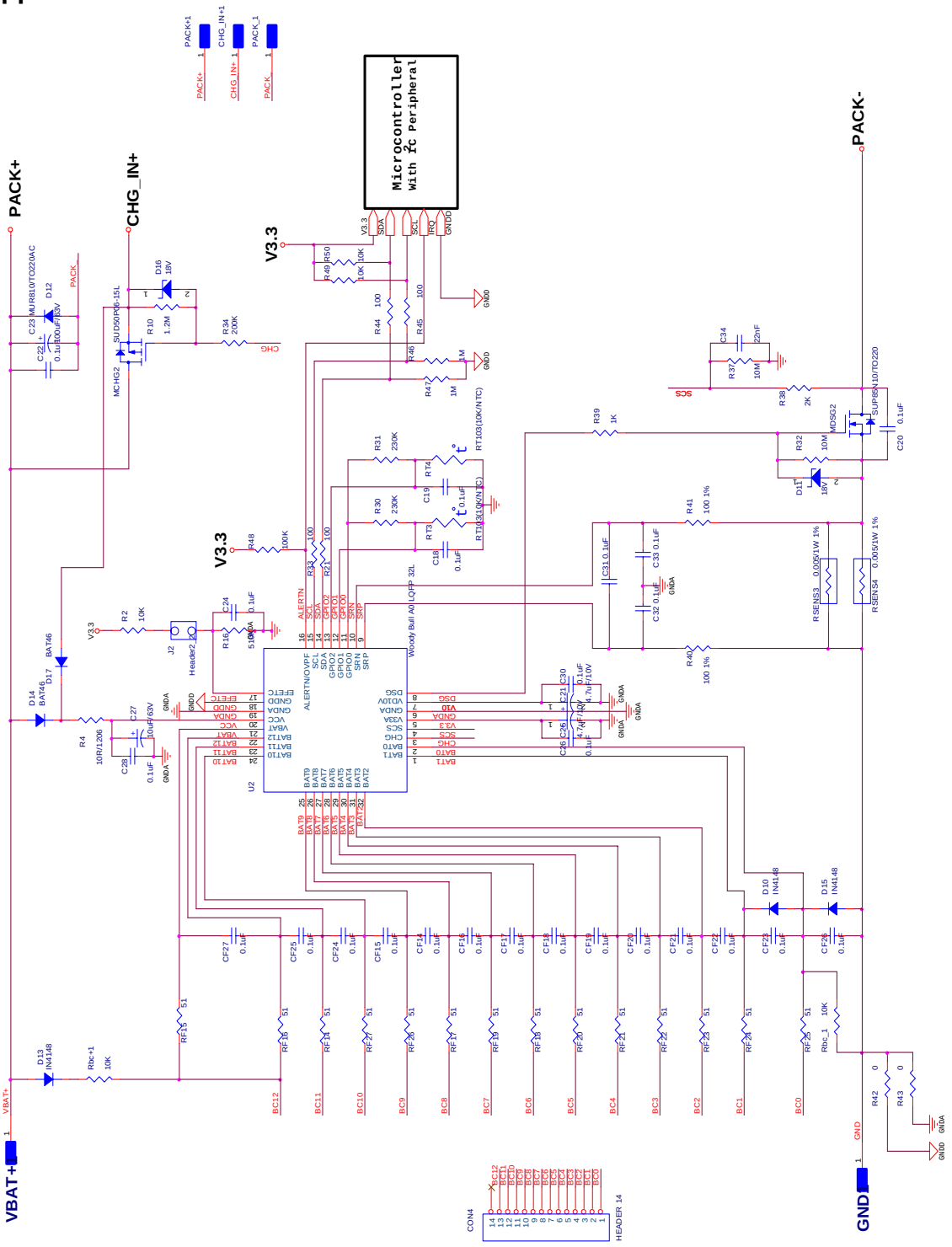
Note 1: All GPIO or open drain pins needs be pull-high or pull-low when not used.

TYPICAL APPLICATION SCHEMATICS

Hardware Mode



Application with MCU



DC CHARACTERISTICS

Absolute Maximum Ratings

Supply voltage range		VCC,VBAT	-0.3V to 60V
Input	Analog	SRP,SRN	-0.3V to 5.5V
	Analog	THERM1(12bits ADC input),THERM2(12bits)	-0.3V to 5.5V
	Analog	BAT0 to BAT1,BAT1 to BAT2,BAT2 to BAT3,BAT3 to BAT4,BAT4 to BAT5,BAT5 to BAT6,BAT6 to BAT7,BAT7 to BAT8, BAT8 to BAT9, BAT9 to BAT10, BAT10 to BAT11, BAT11 to BAT12	-0.3V to 5.5V
	Analog	SCS	-0.3V to 60V
Output	Analog	CHG(10uA sink current)	-0.3V to 60V
	Analog	DSG	-0.3V to 12V
	Analog	THERMV(power supply for temperature sense resistor)	-0.3V to 5.5V
	Digital	ALERTN/OVPF	-0.3V to 5.5V
I/O	Digital	GPIO[0:2], SCL, SDA, EFETC,	-0.3V to 5.5V
Operating free-air temperature range, TA			-40℃ to 85℃
Storage temperature range, Tstg			-55℃ to 150℃
Lead temperature(soldering, 10 sec)			300℃

Note 1: All voltages are with respect to ground of this device except BATn - BAT(n-1),where n=1,2,3,4,5,6,7,8,9,10,11,12cell voltage
Note 2: Ground refers to common node of GNDA and GNDD

Electrical Characteristics

Power Supply					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Supply Voltage(VCC)		9		60	V
Supply Current	Full Power Mode			500	uA
	Sleep Mode			30	uA

General Purpose Inputs And Outputs(GPIO)					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
V_{IH} High-level Input Voltage		2			V
V_{IL} Low-level Input Voltage				0.8	V
V_{OH} Output Voltage High	ILoad=-0.5mA	V3.3-0.7			V
V_{OL} Output Voltage Low	ILoad=0.5mA			0.4	V
Current Drive Capability	GPIO0		1		mA
Current Drive Capability	GPIO1, 2		8		mA

Note 1: All GPIO or open drain pins needs be pull-high or pull-low when not used.

3.3V LDO Regulator					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Regulator Output Voltage (Full power mode)	I_o<30mA	2.97	3.3	3.63	V
Line Regulation @ iload=20mA				200	mV
Load Regulation @ Vcc=32V				127	mV
3.3V Current Limit (Full power mode)				30	mA
Regulator Output Voltage (sleep mode)	I_o<100uA	2.8	2.95		V
Current Limit (sleep mode)				100	uA

10V LDO Regulator					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Regulator Output Voltage (Full power mode, Sleep mode)	I_o<10mA	9.45	10.5	11.55	V
Line Regulation @ iload=5mA				500	mV
Load Regulation @ Vcc=32V				1500	mV
10V Current Limit				10	mA

Multi-Channel ADC						
Parameter		**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Lion-ion Cell Voltage Channel	Input Voltage Range		0.45		5	V
	Resolution			12 bits		
	Conversion Time			16		mS
	Offset		Auto offset cancellation			
	Slope		Support slope calibration in MCU application			
Internal Temperature (1 channel)	Input Voltage Range		0.1		2.5	V
	Resolution			12 bits		
	Conversion Time			16		mS
	Offset		Auto offset cancellation			
	Slope		Support slope calibration in MCU application			
GPIO[1:2] channel	Input Voltage Range		0.1		2.5	V
	Resolution			12 bits		
	Conversion Time			16		mS
	Offset		Auto offset cancellation			
	Slope		Support slope calibration in MCU application			

Internal Oscillator					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
512kHz Oscillator Frequency		470	512	552	KHz
32kHz Oscillator Frequency		25.6	32	38.4	KHz

Over-Current(OC) And Short-Circuit(SC) Protection				
Parameter	**Test Conditions**	**MIN**	**MAX**	**Step/Unit**
OC Detection Threshold Range (Voltage across SRP & SRN)	Charge Over Current (COC)	10mV	105mV	5mV
	Discharge Over Current 0(DOC0)	30mV	285mV	5mV
	Discharge Over Current 1(DOC1)	50mV	620mV	10mV
OC Hysteresis Value	COC	N/A		
	DOC0	10mV		mV
	DOC1	20mV		mV
OC Delay Time (8-bit setup)	COC	2ms	512ms	***Note1***
	DOC0	2ms	16S	***Note2***
	DOC1	32us	256mS	***Note3***
OC Release Time (3-bit setup)	COC	1s	8s	Variable
	DOC0	1s	4s	Variable
	DOC1	1		Minute
SC Detection Threshold Range (SCS pin voltage)	SC	1.0	1.2	V
SC Hysteresis Value	SC	N/A		
SC Delay Time (8-bit setup)	SC	128us	1ms	***Note 4***
SC Release Time (3-bit setup)	SC	1min		Minute

Note1: The 3 bits are used to indicate the COC delay time as following:

COC delay	COC delay time	COC delay	COC delay time
3'b000	2ms	3'b100	64ms
3'b001	4ms	3'b101	128ms
3'b010	8ms	3'b110	256ms
3'b011	16ms	3'b111	512ms

Note2: The 4 bits are used to indicate the DOC0 delay time as following:

DOC0 delay	*DOC0 delay time*	*DOC0 delay*	*DOC0 delay time*
4'b0000	***2ms***	4'b1000	***256ms***
4'b0001	***4ms***	4'b1001	***512ms***
4'b0010	***8ms***	4'b1010	***768ms***
4'b0011	***16ms***	4'b1011	***1s***
4'b0100	***32ms***	4'b1100	***2s***
4'b0101	***64ms***	4'b1101	***4s***
4'b0110	***96ms***	4'b1110	***8s***
4'b0111	***128ms***	4'b1111	***16s***

Note3: The 4 bits are used to indicate the DOC1 delay time as following:

DOC1 delay	**DOC1 delay time**	**DOC1 delay**	**DOC1 delay time**
4'b0000	32us	4'b1000	8ms
4'b0001	64us	4'b1001	16ms
4'b0010	128us	4'b1010	32ms
4'b0011	256us	4'b1011	48ms
4'b0100	512us	4'b1100	64ms
4'b0101	1ms	4'b1101	96ms
4'b0110	2ms	4'b1110	128ms
4'b0111	4ms	4'b1111	256ms

Note4: The 2 bits are used to indicate the SC delay time as following:

SC delay	**SC delay time**	**SC delay**	**SC delay time**
2'b00	0us	2'b10	512us
2'b01	128us	2'b11	1ms

Over-Voltage(OV) And Under-Voltage(UV) Protection					
Parameter	**Test Condition**	**MIN**	**TYP**	**MAX**	**Unit/step**
OV Detection Threshold Value		12bits programmable (0-5V)			V
OV Release Value		12bits programmable (0-5V)			V
OV Delay Time (2-bit setup)		2		8	Scan Cycle
OV Release Time (same as OV delay time)		2		8	Scan Cycle
UV Detection Threshold Value		12bits programmable (0-5V)			V
UV Release Value		12bits programmable (0-5V)			V
UV Delay Time (4-bit setup)		1		8	Scan Cycle
UV Release Time (same as UV delay time)		1		8	Scan Cycle

Note: 1 Scan cycle time = 0.25s for the non-bleeding period and 1s for the bleeding time

Over Voltage Permanent Fail(OVPF) Protection					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**units/step**
OVPF Threshold Range		12bits programmable (0-5V)			V
OVPF Release Value		12bits programmable (0-5V)			V
OVPF Delay Time			8		Scan Cycle
OVPF Release Time (same as OVPF delay time)			8		Scan Cycle

Note: 1 Scan cycle time = 0.25s for the non-bleeding period and 1s for the bleeding time

Internal Thermal Protection (OT & UT)					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit/Step**
OT Detection Threshold value		User Programmable			1°C /2.1mV
OT Detection release Range		User Programmable			1°C /2.1mV
OT Delay Time (2-bit setup)		2		8	Scan Cycle
OT Release Time (same as OT delay time)		2		8	Scan Cycle
UT Detection Threshold Value		User Programmable			V
UT Detection Release Value		User Programmable			V
UT Delay Time (2-bit setup)		2		8	Scan Cycle
UT Release Time (same as UT delay time)		2		8	Scan Cycle

Note: 1 Scan cycle time = 0.25s for the non-bleeding period and 1s for the bleeding time

External Thermal Protection (OT & UT)					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit/Step**
OT Detection Threshold value		User Programmable			***(Note1)***
OT Detection release Range		User Programmable			***(Note1)***
OT Delay Time (2-bit setup)		2		8	Scan Cycle
OT Release Time (same as OT delay time)		2		8	Scan Cycle
UT Detection Threshold Value		User Programmable			V
UT Detection Release Value		User Programmable			V
UT Delay Time (2-bit setup)		2		8	Scan Cycle
UT Release Time (same as UT delay time)		2		8	Scan Cycle

Note1: Depends on external temperature sensor characteristics, refer to 'External Temperature Sensor'.
1 Scan cycle time = 0.25s for the non-bleeding period and 1s for the bleeding time

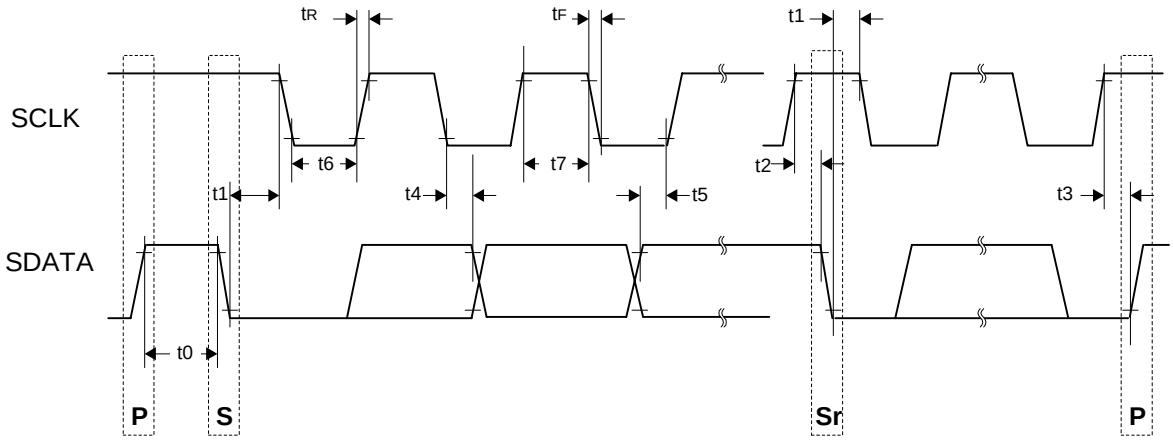
Unbalance Protection (UB)					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit/Step**
UB Detection Threshold value		User Programmable			***(Note1)***
UB Delay Time (2-bit setup)		2		8	Scan Cycle
UB Release Time (same as UB delay time)		2		8	Scan Cycle

Note: 1 Scan cycle time = 0.25s for the non-bleeding period and 1s for the bleeding time

Power MOSFET Driver Circuit					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
CHG on, sink current (constant current source),			10		uA
CHG off, no sink current (high impedance)			0		uA
DSG High Level		9.45	10.5	11.55	V
DSG Low Level		0		0.5	V
Rise Time			TBD		
Fall Time			TBD		

AC TIMING

SMBUS Bus Timing



Symbol	Parameter	Limits		*Units*	Note
		Min	Max		
FSMB	SMBUS Bus Operating Frequency	10	250	KHz	
t0	Bus free time between Stop and Start condition	4.7	-	µs	
t1	Hold time after (Repeated) Start condition. After this period, the first clock is generated	4.0	-	µs	
t2	Repeated Start condition set up time	4.7	--	µs	
t3	Stop Condition setup time	4.0	-	µs	
t4	Data hold time	150	-	ns	
t5	Data setup time	250	-	ns	
TIMOUT		25	35	ms	See **Note 1**
t6	Clock low period	4.7	-	µs	
t7	Clock high period	4.0	50	µs	See **Note 2**
TLOW:SEXT	Cumulative clock low extend time (slave device)	-	25	ms	See **Note 3**
TLOW:MEXT	Cumulative clock low extend time (master device)	-	10	ms	See **Note 4**
tF	Clock/Data Fall time	-	300	ns	See **Note 5**
tR	Clock/Data Rise Time	-	1000	ns	See **Note 5**

Note 1: A device will timeout when any clock low duration exceeds this value
Note 2: t5 Max provides a simple guaranteed method for devices to detect bus idle conditions.
Note 3: TLOW:SEXT is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to stop. If a slave device exceeds this time, it is expected to release both its clock and data lines and reset itself.
Note 4: TLOW:MEXT is the cumulative time a master device is allowed to extend its clock cycles within one byte of a message as defined from start-to-ack, ack-to-ack, or ack-to-stop.
Note 5: Rise and Fall times are measured between 10% to 90% of the signal amplitude.

FUNCTIONAL DESCRIPTION

OZ8940 Power-Up Sequence

Fig.1 shows the OZ8940 power up sequence. When power supply is applied and VCC>9V, the 10V LDO and 3.3V LDO starts first. When Vldo3.3>2.4V, the power on reset block releases a Power-On-Reset (POR) signal to enable the 512KHz oscillator and initializes the digital section. When Power and clock are ready, the digital circuits will read EEPROM data, and then go to different working state based on the ***auto_scan_start*** setting.

In assembly state, the protection board of OZ8940 will be connected to the battery cells ,it is necessary that the ***auto_scan_start*** =0 (1 bit in EEPROM register auto_scan_start ***[17h]***) will be set first so that OZ8940 does not do ADC scan to prevent erroroneous operation.

After battery assembly and OZ8940 power up, ***auto_scan_start*** =1 needs to be set and OZ8940 will directly go to the normal working state.

When Vcc is lower than 9V, the OZ8940 is in power off state. All LDOs, V3.3 and V10 are disabled and all MOSFETs are disabled.

Reset Generation (implemented in reset_ctrl)
In OZ8940, there are 2 system reset sources: one is power on reset when V3.3>2.4V; the other is generated when ***sleep_support*** and ***sleep_nsupport*** bits are not complementary to each other set by MCU or software.

OZ8940 Power Up Sequence Flowchart

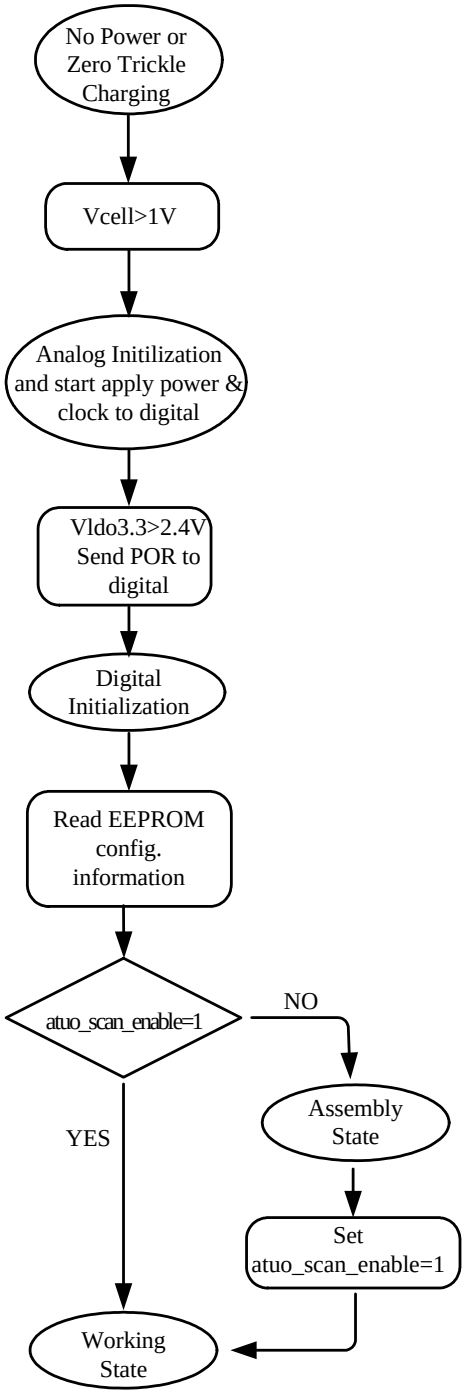


Fig. 1 OZ8940 Power Up

Measurements

OZ8940's multi-channel ADC (as shown in Fig. 2) measures up to 12 cell voltages, internal temperature and external temperature based on cyclic scan and time slot method. It will periodically measure all these values by predefined scan rate. During one measurement period, voltage and other entities will be measured one by one in different time slot.

1. ADC Channel Description

a. Lion-ion Cell Voltage Channel (6~12 channels)

These channels are designed for cell voltage measurement.
Resolution: 12bits (signed)
Input Voltage Range: 0.45V~5.0V
Slope calibration can be implemented in MCU application for better accuracy.

b. Internal Temperature (1 channel)

This channel is designed for internal temperature sensor.
Resolution: 12bits (signed)
Input Voltage Range: 0.1V~2.5V
Slope calibration can be implemented in MCU application for better accuracy.

c. GPIO Channel (2 channel)

GPIO1 and GPIO2 can be configured as external temperature sensor (please refer to the external thermal sensor section) or other analog input in MCU application, for detailed configuration information please refer to EEPROM register ***GPIO ctrl [16h]***.
GPIO1, GPIO2 can be configure to the external thermal sensor
Accuracy: 12bits (signed)
Input Voltage Range: 0.1V~2.5V
Slope calibration can be implemented in MCU application for better accuracy.
GPIO1, GPIO2 can be configured to other analog input or digital I/O.

2. ADC Time Slot

- Maximum number of the adc channel is 15 (6~12 cell channels + 1 internal temperature + 2 possible external temperature channels)

ADC Channel Time

The ADC time as following: The adc clock is 256KHz, the longest scan period = (12bit ADC time) * 15 =4164*15/256K=62460/256K=238.27ms. The ADC scan cycle is in 0.25 second.

Internal Bleeding

OZ8940 has embedded O2micro "Balance on Demand (BOD)" technology and Bleeding occurs:

- Battery pack is in charge state (current larger than charge current threshold) or in idle state (current smaller than charge current threshold and larger than discharge current threshold)
- The highest cell voltage exceeds the ***Bleeding Start*** voltage and the start bleeding voltage point is programmable (***BLD Threshold:*** 12 Bits in EEPROM registers ***[2dh]***),
- The cell voltages' difference exceeds the ***Bleeding Accuracy*** and the Balance accuracy is 9.76mV~39mV programmable (***Bleeding Accuracy:*** 3 Bits in EEPROM register ***[17h]***).
- No error event except OV, like OT, UT, UV, UB, OC0, OC, SC. If any error event happens, bleeding stops right away.

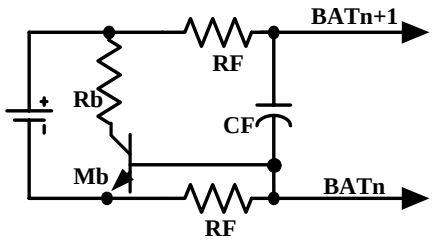


Fig.2 External Bleeding Diagram

This function can also support external bleeding by using some extra components (Fig.2).

Bleeding Control

(1) During in the bleeding state, the scan rate is 1s (0.25s for adc scan, 0.75s for cell bleeding); during in the cell scan period, any bleeding is stopped; after every scan, do the maximum cell bleeding if it meets the bleeding condition (the maximum cell voltage > bleeding threshold, and the difference between max. cell and min. cell > bleeding_accuracy), while don't care if it has OV or not, and don't care if it is in charge state or in idle state.
(2) When OT, UT, SC, OC, UB, UV FET disable or in_discharge occurs, any bleeding is stopped.
(3) During in the non-bleeding state, the scan rate is 0.25s.

Battery Protection

OZ8940 includes a digital Battery Protection Engine (BPE), the BPE constantly monitors data from the ADC and other circuits described below. If a protection error condition is detected and persists, the BPE will force the charge and/or discharge MOSFET off.
Note: The following description for battery protection is based on ***fet_control_sel* = 0** in reg. 19h, for ***fet_control_sel* = 1**, please refer to **the MOSFET Control Matrix.**

Over-current (OC)

OZ8940 includes an independent hardware over-current detector that monitors the voltage across the sense resistor to detect over-current in either charge or discharge. There are 1 level for charge OC (COC) and 2 level for the discharge OC (DOC0 and DOC1). If the over-current condition continues for a programmable delay, the protection circuit will turn off the charge and discharge MOSFETs. The charge and discharge over-current thresholds are set in protection register and EEPROM.
In sleep mode, OC detection is not available, only when sleep wakeup timer expired or wakeup by I2C access, or charging /discharging or SC event happened, the OZ8940 will return to full power mode right away, then OC detection is available.
The over-current delay allows the system to momentarily accept a high current condition. This delay time can be programmed

OC Value	COC	5bits EEPROM (map to reg.) Control: Start: 10mV; Stop:105mV; Step:5mV
	DOC0	6bits EEPROM (map to reg.) Control: Start: 30mV; Stop:285mV; Step: 5mV
	DOC1	6bits EEPROM (map to reg.) Control:Start:50mV; Stop:620mV; Step:10mV
Hyst. Value	COC	N/A
	DOC0	10mV
	DOC1	20mV
Delay Time	COC	3Bits EEPROM (map to reg.) control: "000": 2ms "001": 4ms "010": 8ms "011": 16ms "100": 64ms "101": 128ms "110": 256ms "111": 512ms
	DOC0	4Bits EEPROM (map to reg.) control: "0000": 2ms "0001": 4ms "0010": 8ms "0011": 16ms "0100": 32ms "0101": 64ms "0110": 96ms "0111": 128ms "1000": 256ms "1001": 512ms "1010": 768ms "1011": 1s "1100": 2s "1101": 4s "1110": 8s "1111": 16s
	DOC1	4Bits EEPROM (map to reg.) control: "0000": 32us "0001": 64us "0010": 128us "0011": 256us "0100": 512us "0101": 1ms "0110": 2ms "0111": 4ms "1000": 8ms "1001": 16ms "1010": 32ms "1011": 48ms "1100": 64ms "1101": 96ms "1110": 128ms "1111": 256ms
Release	COC	2 bits EEPROM (map to reg.) Control: 00:1S; 01:2S; 10:4S; 11:8S
	DOC0	2 bits control EEPROm (map to reg.): 00: external release; 01: 1S; 10: 2S; 11; 4S
	DOC1	1 bit control: 0: external release; 1: 1 min. release

Short circuit (SC)

Short-circuit detection circuit independently sense the PACK- voltage when discharge MOSFET is on. When short-circuit condition is detected, OZ8940 will turn off charge and discharge MOSFETs. Short-circuit threshold is fixed and can't adjusted, but its delay time is programmable

SC threshold	1.0V+/- 300mV
Hysteresis Value	N/A
Delay Time	2 bits EEPROM (map to reg.) Configure: "00": 0, immediately (nature delay) "01": 128us "10": 512us "11": 1ms
Release	1 bit control: 0: external release; 1: 1 min. release

Even in sleep mode, the SC detector still alive. When short-circuit condition happened and detected in sleep mode, OZ8940 will OFF charge/discharge FETs and turn to full power working mode.

Over-voltage (OV)

The protection engine performs over-voltage detection by comparing 12 bits values from the ADC with an OV threshold, which is programmable. The threshold is setup in EEPROM. When over-voltage condition is detected, OZ8940 will turn off the charge FET after a delay time. This delay time is programmed in EEPROM.

In sleep mode, OV detection is not available, only when sleep wakeup timer expired or wakeup by I2C access, or charging /discharging or SC event, the OZ8940 will return to full power mode, then OV detection is available.

OV Value	12Bits EEPROM programmable
OV Delay Time	2Bits EEPROM (map to reg.) Control:1.2. 4. 8 scan cycles
Release Value	12Bits EEPROM programmable
Release Delay Time	Same as OV delay time

Note: 1 Scan cycle time = 0.25s for the non-bleeding period and 1s for the bleeding time

Under-voltage (UV)

Under-voltage detection operates in the same way as over-voltage detection. Its threshold also can be programmed. The threshold is setup in EEPROM. Under-voltage protection has the same delay time as the over-voltage protection.

In sleep mode, UV detection is not available, only when sleep wakeup timer expired or wakeup by I2C access, or charging /discharging or SC event, the OZ8940 will return to full power mode, then UV detection is available.

UV Value	12Bits EEPROM programmable
UV Delay Time	2 Bits EEPROM (map to reg.) Control:1, 2, 4, 8 scan cycles (Share with OV)
Release Value	12Bits EEPROM programmable
Release Delay Time	Same as UV delay time

Note: 1 Scan cycle time = 0.25s for the non-bleeding period and 1s for the bleeding time

Cells voltage unbalance (UB)

When cell to cell voltage difference is large compared to the set value (12 bits EEPROM configuration) for longer than delay time (set as 2 bits of EEPROM configuration), OZ8940 will turn off the charge and discharge MOSFET. This protection can act as the cell voltage sense wire disconnection detection function. When one or more cell's sense wire disconnection is detected, the sensed cell's voltage compared to any other adjoining cell is larger than 1.2V while it's own cell voltage is higher than 2.2V, this characteristic can be used as the wire disconnection detection.

In sleep mode, UB detection is not available, only when sleep wakeup timer expires or wakeup by I2C access takes place, or charging /discharging or SC event, the OZ8940 will return to full power mode, then UB detection is available.

UB value	12Bits EEPROM programmable
UB delay	2 Bits EEPROM (map to reg.) Control: 2, 4, 6, 8 scan cycles
Release Value	12 Bits EEPROM programmable
Release Delay Time	Same as UB delay

Note: 1 Scan cycle time = 0.25s for the non-bleeding period and 1s for the bleeding time

Thermal Protection (OT & UT)

Thermal protection is performed based on inputs from both the internal temperature sensor and the optional external temperature sensors. Thermal information may be used to temporarily interrupt the charge cycle, or to disable discharge; OZ8940 provides both low temperature and high temperature protection.

In sleep mode, OT/UT detection is not available, only when sleep wakeup timer expired or wakeup by I2C access, or charging /discharging or SC event, the OZ8940 will return to full power mode, then OT/UT detection is available.

OT Value	External: 12Bits EEPROM Internal: 12Bits EEPROM
OT Delay Time	2Bits EEPROM (map to reg.) control: 2, 4, 6, 8 scan cycles
Release Value	External: 12Bits EEPROM Internal: 12Bits EEPROM
Release Delay Time	Same as OT delay time

UT Value	Charge	External: 12Bits EEPROM / Internal: 12Bits EEPROM
	Discharge	N/A
UT Delay Time		2Bits EEPROM (map to reg.) control: 2, 4, 6, 8 scan cycles (Share with OT)
Release Value	Charge	External: 12Bits EEPROM Internal: 12Bits EEPROM
	Discharge	N/A
Release Delay Time		Same as UT delay time

Note: 1 Scan cycle time = 0.25s for the non-bleeding period and 1s for the bleeding time

Over Voltage Permanent Failure (OVPF)

In case the OV protection fails, such as when the charge control mosfet is broken, OZ8940 provides the secondary protection PF function, there are 12Bits EEPROM for the OVPF threshold voltage and 12Bits EEPROM for the release voltage, when the cell voltage exceeds the threshold voltage and after a delay of 8 scan times, the OVPF event occurs and OZ8940 will send out the PF signal to blow the fuse, only when the cell voltage is less than the PF release voltage and delay 8 scan times, the PF signal can be released.

In OVPF, the discharge MOSFET and charge MOSFET are kept on previous status, and OZ8940 is still in full power mode when OVPF occurs, and scan rate is 0.25S.

Power Mode

To save power, OZ8940 works in different power modes according to the system status. There are 2 power modes as shown below:

Full Power Mode: < 500µA
Sleep Mode: < 30uA

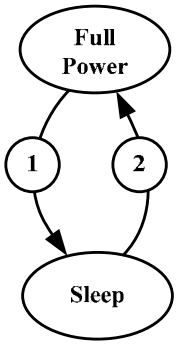


Fig. 4 OZ8940 Power Mode Diagram

Detail description for power mode transition

State Description (Fig. 4)

State	Description
Full Power	Voltage, temp. scan Safety protection check V3.3 (can supply up to 30mA) and V10 (can supply up to 10mA) power supply enabled OCP,SCP current detector and wakeup integrator block enabled Wake-up timer disabled
Sleep	Stop voltage and temp scan Stop safety protection check except for SC event detection based on SCS pin Backup V3.3 (can only supply 100uA) and V10 (can supply up to 10mA) supply enabled Wake-up integrator for current detector, Wakeup timer enabled SC detection based on SCS pin enabled

Transition Description

Transition	Initial State	Condition	Final State
1	Full Power	➢ No charge/discharge and No OV, OT, UT, OC, SC, event for 4 consecutive scan times *Note: OZ8940 can enter into sleep mode in UV and UB event.* ➢ No bleeding event ➢ SMBUS is not active	Sleep
2	Sleep	➢ sleep timer expired ➢ SC event occurs ➢ SMBUS activity ➢ charge/discharge current (detected by wake-up integrator)	Full Power

Notes

(1) The wake-up integrator is always enabled in sleep mode. It monitors charge/discharge current, so that in_charge, in_discharge or idle state can be identified.

(2) Once any cell is in bleeding (i.e. bleeding condition is met), OZ8940 changes the scan rate from 0.25s to 1s, i.e. 0.25s for ADC scan, and 0.75s for bleeding.

(3) If no protection event (no OV, OT/UT, OC/SC) occurs and no bleeding in idle state (no charge and discharge) for four consecutive ADC scan cycles, OZ8940 will enter sleep mode. SC (Short-circuit) event, wake-up integrator detect charge/discharge current, SMBus activity or wakeup timer (1 or 4 Minutes) expiry will wake up OZ8940 from sleep mode to full power mode. After wakeup, the 12h~1fh EEPROM data will be automatically mapped again into the corresponding operation registers to improve reliability.

MOSFET Control Matrix

If **fet_control_sel=0 in reg. 19h**, please refer the FET control as follows:

Events	*ALERTR and* Status	MOSFET State
1.No protection event		DSG and CHG on
2.Normal to short circuit(SC) event	sc_alert_flag=1	DSG and CHG off
3.Normal to over current(OC) event	oc_alert_flag=1	DSG and CHG off
4.Normal to over temperature(OT) event	ot_alert_flag=1	DSG and CHG off
5.Normal to unbalance(UB) event	ub_alert_flag=1	DSG and CHG off
6.Normal to under temperature(UT) only event	ut_alert_flag=1	DSG on and CHG off
7.Normal to under temperature(UT) and in discharge event	ut_alert_flag=1	DSG and CHG on
8.Normal to under voltage (UV) and no charge event	uv_alert_flag=1	DSG off and CHG on
9.Normal to under voltage (UV) and in charge event	uv_alert_flag=1	DSG and CHG on
10.Normal to under voltage (UV) and under temperature (UT) event	uv_alert_flag=1 & ut_alert_flag=1	DSG and CHG off
11.Normal to over voltage (OV) and no discharge event	ov_alert_flag=1	DSG on and CHG off
12.Normal to over voltage (OV) and in discharge event	ov_alert_flag=1	DSG and CHG on
13.Normal to over voltage (OV) and under voltage(UV) event	ov_alert_flag=1& uv_alert_flag=1	DSG and CHG off
14. Over Voltage PF(OVPF) event	ovpf_alert_flag=1	DSG and CHG keep on previous status

If **fet_control_sel = 1 in reg.19h**, please refer to FET control as follows:

<table>
<tr><th>Events</th><th colspan="5">ALERTR and Status</th><th>MOSFET State</th></tr>
<tr><td>1 No protection event</td><td colspan="5"></td><td>DSG and CHG on</td></tr>
<tr><td rowspan="4">2.Normal to unbalance(UB) | over temperature(OT) event</td><td>UB</td><td>OT</td><td colspan="3">ALERTR</td><td rowspan="4">DSG and CHG off</td></tr>
<tr><td>0</td><td>1</td><td colspan="3">ot_alert_flag=1</td></tr>
<tr><td>1</td><td>0</td><td colspan="3">ub_alert_flag=1</td></tr>
<tr><td>1</td><td>1</td><td colspan="3">ot_alert_flag=1& ub_alert_flag=1</td></tr>
<tr><td>3.Normal to charge over current(COC) & no under voltage(!UV) event</td><td colspan="5">oc_alert_flag=1</td><td>DSG on and CHG off</td></tr>
<tr><td>4.Normal to charge over current(COC) & under voltage(UV) event</td><td colspan="5">oc_alert_flag=1& uv_alert_flag=1</td><td>DSG and CHG off</td></tr>
<tr><td>4.Normal to short circuit(SC) | discharge over current0 (DOC0) | discharge over current1(DOC1)&no over voltage(!OV) &no under temperature(!UT) event</td><td colspan="5">oc_alert_flag=1 | sc_alert_flag=1</td><td>DSG off and CHG on</td></tr>
<tr><td rowspan="4">5.Normal to short circuit(SC) | discharge over current0 (DOC0) | discharge over current1(DOC1)&over voltage(OV) under temperature(UT) event</td><td>OV</td><td>UT</td><td colspan="2">SC,DOC0, DOC1</td><td>ALERTR</td><td rowspan="4">DSG and CHG off</td></tr>
<tr><td>0</td><td>1</td><td colspan="2">1</td><td>oc_alert_flag=1 | sc_alert_flag=1 & ut_alert_flag=1</td></tr>
<tr><td>1</td><td>0</td><td colspan="2">1</td><td>oc_alert_flag=1 | sc_alert_flag=1 & ov_alert_flag=1</td></tr>
<tr><td>1</td><td>1</td><td colspan="2">1</td><td>oc_alert_flag=1 | sc_alert_flag=1 & ov_alert_flag=1 & ut_alert_flag=1</td></tr>
<tr><td rowspan="2">6. Normal to no over voltage(!OV) & no under voltage(!UV) & under temperature(UT) event</td><td colspan="2">No discharge</td><td colspan="3">ut_alert_flag=1</td><td>DSG on and CHG off</td></tr>
<tr><td colspan="2">discharge</td><td colspan="3">ut_alert_flag=1</td><td>DSG and CHG on</td></tr>
<tr><td rowspan="2">7.Normal to no over voltage(!OV) & under voltage(UV) & no under temperature(!UT)</td><td colspan="2">No charge</td><td colspan="3">uv_alert_flag=1</td><td>DSG off and CHG on</td></tr>
<tr><td colspan="2">charge</td><td colspan="3">uv_alert_flag=1</td><td>DSG and CHG on</td></tr>
<tr><td>8.Normal to no over voltage(!OV) & under voltage(UV) & under temperature(UT) event</td><td colspan="5">uv_alert_flag=1& ut_alert_flag=1</td><td>DSG and CHG off</td></tr>
</table>

Events	*ALERTR and* Status			MOSFET State
9 Normal to over voltage(OV) & no under voltage(!UV) & (under temperature(UT) or no under temperature (!UT) event	Charge/ Discharge	OV	ALERTR	
	No discharge	1	ov_alert_flag=1	DSG on and CHG off
	discharge	1	ov_alert_flag=1	DSG and CHG on
10.Normal to over voltage (OV) & under voltage(UV) & (under temperature(UT) or no under temperature(!UT) event	ov_alert_flag=1 & uv_alert_flag=1			DSG and CHG off
11 Over Voltage PF	ovpf_alert_flag=1			DSG and CHG keep on previous status

Alert (interrupt) Operation

If OZ8940 co-work with external MCU, it can output negative pulse interrupt signal to inform MCU what happened. The interrupt signal will be generated when one ADC data is finished, or SC, OC, OV, UV, OT, UT, UB, or OVPF happened.

Internal Temperature Sensor

OZ8940 takes advantage of silicon device physics and circuit design technology for the internal temperature sensor. The internal temperature sensor generates a voltage level which is proportional to the temperature. As Fig.5 showing below, with a temperature increase of 1°C, internal temperature sensor output voltage will increase 2.0976mV. The offset can be get from the 12Bit EEPROM which measured in the ATE test. So, if at T0, ADC reading out VT0, the characteristic curve function can be get:

VTS (mV)=2.0976*T+(VT0 – 2.0976*T0)

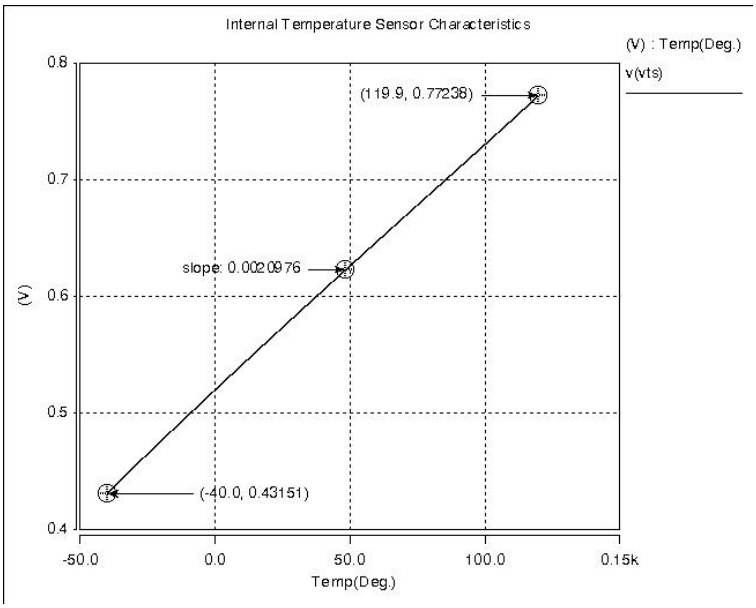


Fig. 5 Internal Temperature Sensor Curve

External Temperature Sensor

OZ8940 provides 3 GPIOs for external temperature detection, the application circuitry is shown in Fig.6. We recommend using 103 NTC type thermistor.
103 NTC Thermistor RT characteristics are shown in Fig. 7. The sensed voltage Vt characteristics are shown in Fig. 8

For Example: Vt2=3.3V * RT2 / (RB2 + RT2)

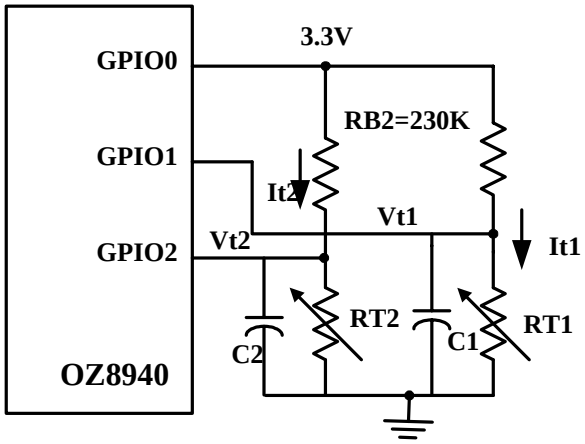


Fig.6 External Temperature Sensor Application

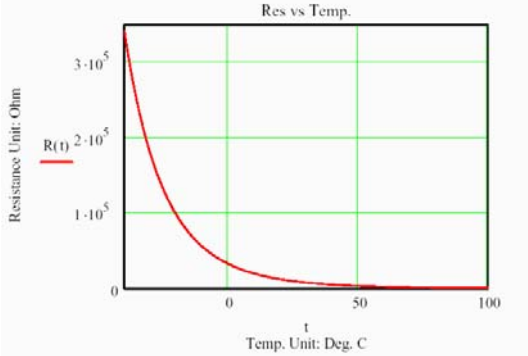


Fig.7 Thermistor RT characteristics

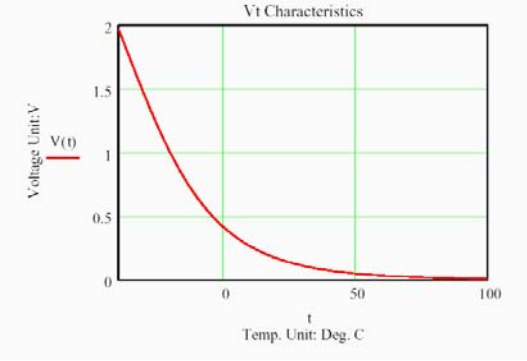


Fig.8 The sensed voltage Vt characteristics

Power MOSFET Driver Control

Smart MOSFET driver is designed for N-type MOSFET controlled charge, and discharge. The driver also supports parallel and series charge discharge loop.
The charge and discharge MOSFET are controlled through protection register, subject to override by the Battery Protection Engine (BPE). OZ8940 also provides a pin (EFETC) for external MOSFET control signal input or internal MOSFET control signal outputit makes the MOSFET control very flexible. The discharge (DSG) MOSFET gate-to-source voltage is clamped to 10V (typical) when MOSFET is in ON state; CHG pin internally embedded a 10uA current sink for P-type charge driver or level shift for N-type charge MOSFET driver in ON state. When charge MOSFET in OFF state, this 10uA current source is disable and CHG pin is

Note 2Bits in EEPROM configure the PIN's function: charge & discharge FET off (input), charge FET off (input), discharge FET off (input) and discharge FET off (output)

in high impedance state. The charge MOSFET gate-to-source voltage is decided by external divider resistor and the pack voltage. MOSFET driver circuits are shown in Fig.9 and Fig.10.

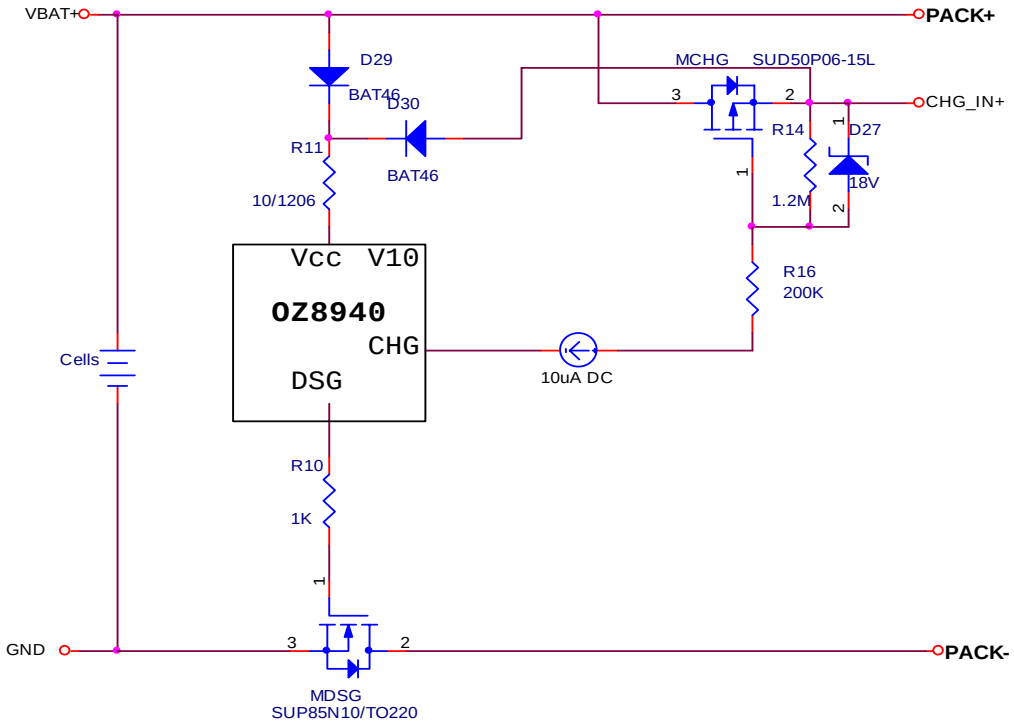


Fig.9 MOSFET drive circuit with P-type charge MOSFET

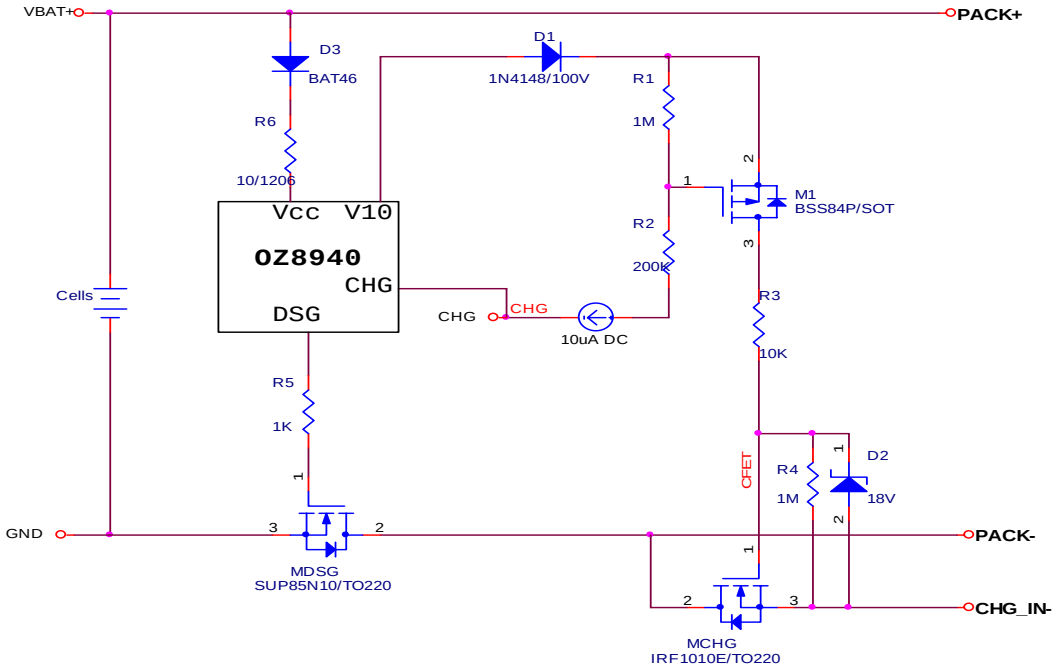


Fig.10 MOSFET drive circuit with N-type charge MOSFET

Serial Communication Bus

OZ8940 supports SMBus communication interface. The SMBUS master can access OZ8940's registers with SMBUS protocol. In this condition, OZ8940 is working as an SMBUS slave device.

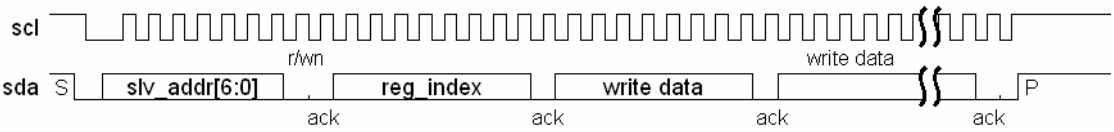
2-wire SMBUS Bus
In OZ8940, the 3-bit SMBus address config specifies the 8-bit SMBus address as 8'h60 + 2*N.

The following slave address byte indicates the SMBus device address is 8-bit 60h (Bit7~bit1 is the device address, the bit0 selects SMBus read or write).

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	1	1	0	0	0	0	r/wn

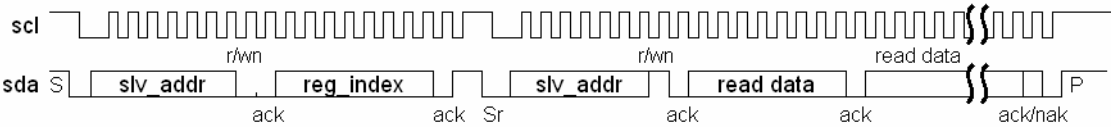
Write Data Access
In write data access, there are some bytes transmitted from master to slave as following:
slave address byte: slv_addr[6:0], r/wn;
register index byte: reg_index[7:0];
write data bytes: write data.

slv_addr[6:0] is the SMBus address to select an SMBus device.
r/wn is the read/write bit. If "1", selects read access; if "0", selects write access. Here for write data access, it is "0".
reg_index[7:0] is used to select register index.
write data are the data for write data access.



The above diagram shows the timing of writing data access. At first is slave_addr[6:0] to select one slave node; the next byte is reg_index to define the register index; the next bytes are some bytes data for write.
The first write address is reg_index. Once one byte data is written successful, the internal register address will be +1 automatically so that the next bytes data will be written in continuous address registers.

Read Data Access
For the read data access, there are two cases: one is with setting reg_index; the other is without setting reg_index.
In read data access with setting reg_index, there are some bytes transmitted as following:
slave address byte from master to slave: slv_addr[6:0], r/wn;
register index byte from master to slave: reg_index[7:0];
read data bytes from slave to master: read data.



The above diagram shows the read data access with setting reg_index. First is the slave address to select one slave device; then is reg_index to select the register index; then is repeated start; then is slave address again, next are some bytes read data from slave device.

Timeout
Consideration the reliability, if SCL or SDA line is kept low for more than 25ms, the SMBus engine will be reset and guarantee not to drive the SCL or SDA to low by OZ8940.

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Wake-up Integrator and charge/discharge detector

The wake-up integrator is used to detect small charge / discharge current and make decision that the system is in charge, or in discharge state.

For saving power, OZ8940 will enter into sleep mode if charge/discharge current less than the threshold for four consecutive ADC scan cycles and no safety events happen. In this case, the wakeup integrator is used to wakeup OZ8940 from sleep mode when charge/discharge current is detected. In the sleep mode, backup 3.3V power supply provides system power, internal 32KHz oscillator provides system clock, wakeup integrator monitors the charge/discharge current and SCS circuit provides short circuit protection. If the charge/discharge current is higher than the wakeup current threshold, the integrator wakes up the whole system. If SCS pin detects short circuit event, it will turn off discharge MOSFET immediately, then inform the OZ8940 to wakeup. Additionally, OZ8940 also provides wakeup timer and SMBUS bus activity wakeup mechanism.

The Wake-up charge and discharge current can be adjusted by setting ***chg/dsg_ integ_ctrl[1:0]*** in EEPROM register ***integrator control [18h]***.
Wake-up current can be estimated using the equation below.

$$(I_{\min} \times R_{\text{sens}}) \times F_{\text{osc32k}} \times T_{\text{integ}} = 2.0V$$

Here, $I_{\min}$ is the minimum charge/discharge current to wake up the system

R_{sens} is resistance of sense resistor,

F_{osc32k} is the output frequency of internal 32k clock which is between 21k and 37k.

T_{integ} is the integrating time for discharge or charge which can be programmed in EEPROM register ***integrator control [18h]***. The threshold voltage 2.0V is a fixed design value.

For example, $F_{\text{osc32k}} = 26K, R_{\text{sens}} = 2.5m\Omega, T_{\text{integ}} = 64mS$

Then we can get $I_{\min} = 2000/(2.5 \times 26 \times 64) = 0.48A$

In sleep mode, when discharge or charge current is higher than 0.48A, OZ8940 will wake up from sleep mode in about 64mS. Otherwise, OZ8940 will stay in sleep mode.

EEPROM AND OPERATION REGISTERS MAP

OZ8940 has two types of registers. One type is OZ8940's operation registers which addresses from 00h to 3fh; the other type is embedded EEPROM registers which addresses from 00h to 3fh. Software can directly access OZ8940's operation registers via SMBUS; and software can access the EEPROM registers indirectly by access the operation registers 08h~0bh.

EEPROM registers are used to store important battery pack, battery cell information and to configure the OZ8940 chip. Operation registers are used to store ADC instant data, OZ8940 status information, and some parameters to control OZ8940 state-machine, etc. When system is powered on, the data in EEPROM register 12h-1fh will be loaded into the Operation registers 12h-1fh respectively. Fig. 11 shows the configuration of EEPROM registers and Operation registers.

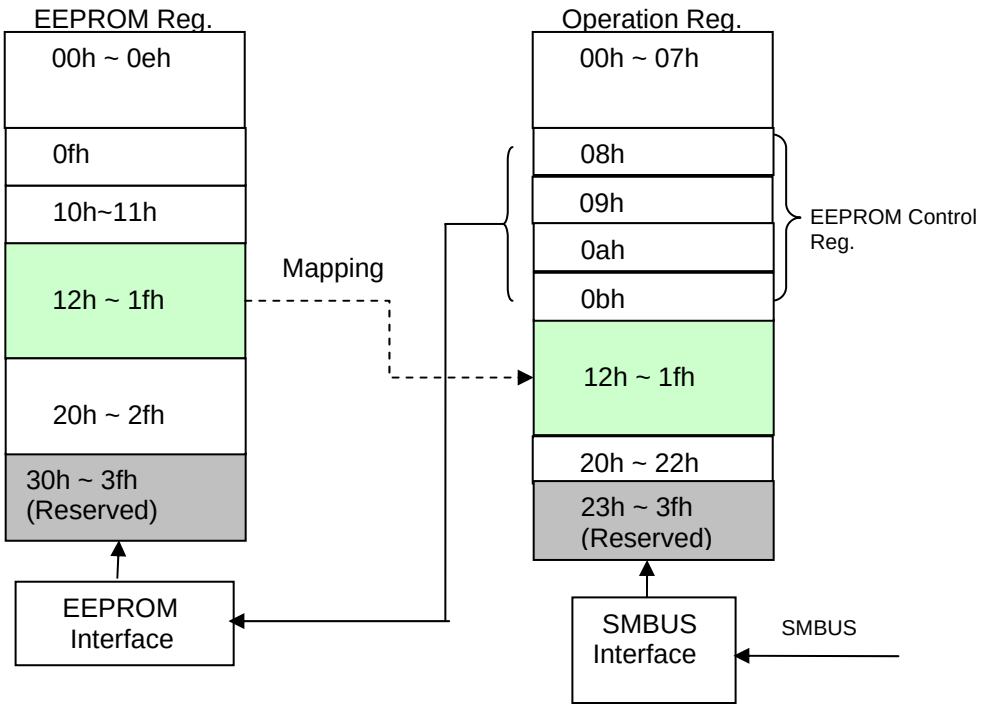


Fig.11 Configuration of EEPROM Register and Operation Register

OZ8940 Operation Registers

The EEPROM data from 12h to 1fh will be mapped into the operation registers from 12h to 1fh.

Reg. (hex)	Register Name	Bit Number							
		7	6	5	4	3	2	1	0
00	OZ8940Ver	chip_id[3:0]				chip_version[3:0]			
01		Reserved							
02	ADCDR1	adc_data[3:0]				adc_channel[3:0]			
03	ADCDR2	adc_data[11:4]							
04	MinDR1	cell_min_data[3:0]				cell_min_channel[3:0]			
05	MinDR2	cell_min_data[11:4]							
06	MaxDR1	cell_max_data[3:0]				cell_max_channel[3:0]			
07	MaxDR2	cell_max_data[11:4]							
08	EEHByte	Reserved				ee_data[11:8]			
09	EELByte	ee_data[7:0]							
0a	EEADDR	Reserved		ee_addr[5:0]					
0b	EECTRL	ee_busy	Reserved		ee_mode[1:0]		ee_op_code[2:0]		
0c	SYSSR1	chg_enable	dsg_enable	in_charge	in_discharge	ov_fet_disable	uv_fet_disable	ot_fet_disable	ut_fet_disable
0d	SYSSR2	ub_fet_disable	sc_fet_disable	coc_fet_disable	doc0_fet_disable	doc1_fet_disable	scp	cocp	docp0
0e	SYSSR3	docp1	in_bleeding	sleep_state	ref_enable	cd_enable	ocp_enable	scp_enable	ovpf
0f	ALERTR	adc_alert_flag	sc_alert_flag	oc_alert_flag	ov_alert_flag	uv_alert_flag	ot_alert_flag	ut_alert_flag	ub_alert_flag
10	WakeupFR	integ_wakeup_flag	sc_wakeup_flag	SMBUS_wakeup_flag	timer_wakeup_flag	ovpf_alert_flag	Reserved		
11~14		Reserved							
15	ATEctrl	ate_freeze	Reserved						
16	SYSconfig	gpio_ctrl[1:0]		SMBus_addr[2:0]			cell_number[2:0]		
17	MiscCtrl	auto_scan_start	sleep_time	ovpf_enable	Reserved	bleeding_accuracy[1:0]		efetc_mode[1:0]	
18	IntegratorCtrl	Reserved				chg_integ_ctrl[1:0]		dsg_integ_ctrl[1:0]	
19	COCctrl	fet_control_sel	coc_release[1:0]		coc_ctrl[4:0]				
1a	DOC0ctrl	doc0_release[1:0]		doc0_ctrl[5:0]					
1b	DOC01delay	doc0_delay[3:0]				doc1_delay[3:0]			
1c	DOC1ctrl	sc_release	doc1_release	doc1_ctrl[5:0]					
1d	COCSCdelay	Reserved			coc_delay[2:0]			sc_delay[1:0]	
1e	VTUBTimeout	user_freeze	ub_enable	ovuv_timeout[1:0]		otut_timeout[1:0]		ub_timeout[1:0]	
1f	FunctionCtrl	ee_enable	test_enable	Reserved				sleep_support	sleep_nsupport
20	OUVtimer	Reserved		ov_timer[2:0]			uv_timer[2:0]		
21	OUTtimer	Reserved		ot_timer[2:0]			ut_timer[2:0]		
22	UBtimer	Reserved					ub_timer[2:0]		
23~3f	Reserved	Reserved							

Detailed Operation Register Information

Register 00h – Chip ID & Revision Register (OZ8940Ver)

Bit #	Name	Description	R/W	Reset Value
7:4	chip_id[3:0]	This indicates the chip ID of OZ8940.	R	2h
3:0	chip_version[3:0]	This indicates the chip revision of OZ8940. "0" indicates A version, "1" indicates B version, "2" indicates C version,, and so on.	R	0h

Register 01h – Reserved Register

Register 02h & 03h – ADC Data Register (ADCDR1 & ADCDR2)

This two registers are used to save the ADC data for every channel, The adc_channel[3:0] is used to distinguish this data belong to which channel.

Bit #	Name (Reg.02h)	Description	R/W	Reset
7:4	adc_data[3:0]	the ADC data low byte	R	0h
3:0	adc_channel[3:0]	"0000": don't use; "0001" ~ "1100": indicates cell1 ~ cell12; "1101" : internal temperature chanel; "1110": gpio1 channel; "1111": gpio2 channel.	R	0h

Bit #	Name(Reg.03h)	Description	R/W	Reset
7:0	adc_data[11:4]	the ADC data high byte	R	0h

Register 04h & 05h – Min. Cell ADC Data Register (MinDR1 & MinDR2)

This two registers are used to save the minimum cell voltage ADC data.

Bit #	Name(Reg.04h)	Description	R/W	Reset
7:4	cell_min_data[3:0]	the ADC data low byte of the minimum cell voltage	R	0h
3:0	cell_min_channel[3:0]	"0000": don't use; "0001" ~ "1100": indicates cell1 ~ cell12; "1101"~"1111" : Reserved.	R	0h

Bit #	Name(Reg.05h)	Description	R/W	Reset
7:0	cell_min_data[11:4]	the ADC data high byte of the minimum cell voltage	R	0h

Register 06h & 07h – Max. Cell ADC Data Register (MaxDR1 & MaxDR2)

This two registers are used to save the maximum cell voltage ADC data.

Bit #	Name(Reg.06h)	Description	R/W	Reset
7:4	cell_max_data[3:0]	the ADC data low byte of the maximum cell voltage	R	0h
3:0	cell_max_channel[3:0]	"0000": don't use; "0001" ~ "1100": indicates cell1 ~ cell12; "1101"~"1111" : Reserved.	R	0h

Bit #	Name(Reg.07h)	Description	R/W	Reset
7:0	cell_max_data[11:4]	the ADC data high byte of the maximum cell voltage	R	00h

Register 08h & 09h – EEPROM Data Register (EEHByte & EELByte)

The EEPROM word is 16bits, but for our application, the EEPROM word is organized as 12bits, so the high byte is only 4bits. If you want to write one byte in EEPROM, ee_data[11:8] (Reg. 08h) don't care.

Bit #	Name(Reg.08h)	Description	R/W	default
7:4	Reserved	Reserved (unimplemented)		
3:0	ee_data[11:8]	high byte for eeprom	RW	0h

Bit #	Name(Reg.09h)	Description	R/W	default
7:0	ee_data[7:0]	low byte for eeprom	RW	00h

Register 0ah – EEPROM Address Register (EEADDR)

Bit #	Name	Description	R/W	default
7:6	Reserved	Reserved (unimplemented)		
5:0	ee_addr	used to access the EEPROM from 00h ~ 3fh.	RW	0h

Register 0bh – EEPROM Control Register (EECTRL)

Bit #	Name	Description	R/W	Default
7	ee_busy	This bit is high indicating the eeprom is being accessed. After the access, it is low. Only when this bit is low, the software can start another eeprom's access.	R	0h
6:5	Reserved	Reserved (unimplemented)		
4:3	ee_mode	These bits are used to select eeprom mode. If set to "11", select eeprom mode; if set to other values, select non-eeprom mode. In eeprom mode, software can access the eeprom and the safety scan is disabled. In non-eeprom mode, software can not access the eeprom.	RW	0h

Bit #	Name	Description	R/W	Default
2:0	ee_op_code	These bits are used to specify the eeprom's accesses as following: ee_op_code[2:0] / Access 3'b000 / no access 3'b001 / Word erase 3'b010 / Word write 3'b011 / Block erase 3'b100 / Block Write for EE Test 3'b101 / Normal read 3'b110 / do mapping 3'b111 / Reserved	RW	0h

Register 0ch – System Status Register1 (SYSSR1)

Bit #	Name	Description	R/W	default
7	chg_enable	active high to enable charge MOSFET	R	0
6	dsg_enable	active high to enable discharge MOSFET	R	0
5	in_charge	active high to indicate system is in charge state	R	0
4	in_discharge	active high to indicate system is in discharge state	R	0
3	ov_fet_disable	active high to indicate over voltage has been confirmed, the reset value after reset is "1" for more safety, because the charge MOSFET will be switched off when this bit is set to 1.	R	1
2	uv_fet_disable	active high to indicate under voltage has been confirmed, the reset value after reset is "1" for more safety, because the discharge MOSFET will be switched off when this bit is set to 1.	R	1
1	ot_fet_disable	active high to indicate over temperature has been confirmed	R	0
0	ut_fet_disable	active high to indicate under temperature has been confirmed	R	0

Register 0dh – System Status Register2 (SYSSR2)

Bit #	Name	Description	R/W	default
7	ub_fet_disable	active high to indicate unbalance has been confirmed	R	0
6	sc_fet_disable	active high to indicate short circuit has been confirmed	R	0
5	coc_fet_disable	active high to indicate charge over current has been confirmed	R	0
4	doc0_fet_disable	active high to indicate discharge level0 over current has been confirmed	R	0
3	doc1_fet_disable	active high to indicate discharge level1 over current has been confirmed	R	0
2	scp	short circuit signal from analog block	R	0
1	cocp	charge over current signal from analog	R	0
0	docp0	discharge over current level0 signal from analog	R	0

Register 0eh – System Status Register3 (SYSSR3)

Bit #	Name	Description	R/W	default
7	docp1	discharge over current level1 signal from analog	R	0
6	in_bleeding	active high to indicate bleeding condition is met (max cell voltage > bleeding threshold, and max cell voltage – min cell voltage > bleeding accuracy)	R	0
5	sleep_state	active high to indicate system is in sleep state	R	0
4	ref_enable	to observe ref_enable signal	R	0
3	cd_enable	to observe cd_enable signal	R	0

Bit #	Name	Description	R/W	default
2	ocp_enable	to observe ocp_enable signal	R	0
1	scp_enable	to observe scp_enable signal	R	0
0	ovpf	active high to indicate OV PF has been confirmed.	R	0

Register 0fh – Alert Flag Register (ALERTR)

Bit #	Name	Description	RWC	defult
7	adc_alert_flag	set by hardware when one adc data (including adc fft) is finished, and cleared by SMBUS writing one to this bit.	RC	0
6	sc_alert_flag	set by hardware when sc is confirmed, and cleared by SMBUS writing one to this bit.	RC	0
5	oc_alert_flag	set by hardware when oc is confirmed, and cleared by SMBUS writing one to this bit.	RC	0
4	ov_alert_flag	set by hardware when ov is confirmed, and cleared by SMBUS writing one to this bit.	RC	0
3	uv_alert_flag	set by hardware when uv is confirmed, and cleared by SMBUS writing one to this bit.	RC	0
2	ot_alert_flag	set by hardware when ot is confirmed, and cleared by SMBUS writing one to this bit.	RC	0
1	ut_alert_flag	set by hardware when ut is confirmed, and cleared by SMBUS writing one to this bit.	RC	0
0	ub_alert_flag	set by hardware when ub is confirmed, and cleared by SMBUS writing one to this bit.	RC	0

Note: *one low pulse unmasked interrupt signal will be generated when one adc data is finished, or SC, OC, OV, UV, OT, UT, UB or OVPF happened.*

Register 10h – Wakeup Event Flag Register (WakeupFR)

Bit #	Name	Description	R/C	default
7	integ_wakeup_flag	set by hardware when there is output from integrator in sleep state, and cleared by SMBUS writing one to this bit.	RC	0
6	scp_wakeup_flag	set by hardware when sc event occurs in sleep state, and cleared by SMBUS writing one to this bit.	RC	0
5	SMBUS_wakeup_flag	set by hardware when SMBUS access (slave address matched) occurs in sleep state, and cleared by SMBUS writing one to this bit.	RC	0
4	timer_wakeup_flag	set by hardware when the sleep timer (1 or 4 minutes) is expired, and cleared by SMBUS writing one to this bit.	RC	0
3	ovpf_alert_flag	set by hardware to indicate OV PF occurs ever, and cleared by SMBUS writing one to this bit.	RC	0
2:0	Reserved	Reserved (unimplemented)		

Register 11h~14h – Reserved

Register 15h – ATE Control Register (ATEctrl)

This register is mapped from EEPROM data 15h.

Bit #	Name	Description	R/W	Default
7	ate_freeze	active high to freeze the mapped ATE data in internal register 12h~15h and the ATE data in EEPROM register from 00h~15h. But block erase is always open to SMBUS via the EEPROM controller when the EEPROM is enabled by ee_enable=1. This bit can only be read via SMBUS. This bit can be written by mapping the corresponding EEPROM data.	R	0h
6:0	Reserved	Reserved (unimplemented)		

Register 16h – System Configuration Register (SYSconfig)

This register is mapped from EEPROM data 16h.

Bit #	Name	Description	R/W	Default
7:6	gpio_ctrl[1:0]	"00": no external temperature channel (gpio0, gpio1 and gpio2 are configured as digital input); "01': select gpio1 as external temperature channel (gpio0 is configured as digital output for outputting 3.3V to power the external thermal sensor circuit when scanning this channel, gpio1 is configured as analog pin, gpio2 is configured as digital input pin in normal work state); "10": select gpio2 as external temperature channel (gpio0 is configured as digital output for outputting 3.3V to power the external thermal sensor circuit when scanning this channel, gpio2 is configured as analog pin, gpio1 is configured as digital input pin in normal work state); "11": select gpio1 and gpio2 as external temperature channels (gpio0 is configured as digital output for outputting 3.3V to power the external thermal sensor circuit when scanning this channel, gpio1 and gpio2 are configured as analog pin in normal work state);	RW	0h
5:3	SMBus_addr[2:0]	Specify the 8-bit SMBus device address as 8'h60 + 2*N.	RW	0h
2:0	cell_number[2:0]	Specify the cell count in the battery pack as following: cell number: cell count in the battery pack 3'b000: Reserved, don't do scan 3'b001: 6 3'b010: 7 3'b011: 8 3'b100: 9 3'b101: 10 3'b110: 11 3'b111: 12	RW	0h

Register 17h – Misc Control Register (MiscCR)

This register is mapped from EEPROM data 17h.

Bit #	Name	Description	R/W	reset
7	auto_scan_start	This bit will be checked only after power on reset or internal reset and after EEPROM mapping. After the reset mapping, if cell_number is not "000" and auto_scan_start = 1, ADC scan will be started.	RW	0
6	sleep_time	'0': for 1 Minute; '1': for 4 Minutes.	RW	0
5	ovpf_enable	'0': disable OV PF output; '1': enable OV PF output to TCLK/ALERTN/OVPF pin	RW	0

<table>
<tr><th>Bit #</th><th>Name</th><th>Description</th><th>R/W</th><th>reset</th></tr>
<tr><td>4</td><td>Reserved</td><td>Reserved (unimplemented)</td><td></td><td></td></tr>
<tr><td>3:2</td><td>bleeding_accuracy[1:0]</td><td>Select bleeding accuracy as follows:
<table>
<tr><td>2 bits</td><td>Bleeding accuracy</td></tr>
<tr><td>2’b00</td><td>4*2.44 = 9.76mv</td></tr>
<tr><td>2’b01</td><td>8*2.44 = 19.5mv</td></tr>
<tr><td>2’b10</td><td>12*2.44 = 29.3mv</td></tr>
<tr><td>2’b11</td><td>16*2.44 = 39.0mv</td></tr>
</table>
The cell bleeding is be stopped if the max_voltage – min_voltage < bleeding accuracy.</td><td>RW</td><td>00</td></tr>
<tr><td>1:0</td><td>efetc_mode[1:0]</td><td>Select EFETC pin function as following:
<table>
<tr><td>code</td><td>EFETC pin function</td></tr>
<tr><td>00</td><td>If “1”, force charge FET OFF; if “0”, charge FET is decided by the internal logic.</td></tr>
<tr><td>01</td><td>if “1”, force discharge FET OFF; if “0”, discharge fet is decided by the internal logic.</td></tr>
<tr><td>10</td><td>If “1”, force charge FET and discharge FET OFF; if “0”, charge FET and discharge FET are decided by the internal logic.</td></tr>
<tr><td>11</td><td>output the internal discharge MOSFET control signal</td></tr>
</table></td><td>RW</td><td>0h</td></tr>
</table>

Register 18h – Integrator Control Register (IntegratorCtrl)

This register is mapped from EEPROM data 18h.

<table>
<tr><th>Bit #</th><th>Name</th><th>Description</th><th>R/W</th><th>Default</th></tr>
<tr><td>7:4</td><td>Reserved</td><td>Reserved (unimplemented)</td><td></td><td></td></tr>
<tr><td>3:2</td><td>chg_integ_ctrl[1:0]</td><td>Integration time for charge as following:
<table>
<tr><td>charge integrator control</td><td>Integration time</td></tr>
<tr><td>2’b00</td><td>32ms</td></tr>
<tr><td>2’b01</td><td>64ms</td></tr>
<tr><td>2’b10</td><td>128ms</td></tr>
<tr><td>2’b11</td><td>256ms</td></tr>
</table></td><td>RW</td><td>00</td></tr>
<tr><td>1:0</td><td>dsg_integ_ctrl[1:0]</td><td>Integration time for discharge as following:
<table>
<tr><td>Discharge integrator control</td><td>Integration time</td></tr>
<tr><td>2’b00</td><td>16ms</td></tr>
<tr><td>2’b01</td><td>32ms</td></tr>
<tr><td>2’b10</td><td>64ms</td></tr>
<tr><td>2’b11</td><td>128ms</td></tr>
</table></td><td>RW</td><td>00</td></tr>
</table>

Register 19h – COC Control Register (COCctrl)
This register is mapped from EEPROM data 19h.

Bit #	Name	Description	R/W	Reset
7	fet_control_sel	"0": switch off charge and dischare MOSFET when charge OC, discharge OC or/and SC occur, while don't care if in charge or in discharge state; "1": switch off charge MOSFET when COC occurs, while discharge MOSFET keeps on if no UV, no OT and no UB; switch off discharge MOSFET when DOC or/and SC occur, while charge MOSFET keeps on if no OV, no OT, no UT and no UB		
6:5	coc_release[1:0]	Control the charge OC release as following: 2-bit: charge OC release 00: 1s release. The charge OC will not be released until 1s time out. 01: 2s release. The charge OC will not be released until 2s time out. 10: 4s release. The charge OC will not be released until 4s time out. 11: 8s release. The charge OC will not be released until 8s time out.	RW	00

Bit4 – Bit0 COC_ctrl [bit4:bit0]: Configure the charge over current threshold.

Bit4 – Bit0	COC threshold	Bit4 – Bit0	COC threshold
00000 – 00101	Reserved	10000	60mV / Rs
00110	10mV / Rs	10001	65mV / Rs
00111	15mV / Rs	10010	70mV / Rs
01000	20mV / Rs	10011	75mV / Rs
01001	25mV / Rs	10100	80mV / Rs
01010	30mV / Rs	10101	85mV / Rs
01011	35mV / Rs	10110	90mV / Rs
01100	40mV / Rs	10111	95mV / Rs
01101	45mV / Rs	11000	100mV / Rs
01110	50mV / Rs	11001	105mV / Rs
01111	55mV / Rs	10010 – 11111	Reserved

Register 1ah – Discharge OC0 Control Register (DOC0ctrl)
This register is mapped from EEPROM data 1ah.

Bit #	Name	Description	R/W	Reset
7:6	doc0_release[1:0]	Control the discharge OC0 release as following: 2-bit: Discharge OC0 release 00: External release. Release the doc0 if scp=0 (detected by SCS pin) after 1ms when doc0_fet_disable = 1. 01: 1s release. The discharge OC will not be released until 1s time out. 10: 2s release. The discharge OC will not be released until 2s time out.	RW	0h

		11	4s release. The discharge OC will not be released until 4s time out.		

Bit5 – Bit0 doc0_ctrl [bit5:bit0] Configure the discharge over current DOC0 threshold.

Bit5 – Bit0	DOC0 threshold	Bit5 – Bit0	DOC0 threshold
000000 – 000101	Reserved	100000	160mV / Rs
000110	30mV / Rs	100001	165mV / Rs
000111	35mV / Rs	100010	170mV / Rs
001000	40mV / Rs	100011	175mV / Rs
001001	45mV / Rs	100100	180mV / Rs
…	…	…	…
011011	135mV / Rs	110110	270mV / Rs
011100	140mV / Rs	110111	275mV / Rs
011101	145mV / Rs	111000	280mV / Rs
011110	150mV / Rs	111001	285mV / Rs
011111	155mV / Rs	111010 – 111111	Reserved

Register 1bh – DOC0 & DOC1 Delay Register (DOC01delay)

This register is mapped from EEPROM data 1bh.

Bit #	Name	Description	R/W	default
7:4	doc0_delay[3:0]	“0000”: 2ms “0001”: 4ms “0010”: 8ms “0011”: 16ms “0100”: 32ms “0101”: 64ms “0110”: 96ms “0111”: 128ms “1000”: 256ms “1001”: 512ms “1010”: 768ms “1011”: 1s “1100”: 2s “1101”: 4s ”1110”: 8s “1111”: 16s	RW	0h

Bit #	Name	Description	R/W	default
3:0	doc1_delay[3:0]	"0000": 32us "0001": 64us "0010": 128us "0011": 256us "0100": 512us "0101": 1ms "0110": 2ms "0111": 4ms "1000": 8ms "1001": 16ms "1010": 32ms "1011": 48ms "1100": 64ms "1101": 96ms "1110": 128ms "1111": 256ms	RW	0h

Register 1ch – DOC1 Control Register (DOC1ctrl)

This register is mapped from EEPROM data 1ch.

Bit #	Name	Description	R/W	Reset
7	sc_release	Control the SC release as following: 1-bit: SC release 0: External release. Release the SC if scp=0 (detected by SCS pin) after 1ms when sc_fet_disable = 1. 1: 1 minute release. The SC will not be released until 1 minute time out.	RW	0h
6	doc1_release	Control the Discharge OC1 release as following 1-bit: Discharge OC1 release 0: External release. Release the DOC1 if scp=0 (detected by SCS pin) after 1ms when sc_fet_disable = 1. 1: 1 minute release. The DOC1 will not be released until 1 minute time out.		

Bit5 – Bit0 doc1_ctrl [bit5:bit0]: Configure the discharge over current DOC1 threshold.

Bit5 – Bit0	DOC1 threshold	Bit5 – Bit0	DOC1 threshold
000000 – 000010	Reserved	100000	340mV / Rs
000011	50mV / Rs	100001	350mV / Rs
000100	60mV / Rs	100010	360mV / Rs
000101	70mV / Rs	100011	370mV / Rs
000110	80mV / Rs	100100	380mV / Rs
000111	90mV / Rs	100101	390mV / Rs
001000	100mV / Rs	100110	400mV / Rs
001001	110mV / Rs	100111	410mV / Rs
,,,	…	…	…
011011	290mV / Rs	111001	590mV / Rs
011100	300mV / Rs	111010	600mV / Rs
011101	310mV / Rs	111011	610mV / Rs
011110	320mV / Rs	111100	620mV / Rs
011111	330mV / Rs	111101 – 111111	Reserved

Register 1dh – COC & SC Delay Register (COCSCdelay)

This register is mapped from EEPROM data 1dh.

Bit #	Name	Description	R/W	Default
7:5	Reserved	Reserved (unimplemented)		
4:2	coc_delay[2:0]	"000": 2ms "001": 4ms "010": 8ms "011": 16ms "100": 64ms "101": 128ms "110": 256ms "111": 512ms	RW	000
1:0	sc_delay[1:0]	"00": 0, immediately (nature delay) "01": 128us "10": 512us "11": 1ms	RW	00

Register 1eh – OT/UT, OV/UV, UB Delay/Release and Parameter Freeze Register (TVUBTimeout)

This register is mapped from EEPROM data 1eh.

Bit #	Name	Description	R/W	Reset
7	user_freeze	active high to freeze the user parameter including internal register from 16h~1eh and EEPROM data from 16h~3fh. But the block erase is always open to SMBUS when ee_enable = 1. This bit can only be read via SMBUS, and can be written by mapping the corresponding EEPROM data.	RW	0
6	ub_enable	active high to enable Unbalance detection	RW	0
5:4	ovuv_timeout[1:0]	Control the OV delay time and release time as (2,4,6,8) scan cycles Control the UV delay time and release time as (1,2,4,8) scan cycles	RW	00
3:2	otut_timeout[1:0]	Control the OT/UT delay time and release time as (2,4,6,8) scan cycles	RW	00
1:0	ub_timeout[1:0]	Control the UB delay time and release time as (2,4,6,8) scan cycles	RW	00

Register 1fh – Function Control Register (FunctionCtrl)

This register is mapped from EEPROM data 1fh.

Bit #	Name	Description	R/W	Reset
7	ee_enable	active high to enable EEPROM operation (i.e. Reg.0bh is not checked until ee_enable = 1 for reliabilty). This bit can be directly read and written via SMBUS, and also can be written by EEPROM mapping.	RW	0
6:2	Reserved	Reserved (unimplemented)		
1	sleep_support	'1': support sleep function when sleep_nsupport = 0; '0': don't support sleep function when sleep_nsupport = 1; This bit is a critical bit, which must be the complement of sleep_nsupport. Otherwise an internal reset will be generated to reset the chip. So it can be used as soft reset. **OZ8940 will enter sleep state when no events for 4 consecutive ADC scan cycles. OZ8940 will automatically do EEPROM mapping as soon as it is waked up.**	RW	1
0	sleep_nsupport	'0': support sleep function when sleep_support = 1; '1': don't support sleep function when sleep_support = 0; This bit is a critical bit, which must also be the complement of sleep_support.	RW	0

Register 20h – OV/UV Timer Register (OUVtimer)

Bit #	Name	Description	R/W	Reset Value
7:6	Reserved	Reserved		
5:3	ov_timer[2:0]	ov timer(unit is a scan cycle)	R	0h
2:0	uv_timer[2:0]	uv timer(unit is a scan cycle)	R	0h

Register 21h – OT/UT Timer Register (OUTtimer)

Bit #	Name	Description	R/W	Reset Value
7:6	Reserved	Reserved		
5:3	ot_timer[2:0]	ot timer(unit is a scan cycle)	R	0h
2:0	ut_timer[2:0]	ut timer(unit is a scan cycle)	R	0h

Register 22h – UB Timer Register (UBtimer)

Bit #	Name	Description	R/W	Reset Value
7:3	Reserved	Reserved.		
2:0	ub_timer[2:0]	UB timer (unit is a scan cycle).	R	0h

Register 23h~3fh – Reserved Register

OZ8940 EEPROM Registers

OZ8940 EEPROM register is organized as 12 bits. 00h~1fh EEPROM bit11- bit8 are not used.
EEPROM 12h~1fh bit7 – bit0 will be mapped to operation register 12h~1fh bit7 – bit0 correspondingly.

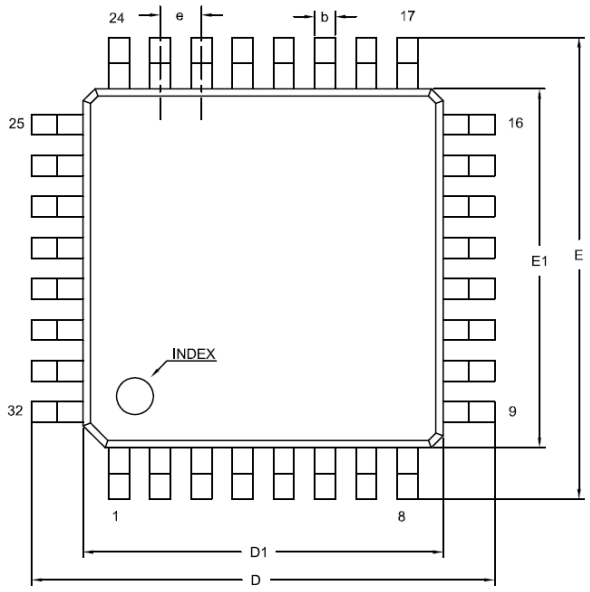
EEPROM Section	Description
00h~11h	Reserved
12h~1fh	This section is used to save the control data to control the system operation. Bit7 – bit0 of this section EEPROM registers will be automatically mapped into the operation register 12h~1fh one by one. Please see the corresponding description in operation register 12h~1fh.
20h~2fh Log Data	This section are used to save the required threshold and release value for OV, UV, OT, UT, UB, OVPF and Bleeding, which will not mapped into the operation registers. When needed, hardware will require EEPROM Controller to read out the corresponding data.

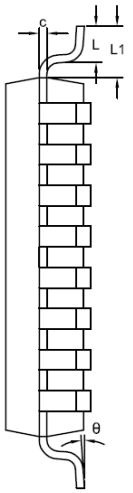
Data index (hex)	Data Name	Bit Number								
		11~8	7	6	5	4	3	2	1	0
00~14		Reserved								
15	ATEctrl	0000	ate_freeze	Reserved						
16	SYSconfig	0000	gpio_ctrl[1:0]		SMBus_addr[2:0]			cell_number[2:0]		
17	MiscCtrl	0000	auto_scan_start	sleep_time	ovpf_enable	Reserved	bleeding_accuracy[1:0]		efetc_mode[1:0]	

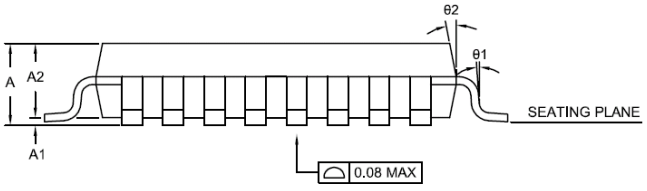
Data index (hex)	Data Name	Bit Number								
		11~8	7	6	5	4	3	2	1	0
18	IntegratorCtrl	0000	Reserved				chg_integ_ctrl[1:0]		dsg_integ_ctrl[1:0]	
19	COCctrl	0000	fet_control_sel	coc_release[1:0]		coc_ctrl[4:0]				
1a	DOC0ctrl	0000	doc0_release_ctrl[1:0]		doc0_ctrl[5:0]					
1b	DOC01delay	0000	doc0_delay[3:0]				doc1_delay[3:0]			
1c	DOC1ctrl	0000	sc_release	doc1_release	doc1_ctrl[5:0]					
1d	COCSCdelay	0000	Reserved			coc_delay[2:0]			sc_delay[1:0]	
1e	VTUBTimeout	0000	user_freeze	ub_enable	ovuv_timeout[1:0]		otut_timeout[1:0]		ub_timeout[1:0]	
1f	FunctionCtrl	0000	ee_enable	Reserved					sleep_support	sleep_nsupport
20	OV_Threshold	ov_threshold[11:0]								
21	OV_Release	ov_release[11:0]								
22	UV_Threshold	uv_threshold[11:0]								
23	UV_Release	uv_release[11:0]								
24	UB_ Threshold	ub_threshold[11:0]								
25	OTI_Threshold	OTI_threshold[11:0]								
26	OTI_Release	OTI_release[11:0]								
27	UTI_Threshold	UTI_threshold[11:0]								
28	UTI_Release	UTI_release[11:0]								
29	OTE_Threshold	ote_threshold[11:0]								
2a	OTE_Release	ote_release[11:0]								
2b	UTE_Threshold	ute_threshold[11:0]								
2c	UTE_Release	ute_release[11:0]								
2d	BLD_Threshold	bleeding_threshold[11:0]								
2e	OVPF_threshold	ovpf_threshold[11:0]								
2f	OVPF_release	ovpf_release[11:0]								
30~3f	user data Reserved	Reserved								

PACKAGE INFORMATION

32L LQFP 7x7mm Package Outline Drawing







SYMBOL	DIMENSION (MM)		
	MIN	NOR	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.30	-	0.45
c	0.09	-	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.80 BSC		
L	0.45	-	0.75
L1	1.00 REF		
θ	0°	-	7°
θ1	0°	-	-
θ2	11°	12°	13°

TE:
REFER TO JEDEC STD MS-026 BBA
DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSIONS.
ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE." DI" AND "E1" ARE
MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDE MOLD
MISMATCH

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