Battery Pack Protection and Monitor IC

FEATURES

- **Supports 5-13 Series Li-ion and Li-polymer Battery Cells or 20/30 Series NiMH battery Cells**
- **Multi-channel ADC for current, voltage and temperature measurement**
  - 13 channels for LiIon cell voltage measurement (signed 13 bits).
  - 2 channels for 20S NiMH cell voltage measurement (signed 13 bits), when configured to 20S NiMH
  - 3 channels for 30S NiMH cell voltage measurement (signed 13 bits), when configured to 30S NiMH
  - 1 channel for current measurement (signed 16 bits, accuracy down to 2.1nVhr)
  - 1 channel for internal temperature measurement (signed 13 bits)
  - 3 channels reserved for customer specific applications (one 16bits; two 13bits)
- **Built-in Protections include:**
  - Over voltage (OV)
  - Under voltage (UV)
  - Over current (OC)
  - Short circuit (SC)
  - Over temperature (OT)
  - Under temperature (UT)
  - Permanent Fail (PF)
- **Embedded 64X16Bits EEPROM for programmable protection thresholds and variable threshold detection / release time**
- **Supports Internal/External Bleeding for Cell balance**
- **Supports hardware mode (without uP) or software mode (with uP)**
- **Embedded voltage based gas gauge function**
- **Supports separate charge and discharge loop**
- **Integrated 2.5V, 3.3V voltage regulator**
- **Integrated MOSFET driver**
- **Supports PWM discharge (for power tools application)**
- **Supports I^2C serial Interface**
- **Supports battery authentication for better security**
- **Low power consumption**
- **Package: LQFP 64L**
- **Operating Temperature Range: -40°C to +70°C**

APPLICATIONS

- **Electric Bicycle**
- **Electric Motorcycle**
- **Power Tools**
- **UPS backup battery**

GENERAL DESCRIPTION

OZ890 is a highly integrated battery pack protection and monitor IC for managing Li-Ion or NiMH battery pack in electric bicycle, electric motorcycle, power tools, and UPS applications. It supports 5-13 (4-Bit EEPROM configuration) series Li-Ion battery pack or 20/30 series NiMH battery pack applications.

The integrated protection circuits work constantly to monitor each cell's voltage, the charge/discharge current and the pack temperature to provide over-voltage, under-voltage, over-current, short circuit, over-temperature and under-temperature safety protection. Working with embedded FET driver circuits, the protection circuits will independently shut off the FETs if necessary. When cell voltage is higher than the pre-set maximum rating voltage PFVH or lower than pre-set lowest working voltage PFVL, OZ890 can automatically assert the Permanent Fail (PF) signal to blow an external fuse or the PF signal can be used to drive an LED to signal an alarm to user. All of the protection thresholds and their related delay time are programmable through the settings in EEPROM for different battery types and the needs of actual applications.

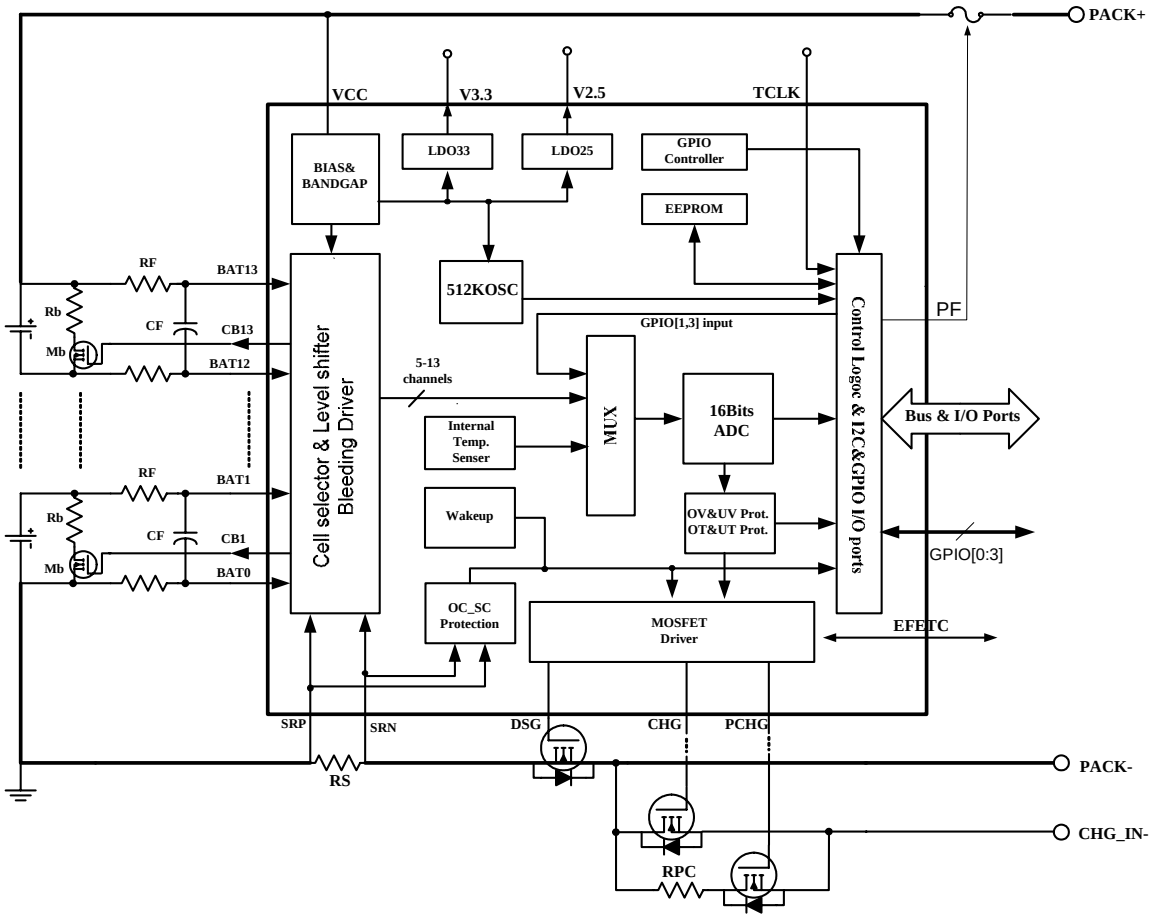
With integrated multi-channel 16-bit ADC, OZ890 measures the voltage, current and temperature of the battery pack, and implements a simple voltage based gas gauge. With the option of working with O_2Mircro's gas gauge uP or other general MCU, a more accurate coulomb counting gas gauge function can be implemented.

OZ890 supports internal/external bleeding for cell voltage balance during charge state, ensuring longer battery life.

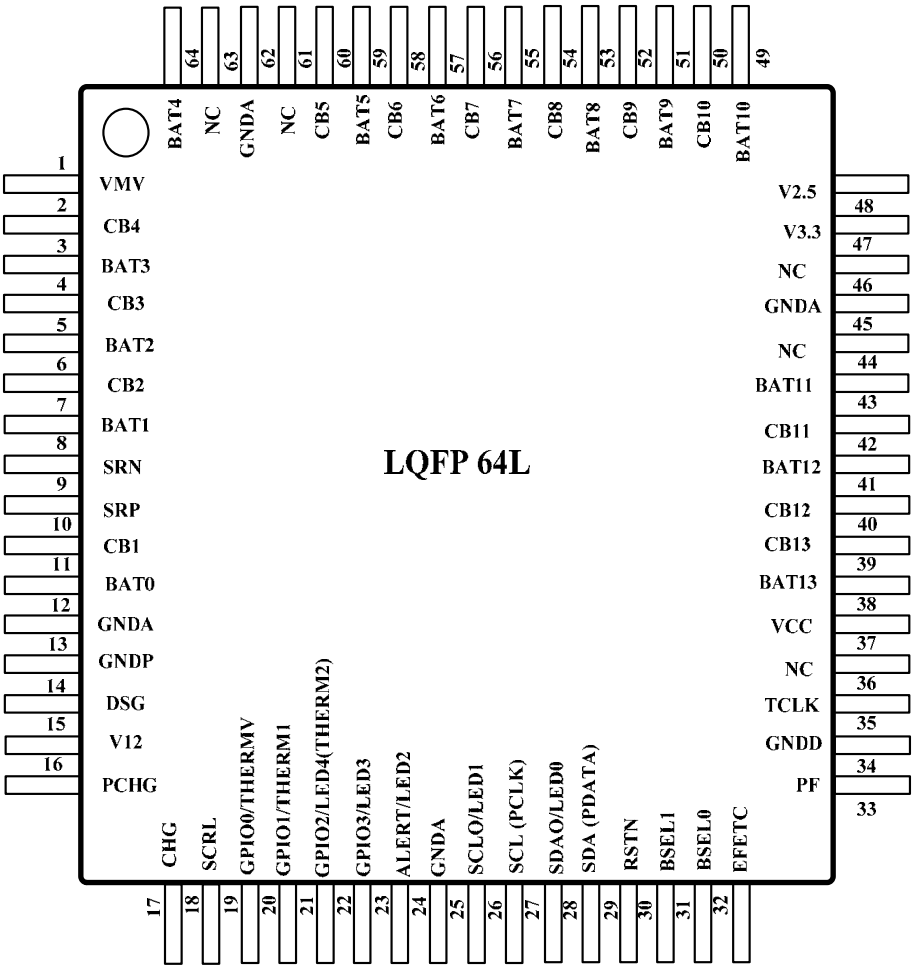
OZ890 can be configured to work in hardware mode (without uP) or software mode (with uP) by embedded EEPROM (2Bits). In hardware mode OZ890 can work independently for Li-ion or NiMH battery pack protection and Monitoring. In software mode, OZ890 can work with external uP or MCU to

implement a more accurate coulomb counting gas gauge function. In software mode, the protection engine and state machine can be controlled by the uP.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Name	Pin No	I/O	Description	
			Hardware Mode	Software Mode
VMV	1	Power	Supply Power for chip; for internal use only	
CB4	2	O	Cell4 external bleeding control	
BAT3	3	I	Cell3 positive input	
CB3	4	O	Cell3 external bleeding control	
BAT2	5	I	Cell2 positive input.	
CB2	6	O	Cell2 external bleeding control	

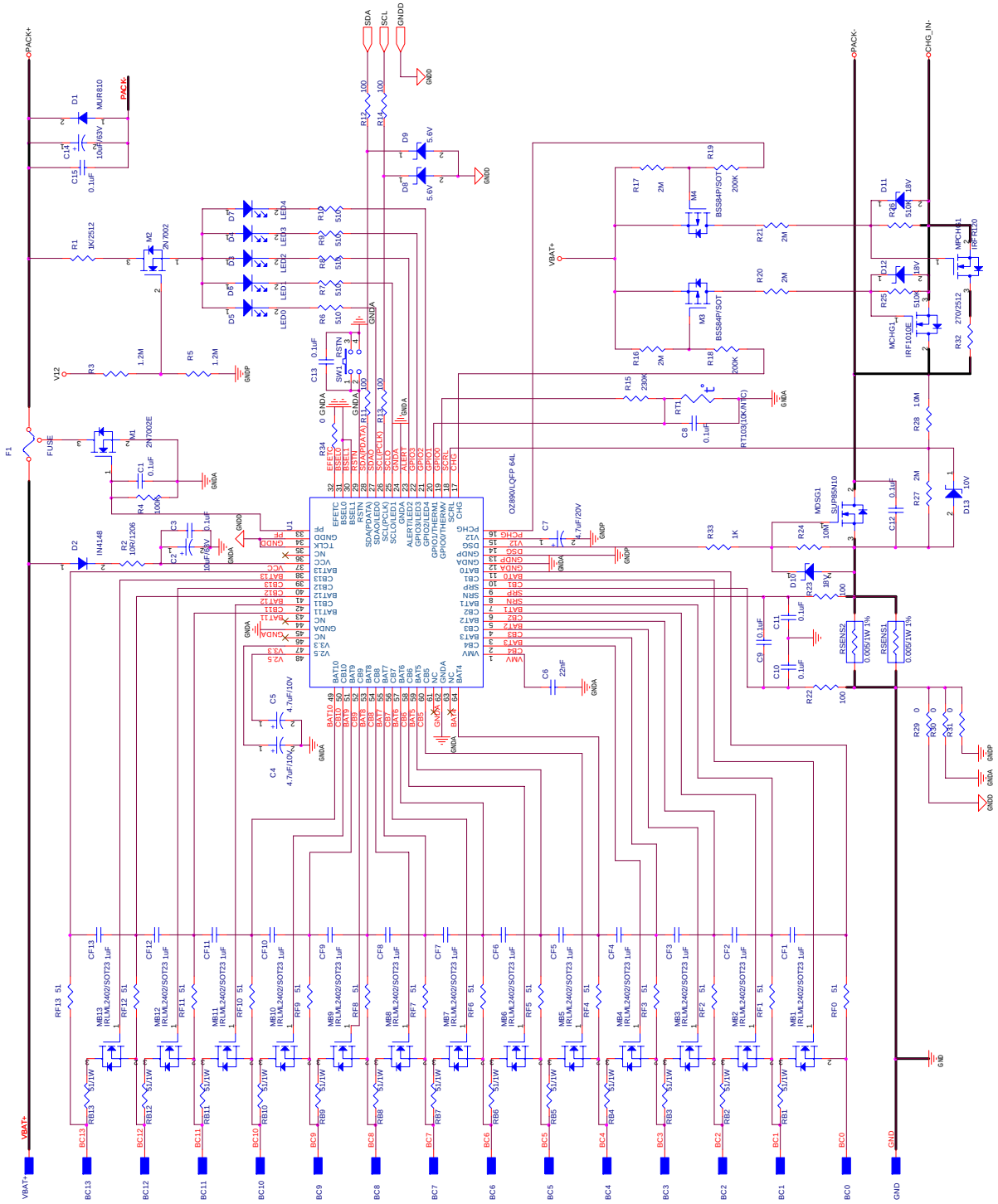
Name	Pin No	I/O	Description	
			Hardware Mode	Software Mode
BAT1	7	I	Cell1 positive input	
SRN	8	I	Current sense resistor negative terminal	
SRP	9	I	Current sense resistor positive terminal	
CB1	10	O	Cell1 external bleeding control	
BAT0	11	I	Cell1 negative input	
GNDA	12	Ground	Analog ground	
GNDP	13	Ground	Power ground	
DSG	14	O	Discharge MOSFET control	
V12	15	Power	12V power for discharge MOSFET driver.	
PCHG	16	O	Pre-charge MOSFET control	
CHG	17	O	Charge power MOSFET control	
SCRL	18	I	Short circuit external automatic release input	
THERMV/ GPIO0	19	I/O	External thermal sensor driver voltage	GPIO0
THERM1/GPIO1	20	I/O	External thermal sensor input1	GPIO1
LED4 (THERM2)[1] /GPIO2	21	I/O	LED driver or optional external thermal sensor input2	GPIO2
LED3/GPIO3	22	I/O	LED driver	GPIO3
LED2/ALERT	23	O	LED driver	Alert output to uP
GNDA	24	Ground	Analog ground	
LED1/SCLO	25	I/O	LED driver	4-wire I2C clock output
SCL (PCLK)	26	I/O	I2C / PBUS clock line	I2C / PBUS clock line or 4-wire I2C clock input
LED0/SDAO	27	I/O	LED driver	4-wire I2C data output
SDA (PDATA)	28	I/O	I2C / PBUS data line	I2C / PBUS data line or 4-wire I2C data input
RSTN	29	I/O	External reset input	External reset input / DeadMan reset output
BSEL1	30	I	Bus type configure input1	
BSEL0	31	I	Bus type configure input0	
EFETC	32	I/O	External FET control signal, can be configured to input or output	
PF	33	O	Permanent failure output. Active high	
GNDD	34	Ground	Digital ground	
TCLK	35	I	External clock input	
NC	36		Not connected	

[1] In hardware mode, if 2 external thermal sensors are chosen, LED4 will be replaced by THERM2

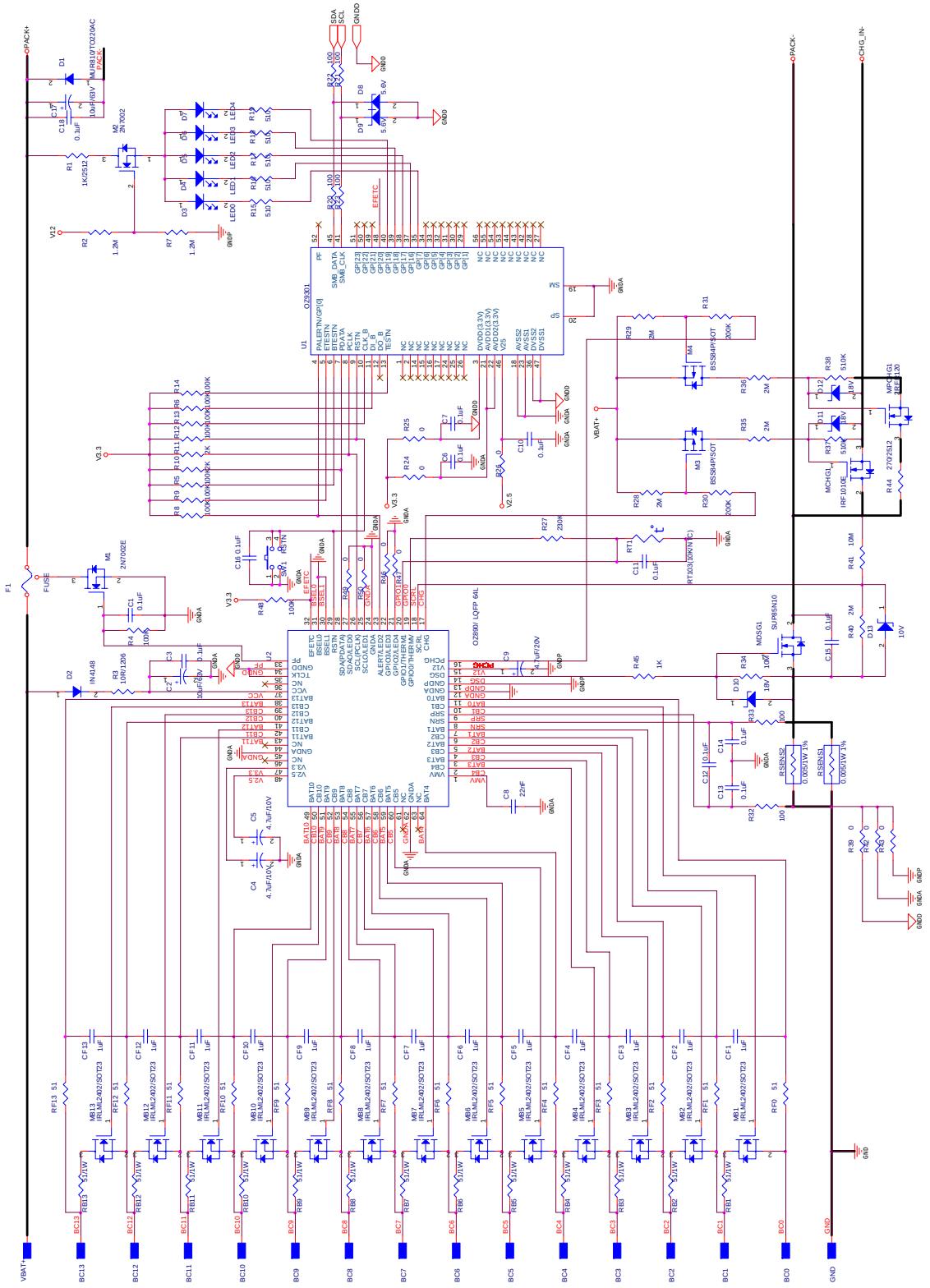
Name	Pin No	I/O	Description	
			Hardware Mode	Software Mode
VCC	37	Power	Chip Power supply	
BAT13	38	I	Cell13 positive input	
CB13	39	O	Cell13 external bleeding control	
CB12	40	O	Cell12 external bleeding control	
BAT12	41	I	Cell12 positive input	
CB11	42	O	Cell11 external bleeding control	
BAT11	43	I	Cell11 positive input	
NC	44		Not connected	
GNDA	45	Ground	Analog ground	
NC	46		Not connected	
V3.3	47	Power	3.3V Power Supply	
V2.5	48	Power	Disabled	2.5V Power Supply
BAT10	49	I	Cell10 positive input	
CB10	50	O	Cell10 external bleeding control	
BAT9	51	I	Cell9 positive input	
CB9	52	O	Cell9 external bleeding control	
BAT8	53	I	Cell8 positive input	
CB8	54	O	Cell8 external bleeding control	
BAT7	55	I	Cell7 positive input	
CB7	56	O	Cell7 external bleeding control	
BAT6	57	I	Cell6 positive input	
CB6	58	O	Cell6 external bleeding control	
BAT5	59	I	Cell5 positive input	
CB5	60	O	Cell5 external bleeding control	
NC	61		Not connected	
GNDA	62	Ground	Analog ground	
NC	63		Not connected	
BAT4	64	I	Cell4 positive input	

TYPICAL APPLICATION SCHEMATICS

Hardware Mode



Software Mode



DC CHARACTERISTICS

Absolute Maximum Ratings

Supply voltage range		VCC	-0.5V to 56V
Input	Analog	SRP,SRN	-0.5V to 0.5V
	Analog	THERMV(power supply for temperature sense resistor)	-0.5V to 6V
	Analog	THERM1(13bits ADC input),THERM2(13bits),THERM3(13-16bits)	-0.5V to 6V
	Analog	BAT0 to BAT1,BAT1 to BAT2,BAT2 to BAT3,BAT3 to BAT4,BAT4 to BAT5,BAT5 to BAT6,BAT6 to BAT7,BAT7 to BAT8,BAT8 to BAT9,BAT9 to BAT10,BAT10 to BAT11,BAT11 to BAT12,BAT12 to BAT13	-0.5V to 6V (VBATn=Vcell*n)
	Analog	SCRL	-0.5V to 12V
	Analog	VMV	-0.5V to 20V
	Digital	BSEL0,BSEL1	-0.5V to 3.6V
	Digital	RSTN, TCLK	-0.5V to 3.6V
		All other input pins	
Output	Analog	PCHG,CHG	-0.5V to 48V
	Analog	DSG	-0.5V to 12V
	Digital	PF	-0.5V to 3.6V
	Digital	CB1,CB2,…CBn…CB13	(n-1)*Vcell to n*Vcell
I/O	Digital	GPIO[0:3]/LEDx, SCLO, SCL(PCLK), SDAO, SDA(PDATA), EFETC	-0.5V to 3.6V
Operating free-air temperature range, TA			-40°C to 70°C
Storage temperature range, Tstg			-55°C to 150°C
Lead temperature(soldering, 10 sec)			300°C

Note 1: All voltages are with respect to ground of this device except BATn - BAT(n-1),where n=1,2,3,4,5,6,7,8,9,10,11,12,13 cell voltage
Note 2: Ground refers to common node of GNDA, GNDD, and GNDP

Electrical Characteristics

Power Supply					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Supply Voltage(VCC)		8		56	V
Supply Current	Normal Mode			2000	uA
	Idle Mode			200	uA
	Sleep Mode			50	uA

General Purpose Inputs And Outputs(GPIO)					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
V_{IH} High-level Input Voltage		2			V
V_{IL} Low-level Input Voltage				0.8	V
V_{OH} Output Voltage High	Iload = -0.5mA	V3.3 -0.7			V
V_{OL} Output Voltage Low	Iload = 0.5mA			0.4	V
Current Drive Capability	GPIO0		1		mA
Current Drive Capability	GPIO1, 2, 3		8		mA

3.3V LDO Regulator					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Regulator Output Voltage	I_O <60mA	2.97	3.3	3.63	V
Line Regulation		40			dB
Load Regulation			TBD		mV
3.3V Current Limit				80	mA

2.5V LDO Regulator					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Regulator Output Voltage		2.25	2.5	2.75	V
Line Regulation		40			dB
Load Regulation			TBD		mV
2.5V Current Limit				50	mA

12V Power					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Regulator Output Voltage		10.8	12	13.2	V
Line Regulation					mV
Load Regulation			TBD		mV
12V Current Limit				15	mA

Multi-Channel ADC						
Parameter		**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Current Channel (1 channel)	Input Voltage Range		-250		+250	mV
	Resolution			16 bits		
	Conversion Time				270	mS
	Offset		Auto offset cancellation			
	Slope		In software mode, support Slope Calibration			
Lion-ion Cell Voltage Channel	Input Voltage Range		-0.3		5.0	V
	Resolution			13 bits		
	Conversion Time				32	mS
	Offset		Auto offset cancellation			
	Slope		In software mode support slope calibration			
NiMH Cell Voltage Channel	Input Voltage Range		-0.3		5.0	V
	Resolution			13 bits		
	Conversion Time				32	mS
	Offset		Auto offset cancellation			
	Slope		In software mode support slope calibration			
Internal Temperature (1 channel)	Input Voltage Range		-0.3		2.5	V
	Resolution			13 bits		
	Conversion Time				32	mS
	Offset		Auto offset cancellation			
	Slope		In software mode support slope calibration			
GPIO[1:2] channel	Input Voltage Range		-0.3		2.5	V
	Resolution			13 bits		
	Conversion Time				32	mS
	Offset		Auto offset cancellation			
	Slope		In software mode support slope calibration			
GPIO[3]	Input Voltage Range		-0.3		2.5	V
	Resolution		13bit		16 bits	
	Conversion Time		32		270	mS
	Offset		Auto offset cancellation			
	Slope		In software mode support slope calibration			

Internal Oscillator					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
512kHz Oscillator Frequency		470	512	552	KHz
32kHz Oscillator Frequency		28	30	33	KHz

Over-Current(OC) And Short-Circuit(SC) Protection				
Parameter	**Test Conditions**	**MIN**	**MAX**	**Step**
OC Detection Threshold Range	Charge	10mV	105mV	5mV
	Discharge	30mV	285mV	5mV
OC Hysteresis Value	Charge	5mV		
	Discharge	10mV		
OC Delay Time (8-bit setup)		2mS	16.3S	***Note1***
OC Release Time (4-bit setup)	Charge	0.5min	4.5min	0.25min
	Discharge	0.5min	4.5min	0.25min
SC Detection Threshold Range	Discharge	50mV	620mV	10mV
SC Hysteresis Value	Charge	N/A		
	Discharge	20mV		
SC Delay Time (8-bit setup)		4uS	31.6mS	***Note 2***
SC Release Time (4-bit setup)		0.5min	4.5min	0.25min

Note1: 8-bit OC delay control byte divided into two sections, The high 5 bits are used to indicate the over current delay time as N+1 (N is the 5 bits value) delay units ; the low 3 bits are used to indicate the OC delay unit as following:

OC delay scale	OC delay unit	OC delay scale	OC delay unit
3'b000	2ms*1=2ms	3'b100	2ms*31=62ms
3'b001	2ms*3=6ms	3'b101	2ms*63=126ms
3'b010	2ms*7=14ms	3'b110	2ms*127=254ms
3'b011	2ms*15=30ms	3'b111	2ms*255=510ms

The OC delay time = (N+1)*(OC delay unit), so its range is 2ms~16.3s

Note2: 8-bit SC delay control byte divided into two sections. The high 5 bit are used to indicate the short circuit delay time as N+1 (N is the 5 bits value) delay units; the low 3 bits are used to indicate the SC delay unit as following:

SC delay scale	SC delay unit	SC delay scale	SC delay unit
3'b000	4us*2=8us	3'b100	4us*32=128us
3'b001	4us*4=16us	3'b101	4us*64=256us
3'b010	4us*8=32us	3'b110	4us*128=512us
3'b011	4us*16=64us	3'b111	4us*256=1024us

The SC delay time = (N+1)*(SC delay unit), so its range is 8us~32.8ms

Over-Voltage(OV) And Under-Voltage(UV) Protection					
Parameter	**Test Condition**	**MIN**	**TYP**	**MAX**	**Unit/step**
OV Detection Threshold Value		13bits programmable (0-5V)			V
OV Release Value		13bits programmable (0-5V)			V
OV Delay Time (4-bit setup)		1		16	Sec.
OV Release Time (same as OV delay time)		1		16	Sec.
UV Detection Threshold Value		13bits programmable (0-5V)			V
UV Release Value		13bits programmable (0-5V)			V
UV Delay Time (4-bit setup)		1		16	Sec.
UV Release Time (same as UV delay time)		1		16	Sec.

Permanent Fail Voltage (PFVL and PFVH) Protection					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**units/step**
PFVL Threshold Range		13bits programmable (0-5V)			V
PFVL Delay Time (2-bit setup)		2		8	2 Sec.
PFVH Threshold Range		13bits programmable (0-5V)			V
PFVH Delay Time (2-bit setup)		2		8	2 Sec.

Internal Thermal Protection (OT & UT)					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit/Step**
OT Detection Threshold value		User Programmable			1°C /2.1mV
OT Detection release Range		User Programmable			1°C /2.1mV
OT Delay Time (4-bit setup)		1		16	TSP ***(Note1)***
OT Release Time (same as OT delay time)		1		16	TSP
UT Detection Threshold Value		User Programmable			V
UT Detection Release Value		User Programmable			V
UT Delay Time (4-bit setup)		1		16	TSP
UT Release Time (same as UT delay time)		1		16	TSP

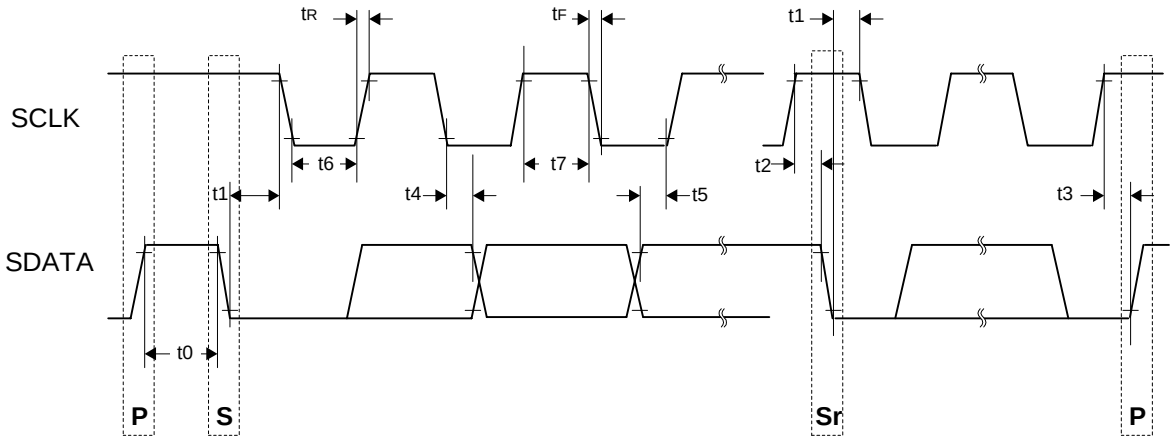
External Thermal Protection (OT & UT)					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit/Step**
OT Detection Threshold value		User Programmable			***(Note2)***
OT Detection release Range		User Programmable			***(Note2)***
OT Delay Time (4-bit setup)		1		16	TSP
OT Release Time (same as OT delay time)		1		16	TSP
UT Detection Threshold Value		User Programmable			V
UT Detection Release Value		User Programmable			V
UT Delay Time (4-bit setup)		1		16	TSP
UT Release Time (same as UT delay time)		1		16	TSP

Note1: *TSP = Temperature Scan Period for all Temperature Channels*
Note2: Depends on external temperature sensor characteristics, refer to Fig.10.

Power MOSFET Driver Circuit					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
CHG High Level		TBD			V
CHG Low Level		TBD			V
PCHG High Level		TBD			V
PCHG Low Level		TBD			V
Rise Time			TBD		
Fall Time			TBD		
DSG High Level		9	11	13.5	V
DSG Low Level		0		0.5	V
Rise Time			TBD		
Fall Time			TBD		
PWM Discharger Frequency		1		8	kHz

AC TIMING

I²C Bus Timing



Symbol	Parameter	Limits		*Units*	Note
		Min	Max		
FSMB	I²C Bus Operating Frequency	10	250	KHz	
t0	Bus free time between Stop and Start condition	4.7	-	µS	
t1	Hold time after (Repeated) Start condition. After this period, the first clock is generated	4.0	-	µS	
t2	Repeated Start condition set up time	4.7	--	µS	
t3	Stop Condition setup time	4.0	-	µS	
t4	Data hold time	150	-	ns	
t5	Data setup time	250	-	ns	
TIMOUT		25	35	ms	See **Note 1**
t6	Clock low period	4.7	-	µS	
t7	Clock high period	4.0	50	µS	See **Note 2**
TLOW:SEXT	Cumulative clock low extend time (slave device)	-	25	ms	See **Note 3**
TLOW:MEXT	Cumulative clock low extend time (master device)	-	10	ms	See **Note 4**
tF	Clock/Data Fall time	-	300	ns	See **Note 5**
tR	Clock/Data Rise Time	-	1000	ns	See **Note 5**

Note 1: A device will timeout when any clock low duration exceeds this value
Note 2: t5 Max provides a simple guaranteed method for devices to detect bus idle conditions.
Note 3: TLOW:SEXT is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to stop. If a slave device exceeds this time, it is expected to release both its clock and data lines and reset itself.
Note 4: TLOW:MEXT is the cumulative time a master device is allowed to extend its clock cycles within one byte of a message as defined from start-to-ack, ack-to-ack, or ack-to-stop.
Note 5: Rise and Fall times are measured between 10% to 90% of the signal amplitude.

FUNCTIONAL DESCRIPTION

OZ890 Power Up Sequence

Fig.1 shows the OZ890 power up sequence. When power supply is applied to VCC, the common bias starts first, followed by the band-gap and 3.3V & 2.5V LDOs. When V3.3>2.2V, the power on reset block generates POR signal to enable the 512K oscillator and initializes the digital section. When Power and clock are ready, the digital circuits will read the pin configuration and EEPROM data, which in turn determines the working state.

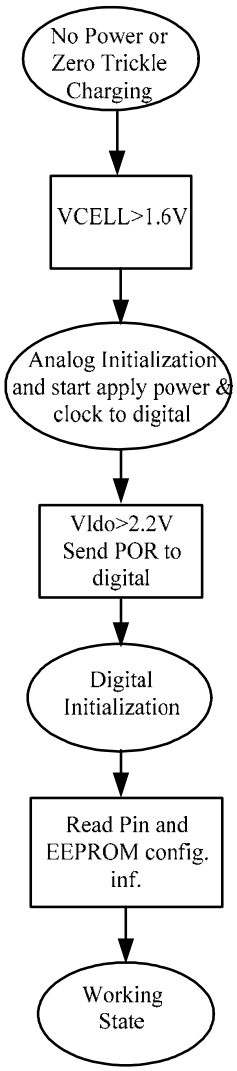


Fig.1 OZ890 Power Up Sequence

Measurements

OZ890 includes a multi-channel ADC (as shown in Fig. 2) for current, voltage and temperature measurement. OZ890's multi-channel ADC measures up to 13 cell voltages, current, internal temperature and external temperature based on cyclic scan and time slot method. It will periodically measure all these values by predefined scan rate. During one measurement period, voltage, current, etc will be measured one by one in different time slot.

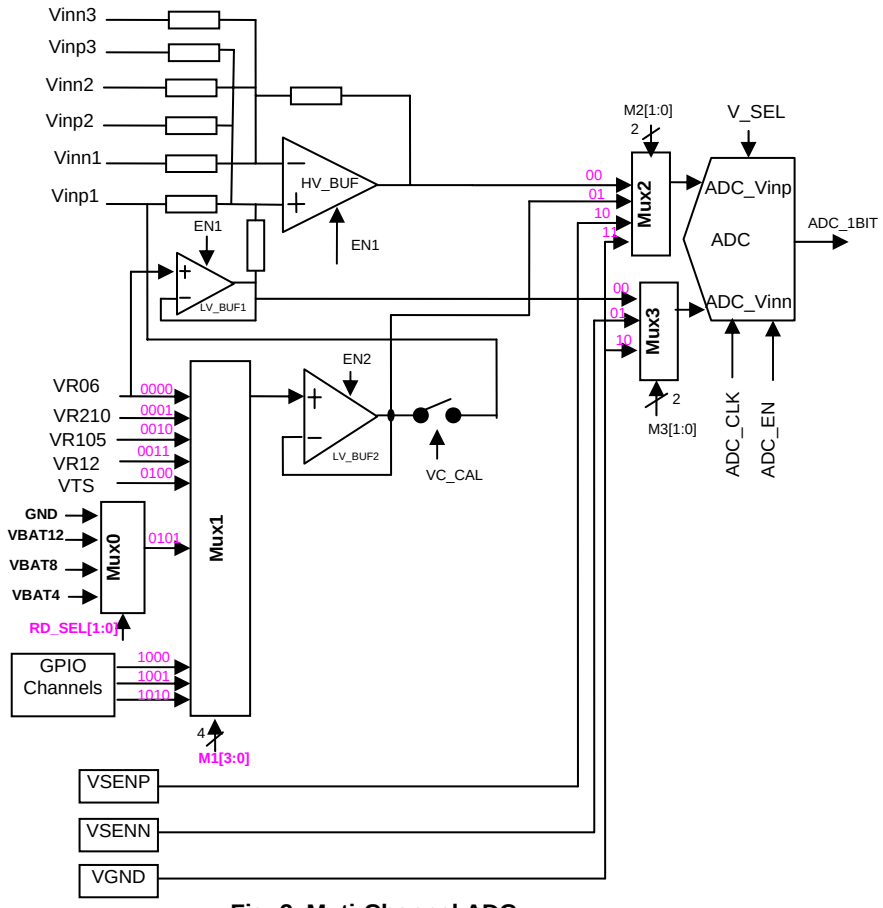


Fig. 2, Muti-Channel ADC

1. ADC Channel Description

a. Current Channel (1 channel)

This is a dedicated channel to measure the current across the sense resistor (2mΩ to 10mΩ), during charging and discharging for coulomb counting or other purpose.

Resolution: 16-bit (signed)

Input Voltage Range: ± 250mV

Auto offset cancellation

Slope calibration can be implemented in software mode for better accuracy.

b. Lion-ion Cell Voltage Channel (5~13 channels)

These channels are designed for cell voltage measurement.

Resolution: 13bits (signed)

Input Voltage Range: -0.3V~5.0V

Auto offset cancellation

Slope calibration can be implemented in software mode for better accuracy.

c. NiMH Cell Voltage Channel (2 channels for 20S, 3 channels for 30S)

For monitoring NiMH battery pack, OZ890 does not scan each cell's voltage, instead it only scans every 10-series NiMH cell total voltage. For 20S NiMH battery pack, 10S tap connects to BAT4 pin, the top positive terminal (20S) connects to BAT8 pin. For 30S NiMH battery pack, 10S tap connects to BAT4 pin, the 20S tap connects to BAT8 pin, the top positive terminal (30S) connects to BAT12 pin.

In order to scale the respective sense point voltage to the ADC input range, OZ890 has 3 internal dividers to scale down the sense point voltage. For the BAT4 point sense voltage, divided by 6.667; for the BAT8 point sense voltage, divided by 13.333; For BAT12 point sense voltage, divided by 20.

For 20 series NiMH battery pack, OZ890 only scans the BAT4 and BAT8 voltage channel instead of scanning all the individual cell voltage channels; and also, for 30 series NiMH battery pack, OZ890 only scans the BAT4, BAT8 and BAT12 voltage. Additionally, it can be configured to just sense BAT12 (for 30S) or BAT8 (for 20S) voltage by 1 bit in EEPROM register 26h bit7.

Resolution: 13bits (signed)
Input Voltage Range: -0.3V~5.0V
Auto offset cancellation
Slope calibration can be implemented in software mode for better accuracy.

d. Internal Temperature (1 channel)

This channel is designed for internal temperature sensor.
Accuracy: 13bits (signed)
Input Voltage Range: -0.3V~2.5V
Auto offset cancellation
Slope calibration can be implemented in software mode for better accuracy.

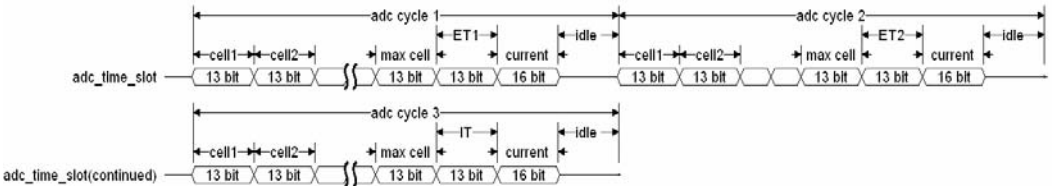
e. GPIO Channel (3 channel)

GPIO1, GPIO2 and GPIO3 can be configured as external temperature sensor (please refer to the external thermal sensor section) or other analog input in software mode, for detailed configuration information please refer to Operation register 2dh. In hardware mode, only GPIO1 (GPIO2 optional) can be active as external temperature sensor channel; GPIO2 and GPIO3 are used for other purposes.

Accuracy: 13bits (signed)
Input Voltage Range: 0.3V~2.5V
Auto offset cancellation
Slope calibration can be implemented in software mode for better accuracy.
(When GPIO3 is not configured to temperature sensor in software mode, its accuracy is 16 bits.

2. Time Slot in Different Configuration

a. The ADC Time Slots for Li-ion in Hardware Mode



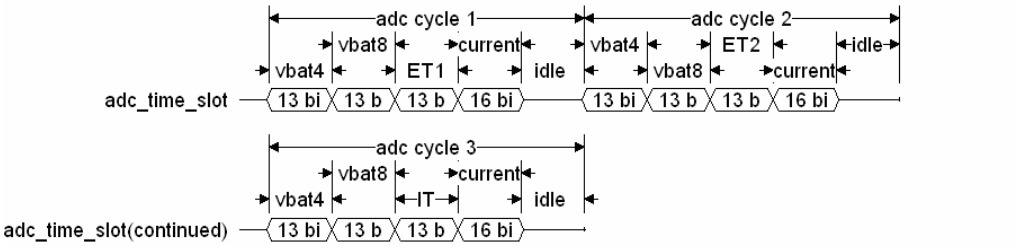
Note:

(1)The slot's length is not in scale.

(2) ET1, ET2 indicate the external temperature; IT indicates the internal temperature; current indicates the current channel from current sensor voltage.

(3) If external temperatures ET1, ET2 are there, adc cycle1, adc cycle2, adc cycle3 will be repeated; if only ET1 is there, adc cycle1, adc cycle3 will be repeated; if only ET2 is there, adc cycle2, adc cycle3 will be repeated; if there is no external temperature, only adc cycle3 will be repeated.

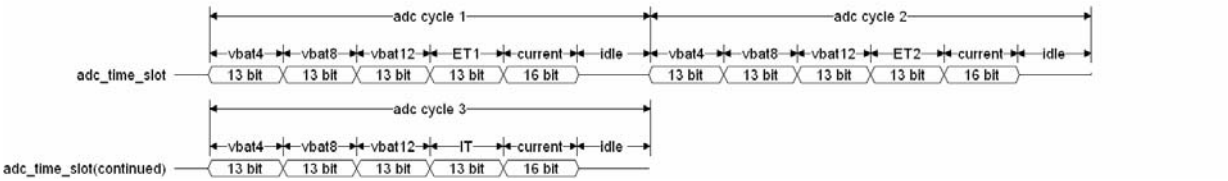
b. The ADC Time Slots for 20S NiMH in Hardware Mode



Note:

(1) The slot's length is not in scale.
(2) ET1, ET2 indicate the external temperature; IT indicates the internal temperature; current indicates the current channel from current sensor voltage.
(3) The vbat4 is for 10 cells' voltage; the vbat8 is for 20 cells' voltage. If the bit NiMH_vpack_only in EEPROM register 26h bit7 is 1, there is only vbat8 time slot without vbat4 time slot; if the bit NiMH vpack only is 0, there are vbat4, vbat8 time slots.
(4) If external temperature ET1 & ET2 are there, adc cycle1, adc cycle2, adc cycle3 will be repeated; if only ET1 is there, adc1 cycle1, adc cyle3 will be repeated; if only ET2 is there, adc cycle2, adc cycle3 will be repeated; if no external temperature is there, only adc cycle3 will be repeated.

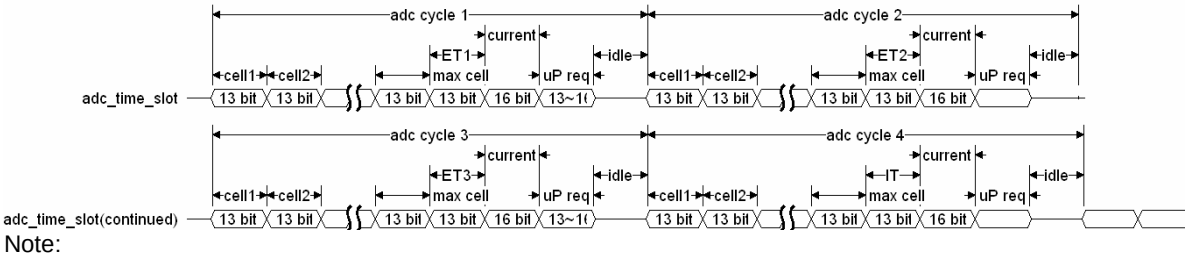
c. The ADC Time Slots for 30S NiMH in Hardware Mode



Note:

(1) The slot's length is not in scale.
(2) ET1, ET2 indicates the external temperature; IT indicates the internal temperature; current indicates the current channel from current sensor voltage.
(3) The vbat4 is for 10 cells' voltage; the vbat8 is for 20 cells' voltage, the vbat12 is for 30 cells' voltage. If the bit NiMH vpack only in EEPROM register 26h bit7 is 1, there is only vbat12 time slot without vbat4, vbat8 time slot; if the bit NiMH vpack only is 0, there are vbat4, vbat8, vbat12 time slots.
(4) If ET1, ET2 external temperature are there, adc cycle1, adc cycle2, adc cycle3 will be repeated; If there is only ET1 external temperature, adc cycle1, adc cycle3 will be repeated; if there is only ET2 external temperature, adc cycle2, adc cycle3 will be repeated; if no external temperature, only adc cycle3 will be repeated.

d. The ADC Time Slots for Li-ion in Software Mode



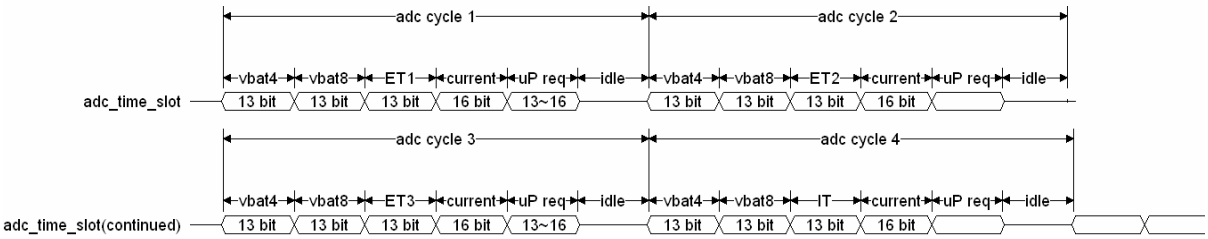
Note:

(1)The slot's length is not in scale.
(2) ET1, ET2, ET3 indicates the external temperature; IT indicates the internal temperature; current indicates the current channel from current sensor voltage or GPIO3 decided by the corresponding register settings.
(3) The "uP req" indicates the ADC request from the uP which can be 13~16bit. In one adc cycle, at least one uP ADC request can be completed. The uP will not launch new adc request until the

previous adc request is finished. In OZ890, there is an ADC busy bit to inform the uP ADC request is being processed; also OZ890 will provide ADC event bit to tell the uP that the ADC request is completed.

(4) If ET1, ET2, ET3 external temperature are there, adc cycle1, adc cycle2, adc cycle3, adc cycle4 will be repeated; if only ET1, ET2 external temperature are there, adc cycle1, adc cycle2, adc cylce4 will be repeated; if only ET1 external temperature is there, adc cycle1, adc cylcle4 will be repeated; if there is no external temperature, only adc cycle4 will be repeated.

e. The ADC time slots for 20S NiMH in software mode



Note:

(1)The slot's length is not in scale.

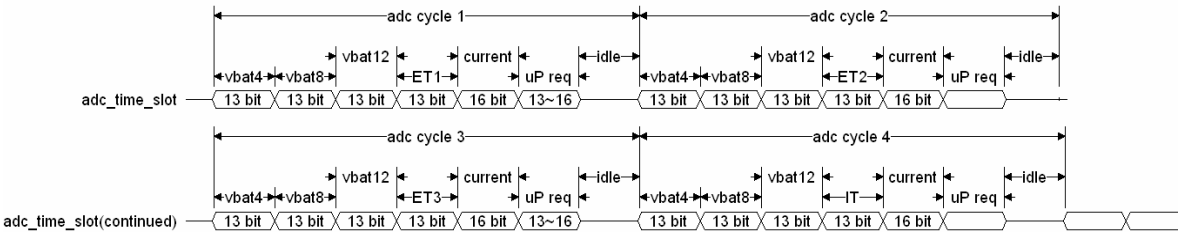
(2) ET1, ET2, ET3 indicates the external temperature; IT indicates the internal temperature; current indicates the current channel from current sensor voltage or GPIO3 decided by the corresponding register settings.

(3) The vbat4 is for 10 cells' voltage; the vbat8 is for 20 cells' voltage. If the bit NiMH vpack only in EEPROM register 26h bit7 is 1, there is only vbat8 time slot without vbat4 time slot; if the bit NiMH vpack only is 0, there are vbat4, vbat8 time slots.

(4) The "uP req" indicates the ADC request from the uP which can be 13~16bit. In one adc cycle, at least one uP ADC request can be completed. The uP will not launch new adc request until the previous adc request is finished. In OZ890, there is an ADC busy bit to inform the uP ADC request is being processed; also OZ890 will provide ADC event bit to tell the uP that the ADC request is completed.

(5) If ET1, ET2, ET3 external temperature are there, adc cycle1, adc cycle2, adc cycle3, adc cycle4 will be repeated; if only ET1, ET2 external temperature are there, adc cycle1, adc cycle2, adc cylce4 will be repeated; if only ET1 external temperature is there, adc cycle1, adc cylcle4 will be repeated; if there is no external temperature, only adc cycle4 will be repeated.

f. The ADC Time Slots for 30S NiMH in Software Mode



Note:

(1)The slot's length is not to scale.

(2) ET1, ET2, ET3 indicates the external temperature; IT indicates the internal temperature; current indicates the current channel from current sensor voltage or GPIO3 decided by the corresponding register settings.

(3) The vbat4 time slot is for 10 cells' voltage; vbat8 is for 20 cells' voltage and vbat12 is for 30 cells' voltage. If the NiMH vpack only bit in EEPROM register 26h bit7 is 1, only the vbat12 time slot is present without the vbat4, vbat8 time slots; if the NiMH vpack only bit is 0, vbat4, vbat8, vbat12 time slots are all present.

(4) The “uP req” indicates the ADC request from the uP which can be 13~16bit. In one adc cycle, at least one uP ADC request can be completed. The uP will not launch new adc request until the previous adc request is finished. In OZ890, there is an ADC busy bit to inform the uP that ADC request is being processed; also OZ890 will provide ADC event bit to tell the uP that the ADC request is completed.

(5) If ET1, ET2, ET3 external temperature are there, adc cycle1, adc cycle2, adc cycle3, adc cycle4 will be repeated; if only ET1, ET2 external temperatures are there, adc cycle1, adc cycle2, adc cylce4 will be repeated; if only ET1 external temperature is there, adc cycle1, adc cylcle4 will be repeated; if there is no external temperature, only adc cycle4 will be repeated.

Voltage Based Gas Gauge

OZ890 has a simple integrated voltage based gas gauge, the battery capacity is displayed by 5 or 4 LEDs. The LEDs are also used for displaying different protection events for debugging purpose when protection event occurs, such as LED0 blinking indicates OC or SC, LED1 blinking indicates OV, LED2 blinking indicates OT; LED3 blinking indicates UT; LED2, LED3 blinking indicates Authentication failure. The LEDs can be controlled by external application circuit to be always on or only on when push button is pressed.

There are 5X13 Bits of EEPROM space for lookup table data setting in registers 66h-6fh, with five variables ***GaugeV1 –GaugeV5.***

Working Mode	Hardware Mode			Software Mode		
Battery Type	M. Li-ion	P. Li-ion	NiMH(20S/30S)	M. Li-ion	P. Li-ion	NiMH(20S/30S)
Lookup Table	GaugeV1: 13Bits EEPROM (20% or 25%)			Coulomb Counting Based Gas Gauge		
	GaugeV2: 13Bits EEPROM (40% or 50%)					
	GaugeV3: 13Bits EEPROM (60% or 75%)					
	GaugeV4: 13Bits EEPROM (80% or 100%)					
	GaugeV5: 13Bits EEPROM (100%)					

Internal/External Bleeding

To keep the balance among battery cells, OZ890 can do cell bleeding for Li-ion batteries when the cells are charged in Hardware Mode; OZ890 will not do cell bleeding for NiMH batteries in any conditions. OZ890 supports internal bleeding and external bleeding. For internal bleeding, the current will be 10mA~15mA for the thermal consideration, and only supports the highest cell bleeding; for the external bleeding, bleeding current is decided by external bleeding resistor Rb (Fig. 3), and can support simultaneously 4 cell bleeding. By configuring EEPROM register 33h, we can enable the bleeding (bit3) (***BleedEnable***), select external/internal bleeding (bit2) (***ExtBleedSel***) and set the maximum external bleeding cell number (bit1:0) (***BleedCellNumber***). EEPROM register 48h, 49h config variables ***BleedStartPoint*** and ***BleedAccuracy*** specify the bleeding start voltage and bleeding accuracy.

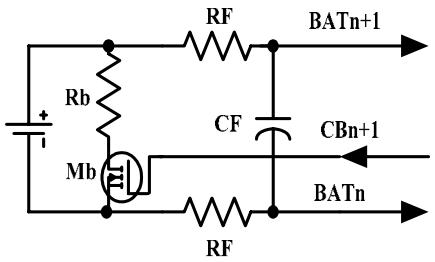


Fig.3 External Bleeding Diagram

In summary, when meeting the following conditions in hardware mode, cell bleeding will automatically start:

- Battery pack is in charge state (current larger than charge current threshold)
- The bleeding function is enabled
- The highest cell voltage exceeds the ***BleedStartPoint*** voltage
- The cell voltages’ difference exceeds the ***BleedAccuracy***
- No error event, like OT, UT, OV, UV, OC, SC. If any error event happens, bleeding stops right away.

In Software Mode, the OZ890 can do cell balance at any time, as controlled by the uP.

Battery Protection

OZ890 includes a digital Battery Protection Engine (BPE), which can operate independently from the uP. The BPE constantly monitors data from the ADC and other circuits described below. If a protection error condition is detected and persists for certain time, the BPE will force the charge and/or discharge FET off. If some vital safety condition, such as extremely high cell voltage (PFVH) or extremely low cell voltage (PFVL) happens, or the Power MOSFET fails, the BPE will assert the Permanent Fail (PF) signal to instruct an optional external fuse circuit to permanently disable the battery pack. In software mode the chip provides an exclusive pin Alert to send the error message to uP except force the charge and/or discharge FET off when error condition happens. But in software mode, the chip does not take any release action, it fully relies on the software decision.

1. Over-current (OC)

OZ890 includes an independent hardware over-current detector that monitors the current that flows through the sense resistor to detect over-current condition in either charge or discharge. If the over-current condition continues for a programmable delay time, the protection circuit will turn off the charge and discharge FETs. The charge and discharge over-current thresholds (***CHGOverCurrentTH*** and ***DSGOverCurrentTH***) are set in EEPROM registers 28h and 29h.
Charge Voc: 10mV to 105mV, 5mV steps.
Discharge Voc: 30mV to 285mV, 5mV steps.
The real OC value is the Voc/Rs, where Rs is current sense resistor value. The over-current delay allows the system to momentarily accept a high current condition. The delay time can be programmed from 2ms to 16.3sec by the parameter ***OverCurrentDelay*** in EEPROM register 2ah. Charge and discharge OC share the same delay time. OC release time can be programmed from 0.5min to 4.25min in 0.25min steps in EEPROM register 2dh. OZ890 also supports an external manual release function, when OC happens, the Chip will release when the input analog signal of Pin SCRL come back to the normal levels, this function is set by the ***OCSCAutoRelease*** in bit4, 2dh EEPROM register.

2. Short-circuit (SC)

Short circuit detection is very similar to over-current detection. When short circuit condition is detected, OZ890 will turn off charge and discharge FETs. Short circuit threshold Vsc can be programmed from 50mV to 620mV in 10mV steps by the parameter ***ShortCurrentTH*** in EEPROM register 2bh.The real current is Vsc/Rs. Short circuit delay time can be programmed from 4us to 32.6ms. The short circuit delay time is configured by EEPROM register 2ch by the parameter ***ShortCurrentDelay***. SC and OC share the same release time in EEPROM register 2dh by the parameter ***OCSCReleaseTime***.

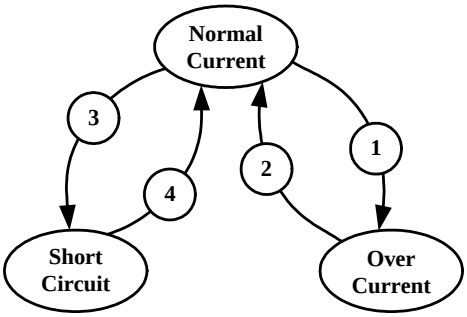


Fig.4 OC&SC State Machine

Description of States (Fig. 4)

State	Description
Normal Current	• No OC, SC event; Permit charge and discharge(permit pre-charge if ***PreCHGEnable***='1' in bit4, 33h EEPROM register
Short Circuit	• Prohibit discharge, charge and pre-charge if ***PreCHGEnable***=1 • If ***OCSCAutoRelease*** ='1' in 2dh EEPROM register, waiting for the timer release • If ***OCSCAutoRelease*** ='0' in 2dh EEPROM register, waiting for external short circuit condition being removed
Over Current	• Prohibit discharge, charge and pre-charge if PreCHGEnable=1 • If ***OCSCAutoRelease*** ='1' in 2dh EEPROM register, waiting for the timer release • If ***OCSCAutoRelease*** ='0' in 2dh EEPROM register, waiting for external discharge OC condition being removed. For charge OC condition, still rely on timer release.

Transition Description (Fig. 4)

Transition	Initial State	Condition		Final State
		Hardware Mode	Software Mode	
1	Normal Current	OC event occurs (charge or discharge current ≥ ***CHG/DSGOverCurrentTH*** & delay timer expires)		Over Current
2	Over Current	In charge condition: release timer expires; In discharge condition: release timer expires if ***OCSCAutoRelease*** ='1' or external release happens if ***OCSCAutoRelease*** ='0'	uP makes decision	Normal Current
3	Normal Current	SC event occurs (discharge current ≥ ***ShortCurrentTH*** & delay timer expires)		Short Circuit
4	Short Circuit	Release timer expires if ***OCSCAutoRelease*** ='1' or external release happens if ***OCSCAutoRelease*** ='0'	uP makes decision	Normal Current

3. Over-voltage (OV)

Figure 5 shows the cell voltage protection state machine. The protection engine performs over-voltage detection by comparing 13 bit values from the ADC with an OV threshold, which is programmed in EEPROM registers 4ah and 4bh as parameter ***OverVoltageTH***. When over-voltage condition is detected, OZ890 will turn off the charge FET after a delay time. This delay time can be programmed from 1s to 16s in 1s steps in EEPROM register 2eh as parameter ***OVUVDelay***. When cell voltage is less than the OV release value and persists for the specified time (**OVUVDelay**), OZ890 Protection Engine will quit the OV condition and turn on the charge FET. The OV release value also can be programmed in EEPROM registers 4ch and 4dh as parameter ***OVRelease***. The OV release value should set lower than OV threshold value.

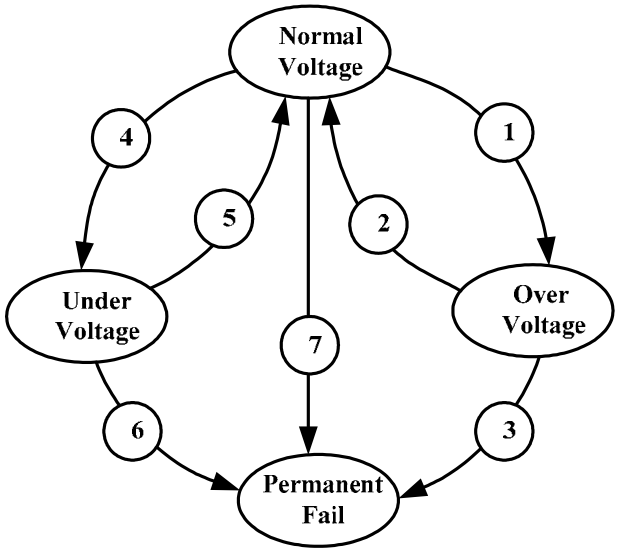


Fig.5 Cell Voltage Protection State Machine

4. Under-voltage (UV)

Under-voltage protection operates in the same way as over-voltage protection. Its threshold can also be programmed in EEPROM registers 4eh and 4fh as parameter ***UnderVoltageTH***. UV release value can be programmed in EEPROM registers 50h and 51h as parameter ***UVRelease***. The UV release voltage value should be set higher than UV threshold value. Under-voltage protection and release has the same delay time as the over-voltage protection and release.

5. Permanent Fail (PF)

There are two Permanent Fail voltage thresholds, one is Permanent Fail Voltage High (PFVH) threshold, and the other is Permanent Fail Voltage Low (PFVL) threshold. If any cell voltage is lower than PFVL or higher than PFVH for the pre-set time, OZ890 will assert a PF signal to blow the external fuse and the pack will have permanent failure. This function acts as the secondary voltage protection and can be disabled by setting the EEPROM register 2fh, bit5:4, ***PFVHEnable*** and ***PFVLEnable***. The PFVL and PFVH thresholds are programmed in EEPROM registers 52h and 53h as parameter ***PFVHTH*** and in EEPROM registers 54h and 55h as parameter ***PFVLTH***. The PF delay time (***PFDelay***) can be programmed from 2s to 32s in 2s steps in EEPROM register 2fh, bit3:0.

When the cells get aged, the imbalance between cells may become progressively worse. When a voltage mismatch between cells reaches a threshold value (***PFUnbalanceTH***) set in EEPROM register 46h and 47h, BPE also will generate PF signal.

Another PF function is Power MOSFET failure. When the charge and/or discharge Power MOSFET is off but still some current flows into or out of the battery pack for about **PFDelay** time, OZ890 will assert a PF signal. This function can be enabled by setting the ***MOSFailEnable*** in 2fh EEPROM register bit6.

States Description (Fig. 5)

State	Description
Normal Voltage	• No OV UV event; Permit charge ,discharge and pre-charge if ***PreCHGEnable***='1' in 33h EEPROM register
Over Voltage	• Prohibit charge and pre-charge if ***PreCHGEnable***='1' • Permit discharge
Under Voltage	• Prohibit discharge • When ***PreCHGEnable***='1', if Vcell < ***UnderVoltageTH*** , permit pre-charge but prohibit charge; if Vcell >= ***UnderVoltageTH***, permit pre-charge and charge • When ***PreCHGEnable***='0', prohibit pre-charge but permit charge
Permanent Fail	• Blown Fuse • System shut down

Transition Description (Fig. 5)

Transition	Initial State	Condition		Final State
		Hardware Mode	Software Mode	
1	Normal Voltage	• OV event occurs(Vcell ≥ ***OverVoltageTH*** & delay timer expires)		Over Voltage
2	Over Voltage	• OV event clears (Vcell ≤ ***OVRelease*** voltage and delay timer expires)	uP makes decision	Normal Voltage
3	Over Voltage	• PFVH event occurs(Vcell ≥ ***PFVHTH*** and delay timer expires);		Permanent Fail
4	Normal Voltage	• UV event occurs(Vcell ≤ ***UnderVoltageTH*** & delay timer expires);		Under Voltage
5	Under Voltage	• UV event clears (Vcell ≥ ***UVRelease*** voltage and delay timer expires)	uP makes decision	Normal Voltage
6	Under Voltage	• PFVL event occurs (Vcell ≤ ***PFVLTH*** and delay timer expires);		Permanent Fail
7.	Normal Voltage	• PFVL or PFVH event occurs (Vcell ≤ ***PFVLTH*** and delay timer expires or Vcell ≥ ***PFVHTH*** and delay timer expires) • Or Power MOSFET failure happens • Or Cell Aging Unbalance Happens		Permanent Fail

6. Thermal Protection (OT and UT)

Thermal protection is performed based on inputs from both the internal temperature sensor and the optional external temperature sensors. Thermal information may be used to temporarily interrupt the charge cycle and/or disable discharge. OZ890 provides both under temperature (UT) and over temperature (OT) protection. Both OT and UT thresholds are programmable. External over temperature (OTE) threshold setting is in EEPROM registers 56h and 57h as parameter ***ExtOverTempTH***, OTE release value programmed in EEPROM registers 58h and 59h as parameter as ***ExtOverTempRelease***. External under temperature (UTE) threshold is set up in EEPROM registers 5ah and 5bh as parameter ***ExtUnderTempTH,*** UTE release value programmed in EEPROM registers 5ch and 5dh as parameter ***ExtUnderTempRelease.*** Internal over temperature (OTI) threshold setting is in EEPROM registers 5eh and 5fh as parameter ***IntOverTempTH.*** OTI release value is programmed in EEPROM registers 60h and 61h as parameter ***IntOverTempRelease***. Internal under temperature (UTI) threshold setting is in EEPROM registers 62h and 63h as parameter ***IntUnderTempTH***. UTI release value is programmed in EEPROM registers 64h and 65h as parameter ***IntUnderTempRelease***, External and

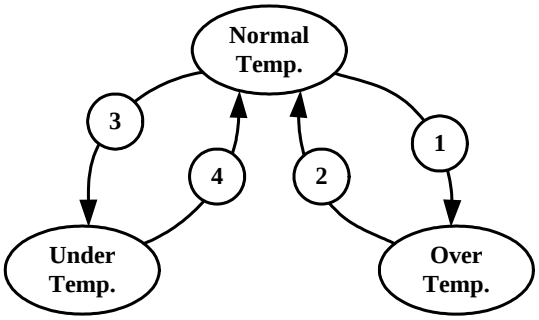


Fig.6 Temperature Protection State Machine

Internal OT/UT delay time can be programmed from 1TSP (Temperature Scan Period) to 16TSP in 1TSP steps in EEPROM register 2eh, bit3:0 as ***OTUTDelay***.

States Description (Fig. 6)

State	Description
Normal Temp	• ***IntUnderTempTH*** < Internal Temperature < ***IntOverTempTH*** • ***ExtUnderTempTH*** < External Temperature < ***ExtOverTempTH*** • Permit charge/discharge if no other protection events • OT UT check
Over Temp.	• Prohibit charge, discharge • Prohibit pre-charge if ***PreCHGEnable***='1' in bit4, 33h EEPROM register • OT check
Under Temp.	• Prohibit charge (& pre-charge if ***PreCHGEnable***='1' in bit4, 33h EEPROM register) • Permit discharge • UT check

Transition Description② (Fig. 6)

Transition	Initial State	Condition		Final State
		Hardware Mode	**Software Mode**	
1	Normal Temp.	• OT event occurs (external Temp ≥ ***ExtOverTempTH*** or Internal temperature ≥ ***IntOverTempTH*** & delay timer expires)		Over Temp.
2	Over Temp.	• OT event clears (external temperature ≤ ***ExtOverTempRelease*** & Internal temperature ≤ ***IntOverTempRelease*** & delay timer expires)	uP makes decision	Normal Temp.
3	Normal Temp.	• UT event occurs (external temperature ≤ ***ExtUnderTempTH*** or Internal temperature ≤ ***IntUnderTempTH*** & delay timer expires)		Under Temp
4	Under Temp	• UT event clears(external temperature ≥ ***ExtUnderTempRelease***& internal temperature ≥ ***IntUnderTempRelease*** & delay timer expires)	uP makes decision	Normal Temp

Power Mode

To save power, OZ890 works in different power mode according to the system status. There are 3 power modes as follows:

Full Power Mode: < 2mA
Idle Mode: < 250uA
Sleep Mode (Optional): < 50uA

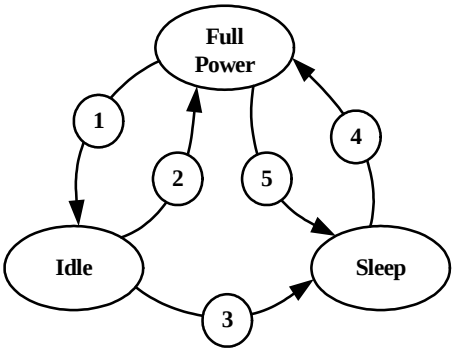


Fig. 7 Power Mode State Machine

State Description (Fig. 7)

State	Description
Full Power	• Normal voltage, temp. and current scan (period: 1S) • Safety protection check • Power Consumption < 2mA
Idle	• Slower voltage, temp. and current scan period (configuration through bit6:4 in EEPROM register 27h : 1~ 56s step:8s) • Safety protection check • Power consumption < 250uA
Sleep	• Stop voltage, temp. and current scan • Stop safety protection check • Most blocks are powered down, internal backup 3.3V and 2.5V(software mode) power supply enable • Power consumption < 50uA • Waiting for the wake up events: ➢ I2C bus active ➢ Sleep timer expires ➢ External SC event happens ➢ Charge/discharge occur

Transition Description (Fig. 7)

Transition	Initial State	Condition		Final State
		Hardware Mode	Software Mode	
1	Full Power	No charge/discharge and No protection event occurs for 5 minutes	uP makes decision	Idle
2	Idle	Charge/discharge or any protection event occurs	uP makes decision	Full Power
3	Idle	No charge/discharge and No protection event occurs for 10 minutes	uP makes decision	Sleep
4	Sleep	Any one of the Wake up events happens: ➢ I2C bus active ➢ Sleep timer expires ➢ External SC event happens ➢ Charge/discharge occur		Full Power
5	Full Power	If no event occurs after wakeup directly from the Sleep Mode	uP makes decision	Sleep

Internal Temperature Sensor

OZ890 takes advantage of silicon device physics and circuit design technology for the internal temperature sensor. The internal temperature sensor generates a voltage level which is proportional to the temperature. As Fig. 8 shows, with a temperature increase of 1°C, internal temperature sensor output voltage will increase by 2.0976mV. The internal temperature range is -40°C~120°C.

External Temperature Sensor

OZ890 provides 3 GPIO ports for external temperature detection, the application circuitry is shown in Fig. 9. These 2 external temperature measurement channels can be enabled by the ***ExtTCh1Enable*** and ***ExtTCh2Enable*** bits in the 32h EEPROM register. We recommend using 103 NTC type thermistor.

103 NTC Thermistor RT characteristics are shown in Fig. 10. The sensed voltage Vt characteristics are shown Fig. 11

For Example: Vt2=3.3V * RT2 / (RB2 + RT2)

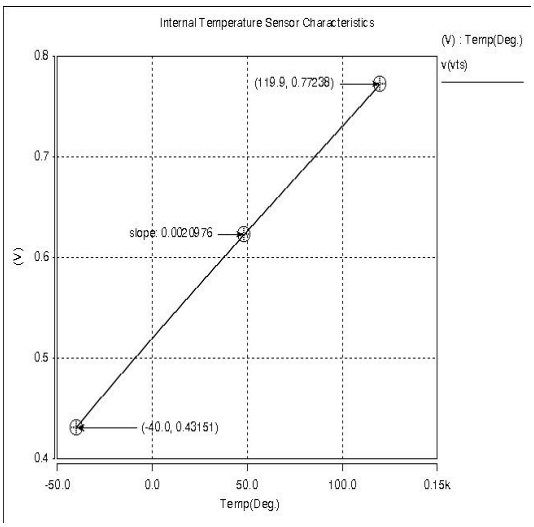


Fig.8 Internal Temperature Sensor Curve

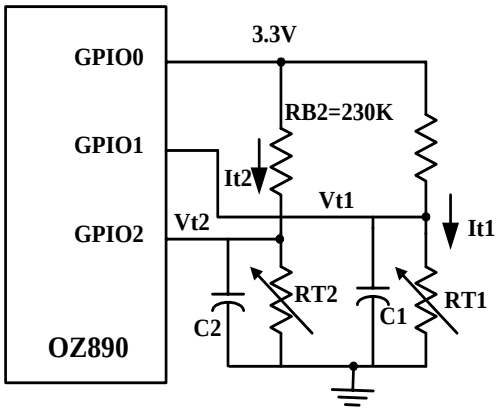


Fig.9 External Temperature Sensor Application

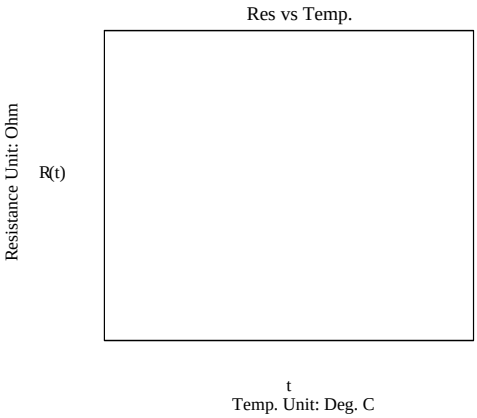


Fig.10 Thermistor RT characteristics

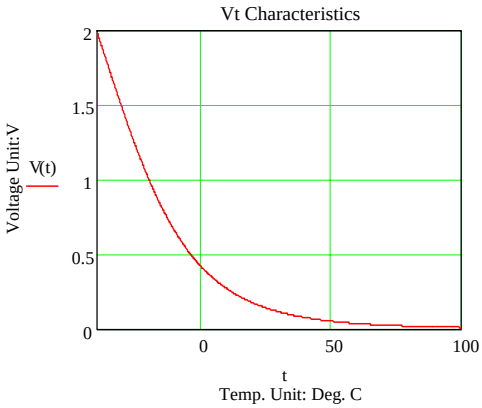


Fig.11 The sensed voltage Vt characteristics

Power MOSFET Driver Control

Patent pending smart MOSFET driver supports charge, pre-charge and PWM discharge. When working with uP, the discharge current can be controlled by pulse width of the discharge MOSFET control signal. The driver also supports parallel and series charge / discharge loop.

In hardware mode, the charge/discharge MOSFET is fully controlled by Battery Protection Engine (BPE) state machine. Refer to the “Battery Protection” section for detailed information.

In software mode, the charge and discharge MOSFETs are controlled through operation register 1eh, but if some error condition occurs, the hardware BPE will turn of the MOSFET regardless of the software control bit. OZ890 also provides a pin (EFETC) for external MOSFET control signal input or internal MOSFET control signal output. This makes the MOSFET control very flexible. The discharge (DSG) MOSFET gate-to-source voltage is clamped to 12V (typical) when FET is in ON state; the charge and pre-charge FET gate-to-source voltage is decided by external resistor divider and the pack voltage. (Please refer to the application circuits).

The PWM discharge frequency is configured by 2 bits in the operation register 1dh, bits[5:4]. The frequency range is 1kHz ~ 8kHz and the pulse width is 0 ~ 100%, which is controlled by 4 bits in operation register 1dh, bit[3:0]. The register bits can be configured by the uP when working in the Software Mode.

LED Error Indication

OZ890 can display the 5-level / 4-level battery capacity based on voltage gas gauge function. 5 or 4 LEDs are used for bar-graph display. When OV, UV, OT, UT, OC, SC event happens or authentication fails, the normal gas gauge display will be disabled; instead the related error message will be displayed. The following is protection events indication:

- OC or SC event happens,LED0 will blink at 1Hz;
- OV event happens,LED1 will blink at 1Hz;
- OT event happens,LED2 will blink at 1Hz;
- UT event happens,LED3 will blink at 1Hz;
- Authentication fails, LED2 and LED3 will blink at 1Hz.

Serial Communication Bus

OZ890 supports 3 kinds of serial bus protocol to communicate with external uP or host. In all cases, OZ890 chip acts as slave device.

BSEL1, BSEL0 (Pin30, Pin31)	Bus Type Description
2'b00	2-wire I2C bus
2'b01	4-wire I2C bus (unilateral bus)
2'b10	O2Micro defined Pbus serial bus protocol.
2'b11	Reserved for ATE test.

2-wire I2C Bus

In this case, Pin26 is input clock pin and the clock comes from external I2C host, Pin28 is the bi-directional data pin. For detailed I2C protocol and timing information, please refer to the I2C Specifications.

4-wire I2C Bus

In this case, Pin25 is the output clock pin (SCLO) and Pin26 is the input clock pin (SCL), Pin27 is the output data pin (SDAO), Pin28 is the input data pin (SDA). This bus protocol and timing is the same as 2-wire I2C bus except separating input/output line.

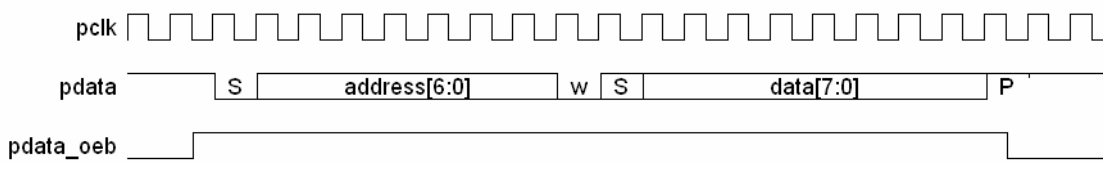
4-wire I2C bus is easy to work with external general purpose MCU / uP and opto-coupler, it will be useful in some non-common ground and/or noisy application.

PBus

PBus is O2Micro defined low-cost serial bus. It will work with O2Micro's uP solution.

There are 2 signals in the Pbus: one is clock signal PCLK; the other is bidirectional data signal PDATA.

The PCLK (Pin26) of Pbus is output from OZ890, so the synchronization between Pbus clock and the internal clock will be relatively simple.

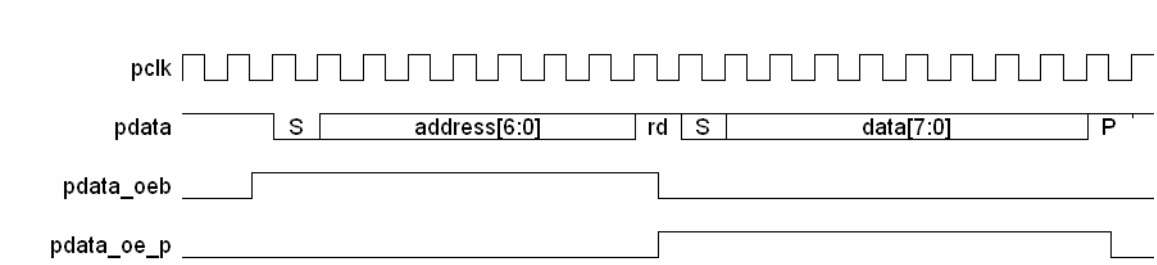


The above timing diagram is a write operation to a register in OZ890 from uP. The signal called pdata_oe_b is the output enable on PDATA pin on the uP side. "S" means start bit; "P" means stop bit.

The serial bus will be high when idle.

Reads and writes both begin with a “start” bit followed by 7 address bits, allowing 128 registers to be accessed. After the last address bit, the rd/wr# bit indicates the transfer direction (low for write, as shown above).

Following the rd/wr# bit is a second start bit, followed by 8 data bits. After the final data bit, a stop bit finishes the transfer. The transmitting device switches PDATA on the rising edge of PCLK. The receiving device can strobe the results on the falling edge of PCLK.



The above timing diagram is a read operation from a register in OZ890. The address byte is sent by the uP as before. In the middle of the rd/wr# bit, the uP tri-states its PDATA driver and OZ890 turns on its PDATA driver. The signal called pdata_oe_p is the output enable on PDATA pin in OZ890 side.

After the rd/wr# bit, the second start bit and data byte are driven by OZ890. The timing for read operation is identical to the timing for write operation. The “start” bit at the start of the data byte is a way to verify that OZ890 is responding to the read request. After the data byte has been transferred, OZ890 will disable its PDATA driver in the middle of the stop bit.

The uP can start another read or write transfer immediately after the stop bit. Each read or write takes 19 cycles of PCLK.

Password Verification Function

OZ890 has 128-byte internal EEPROM, which stores the important battery pack, battery cell, and OZ890 chip configuration information. In order to prevent that important information from accidentally being erased or illegally accessed. OZ890 provides the EEPROM “freeze” bits and password verification mechanism.

The EEPROM block erase function is limited. After the EEPROM freeze is set (if ate_freeze=1 or user_control=10 or user_control=11 or secret_freeze=1, we will say the EEPROM freeze is set; otherwise, the EEPROM freeze is not set), the EEPROM can not be block erased except any of the following case:

(1) bsel1, bsel0 = 11 (ATE test mode);
(2) the password verification is passed.

We can enter into ATE test mode to block-erase EEPROM. However this method needs pin changes (bsel1, bsel0=11), so we recommend the password verification method because we can block-erase the EEPROM via i2c interface without the pin re-configuration.

Registers Related to Password Verification:

(1) the 16-bit password is stored in EEPROM register 7ah and 7bh: Its access is controlled by the secret_freeze bit (EEPROM register 7fh, bit7). If the secret_freeze = 0, this password can be read; if the secret_freeze =1, this password cannot be read.

(2) 16-bit (2 bytes) password registers in operation register 69h and 6ah: the user can enter the password into these two registers for verification.

(3) 2-bit password verification status (password_ok, password_fail) bits in operation register 6fh, bit7:6: The user can check the password verification status by reading these two bits. Before password verification, password_ok=0, password_fail=0. The 2 bits are described in the following table:

2-bit password verification status	Description
password_ok=0, password_falil=0	The password verification is not completed.
password_ok=0, password_fail=1	The password verification has failed.
password_ok=1, password_fail=0	The password verification has passed.
password_ok=1, password_fail=1	Not possible

Password Verification Flow

(1) Set OZ890 into EEPROM mode by writing operation register 5fh, bit4=1, which will make the safety scan stop. This will make sure there is no EEPROM read request from safety scan in the password verification.

(2) The user enters the password into the password registers (operation register 69h and 6ah). OZ890 will record the times of the password entry.
In the first 8 times, if the entered password is matched with the password stored in the EEPROM, the password verification is ok (password_ok=1).
If the time = 8, no matched password is found, the password verification fails (password_fail=1). Once password_fail is set to "1", it will be kept until the power on reset. Note that the external reset pin will not clear the password entry time.

(3) Once the password verification is ok, the EEPROM can be block-erased.

(4) After the EEPROM is block-erased, then EEPROM block-read is needed to map the erased-EEPROM data (all are "0") into operation registers so that all the frozen bits (ATE freeze, user control, secret freeze bits) are cleared. As a result, the user can write the EEPROM registers freely. After user finishes the writing of the EEPROM registers, EEPROM block-read is needed again to map the new written EEPROM data into the operation registers.

It is noted that the EEPROM block read will clear the password_ok bit to "0", password entering time =0, the entered password =0. This mechanism will make sure that one time password verification OK will be valid only for one time EEPROM block-erase.

(5) Make OZ890 exit EEPROM mode by clearing operation register 5fh, bit4, which will make the safety scan run normally.

Authentication

For better safety, OZ890 provides the authentication mechanism for the charging operation and/or the discharging operation. The authentication is processed between OZ890 and the charger/load. If the authentication fails, OZ890 will turn off the charge/discharge MOSFET so that OZ890 cannot work with the unauthorized charger/load. To guarantee the security, OZ890 will check authentication data 2 times in one authentication cycle.

The basic authentication flow is as follows:

(1) Charger/load reads out the 16-bit random number from operation register 6bh and 6ch;

(2) Charger/load calculates the 16-bit authentication data with 16-bit random number using the authentication algorithm, which is the same as OZ890's internal algorithm specified by the 16-bit authentication code in EEPROM register 7ch and 7dh;

(3) Charger/load writes back the 16-bit calculated authentication data into OZ890 operation register 6dh and 6eh.

(4) OZ890 calculates the 16-bit authentication data internally using the same random number and compare with the charger/load write back authentication data in operation register 6dh and 6eh;

(5) If the authentication data is matched, then repeat step 1 to 4 another time. If the second authentication data also matches, then authentication passes; if any authentication data does not match, the authentication fails.

(6) For charge authentication, it starts at the beginning of the charging operation and the charger should finish the step 1 to 5 within 30 seconds. Otherwise, OZ890 will consider this as failed charge authentication and turn off the charge FET to stop charge.
For discharge authentication, it starts at the beginning of the discharging operation and the load should finish the step 1 to 5 within 30 seconds. Otherwise, OZ890 will consider this as failed discharge authentication and turn off the discharge FET to stop discharge.

Authentication function can be disabled, or only enabled for charge operation or only for discharge operation, or for both, which is configured by EEPROM register 7fh, bit1:0.

Deadman

OZ890 provides a dead man function to check the communication between external uP and OZ890 in software mode.

In the Software Mode, it should have a periodic handshake protocol between the uP and OZ890. When a successful handshake happens, the deadman timer is cleared. If the communication between OZ890 and software is blocked or the software hangs, the handshake protocol problem persists and the deadman timer expires, the deadman event occurs, then appropriate actions can be taken.

If the ***deadman reset enable*** bit is "1" in operation register 1ah, OZ890 will send out a 64ms low active pulse to RSTN pin to reset the external uP; if the ***deadman reset enable*** bit is "0" in operation register 1ah, then OZ890 will turn off all the MOSFETs and send out a PF signal and then shut down itself.

Operation register 1ah is the deadman control register, operation register 1bh is the deadman timer register.

In hardware mode, this deadman function is disabled.

EEPROM AND OPERATION REGISTERS MAP

OZ890 has 128-byte built-in EEPROM registers (00h-7fh) and 128-byte Operation registers (00h-7fh). EEPROM registers are used to store important battery pack, battery cell information and configure the OZ890 chip. Operation registers are used to store ADC instant data, OZ890 status information, and to control OZ890 state-machine, etc. When system is powered on, the data in EEPROM register 26h-33h, 7ch-7fh will be loaded into the Operation registers 06h-13h, 7ch-7fh respectively. Fig. 12 shows the configuration of EEPROM registers and Operation registers.

Serial Bus (I2C or PBus) can directly access Operation registers. It can also indirectly access EEPROM registers through Operation registers 5ch ~ 5fh.

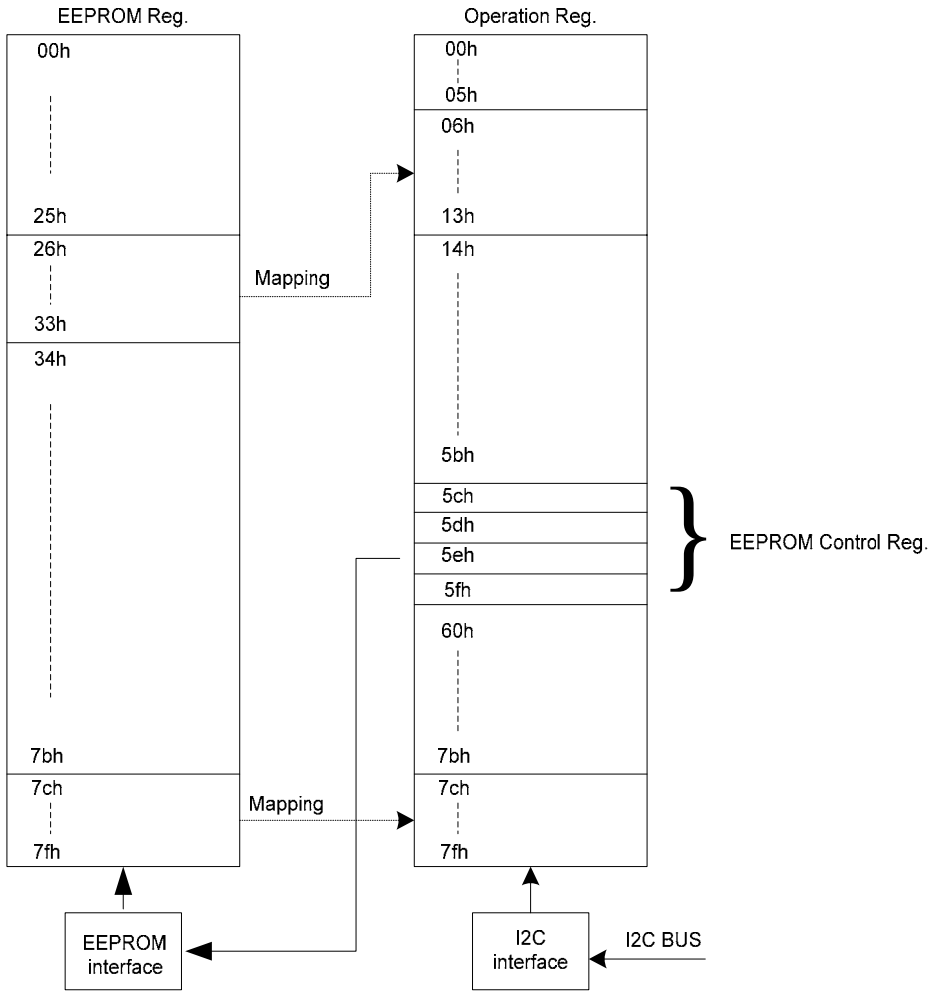


Fig. 12 Configuration of EEPROM Register and Operation Register

EEPROM Registers

EEPROM registers are used to store important battery pack, battery cell information, protection parameters, config OZ890 chip, etc.

EEPROM registers are divided into 3 sections. Each section has individual “freeze” bit to control the access limitation.

EEPROM Section	Description
00h~25h ATE data	This section reserved for O2Micro internal use only. Register 25h, bit7 is ate_freeze bit. ate_freeze =0: can read/write ATE data section ate_freeze =1: read only
26h~6fh User data	This section used for user control, programming data. 26h~33h are mapped into the Operation registers 06h~13h; 34h~6fh are not mapped into the Operation registers. Register 33h, bit7:6 is user_control bits: user_control = 00: the safety scan is disabled; user data section can be read/written; user_control = 01: the safety scan is enabled; user data section can be read/written; user_control = 10: the safety scan is enabled; user data section is read only; user_control = 11: the safety scan is enabled; 26h~33h registers and 46h~6fh registers can not be read/written; 34h~45h registers can be read, cannot be written.
70h~7fh Secret data	This section stores secret information, such as password, authentication code, etc. 70h~7bh are not mapped into the Operation registers. 7ch~7fh are mapped into the Operation registers 7ch~7fh. Register 7fh, bit7 is secret_freeze bit: secret_freeze = 0: secret data section can be read/written; secret_freeze = 1: secret data can’t be accessed at all.

Reg index (hex)	EEPROM Reg Name	Bit Number							
		7	6	5	4	3	2	1	0
00-25		Reserved							
26	Cell number	NiMH Vpack Check	Reserved	Battery type		Cell number			
27	Scan Rate	No sensor resistor	Scan Rate			Reserved	Efetc_shutdown_enable	EFETC mode	
28	OC charge Control	discharge current threshold config				OC config for charge			
29	OC discharge Control	charge current threshold config				OC config for discharge			
2a	OC delay	OC delay number						OC delay scale	
2b	SC Control	Reserved				SC config			
2c	SC delay	SC delay number						SC delay scale	

Reg index (hex)	EEPROM Reg Name	Bit Number							
		7	6	5	4	3	2	1	0
2d	SC, OC Release Control	Reserved		Disable oc_sc detect if no FET	select oc_sc time release	SC/OC release control			
2e	OT/UT, OV/UV Delay Control	OT/UT delay				OV/UV delay			
2f	PF control	Reserved	Pf_mosfet _enable	PFVH enable	PFVL enable	Pf delay			
30	I2c address config	Reserved10h_bit7	Reserved 10h_bit6	Reserved 10h_bit5	pec enable	I2c address config			
31	Reserved	Reserved							
32	Mode Control	Thermal2 enable	Thermal 1 enable	Reserved 12h_bit5	Reserved 12h_bit4	Reserved 12h_bit3	Reserved 12h_bit2	Reserved 12h_bit1	Hardware mode
33	Hardware bleeding	User data access control		Sleep state support	Precharge support	Bleeding support	Select external bleeding	Bleeding cell number config	
34~35	Reserved	Reserved							
36~3f	Factory Name	Factory Name(ASCII code)							
40~44	Project Name	Project Name(ASCII code)							
45	Version Number	Version Number							
46-47	Cell unbalance threshold	Cell unbalance threshold (13 bits)							
48	Bleeding Start's Voltage low byte	Bleeding Start's low byte (5bits)					Bleeding Accuracy		
49	Bleeding Start's Voltage high byte	Bleeding Start's high byte							
4a-4b	OV threshold value	OV threshold value (13 bits)							
4c-4d	OV release value	OV release value (13 bits)							
4e-4f	UV threshold value	UV threshold value (13 bits)							
50-51	UV release value	UV release value (13 bits)							
52-53	PFVH value	PFVH threshold value (13 bits)							
54-55	PFVL value	PFVL threshold value (13 bits)							
56-57	OTE threshold	OTE threshold value (13 bits)							
58-59	OTE release value	OTE release value (13 bits)							
5a-5b	UTE threshold	UTE threshold value (13 bits)							
5c-5d	UTE release value	UTE release value (13 bits)							
5e-5f	OTI threshold	OTI threshold value (13 bits)							
60-61	OTI release value	OTI release value (13 bits)							
62-63	UTI threshold	UTI threshold value (13 bits)							
64-65	UTI release value	UTI release value (13 bits)							

Reg index (hex)	EEPROM Reg Name	Bit Number							
		7	6	5	4	3	2	1	0
66-67	Gas-gauge V1 value	Gas-gauge V1 value (13 bits)							
68-69	Gas-gauge V2 value	Gas-gauge V2 value (13 bits)							
6a-6b	Gas-gauge V3 value	Gas-gauge V3 value (13 bits)							
6c-6d	Gas-gauge V4 value	Gas-gauge V4 value (13 bits)							
6e-6f	Gas-gauge V5 value	Gas-gauge V5 value (13 bits)							
70~79	Reserved	Reserved							
7a-7b	Password	16-bit password							
7c-7d	Authentication code	16-bit Authentication code							
7e	Reserved	Reserved							
7f	Authentication control	secret_freeze	reserved					auth_control	

Detailed EEPROM Register Information

Cell Number Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
26h	NiMH Vpack	Reserved	BTYP1	BTYP0	CNUM3	CNUM2	CNUM1	CNUM0

This register selects the cell number, battery type and controls the checking for NiMH battery.
Bit3 – Bit0 (CNUM3– CNUM0): These 3 bits specify the number of Li-ion cells in series in the battery pack:

CNUM3– CNUM0	Cell Count	CNUM3– CNUM0	Cell Count
0101	5	1010	10
0110	6	1011	11
0111	7	1100	12
1000	8	1101	13
1001	9	Others	Reserved

Bit5 - Bit4 (BTYP1–BTYP0): These 2 bits indicate battery type

BTYP1– BTYP0	Battery type
00	30S NiMH
01	20S NiMH
10	Phsophate Li-ion
11	Cobalt/Manganese Li-ion

Bit7: This bit is used to control the voltage checking for NiMH battery.
For 20S NiMH battery, if this bit is “1”, only vbat8 will be checked; if this bit is “0”, vbat4, vbat8 will be checked.

For 30S NiMH battery, if this bit is “1”, only vbat12 will be checked; if this bit is “0”, vbat4, vbat8, vbat12 will be check.

==========

Scan Rate Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
27h	NSR	Scan Rate2	Scan Rate1	Scan Rate0	Reserved	EFETC__SHDN_ENB	EFETC1	EFETC0

This register specifies the scan period and config EFETC pin function.

Bit1 – Bit0 (EFETC1– EFETC0): These 2 bits are used to define the EFETC pin’s function when EFETC__SHDN_ENB register bit is “0” as shown in the following table:

EFETC1– EFETC0	EFETC function
00	EFETC is an input pin. If EFETC is “1”, disable charge FET; if EFETC is “0”, the charge FET is controlled by the internal logic.
01	EFETC is an input pin. . If EFETC is “1”, disable discharge FET; if EFETC is “0”, the discharge FET is controlled by the internal logic.
10	EFETC is an input pin. If EFETC is “1”, disable charge FET and discharge FET; if EFETC is “0”, the charge FET and discharge FET are controlled by the internal logic.
11	EFETC is output pin. It will output the discharge FET control logic.

When EFETC__SHDN_ENB register bit is “1”, EFETC1 & EFETC0 are ignored.

Bit2: Enable EFETC pin as external shut down signal.

If “1”, enable EFETC pin as shut down pin (when EFETC is “1”, shut down OZ890; when EFETC is “0”, the system will work normally.);

if “0”, EFETC pin function controlled by the EFETC1 & EFETC0 bits.

Bit6-Bit4 (Scan Rate2– Scan Rate0): In hardware mode, these 3 bits are used to specify the scan period in idle state; in software mode, these 3 bits are used to specify the scan period, software can change the scan rate anytime. The detailes are shown in the following table:

Scan Rate2– Scan Rate0	Scan period
000	1s
001	8s
010	16s
011	24s
100	32s
101	40s
110	48s
111	56s

Bit7: This bit is used to indicate the sensor resistor presence. If “1”, means no sensor resistor is used; if “0”, means sensor resistor is used.

==========

OC Charge Control Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
28h	DCTC2	DCTC1	DCTC0	OCCFC4	OCCFC3	OCCFC2	OCCFC1	OCCFC0

This register sets the charge over current (COC) protection threshold and the current threshold for discharge.
Bit4 – Bit0 (OCCFC4 – OCCFC0): Configure the charge over current threshold.

Bit4 – Bit0	COC threshold	Bit4 – Bit0	COC threshold
00000 – 00101	Reserved	10000	60mV / Rs
00110	10mV / Rs	10001	65mV / Rs
00111	15mV / Rs	10010	70mV / Rs
01000	20mV / Rs	10011	75mV / Rs
01001	25mV / Rs	10100	80mV / Rs
01010	30mV / Rs	10101	85mV / Rs
01011	35mV / Rs	10110	90mV / Rs
01100	40mV / Rs	10111	95mV / Rs
01101	45mV / Rs	11000	100mV / Rs
01110	50mV / Rs	11001	105mV / Rs
01111	55mV / Rs	10010 – 11111	Reserved

Bit7 – Bit5 (DCTC2 – DCTC0): Define the discharge current threshold. When OZ890 detects current across sense resistor smaller than this threshold (discharge current is negative value), it will think system is in discharge state.

DCTC2 – DCTC0	discharge current threshold
000	-12mV/Rs
001	-24mV/Rs
010	-48mV/Rs
011	-72mV/Rs
100	-108mV/Rs
101	-144mV/Rs
110	-192mV/Rs
111	-250mV/Rs

Here, Rs is the sense resistor.
==========

OC Discharge Control Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
29h	CCTC1	CCTC0	OCCFD5	OCCFD4	OCCFD3	OCCFD2	OCCFD1	OCCFD0

This register sets the discharge over current (DOC) protection threshold and the charge current threshold.
Bit5 – Bit0 (OCCFD5 – OCCFD0): Configure the discharge over current threshold.

Bit5 – Bit0	DOC threshold	Bit5 – Bit0	DOC threshold
000000 – 000101	Reserved	100000	160mV / Rs
000110	30mV / Rs	100001	165mV / Rs
000111	35mV / Rs	100010	170mV / Rs
001000	40mV / Rs	100011	175mV / Rs
001001	45mV / Rs	100100	180mV / Rs
…	…	…	…
011011	135mV / Rs	110110	270mV / Rs
011100	140mV / Rs	110111	275mV / Rs
011101	145mV / Rs	111000	280mV / Rs
011110	150mV / Rs	111001	285mV / Rs
011111	155mV / Rs	111010 – 111111	Reserved

Bit7 – Bit6 (CCTC1 – CCTC0): Define the charge current threshold. When OZ890 detects current across sense resistor larger than this threshold, it will consider the system to be in charge state.

CCTC1 – CCTC0	charge current threshold
00	12 mV/Rs
01	24mV/Rs
10	48mV/Rs
11	120mV/Rs

==========

OC Delay Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2ah	OCDN4	OCDN3	OCDN2	OCDN1	OCDN0	OCDS2	OCDS1	OCDS0

This register sets over current delay time (for both DOC and COC).
Bit2 – Bit0 (OCDS2 – OCDS0): Define the OC delay unit as follows:

OCDS2 – OCDS0	OC delay unit
000	2ms
001	6ms
010	14ms
011	30ms
100	62ms
101	126ms
110	254ms
111	510ms

Bit7 – Bit3 (OCDN4 – OCDN0): Define the over current delay number as N+1 (N is the 5 bit value).
The OC delay time= (N+1) × (OC delay unit), so its range is 2ms~16.3s

==========

SC Control Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2bh	Reserved	Reserved	SCC5	SCC4	SCC3	SCC2	SCC1	SCC0

This register sets up the short circuit (SC) current threshold voltage.
Bit5 – Bit0 (SCC5 – SCC0): Set up the short circuit current threshold voltage.

Bit5 – Bit0	SC threshold	Bit5 – Bit0	SC threshold
000000 – 000010	Reserved	100000	340mV / Rs
000011	50mV / Rs	100001	350mV / Rs
000100	60mV / Rs	100010	360mV / Rs
000101	70mV / Rs	100011	370mV / Rs
000110	80mV / Rs	100100	380mV / Rs
000111	90mV / Rs	100101	390mV / Rs
001000	100mV / Rs	100110	400mV / Rs
001001	110mV / Rs	100111	410mV / Rs
,,,	…	…	…
011011	290mV / Rs	111001	590mV / Rs
011100	300mV / Rs	111010	600mV / Rs
011101	310mV / Rs	111011	610mV / Rs
011110	320mV / Rs	111100	620mV / Rs
011111	330mV / Rs	111101 – 111111	Reserved

==========

SC Delay Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2ch	SCDN4	SCDN3	SCDN2	SCDN1	SCDN0	SCDS2	SCDS1	SCDS0

This register sets short circuit delay time.
Bit2 – Bit0 (SCDS2 – SCDS0): Define the short circuit delay unit.

SCDS2 – SCDS0	SC delay unit
000	8us
001	16us
010	32us
011	64us
100	128us
101	256us
110	512us
111	1024us

Bit7 – Bit3 (SCDN4 – SCDN0): Define the short circuit delay number as N+1 (N is the 5 bits value).
The SC delay time= (N+1) × (SC delay unit), so its range is 8us~32.8ms.
==========

SC, OC Release Control Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2dh	Reserved	Reserved	Disable OC_SC	Select OC_SC TR	SC/OC RC3	SC/OC RC2	SC/OC RC1	SC/OC RC0

This register sets SC,OC release time and release method.
Bit3 – Bit0 (SC/OC RC3 – SC/OC RC0): Configure the SC/OC release time.
The release time = 0.5 + (N* 0.25) min, the range is 0.5min~4.25min.
Bit4 (Select OC_SC TR): Select the OC_SC release's method in hardware mode.
If set to "1", select the OC_SC time release method;
If set to "0", select the OC_SC external release method.
In software mode, this bit is ignored. The OC_SC release is decided by the software.

If the OC_SC time release method is selected, the SC, DOC and COC will be released after the time delay. If the OC_SC external release method is selected, the SC and DOC will be released by the SCRL signal from external, the COC still will be released after the time delay.
Bit5 (Disable OC_SC detect if no FET): If set to "1", we can save power by tuning off the over current and short circuit detectors when all FETs are open. If set to "0", Leave these detectors running at all times.
==========

OT/UT, OV/UV Delay Control Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2eh	OT/UT D3	OT/UT D2	OT/UT D1	OT/UT D0	OV/UV D3	OV/UV D2	OV/UV D1	OV/UV D0

This register sets OT/UT, OV/UV delay time.
Bit3 – Bit0 (OV/UV D3 – OV/UV D0): Configure the OV/UV delay time as follows:
OV/UV delay time = (N+1) × (scan cycles).
Bit7 – Bit4 (OT/UT D3 – OT/UT D0): Configure the OT/UT delay time as follows:
OT/UT delay time = (N+1) × (Temperature Scan Period, TSP).
==========

PF Control Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2fh	Reserved	PF_MOS_E	PFVH_E	PFVL_E	PF D3	PF D2	PF D1	PF D0

This register sets PF delay time and PF function enable/disable.

Bit3 – Bit0 (PF D3 – PF D0): Configure the PFVH/PFVL delay time.
PFVH/PFVL delay time = (2N+2) × (scan cycles). So, the PF delay is 2 ~ 32 scan cycles.
Bit4 (PFVL_E): Enable PFVL function if set to “1”.
Bit5 (PFVH_E): Enable PFVH function if set to “1”.
Bit6 (PF_MOS_E): Enable MOSFET fail detection function if set to “1”.
When this bit is “1”, if the charge MOSFET and the pre-charge MOSFET both are turned off, but the chip is in charge state (current > the charge current threshold), the MOSFET will be regarded as having failed; on the other hand, if the discharge MOSFET is turned off, but the chip is in discharge state (current < the discharge current threshold), the MOSFET will be regarded as having failed.
In hardware mode, if the MOSFET failure is detected for continuous times specified by the PF delay time, it will send out PF signal and shut down the system.
In software mode, once the MOSFET failure is detected, it will make alert_n active to inform the host, the host can read the corresponding event register and take the corresponding action.
==========

I2C Address Configure Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
30h	Reserved	Reserved	Reserved	PEC enable	I2C Addr3	I2C Addr2	I2C Addr1	I2C Addr0

This register sets up the OZ890 I2C address.
Bit3 – Bit0 (I2C Addr3 – I2C Addr0): Configure the I2C address.
The I2C address = 60h (7 bits) +2N (N: 0~15).
Bit4 (PEC enable): Enable PEC (packet error check) in I2C protocol if set to “1” (It is noted that when PEC enable bit is “1”, OZ890 only supports one-byte I2C PEC-write, one-byte I2C PEC-read; doesn’t support multi-byte I2C PEC-write, doesn’t support multi-byte I2C PEC-read; when PEC_enable bit is “0”, OZ890 can support one-byte I2C write without PEC, one-byte I2C read without PEC; also can support multi-byte I2C no-PEC write, multi-byte I2C no-PEC read.
==========

Mode Control Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
32h	T2E (RW)	T1E (RW)	Reserved	Reserved	Reserved	Reserved	Reserved	HM (R)

This register selects the working mode and enables the external temperature sensors.
Bit0 (HM): Select hardware mode or software mode.
If set to “1”, select hardware mode; if set to “0”, select software mode.
In hardware mode, all controls are handled by OZ890 chip; in software mode, many controls such as bleeding are handled by the external host.
Bit6 (T1E): Enable the first external temperature sensor (THERM1) check in hardware mode.
In hardware mode, if this bit is “1”, the first external temperature will be checked; if this bit is “0”, the first external temperature will not be checked. In software mode, this bit is ignored.
Bit7 (T2E): Enable the second external temperature sensor (THERM2) check in hardware mode.
In hardware mode, if “1”, enable to check the second external temperature; if “0”, disable to check the second external temperature. In software mode, this bit is ignored.
==========

Hardware Bleeding Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
33h	UC1 (R)	UC0 (R)	SS (RW)	PS (RW)	BS (RW)	SEB (RW)	BCNC1 (RW)	BCNC0 (RW)

Bit1 – Bit0 (BCNC1 – BCNC0): Specify the maximum simultaneously bleeding cell number for external bleeding. If internal bleeding is selected, these two bits are ignored, always just bleed the highest cell.

BCNC1 – BCNC0	Maximum bleeding cell number
00	1
01	2
10	3
11	4

Bit2 (SEB): Select the external bleeding or internal bleeding.
If "1", select the external bleeding function; if "0", select the internal bleeding.
Bit3 (BS): Enable bleeding function if set to "1", otherwise disabled.
Bit4 (PS): Enable pre-charge function if set to "1", otherwise disabled.
Bit5 (SS): Enable the sleep mode if set to "1". Otherwise, can't enter sleep mode.
Bit7 – Bit6 (UC1 – UC0): Configure the EEPROM user data section access limitation.

UC1 – UC0	Safety scan, access to user data
00	The safety scan is disabled; can read/write user data section
01	The safety scan is enabled; can read/write user data section
10	The safety scan is enabled; can read user data section but cannot write user data section.
11	The safety scan is enabled; cannot read/write user data section..

==========

Factory Name Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
36h-3fh	FN7	FN6	FN5	FN4	FN3	FN2	FN1	FN0

These 10 registers (10-byte) store user factory name (ASCII code). Name length can be up to 10 characters.

Project Name Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
40h-44h	PN7	PN6	PN5	PN4	PN3	PN2	PN1	PN0

These 5 registers (5-byte) store user project name (ASCII code). Name length can be up to 5 characters.

Version Number Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
45h	VNR7	VNR6	VNR5	VNR4	VNR3	VNR2	VNR1	VNR0

This register (1-byte) stores user version number.

==========

Cell Imbalance Threshold Value's Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
46h	CUT4	CUT3	CUT2	CUT1	CUT0	Reserved	Reserved	Reserved
47h	CUT12	CUT11	CUT10	CUT9	CUT8	CUT7	CUT6	CUT5

These 2 registers are used to specify the 13-bit cell unbalanced threshold voltage (-300mV ~ 5000mV). If the voltage difference between highest cell and lowest cell exceeds this threshold, OZ890 will generate PF signal. To disable this PF function, just fill a very large voltage value in these two registers.

==========

Bleeding Start's Low /High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
48h	BSV4	BSV3	BSV2	BSV1	BSV0	BA2	BA1	BA0
49h	BSV12	BSV11	BSV10	BSV9	BSV8	BSV7	BSV6	BSV5

These 2 registers set the bleeding start voltage and bleeding accuracy.
Bit2 – Bit0 (BA2 – BA0): Specify the bleeding accuracy.

BA2 – BA0	Bleeding accuracy
000	8*1.22 = 9.76mv
001	16*1.22 = 19.5mv
010	24*1.22 = 29.3mv
011	32*1.22 = 39.0mv
100	40*1.22 = 48.80mv
101	48*1.22 = 58.56mv
110	56*1.22 = 68.3mv
111	64*1.22 = 78.1mv

The cell bleeding will be ceased if the Vcell-max – Vcell-min < bleeding accuracy.
BSV12 – BSV0 : Specify the 13-bit bleeding start voltage (-300mV ~ 5000mV).

==========

OV Threshold Value's Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4ah	OVT4	OVT3	OVT2	OVT1	OVT0	Reserved	Reserved	Reserved
4bh	OVT12	OVT11	OVT10	OVT9	OVT8	OVT7	OVT6	OVT5

These 2 registers specify the 13-bit (OVT12 – OVT0) OV threshold voltage (-300mV ~ 5000mV).

==========

OV Release Value's Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4ch	OVR4	OVR3	OVR2	OVR1	OVR0	Reserved	Reserved	Reserved
4dh	OVR12	OVR11	OVR10	OVR9	OVR8	OVR7	OVR6	OVR5

These 2 registers specify the 13-bit (OVR12 – OVR0) OV release voltage (-300mV ~ 5000mV). User should set this OV release voltage lower than OV threshold voltage.

==========

UV Threshold Value's Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4eh	UVT4	UVT3	UVT2	UVT1	UVT0	Reserved	Reserved	Reserved
4fh	UVT12	UVT11	UVT10	UVT9	UVT8	UVT7	UVT6	UVT5

These 2 registers specify the 13-bit (UVT12 – UVT0) UV threshold voltage (-300mV ~ 5000mV).

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UV Release Value's Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
50h	UVR4	UVR3	UVR2	UVR1	UVR0	Reserved	Reserved	Reserved
51h	UVR12	UVR11	UVR10	UVR9	UVR8	UVR7	UVR6	UVR5

These 2 registers specify the 13-bit (UVR12 – UVR0) UV release voltage (-300mV ~ 5000mV). User should set this UV release voltage higher than UV threshold voltage.

==========

PFVH Value's Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
52h	PFVH4	PFVH3	PFVH2	PFVH1	PFVH0	Reserved	Reserved	Reserved
53h	PFVH12	PFVH11	PFVH10	PFVH9	PFVH8	PFVH7	PFVH6	PFVH5

These 2 registers specify the 13-bit (PFVH12 – PFVH0) PFVH voltage (-300mV ~ 5000mV). User should set this PFVH value higher than OV threshold voltage.

==========

PFVL Value's Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
54h	PFVL4	PFVL3	PFVL2	PFVL1	PFVL0	Reserved	Reserved	Reserved
55h	PFVL12	PFVL11	PFVL10	PFVL9	PFVL8	PFVL7	PFVL6	PFVL5

These 2 registers specify the 13-bit (PFVL12 – PFVL0) PFVL voltage (-300mV ~ 5000mV). User should set this PFVL value lower than UV threshold voltage.

==========

OTE Threshold Value's Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
56h	OTET4	OTET3	OTET2	OTET1	OTET0	Reserved	Reserved	Reserved
57h	OTET12	OTET11	OTET10	OTET9	OTET8	OTET7	OTET6	OTET5

These 2 registers specify the 13-bit external over temperature threshold voltage (-300mV ~ 2500mV). Please refer to "External Temperature Sensor" section.

OTE Release Value's Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
58h	OTER4	OTER3	OTER2	OTER1	OTER0	Reserved	Reserved	Reserved
59h	OTER12	OTER11	OTER10	OTER9	OTER8	OTER7	OTER6	OTER5

These 2 registers specify the 13-bit external over temperature release voltage (-300mV ~ 2500mV). Please refer to "External Temperature Sensor" section.

==========

UTE Threshold Value's Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5ah	UTET4	UTET3	UTET2	UTET1	UTET0	Reserved	Reserved	Reserved
5bh	UTET12	UTET11	UTET10	UTET9	UTET8	UTET7	UTET6	UTET5

These 2 registers specify the 13-bit external under temperature threshold voltage (-300mV ~ 2500mV). Please refer to "External Temperature Sensor" section.

UTE Release Value's Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5ch	UTER4	UTER3	UTER2	UTER1	UTER0	Reserved	Reserved	Reserved
5dh	UTER12	UTER11	UTER10	UTER9	UTER8	UTER7	UTER6	UTER5

These 2 registers specify the 13-bit external under temperature release voltage (-300mV ~ 2500mV). Please refer to “External Temperature Sensor” section.

==========

OTI Threshold Value’s Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5eh	OTIT4	OTIT3	OTIT2	OTIT1	OTIT0	Reserved	Reserved	Reserved
5fh	OTIT12	OTIT11	OTIT10	OTIT9	OTIT8	OTIT7	OTIT6	OTIT5

These 2 registers specify the 13-bit internal over temperature threshold voltage (-300mV ~ 2500mV). Please refer to “Internal Temperature Sensor” section.

OTI Release Value’s Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
60h	OTIR4	OTIR3	OTIR2	OTIR1	OTIR0	Reserved	Reserved	Reserved
61h	OTIR12	OTIR11	OTIR10	OTIR9	OTIR8	OTIR7	OTIR6	OTIR5

These 2 registers specify the 13-bit internal over temperature release voltage (-300mV ~ 2500mV). Please refer to “Internal Temperature Sensor” section.

==========

UTI Threshold Value’s Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
62h	UTIT4	UTIT3	UTIT2	UTIT1	UTIT0	Reserved	Reserved	Reserved
63h	UTIT12	UTIT11	UTIT10	UTIT9	UTIT8	UTIT7	UTIT6	UTIT5

These 2 registers specify the 13-bit internal under temperature threshold voltage (-300mV ~ 2500mV). Please reference to “Internal Temperature Sensor” section.

UTI Release Value’s Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
64h	UTIR4	UTIR3	UTIR2	UTIR1	UTIR0	Reserved	Reserved	Reserved
65h	UTIR12	UTIR11	UTIR10	UTIR9	UTIR8	UTIR7	UTIR6	UTIR5

These 2 registers specify the 13-bit internal under temperature release voltage (-300mV ~ 2500mV). Please refer to “Internal Temperature Sensor” section.

==========

Gauge V1’s Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
66h	GGVA4	GGVA3	GGVA2	GGVA1	GGVA0	Reserved	Reserved	Reserved
67h	GGVA12	GGVA11	GGVA10	GGVA9	GGVA8	GGVA7	GGVA6	GGVA5

These 2 registers specify the 13-bit Gauge V1 voltage (-300mV ~ 5000mV). Please refer to “Voltage Based Gas Gauge” section.

Gauge V2’s Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
68h	GGVB4	GGVB3	GGVB2	GGVB1	GGVB0	Reserved	Reserved	Reserved
69h	GGVB12	GGVB11	GGVB10	GGVB9	GGVB8	GGVB7	GGVB6	GGVB5

These 2 registers specify the 13-bit Gauge V2 voltage (-300mV ~ 5000mV). Please refer to “Voltage Based Gas Gauge” section.

Gauge V3’s Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6ah	GGVC4	GGVC3	GGVC2	GGVC1	GGVC0	Reserved	Reserved	Reserved
6bh	GGVC12	GGVC11	GGVC10	GGVC9	GGVC8	GGVC7	GGVC6	GGVC5

These 2 registers specify the 13-bit Gauge V3 voltage (-300mV ~ 5000mV). Please refer to "Voltage Based Gas Gauge" section.

Gauge V4's Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6ch	GGVD4	GGVD3	GGVD2	GGVD1	GGVD0	Reserved	Reserved	Reserved
6dh	GGVD12	GGVD11	GGVD10	GGVD9	GGVD8	GGVD7	GGVD6	GGVD5

These 2 registers specify the 13-bit Gauge V4 voltage (-300mV ~ 5000mV). Please refer to "Voltage Based Gas Gauge" section.

Gauge V5's Low/High Byte Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6eh	GGVE4	GGVE3	GGVE2	GGVE1	GGVE0	Reserved	Reserved	Reserved
6fh	GGVE12	GGVE11	GGVE10	GGVE9	GGVE8	GGVE7	GGVE6	GGVE5

These 2 registers specify the 13-bit Gauge V5 voltage (-300mV ~ 5000mV). Please refer to "Voltage Based Gas Gauge" section.

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Password Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
7ah	PWD7	PWD6	PWD5	PWD4	PWD3	PWD2	PWD1	PWD0
7bh	PWD15	PWD14	PWD13	PWD12	PWD11	PWD10	PWD9	PWD8

These 2 registers specify the 16-bit customer password for EEPROM block erase. Please refer to "Password Verification Function" section.

==========

Authentication Code Rregisters

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
7ch	ATHC7	ATHC6	ATHC5	ATHC4	ATHC3	ATHC2	ATHC1	ATHC0
7dh	ATHC15	ATHC14	ATHC13	ATHC12	ATHC11	ATHC10	ATHC9	ATHC8

These 2 registers specify the 16-bit authentication code (seed) for OZ890 internal CRC algorithm. Please refer to "Authentication" section.

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Authentication Control Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
7fh	STFRZ	Reserved					ATHCC1	ATHCC0

Bit1 – Bit0 (ATHCC1 – ATHCC0): Specify the authentication scope.

ATHCC1 – ATHCC0	Descriptioin
00	Disable charge authentication Disable discharge authentication
01	Enable charge authentication Disable discharge authentication
10	Disable charge authentication Enable discharge authentication
11	Enable charge authentication Enable discharge authentication

Bit7 (STFRZ): Freeze the EEPROM secret_data section if set to "1".

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OZ890 Operation Registers

OZ890 Operation registers store the instant ADC readings, OZ890 chip status information, etc. They also provide the control registers to control OZ890's operation.

Register index (hex)	Register Name	Bit Number							
		7	6	5	4	3	2	1	0
00h	Chip ID & Chip Revision	Chip ID				Chip revision			
01h	LDO25 enable	Reserved							LDO25 enable
02h 03h 04h 05h	Reserved	Reserved							
06h	Cell number	NiMH vpack only	Reserved	Battery type		Cell number			
07h	Scan Rate	No sensor resistor	Scan Rate			Reserved	Efetc_shut down_ena ble	EFETC_mode	
08h	OC charge control	discharge current threshold config				OC config for charge			
09h	OC discharge control	charge current threshold config				OC config for discharge			
0ah	OC Delay	OC delay number						OC delay scale	
0bh	SC control	reserved				SC config			
0ch	SC Delay	SC delay number						SC delay scale	
0dh	SC, OC Release Control	Reserved		Disable oc_sc detect if no FET	select oc_sc time release	SC/OC release control			
0eh	OT/UT, OV/UV Delay Control	OT/UT Delay				OV/UV Delay			
0fh	Pf control	Reserved	Pf_mosfet _enable	PFVH enable	PFVL enable	Pf delay			
10h	I2c address config	Reserved10h _bit7	Reserved 10h_bit6	Reserved _10h_bit5	pec enable	I2c address config			
11h	Reserved	Reserved							
12h	Mode Control	Thermal2 enable	Thermal1 enable	Reserved 12h_bit5	Reserved1 2h_bit4	Reserved1 2h_bit3	Reserved12 h_bit2	Reserv ed12h_ bit1	Hardware mode
13h	Hardware bleeding	user_control		sleep state support	Precharge_ support	Bleeding support	Select external bleeding	Bleeding cell number config	

Register index (hex)	Register Name	Bit Number							
		7	6	5	4	3	2	1	0
14h	Software sleep control	reserved				Sleep_expired_event	Integrator_wakeup_event	Sc_wakeup_event	sleep state
15h	Software shut down	Reserved			Cell unbalance	MOSFET fail event	PFVH event	PFVL event	Shut down
16h	OV/UV timer	Reserved			OV/UV timer				
17h	OT/UT timer	Reserved			OT/UT timer				
18h	OC Timer	Reserved		Over current timer					
19h	PF timer	Reserved		PF timer					
1ah	Deadman Control	Reserved				Deadman Reset enable	Deadman control		
1bh	Deadman Timer	Reserved	Clear timer	Deadman timer					
1ch	Reserved	Reserved							
1dh	PWM for discharge	Reserved		PWM frequency control		PWM duty control			
1eh	FET enable	Reserved					Precharge enable	Charge enable	Discharge enable
1fh	FET disable	Reserved		Under temp disable	Over temp disable	Short circuit disable	Over current disable	Under voltage disable	Over voltage disable
20h	charge/discharge state	Reserved				Hardware in charge	Hardware in discharge	Software In charge	Software In discharge
21h	Reserved	Reserved							
22h	Software Bleeding1	Bleeding cell's low byte							
23h	Software Bleeding2	TCLK frequency		Bleeding enable	Bleeding cell's high byte				
24h	ADC request	ADC resolution		Channel selection					
25h	ADC busy	ADC data resolution		Reserved					ADC busy
26h	ADC low data	Low byte of left-justified ADC data							
27h	ADC high data	High byte of left-justified ADC data							
28h	reserved	Reserved							
29h	reserved	Reserved							
2ah	Event Enable	scan event enable	adc event enable	Under Temperature event enable	Over Temperature event enable	Short circuit event enable	Over current event enable	Under voltage event enable	Over voltage event enable
2bh	Event	scan event	adc event	Under Temperature event	Over Temperature event	Short circuit event	Over current event	Under voltage event	Over voltage event

Register index (hex)	Register Name	Bit Number							
		7	6	5	4	3	2	1	0
2ch	1S timer	reserved	sc release	timer_1s					
2dh	GPIO mode	GP3 mode		GP3 ADC resolution		GP2 mode		GP1 mode	
2eh	GPI event & data	GP3 event	GP2 event	GP1 event	GP0 event	GP3 in	GP2 in	GP1 in	GP0 in
2fh	GPI event enable	GP3 event enable	GP2 event enable	GP1 event enable	GP0 event enable	Reserved			
30h	GPO enable & data	GP3 out enable	GP2 out enable	GP1 out enable	GP0 out enable	GP3 out	GP2 out	GP1 out	GP0 out
31h	Reserved	Reserved							
32h	Cell 1's low byte ADC data	Cell 1's low byte of left-justified ADC data					Reserved		
33h	Cell 1's high byte ADC data	Cell 1's high byte of left-justified ADC data							
34h	Cell 2's low byte ADC data	Cell 2's low byte of left-justified ADC data					Reserved		
35h	Cell 2's high byte ADC data	Cell 2's high byte of left-justified ADC data							
36h	Cell 3's low byte ADC data	Cell 3's low byte of left-justified ADC data					Reserved		
37h	Cell 3's high byte ADC data	Cell 3's high byte of left-justified ADC data							
38h	Cell 4's low byte ADC data	Cell 4's or Vbat4's low byte of left-justified ADC data					Reserved		
39h	Cell 4's high byte ADC data	Cell 4's or Vbat4's high byte of left-justified ADC data							
3ah	Cell 5's low byte ADC data	Cell 5's low byte of left-justified ADC data					Reserved		
3bh	Cell 5's high byte ADC data	Cell 5's high byte of left-justified ADC data							
3ch	Cell 6's low byte ADC data	Cell 6's low byte of left-justified ADC data					Reserved		
3dh	Cell 6's high byte ADC data	Cell 6's high byte of left-justified ADC data							

Register index (hex)	Register Name	Bit Number							
		7	6	5	4	3	2	1	0
3eh	Cell 7's low byte ADC data	Cell 7's low byte of left-justified ADC data					Reserved		
3fh	Cell 7's high byte ADC data	Cell 7's high byte of left-justified ADC data							
40h	Cell 8's low byte ADC data	Cell 8's or Vbat8's low byte of left-justified ADC data					Reserved		
41h	Cell 8's high byte ADC data	Cell 8's or Vbat8's high byte of left-justified ADC data							
42h	Cell 9's low byte ADC data	Cell 9's low byte of left-justified ADC data					Reserved		
43h	Cell 9's high byte ADC data	Cell 9's high byte of left-justified ADC data							
44h	Cell 10's low byte ADC data	Cell 10's low byte of left-justified ADC data					Reserved		
45h	Cell 10's high byte ADC data	Cell 10's high byte of left-justified ADC data							
46h	Cell 11's low byte ADC data	Cell 11's low byte of left-justified ADC data					Reserved		
47h	Cell 11's high byte ADC data	Cell 11's high byte of left-justified ADC data							
48h	Cell 12's low byte ADC data	Cell 12's or Vbat12's low byte of left-justified ADC data					Reserved		
49h	Cell 12's high byte ADC data	Cell 12's or Vbat12's high byte of left-justified ADC data							
4ah	Cell 13's low byte ADC data	Cell 13's low byte of left-justified ADC data					Reserved		
4bh	Cell 13's high byte ADC data	Cell 13's high byte of left-justified ADC data							
4ch	GPIO1's low byte ADC data	GPIO1's low byte of left-justified ADC data					Reserved		
4dh	GPIO1's high byte ADC data	GPIO1's high byte of left-justified ADC data							

Register index (hex)	Register Name	Bit Number							
		7	6	5	4	3	2	1	0
4eh	GPIO2's low byte ADC data	GPIO2's low byte of left-justified ADC data					Reserved		
4fh	GPIO2's high byte ADC data	GPIO2's high byte of left-justified ADC data							
50h	GPIO3's low byte ADC data	GPIO3's low byte of left-justified ADC data(5 bits for temperature sensor 3; 8 bits for hall voltage)							
51h	GPIO3's high byte ADC data	GPIO3's high byte of left-justified ADC data							
52h	Internal Temp's low byte ADC data	Internal Temperature sensor's low byte of left-justified ADC data					Reserved		
53h	Internal Temp's high byte ADC data	Internal Temperature sensor's high byte of left-justified ADC data							
54h	Current sensor's low byte ADC data	Current sensor's low byte of left-justified ADC data							
55h	Current sensor's high byte ADC data	Current sensor's high byte of left-justified ADC data							
56h	Group1 offset for Cell voltage	Group1 offset for cell voltage for calibration							
57h	Group 2 offset for cell voltage	Group2 offset for cell voltage for calibration							
58h	Group 3 offset for cell voltage	Group3 offset for cell voltage for calibration							
59h	GPIO offset for cell voltage	GPIO offset for calibration							
5ah	Current sensor offset for cell voltage	Current offset for calibration							
5bh	offset overflow	Reserved			Current offset overflow	GPIO offset overflow	Group3 offset overflow	Group2 offset overflow	Group1 offset overflow
5ch	EEPROM low byte data	ee writing data or read back data							

Register index (hex)	Register Name	Bit Number							
		7	6	5	4	3	2	1	0
5dh	EEPROM high byte data	ee writing data or read back data							
5eh	EEPROM address	Reserved		ee address					
5fh	EEPROM control	ee busy	Reserved	reserved	ee mode	ee op_code			
60h 61h 62h 63h 64h 65h 66h 67h 68h	Reserved	Reserved							
69h-6ah	Entered password	Entered password byte							
6bh-6ch	Authentication random number	Authentication random number's byte							
6dh-6eh	Authentication data	Authentication data's byte							
6fh	Password/Authentication Status	password_fail	Password_ok	Password busy	Reserved	auth_dischg_fail	auth_dischg_ok	auth_chg_fail	auth_chg_ok
70h~7bh	Reserved	Reserved							
7ch-7dh	Authentication code	Authentication code's low byte							
7eh	Reserved	Reserved							
7fh	Authentication control	secret_freeze	Reserved					auth_control	

Detailed Operation Register Information

Register 00h – Chip ID & Revision Register

Bit #	Name	Description	R/W	Default value
7:4	Chip ID	This indicates the chip ID of OZ890.	R	0h
3:0	Chip Revision	This indicates the chip revision of OZ890.	R	0h

Register 01h – LDO25 Enable Register

Bit #	Name	Description	R/W	Default value
7:1	Reserved	Reserved.	R	0
0	LDO25 enable	This bit is used to enable OZ890 internal 2.5V LDO output in software mode. In hardware mode, this bit is ignored.	RW	1

Register 06h – Register 13h

Operation Registers 06h-13h are mapped from EEPROM registers 26h – 33h during EEPROM block read. (During power up sequence, it will automatically have an EEPROM block read operation).
Please refer to "Detailed EEPROM Register information" section for detailed register definition.

Register 14h – Software Sleep Control Register

Bit #	Name	Description	R/W	Default value
7:4	Reserved	Reserved.	R	0h
3	sleep_expired_event	When the sleep timer is expired, this bit will be set to "1" and be kept until the software clears it by writing "1" into this bit. In sleep state, if any of sleep_expired_event, integrator_wakeup_event, sc_wakeup_event is found, the alert_n will be active to inform the software. In full power state or idle state, the above events will not make alert_n active.	RW	0h
2	integrator_wakeup_event	When the wakeup from wakeup integrator block is active, this bit will be set to "1" and be kept until the software clears it by writing "1" into this bit.	RW	0h
1	sc_wakeup_event	When the sc_wakeup signal is active, this bit will be set to "1" and be kept until the software clears it by writing "1" into this bit.	RW	0h
0	sleep request	In software mode, this bit can be set to "1" by the software to request the chip to enter sleep state (if no OV, OC, SC, OT, UT, PFVH, PFVL event), this sleep request bit set "1" will make the chip enter sleep state; if any of these events occurs, the chip will stay in full power mode even though sleep request bit is set to "1"); also this bit can be cleared to "0" by software to keep the chip in full power state. In hardware mode, this bit will be ignored.	RW	0h

Register 15h – Software Shut Down Register

Bit #	Name	Description	R/W	Default value
7:5	Reserved	Reserved.	R	0h
4	Cell unbalance	Indicates the cell imbalance error. If "1", cells are unbalanced; if "0", it's normal.	R	NA
3	MOSFET fail	Indicates the MOSFET fail error. If "1", MOSFET failure detected; if "0, it's normal.	R	NA
2	PFVH	Indicates the PFVH error. If "1", PFVH is detected; if "0", it's normal.	R	NA
1	PFVL	Indicates the PFVL error. If "1", PFVL is detected; if "0", it's normal.	R	NA

0	Software shut down	In software mode, the software can shut down the OZ890 by writing this register bit with "1". In hardware mode, this bit will be ignored.	RW	0h

Register 16h – OV/UV Timer Register

Bit #	Name	Description	R/W	Default value
7:5	Reserved	Reserved.	R	0h
4:0	OV/UV timer	This is the timer for the OV/UV event. Its unit is a scan cycle (in normal case, it is 1second).	R	NA

Register 17h – OT/UT Timer Register

Bit #	Name	Description	R/W	Default value
7:5	Reserved	Reserved.	R	0h
4:0	OT/UT timer	This is the timer for the OT/UT event. Its unit is a scan cycle (in normal case, it is 1second).	R	NA

Register 18h – OC Timer Register

Bit #	Name	Description	R/W	Default value
7:6	Reserved	Reserved.	R	0h
5:0	OC timer	This is the timer for the OC event. Its unit is OC delay unit defined in OC delay register (EEPROM register 2ah, bit2:0).	R	NA

Register 19h – PF Timer Register

Bit #	Name	Description	R/W	Default value
7:6	Reserved	Reserved.	R	0h
5:0	PF timer	This is the timer for the Permanent Fail event. Its unit is a scan cycle (in normal case, it is 1 second).	R	NA

Register 1ah – Deadman Control Register

Bit #	Name	Description	R/W	Default value
7:4	Reserved	Reserved.	R	0h
3	Deadman Reset enable	Enable the deadman reset function. If "1", when the deadman event occurs, the chip will assert a low active pulse to the RSTN pin to reset the external uP. If "0", when the deadman event occurs, the chip just turns off all MOSFETs and sends PF signal and then shuts down itself.	RW	0h
2:0	Deadman Control	These 3 bits specify the expiry time for the deadman timer. Mad Wid / Max Time Allowed 000 / Infinite(deadman check is disabled) 001 / 3 seconds 010 / 7 seconds 011 / 15 seconds 100 / 31 seconds >=101 / 63 seconds	RW	0h

Register 1ah is the deadman control register, register 1bh is the deadman timer register.

In hardware mode, the deadman check is disabled.
In software mode, OZ890 will increment the deadman timer every second when the safety scan is enabled. The host should check the deadman timer register regularly.
If the deadman check is enabled by writing a non-zero value to "deadman control" register, then the host is required to do the following within the specified time period:

- Check the deadman timer by reading the Operation register 1bh
- Write "1" into the bit 6 "clear timer" of Operation register 1bh to clear the deadman timer.

If the handshake between OZ890 and the host is normal, the host will clear the deadman timer before it expires. As a result, no deadman event will occur.
If the handshake has some problem, the host cannot clear the deadman timer in time, then the deadman timer will expired after the defined maximum time. In a result, the deadman event occurred. If the deadman reset enable bit is "1", the chip will send out a 64ms low active pulse to RSTN pin to reset the external uP; if the deadman reset enable bit is "0", the chip will turn off all the MOSFETs and send out a PF signal and then shut down itself.

It should be noted that when starting up the deadman check, it's possible to get a false deadman event. To avoid this problem, do the above handshake procedure immediately after writing a non-zero value to "deadman control".

Register 1bh – Deadman Timer Register

Bit #	Name	Description	R/W	Default value
7	Reserved	Reserved.	R	0h
6	Clear timer	If host writes "1" into this bit, the deadman timer will be cleared to "0". If host writes "0" into this bit, no effect on the deadman timer. If host reads this bit, it always reads as "0".	RW	0h
5:0	Deadman timer	Deadman timer and its unit is 1s.	RW	0h

Register 1dh – PWM Control for Discharge Register

Bit #	Name	Description	R/W	Default value
7:6	Reserved	Reserved.	R	0h
5:4	PWM frequency control	These 2 bits specify the PWM frequency in discharge state PWM frequency control: PWM frequency 2'b00: 1khz 2'b01: 2khz 2'b10: 4khz 2'b11: 8khz	RW	1h
3:0	PWM duty control	These 4 bits specify the PWM duty in discharge state PWM duty control: PWM duty(high active) 4'b0000: Always low(full off) 4'b0001: 6/32=18.8% high 4'b0010: 8/32=25% high 4'b0011: 10/32=31.3% high 4'b0100: 12/32=37.5% high 4'b0101: 14/32=43.8% high 4'b0110: 16/32=50% high 4'b0111: 18/32=56.3% high 4'b1000: 20/32=62.5% high 4'b1001: 22/32=68.8% high 4'b1010: 24/32=75% high 4'b1011: 26/32=81.3% high 4'b1100: 28/32=87.5% high 4'b1101: 30/32=93.8% high 4'b1110: 31/32=96.9% high 4'b1111: 100% high(full on)	RW	fh

Register 1eh – FET Enable Register

Bit #	Name	Description	R/W	Default value
7:3	Reserved	Reserved.	R	0h
2	PreCharge enable	In software mode, set to "1" to turn on the precharge FET if the safety check doesn't force the FET to off; set to "0" to unconditionally turn off the precharge FET. In hardware mode, this bit is ignored.	RW	0h
1	Charge enable	In software mode, set to "1" to turn on the charge FET if the safety check doesn't force the FET to off; set to "0" to unconditionally turn off the charge FET. In hardware mode, this bit is ignored.	RW	0h
0	Discharge enable	In software mode, set to "1" to turn on the discharge FET if the safety check doesn't force the FET to off; set to "0" to unconditionally turn off the discharge FET. In hardware mode, this bit is ignored.	RW	0h

Register 1fh – FET Disable Register

Bit #	Name	Description	R/W	Default value
7:6	Reserved	Reserved.	R	0h
5:0	Under temp disable, Over temp disable, Short circuit disable, Over current disable, Under voltage disable, Over voltage disable	Each of bits 5~0 will be set by the OZ890 in response to a persistent error event which will force one or more FETs to be OFF. This happens in response to the expiration of the associated event timer. The FET disable bits can only be cleared by the software writing a "1" to them in software mode; while the FET disable bits can be cleared automatically after some time when the corresponding events disappear in hardware mode. In general, the xx_disable bits will control the FETs as following table:	RW	0h

xx_disable bit	FETs control
Under temp disable =1	Disable charge FET, precharge FET.
Over temp disable =1 or Short circuit disable =1 or Over current disable = 1	Disable discharge FET, charge FET, precharge FET
Under voltage disable=1	Disable discharge FET
Over voltage disable=1	Disable charge FET, precharge FET

Register 20h – Charge/discharge State Register

Bit #	Name	Description	R/W	Default value
7:4	Reserved	Reserved.	RW	0h
3	Hardware in charge	In hardware mode, this bit indicates OZ890 is in charge state When OZ890 detects current across sense resistor larger than EEPROM register 29h defined charge current threshold, this bit will be set. This bit is read only.	R	NA
2	Hardware in discharge	In hardware mode, this bit indicates OZ890 is in discharge state. When OZ890 detects current across sense resistor smaller than EEPROM register 28h defined discharge current threshold (discharge current is negative), this bit will be set. This bit is read only.	R	NA
1	Software in charge	In software mode, this bit is used to specify the OZ890 is in charge state. "1" indicates OZ890 is in charge state; "0" indicates OZ890 is not in charge state. This bit will be updated only by the host. The internal logic will not change its value.	RW	0h
0	Software in discharge	In software mode, this bit is used to specify the OZ890 is in discharge state. "1" indicates OZ890 is in discharge state; "0" indicates OZ890 is not in discharge state. This bit only will be updated only by the host. The internal logic will not change its value.	RW	0h

Register 22h – Software Bleeding1 Register

Bit #	Name	Description	R/W	Default value
7:0	bleeding_cell's low byte	There 8 bits correspond to cell8~cell1 respectively for the software cell bleeding, for example, bit 7 is set to "1" to select cell 8 for bleeding; bit 0 is set to "1" to select cell1 for bleeding.	RW	0h

Register 23h – Software Bleeding2 Register

Bit #	Name	Description	R/W	Default value
7:6	TCLK frequency	When the external clock is used as working clock, these 2 bits indicate the clock's frequency. We need to prescale the clock. The TCLK frequency is as follows:	RW	0h

TCLK frequency	TCLK clock frequency
2'b00	512KHz
2'b01	1MHz

		2'b10 2MHz 2'b11 4MHz		
5	Bleeding enable	Enable the software bleeding when set to "1". In hardware mode, this bit will be ignored.	RW	0h
4:0	Bleeding_cell's high byte	There 5 bits correspond to cell 13~cell 9 respectively for the software cell bleeding. For example, bit 5 is set to "1" to select cell13 for bleeding; bit 0 is set to "1" to select cell 9 for bleeding.	RW	0h

Once cell bleeding has been turned on by host in software mode, it remains active until the host turns it off or until an error condition occurrs. Errors include over voltage, under voltage, over current, short circuit, over temperature, under temperature, etc.

Register 24h – ADC Request Register

Bit #	Name	Description	R/W	Default value
7:6	ADC resolution	Specify the ADC's resolution as following: 2'b00 13 bits 2'b01 14 bits 2'b10 15 bits 2'b11 16 bits	RW	0h
5:0	Channel selection	Select one of ADC channels as following: 6'b000000 No channel is selected 6'b000001 Cell1's voltage 6'b000010 Cell2's voltage 6'b000011 Cell3's voltage 6'b000100 Cell4's voltage 6'b000101 Cell5's voltage 6'b000111 Cell6's voltage 6'b000111 Cell7's voltage 6'b001000 Cell8's voltage 6'b001001 Cell9's voltage 6'b001010 Cell10's voltage 6'b001011 Cell11's voltage 6'b001100 Cell12's voltage 6'b001101 Cell13's voltage 6'b001110 GPIO1's voltage 6'b001111 GPIO2's voltage 6'b010000 GPIO3's voltage 6'b010001 Internal temperature's voltage 6'b010010 Current sensor's voltage 6'b010011 Group1's 0v voltage(s1p, s2n are active at the same time) 6'b010100 Group2's 0v voltage(s6p, s7n are active at the same time) 6'b010101 Group3's 0v voltage(s10p, s11n are active at the same time) 6'b010110 Voltage ADC only 0v voltage 6'b010111 Current sensor's 0v voltage 6'b011000 0.6v reference for cell voltage offset calculation 6'b011001 2.1v reference for cell voltage offset calculation. 6'b011010 0.6v reference for GPIO voltage offset calculation. 6'b011011 2.1v reference for GPIO voltage offset calculation. 6'b011100 VR105 reference for GPIO voltage offset calculation. 6'b011101 VR12 reference for GPIO voltage offset calculation.	RW	00h

		6'b011110	Vbat12's voltage		
		6'b011111	Vbat8's voltage		
		6'b100000	Vbat4's voltage		
		Others	Reserved		

Except the regular current, cell voltages, temperature scan during regular ADC scan cycle, OZ890 still reserves the time slot for the host requested ADC channel measurements in software mode. Refer to "Time Slot in Different Configuration" section for detail. The host can send the request to do the ADC measurement for any channel at specified resolution. The measurement result is stored in Operation register 26h & 27h.

Register 25h – ADC Busy Register

Bit #	Name	Description	R/W	Default value
7:6	ADC data resolution	Indicate the ADC data resolution of Operation register 26h and 27h.	R	00h
5:1	Reserved	Reserved.	R	00h
0	ADC busy	If the ADC's request from host is not completed, this bit is high; if the ADC's request from host is done, this bit is low.	R	0h

Register 26h – ADC Low Data Register

Bit #	Name	Description	R/W	Default value
7:0	ADC low data	Low byte of left-justified ADC data	RW	00h

Register 27h – ADC High Data Register

Bit #	Name	Description	R/W	Default value
7:0	ADC high data	High byte of left-justified ADC data	RW	00h

Register 2ah – Event Enable Register

Bit #	Name	Description	R/W	Default value
7	scan event enable	Enable scan event to trigger the interrupt signal alert_n if set to "1"	RW	0h
6	adc event enable	Enable ADC event to trigger the interrupt signal alert_n if set to "1"	RW	0h
5	Under temperature event enable	Enable UT event to trigger the interrupt signal alert_n if set to "1"	RW	0h
4	over temperature event enable	Enable OT event to trigger the interrupt signal alert_n if set to "1"	RW	0h
3	Short circuit event enable	Enable SC event to trigger the interrupt signal alert_n if set to "1"	RW	0h
2	Over current event enable	Enable OC event to trigger the interrupt signal alert_n if set to "1"	RW	0h
1	Under voltage event enable	Enable UV event to trigger the interrupt signal alert_n if set to "1"	RW	0h
0	Over voltage event enable	Enable OV event to trigger the interrupt signal alert_n if set to "1"	RW	0h

Register 2bh – Event Register

Bit #	Name	Description	R/W	Default value
7	scan event	When an ADC scan is completed, this bit will be set to "1". Once this bit is set to "1", it will be kept until host clears it by writing "1" into this bit.	RW	0h
6	ADC event	When the ADC request from host is completed, this bit will be set to "1". And it will remain as "1" until host clear it by writing "1" into this bit.	RW	0h
5	Under temp event	Once under temperature event happens, this bit will be set to "1". And it will remain as "1" until host clears it by writing "1" into this bit.	RW	0h
4	Over temp event	Once over temperature event happens, this bit will be set to "1". And it will remain as "1" until host clears it by writing "1" into this bit.	RW	0h
3	Short circuit event	Once short circuit event happens, this bit will be set to "1". And it will remain as "1" until host clears it by writing "1" into this bit.	RW	0h
2	Over current event	Once over current event happens, this bit will be set to "1". And it will remain as "1" until host clears it by writing "1" into this bit.	RW	0h
1	Under voltage event	Once under voltage event happens, this bit will be set to "1". And it will remain as "1" until host clears it by writing "1" into this bit.	RW	0h
0	Over voltage event	Once over voltage event happens, this bit will be set to "1". And it will remain as "1" until host clears it by writing "1" into this bit.	RW	0h

Register 2ch – 1S Counter Register

Bit #	Name	Description	R/W	Default value
7	reserved	Reserved.	R	0
6	sc release	Short circuit release signal from SCRL pin. In software mode, software can use this information to release the FETs after OC/SC event.	R	NA
5:0	timer_1s	This timer will be used by the software to calculate the gas gauge. If the scan event enable bit is "1", it will increase 1 per second; and it will be cleared to "0" after host reads it and restarts to do the incremental operation. If the scan event enable bit is "0", this timer remains zero.	R	NA

Register 2dh – GPIO Mode Register

Bit #	Name	Description	R/W	Default value
7:6	GP3 mode	In software mode, select GP3 mode; in hardware mode, these bits are ignored. The mode selection function is as follows:	RW	0h

GP3 mode	GP3 function
2'b00	Normal ADC channel analog input which is not in scan cycle.
2'b01	Temperature ADC channel analog input.
2'b10	General purpose digital input/output.
2'b11	Normal ADC channel analog input which is enabled to scan as a special 16-bit ADC channel. And in this mode, the current sensor channel is disabled in scan cycle. This mode is useful for other current detection device, like Hall Effect device to detect current.

Bit #	Name	Description	R/W	Default value
5:4	GP3 ADC resolution	In software mode, these 2 bits select the GP3 ADC scan resolution when GP3 mode is 2'b11. In hardware mode, these bits are ignored. GP3 / GP3 ADC resolution when GP3 is scanned 2'b00 / 13bit 2'b01 / 14bit 2'b10 / 15bit 2'b11 / 16bit		
3:2	GP2 mode	In software mode, select GP2 mode; in hardware mode, these bits are ignored. The mode selection function is as follows: GP2 mode / GP2 function 2'b00 / Normal ADC channel analog input which is not in the scan cycle. 2'b01 / Temperature ADC channel analog input. 2'b10 / General purpose digital input/output. 2'b11 / Reserved.	RW	0h
1:0	GP1 mode	In software mode, select GP1 mode; in hardware mode, these bits are ignored. The mode selection function is as follows: GP1 mode / GP1 function 2'b00 / Normal ADC channel analog input which is not in the scan cycle. 2'b01 / Temperature ADC channel analog input. 2'b10 / General purpose digital input/output. 2'b11 / Reserved.	RW	0h

Register 2eh – GPIO Event & Data Register

Bit #	Name	Description	R/W	Default value
7	GP3 event	When GPIO3 data in has a change, gp3 event will be set to "HIGH". And then it is kept to "HIGH" until software clears it by writing "1" into this bit.	RW	0h
6	GP2 event	When GPIO2 data in has a change, gp2 event will be set to "HIGH". And then it is kept to "HIGH" until software clears it by writing "1" into this bit.	RW	0h
5	GP1 event	When GPIO1 data in has a change, gp1 event will be set to "HIGH". And then it is kept to "HIGH" until software clears it by writing "1" into this bit.	RW	0h
4	GP0 event	When GPIO0 data in has a change, gp0 event will be set to "HIGH". And then it is kept to "HIGH" until software clears it by writing "1" into this bit.	RW	0h
3	GP3 in	GPIO3 data in. When GP3 mode is 2'b10 (general purpose digital input/output), its data is from the GPIO3 pin; other wise, it is always 0.	R	NA
2	GP2 in	GPIO2 data in. When GP2 mode is 2'b10, its data is from the GPIO2 pin; other wise, it is always 0.	R	NA
1	GP1 in	GPIO1 data in When GP1 mode is 2'b10, its data is from the GPIO1 pin; other wise, it is always 0.	R	NA
0	GP0 in	GPIO0 data, its data is from the GPIO0 pin; other wise, it is always 0.	R	NA

Register 2fh – GPI Event Enable Register

Bit #	Name	Description	R/W	Default value
7	GP3 event enable	Enable GPIO3 event to trigger the interrupt signal alert_n if set to “1”	RW	0h
6	GP2 event enable	Enable GPIO2 event to trigger the interrupt signal alert_n if set to “1”	RW	0h
5	GP1 event enable	Enable GPIO1 event to trigger the interrupt signal alert_n if set to “1”	RW	0h
4	GP0 event enable	Enable GPIO0 event to trigger the interrupt signal alert_n if set to “1”	RW	0h
3:0	Reserved	Reserved.	R	0h

Register 30h – GPO Enable & Data Register

Bit #	Name	Description	R/W	Default value
7	GP3 out enable	Enable the GPIO3 output if set to “1”.	RW	0h
6	GP2 out enable	Enable the GPIO2 output if set to “1”.	RW	0h
5	GP1 out enable	Enable the GPIO1 output if set to “1”.	RW	0h
4	GP0 out enable	Enable the GPIO0 output if set to “1”.	RW	0h
3	GP3 out	GPIO3 output data.	RW	0h
2	GP2 out	GPIO2 output data.	RW	0h
1	GP1 out	GPIO1 output data.	RW	0h
0	GP0 out	GPIO0 output data.	RW	0h

Register 32h~4bh – Cell Voltage ADC Data Register

These registers store the cell1~cell13's ADC data. cell4 and vbat4 share the same ADC registers; cell8 and vbat8 share the same ADC registers; cell12 and vbat12 share the same ADC registers.
The cell1~cell5's ADC data are the adjusted value with the related offset register (56h); the cell6~cell9's ADC data are the adjusted value with the related offset register(57h); the cell10~cell13's ADC data are the adjusted value with the related offset register(58h).

Register 4ch~51h – GPIO ADC Data Register

These registers store the 3 GPIOs' ADC data.
The ADC data are the adjusted value with the related offset register (59h).

Register 52h~53h – Internal Temperature ADC Data Register

These registers store the internal temperature's ADC data.

Register 54h~55h – Current Sensor ADC Data Register

These registers store the current sensor's ADC data. The ADC data is the adjusted value with the related offset register (5ah).

Register 56h~5ah – Offset for Calibration Register

These registers store the offset's data for voltage and current calibration. Register 56h is the offset of the group1 cell voltages; Register 57h is the offset of the group2 cell voltages; Register 58h is the offset of the group3 cell voltages; Register 59h is the offset of the GPIO channels; Register 5ah is the offset of the current sensor channel.

For register 56h~58h, offset = N*5/(2^12)v = N*0.00122v=N*1.22mv (N:-128~127).
For register 59h, offset = N*2.5v/(2^12) = N*0.00061v=N*0.61mv (N:-128~127);
For register 5ah, offset = N*250mv/(2^15) (N:-128~127);

In hardware mode, OZ890 will do ADC offset calibration every 30 minutes.
In software mode, OZ890 will not do ADC offset calibration automatically, instead, the host can request to do the ADC offset measurement by writing the corresponding registers and get the values, then write the offset value into the corresponding registers.

Register 5b – Offset Overflow Register

Bit #	Name	Description	R/W	Default value
7:5	Reserved	Reserved.	R	0h
4	Current offset overflow	"1" indicates the current's offset is overflow; "0" indicates the current's offset is normal.	R	0h
3	GPIO offset overflow	"1" indicates the GPIO's offset is overflow; "0" indicates the GPIO's offset is normal.	R	0h
2	Group3 offset overflow	"1" indicates the group3's offset is overflow; "0" indicates the group3's offset is normal.	R	0h
1	Group2 offset overflow	"1" indicates the group2's offset is overflow; "0" indicates the group2's offset is normal.	R	0h
0	Group1 offset overflow	"1" indicates the group1's offset is overflow; "0" indicates the group1's offset is normal.	R	0h

When overflow happens, the offset value exceeds OZ890's defined range. In this case, OZ890 will assign the maximum or minimum offset value to the related offset register.

Register 5ch – EEPROM Low Byte Data Register

When writing word into EEPROM, this register is used to store the low byte of the writing data; when a word is read from the EEPROM, this register is used to store the low byte of the word that is read back.
When writing a byte into the EEPROM, this register is used to store the writing data.

Register 5dh – EEPROM High Byte Data Register

When writing a word into the EEPROM, this register is used to store the high byte of the writing data; when a word is read from the EEPROM, this register is used to store the high byte of the word that is read back. When writing a byte into the EEPROM, this register is not used.

Register 5eh – EEPROM Address Register

Bit #	Name	Description	R/W	Default value
7	Reserved	Reserved.	R	0h
6:0	ee_address	ee_address[6:1] are used to specify the EEPROM's word address. For byte write, ee_address[0] is used to specify the high or low byte. If "0", select the low byte; if "1", select the high byte.	RW	0h

Register 5fh – EEPROM Control Register

Bit #	Name	Description	R/W	Default value
7	ee_busy	This bit is high indicating the EEPROM is being accessed. After the access, it is low. Only when this bit is low, the host can start another EEPROM access.	R	0h
6:5	Reserved	Reserved.	R	0h
4	ee_mode	This bit selects EEPROM mode. If set to "1", select EEPROM mode; if set to "0", select non-EEPROM mode. In EEPROM mode, host can access the EEPROM and the ADC safety scan is disabled. In non-EEPROM mode, software cannot access the EEPROM and the safety scan is enabled.	RW	0h
3:0	ee op code	Specify the EEPROM access operation as follows:	RW	0h

ee_op_code	Accesses
4'b0000	no access
4'b0001	Word erase
4'b0010	Word write
4'b0011	Block erase
4'b0100	Block Write
4'b0101	Normal read
4'b0110	Internal high test read
4'b0111	Internal low test read
4'b1000	External high test read
4'b1001	External low test read
4'b1010	Block read
4'b1011	Byte write
Others	Reserved

Register 69h, 6ah – Entered password's low/high byte registers

These 2 registers are used for password verification. User can enter the password into these 2 registers for verification. After EEPROM block read (mapping EEPROM data into internal registers), these 2 registers will be cleared.

Register 6bh, 6ch – Authentication random number's low/high byte registers

These 2 registers are read only. They are used for authentication calculation.

Register 6dh, 6eh – Authentication data's low/high byte registers

These 2 registers are used to load the authentication data. User can enter the authentication data into these two registers for the authentication process.

Register 6fh – Authentication Status Register

<table>
<tr><th>Bit #</th><th>Name</th><th>Description</th><th>R/W</th><th>Default value</th></tr>
<tr><td>7</td><td>password_fail</td><td rowspan="2">Indicate the password verification status:
<table><tr><th>Register bits</th><th>Description</th></tr><tr><td>password_fail =0,
password_ok=0</td><td>Password verification is not completed.</td></tr><tr><td>password_fail=0,
password_ok=1</td><td>Password verification is OK</td></tr><tr><td>password_fail=1,
password_ok=0</td><td>Password verification is failed</td></tr><tr><td>Password_fail=1,
password_ok=1</td><td>No possible</td></tr></table></td><td>R</td><td>0h</td></tr>
<tr><td>6</td><td>password_ok</td><td>R</td><td>0h</td></tr>
<tr><td>5</td><td>Password_busy</td><td>“1” indicates the password verification is being processed; “0” indicates no password verification is being processed.</td><td></td><td></td></tr>
<tr><td>4</td><td>Reserved</td><td>Reserved.</td><td>R</td><td>0h</td></tr>
<tr><td>3</td><td>auth_dischg_fail</td><td rowspan="2">Indicate the discharge authentication status:
<table><tr><th>Discharge authentication status</th><th>Description</th></tr><tr><td>auth_dischg_fail=0,
auth_dischg_ok=0</td><td>The discharge authentication is uncompleted. When the discharge current is detected, the discharge authentication cycle will be started.</td></tr><tr><td>auth_dischg_fail=0,
auth_dischg_ok=1</td><td>The discharge authentication is passed.</td></tr><tr><td>auth_dischg_fail=1,
auth_dischg_ok=0</td><td>The discharge authentication is failed.</td></tr><tr><td>auth_dischg_fail=1,
auth_dischg_ok=1</td><td>No possible.</td></tr></table></td><td>R</td><td>0h</td></tr>
<tr><td>2</td><td>auth_dischg_ok</td><td>R</td><td>0h</td></tr>
<tr><td>1</td><td>auth_chg_fail</td><td rowspan="2">Indicate the charge authentication status:
<table><tr><th>Charge authentication status</th><th>Description</th></tr><tr><td>auth_chg_fail=0,
auth_chg_ok=0</td><td>The charge authentication is uncompleted. When the charge current is detected, the charge authentication cycle will be started.</td></tr><tr><td>auth_chg_fail=0,
auth_chg_ok=1</td><td>The charge authentication is passed.</td></tr><tr><td>auth_chg_fail=1,
auth_chg_ok=0</td><td>The charge authentication is failed.</td></tr><tr><td>auth_chg_fail=1,
auth_chg_ok=1</td><td>No possible.</td></tr></table></td><td>R</td><td>0h</td></tr>
<tr><td>0</td><td>auth_chg_ok</td><td>R</td><td>0h</td></tr>
</table>

Register 7ch – Register 7fh

Operation Registers 7ch-7fh are mapped to EEPROM registers 7ch – 7fh during EEPROM block read. (During power up sequence, it will automatically have an EEPROM block read operation).
Please refer to “Detailed EEPROM Register information” section for detailed register definition.

User Configurable Parameters

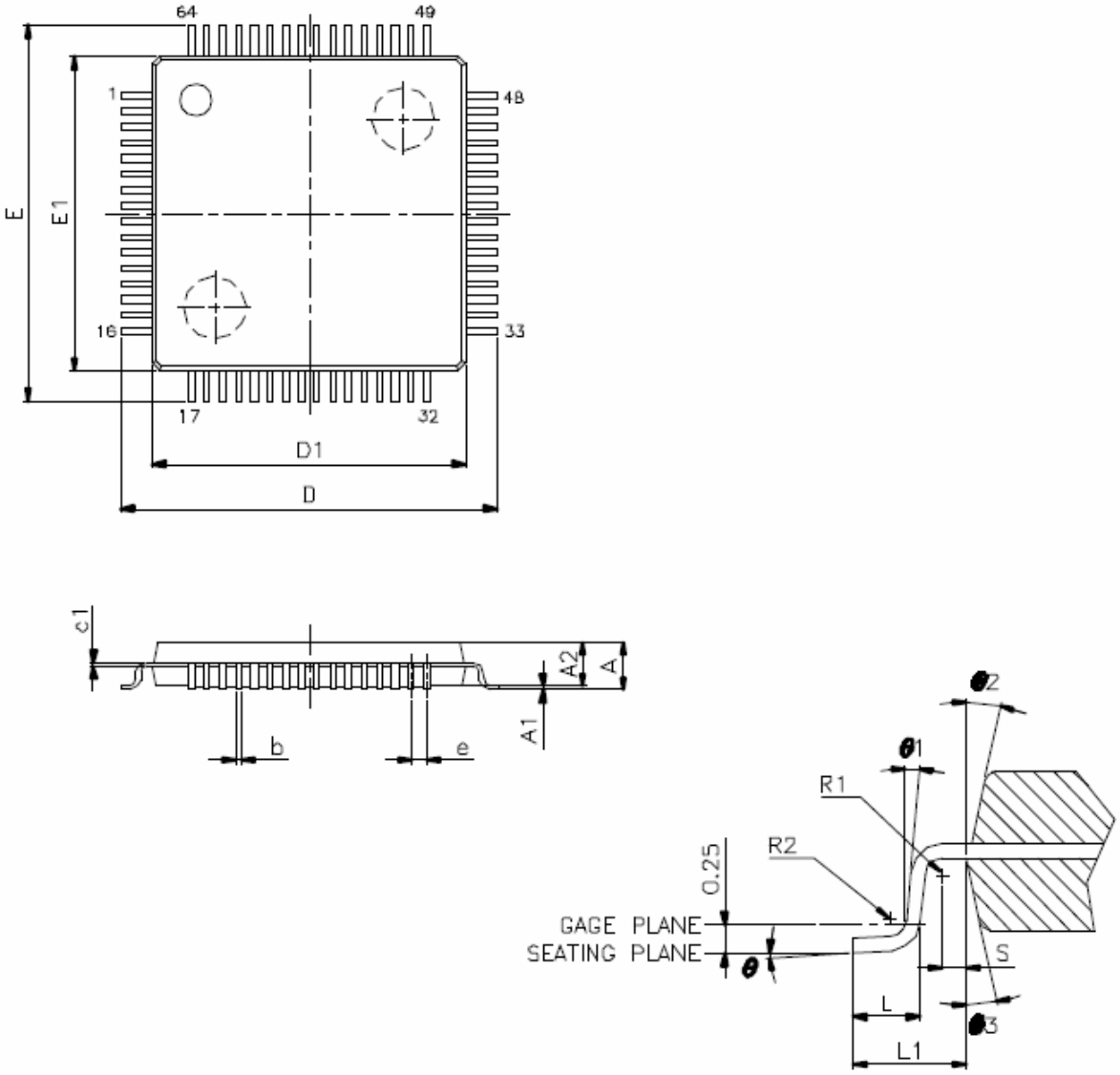
In order to make OZ890 work normally and protect the battery pack, user should configure EEPROM registers correctly. Instead of setting EEPROM registers in recondite binary code, O2Micro developed a software utility (Cowboy) to help end user configure the EEPROM registers easily understandable, intuitive engineering parameters.

Group	Name	Units/Steps/Values	Description
Battery Setting	*BatteryType*	20-NiMH in series	To set the Battery type , support NiMH and Li-Battery
		30-NiMH in series	
		Phosphor Li-ion	
		Cobalt/Manganese	
	CellNumber	5-13 Li battery in series	To set the number of the battery Pack cells
	NiMHVpackOnly		In NiMH application, only measure the voltage of the battery pack
Mode	*HWMode*		Hard/Software Mode selection
I2C Configuration	*I2CAddress*	N : 4 bits, Addr: 60h+2*N Support up to 16 devices	I2C address setting
	PECEnable		Enable packet error check based on I2C protocol
Options	*PreCHGEnable*		Pre-charge function enable
	Rsense	mOhm	The value of the sense resistor (Rs)
Idle Mode Configuration	*CHGCurrentTH*	12mV/Rs-120mV/Rs	Charge current threshold
	DSGCurrentTH	-12mV/Rs- -250mV/Rs	Discharge current threshold
	IdleScanRate	1,8,16,24,32,40,48,56 seconds	To Specify the protection scan period in Idle Mode
Sleep Mode Configuration	*SleepEnable*		Enable the sleep mode
	SleepTime	0-15 Minutes step:1 Min	To select the period of sleep mode, after every sleep interval the chip will do protection scan
OC/SC Configuration	*CHGOverCurrentTH*	10mV/Rs-105mV/Rs with step of 5mV/Rs	Charge over current threshold
	DSGOverCurrentTH	30mV/Rs-285mV/Rs with step of 5mV/Rs	Discharge over current threshold
	OverCurrentDelay	2ms-16.3s	Over current delay time
	ShortCurrentTH	50mV/Rs-620mV/Rs with step of 20mV/Rs	Short current threshold
	ShortCurrentDelay	4us-32.6mS	Short current delay time
	OCSCReleaseTime	0.5Min-4.25Min with step of 0.25Min	OC,SC release time setting
	OCSCAutoRelease		OC,SC auto release enable
OV/UV Configuration	*OverVoltageTH*	0-5V	Over voltage(OV) threshold voltage setting
	OVRelease	0-5V	OV release voltage setting
	UnderVoltageTH	0-5V	Under voltage(UV) threshold voltage setting
	UVRelease	0-5V	UV release voltage setting

Group	Name	Units/Steps/Values	Description
	OVUVDelay	seconds	OV and UV delay time setting
OT/UT Configuration	*ExtTCh1Enable*		Enable the 1st external temperature measurement channel
	ExtTCh2Enable		Enable the 2nd external temperature measurement channel
	ExtOverTempTH		External over temperature (OT) threshold
	ExtOverTempRelease		External OT release Value
	ExtUnderTempTH		External under temperature (UT) threshold
	ExtUnderTempRelease		External UT release calue
	IntOverTempTH		Internal OT threshold
	IntOverTempRelease		Internal OT release value
	IntUnderTempTH		Internal UT threshold
	IntUnderTempRelease		Internal UT release value
	OTUTDelay	1-16 Temperature scan cycles	OT UT delay time setting
PF Configuration	*PFVHTH*	0-5V	Permanent failure(PF) high voltage threshold set
	PFVLTH	0-5V	PF low voltage threshold setting
	PFDelay	2-32 seconds steps: 2S	PF delay time
	PFVHEnable		PFVH function enable
	PFVLEnable		PFVL function enable
	MOSFailEnable		PF of MOSFET failure enable
	PFUnbalanceTH		PF of the cell unbalance threshold
Bleeding Configuration	*BleedEnable*		Bleeding function enable
	ExtBleedSel		To select the external or internal bleeding method
	BleedCellNumber	1-4	Max bleeding cell number in external bleeding method
	BleedStartPoint	0-5V	Bleeding start point voltage
	BleedAccuracy	9.76, 19.50, 29.30, 39.00, 48.80, 58.56, 68.30, 78.10mV	Bleeding accuracy setting
Voltage GasGauge	*GaugeV1*	0-5V	Voltage gas-gauge Level 1
	GaugeV2	0-5V	Voltage gas-gauge Level 2
	GaugeV3	0-5V	Voltage gas-gauge Level 3
	GaugeV4	0-5V	Voltage gas-gauge Level 4
	GaugeV5	0-5V	Voltage gas-gauge Level 5
EFETC Control	*EfetcMode*	Charge FET control	To set the EFETC control mode
		Discharge FET Control	
		Charge/Discharge FET Control	

Group	Name	Units/Steps/Values	Description
		Output Discharge control logic	
	EfetcShutDown		To select the EFETC pin as a shut down input pin
Battery Protection	*AuthentCode*		Authentication code
	AuthentEnable		Authentication control
Data Protection	*PassWord*	16 bits binary	
	UserControl	2 bits	Protect the user area data
	SecretFreeze	1bit	Protect the secret area data: AuthentCode and PassWord

PACKAGE INFORMATION



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c1	0.09	—	0.16
D		12.00 BSC	
D1		10.00 BSC	
E		12.00 BSC	
E1		10.00 BSC	
e		0.50 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
S		0.20 REF	
θ		3.5° REF	
θ1		5.0° REF	
θ2		12° REF	
θ3		12° REF	
R1		0.16 REF	
R2		0.15 REF	

NOTES:

1. JEDEC OUTLINE: MS-026 BCD
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm

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