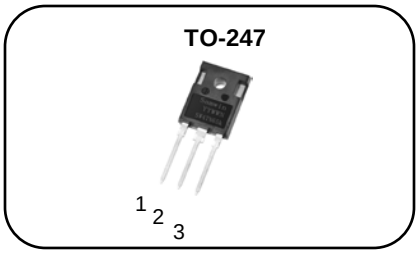
Samwin®

SW47N65K

N-channel Enhanced mode TO-247 MOSFET

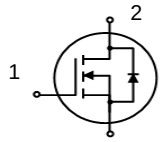
Features

- High ruggedness
- Low $R_{DS(ON)}$ (Typ 60mΩ)@V_{GS}=10V
- Low Gate Charge (Typ 152nC)
- Improved dv/dt Capability
- 100% Avalanche Tested
- Application:Charge,LED,PC Power



1. Gate 2. Drain 3. Source

BV_{DSS} : 650V
I_D : 47A
$R_{DS(ON)}$:60mΩ



General Description

This power MOSFET is produced with advanced technology of SAMWIN.
This technology enable the power MOSFET to have better characteristics, including fast switching time, low on resistance, low gate charge and especially excellent avalanche characteristics.

LEAD-FREE RoHS

Order Codes

Item	Sales Type	Marking	Package	Packaging
1	SW A 47N65 K	SW47N65K	TO-247	TUBE

Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to source voltage		650	V
I_D	Continuous drain current (@T_C=25°C)		47*	A
	Continuous drain current (@T_C=100°C)		29.6*	A
I_{DM}	Drain current pulsed	(note 1)	188	A
V_{GS}	Gate to source voltage		±30	V
E_{AS}	Single pulsed avalanche energy	(note 2)	1200	mJ
E_{AR}	Repetitive avalanche energy	(note 1)	150	mJ
dv/dt	Peak diode recovery dv/dt	(note 3)	5	V/ns
P_D	Total power dissipation (@T_C=25°C)		328.9	W
	Derating factor above 25°C		2.6	W/°C
T_{STG}, T_J	Operating junction temperature & storage temperature		-55 ~ + 150	°C
T_L	Maximum lead temperature for soldering purpose, 1/8 from case for 5 seconds.		300	°C

*. Drain current is limited by junction temperature.

Thermal characteristics

Symbol	Parameter	Value	Unit
R_{thjc}	Thermal resistance, Junction to case	0.38	°C/W
R_{thja}	Thermal resistance, Junction to ambient	34.9	°C/W

Electrical characteristic (T_C = 25ºC unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	V_{GS}=0V, I_D=250uA	650			V
ΔBV_{DSS} / ΔT_J	Breakdown voltage temperature coefficient	I_D=250uA, referenced to 25ºC		0.62		V/ºC
I_{DSS}	Drain to source leakage current	V_{DS}=650V, V_{GS}=0V			1	uA
		V_{DS}=520V, T_C=125ºC			50	uA
I_{GSS}	Gate to source leakage current, forward	V_{GS}=30V, V_{DS}=0V			100	nA
	Gate to source leakage current, reverse	V_{GS}=-30V, V_{DS}=0V			-100	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250uA	2		5	V
$R_{DS(ON)}$	Drain to source on state resistance	V_{GS}=10V, I_D=23A		60	72	mΩ
G_{fs}	Forward transconductance	V_{DS}=30V, I_D=23A		33		S
Dynamic characteristics						
C_{iss}	Input capacitance	V_{GS}=0V, V_{DS}=200V, f=1MHz		5670		pF
C_{oss}	Output capacitance			175		
C_{rss}	Reverse transfer capacitance			25		
$t_{d(on)}$	Turn on delay time	V_{DS}=325V, I_D=47A , V_{GS}=10V, R_G=25Ω (note 4,5)		70		ns
t_r	Rising time			99		
$t_{d(off)}$	Turn off delay time			302		
t_f	Fall time			84		
Q_g	Total gate charge	V_{DS}=520V, V_{GS}=10V, I_D=47A (note 4,5)		152		nC
Q_{gs}	Gate-source charge			48		
Q_{gd}	Gate-drain charge			66		

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET			47	A
I_{SM}	Pulsed source current				188	A
V_{SD}	Diode forward voltage drop.	I_S=47A, V_{GS}=0V			1.4	V
t_{rr}	Reverse recovery time	I_S=20A, V_{GS}=0V, dI_F/dt=100A/us		1584		ns
Q_{rr}	Reverse recovery charge			31		uC

※. Notes

1. Repeatitive rating : pulse width limited by junction temperature.
2. L = 37.2mH, I_{AS} =8 A, V_{DD} = V, R_G=25Ω, Starting T_J = 25ºC
3. I_{SD} ≤ 20A, di/dt = 100A/us, V_{DD} ≤ BV_{DSS}, Staring T_J =25ºC
4. Pulse Test : Pulse Width ≤ 300us, duty cycle ≤ 2%
5. Essentially independent of operating temperature.

Fig. 1. On-state characteristics

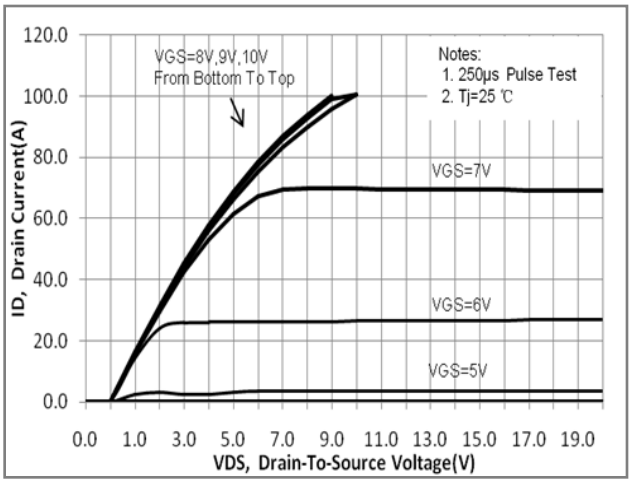


Fig. 2. On-resistance variation vs. drain current and gate voltage

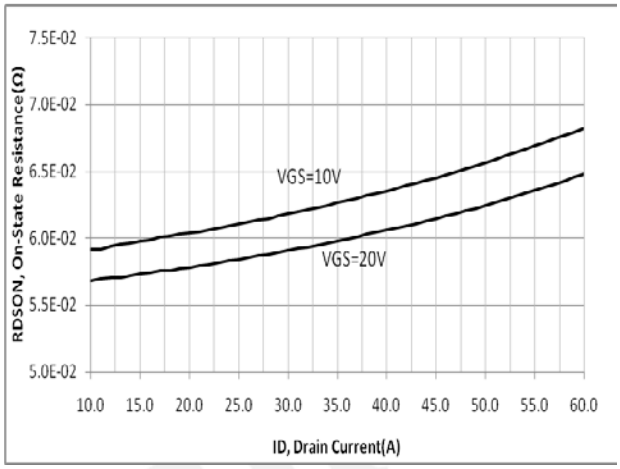


Fig. 3. Gate charge characteristics

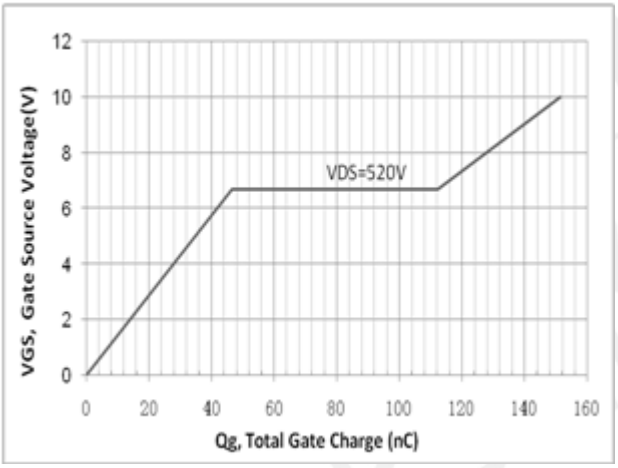


Fig. 4. On state current vs. diode forward voltage

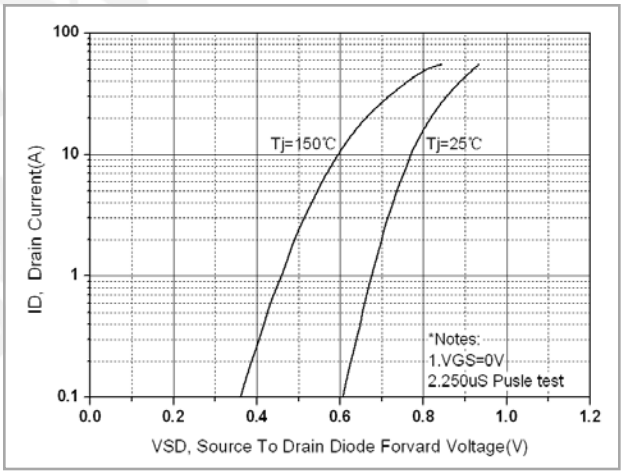


Fig 5. Breakdown Voltage Variation vs. Junction Temperature

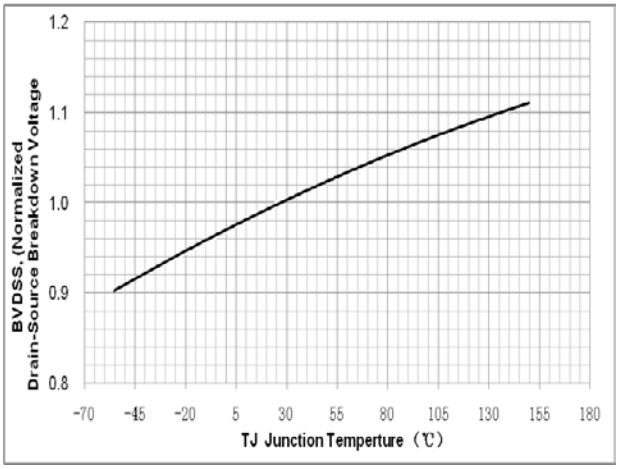


Fig. 6. On resistance variation vs. junction temperature

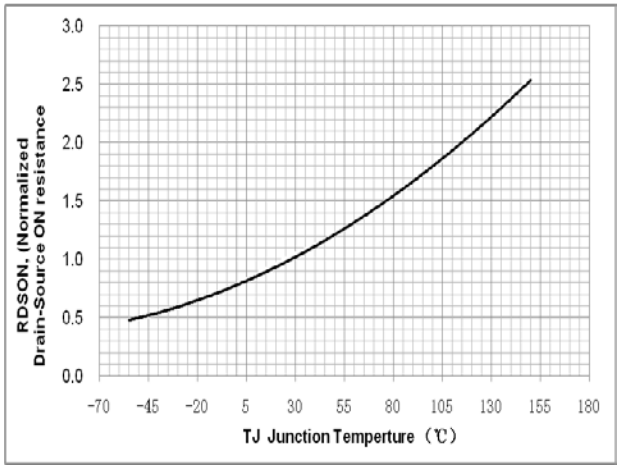


Fig. 7. Maximum safe operating area

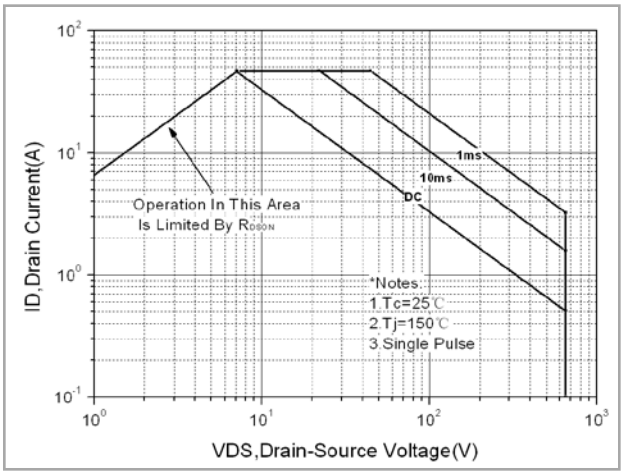


Fig. 8. Capacitance Characteristics

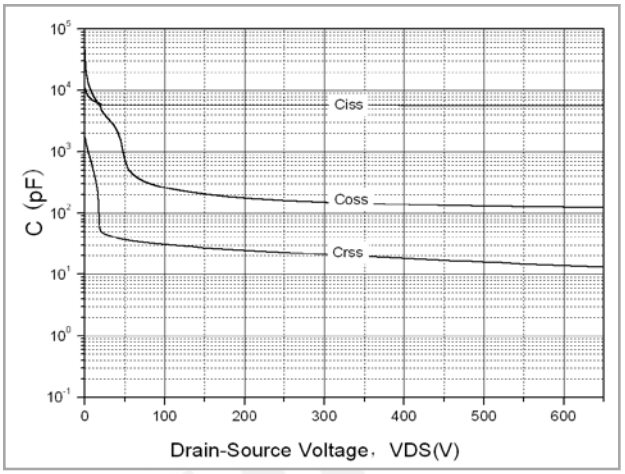


Fig. 9. Transient thermal response curve

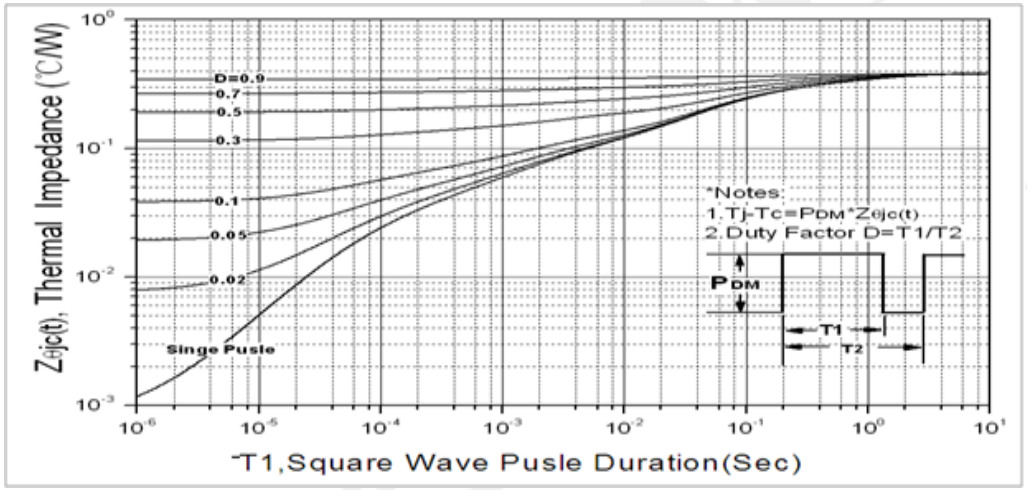


Fig. 10. Gate charge test circuit & waveform

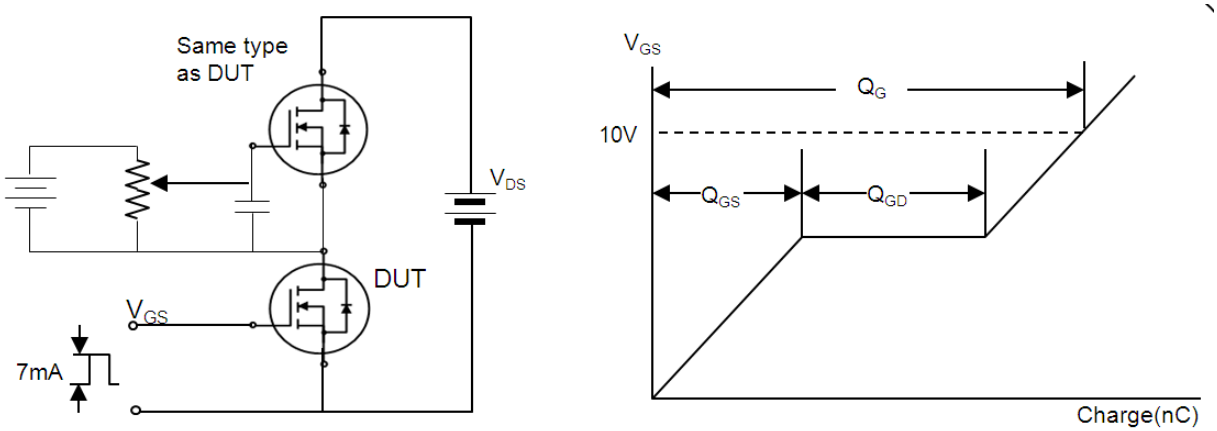


Fig. 11. Switching time test circuit & waveform

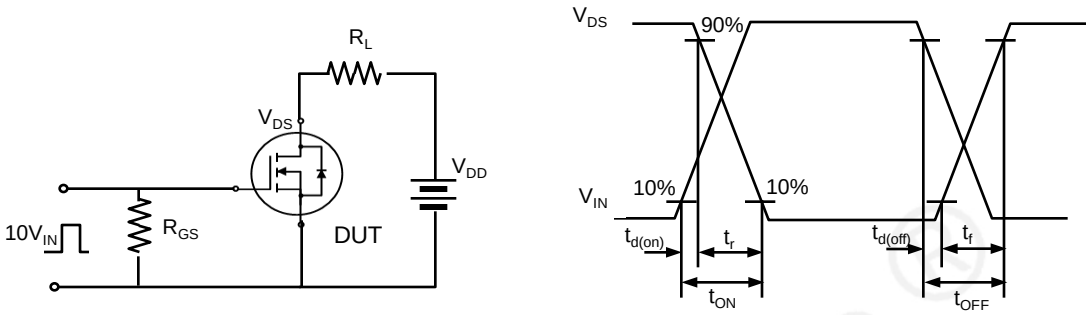


Fig. 12. Unclamped Inductive switching test circuit & waveform

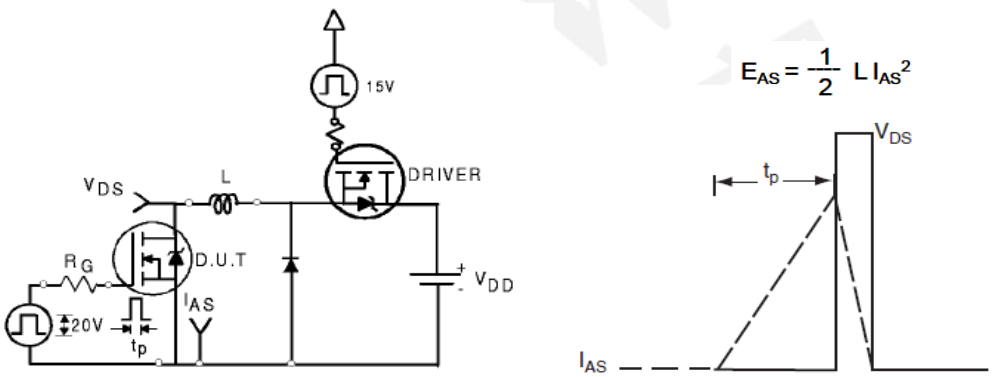
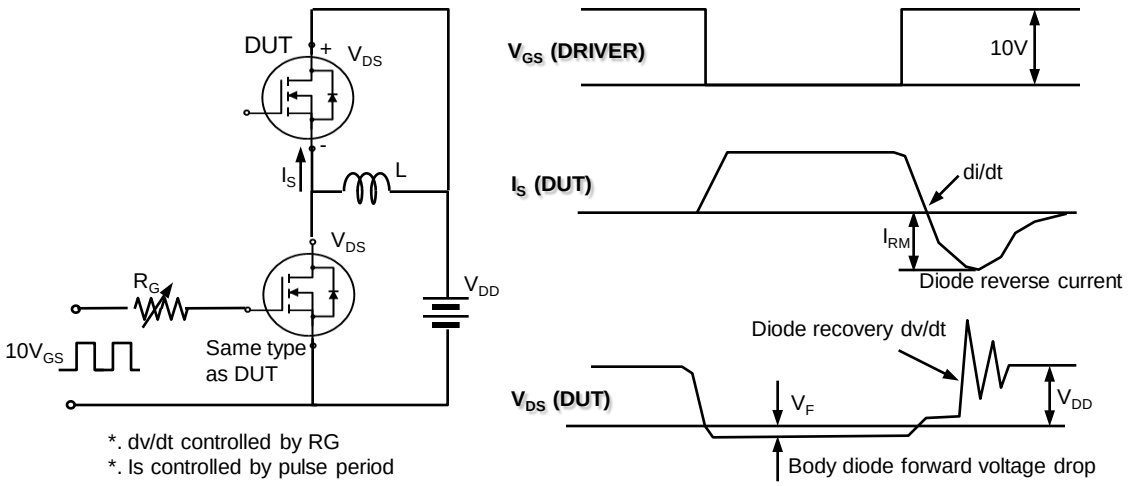


Fig. 13. Peak diode recovery dv/dt test circuit & waveform



*. dv/dt controlled by RG
*. Is controlled by pulse period

DISCLAIMER

* All the data & curve in this document was tested in XI'AN SEMIPOWER TESTING & APPLICATION CENTER.
* This product has passed the PCT,TC,HTRB,HTGB,HAST,PC and Solderdunk reliability testing.
* Qualification standards can also be found on the Web site (**http://www.semipower.com.cn**)
* Suggestions for improvement are appreciated, Please send your suggestions to **samwin@samwinsemi.com**