

♦ DESCRIPTION

The MTDS3906 is the N-Channel logic enhancement mode power field effect transistor are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

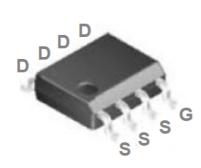
◆ FEATURES

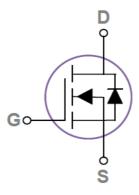
- ightharpoonup 30V/20A, R_{DS(ON)} = 6mΩ @ V_{GS} = 10V
- Improved dv/dt capability
- Fast switching
- 100% EAS Guaranteed
- Green Device Available
- SOP-8 package design

♦ APPLICATIONS

- POWER Management in Note
- Portable Equipment
- DC/DC Converter
- Load Switch
- LED Lighting

◆ PIN CONFIGURATION SOP-8







♦ ABSOLUTE MAXIMUM RATINGS

(T_A=25° Unless Otherwise Noted)

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	T _C = 25°C	l_	20	۸
	Tc = 100°C	l _D	12.6	A
Pulsed Drain Current		I _{DM}	80	А
Power Dissipation	Tc = 25°C	D	5.4	W
	Derate above 25℃	P _D	0.043	W/°C
Operating junction temperature range		TJ	- 55 to 150	°C
Storage temperature range		T _{STG}	- 55 to 150	°C

♦ THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Unit	
Junction-to-Ambient	R ₀ JA	85	0CAM	
Junction-to-Case	Rejc	23	°C/W	

♦ ORDERING INFORMATION

Device	Package	REMARK
MTDS3906	SOP-8	



♦ ELECTRICAL CHARACTERISTICS

(TA=25° Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static Parameters						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0V$, $I_D = 250 \mu A$	30	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250µA	1.2	1.6	2.5	V
Gate Leakage Current	Igss	$V_{DS} = 0V, V_{GS} = \pm 20 V$	-	-	±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} = 0V, T _J = 25 °C	-	-	1	μΑ
		V _{DS} =24V, V _{GS} = 0V, T _J = 125 °C	-	-	10	
Forward Trans conductance	g fs	V _{DS} = 10V, I _D = 10A	-	18	-	S
Drain-Source On Resistance	R _{DS(ON)}	V _{GS} = 4.5V, I _D =5A	-	6.5	9	mΩ
		V _{GS} = 10V, I _D =10A	-	5	6	
Diode Forward Voltage	V_{SD}	I _S = 1A	-	-	1	V
Dynamic Parameters						
Input Cap.	C _{iss}	V _{DS} = 25V, V _{GS} = 0V, F = 1MH _z	-	1160	1900	pF
Output Cap.	Coss		-	200	400	
Reverse Transfer Cap.	Crss		-	180	360	
Total Gate Charge	Qg	V _{DS} = 15V, V _{GS} = 4.5V, I _D =20A	-	11.1	22	
Gate-Source Charge	Q_{gs}		-	1.85	3.7	nC
Gate-Drain Charge	Q_{gd}		=	6.8	13	
Turn-On Time	T _{D(ON)}	V _{DS} =15V, V _{GS} =10V ,	-	7.5	15	
	tr		-	14.5	28	nS
Turn-Off Time	T _{D(OFF)}	$R_L = 3.3\Omega$, $I_D = 15A$	-	35.2	60	
	t _f		-	9.6	19	
Gate Resistance	Rg	V_{DS} = 0V, V_{GS} = 0V, F = 1MH _Z	-	2.5	5	Ω

♦ TYPICAL CHARACTERICTICS

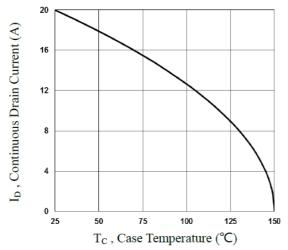


Fig.1 Continuous Drain Current vs. Tc

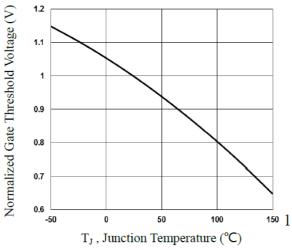


Fig.3 Normalized V_{th} vs. T_J

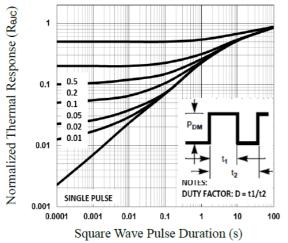


Fig.5 Normalized Transient Impedance

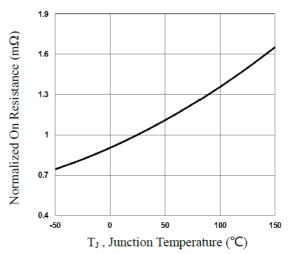


Fig.2 Normalized RDSON vs. T_J

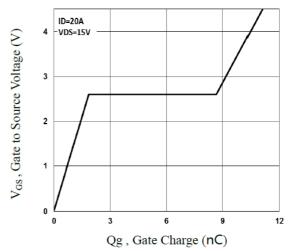


Fig.4 Gate Charge Waveform

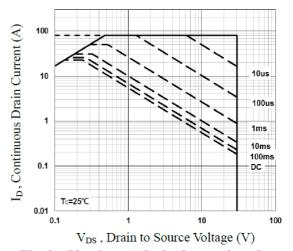


Fig.6 Maximum Safe Operation Area



♦ TYPICAL CHARACTERICTICS

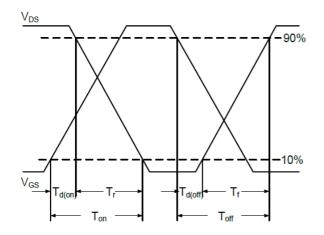


Fig.7 Switching Time Waveform

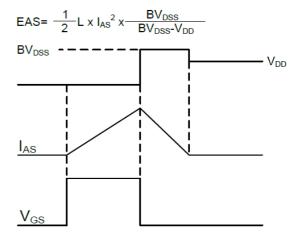


Fig.8 EAS Waveform



♦ PHYSICAL DIMENSIONS

8-Pin surface Mount SOP-8

