BATTERY PROTECTION IC FOR 3-SERIAL OR 4-SERIAL-CELL PACK

S-8254 Series

The S-8254 series is a protection IC for 3-serial or 4-serial cell lithium ion rechargeable batteries and includes a high-accuracy voltage detector and delay circuit.
The S-8254 series protects both 3-serial or 4-serial cells using the SEL pin for switching.

■ Features

(1) High-accuracy voltage detection for each cell

- Overcharge detection voltage n (n = 1 to 4) 3.9 V to 4.4 V (50 mV steps) Accuracy ±25 mV
- Overcharge release voltage n (n = 1 to 4) 3.8 V to 4.4 V[*1] Accuracy ±50 mV

***1.** Overcharge hysteresis voltage n (n = 1 to 4) can be selected as 0 V or from a range of 0.1 V to 0.4 V in 50 mV steps.

(Overcharge hysteresis voltage = Overcharge detection voltage − Overcharge release voltage)

- Overdischarge detection voltage n (n = 1 to 4) 2.0 V to 3.0 V (100 mV steps) Accuracy ±80 mV
- Overdischarge release voltage n (n = 1 to 4) 2.0 V to 3.4 V[*2] Accuracy ±100 mV

***2.** Overdischarge hysteresis voltage n (n = 1 to 4) can be selected as 0 V or from a range of 0.2 V to 0.7 V in 100 mV steps.

(Overdischarge hysteresis voltage = Overdischarge release voltage − Overdischarge detection voltage)

(2) Three-level overcurrent protection

- Overcurrent detection voltage 1 0.05 V to 0.3 V (50 mV steps) Accuracy ±25 mV
- Overcurrent detection voltage 2 0.5 V Accuracy ±100 mV
- Overcurrent detection voltage 3 VC1 − 1.2 V Accuracy ±300 mV

(3) Delay times for overcharge detection, overdischarge detection and overcurrent detection 1 can be set by external capacitors. (Delay times for overcurrent detection 2 and 3 are fixed internally.)

(4) Switchable between a 3-serial cell and 4-serial cell using the SEL pin

(5) Charge/discharge operation can be controlled via the control pins.

(6) Withstanding voltage element Absolute maximum rating: 26 V

(7) Wide operating voltage range 2 V to 24 V

(8) Wide operating temperature range −40°C to +85 °C

(9) Low current consumption

- Operation mode 30 μA max. (+25°C)
- Power-down mode 0.1 μA max. (+25°C)

■ Applications

- Lithium-ion rechargeable battery packs

■ Package

- 16-Pin TSSOP (Package drawing code: FT016-A)

■ Block Diagram

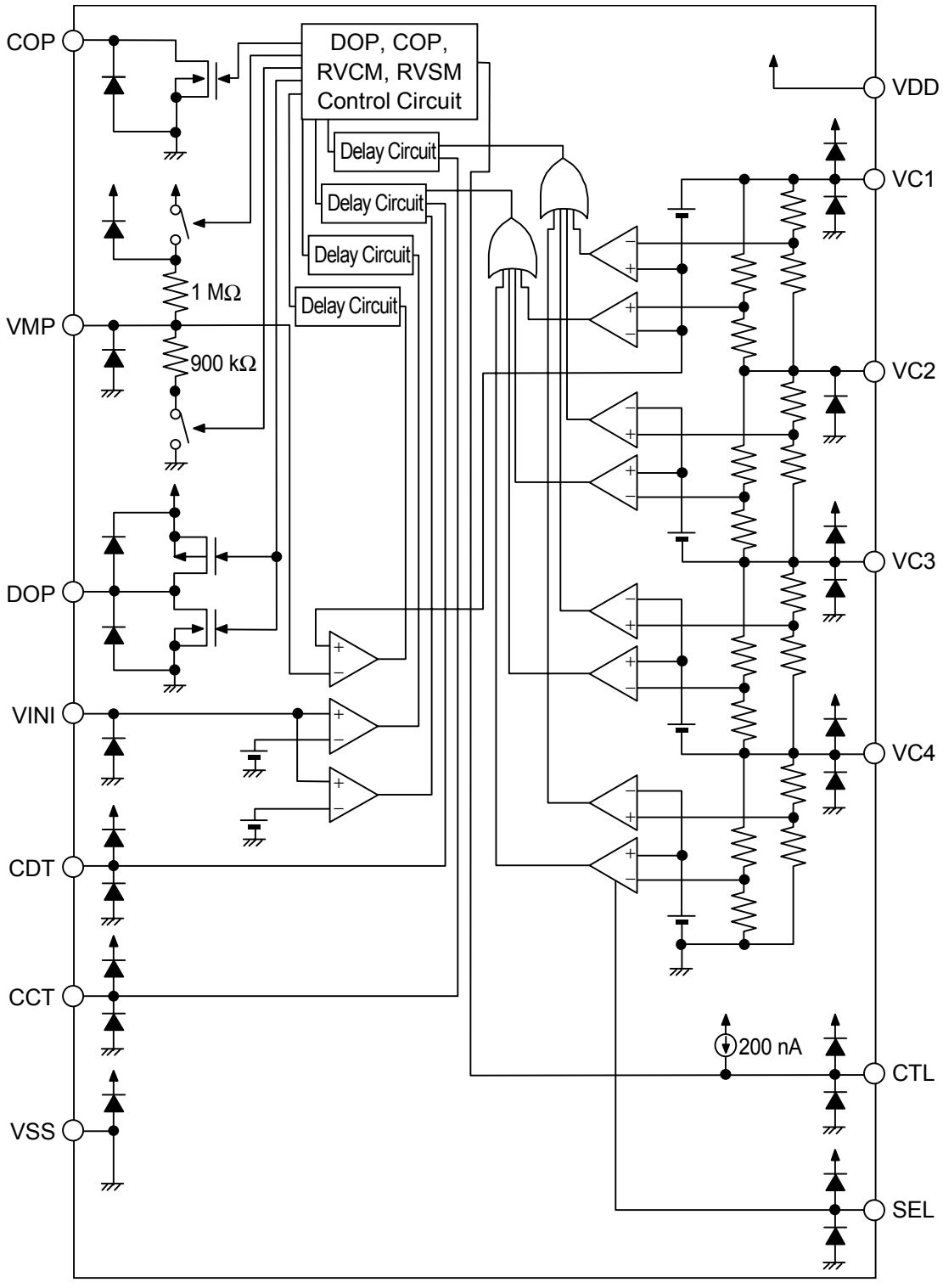
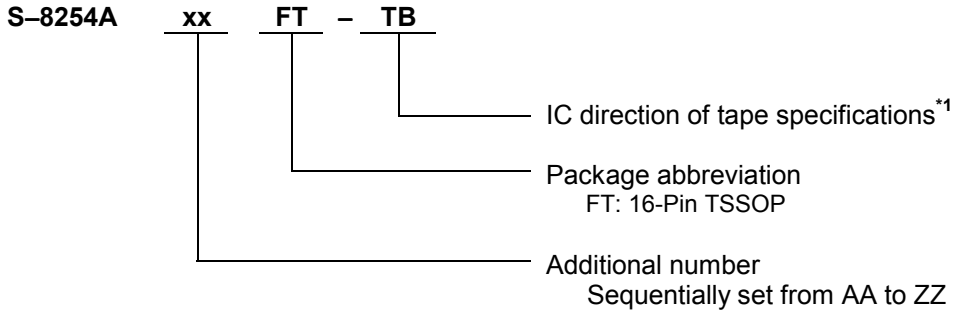


Figure 1

■ Selection Guide

1. Product Name



***1.** Refer to the taping drawing.

2. Product Name List

Table 1

Product Name/Parameter	Overcharge Detection Voltage V_{CU}	Overcharge Release Voltage V_{CL}	Overdischarge Detection Voltage V_{DL}	Overdischarge Release Voltage V_{DU}	Overcurrent Detection Voltage 1 V_{IOV1}	0 V Battery Charge Function
S-8254AAAFT-TB	4.350 ± 0.025 V	4.150 ± 0.050 V	2.00 ± 0.080 V	2.70 ± 0.100 V	0.30 ± 0.025 V	Provided
S-8254AABFT-TB	4.250 ± 0.025 V	4.250 ± 0.025 V	2.00 ± 0.080 V	2.70 ± 0.100 V	0.30 ± 0.025 V	Provided
S-8254AAEFT-TB	4.350 ± 0.025 V	4.150 ± 0.050 V	2.00 ± 0.080 V	2.70 ± 0.100 V	0.20 ± 0.025 V	Provided
S-8254AAFFT-TB	4.350 ± 0.025 V	4.150 ± 0.050 V	2.40 ± 0.080 V	3.00 ± 0.100 V	0.20 ± 0.025 V	Provided
S-8254AAGFT-TB	4.275 ± 0.025 V	4.075 ± 0.050 V	2.30 ± 0.080 V	2.70 ± 0.100 V	0.13 ± 0.025 V	Provided

Remark If a product with the required detection voltage does not appear in the above list, contact our sales office.

■ Pin Assignment

16-Pin TSSOP
Top view

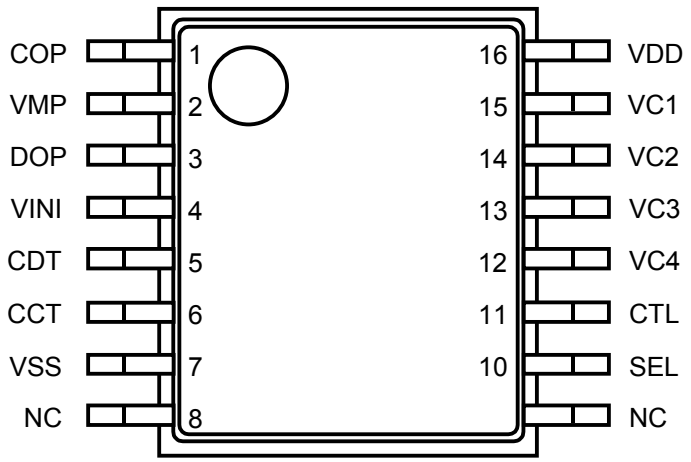


Figure 2

Table 2

Pin No.	Name	Function
1	COP	Connection of charge control FET gate (Nch open-drain output)
2	VMP	Voltage detection between VC1 and VMP (overcurrent 3 detection pin)
3	DOP	Connection of discharge control FET gate (CMOS output)
4	VINI	Voltage detection between VSS and VINI (overcurrent 1, 2 detection pin)
5	CDT	Capacitor connection for overdischarge detection and overcurrent detection 1 delay
6	CCT	Capacitor connection for overcharge detection delay
7	VSS	Negative power supply input, negative voltage connection for battery 4
8	NC	No connection*1
9	NC	No connection*1
10	SEL	Pin for switching 3-serial cell/4-serial cell VSS level: 3-serial cell, VDD level: 4-serial cell
11	CTL	Control of charge FET and discharge FET
12	VC4	Connection for negative voltage of battery 3 and positive voltage of battery 4
13	VC3	Connection for negative voltage of battery 2 and positive voltage of battery 3
14	VC2	Connection for negative voltage of battery 1 and positive voltage of battery 2
15	VC1	Connection for positive voltage of battery 1
16	VDD	Connection for positive power supply input and positive voltage of battery 1

***1.** NC indicates that the pin is electrically open. Therefore, the pin can be connected to VDD or VSS.

■ Absolute Maximum Ratings

Table 3

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Applicable Pins	Rating	Unit
Input voltage between VDD and VSS	V_{DS}	—	V_{SS} − 0.3 to V_{SS} + 26	V
Input pin voltage	V_{IN}	VC1, VC2, VC3, VC4, CTL, SEL, CCT, CDT, VINI	V_{SS} − 0.3 to V_{DD} + 0.3	
VMP pin input voltage	V_{VMP}	VMP	V_{SS} − 0.3 to V_{SS} + 26	
DOP pin output voltage	V_{DOP}	DOP	V_{SS} − 0.3 to V_{DD} + 0.3	
COP pin output voltage	V_{COP}	COP	V_{SS} − 0.3 to V_{SS} + 26	
Power dissipation	P_D	—	400	mW
Operating temperature range	Topr	—	−40 to +85	°C
Storage temperature range	Tstg	—	−40 to +125	

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Electrical Characteristics

Table 4 (Ta = 25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test Circuit
DETECTION VOLTAGE								
Overcharge detection voltage n n = 1, 2, 3, 4	V_{CUn}	3.9 to 4.4 V, adjustable in 50 mV steps		V_{CUn} – 0.025	V_{CUn}	V_{CUn} + 0.025	V	2
Overcharge release voltage n n = 1, 2, 3, 4	V_{CLn}	3.8 to 4.4 V, adjustable in 50 mV steps	$V_{CL} \neq V_{CU}$	V_{CLn} – 0.05	V_{CLn}	V_{CLn} + 0.05	V	
			$V_{CL} = V_{CU}$	V_{CLn} – 0.025	V_{CLn}	V_{CLn} + 0.025	V	
Overdischarge detection voltage n n = 1, 2, 3, 4	V_{DLn}	2.0 to 3.0 V, adjustable in 100 mV steps		V_{DLn} – 0.08	V_{DLn}	V_{DLn} + 0.08	V	
Overdischarge release voltage n n = 1, 2, 3, 4	V_{DUn}	2.0 to 3.4 V, adjustable in 100 mV steps	$V_{DL} \neq V_{DU}$	V_{DUn} – 0.10	V_{DUn}	V_{DUn} + 0.10	V	
			$V_{DL} = V_{DU}$	V_{DUn} – 0.08	V_{DUn}	V_{DUn} + 0.08	V	
Overcurrent detection voltage 1	V_{IOV1}	0.05 to 0.3 V, adjustable		V_{IOV1} – 0.025	V_{IOV1}	V_{IOV1} + 0.025	V	
Overcurrent detection voltage 2	V_{IOV2}	—		0.4	0.5	0.6	V	
Overcurrent detection voltage 3	V_{IOV3}	—		V_{C1} – 1.5	V_{C1} – 1.2	V_{C1} – 0.9	V	
Temperature coefficient 1	T_{COE1}	Ta = 0 to 50°C*1		–1.0	0	1.0	mv/°C	
Temperature coefficient 2	T_{COE2}	Ta = 0 to 50°C*2		–0.5	0	0.5	mv/°C	
DELAY TIME								
Overcharge detection delay time	t_{CU}	CCT pin capacitance = 0.1 µF		0.5	1.0	1.5	s	3
Overdischarge detection delay time	t_{DL}	CDT pin capacitance = 0.1 µF		50	100	150	ms	
Overcurrent detection delay time 1	t_{IOV1}	CDT pin capacitance = 0.1 µF		5	10	15	ms	
Overcurrent detection delay time 2	t_{IOV2}	—		0.4	1	1.6	ms	
Overcurrent detection delay time 3	t_{IOV3}	FET gate capacitance = 2000 pF		100	300	600	µs	
0 V BATTERY CHARGE FUNCTION								
0 V charge starting charger voltage	V_{0CHA}	With 0 V charge		—	0.8	1.5	V	4
0 V battery charge inhibition battery voltage	V_{0INH}	Without 0 V charge		0.4	0.7	1.1	V	
INTERNAL RESISTANCE								
Resistance between VMP and VDD	R_{VMD}	—		0.5	1	1.5	MΩ	5
Resistance between VMP and VSS	R_{VMS}	—		450	900	1800	kΩ	
INPUT VOLTAGE								
Operating voltage between VDD and VSS	V_{DSOP}	Output voltage of DOP and COP fixed		2	—	24	V	2
CTLn input voltage, high	V_{CTLH}	—		$V_{DD} \times 0.8$	—	—	V	
CTLn input voltage, low	V_{CTLL}	—		—	—	$V_{DD} \times 0.2$	V	
SEL input voltage, high	V_{SELH}	—		$V_{DD} \times 0.8$	—	—	V	
SEL input voltage, low	V_{SELL}	—		—	—	$V_{DD} \times 0.2$	V	
INPUT CURRENT								
Current consumption	I_{OPE}	V1 = V2 = V3 = V4 = 3.5 V		—	12	30	µA	1
Current consumption at power down	I_{PDN}	V1 = V2 = V3 = V4 = 1.5 V		—	—	0.1	µA	
VC1 pin current	I_{VC1}	V1 = V2 = V3 = V4 = 3.5 V		—	1.5	3	µA	5
VC2 pin current	I_{VC2}	V1 = V2 = V3 = V4 = 3.5 V		–0.3	0	0.3	µA	
VC3 pin current	I_{VC3}	V1 = V2 = V3 = V4 = 3.5 V		–0.3	0	0.3	µA	
VC4 pin current	I_{VC4}	V1 = V2 = V3 = V4 = 3.5 V		–0.3	0	0.3	µA	
CTL pin current, high	I_{CTLH}	V1 = V2 = V3 = V4 = 3.5 V $V_{CTL} = V_{DD}$		—	—	0.1	µA	
CTL pin current, low	I_{CTLL}	V1 = V2 = V3 = V4 = 3.5 V $V_{CTL} = V_{SS}$		–0.4	–0.2	—	µA	
SEL pin current, high	I_{SELH}	V1 = V2 = V3 = V4 = 3.5 V $V_{SEL} = V_{DD}$		—	—	0.1	µA	
SEL pin current, low	I_{SELL}	V1 = V2 = V3 = V4 = 3.5 V $V_{SEL} = V_{SS}$		–0.1	—	—	µA	
OUTPUT CURRENT								
COP pin leakage current	I_{COH}	V_{COP} = 24 V		—	—	0.1	µA	5
COP pin sink current	I_{COL}	$V_{COP} = V_{SS}$ + 0.5 V		10	—	—	µA	
DOP pin source current	I_{DOH}	$V_{DOP} = V_{DD}$ – 0.5 V		10	—	—	µA	
DOP pin sink current	I_{DOL}	$V_{DOP} = V_{SS}$ + 0.5 V		10	—	—	µA	

***1.** Voltage temperature coefficient 1: Overcharge detection voltage

***2.** Voltage temperature coefficient 2: Overcurrent detection voltage 1

■ Test Circuits

This chapter describes how to test the S-8254 series when a 4-serial cell is selected by setting the SEL pin to the VDD level. When a 3-serial cell is selected by setting the SEL pin to the VSS level, short the power supply V4.

1. Current consumption

(Test circuit 1)

The current at the VSS pin when V1 = V2 = V3 = V4 = 3.5 V and $V_{VMP} = V_{DD}$ is the current consumption (I_{OPE}) during operation.
The current at the VSS pin when V1 = V2 = V3 = V4 = 1.5 V and $V_{VMP} = V_{SS}$ is the current consumption (I_{PDN}) at power down.

2. Overcharge detection voltage, overcharge release voltage, overdischarge detection voltage, overdischarge release voltage, overcurrent detection voltage 1, overcurrent detection voltage 2, overcurrent detection voltage 3, CTL input voltage (high), CTL input voltage (low), SEL input voltage (high), SEL input voltage (low)

(Test circuit 2)

Confirm that the COP and DOP pins are low (V_{DD} is 0.1 V or lower) when $V_{VMP} = V_{SEL} = V_{DD}$, $V_{INI} = V_{CTL} = V_{SS}$, the CDT pin is open, and V1 = V2 = V3 = V4 = 3.5 V (this status is referred to as the initial status).

- **Overcharge detection voltage (V_{CU1}), overcharge release voltage (V_{CL1})**
  The overcharge detection voltage (V_{CU1}) is the voltage of V1 when the voltage of the COP pin is high ($V_{DD} \times 0.9$ V or more) after the V1 voltage has been gradually increased starting at the initial status. The overcharge release voltage (V_{CL1}) is the voltage of V1 when the voltage at the COP pin is low after the V1 voltage has been gradually decreased.

- **Overdischarge detection voltage (V_{DL1}), overdischarge release voltage (V_{DU1})**
  The overdischarge detection voltage (V_{DL1}) is the voltage of V1 when the voltage of the DOP pin is high after the V1 voltage has been gradually decreased starting at the initial status. The overdischarge release voltage (V_{DU1}) is the voltage of V1 when the voltage at the DOP pin is low after the V1 voltage has been gradually increased.
  When the voltage of Vn (n = 2 to 4) is changed, the overcharge detection voltage (V_{CUn}), overcharge release voltage (V_{CLn}), overdischarge detection voltage (V_{DLn}), and overdischarge release voltage (V_{DUn}) can be determined in the same way as when n = 1.

- **Overcurrent detection voltage 1 (V_{IOV1})**
  Overcurrent detection voltage 1 (V_{IOV1}) is the voltage of the VINI pin when the voltage of the DOP pin is high after the VINI pin voltage has been gradually increased starting at the initial status.

- **Overcurrent detection voltage 2 (V_{IOV2})**
  Overcurrent detection voltage 2 (V_{IOV2}) is the voltage of the VINI pin when the voltage of the DOP pin is high after the voltage of the CDT pin was set to V_{SS} following the initial status and the voltage of the VINI pin has been gradually decreased.

- **Overcurrent detection voltage 3 (V_{IOV3})**
  Overcurrent detection voltage 3 (V_{IOV3}) is the voltage difference between V_{DD} and V_{VMP} ($V_{DD} - V_{VMP}$) when the voltage of the DOP pin is high after the VMP voltage has been gradually decreased starting at the initial status.

- **CTL input voltage (high) (V_{CTLH}), CTL input voltage (low) (V_{CTLL})**
  The CTL input voltage (high) (V_{CTLH}) is the voltage of CTL when the voltages at the COP and DOP pins are high after the CTL voltage has been gradually increased starting at the initial status. The CTL input voltage (low) (V_{CTLL}) is the voltage of CTL when the voltages at the COP and DOP pins are low after the CTL voltage has been gradually decreased.

- **SEL input voltage (high) (V_{SELH}), SEL input voltage (low) (V_{SELL})**
  Apply 0 V to V4 in the initial status and confirm that the DOP pin is high. The SEL input voltage (low) (V_{SELL}) is the voltage of the SEL pin when the voltage at the DOP pin is low after the SEL voltage has been gradually decreased. The SEL input voltage (high) (V_{SELH}) is the voltage of the SEL pin when the voltage of the DOP pin is low after the SEL voltage has been gradually increased.

3. Overcharge detection delay time, overdischarge detection delay time, overcurrent detection delay time 1, overcurrent detection delay time 2, overcurrent detection delay time 3

(Test circuit 3)

Confirm that the COP and DOP pins are low when $V_{VMP} = V_{DD}$, $V_{INI} = V_{SS}$, and V1 = V2 = V3 = V4 = 3.5 V (this status is referred to as the initial status).

- **Overcharge detection delay time (t_{CU})**
  The overcharge detection delay time (t_{CU}) is the time it takes for the voltage of the COP pin to change from low to high after the voltage of V1 is instantaneously changed to 4.5 V from the initial status.

- **Overdischarge detection delay time (t_{DL})**
  The overdischarge detection delay time (t_{DL}) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of V1 is instantaneously changed to 1.5 V from the initial status.

- **Overcurrent detection delay time 1 (t_{IOV1})**
  Overcurrent detection delay time 1 (t_{IOV1}) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of the VINI pin is instantaneously changed to 0.4 V from the initial status.

- **Overcurrent detection delay time 2 (t_{IOV2})**
  Overcurrent detection delay time 2 (t_{IOV2}) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of the VINI pin is instantaneously changed to V_{IOV2} max. + 0.2 V from the initial status.

- **Overcurrent detection delay time 3 (t_{IOV3})**
  Overcurrent detection delay time 3 (t_{IOV3}) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of the VMP pin is instantaneously changed to V_{IOV3} min. − 0.2 V from the initial status.

4. 0 V battery charge starting charger voltage or 0 V battery charge inhibition battery voltage

(Test circuit 4)

Ether the 0 V battery charge starting charger voltage or the 0 V battery charge inhibition battery voltage is applied to each product according to the 0 V battery charging function.
The starting condition is V1 = V2 = V3 = V4 = 0 V for a product in which 0 V battery charging is available.
The COP pin voltage should be lower than V_{0CHA} max. − 1 V when the VMP pin voltage $V_{MP} = V_{0CHA}$ max.
The starting condition is V1 = V2 = V3 = V4 = V_{0INH} for a product in which 0 V battery charging is inhibited.
The COP pin voltage should be higher than V_{MP} − 1 V when the VMP pin voltage V_{MP} = 24 V.

5. Resistance between VMP and VDD, resistance between VMP and VSS, VC1 pin current, VC2 pin current, VC3 pin current, VC4 pin current, CTL pin current (high), CTL pin current (low), SEL pin current (high), SEL pin current (low), COP pin leakage current, COP pin sink current, DOP pin source current, DOP pin sink current

(Test circuit 5)

$V_{VMP} = V_{SEL} = V_{DD}$, $V_{INI} = V_{CTL} = V_{SS}$, V1 = V2 = V3 = V4 = 3.5 V, and other pins left open (this status is referred to as the initial status).

The resistance between VMP and VDD (R_{VDM}) is obtained from $R_{VDM} = V_{DD}/I_{VDM}$ using the current value of the VMP pin (I_{VDM}) when V_{VMP} is V_{SS} after the initial status.

The resistance between VMP and VSS (R_{VSM}) is obtained from $R_{VSM} = V_{DD}/I_{VSM}$ using the current value of the VMP pin (I_{VSM}) when V1 = V2 = V3 = V4 = 1.8 V after the initial status.

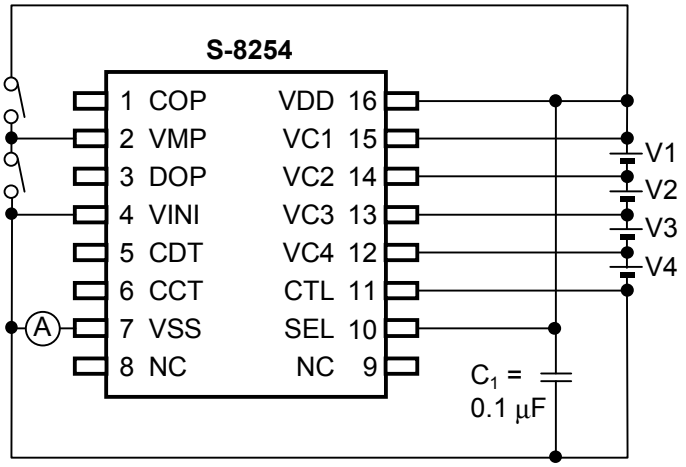
At the initial status, the current that flows through the VC1 pin is the VC1 pin current (I_{VC1}), the current that flows through the VC2 pin is the VC2 pin current (I_{VC2}), the current that flows through the VC3 pin is the VC3 pin current (I_{VC3}), and the current that flows through the VC4 pin is the VC4 pin current (I_{VC4}).

In the initial status, the current that flows through the CTL pin is the CTL pin current (low) (I_{CTLL}), after that, when $V_{CTL} = V_{DD}$, the current that flows through the CTL pin is the CTL pin current (high) (I_{CTLH}).

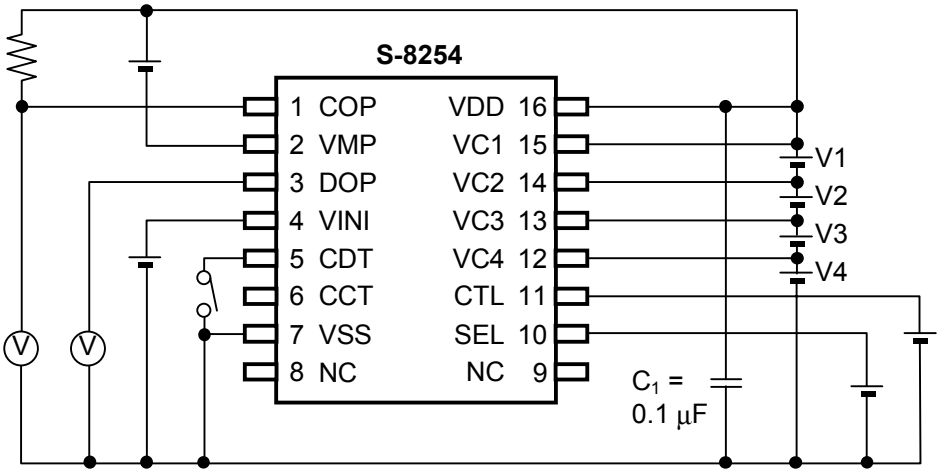
In the initial status, the current that flows through the SEL pin is the SEL pin current (high) (I_{SELH}), after that, when $V_{SEL} = V_{SS}$, the current that flows through the SEL pin is the SEL pin current (low) (I_{SELL}).

The COP pin sink current (I_{COL}) is the current that flows through the COP pin when $V_{COP} = V_{SS} + 0.5$ V after the initial status. After that, the current that flows through the COP pin when V1 = V2 = V3 = V4 = 6 V and $V_{COP} = V_{DD}$ is the COP pin leakage current (I_{COH}).

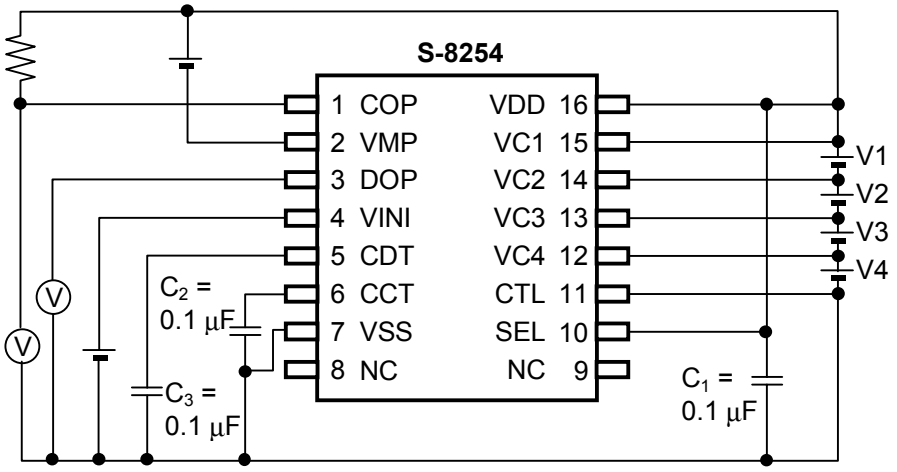
The DOP pin sink current (I_{DOL}) is the current that flows through the DOP pin when $V_{DOP} = V_{SS} + 0.5$ V after the initial status. After that, the current that flows through the DOP pin when $V_{VMP} = V_{DD} - 2$ V and $V_{DOP} = V_{DD} - 0.5$ V is the DOP pin source current (I_{DOH}).



Test Circuit 1

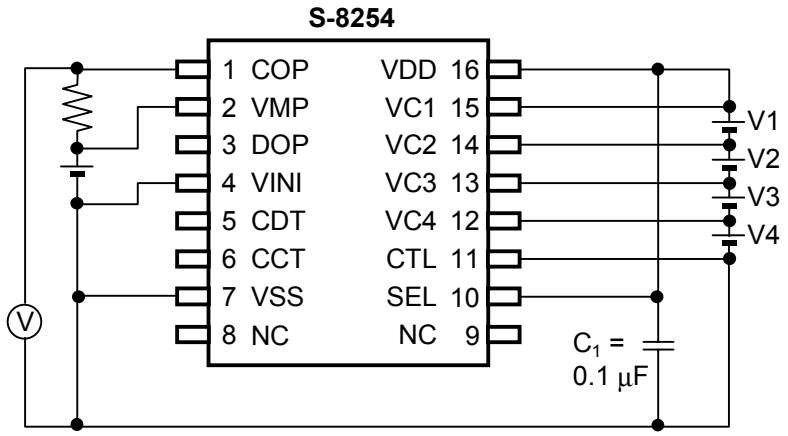


Test Circuit 2

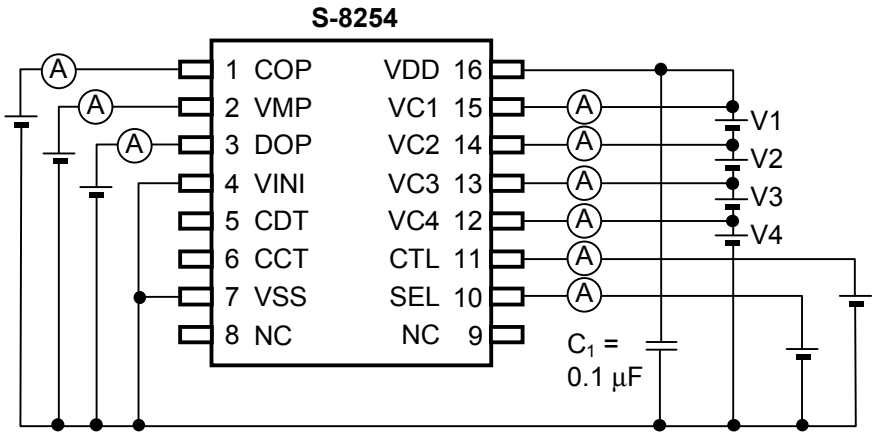


Test Circuit 3

Figure 3 Test Circuit (1/2)



Test Circuit 4



Test Circuit 5

Figure 3 Test Circuit (2/2)

■ Description of Operation

Remark Refer to "■ **Standard Circuit**".

1. Normal status

When all of the battery voltages are in the range from V_{DLn} to V_{CUn} and the discharge current is lower than the specified value (the VINI pin voltage is lower than V_{IOV1} and V_{IOV2}, and the VMP pin voltage is higher than V_{IOV1}), the charging and discharging FETs are turned on.

2. Overcharge status

When any one of the battery voltages becomes higher than V_{CUn} and the state continues for t_{CU} or longer, the COP pin becomes high impedance. The COP pin is pulled up to the EB+ pin voltage by an external resistor, and the charging FET is turned off to stop charging. This is called the overcharge status. The overcharge status is released when one of the following two conditions holds.

a) **All battery voltages become V_{CLn} or lower.**
b) **All of the battery voltages are V_{CUn} or lower, and the VMP pin voltage is 39/40 $\times$ V_{DD} or lower (A load is connected and discharging is started via the body diode of the charging FET.)**

3. Overdischarge status

When any one of the battery voltages becomes lower than V_{DLn} and the state continues for t_{DL} or longer, the DOP pin voltage becomes V_{DD} level, and the discharging FET is turned off to stop discharging. This is called the overdischarging status. After discharging is stopped due to the overdischarge status, the S-8254 enters the power-down status.

4. Power-down status

When discharging has stopped due to the overdischarge status, the VMP pin is pulled down to the V_{SS} level by the RVSM resistor. When the VMP pin voltage is lower than $V_{DD}/2$, the S-8254 enters the power-down status. In the power-down status, almost all the circuits of the S-8254 stop and the current consumption is I_{PDN} or lower. The conditions of each output pin are as follows.

a) **COP Hi-Z**
b) **DOP V_{DD}**

The power-down status is released when the following condition holds.

a) **The MVP pin voltage is $V_{DD}/2$ or higher. (A charger is connected.)**

5. Overcurrent status

The S-8254 has three overcurrent detection levels (V_{IOV1}, V_{IOV2}, and V_{IOV3}) and three overcurrent detection delay times (t_{IOV1}, t_{IOV2}, and t_{IOV3}) corresponding to each overcurrent detection level. When the discharging current becomes higher than the specified value (the voltage between V_{DD} and V_{MP} is greater than V_{IOV1}) and the state continues for t_{IOV1} or longer, the S-8254 enters the overcurrent status, in which the DOP pin voltage becomes V_{DD} level to turn off the discharging FET to stop discharging, the COP pin becomes high impedance and is pulled up to the EB+ pin voltage to turn off the charging FET to stop charging, and the VMP pin is pulled up to the V_{DD} voltage by the internal resistor R_{VDM}. Operation of overcurrent detection level 2 (V_{IOV2}) and overcurrent detection delay time 2 (t_{IOV2}) is the same as for V_{IOV1} and t_{IOV1}.
In the overcurrent status, the VMP pin is pulled up to the V_{DD} level by the internal RVMD resistor. The overcurrent status is released when the following condition holds.

a) **The VMP pin voltage is V_{IOV3} or higher because a charger is connected or the load (30 MΩ or more) is released.**

6. 0 V battery charge function

Regarding the charging of a self-discharged battery (0 V battery), the S-8254 has two functions from which one should be selected.

a) 0 V battery charging is allowed (0 V battery charging is available)
When the charger voltage is higher than V_{0CHA}, the 0 V battery can be charged.

b) 0 V battery charging is prohibited (0 V battery charging is impossible)
When one of the battery voltages is lower than V_{0INH}, the 0 V battery cannot be charged.

Caution When the VDD pin voltage is lower than the minimum value of V_{DSOP}, the operation of the S-8254 series is not guaranteed.

7. Delay time setting

The overcharge detection delay time (t_{CU}) is determined by the external capacitor connected to the CCT pin. The overdischarge detection delay time (t_{DL}) and overcurrent detection delay time 1 (t_{IOV1}) are determined by the external capacitor connected to the CDT pin. Overcurrent detection delay times 2 and 3 (t_{IOV2}, t_{IOV3}) are fixed internally.

	Min.	Typ.	Max.	
t_{CU} [s] =	(5.00,	10.0,	15.0)	$\times C_{CCT}$ [μF]
t_{DL} [s] =	(0.50,	1.00,	1.50)	$\times C_{CCT}$ [μF]
t_{IOV1} [s] =	(0.05,	0.10,	0.15)	$\times C_{CCT}$ [μF]

8. CTL pin

The S-8254 has control pins. The CTL pin is used to control the COP and DOP pin output voltages. CTL2 takes precedence over the battery protection circuit.

Table 5 Conditions Set by CTL Pin

CTL Pin	COP Pin	DOP Pin
High	Hi-Z	V_{DD}
Open	Hi-Z	V_{DD}
Low	Normal status*1	Normal status*1

***1.** The status is controlled by the voltage detector.

9. SEL pin

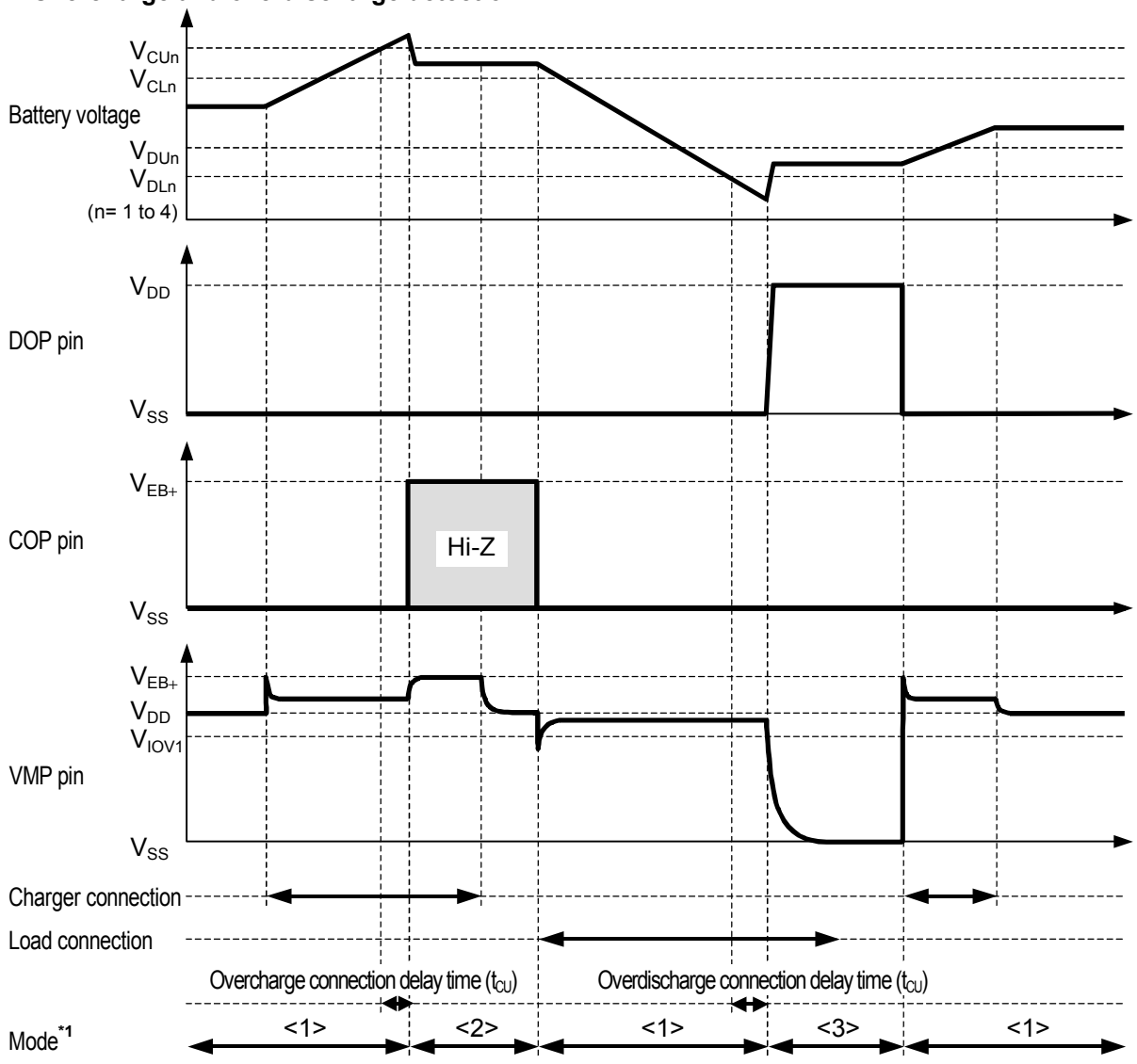
The S-8254 has control pins. The SEL pin is used to switch between 3-cell and 4-cell protection. When the SEL pin is low, overdischarge detection of the V4 cell is prohibited and an overdischarge is not detected even if the V4 cell is shorted, therefore, the V4 cell can be used for 3-cell protection. The SEL pin takes precedence over the battery protection circuit. Use the SEL pin at high or low.

Table 6 Conditions Set by SEL Pin

SEL Pin	Condition
High	4-cell protection
Open	Undefined
Low	3-cell protection

■ Operation Timing Chart

1. Overcharge and overdischarge detection

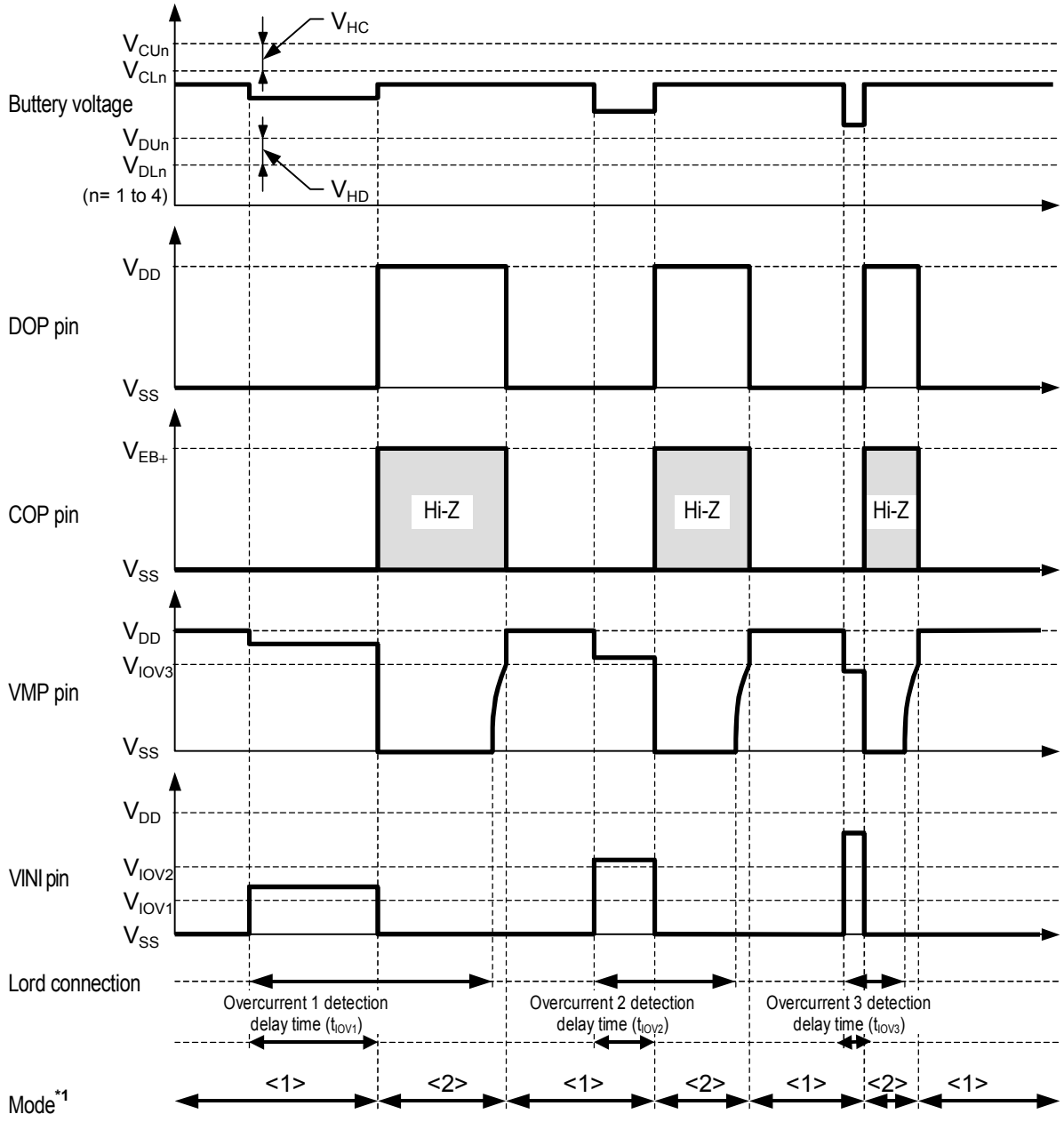


***1.** <1>: Normal mode
<2>: Overcharge mode
<3>: Overdischarge mode

Remark The charger is assumed to charge with a constant current. V_{EB+} indicates the open voltage of the charger.

Figure 4

2. Overcurrent detection



***1.** <1>: Normal mode
<2>: Overcurrent mode

Remark The charger is assumed to charge with a constant current. V_{EB+} indicates the open voltage of the charger.

Figure 5

■ Standard Circuit

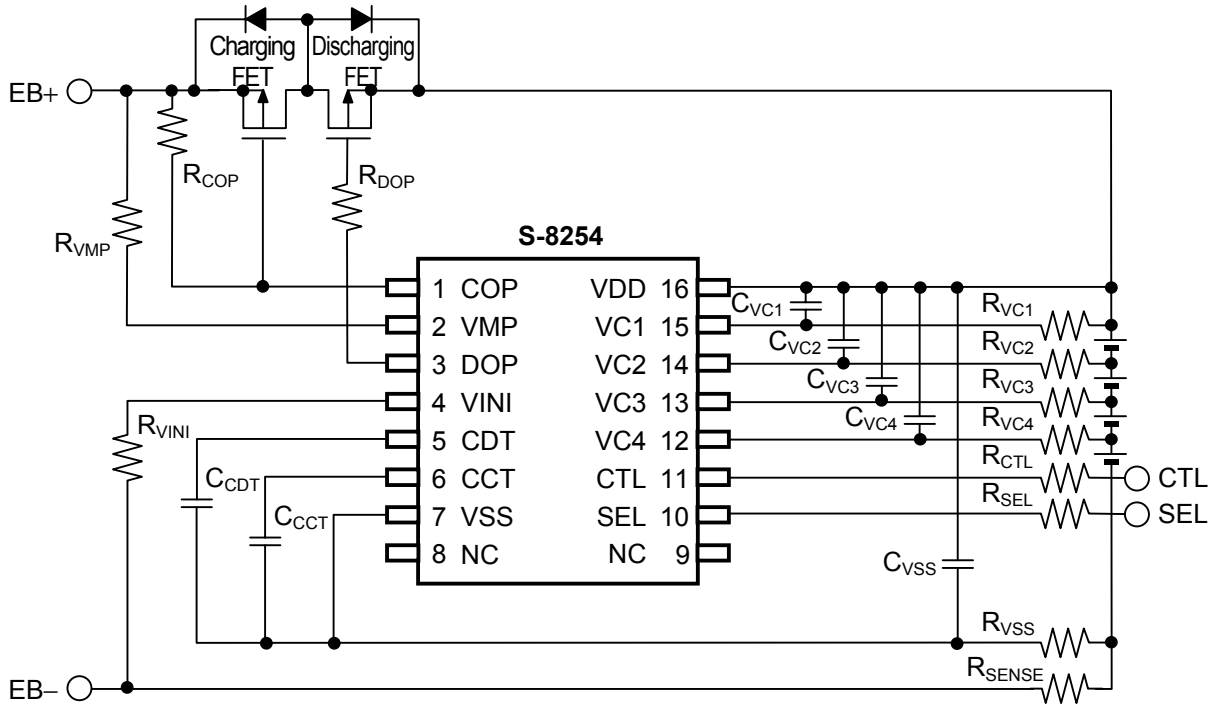


Figure 6

Table 7 Recommended Value for External Parts

No.	Part	Recommended value	Range	Unit
1	R_{VC1}	1	0 to 1	kΩ
2	R_{VC2}	1	0 to 1	kΩ
3	R_{VC3}	1	0 to 1	kΩ
4	R_{VC4}	1	0 to 1	kΩ
5	R_{DOP}	5.1	2 to 10	kΩ
6	R_{COP}	1	0.1 to 1	MΩ
7	R_{VMP}	5.1	1 to 10	kΩ
8	R_{CTL}	0	0 to 100	kΩ
9	R_{VINI}	0	0 to 100	kΩ
10	R_{SEL}	0	0 to 100	kΩ
11	R_{SENSE}	—	0 or higher	mΩ
12	R_{VSS}	0	0 to 51	Ω
13	C_{VC1}	0.1	0 to 0.33	µF
14	C_{VC2}	0.1	0 to 0.33	µF
15	C_{VC3}	0.1	0 to 0.33	µF
16	C_{VC4}	0.1	0 to 0.33	µF
17	C_{CCT}	0.1	0.01 or higher	µF
18	C_{CDT}	0.1	0.02 or higher	µF
19	C_{VSS}	1	0 to 10	µF

Caution The standard circuit above does not guarantee proper operation. Evaluation in the actual application is needed to determine the correct constants.

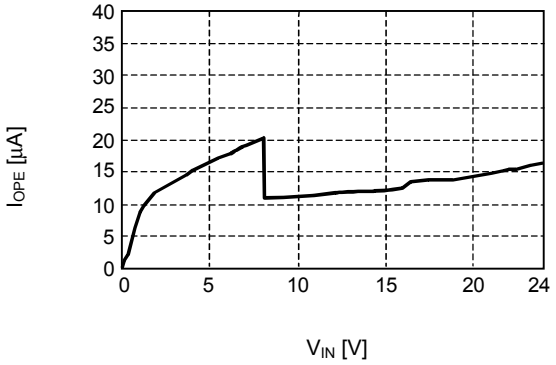
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Batteries can be connected in any order, however, there may be cases when discharging cannot be performed when a battery is connected. In this case, short the VMP and VDD pins or connect the battery charger to return to the normal mode.
- When an overcharged battery and an overdischarged battery intermix, the circuit is in both the overcharge and overdischarge statuses, so charging and discharging are not possible.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

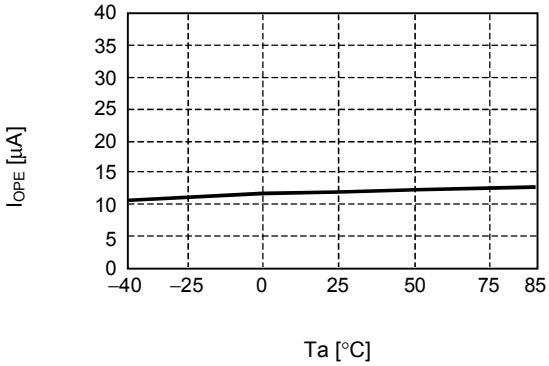
■ Characteristics (Typical Data)

(1) Current consumption

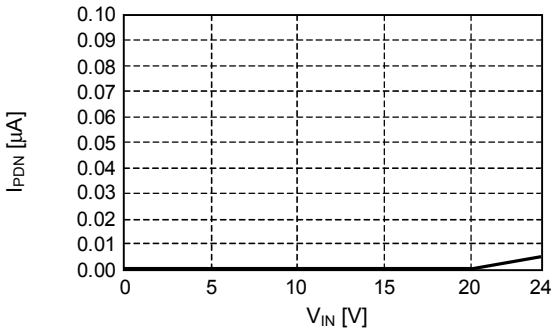
1. I_{OPE}-V_{IN}



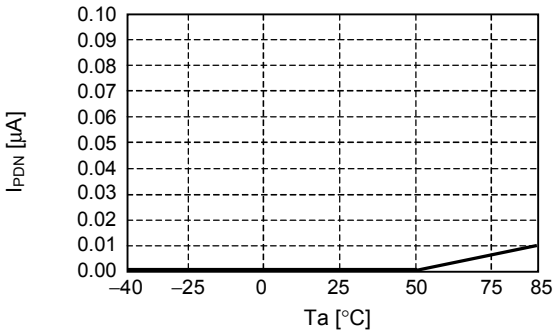
2. I_{OPE}-Ta



3. I_{PDN}-V_{IN}

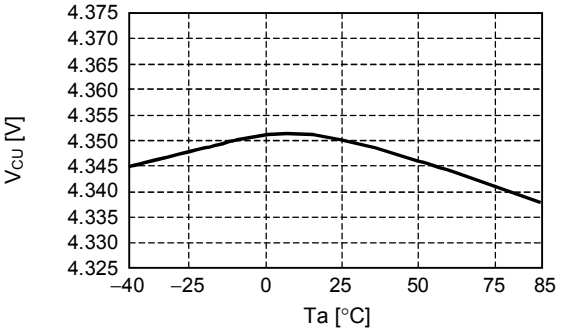


4. I_{PDN}-Ta

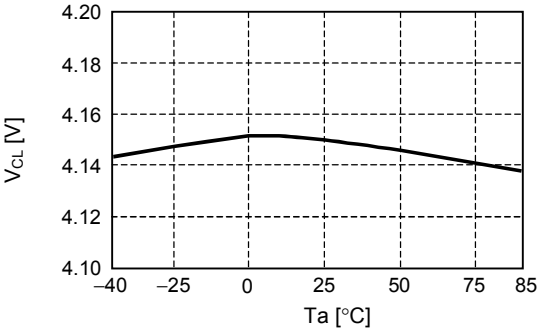


(2) Overcharge detection/release voltage, overdischarge detection/release voltage, overcurrent detection voltage, and delay times

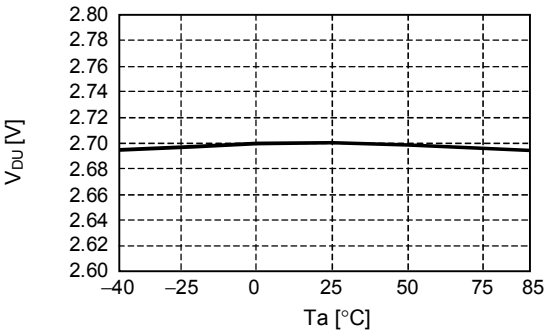
1. V_{CU}-Ta



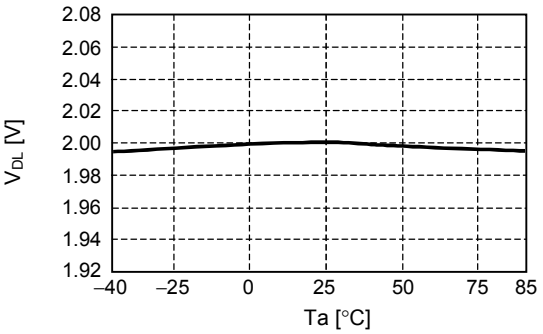
2. V_{CL}-Ta



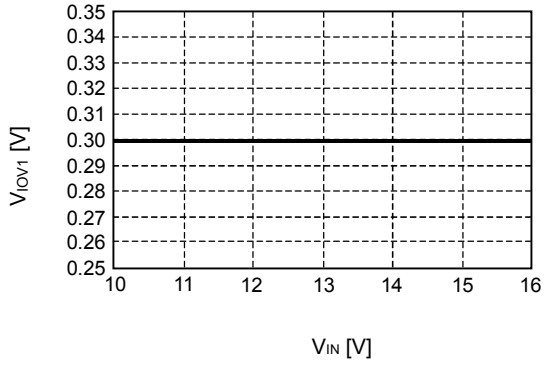
3. V_{DU}-Ta



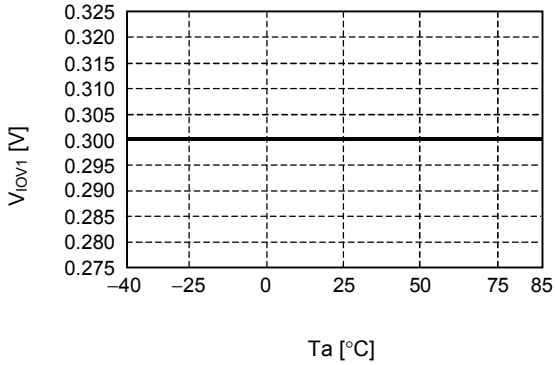
4. V_{DL}-Ta



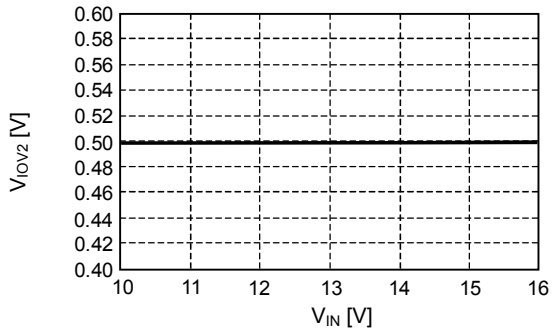
5. V_{IOV1}-V_{IN}



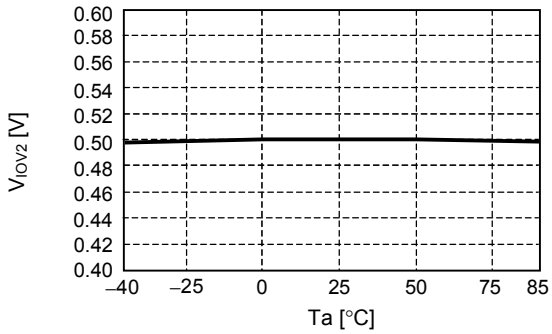
6. V_{IOV1}-Ta



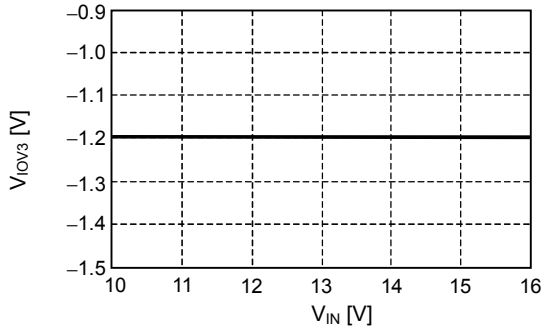
7. V_{IOV2}-V_{IN}



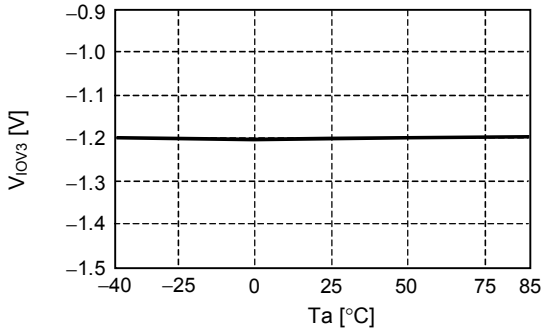
8. V_{IOV2}-Ta



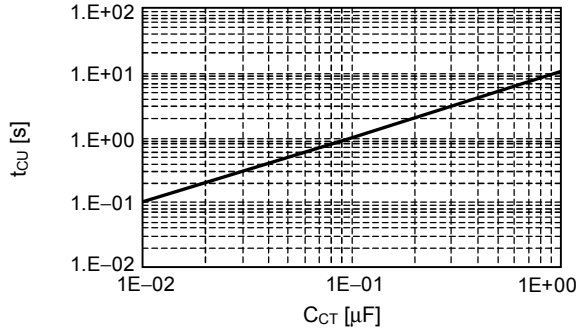
9. V_{IOV3}-V_{IN}



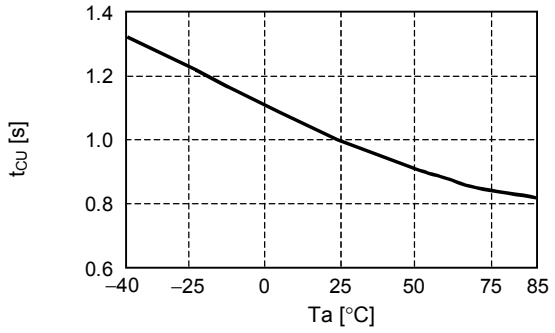
10. V_{IOV3}-Ta



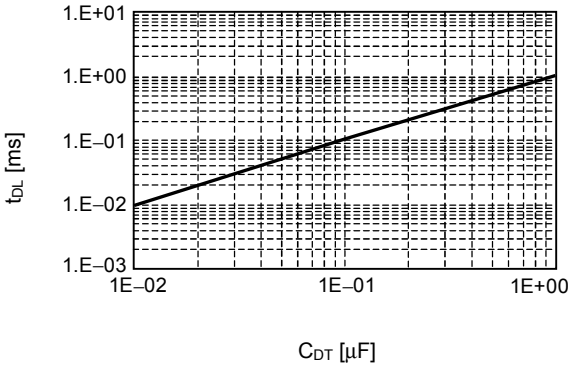
11. t_{CU}-C_{CT}



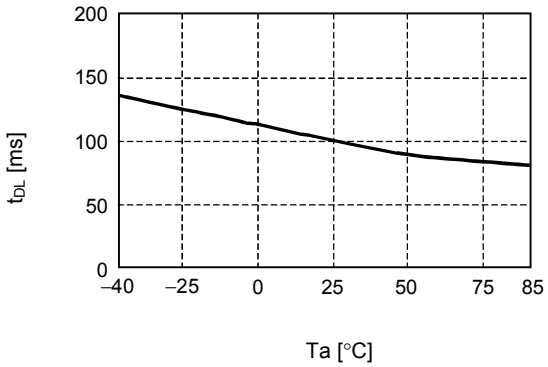
12. t_{CU}-Ta



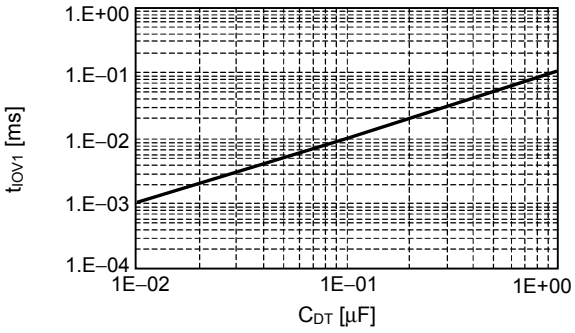
13. t_{DL}-C_{DT}



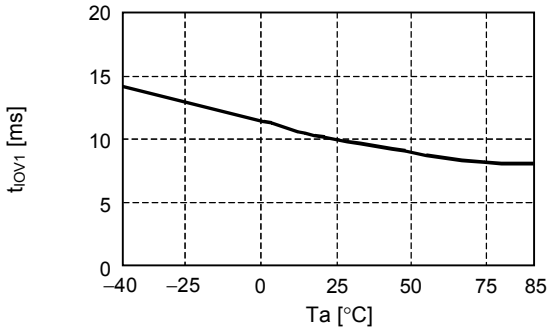
14. t_{DL}-Ta



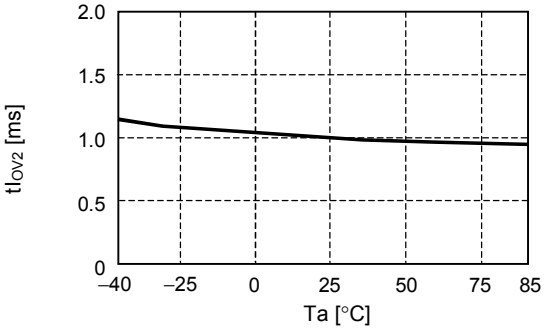
15. t_{IOV1}-CDT



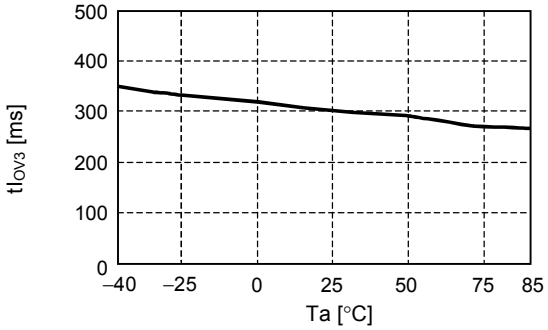
16. t_{IOV1}-Ta



17. t_{IOV2}-Ta

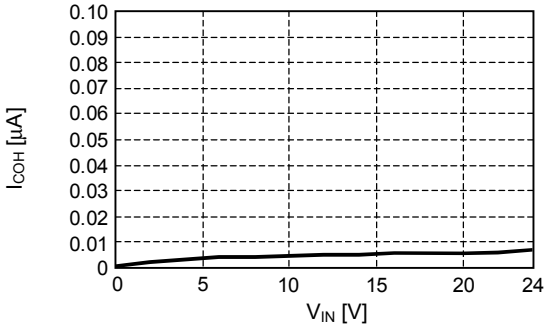


18. t_{IOV3}-Ta

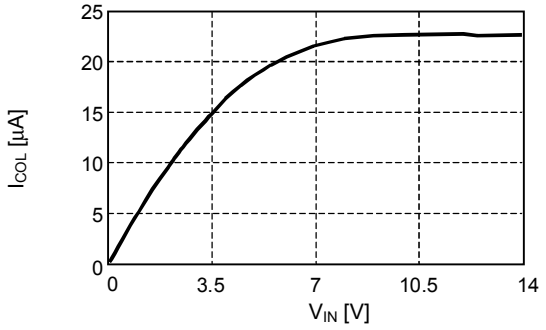


(3) COP/DOP pin

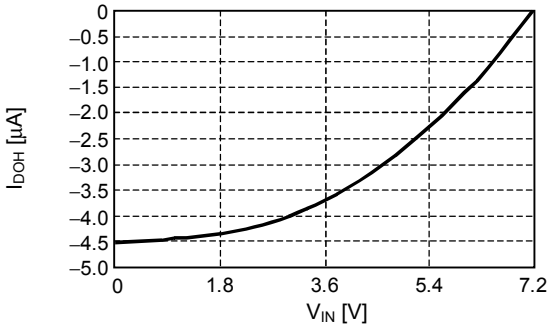
1. I_{COH}-V_{IN}



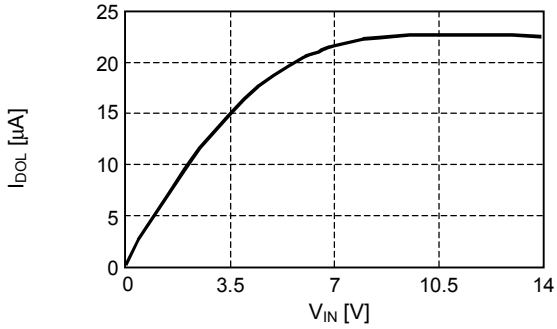
2. I_{COL}-V_{IN}

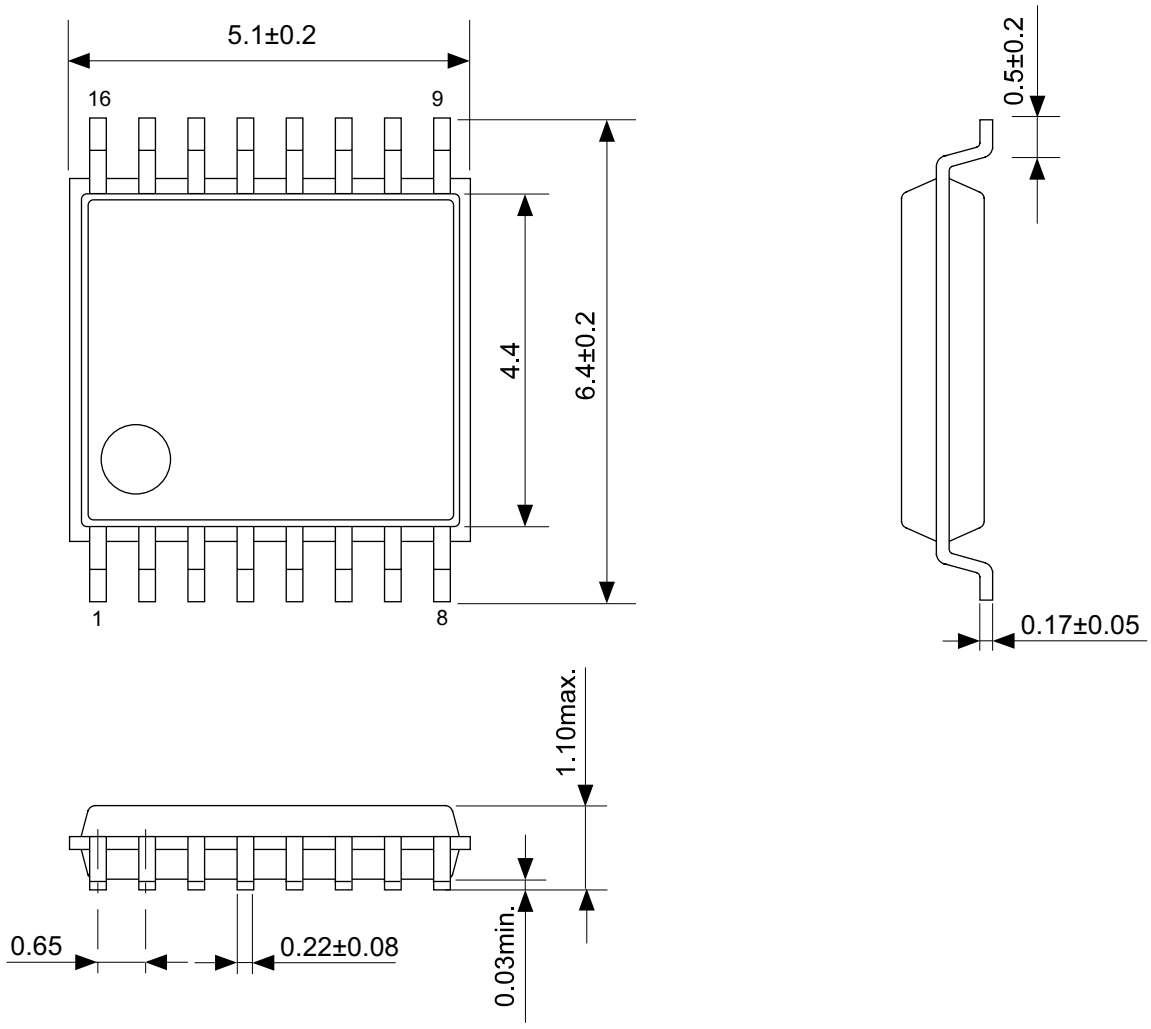


3. I_{DOH}-V_{IN}



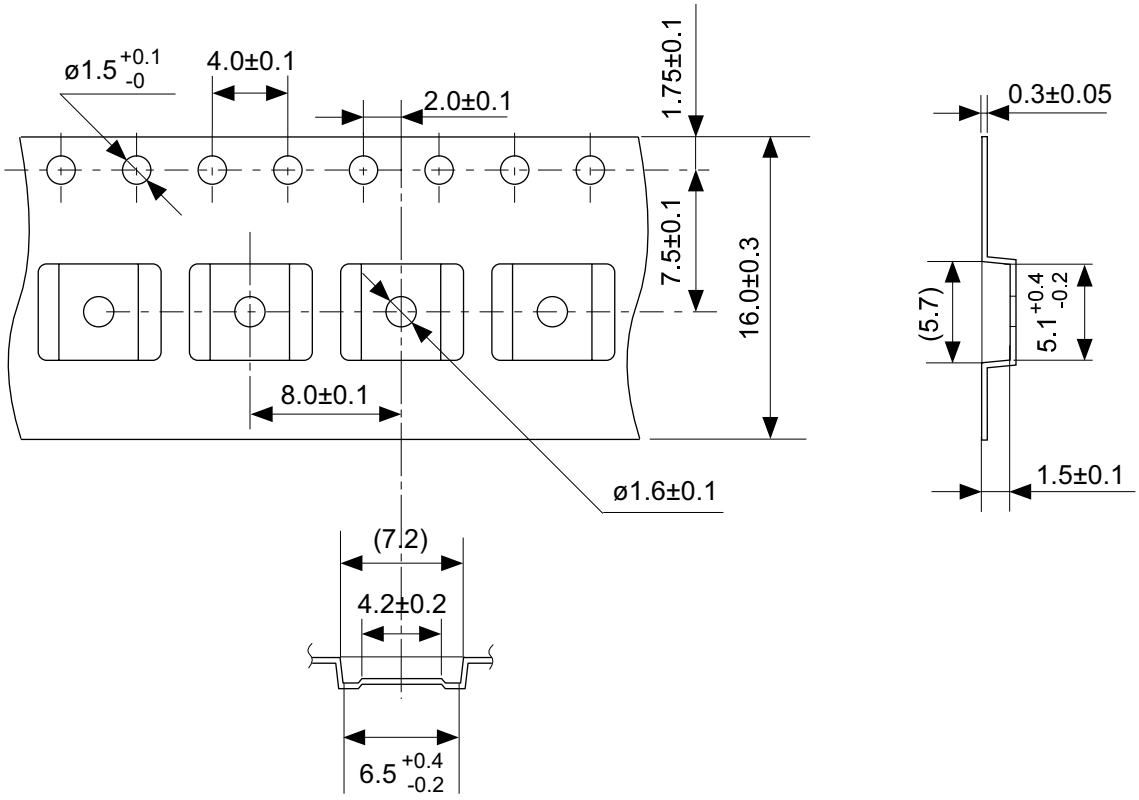
4. I_{DOL}-V_{IN}

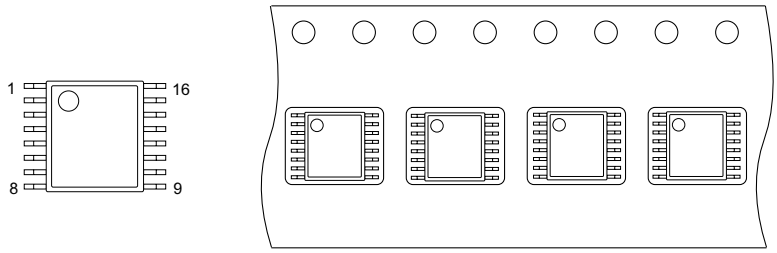




No. FT016-A-P-SD-1.1

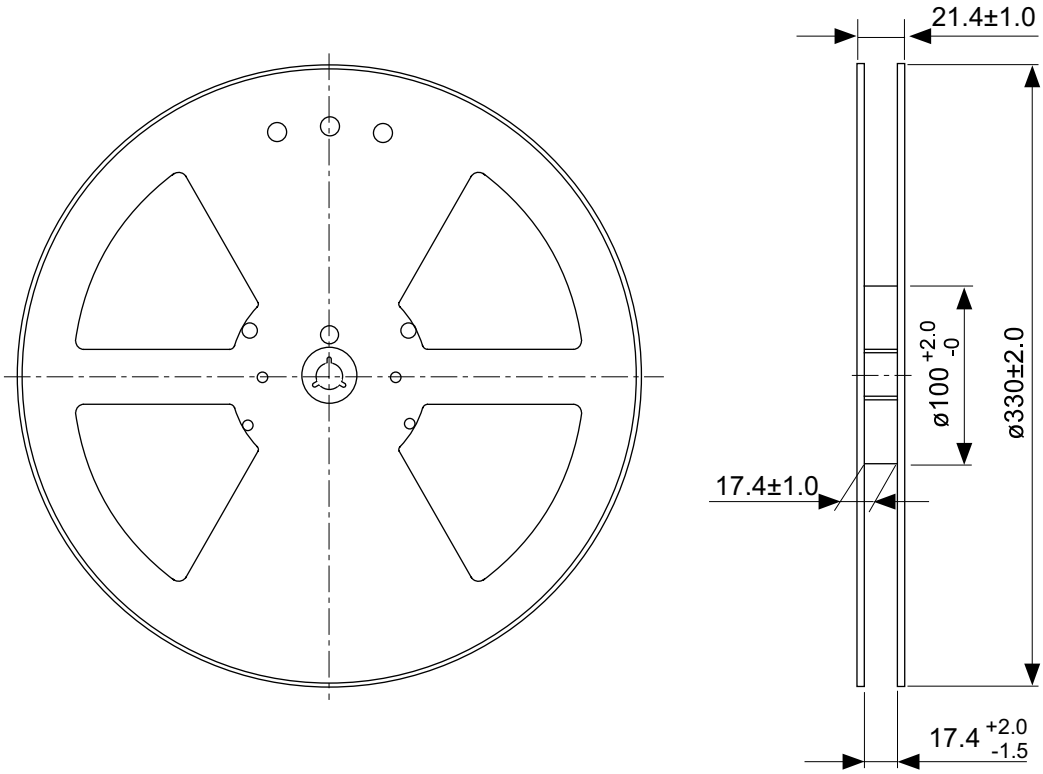
TITLE	TSSOP16-A-PKG Dimensions
No.	FT016-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



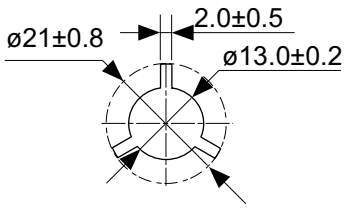


No. FT016-A-C-SD-1.1

TITLE	TSSOP16-A-Carrier Tape
No.	FT016-A-C-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FT016-A-R-SD-1.1

TITLE	TSSOP16-A- Reel		
No.	FT016-A-R-SD-1.1		
SCALE		QTY.	2,000
UNIT	mm		
Seiko Instruments Inc.			

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