SINO WEALTH

SH69P43

OTP 4-bit Microcontroller with SAR 8-bit A/D Converter

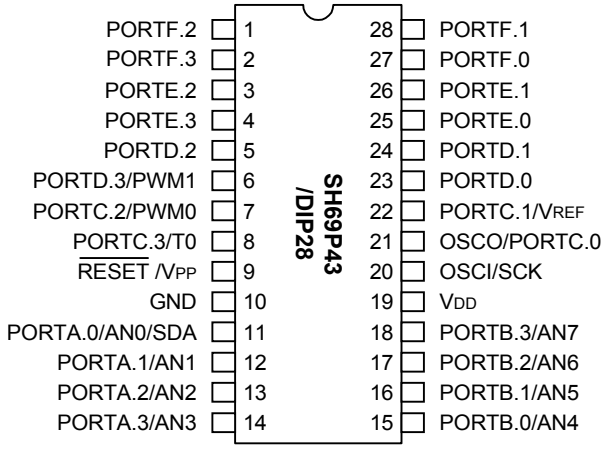
Features

- SH6610D-based single-chip 4-bit microcontroller with 8-bit SAR A/D converter
- OTP ROM: 3072 X 16 bits
- RAM: 192 X 4 bits
  - System register: 48 X 4 bits
  - Data memory: 144 X 4 bits
- Operation voltage:
  - f_{OSC}=400KHz - 4MHz, V_{DD}=2.4V - 5.5V
  - f_{OSC}=8MHz, V_{DD}=4.5V - 5.5V
- 24 CMOS bi-directional I/O pins
- Built in pull-up for I/O port
- Two 8-bit auto re-load timer/counter, One can switch to external clock source
- 8-level subroutine nesting (including interrupts)
- Powerful interrupt sources:
  - A/D interrupt
  - Internal interrupt (Timer1, Timer0)
  - External interrupts: Port A~D (Falling edge)
- Oscillator: (OTP option)
  - Crystal oscillator: 32768Hz, 400KHz ~ 8MHz
  - Ceramic resonator: 400K ~ 8MHz
  - External R_{OSC} RC oscillator: 400K ~ 8MHz
  - Internal R_{OSC} RC oscillator: 4MHz
  - External clock: 30K ~ 8MHz
- Instruction cycle time:
  - 4/32.768KHz (≈122μs) for 32.768KHz
  - 4/8MHz (= 0.5μs) for 8MHz at V_{DD}=5.0V
- 8 channels 8-bit resolution A/D converter
- 2 channels 10-bit PWM output
- Warm-up timer for power on reset
- Low voltage reset function (LVR)
- Internal reliable reset circuit
- Built-in watchdog timer
- Two low power operation modes: HALT and STOP
- OTP type/Code protection
- 28-pin DIP/SOP package

General Description

The SH69P43 is an advanced CMOS 4-bit microcontroller. It provide the following standard features: 3K bytes of OTPROM, 192 bytes of RAM, 8-bit timer/counter, 8-bit A/D converter, 10-bit high speed PWM output, on-chip oscillator clock circuitry, on-chip watchdog timer, low voltage reset function and support power saving modes to reduce power consumption.

Pin Configuration

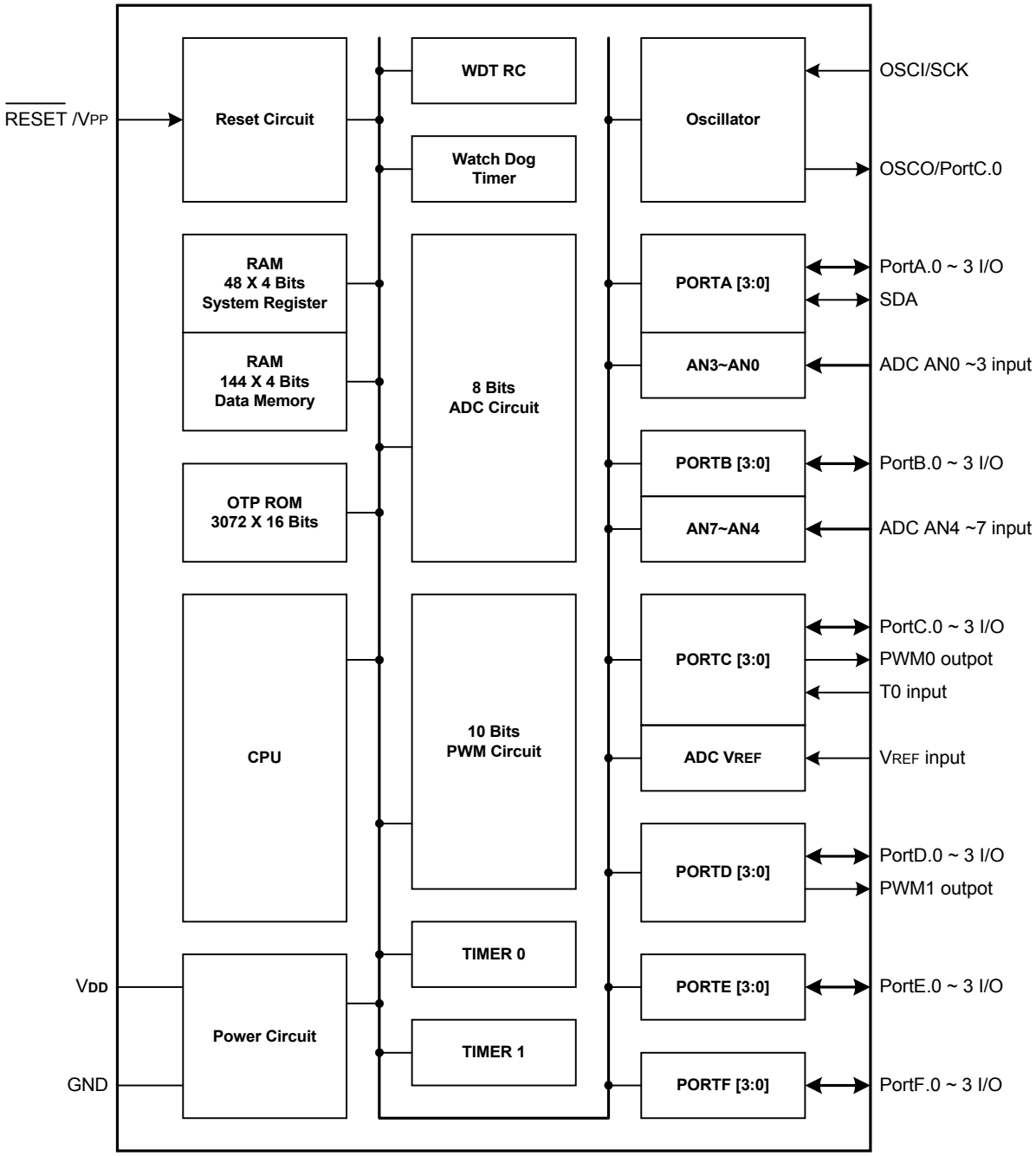


Pin Descriptions

Pin No.	Designation	I/O	Description
1, 2	PORTF.2 ~ 3	I/O	Bit programmable bi-directional I/O port
3, 4	PORTE.2 ~ 3	I/O	Bit programmable bi-directional I/O port
5	PORTD.2	I/O I	Bit programmable bi-directional I/O port Vector port interrupt. (active falling edge)
6	PORTD.3 /PWM1	I/O I O	Bit programmable bi-directional I/O port Vector port interrupt. (active falling edge) Shared with PWM1 output
7	PORTC.2 /PWM0	I/O I O	Bit programmable bi-directional I/O port Vector port interrupt. (active falling edge) Shared with PWM0 output
8	PORTC.3 /T0	I/O I I	Bit programmable bi-directional I/O port Vector port interrupt. (active falling edge) Shared with T0 input
9	$\overline{\text{RESET}}$ /V_{PP}	I P	Reset pin input, (low active) In the OTP program mode, Shared with V_{PP} power input.
10	GND	P	Ground pad
11	PORTA.0 /AN0 /SDA	I/O I I I/O	Bit programmable bi-directional I/O port Vector port interrupt. (active falling edge) Shared with ADC input channel In the OTP program mode, Shared with data I/O.
12, 13, 14	PORTA.1 ~ 3 /AN1 ~3	I/O I I	Bit programmable bi-directional I/O port Vector port interrupt. (active falling edge) Shared with ADC input channel AN1 ~ AN3
15, 16, 17, 18	PORTB.0 ~ 3 /AN4 ~ 7	I/O I I	Bit programmable bi-directional I/O port Vector port interrupt. (active falling edge) Shared with ADC input channel AN4 ~ AN7
19	V_{DD}	P	Power supply 2.4V ~ 5.5V
20	OSCI /SCK	I	Oscillator input pin, connect to crystal/ceramic oscillator or external resistor of RC oscillator. When internal RC oscillator is used, OSCI pin must be left open-circuit. In the OTP program mode, Shared with clock input.
21	OSCO /PORTC.0	O I/O I	Oscillator output pin, connect to crystal/ceramic oscillator. When RC oscillator is used, It is shared with PortC.0. Shared with bit programmable bi-directional I/O port Vector port interrupt. (active falling edge), if it is PortC.0 input.
22	PORTC.1 /V_{REF}	I/O I I	Bit programmable bi-directional I/O port Vector port interrupt. (active falling edge) Shared with external ADC V_{REF} input
23, 24	PORTD.0 ~ 1	I/O I	Bit programmable bi-directional I/O port Vector port interrupt. (active falling edge)
25, 26	PORTE.0 ~ 1	I/O	Bit programmable bi-directional I/O port
27, 28	PORTF.0 ~ 1	I/O	Bit programmable bi-directional I/O port

Total 28 pins.

Block Diagram



Functional Description

1. CPU

The CPU contains the following functional blocks: Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

(a) PC

The PC is used for ROM addressing consisting of 12-bits: Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0). The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.
The program counter cans only 4K program ROM address. (Refer to the ROM description).

(b) ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:
Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BC)
Logic Shift (SHR)
The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or call instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

(c) Accumulator

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

(d) Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The Table Branch Register (TBR) and Accumulator (A) is placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, A)). The address is determined by RTNW to return look-up value into (TBR, A). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into A.

(e) Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bits), DPM (3-bits) and DPL (4-bits). The addressing range can have 3FFH locations. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9 - bit0 comes from DPH, DPM and DPL.

(f) Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 8 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC with the return instructions (RTNI/RTNW).

Note:
The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 8 levels. If the number of calls and interrupt requests exceeds 8, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. RAM

Built-in RAM contains of general-purpose data memory and system register.

(a) RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:
$000 - $02F: System register and I/O
$030 - $0BF: Data memory (144 X 4 bits)

(b) Data Memory

Data memory is organized as 144 X 4 bits ($030 - $0BF). Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT.

(c) Configuration of System Register:

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEAD	IET0	IET1	IEP	R/W	Interrupt enable flags
$01	IRQAD	IRQT0	IRQT1	IRQP	R/W	Interrupt request flags
$02	-	T0M.2	T0M.1	T0M.0	R/W	Bit2-0: Timer0 Mode register
$03	-	T1M.2	T1M.1	T1M.0	R/W	Bit2-0: Timer1 Mode register
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load / counter register low nibble
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load / counter register high nibble
$06	T1L.3	T1L.2	T1L.1	T1L.0	R/W	Timer1 load / counter register low nibble
$07	T1H.3	T1H.2	T1H.1	T1H.0	R/W	Timer1 load / counter register high nibble
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE
$0D	PF.3	PF.2	PF.1	PF.0	R/W	PORTF
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	VREFS	ACR2	ACR1	ACR0	R/W	Bit2-0: A/D port configuration control Bit3: Select Internal/External reference voltage
$14	ADCON	CH2	CH1	CH0	R/W	Bit2-0: Select ADC channel Bit3: Set ADC module operate
$15	A3	A2	A1	A0	R	ADC data low nibble (Read only)
$16	A7	A6	A5	A4	R	ADC data high nibble (Read only)
$17	GO/$\overline{\text{DONE}}$	TADC1	TADC0	ADCS	R/W	Bit0: Set A/D Conversion Time Bit2, Bit1: Select A/D Clock Period Bit3: ADC status flag
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control
$1C	PECR.3	PECR.2	PECR.1	PECR.0	R/W	PORTE input/output control
$1D	PFCR.3	PFCR.2	PFCR.1	PFCR.0	R/W	PORTF input/output control
$1E	-	-	T0S	T0E	R/W	Bit0: T0 signal edge Bit1: T0 signal source
$1F	WD	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watch dog timer control Bit3: Watchdog timer overflow flag (Read only)

Configuration of System Register (continue):

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$20	PWM0S	T0CK1	T0CK0	PWM0	R/W	Bit0: Select PWM0 output Bit2, Bit1: Set PWM0 clock Bit3: Set PWM0 output mode of duty cycle
$21	PWM1S	T1CK1	T1CK0	PWM1	R/W	Bit0: Select PWM1 output Bit2, Bit1: Set PWM1 clock Bit3: Set PWM1 output mode of duty cycle
$22	PP0.3	PP0.2	PP0.1	PP0.0	R/W	PWM0 period low nibble
$23	PP0.7	PP0.6	PP0.5	PP0.4	R/W	PWM0 period middle nibble
$24	-	-	PP0.9	PP0.8	R/W	Bit1, Bit0: PWM0 period high nibble
$25	PD0.3	PD0.2	PD0.1	PD0.0	R/W	PWM0 duty low nibble
$26	PD0.7	PD0.6	PD0.5	PD0.4	R/W	PWM0 duty middle nibble
$27	-	-	PD0.9	PD0.8	R/W	Bit1, Bit0: PWM0 duty high nibble
$28	PP1.3	PP1.2	PP1.1	PP1.0	R/W	PWM1 period low nibble
$29	PP1.7	PP1.6	PP1.5	PP1.4	R/W	PWM1 period middle nibble
$2A	-	-	PP1.9	PP1.8	R/W	Bit1, Bit0: PWM1 period high nibble
$2B	PD1.3	PD1.2	PD1.1	PD1.0	R/W	PWM1 duty low nibble
$2C	PD1.7	PD1.6	PD1.5	PD1.4	R/W	PWM1 duty middle nibble
$2D	-	-	PD1.9	PD1.8	R/W	Bit1, Bit0: PWM1 duty high nibble
$2E	-	-	-	-	-	Reserved
$2F	-	-	-	-	-	Reserved

(d) System Register state:

	Bit 3	Bit 2	Bit 1	Bit 0	Power On Reset /Pin Reset / Low Voltage Reset	WDT Reset
$00	IEAD	IET0	IET1	IEP	0000	0000
$01	IRQAD	IRQT0	IRQT1	IRQP	0000	0000
$02	-	T0M.2	T0M.1	T0M.0	-000	-uuu
$03	-	T1M.2	T1M.1	T1M.0	-000	-uuu
$04	T0L.3	T0L.2	T0L.1	T0L.0	xxxx	xxxx
$05	T0H.3	T0H.2	T0H.1	T0H.0	xxxx	xxxx
$06	T1L.3	T1L.2	T1L.1	T1L.0	xxxx	xxxx
$07	T1H.3	T1H.2	T1H.1	T1H.0	xxxx	xxxx
$08	PA.3	PA.2	PA.1	PA.0	0000	0000
$09	PB.3	PB.2	PB.1	PB.0	0000	0000
$0A	PC.3	PC.2	PC.1	PC.0	0000	0000
$0B	PD.3	PD.2	PD.1	PD.0	0000	0000
$0C	PE.3	PE.2	PE.1	PE.0	0000	0000
$0D	PF.3	PF.2	PF.1	PF.0	0000	0000
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	uuuu
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-uuu
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-uuu
$13	VREFS	ACR2	ACR1	ACR0	0000	uuuu
$14	ADCON	CH2	CH1	CH0	0000	0uuu
$15	A3	A2	A1	A0	xxxx	uuuu
$16	A7	A6	A5	A4	xxxx	uuuu
$17	GO/$\overline{\text{DONE}}$	TADC1	TADC0	ADCS	0000	0uuu
$18	PACR.3	PACR.2	PACR.1	PACR.0	0000	0000
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000	0000
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	0000	0000
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	0000	0000
$1C	PECR.3	PECR.2	PECR.1	PECR.0	0000	0000
$1D	PFCR.3	PFCR.2	PFCR.1	PFCR.0	0000	0000
$1E	-	-	T0S	T0E	--00	--uu
$1F	WD	WDT.2	WDT.1	WDT.0	0000	1000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

System Register state (continue):

	Bit 3	Bit 2	Bit 1	Bit 0	Power On Reset /Pin Reset / Low Voltage Reset	WDT Reset
$20	PWM0S	T0CK1	T0CK0	PWM0	0000	uuu0
$21	PWM1S	T1CK1	T1CK0	PWM1	0000	uuu0
$22	PP0.3	PP0.2	PP0.1	PP0.0	xxxx	uuuu
$23	PP0.7	PP0.6	PP0.5	PP0.4	xxxx	uuuu
$24	-	-	PP0.9	PP0.8	--xx	--uu
$25	PD0.3	PD0.2	PD0.1	PD0.0	xxxx	uuuu
$26	PD0.7	PD0.6	PD0.5	PD0.4	xxxx	uuuu
$27	-	-	PD0.9	PD0.8	--xx	--uu
$28	PP1.3	PP1.2	PP1.1	PP1.0	xxxx	uuuu
$29	PP1.7	PP1.6	PP1.5	PP1.4	xxxx	uuuu
$2A	-	-	PP1.9	PP1.8	--xx	--uu
$2B	PD1.3	PD1.2	PD1.1	PD1.0	xxxx	uuuu
$2C	PD1.7	PD1.6	PD1.5	PD1.4	xxxx	uuuu
$2D	-	-	PD1.9	PD1.8	--xx	--uu

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

(e) Others initial state:

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

3. ROM

The ROM can address 3072 words X 16 bits of program area from $000H to $BFFH.

(a) Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
000H	JMP instruction	Jump to RESET service routine
001H	JMP instruction	Jump to ADC interrupt service routine
002H	JMP instruction	Jump to TIMER0 interrupt service routine
003H	JMP instruction	Jump to TIMER1 interrupt service routine
004H	JMP instruction	Jump to Port interrupt service routine

*JMP instruction can be replaced by any instruction.

4. System Clock and Oscillator

SH69P43 has one clock source. Oscillator is determined by OTP option. The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.

System clock = $F_{OSC}/4$.

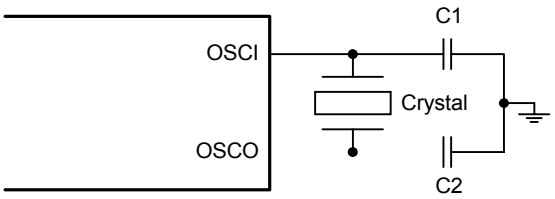
(a) Instruction cycle time:

(1) 4/32768Hz (≈122.1μs) for 32768Hz oscillator.

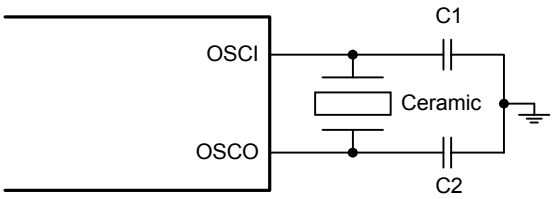
(2) 4/8MHz (=0.5μs) for 8MHz oscillator.

(b) Oscillator type

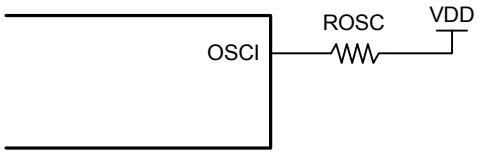
(1) Crystal oscillator: 32768Hz or 400KHz ~ 8MHz



(2) Ceramic resonator: 400KHz ~ 8MHz



(3) RC oscillator: 400KHz - 8MHz



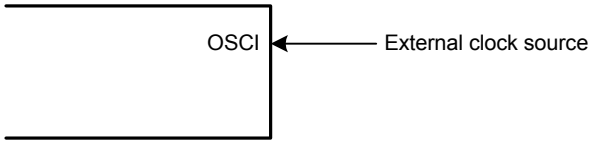
External R_{OSC} RC

Internal R_{OSC} RC (f_{OSC}=4MHz ±2MHz)

Note:

- If selected RC oscillator, OSCO pin is shared with I/O port (PortC.0).

(4) External input clock: 30KHz ~ 8MHz



5. I/O Port

The MCU provides 24 general purpose I/O ports. Each I/O port contains pull-up MOS controllable by the program. Pull-up MOS is controlled by the port data registers (PDR) of each port also when the Port is input port (Write “1” could turn on the pull-up MOS and write “0” could turn off the pull-up MOS). So the pull-up MOS can be turned on and off individually. The port control register (PCR) controls the I/O port’s direction (input or output). When PortA, B, C, D is digital input direction, it cans active port interrupt by falling edge (if port interrupt is enabled).

- PortA.0~3 can be shared with ADC AN0~3 input channel,
- PortB.0~3 can be shared with ADC AN4~7 input channel,
- PortC.0 can be shared with OSCO pin, (if used External clock or RC oscillator, OTP option)
- PortC.1 can be shared with ADC reference voltage input,
- PortC.2 can be shared with PWM0 output,
- PortC.3 can be shared with T0 input,
- PortD.3 can be shared with PWM1 output.

System Register $08 ~ $0D: Port Data Register (PDR)

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE
$0D	PF.3	PF.2	PF.1	PF.0	R/W	PORTF

System Register $18 ~ $1D: Port Control Register (PCR)

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control
$1C	PECR.3	PECR.2	PECR.1	PECR.0	R/W	PORTE input/output control
$1D	PFCR.3	PFCR.2	PFCR.1	PFCR.0	R/W	PORTF input/output control

I/O control register:

PA (/B/C/D/E/F) CR.n, (n = 0, 1, 2, 3)

0: Set I/O as an input direction. (Default)

1: Set I/O as an output direction.

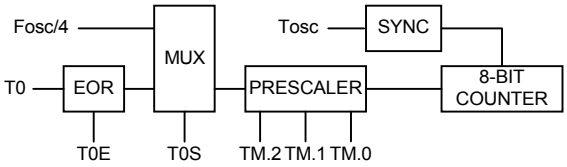
6. Timer

SH69P43 has two 8-bit timers.

The timer / counter has the following features:

- 8-bit up-counting timer/counter.
- Automatic re-loads counter.
- 8-level prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified timer block diagram.



The timers provide the following functions:

- Programmable interval timer function.
- Read counter value.

(a) Timer0 and Timer1 Configuration and Operation

Both the Timer0 and Timer1 consist of an 8-bit write-only timer load register (TL0L, TL0H; TL1L, TL1H) and an 8-bit read-only timer counter (TC0L, TC0H; TC1L, TC1H). Each of them has low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H; TL1L, TL1H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or counter counts overflow from $FF to $00.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:

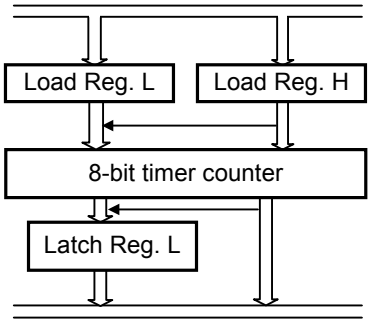
Low nibble first

High nibble to update the counter

Read Operation:

High Nibble first

Low nibble followed.



(b) Timer Mode Register

The timer can be programmed in several different prescaler ratios by setting Timer Mode register (TM0, TM1).

The 8-bit counter prescaler overflow output pulses. The Timer Mode registers (TM0, TM1) are 3-bit registers used for the timer control as shown in Table 1 and Table 2. These mode registers select the input pulse sources into the timer.

Table 1 Timer0 Mode Register ($02)

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock/T0
0	0	1	$/2^{9}$	System clock/T0
0	1	0	$/2^{7}$	System clock/T0
0	1	1	$/2^{5}$	System clock/T0
1	0	0	$/2^{3}$	System clock/T0
1	0	1	$/2^{2}$	System clock/T0
1	1	0	$/2^{1}$	System clock/T0
1	1	1	$/2^{0}$	System clock/T0

Table 2 Timer1 Mode Register ($03)

TM1.2	TM1.1	TM1.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

7. Analog/Digital Converter (ADC)

The 8 channels and 8-bit resolution A/D converter are implemented in this microcontroller.

The A/D converter system registers are $13~$17. The $13, $14 and $17(bit3, bit0) system registers are A/D converter control register, which defines the A/D channel number, analog channel select, reference voltage select, A/D conversion clock select, start A/D conversion control bit and the end of A/D conversion flag. The $15, $16 system registers are A/D conversion result register byte and are read-only.

The approach for A/D conversion:

- Set analog channel and select reference voltage. (When using the external reference voltage, keep in mind that any analog input voltage must not exceed V_{REF})
- Operating A/D converter module and select the converted analog channel.
- Set A/D conversion clock source.
- GO/$\overline{DONE}$ =1, start A/D conversion.

(a) Systems register $13:

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	VREFS	ACR2	ACR1	ACR0	R/W	Bit2-0: A/D port configuration control Bit3: Select Internal/External reference voltage
	X	0	0	0	R/W	See Table 3
	0	X	X	X	R/W	Internal reference voltage (V_{REF}=V_{DD})
	1	X	X	X	R/W	External reference voltage

Table 3 Set analog channels

ACR2	ACR1	ACR0	7	6	5	4	3	2	1	0
0	0	0	PB3	PB2	PB1	PB0	PA3	PA2	PA1	PA0
0	0	1	PB3	PB2	PB1	PB0	PA3	PA2	PA1	AN0
0	1	0	PB3	PB2	PB1	PB0	PA3	PA2	AN1	AN0
0	1	1	PB3	PB2	PB1	PB0	PA3	AN2	AN1	AN0
1	0	0	PB3	PB2	PB1	PB0	AN3	AN2	AN1	AN0
1	0	1	PB3	PB2	PB1	AN4	AN3	AN2	AN1	AN0
1	1	0	PB3	PB2	AN5	AN4	AN3	AN2	AN1	AN0
1	1	1	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

(b) Systems register $14:

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	ADCON	CH2	CH1	CH0	R/W	Bit2-0: Select ADC channel Bit3: Set ADC module operate
	X	0	0	0	R/W	ADC channel AN0
	X	0	0	1	R/W	ADC channel AN1
	X	0	1	0	R/W	ADC channel AN2
	X	0	1	1	R/W	ADC channel AN3
	X	1	0	0	R/W	ADC channel AN4
	X	1	0	1	R/W	ADC channel AN5
	X	1	1	0	R/W	ADC channel AN6
	X	1	1	1	R/W	ADC channel AN7
	0	X	X	X	R/W	A/D converter module not operating
	1	X	X	X	R/W	A/D converter module operating

(c) Systems register $15 ~ $16 for ADC data:

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$15	A3	A2	A1	A0	R	ADC data low nibble (Read only)
$16	A7	A6	A5	A4	R	ADC data high nibble (Read only)

(d) Systems register $17:

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$17	GO/$\overline{\text{DONE}}$	TADC1	TADC0	ADCS	R/W	Bit0: Set A/D Conversion Time Bit2, Bit1: Select A/D Clock Period Bit3: ADC status flag
	X	X	X	0	R/W	A/D Conversion Time = 50 t_{AD}
	X	X	X	1	R/W	A/D Conversion Time = 330 t_{AD}
	X	0	0	X	R/W	A/D Clock Period t_{AD} = t_{OSC}
	X	0	1	X	R/W	A/D Clock Period t_{AD} = 2 t_{OSC}
	X	1	0	X	R/W	A/D Clock Period t_{AD} = 4 t_{OSC}
	X	1	1	X	R/W	A/D Clock Period t_{AD} = 8 t_{OSC}
	0	X	X	X	R/W	A/D conversion not in progress
	1	X	X	X	R/W	A/D conversion in progress, when ADCON=1

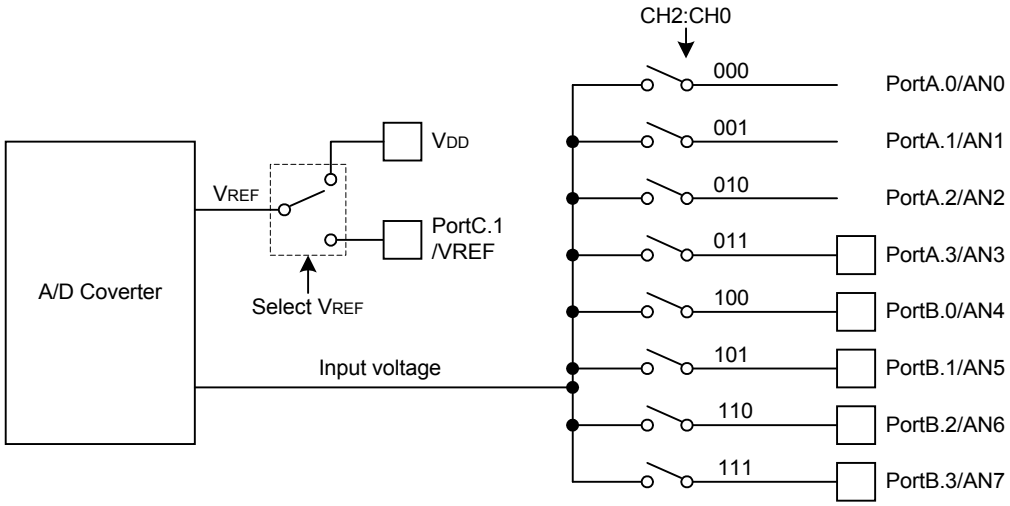


Figure 1 A/D Converter Block Diagram

Notice:

- Select A/D clock period t_{AD}, make sure that 1μs ≤ t_{AD} ≤ 33.4 μs.
- When the A/D conversion is complete, an A/D converter interrupt occurs (if the A/D converter interrupt is enabled).
- The analog input channels must have their corresponding PXCR (X=A, B) bits selected as inputs.
- If select I/O port as analog input, the I/O functions and pull up resistor are disabled.
- Bit GO/$\overline{\text{DONE}}$ is automatically cleared by hardware when the A/D conversion is complete.
- Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion.
- The A/D result register will NOT be updated with the partially completed A/D conversion sample.
- 4-t_{OSC} wait is required before the next acquisition is started.
- A/D converter could keep on working in HALT mode, and would stop automatic when execute "STOP" instruction.
- A/D converter could wake-up SH69P43 from HALT mode (if the A/D converter interrupt is enabled).

8. Pulse Width Modulation (PWM)

The 2 channels and 10-bit PWM output are implemented in this microcontroller. Set PWM output control by system registers PWMC. System registers PWMP set PWM output period cycle and PWMD set PWM output duty cycle.

Systems register $20, $21: (PWMC)

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$20, $21	PWMnS	TnCK1	TnCK0	PWMn	R/W	Bit0: Select PWMn output Bit2, Bit1: Set PWMn clock Bit3: Set PWMn output mode of duty cycle
	X	X	X	0	R/W	Shared with I/O port
	X	X	X	1	R/W	Shared with PWMn, n=0 or 1
	X	0	0	X	R/W	PWMn clock = t_{OSC}
	X	0	1	X	R/W	PWMn clock = $2t_{OSC}$
	X	1	0	X	R/W	PWMn clock = $4t_{OSC}$
	X	1	1	X	R/W	PWMn clock = $8t_{OSC}$
	0	X	X	X	R/W	PWMn output normal mode of duty cycle
	1	X	X	X	R/W	PWMn output negative mode of duty cycle

n=0 or 1

Systems register $22 ~ $24, $28 ~ $2A: (PWMP)

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$22, $28	PPn.3	PPn.2	PPn.1	PPn.0	R/W	PWMn period low nibble
$23, $29	PPn.7	PPn.6	PPn.5	PPn.4	R/W	PWMn period middle nibble
$24, $2A	-	-	PPn.9	PPn.8	R/W	Bit1, Bit0: PWMn period high nibble

n=0 or 1

PWM output period cycle = [PPn.9, PPn.0] x PWMn clock.

After write PWMn period low nibble ($22, $28), [PPn.9, PPn.0] data will be loaded into the re-load counter, start counting at next period.

When [PPn.9, PPn.0]=000H, PWM output GND.

Systems register $25 ~ $27, $2B ~ $2D: (PWMD)

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$25, $2B	PDn.3	PDn.2	PDn.1	PDn.0	R/W	PWMn duty low nibble
$26, $2C	PDn.7	PDn.6	PDn.5	PDn.4	R/W	PWMn duty middle nibble
$27, $2D	-	-	PDn.9	PDn.8	R/W	Bit1, Bit0: PWMn duty high nibble

n=0 or 1

PWM output duty cycle = [PDn.9, PDn.0] x PWMn clock.

After write PWMn duty low nibble ($25, $2B), [PDn.9, PDn.0] data will be loaded into the re-load counter, start counting at next period.

Notice:

- If select I/O port as PWM output, the I/O functions and pull up resistor are disabled.
- After the data are loaded into the re-load counter, start counting at next period.
- PWM could keep on working in HALT mode, and would stop automatic when execute "STOP" instruction.

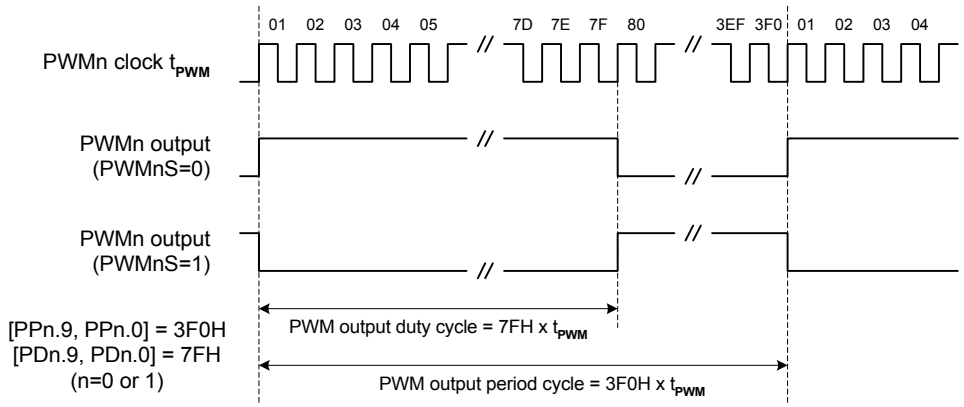


Figure 2 PWM output example

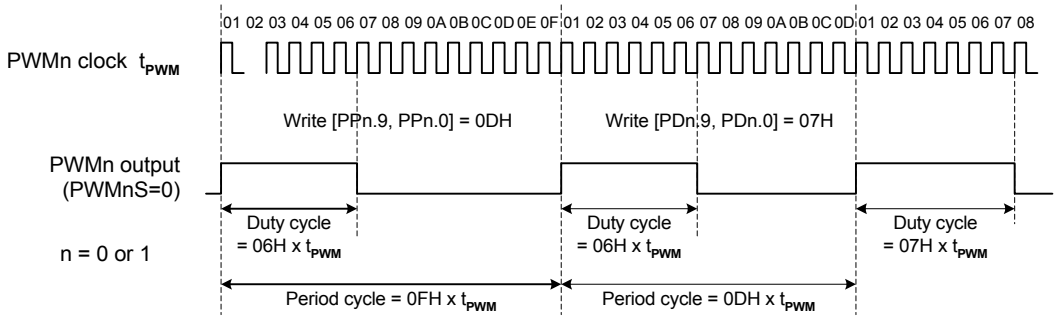


Figure 3 PWM output Period or Duty cycle changing example

9. Low Voltage Reset (LVR)

The LVR function is to monitor the supply voltage and generate an internal reset in the device. It is typically used in AC line applications or large battery where large loads may be switched in and cause the device voltage to temporarily fall below the specified operating minimum.

The LVR function is selected by OTP option.

The LVR circuit has the following functions when LVR function is enabled:

- Generates a system reset when $V_{DD} \leq V_{LVR}$ and $t \geq t_{LVR}$.
- Cancels the system reset when $V_{DD} > V_{LVR}$ or $V_{DD} < V_{LVR}$ and $t < 100\mu s$.

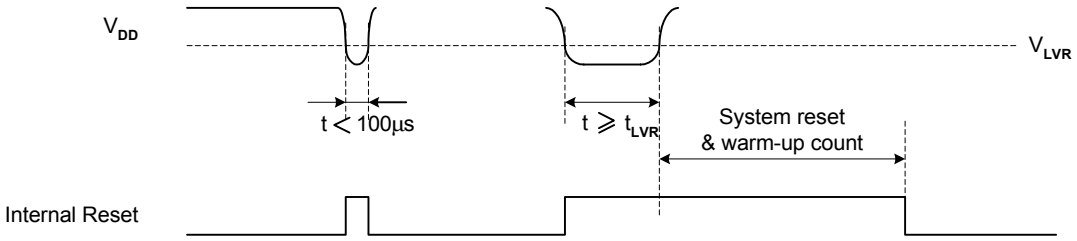


Figure 4 Low voltage reset example

10. External Clock/Event T0 as Timer0 Source

When external clock/event T0 input as Timer0 source, it is synchronized with the CPU system clock. The external source must follow certain constraints. The system clock samples it in instruction frame cycle. Therefore it is necessary to be high (at least 2 t_{OSC}) and low (at least 2 t_{OSC}). When the prescaler ratio selects /20, it is the same as the system clock input.

The requirement is as follows

T0H (T0 high time) $\geq 2\ t_{OSC} + \Delta T$

T0L (T0 low time) $\geq 2\ t_{OSC} + \Delta T$; ΔT= 40ns

When another prescaler ratio is selected, the TM0 is scaled by the asynchronous ripple counter and so the prescaler output is symmetrical. Then:

$$T0\ \text{high time} = T0\ \text{low time} = \frac{N * T0}{2}$$

Where: T0 = Timer0 input period

N = prescaler value

The requirement is:

$$\frac{N * T0}{2} \geq 2t_{OSC} + \Delta T \quad \text{or} \quad T0 \geq \frac{4 * t_{OSC} * 2\Delta T}{N}$$

So, the limitation is applied for the T0 period time only. The pulse width is not limited by this equation. It is summarized as follows:

$$T0 = \text{Timer0 period} \geq \frac{4 * t_{OSC} * 2\Delta T}{N}$$

Systems register $1E: (T0)

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1E	-	-	T0S	T0E	R/W	Bit0: T0 signal edge Bit1: T0 signal source
	-	-	X	0	R/W	Increment on low-to-high transition T0 pin
	-	-	X	1	R/W	Increment on high-to-low transition T0 pin
	-	-	0	X	R/W	Shared with PortC.3, Timer0 source is system clock
	-	-	1	X	R/W	Shared with T0 input, Timer0 source is T0 input clock

11. Interrupt

Four interrupt sources are available on SH69P43:

- A/D interrupt
- Timer0 interrupt
- Timer1 interrupt
- Port A~D interrupts (Falling edge)

(a) Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are cleared to 0 at initialization by the chip reset.

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEAD	IET0	IET1	IEP	R/W	Interrupt enable flags
$01	IRQAD	IRQT0	IRQT1	IRQP	R/W	Interrupt request flags

When IEx is set to 1 and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are reset to 0 automatically, so when IRQx is 1 and IEx is set to 1 again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.

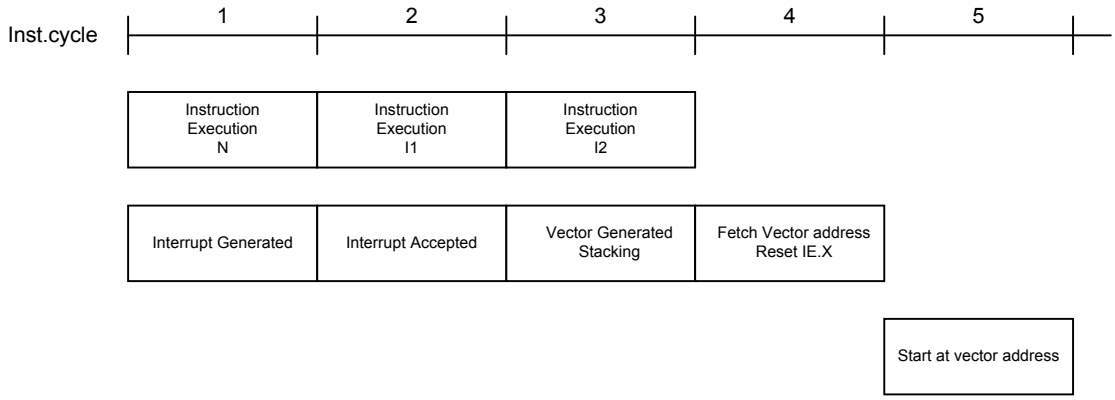


Figure 5 Interrupt Servicing Sequence Diagram

Interrupt Nesting:

During the SH6610D CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

(b) A/D interrupt

Bit3 (IEAD) of system register $00 is the ADC interrupt enable flag. When the A/D conversion is complete, It will generate an interrupt request (IRQAD=1), if the ADC interrupt is enabled (IEAD=1), an ADC interrupt service routine will start. The A/D interrupt can be used to wake the CPU from HALT mode.

(c) Timer (Timer0, Timer1) Interrupt

The input clock of Timer0 and Timer1 are based on system clock or external clock/event T0 input as Timer0 source. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQT0 or IRQT1=1), If the interrupt enable flag is enabled (IET0 or IET1=1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from HALT mode.

(d) Port Interrupt

The PortA ~ D are used as port interrupt sources. Since PortA ~ D I/O is bit programmable I/O, so only the digital input port can generate a port interrupt. The analog input can't generate an interrupt request.

Any one of the PortA ~ D input pin transitions from V_{DD} to GND would generate an interrupt request (IRQP=1). Further falling edge transition would not be able to make a new interrupt request until all of the input pins have returned to V_{DD}. Port Interrupt can be used to wake the CPU from HALT or STOP mode.

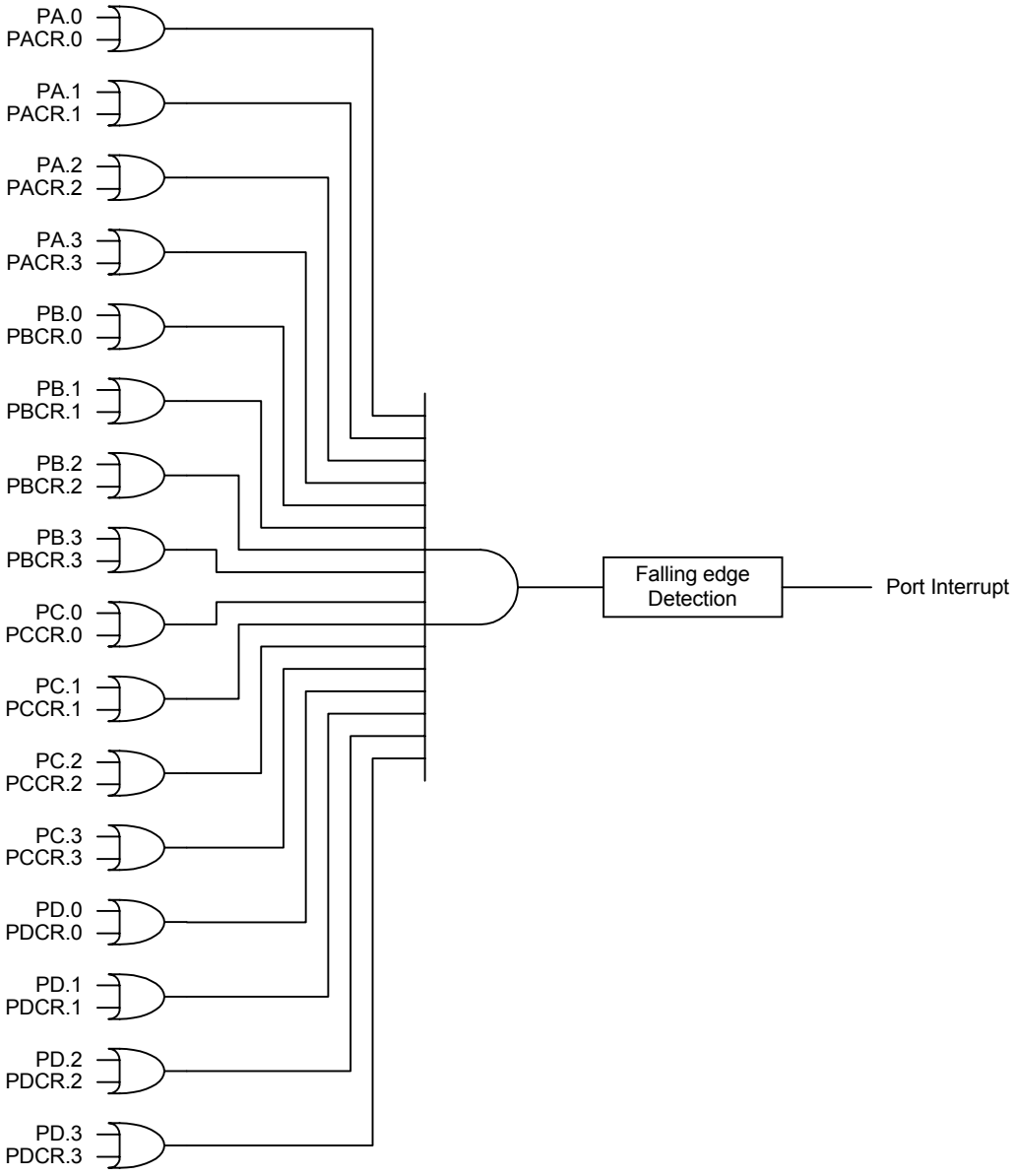


Figure 6 Port Interrupt function block-diagram

12. Watch Dog Timer (WDT)

Watch dog timer is a down-count counter, and its clock source is an independent built-in RC oscillator, so that the WDT will always run even in the STOP mode (if it is enabled). The watchdog timer automatically generates a device reset when it overflows. OTP option can enable and disable this function. The watchdog timer control registers (WDT bit2 ~ 0) is selects different overflow frequency. WDT bit3 is watchdog timer overflow flag.

If the Watchdog timer is enabled, the CPU will be reset when watchdog timer overflows. Repeat reads or writes WDT register ($1F), the watchdog timer should re-count before the overflow happens.

System Register $1F: (WDT)

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1F	WD	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watch dog timer control Bit3: Watchdog timer overflow flag (Read only)
	X	0	0	0	R/W	Watch dog timer-out period = 4096ms
	X	0	0	1	R/W	Watch dog timer-out period = 1024ms
	X	0	1	0	R/W	Watch dog timer-out period = 256ms
	X	0	1	1	R/W	Watch dog timer-out period = 128ms
	X	1	0	0	R/W	Watch dog timer-out period = 64ms
	X	1	0	1	R/W	Watch dog timer-out period = 16ms
	X	1	1	0	R/W	Watch dog timer-out period = 4ms
	X	1	1	1	R/W	Watch dog timer-out period = 1ms
	0	X	X	X	R	No watchdog timer overflow reset
	1	X	X	X	R	Watchdog timer overflow, WDT reset happens

Note: Watchdog timer-out period valid for V_{DD} = 5V.

13. HALT and STOP Mode

After the execution of HALT instruction, The device will enter halt mode. In the halt mode, CPU will stop operating. But peripheral circuit (Timer0, Timer1, ADC and watchdog timer) will keep operating.

After the execution of STOP instruction, The device will enter stop mode. In the stop mode, the whole chip (including oscillator) will stop operating without watchdog timer, if it is enabled.

In HALT mode, SH69P43 can be waked up if any interrupt occurs.

In STOP mode, SH69P43 can be waked up if port interrupt occurs or watchdog timer overflow (WDT is enabled).

14. Warm-up Timer

The device builds in oscillator warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

(a) Power on reset warm-up time interval:

(1) In RC oscillator mode, F_{OSC}=400KHz ~ 2MHz, the warm-up counter prescaler is divided by 2^{10} (1024).

(2) In RC oscillator mode, F_{OSC}=2MHz ~ 8MHz, the warm-up counter prescaler is divided by 2^{12} (4096).

(3) In crystal oscillator or ceramic resonator mode, the warm-up counter prescaler is divided by 2^{12} (4096).

(b) Others warm-up time interval:

- Hardware reset
- Low voltage reset
- Wake-up from stop mode

(1) In RC oscillator mode, F_{OSC}=400KHz ~ 8MHz, the warm-up counter prescaler is divided by 2^{7} (128).

(2) In crystal oscillator or ceramic resonator mode, the warm-up counter prescaler is divided by 2^{12} (4096).

15. OTP option

(a) Oscillator type:

000 = External clock (Default)
011 = Internal R_{OSC} RC oscillator
100 = External R_{OSC} RC oscillator
101 = Ceramic resonator
110 = Crystal oscillator
111 = 32.768KHz Crystal oscillator

(b) Oscillator range:

0 = 2 ~ 8MHz (Default)
1 = 400KHz ~ 2MHz

(c) Watch dog timer:

0 = Enable (Default)
1 = Disable

(d) Low Voltage Reset:

0 = Disable (Default)
1 = Enable

(e) LVR voltage Range:

0 = High LVR voltage (Default)
1 = Low LVR voltage

Instructions

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

1. Arithmetic and Logical Instruction

(a) Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3]; AC[0] → CY; AC shift right one bit	CY

(b) Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I +1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

2. Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx ←Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC, Mx ←Decimal adjust for sub	CY

3. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

4. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC +1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ← ST; TBR ← hhhh; AC ←lll	
RTNI	11010 1000 000 0000	CY, PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page		
ST	Stack	TBR	Table Branch Register

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +7.0V

Input / Output Voltage . . . . . GND-0.3V to VDD+0.3V

Operating Ambient Temperature . . . . . .-40℃ to +85℃

Storage Temperature . . . . . -55℃ to +125℃

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

1. DC Electrical Characteristics

(a) V_{DD} = 4.5V ~ 5.5V, GND = 0V, T_A = 25℃, F_{OSC} = 8MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	4.5	5.0	5.5	V	
Operating Current	I_{OP}	-	1.5	2	mA	All output pins unloaded (Execute NOP instruction)
Stand by Current (HALT)	I_{SB1}	-	-	500	μA	All output pins unload, WDT off, ADC disable
Stand by Current (STOP)	I_{SB2}	-	-	1	μA	All output pins unload, WDT off, ADC disable, LVR off
Input Low Voltage	V_{IL1}	GND	-	0.2 X V_{DD}	V	I/O Ports, pins tri-state
Input Low Voltage	V_{IL2}	GND	-	0.15 X V_{DD}	V	$\overline{\text{RESET}}$, T0, T1, OSCI
Input High Voltage	V_{IH1}	0.8 X V_{DD}	-	V_{DD}	V	I/O Ports, pins tri-state
Input High Voltage	V_{IH2}	0.85 X V_{DD}	-	V_{DD}	V	$\overline{\text{RESET}}$, T0, T1, OSCI
Input Leakage Current	I_{IL}	-1	-	1	μA	Input pad, V_{IN}=V_{DD} or GND
Pull-up Resistor	R_{PH}	-	150	-	KΩ	V_{IN}=GND
Output High Voltage	V_{OH}	V_{DD} - 0.7	-	-	V	I/O Ports, PWM0&1, I_{OH} = -10mA
Output Low Voltage	V_{OL}	-	-	GND + 0.6	V	I/O Ports, PWM0&1, I_{OL} = 20mA

(b) V_{DD} = 2.4V ~ 5.5V, GND = 0V, T_A = 25℃, F_{OSC} = 4MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.4	5.0	5.5	V	
Operating Current	I_{OP}	-	1.0	1.5	mA	All output pins unloaded (Execute NOP instruction)
Stand by Current (HALT)	I_{SB1}	-	-	300	μA	All output pins unload, WDT off, ADC disable
Stand by Current (STOP)	I_{SB2}	-	-	1	μA	All output pins unload, WDT off, ADC disable
Input Low Voltage	V_{IL1}	GND	-	0.2 X V_{DD}	V	I/O Ports, pins tri-state
Input Low Voltage	V_{IL2}	GND	-	0.15 X V_{DD}	V	$\overline{\text{RESET}}$, T0, T1, OSCI
Input High Voltage	V_{IH1}	0.8 X V_{DD}	-	V_{DD}	V	I/O Ports, pins tri-state
Input High Voltage	V_{IH2}	0.85 X V_{DD}	-	V_{DD}	V	$\overline{\text{RESET}}$, T0, T1, OSCI

2. AC Electrical Characteristics

(a) V_{DD} = 2.4V ~ 5.5V, GND = 0V, T_A = 25℃, F_{OSC} = 30KHz ~ 8MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Instruction cycle time	T_{CY}	0.5	-	133.4	μs	
T0 input width	t_{IW}	(T_{CY} + 40)/N	-	-	ns	N = Prescaler divide ratio
Input pulse width	t_{IPW}	t_{IW}/2	-	-	ns	

(b) V_{DD} = 2.4V ~ 5.5V, GND = 0V, T_A = 25℃, F_{OSC} = 30KHz ~ 8MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
RESET pulse width	t_{RESET}	10	-	-	μs	Low active
WDT Period	T_{WDT}	1	-	-	ms	V_{DD}=5.0V, 25℃
Frequency Variation	|ΔF|/F	-	-	20	%	External R_{OSC} Oscillator, Include supply voltage, temperature and chip-to-chip variation
Frequency Variation	|ΔF|/F	-	-	50	%	Internal R_{OSC} Oscillator, F_{OSC} = 4MHz Include supply voltage, temperature and chip-to-chip variation

3. A/D Converter Electrical Characteristics

(a) V_{DD} = 2.4V ~ 5.5V, GND = 0V, T_A = 25℃, F_{OSC} = 30KHz ~ 8MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Resolution	NR	-	-	8	bit	GND ≤ V_{AIN} ≤ V_{REF}
Reference Voltage	V_{REF}	2.4	-	V_{DD}	V	
A/D Input Voltage	V_{AIN}	GND	-	V_{REF}	V	
A/D Input Resistor	R_{AIN}	1000	-	-	KΩ	V_{IN}=5.0V
A/D conversion current	I_{AD}	-	300	500	μA	A/D converter module operating, V_{DD}=5.0V
Nonlinear Error	E_{NL}	-	-	±1	LSB	V_{REF} = V_{DD} = 5.0V
Full scale error	E_F	-	-	±1	LSB	V_{REF} = V_{DD} = 5.0V
Offset error	E_Z	-	-	±1	LSB	V_{REF} = V_{DD} = 5.0V
Total Absolute error	E_{AD}	-	±0.5	±1	LSB	V_{REF} = V_{DD} = 5.0V
A/D Clock Period	t_{AD}	1	-	33.4	μs	F_{OSC} = 30KHz ~ 8MHz
A/D Conversion Time	t_{CNV1}	-	50	-	t_{AD}	Set ADCS=0
A/D Conversion Time	t_{CNV2}	-	330	-	t_{AD}	Set ADCS=1

4. Low Voltage Reset Electrical Characteristics

(a) V_{DD} = 3.0V ~ 5.5V, GND = 0V, T_A = 25℃, F_{OSC} = 32.768KHz ~ 8MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LVR Voltage (High)	V_{LVR1}	3.8	-	4.2	V	LVR enable
LVR Voltage (Low)	V_{LVR2}	2.4	-	2.6	V	LVR enable
LVR Voltage Pulse Width	t_{LVR}	100	-	500	μs	V_{DD} ≤ V_{LVR}

Product SPEC. Change Notice

SH69P43 Specification Revision History		
Version	**Content**	**Date**
0.2	Part number change	Jan.2003
0.1	PII Spec.	Aug.2002
0.0	Original	Jul.2002