JA32010 Specifications

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CONTENT

1. Introduction

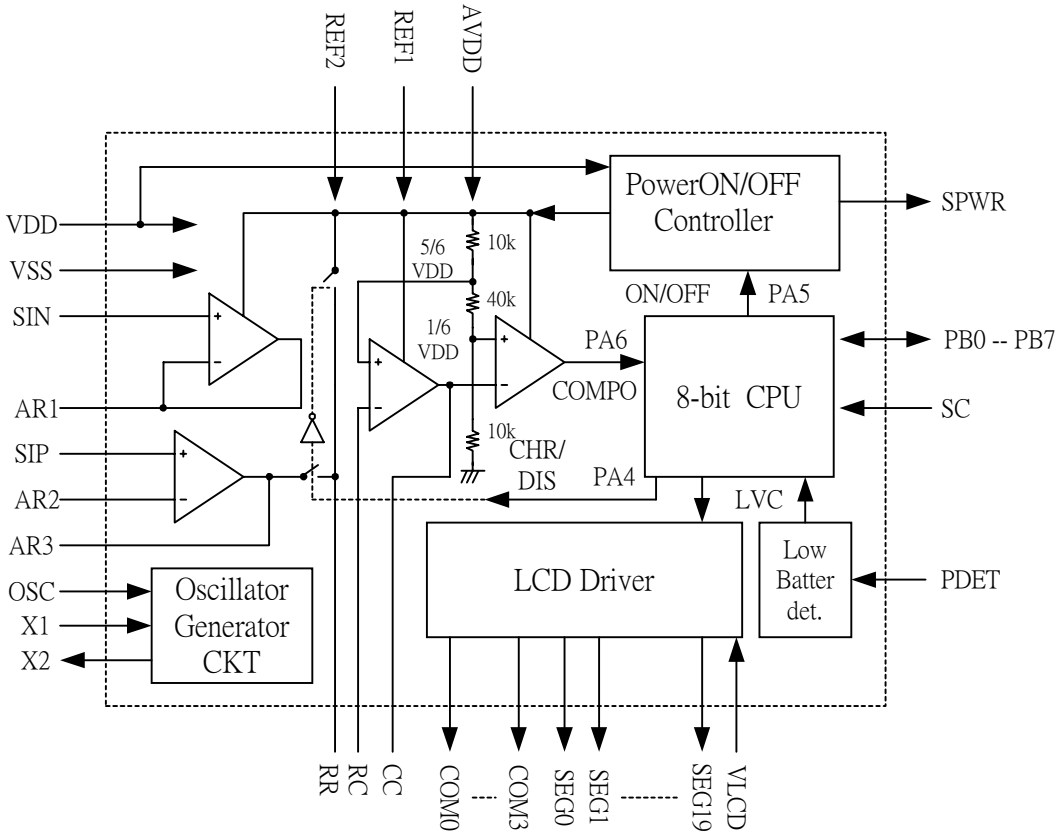
The JA32010 incorporates an 8-bit MCU, ADC, LCD controller, 8 programmable general I/Os and R/F circuits inside. It is designed for measuring application, especially suitable for pressure related product.

2. Features

The features for the JA32010 are listed as follows:

- Operating Voltage: 2.2 V ~ 5.2V
- Built-in LCD driver: 4 COM * 20 SEG
- LCD duty can option as 1/3 duty or 1/4 duty
- LCD bias can option as 1/2 bias or 1/3 bias
- Stand-by Current=1uA @VDD=3V
- Operating Current = 500uA @ Fsys=512K VDD=3V
- R-Bias or C-Bias for LCD by mask option
- R oscillation for system clock
- 32768 Hz for timer
- Internal with dual slope ADC and OP amplifier
- Low battery detect
- Internal with an 8-bit I/O port
- Internal with 16-bit and 8-bit timer
- 7K bytes of Program ROM
- 32 bytes of data RAM

3. Block Diagram



4. Pin Descriptions

Pad No	Pad Name	I/O	Description
1	REF2	I	For reference voltage input
2	CC	O	2nd stage of OPA output end
3	RC	I	2nd stage of OPA negative input end
4	RR	I	2nd stage of internal amplifier
5	AR3	I	Internal amplifier output
6	AR2	I	Internal amplifier negative input
7	AR1	I/O	Internal amplifier voltage follow end
8	SIN	I	Sensor input " — " end
9	SIP	I	Sensor input " + " end
10	PDET	I	Low battery detect input
11	SPWR	O	Sensor power supply
12	VSS	—	Negative power supply
13	REF1	I	For reference voltage input
14, 15	PB0, PB1	I/O	PB0, PB1 pins or for RS, RF control pins
16 ~ 21	PB2 ~ PB7	I/O	I/O pins.
22	OSC	—	Oscillator generator I/O pins
23	AVDD	—	Internal ADC power supply
24	VDD	—	Positive power supply
25	VSS	—	Negative power supply or GND
26	SC	I/O	R/F control pin, connect to CPU TMR pin
27	VLCD	I	LCD panel bias voltage
28 ~ 31	COM3 ~ COM0	O	LCD panel of COMMON driver
32 ~ 51	SEG19 ~ SEG0	O	LCD panel of SEGMENT driver
	CAP1, CAP2	O	CAP1 replace SEG19, CAP2 replace SEG18 in C bias mode
	V30	O	The 3.0V generation pad, replace SEG17 in C bias mode
	V15	O	The 1.5V generation pad, replace SEG16 in C bias mode

5. Electrical Characteristics

Symbol	Parameter	Test Condition		Min..	Typ.	Max.	Unit
		VDD	Condition				
VDD	Operating Voltage	—	—	2.4	3.0	5.2	V
IDD	Operating Current	3V	No Load, Fsys=2MHz	—	2	3	mA
ISTB1	Standby Current	3V	Fsys OFF, 32K ON	—	3	5	μA
ISTB2	Standby Current	3V	Fsys OFF, 32K OFF	—	1	3	μA
RPH	Pull high resistor	3V	PB0 – PB7 & PA4 – PA7	—	100	—	kΩ
IOH1	PB0, PB1 Source Current	3V	VOH1=2.7V	–20	–30	—	mA
IOL1	PB0, PB1 Sink Current	3V	VOL1=0.3V	20	30	—	mA
IOH2	PBZ, BZB Source Current	3V	VOH1=2.7V	–1	–3	—	mA
IOL2	PB2 – PB7 Sink current	3V	VOL2=0.3V	1	3	—	mA
IOL3	SC sink current	3V	VOL3=0.3V	20	30	—	mA
IOL4	LCD COM, SEG Sink Current	3V	VOL4=0.3V	80	150	—	μA
IOH3	LCD COM, SEG Source Current	3V	VOH2=2.7V	50	80	—	μA

6. MCU Function Description

JA32010 contains a 6502 based 8-bit Micro-Controller Unit (MCU) with Program ROM, Special register, user data RAM and 16-bit , 8-bit Timers inside. This chip also provides multi external interrupt pins (I/O Port B), Low Voltage Detector (LVD) function.

6.1 Memory

- Memory Mapping

Address	Definition
00h	POWERC (R/W)
01h	INTC (R/W)
02h	INTF (R/W)
03h	WDTCLR (W)
04h	WDTC (R/W)
05h	TMR0H (R/W)
06h	TMR0L (R/W)
07h	TMR0C (R/W)
08h	Reserved
09h	TMR1L (R/W)
0Ah	TMR1C (R/W)
0Bh	PA (R/W)
0Ch	PAC (R/W)
0Dh	PAR (R/W)
0Eh	PB (R/W)
0Fh	PBC (R/W)
10h	PBR (R/W)
11h-1Fh	Reserved
21h	CON0
22h	Reserved
23h	LCD0
24h	LCD1
E0h ~ FFh	General purpose Data Memory & Stack
200h ~ 213h	LCD data RAM
E000h ~ FFFFh	User Program

- Data RAM

Total of 32 bytes of Data RAM (including the stack) is available from $E0h to $FFh. The stack begins at address $FFh.

- Program ROM

Total of 7K bytes of user ROM located from $E400h to $FFFFh is available.

- Reset & Interrupt Vector

The address of Reset and Interrupt are located from $FFFCh. The vectors should be specified in the program as follows:

```
ORG  $FFFC
JMP  RESET_VECTOR
JMP  INT_VECTOR
```

- Stack Pointer

The stack pointer is set from $FFh after power on.

6.2 Power Configuration

The system provides two modes for power saving; the HALT mode and the STOP mode.

- HALT mode

Writing "1" to the HALT bit cause system enter HALT mode. In HALT mode, the system clock stop running but the internal RC clock (32K) continuously keeps free running. The timer overflow, WDT overflow, external interrupt (INTB) or PA,PB change state can wakeup the system to leave the HALT mode. The HALT bit will be cleared to "0" automatically when system being awakened (STOP bit unchanged).

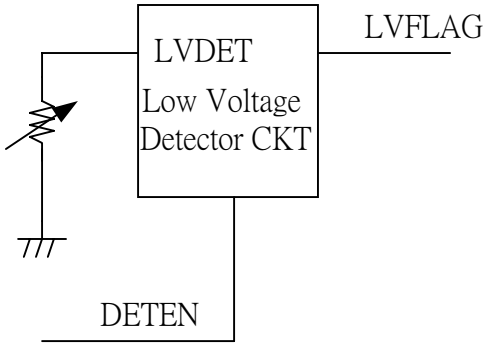
- STOP mode

Writing " 1" to the STOP bit causes system enter STOP mode. In STOP mode, both the system clock and internal RC clock stop running. External interrupt (INTB) or PA,PB change state can wakeup the system. The HALT bit and the STOP bit will be cleared to "0" automatically when system being awakened.

- Low voltage

Writing " 1" to DETEN bit enable the low battery detector circuit of the system. If the low battery situation is detected, the LVFLAG bit will be set to "1" by detector circuit. After writing the DETEN bit, the user must insert 2 NOP instructions in the program before program reading the LVFLAG data.

External resistor shown below adjusts the low voltage level:



POWERC

Register	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
POWERC	00h	LVFLAG	DETEN	—	STOP	—	—	—	HALT

6.3 Reset and Wakeup

The system will be reset by the following conditions:

- Power on
- Reset pin activated (Low)
- Illegal address generation
- WDT overflow
- VDD voltage lower than 1.8V

The system will be awakened from STOP mode or HALT mode by the following conditions:

- Timer overflow
- Level changes on PB input pins
- Active signal on external interrupt input pin

These three cases will make system start running. The starting address depends on the INTF register setting. If the global interrupt bit (INTE) is cleared and the corresponding interrupt bit is set, no wakeup interrupt will be generated and program start running from next instruction in STOP mode or HALT mode. If the global interrupt bit (INTE) is set, the system will execute the corresponding interrupt service routine first then back to execute the next instruction in STOP mode or HALT mode.

6.4 Interrupt

The system will be interrupted by the following conditions:

- Timer overflow
- Level changes on PB input pins
- Active signal on external interrupt input pin

Interrupt control register (INTC) definition is shown below:

INTC (R/W)

Register	Bit No.	Label	Function
INTC	0	INTE	Global interrupt enable bit (1= Enabled; 0 = Disabled)
	1	INT	External INT pin interrupt Enable bit (1= Enabled; 0 = Disabled)
	2	TMR0	TMR0 interrupt Enable bit (1= Enabled; 0 = Disabled)
	3	TMR1	TMR1 interrupt Enable bit (1= Enabled; 0 = Disabled)
	4	PAI	Port A change state interrupt Enable bit (1= Enabled; 0 = Disabled)
	5	PBI	Port B change state interrupt Enable bit (1= Enabled; 0 = Disabled)
	6		Reserved
	7		Reserved

Interrupt Flag (INTF) definition is shown below:

INTF (R/W)

Register	Bit No.	Label	Function
	0	INTF	External INT interrupt flag bit (1= Active; 0 = Inactive)

INTF	1	TMR0F	TMR0 timer interrupt flag bit (1= Active; 0 = Inactive)
	2	TMR1F	TMR1 timer interrupt flag bit (1= Active; 0 = Inactive)
	3		Reserved
	4	PAF	Port A change state interrupt flag bit (1= Active; 0 = Inactive)
	5	PBF	Port B change state interrupt flag bit (1= Active; 0 = Inactive)
	6		Reserved
	7		Reserved

6.5 Timer

The JA3202 contains one16-bit timer (TMR0), one 8-bit timer (TMR1) and one watchdog timer (WDT) inside.

- TMR0 (05h,06h) & TMR0C (07h)

The TMR0 is a 16-bit count-up counter. The clock source may come from system clock, internal RC clock, external pulse input or external 32k crystal. The default value of the control register TMR0C is 00. The definition of TMR0C is listed as following:

Labels	Bits	Function
TON0 (TMR0)	0	Timer0 enable/disable definition bit 0 = Disable; 1 = Enable
TS0, TS1, TS2	1 - 3	Timer clock rate selection bits (prescale)
	4	Reserved
TMR/WDT	5	To assign pre-scale counter to Timer0 or WDT 0: Timer 1: WDT
TM0 TM1	6, 7	To define the operation mode 00= Timer mode (system clock/4) 01= Timer mode (internal RC clock) 10 = Not used 11= Timer mode (32k Hz crystal)

Both TMR0 and WDT share with an 8-bit prescaler. If the prescaler is assigned to TMR0, the WDT clock will be 1:1 to the clock source (no prescale function), vice versa. The ratio table is shown below:

TS2	TS1	TS0	TMR Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

- TMR1 (09h) & TMR1C (0Ah)

The TMR01is an 8-bit count-up counter. The clock source may come from system clock, internal RC

clock, external pulse input or external 32k crystal. The default value of the control register TMR1C is 00. The definition of TMR0C is listed as following:

Labels	Bits	Function
TON1	0	Timer1 enable/disable definition bit 0 = Disable; 1 = Enable
TS0, TS1, TS2	1 - 3	Timer clock source selection bits
—	4	Reserved
TMROUT	5	The set the TMR as input or output pin. 0=input 1=output, it will generate a clock output from TMR pin.
TM0 TM1	6, 7	To define the operation mode 00= Timer mode (system clock/4) 01= Timer mode (internal RC clock) 10= Event count mode from TMR (External SC pin) 11= Timer mode (32k crystal)

There is an 8-bit prescaler dedicated to TMR1. The ratio table is shown below:

TS2	TS1	TS0	TMR1 Clock Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

If TMR was configured as output pin, the output status will be “0” for TON1 = “0”. When TON1=”1”, TMR output status will be as same as MSB bit of TMRL.

- Watchdog Timer

The clock source for watchdog timer (WDT) can be either internal RC (32kHz) or system clock/4; decided by Bit 4 of WDTC register. When WDT is enabled, user shall reset (writing “1”) Bit 0 of WDTCLR register within a specific time to prevent WDT overflow.

WDTCLR (W): 03h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
—	—	—	—	—	—	—	CLRWDT

WDTC (R/W): 04h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
—	—	—	WDTCLK	—	—	—	WDTEN

Bit 4 (WDTCLK): Select the WDT clock source
0=system clock/4 (Default) , 1= Internal RC clock
Bit0 (WDTEN): To enable/disable the WDT, 0= Disable (Default), 1= Enable

6.6 I/O Configuration

The I/O port A (PA) is dedicated to ADC circuit so user can not use PA for other use. Port B (PB) can be used as input and output operations. For input operation, PB is non-latched , for output operation, all the data are latched and remain unchanged till the output latch is re-written.
Each I/O port has its own control register (PAC, PBC) to control the input/output configuration.

- PA Configuration

PA control register specifies the characteristic. Please refer to the table below:

Label	Address	Function	R/W	Default
PA	0Bh	PA data input/output	R/W	FF
PAC	0Ch	PA direction control, 1=input 0=output	R/W	FF
PAR	0Dh	PA pull-high resistor option, 1=With, 0=Without	R/W	FF

In JA32010, PA is dedicated to ADC circuit, PA5 for ON/OFF control, PA6 for COMPO, PA4 for CHAR/DIS (charge/discharge) control, others PA pins can bot be used. Please see the block diagram on first page for reference.

- PB Configuration

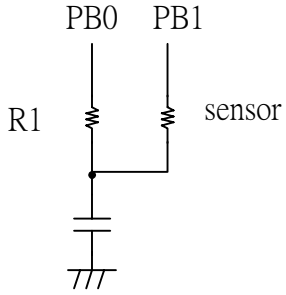
For port B, they can be configured as follows:

Label	Address	Function	R/W	Default
PB	0Eh	PB data input/output	R/W	FF
PBC	0Fh	PB direction control, 1=input 0=output	R/W	FF
PBR	10h	PB pull-high resistor option, 1=With, 0=Without	R/W	FF

7. R/F Function Descriptions

JA32010 PB0, PB1 can be configured (mask option) to perform either R/F function or normal I/O function.

In R/F application, user put reference resistor (R1) to PB0, sensor to PB1. One capacitor also used to from the loop. Please see the following figure for reference:



To active R1, MCU output high signal to PB0, output low signal to PB1. Reference can be generated on the SC pin. Inside the JA32010, the signal on SC pin can be routed to the clock source of timer by programming.

8. LCD Function Descriptions

8.1 LCD Clock

The clock source for LCD can be internal RC (32kHz), external 32k crystal or system clock; decided by Bit 5, Bit 4 of CON0. The Bit 3 of CON0 controls the LCD on/off, "1" for LCD on, "0" for LCD off.

CON0 (R/W): 21h

B7	B6	B5	B4	B3	B2	B1	B0
—	—	OSC1	OSC0	LCD	—	—	—

8.2 LCD Common & Segment

If user chooses R bias for the LCD, the segment will be SEG 0 to SEG 19. If user chooses C bias for the LCD, the segment will be SEG 0 to SEG 15.

The user can configure LCD controller to 2 COM, 3 COM or 4 COM; decided by Bit 6, Bit 5, and Bit 4 of LCD0. The Bit 7 of LCD0 controls frame frequency of LCD, "1" for 170 Hz on, "0" for 85 Hz. Please see the table below:

LCD0 (R/W): 23h

B7	B6	B5	B4	B3	B2	B1	B0
Frame	C2	C1	C0	—	—	—	—

Frame: 0 - 85 Hz
1 – 170 Hz
C2, C1, C0: (1, 0, 1): 2 COM, (1, 0, 0): 3 COM, (0, 1, 1): 4 COM

8.3 LCD Bias

The user can configure LCD controller to 1/2 bias or 1/3 bias; decided by Bit 2, Bit 1, and Bit 0 of LCD1.

LCD1 (R/W): 24h

B7	B6	B5	B4	B3	B2	B1	B0
—	—	—	—	—	B2	B1	B0

B2, B1, B0: (1, 0, 0): 1/2 bias, (0, 1, 1): 1/3 COM.

8.4 LCD Data RAM

The RAM is located from 200h to 213h. Please refer to the table below, "*" means "don't care".

RAM Address	Segment number	Content
200h	Seg0	*,*,*,*,COM3,COM2,COM1,COM0
201h	Seg1	*,*,*,*,COM3,COM2,COM1,COM0
202h	Seg2	*,*,*,*,COM3,COM2,COM1,COM0
203h	Seg3	*,*,*,*,COM3,COM2,COM1,COM0
204h	Seg4	*,*,*,*,COM3,COM2,COM1,COM0

205h	Seg5	*,*,*,*,COM3,COM2,COM1,COM0
206h	Seg6	*,*,*,*,COM3,COM2,COM1,COM0
207h	Seg7	*,*,*,*,COM3,COM2,COM1,COM0
208h	Seg8	*,*,*,*,COM3,COM2,COM1,COM0
209h	Seg9	*,*,*,*,COM3,COM2,COM1,COM0
20Ah	Seg10	*,*,*,*,COM3,COM2,COM1,COM0
20Bh	Seg11	*,*,*,*,COM3,COM2,COM1,COM0
20Ch	Seg12	*,*,*,*,COM3,COM2,COM1,COM0
20Dh	Seg13	*,*,*,*,COM3,COM2,COM1,COM0
20Eh	Seg14	*,*,*,*,COM3,COM2,COM1,COM0
20Fh	Seg15	*,*,*,*,COM3,COM2,COM1,COM0
210h	Seg16	*,*,*,*,COM3,COM2,COM1,COM0
211h	Seg17	*,*,*,*,COM3,COM2,COM1,COM0
212h	Seg18	*,*,*,*,COM3,COM2,COM1,COM0
213h	Seg19	*,*,*,*,COM3,COM2,COM1,COM0

9. ADC Function Description

9.1 ADC General

The JA32010 offers very high accuracy A/D conversion by using Dual Slope integration. It incorporates operational amplifiers, comparators, power on/off control circuit and charge/discharge control circuit inside to achieve high performance for application. A voltage follower was used as buffer for sensor signal input. Because of the buffer's great isolating characteristic, the signal from sensor will be precisely duplicated and sent out at output pin without any distortion.

An operational amplifier was designed for user to properly amplify the sensor signal from buffer. Inside the chip, a current accurately proportional to the amplified signal level will be generated to charge an external RC network for a fixed time interval. After being charged for this interval, the capacitor is discharged by a constant current until the voltage reaches 1/6 VDD. This discharging time is proportional to the input signal level and is used by external controller to enable a counter; the final count is proportional to the input level and can be converted to digital output. Because the charge cycle and discharge cycle go through the same RC network, using a high quality capacitor is recommended.

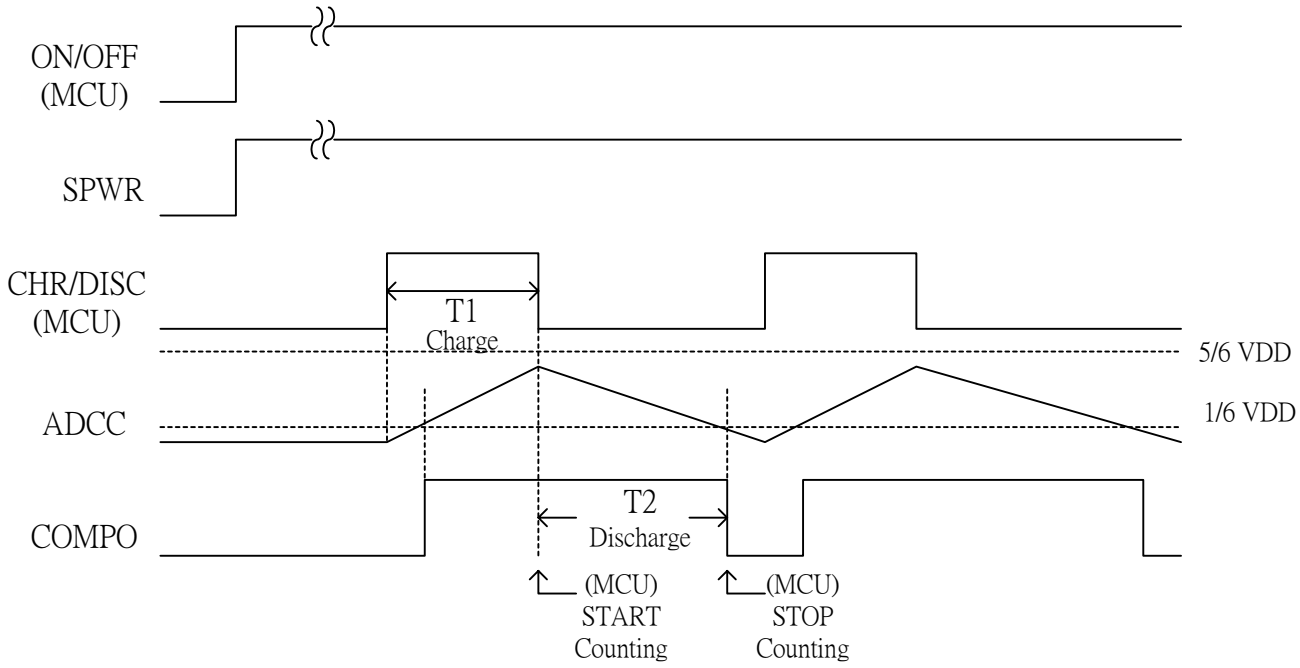
Basic introductions are listed as follows:

a. OP1: OP1 was a voltage follower. It receives sensor signal and amplify the signal with unit gain. The output was sent to pin 2 for OP2 further use.
b. OP2: OP2 was designed for signal amplification. By adjusting the external resistors, user can properly decide the gain of the amplifier.
c. Transmission gates & Integrator: Transmission gate provides a signal accurately proportional to the OP2 amplified signal level. This signal will be used to charge an external RC network at a fixed time interval (See the Timing Diagram T1). Another transmission gate can generate a constant signal to discharge the capacitor. This discharging time is proportional to the input signal level.
d. Comparators: The comparators were used to generate a data (T2) for controller. When the input

signal is charged on integrator after a time interval T1, the controller shall control the CHR/DISC pin to discharge (See the Timing Diagram), and then controller shall enable the internal counter to start counting. When the voltage on ADCC is lower than 1/6 VDD (after discharge a time interval T2), the COMPO pin will transfer from High to Low. At this time the controller shall stop the internal counter. The discharge time T2 is proportional to the input level, the final count of counter can be converted to digital data by controller.

e. Power on/off control: The power on/off control circuit was designed for power saving. The SPWR (Sensor Power Supply) won't be available unless the On/Off actives (High).

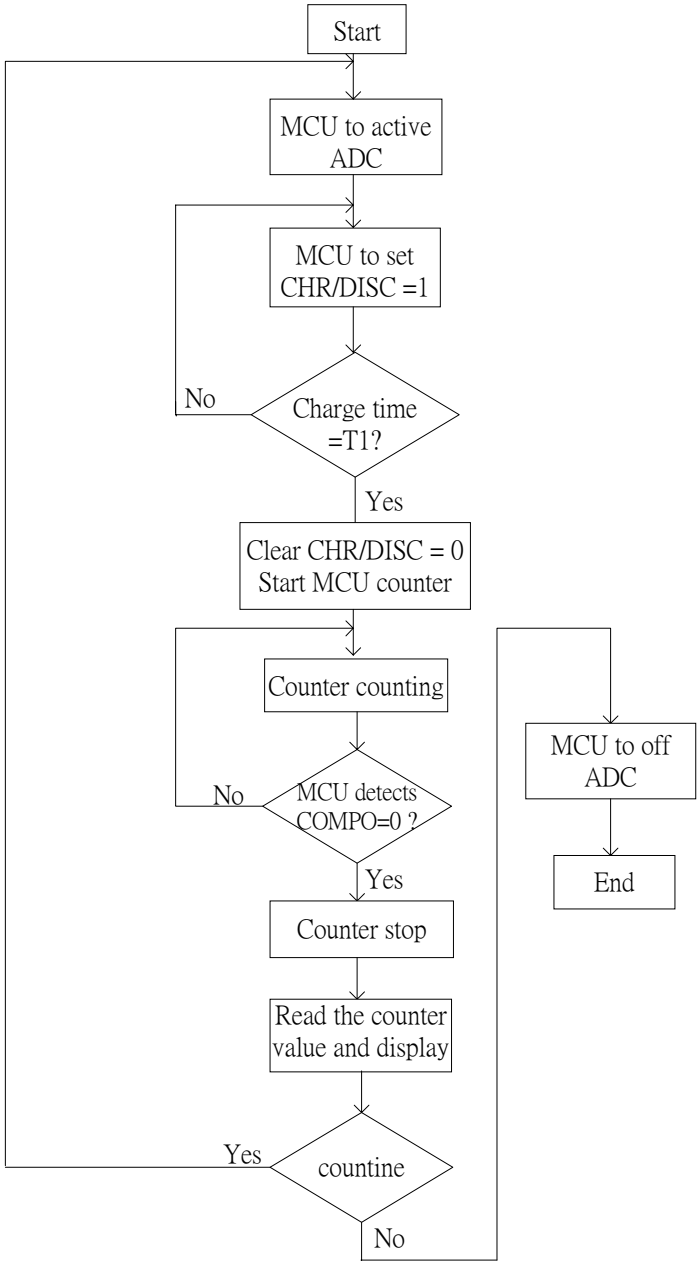
9.2 ADC Timing Diagram



T1(Charge): The fixed charge time control by controller(MCU).
T2 (Discharge): The discharge time provide to controller(MCU).

9.3 ADC Program Flow Chart

The following flow chart is the illustration for JA32020 programming.



a. MCU asserts high signal to activate ADC circuit.
b. ADC provides power to sensor from SPWR pin.
c. MCU asserts high signal on CHR/DISC pin to start charging.
d. After a fixed time interval (decided by MCU program), MCU asserts low signal on CHR/DISC pin to start discharging.
e. MCU enables internal counter start counting.
f. When ADCC of JA32020 below 1/6 VDD (The COMPO pin transfer from High to Low), MCU disables counter. The count value is proportional to the input signal.

9.4 ADC Design Suggestions

The following information is provided for using the dual slope ADC chip Y32210 in measuring application.

a. OP Gain:
The OP gain was suggested not to exceed 20. This is not because the OP characteristic but noise concern. The Y32210 OP was a two stages structure that can handle 100 dB gain with good linearity but when use high gain, the OP feedback resistor value will be large, then any small noise induced at OP input pin will cause large output at OP output.

b: Charge Time:
100 ms charging time is common in measuring application. If the charging time is long, the noise effect may be large.

c. Charge capacitor:
The capacitor quality is importance in dual slope application. The ceramic type (X7R) is suitable. The capacitor should be no more than 104P.

d. Charge/Discharge resistor:
The resistor is better not greater than 560k. Although large resistor can increase charge/discharge time, any noise induced during this time period will affect the result.

e. CAP for REF1, REF2:
The capacitors are needed for REF1 and REF2 pins. They are used to reduce the noise on reference voltage inside the ADC circuit.

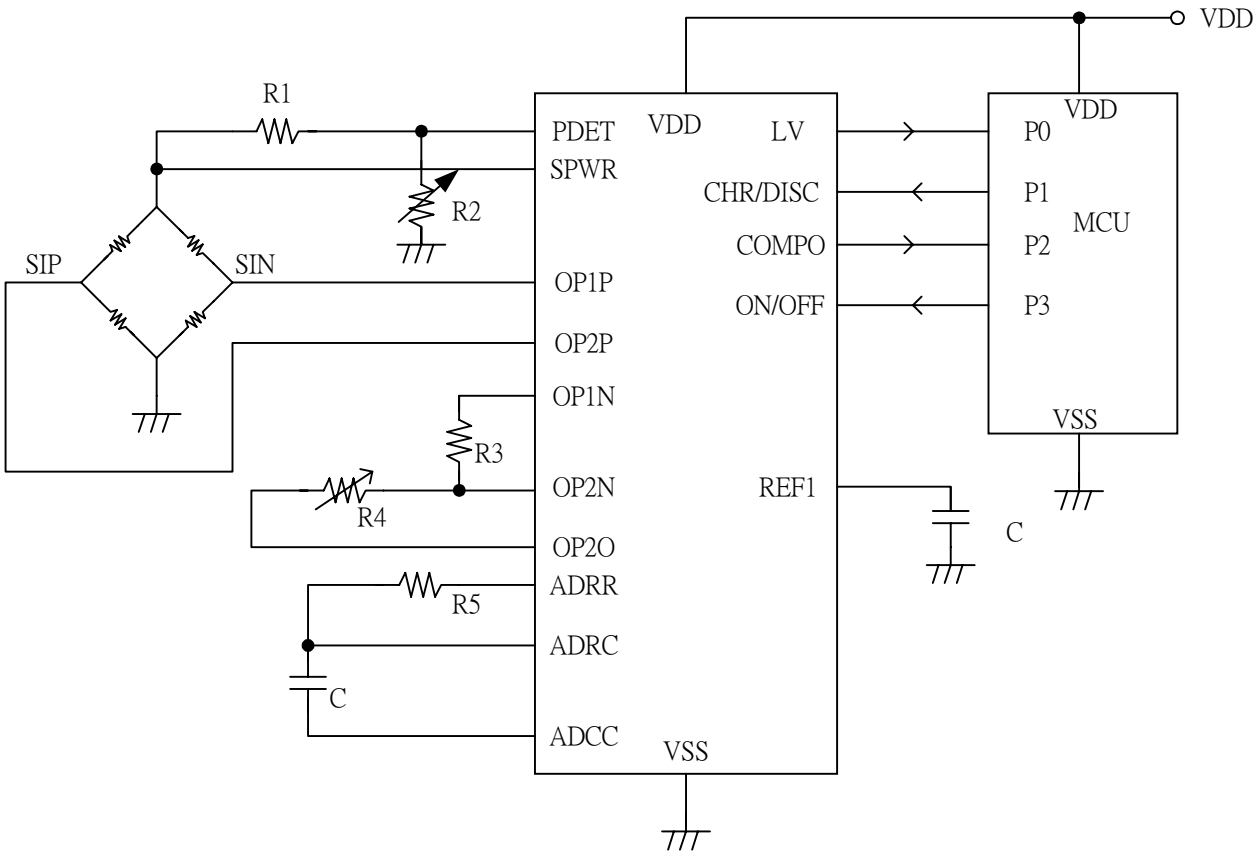
f. Max charging voltage not to exceed 5/6 Vdd:
The Max charging voltage should be lower than 5/6 Vdd. When charging voltage exceeds 6/5 Vdd, the OP linearity may decay and result in distortion. Keep off charging voltage saturation.

g. Min charging voltage not to near 1/6 Vdd:
If the voltage were too close 1/6 Vdd, the counting time will be short for MCU. The counting result may be unstable.

h. Choose proper clock to timer:
Under stable counting condition, choose faster clock for timer. Fast clock can help increase resolution.

10. ADC Application Diagram

The application diagram is a simple illustration for using the JA32101 chip. It shall be noted that inside the JA32010, PA is dedicated to ADC circuit (PA5 for ON/OFF control(PA6 for COMPO, PA4 for CHAR/DIS control), user doesn't need to make wire for them.



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