MITSUBISHI SOUND PROCESSOR ICs

M65831AP/FP

DIGITAL ECHO (DIGITAL DELAY)

DESCRIPTION

The M65831A is an IC developed for producing echo effects added to voice signals
picked up by microphone for karaoke applications.
The IC has the largest memory among the digital delay series. As it's design is aimed
at high performance, it is best suited to provide radio cassette tape recorders and
miniature unit audio system with quality echo function.
Being pin compatible with the M65830CP / FP and M65843AP / FP, the M65831AP / FP is
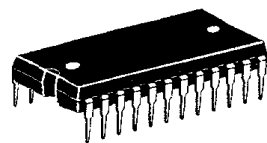suitable for upgrading the series.

FEATURES

•Built-in input / output filters, A-D and D-A conver ters, and
 memory realize a delay system with only a single chip
•Capable of composing low-noise and low-distortion delay
 system at low cost by ADM system
          (No=-92dB typ, THD=0.5% typ)
•Control mode selections available from 2 kinds : easy mode
 using parallel data and microcomputer mode using serial
 data
•Sleep mode can be selected to stop IC functions
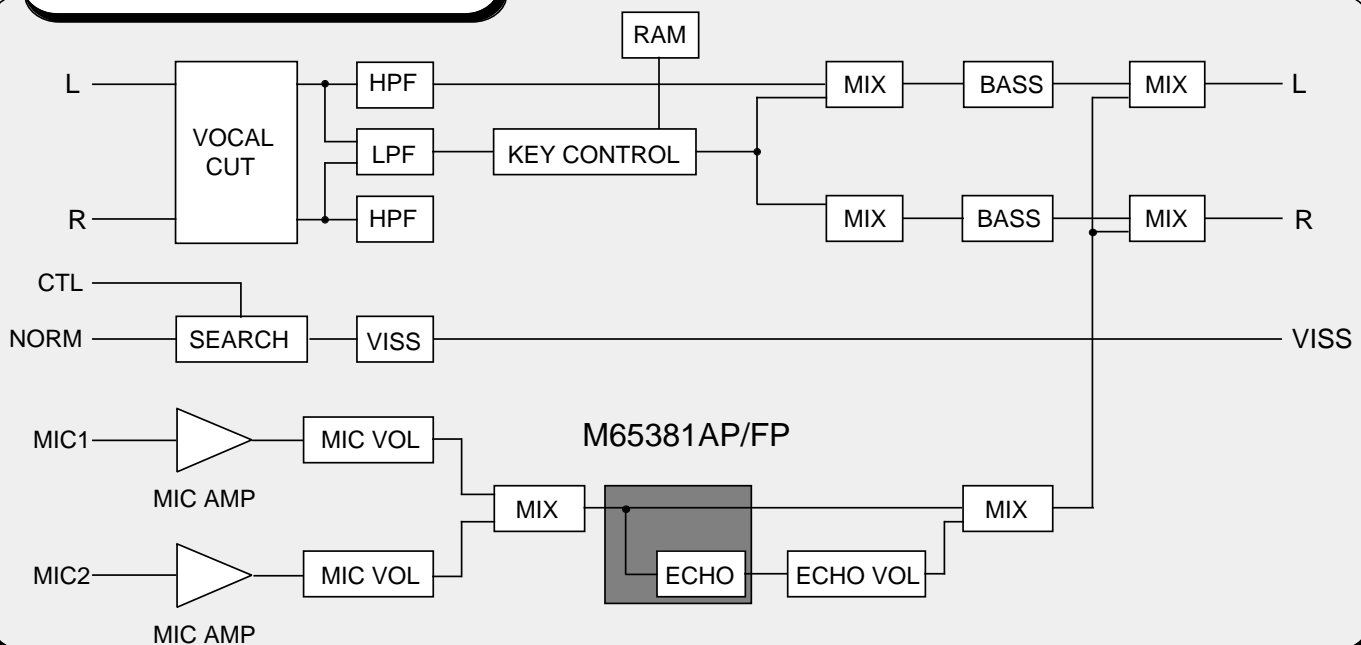•Built-in automatic reset circuit

Outline

Outline   24P4 (AP)
 2.54mm pitch 600mil DIP
 (13.0mm X 31.1mm X 3.8mm)

Outline   24P2W-A(AFP)
 1.27mm pitch 450mil SOP
 (8.4mm X15.0mm X2.0mm)

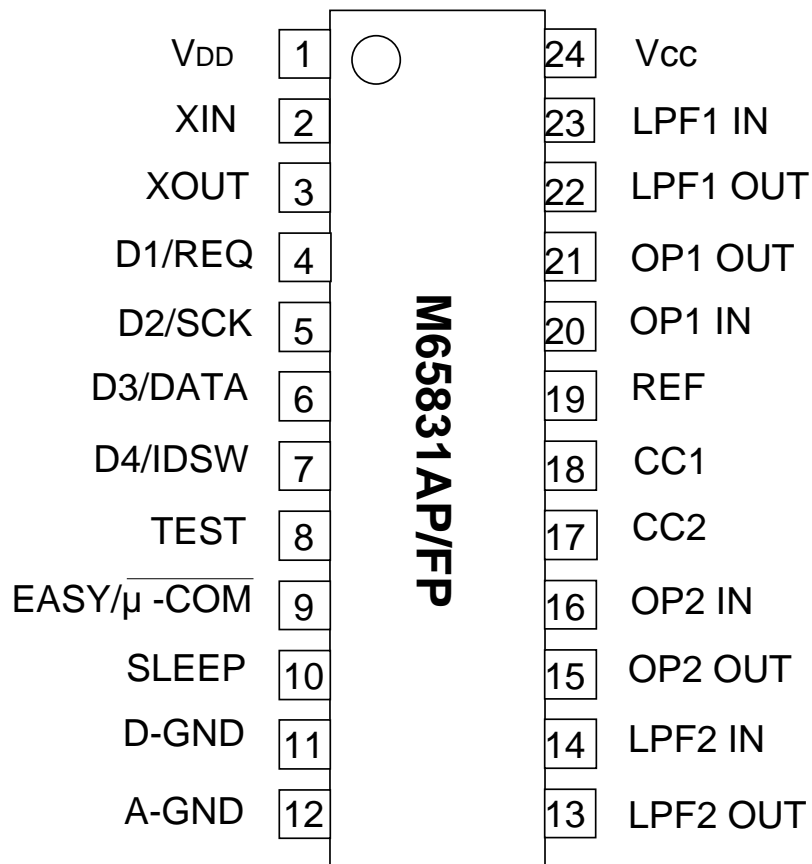## RECOMMENDED OPERATING CONDITIONS

Supply voltage range ----------- VCC,VDD=4.5 to 5.5V
Rated supply voltage ------------------ VCC,VDD=5.0V

SYSTEM CONFIGURATION

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Pin Configuration

Pin	Name		Pin	Name
1	V_{DD}		24	Vcc
2	XIN		23	LPF1 IN
3	XOUT		22	LPF1 OUT
4	D1/REQ		21	OP1 OUT
5	D2/SCK		20	OP1 IN
6	D3/DATA		19	REF
7	D4/IDSW		18	CC1
8	TEST		17	CC2
9	EASY/$\overline{\mu \text{-COM}}$		16	OP2 IN
10	SLEEP		15	OP2 OUT
11	D-GND		14	LPF2 IN
12	A-GND		13	LPF2 OUT

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PRELIMINARY
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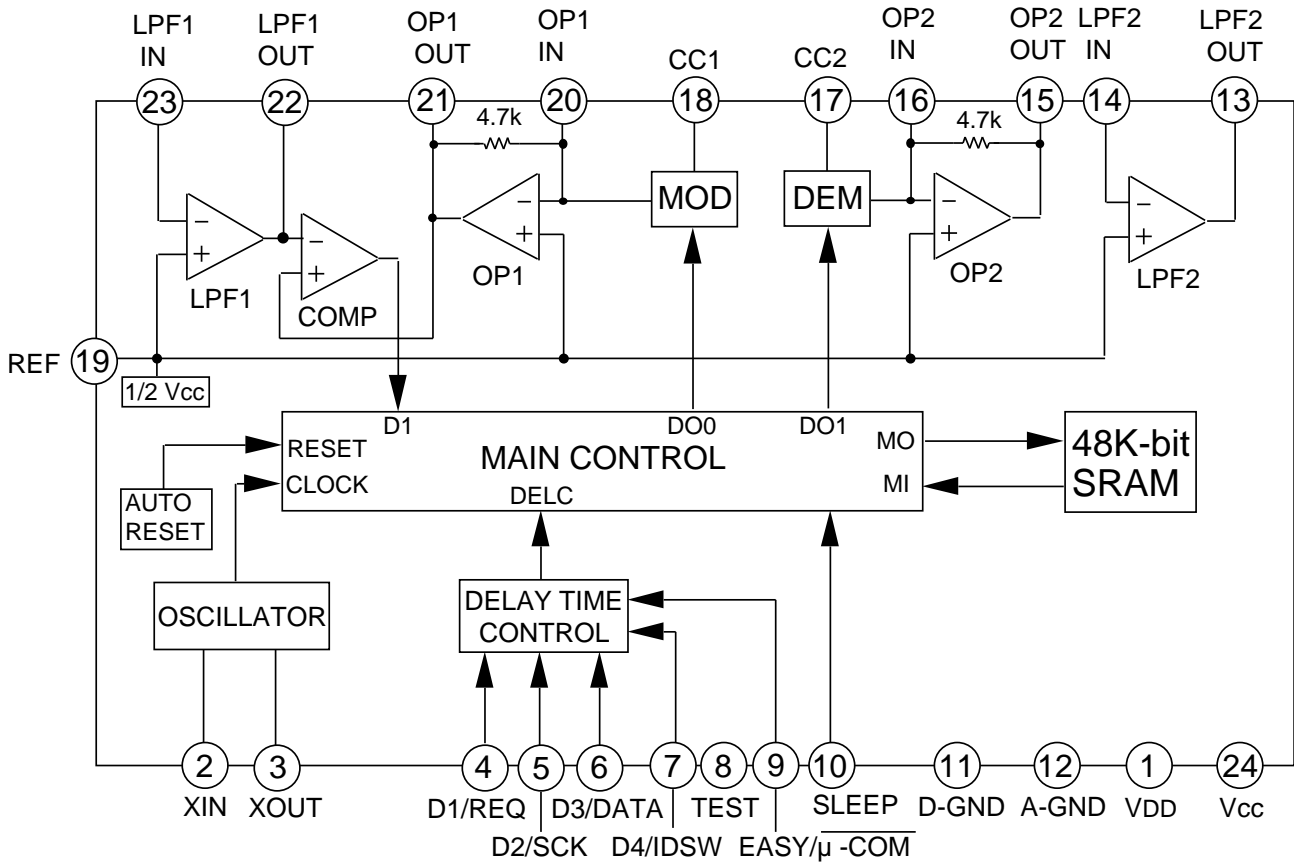
BLOCK DIAGRAM

Unit Resistance:

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PIN DESCRIPTION

No.	Symbol	Name	I/O	Function
①	V_{DD}	Digital V_{DD}	—	Supply voltage
②	X_{IN}	Oscillator input	I	
③	X_{OUT}	Oscillator output	O	Connects to 2MHz ceramic filter
④	D1/REQ	Delay1/Request	I	Easy mode:inputs D1 data μ-COM mode:inputs request data
⑤	D2/SCK	Delay2/Shift clock	I	Easy mode:inputs D2 data μ-COM mode:inputs shift clock
⑥	D3/DATA	Delay3/Serial data	I	Easy mode:inputs D3 data μ-COM mode:inputs serial data
⑦	D4/IDSW	Delay4/ID switch	I	Easy mode:inputs D4 data μ-COM mode:controls ID code
⑧	TEST	Test	I	L=normal mode
⑨	EASY/$\overline{\mu\text{-COM}}$	Easy/$\overline{\mu\text{-COM}}$	I	H=easy mode L=μ-COM mode
⑩	SLEEP	Sleep	I	H=sleep mode L=normal mode
⑪	D GND	Digital GND	—	Connects to analog GND at one point
⑫	A GND	Analog GND	—	Connects to analog GND
⑬	LPF2 OUT	Low pass filter2 output	O	Forms low pass filter with external C.R
⑭	LPF2 IN	Low pass filter2 input	I	
⑮	OP2 OUT	OP-AMP2 output	O	Forms integrator with external C.R
⑯	OP2 IN	OP-AMP2 input	I	
⑰	CC2	Current control 2	—	
⑱	CC1	Current control 1	—	
⑲	REF	Reference	—	=1/2VCC
⑳	OP1 IN	OP-AMP1 input	I	Forms integrator with external C.R
㉑	OP1 OUT	OP-AMP1 output	O	
㉒	LPF1 OUT	Low pass filter1 output	O	Forms low pass filter with external C.R
㉓	LPF1 IN	Low pass filter1 input	I	
㉔	V_{CC}	Analog V_{CC}	—	Supply voltage

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ABSOLUTE MAXIMUM RATINGS

(Vcc=5V,f=1kHz,Vi=100mVrms,Ta=25°C,unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Units
Vcc	Supply voltage			6.5	V
Icc	Circuit cuurent			100	mA
Pd	Power dissipation	M65831AP		1	W
		M65831AFP		650	mW
Topr	Operating temperature			-20~+75	°C
Tstg	Storage temperature			-40~+125	°C

THERMAL DERATING (MAXIMUM RATING)

POWER DISSIPATION   Pd (mW) vs AMBIENT TEMPERATURE   Ta (°C)
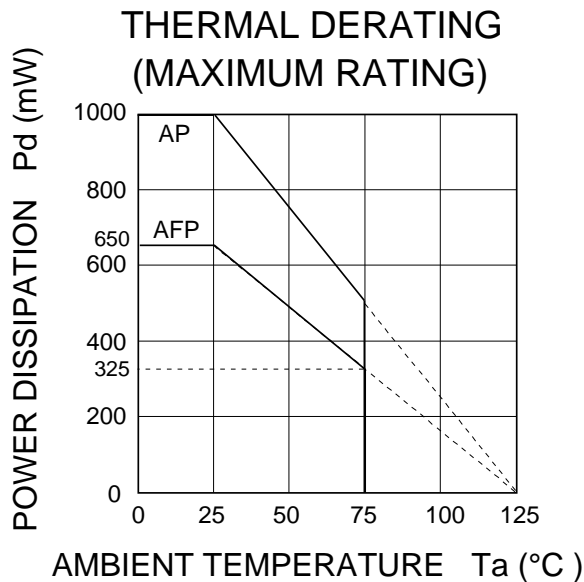
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
Vcc	Supply voltage		4.5	5	5.5	V
VDD	Supply voltage		4.5	5	5.5	V
Vcc-VDD	Difference voltage		-0.3	0	0.3	V
fck	Clock frequency		1	2	3	MHz
VIH	High input voltage		0.7VDD		VDD	V
VIL	Low input voltage		0		0.3VDD	V

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ELECTRICAL CHARACTERISTICS

(Vcc=5V,f=1kHz,Vi=100mVrms,Ta=25°C,unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Units
				Min	Typ	Max	
Icc	Circuit current	No signal		——	18.0	40.0	mA
Gv	Voltage gain	RL=47k		-3.5	-0.5	2.5	dB
Vomax	Maximum output voltage	THD=10%		0.7	1	——	Vrms
THD	Output distortion	30kHz LPF	fs=500kHz	——	0.3	1.0	%
			fs=250kHz	——	0.5	1.5	
No	Output noise voltage	DIN-AUDIO (fs=250kHz)		——	-92	-75	dBV
SVRR	Supply voltage rejection ratio	Vcc=-20dBV,f=100Hz		——	-40	-25	dB
TMUTE	Mute time	Upon changing Delay Time		508	528	548	ms
		Upon canceling Sleep Mode		508	528	548	
Iccs	Circuit current (Sleep mode)	Sleep Mode		——	14.0	30.0	mA

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OPERATION

1) DELAY TIME

D4	D3	D2	D1	fs	Td
L	L	L	L	500	12.3
			H		24.6
		H	L		36.9
			H		49.2
	H	L	L		61.4
			H		73.7
		H	L		86.0
			H		98.3
H	L	L	L	250	110.6
			H		122.9
		H	L		135.2
			H		147.5
	H	L	L		159.7
			H		172.0
		H	L		184.3
			H		196.6

fs=sampling frequency(kHz)
Td=delay time(msec)

DIGITAL ECHO (DIGITAL DELAY)

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2) EASY MODE(EASY / $\overline{\mu\text{-COM}}$=H)

D1,D2,D3,D4 and sleep are for easy mode

D1
D2
D3   } delay time   cf 11-1)
D4
SLEEP   cf 11-5)

3) μ -COM MODE(EASY / $\overline{\mu\text{-COM}}$=L)

REQ

SCK

DATA   ⟨SLEEP⟩⟨D1⟩⟨D2⟩⟨D3⟩⟨D4⟩⟨MUTE⟩⟨ID1⟩⟨ID2⟩⟨ID3⟩⟨ID4⟩

DELAY TIME cf 11-1)   ID CODES

H=SLEEP MODE cf 11-5)   → H=MUTE cf 11-4)
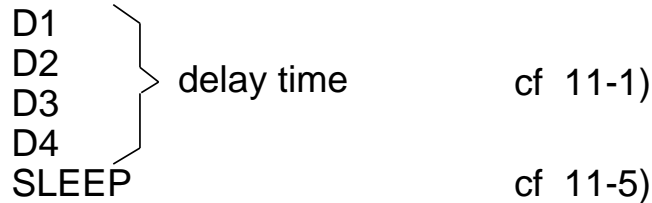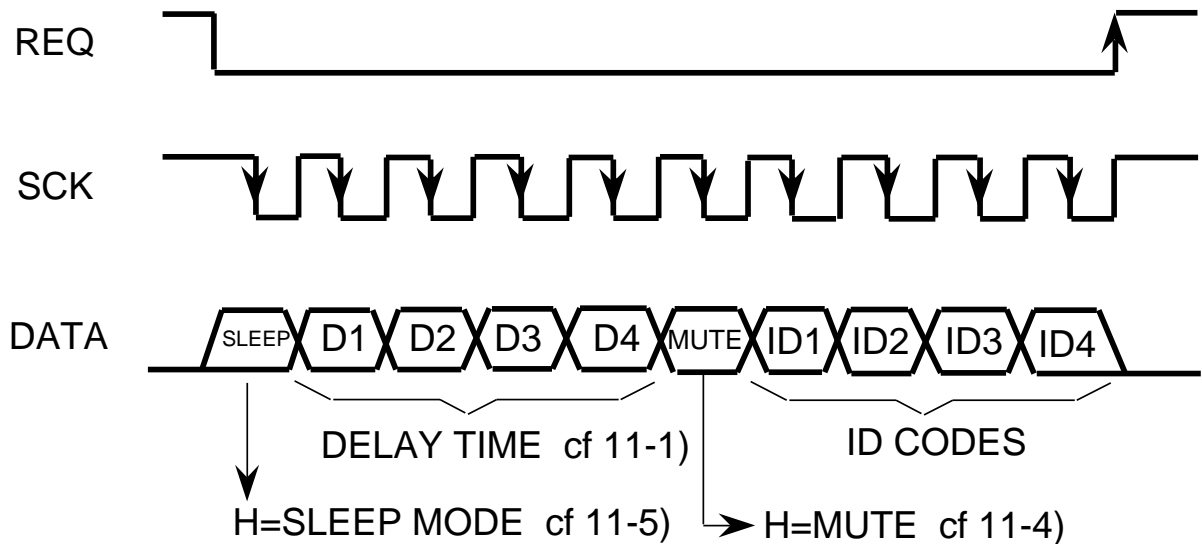
TIMING DIAGRAM

This Timing chart shows that delay time is set by serial data from μ -COM.
DATA signal is latched at the falling edge of SCK signal,the last ten data are set at
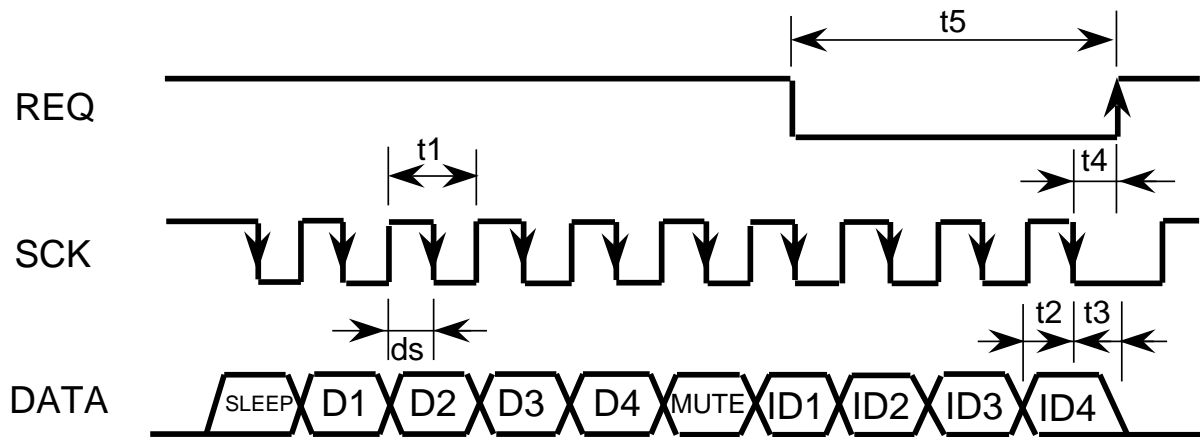the rising edge of REQ signal when ID codes are satisfied. ∗

                    ID1,ID3:L
∗ {   ID2   :H
                    ID4   :equal to IDSW

REQ,SCK,DATA INPUT TIMING

Symbol	Parameter	min	typ	max	Units
t1	SCK pulse width	250	——	——	nsec
ds	SCK pulse duty	——	50	——	%
t2	DATA setup time	100	t1/2	——	nsec
t3	DATA hold time	100	t1/2	——	nsec
t4	REQ hold time	100	——	——	nsec
t5	REQ pulse width	250	——	——	nsec

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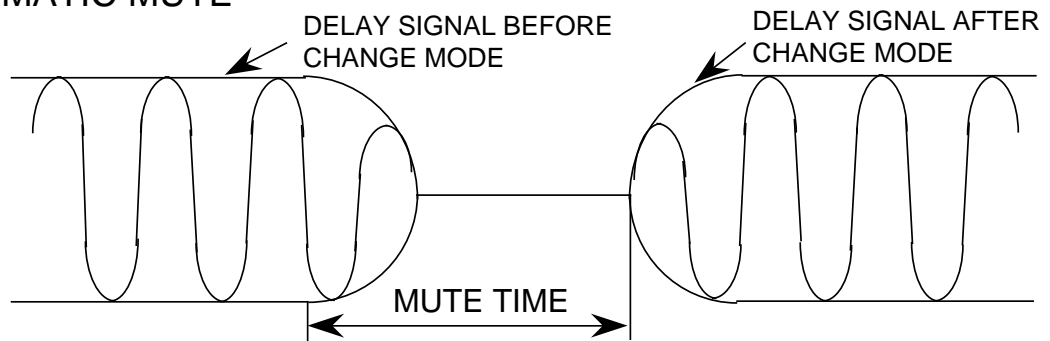## 4) MUTING

(1) Easy mode
Automatic mute upon changing delay time, cancelling SLEEP mode and power-on.

(2) μ -COM mode
MUTE=H:mute
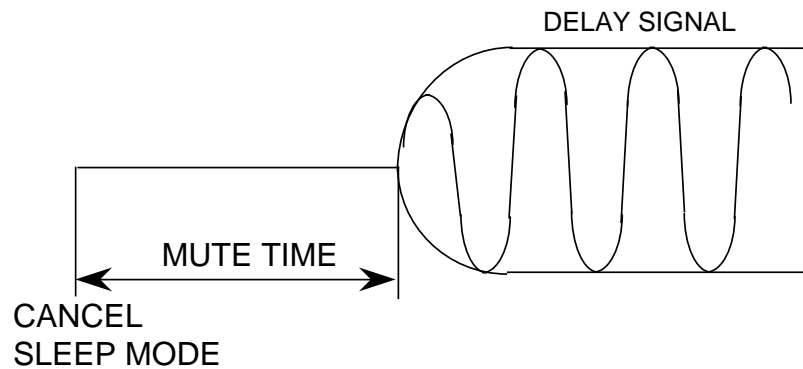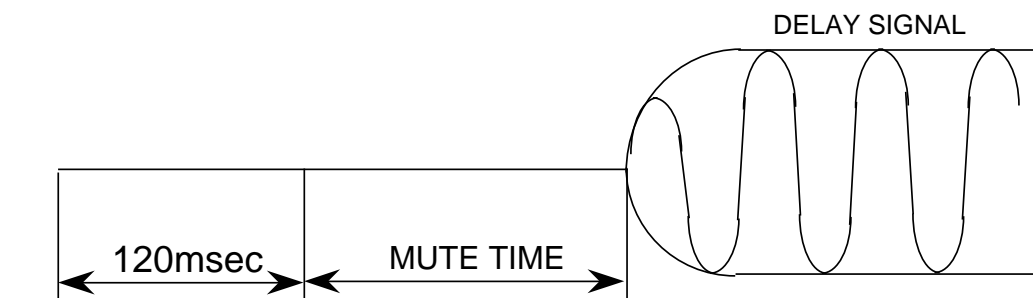MUTE=L:automatic mute

AUTOMATIC MUTE

DELAY SIGNAL BEFORE CHANGE MODE

DELAY SIGNAL AFTER CHANGE MODE

MUTE TIME

(a) UPON CHANGING DELAY TIME

DELAY SIGNAL

MUTE TIME

CANCEL
SLEEP MODE

(b) UPON CANCELLING SLEEP MODE

DELAY SIGNAL

120msec

MUTE TIME

POWER ON

(c) UPON POWER-ON

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5) SLEEP MODE

SLEEP data is

$\Big($ H:clock and RAM stop to reduce circuit current (SLEEP mode)
L:normal operation

6) SYSTEM RESET

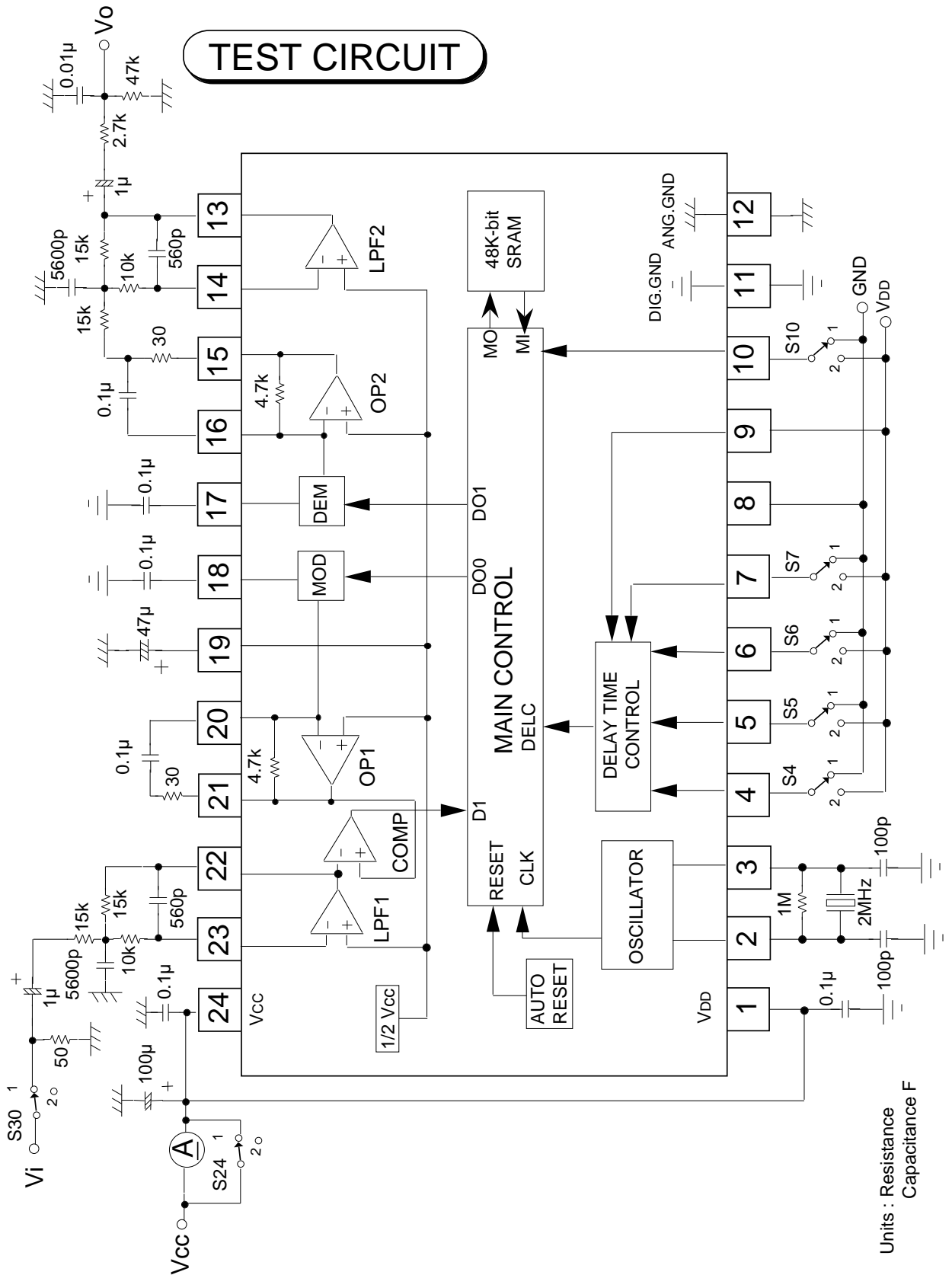Automatically reset power-on. The reset time is about
120msec.
Delay time is set at 147.5msec.

TEST CIRCUIT

Units : Resistance
Capacitance F

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TEST METHODS

Switch condition

* 1 or 2

No	Parameter	Sampling frequency	Symbol	S4	S5	S6	S7	S10	S24	S30	notes
1	Current circuit	—	Icc	1	1	1	1	1	2	2	No signal
2	Voltage gain	500kHz	Gv1	*	*	*	1	1	1	1	
		250kHz	Gv2	*	*	*	2	1	1	1	
3	Delay time	500kHz	Tda	1	1	1	1	1	1	1	cf. 11-1)
			Tdb	2	1	1	1	↓	↓	↓	
			Tdc	1	2	1	1	↓	↓	↓	
			Tdd	2	2	1	1	↓	↓	↓	
			Tde	1	1	2	1	↓	↓	↓	
			Tdf	2	1	2	1	↓	↓	↓	
			Tdg	1	2	2	1	↓	↓	↓	
			Tdh	2	2	2	1	↓	↓	↓	
		250kHz	Tdi	1	1	1	2	↓	↓	↓	
			Tdj	2	1	1	2	↓	↓	↓	
			Tdk	1	2	1	2	↓	↓	↓	
			Tdl	2	2	1	2	↓	↓	↓	
			Tdm	1	1	2	2	↓	↓	↓	
			Tdn	2	1	2	2	↓	↓	↓	
			Tdo	1	2	2	2	↓	↓	↓	
			Tdp	2	2	2	2	1	1	1	
4	Output voltage (max)	500kHz	Vomax 1	*	*	*	1	1	1	1	30kHz L.P.F. THD=10%
		250kHz	Vomax 2	*	*	*	2	1	1	1	
5	Total harmonic distortion	500kHz	THD 1	*	*	*	1	1	1	1	30kHz L.P.F.
		250kHz	THD 2	*	*	*	2	1	1	1	
6	Output noise voltage	250kHz	No	*	*	*	2	1	1	1	DIN AUDIO Vi=0mVrms
7	Supply voltage rejection ratio	—	SVRR	*	*	*	*	1	1	2	Vcc=-20dBv, f=100Hz
8	Mute time	—	MUTE T	$2{\downarrow}1$	*	*	*	1	1	1	Upon changing Delay Time
		—	MUTE S	*	*	*	*	$2{\downarrow}1$	1	1	Upon cancelling Sleep Mode

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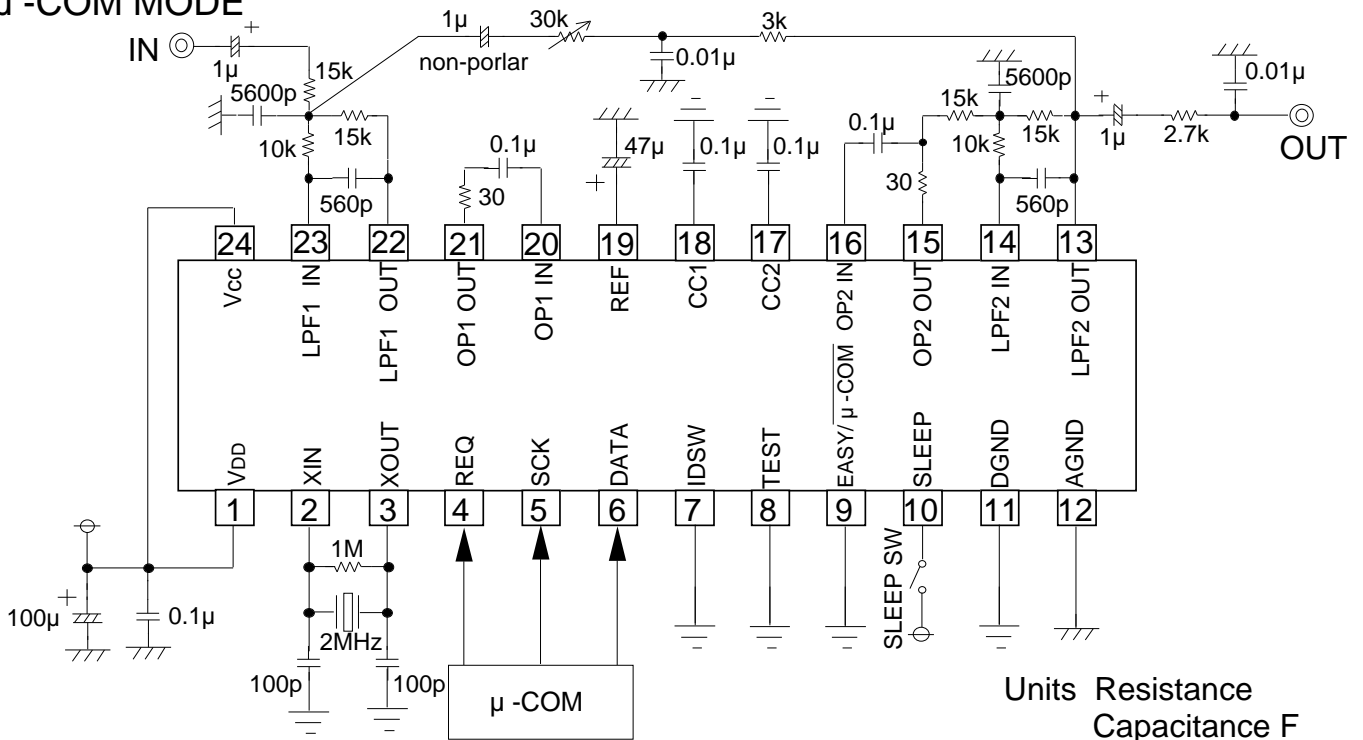**MITSUBISHI SOUND PROCESSOR ICs**

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APPLICATION EXAMPLE

1.EASY MODE
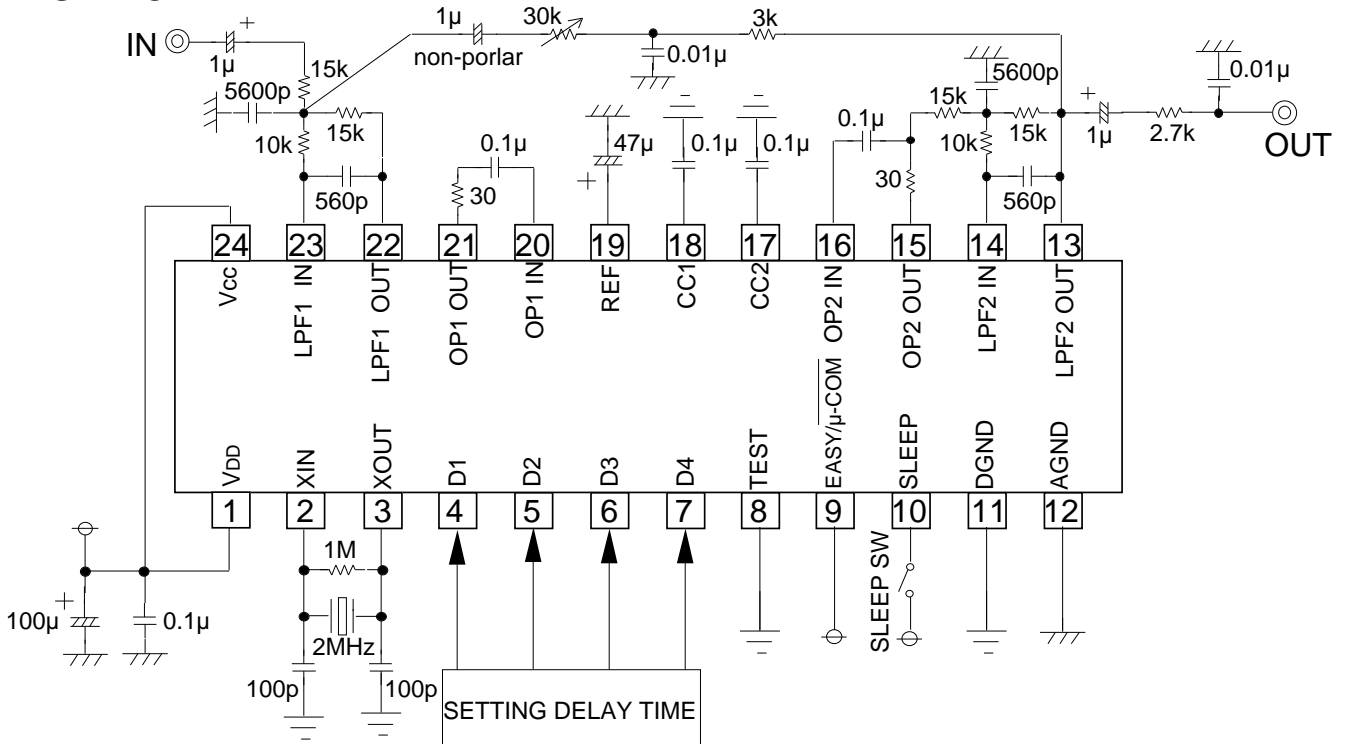
2.µ -COM MODE

Units Resistance
Capacitance F

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