NT6612

2K 4-bit Microcontroller with LCD Driver

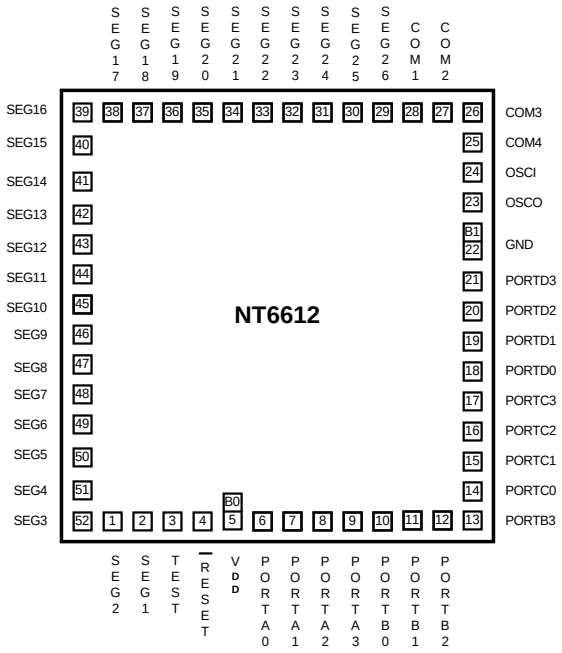
Features

- NT6610C-based single-chip 4-bit microcontroller with LCD driver
- ROM: 2048 × 16 bits
- RAM: 256 × 4 bits (data memory)
- Operation Voltage Range: 2.2V - 5.4V (3V typically)
- 16 CMOS I/O pins (PORTA - D, CMOS or Open Drain by code option)
- 4 level subroutine nesting (including interrupts)
- Two 8-bit timers with pre-divider circuit
- Oscillator warm-up timer
- 4 priority interrupt sources:
  - External interrupt (falling edge)
  - Timer0 interrupt
  - Timer1 interrupt
  - PortB interrupt (falling edge)
- Clock source: 32.768KHz crystal or 262K RC (type is programmable by code option)
- Instruction cycle time:
  4/32.768KHz (≈ 122μs) for 32.768KHz crystal
  4/262KHz (≈ 15μs) for 262KHz RC
- LCD driver
  4 × 26 (1/4 duty , 1/3 bias or 1/3 duty , 1/2 bias)
- Two low power operation modes - HALT or STOP mode
- Built-in alarm generator (carrier frequency: 2KHz or 4KHz code option)
- Low power consumption (Iop < 10μA, 32.768KHz, 3V)
- Bonding option for multi-code software
- Available in CHIP FORM

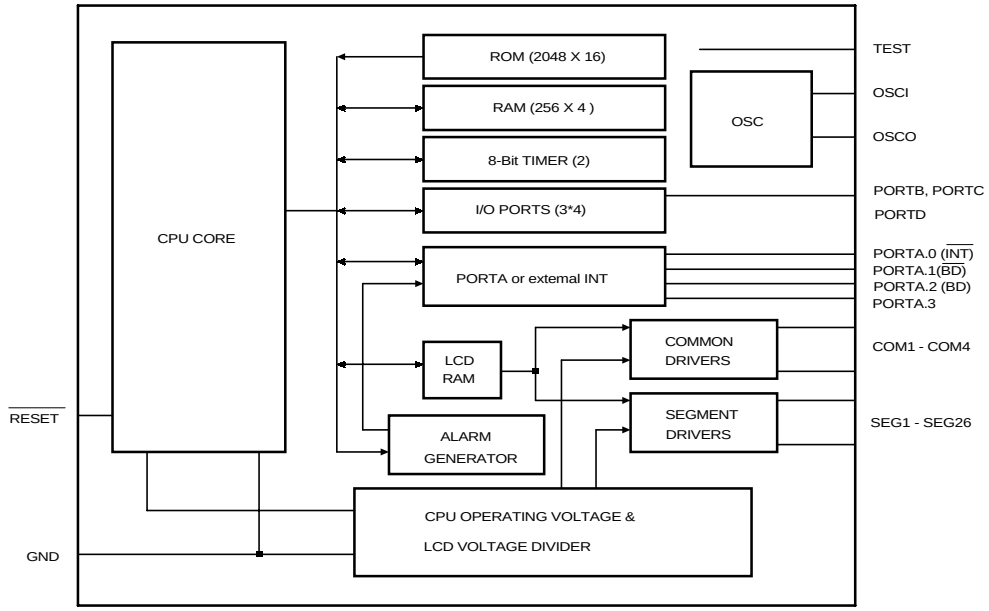
General Description

NT6612 is a single-chip microcontroller integrated with an NT6610C CPU core, SRAM, timer, alarm generator, LCD driver, I/O port, and program ROM.

Pad Configuration



Block Diagram



Pad Description

Pad No.	Designation	I/O	Description
2 - 1, 52 - 29	SEG1 - 26	O	Segment signal output for LCD display. Seg1 - 4 as output
3	TEST	I	Test pin internally pull-down (No connect for user)
4	$\overline{\text{RESET}}$	I	Pad reset input
5	V_{DD}	P	Power pin
5	B0	I	Bonding option, internally pull-low
6 - 9	PORTA0 - 3	I/O	Bit programmable I/O PA.0 could be external interrupt input($\overline{\text{INT}}$) PA.1, PA.2 could be buzzer output PA.1 (BD), PA.2 ($\overline{\text{BD}}$)
10 - 13	PORTB0 - 3	I/O	Bit programmable I/O, vector interrupt (active falling edge)
14 - 17	PORTC0 - 3	I/O	Bit programmable I/O
18 - 21	PORTD0 - 3	I/O	Bit programmable I/O
22	GND	P	Ground pin
22	B1	I	Bonding option, internally pull-high
23	OSCO	O	Oscillator output pin, connected to crystal oscillator
24	OSCI	I	Oscillator input pin, connected to crystal or external resistor
28 - 25	COM1 - 4	O	Common signal output for LCD display

Total 52 pads for mask type.

Functional Description

CPU

The CPU contains the following functional blocks: Program Counter, Arithmetic Logic Unit (ALU), Carry Flag, Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL), and Stacks.

ROM

The ROM can address 2048 words × 16 bits of program area from $000 to $7FF.
There is an area from address $0 through $4 that is reserved for special interrupt service routines, such as starting at vector address.

Address	Instruction	Remarks
000H	JMP instruction	Jump to RESET service routine
001H	JMP instruction	Jump to External interrupt service routine
002H	JMP instruction	Jump to TIMER0 service routine
003H	JMP instruction	Jump to TIMER1 service routine
004H	JMP instruction	Jump to PB service routine (PORTB)

*JMP instruction can be replaced by any instruction.

RAM

Built-in RAM contains of general purpose data memory, LCD RAM, and system register.
Data memory, LCD RAM, and system register can be accessed by direct addressing in one instruction.

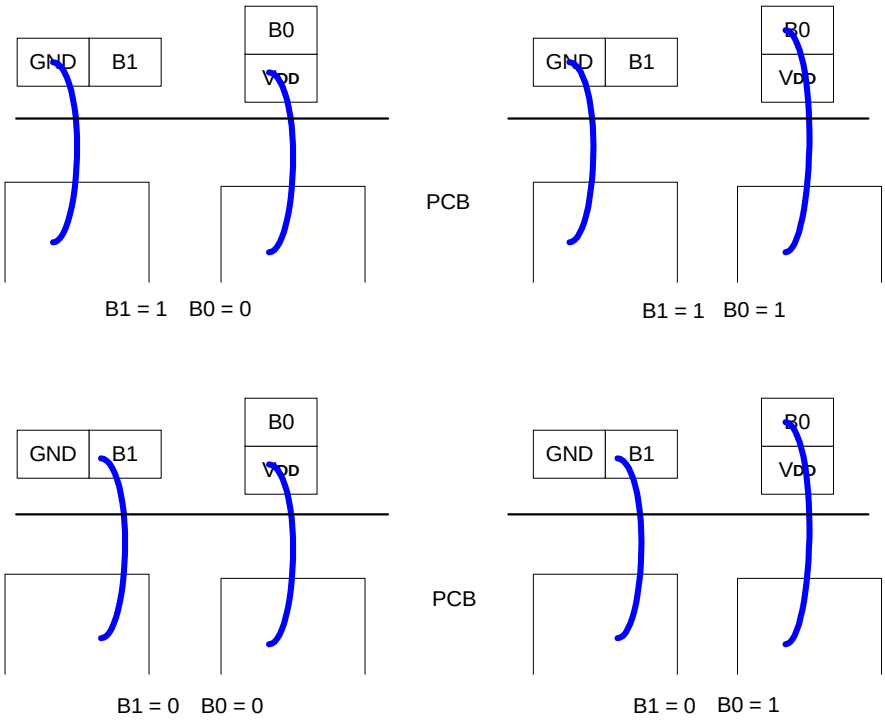
The following is the memory allocation map:
$000 - $01F: System register and I/O
$020 - $11F: Data memory (256 × 4 bits, divided into 2 banks).
$300 - $319: LCD RAM space (26 × 4 bits).

The configuration of system register:

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEX	IET0	IET1	IEP	R/W	Interrupt enable flags
$01	IRQX	IRQT0	IRQT1	IRQP	R/W	Interrupt request flags
$02	-	T0M.2	T0M.1	T0M.0	R/W	Bit0-2: Timer0 Mode register
$03	-	T1M.2	T1M.1	T1M.0	R/W	Bit0-2: Timer1 Mode register
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter register low nibble
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter register high nibble
$06	T1L.3	T1L.2	T1L.1	T1L.0	R/W	Timer1 load/counter register low nibble
$07	T1H.3	T1H.2	T1H.1	T1H.0	R/W	Timer1 load/counter register high nibble
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C	-	-	-	-	-	Reserved
$0D	-	-	B1	B0	R	Bonding option
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	O/S	LCDOFF	HLM	PAM	R/W	Bit0: set PA.1, PA.2 as Alarm O/P Bit1: HEAVY LOAD Mode Bit2: LCD off Bit3: set LCD segment as outport
$14	AEC3	AEC2	AEC1	AEC0	R/W	Alarm Envelope Control
$15	-	-	-	DUTY	R/W	Bit0: change LCD duty to 1/4 duty, 1/3 bias
$16 ~ $1F	-	-	-	-	-	Reserved

System Register 0DH

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power-on
$0DH	-	-	B1	B0	R	Bit0: Bonding option 0, internal weak drive Bit1: Bonding option 1, internal weak drive	Pull low Pull high
	X	X	1	0			Yes
	X	X	0	0		B1 bond to GND	
	X	X	1	1		B0 bond to V_{DD}	
	X	X	0	1		B1 bond to GND and B0 bond to V_{DD}	



NT6612 Bonding Option

Up to 4 different bonding options are possible for the user's needs. The chip's program has 4 different program flows that will vary depending on which bonding option is used. The readable contents of B1 and B0 will differ depending on bonding.

System Register 13

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power on
13	O/S	LCDOFF	HLM	PAM	R/W	Bit0: set PA.1, PA.2 as ALARM output Bit1: heavy load mode Bit2: LCD Power Control Bit3: set seg1 - 4 as output ports	
	X	X	X	0		PORTA.1, PORTA.2 as I/O port	Yes
	X	X	X	1		PORTA.1, PORTA.2 as ALARM output	
	X	X	0	X		No heavy load	Yes
	X	X	1	X		HEAVY LOAD mode	
	X	0	X	X		LCD signal on	Yes
	X	1	X	X		LCD signal off	
	0	X	X	X		Seg1 - 4 as LCD output	Yes
	1	X	X	X		Seg1 - 4 as output ports	

HEAVY LOAD Mode (HLM): This mode is designed for the 32KHz crystal oscillator, so that the oscillation can be maintained in a noisy power environment. The power might drop suddenly when the ALARM is driving a speaker. The HLM is designed to control this power variation. The consumption of power will increase during the use of the HLM mode, but it will not affect the RC oscillator.

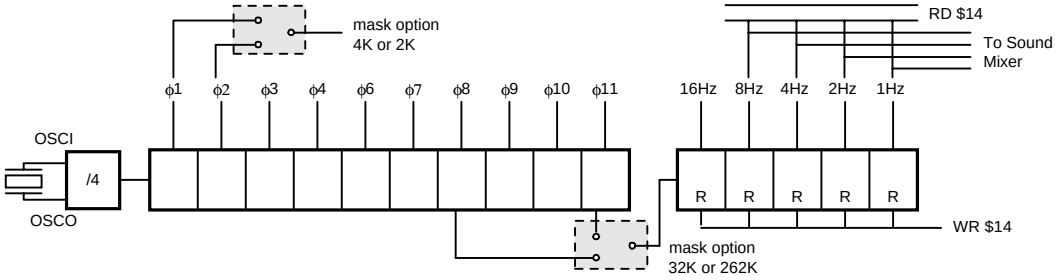
Note: The HLM needs about 5 instruction cycles to set-up the oscillation for 32.768KHz crystal oscillator.

System Register 14, AEC:

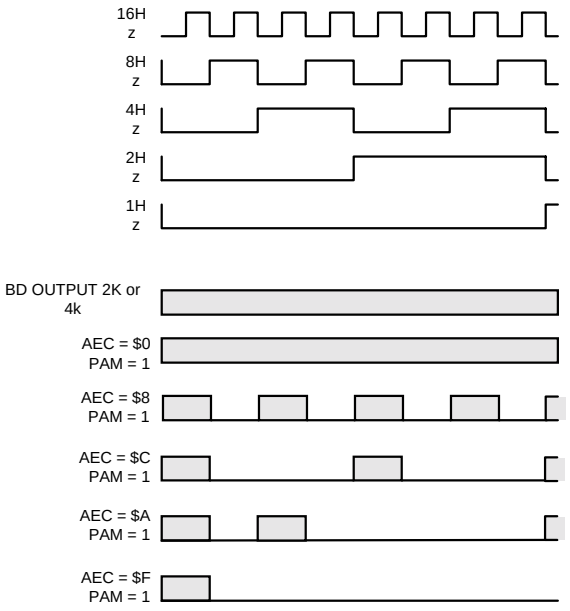
	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power On
$14	AEC3	AEC2	AEC1	AEC0	R/W	ALARM envelope control	
	0	0	0	0		DC envelope	Yes
	X	X	X	1		1Hz envelope	
	X	X	1	X		2Hz envelope	
	X	1	X	X		4Hz envelope	
	1	X	X	X		8Hz envelope	

Default carrier frequency is 4KHz. Can be selected to 2KHz by code option.
WRITE mode: control the envelop selection.
READ mode can read out current envelope wave forms.

Below is the ALARM functional block equivalent circuit diagram. To activate the ALARM function, first switch the PAM to ALARM OUTPUT mode. After setting PAM equal to 1, then set the proper envelope. When the data writes into AEC, the envelope counter will be synchronized at the same time. The programmer can read back the envelope from AEC register and make any pattern changes needed by programmer. The Read operation will not affect the alarm output waveform.



The programming alarm waveform is shown below:



System Register 15

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Description	Power on
$15	-	-	-	DUTY	R/W	Bit0: LCD duty control.	
	-	-	-	1		LCD driver = 1/4 duty, 1/3 bias	
	-	-	-	0		LCD driver = 1/3 duty, 1/2 bias	Yes

LCD Driver

The LCD driver contains a controller, voltage generator, 4 common signal pins, and 26 segment driver pins. There are two different driving modes that are programmable, one is 1/4 duty and 1/3 bias, the other is 1/3 duty and 1/2 bias. DRIVING mode is controlled by register 15 and the power-on status is 1/3 duty , 1/2 bias. The controller consists of display data RAM and a duty generator. The LCD data RAM is a dual port RAM that transfers data to segment pins automatically without a program control.

LCD segment 1 - 4 can also be used as output ports, it is selected by the bit3 of system register 13. When segments 1 - 4 are output ports, data can be written to bit 0 of the same address (300H - 303H). LCD RAM can be used as data memory if needed.
When the "STOP" instruction is executed, the LCD will be turned off, but the data of LCD RAM is the same before execution the "STOP" instruction.

Configuration of LCD RAM area:

(1) When segments 1 - 4 are used as output ports:

Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1
300H	-	-	-	DATA_BIT
301H	-	-	-	DATA_BIT
302H	-	-	-	DATA_BIT
303H	-	-	-	DATA_BIT

(2) When segments 1 - 4 are used as segment outputs:

Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1
300H	SEG1	SEG1	SEG1	SEG1
301H	SEG2	SEG2	SEG2	SEG2
302H	SEG3	SEG3	SEG3	SEG3
303H	SEG4	SEG4	SEG4	SEG4

(3) Segments 5 - 26

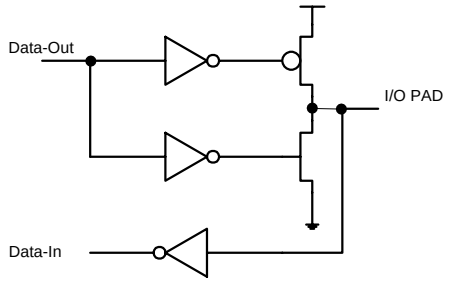
Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1		COM4	COM3	COM2	COM1
304H	SEG5	SEG5	SEG5	SEG5	30FH	SEG16	SEG16	SEG16	SEG16
305H	SEG6	SEG6	SEG6	SEG6	310H	SEG17	SEG17	SEG17	SEG17
306H	SEG7	SEG7	SEG7	SEG7	311H	SEG18	SEG18	SEG18	SEG18
307H	SEG8	SEG8	SEG8	SEG8	312H	SEG19	SEG19	SEG19	SEG19
308H	SEG9	SEG9	SEG9	SEG9	313H	SEG20	SEG20	SEG20	SEG20
309H	SEG10	SEG10	SEG10	SEG10	314H	SEG21	SEG21	SEG21	SEG21
30AH	SEG11	SEG11	SEG11	SEG11	315H	SEG22	SEG22	SEG22	SEG22
30BH	SEG12	SEG12	SEG12	SEG12	316H	SEG23	SEG23	SEG23	SEG23
30CH	SEG13	SEG13	SEG13	SEG13	317H	SEG24	SEG24	SEG24	SEG24
30DH	SEG14	SEG14	SEG14	SEG14	318H	SEG25	SEG25	SEG25	SEG25
30EH	SEG15	SEG15	SEG15	SEG15	319H	SEG26	SEG26	SEG26	SEG26

I/O Port

NT6612 has 16 CMOS quasi-I/O ports, PORTA, PORTB, PORTC, PORTD. All I/O ports are bit programmable.

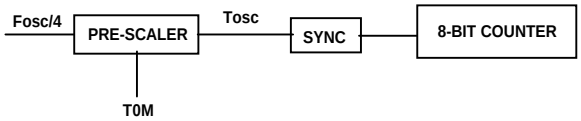
PORTA, B, C, D

If PORTA,B,C,D are pull-high internally, it is weak drive. The equivalent circuit is below:



Timer

NT6612 has two 8-bit timers. Their operation is counting-up. The timers consist of an 8-bit counter and an 8-bit preload register.



The timers provide the following functions:
- Programmable interval timer function.
- Read counter value.

Timer Mode Register

Timer0 and Timer1 Configuration and Operation

Both the Timer0 and Timer1 consists of an 8-bit write-only timer load register (TL0L, TL0H; TL1L, TL1H), and an 8-bit read-only timer counter (TC0L, TC0H; TC1L, TC1H). Each of them has low order digits and high order digits. The timer counter can be initialized by writing data into the timer load register (TL0L, TL0H; TL1L, TL1H).

The low-order digit should be written first, and then the high-order digit. The timer counter is loaded with contents of the load register automatically when the high order digit is written or counts overflow happen. The timer overflow will generate an interrupt if the interrupt enable flag is set.

The timer can be programmed in several different system clock sources by setting the Timer Mode register (TM0,TM1).

Timer Load Register: Since the register H controls the physical READ and WRITE operations, please follow these steps:

Write Operation:
Low nibble first;
High nibble to update the counter

Read Operation:
High Nibble first;
Low nibble followed.

Interrupt

Four interrupt sources are available on NT6612:

- External interrupt ($\overline{INT}$ share with PA.0)
- Timer0 interrupt
- Timer1 interrupt
- Port's falling edge detection interrupt ($\overline{PB}$)

The configuration of system register $00:

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remark
$00	IEX	IET0	IET1	IEP	R/W	Interrupt enable flags

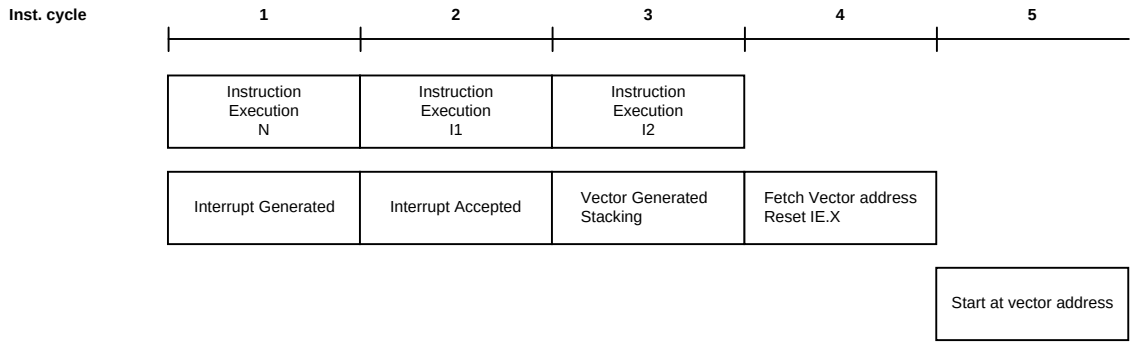
External Interrupt ($\overline{INT}$)

External interrupt is shared with the bit0 of PORTA. When bit3 of system register 0(IEX) is set to 1, the external interrupt will be enabled, and a falling edge signal on PA.0 will generate an external interrupt. (Note: while external interrupt is enabled, writing a "0" to bit0 of PORTA will generate an external interrupt).

Timer0, Timer1 Interrupt, Port Interrupt and I/O Ports

The input clock of Timer0 and Timer1 are based on OSC clock. The programming of Timer interrupt, Port interrupt and I/O ports refer to NT6610C spec.

● Interrupt Servicing Sequence Diagram:



Interrupt Nesting:

During the NT6610C CPU interrupt service, the user can enable any INTERRUPT enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

System Clock

NT6612 has one clock source. OSC1 is 32.768KHz crystal or 262KHz RC determined by code option. The OSC generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals (TIMER0, TIMER1, LCD).

Instructions

All instructions are one cycle and one word instructions. The characteristics is memory oriented operation.

Arithmetic and Logical Instruction

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X(,B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X(,B)	00000 1bbb xxx xxxx	AC,Mx ← Mx + AC + CY	CY
ADD X(,B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X(,B)	00001 1bbb xxx xxxx	AC,Mx ← Mx + AC	CY
SBC X(,B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X(,B)	00010 1bbb xxx xxxx	AC,Mx ← Mx + -AC + CY	CY
SUB X(,B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X(,B)	00011 1bbb xxx xxxx	AC,Mx ← Mx + -AC +1	CY
EOR X(,B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X(,B)	00100 1bbb xxx xxxx	AC,Mx ← Mx ⊕ AC	
OR X(,B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X(,B)	00101 1bbb xxx xxxx	AC,Mx ← Mx | AC	
AND X(,B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X(,B)	00110 1bbb xxx xxxx	AC,Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3]; AC[0] → CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X,I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X,I	01001 iiii xxx xxxx	AC,Mx ← Mx + I	CY
SBI X,I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X,I	01011 iiii xxx xxxx	AC,Mx ← Mx + -I + 1	CY
EORIM X,I	01100 iiii xxx xxxx	AC,Mx ← Mx ⊕ I	
ORIM X,I	01101 iiii xxx xxxx	AC,Mx ← Mx | I	
ANDIM X,I	01110 iiii xxx xxxx	AC,Mx ← Mx & I	

* In the assembler ASM66 V1.0, EORIM memonic is EORI. However, EORI has the same operation identical with EORIM. Same for the ORIM with respect to ORI, and ANDIM with respect to ANDI.

Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC;Mx ← Decimal adjust for add.	CY
DAS X	11001 1010 xxx xxxx	AC;Mx ← Decimal adjust for sub.	CY

Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X(,B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X(,B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X,I	01111 iiii xxx xxxx	AC,Mx ← I	

Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC=0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC≠0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY=1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY≠1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC(0)=1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC(1)=1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC(2)=1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC(3)=1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC +1 PC ← X(Not include p)	
RTNW H;L	11010 000h hhh llll	PC ←ST; TBR ← hhhh; A ← llll	
RTNI	11010 1000 000 0000	CY;PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X(Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (A)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank=000
p	ROM page =0		
ST	Stack	TBR	Table Branch Register

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +5.5V

Input Voltage. . . . . -0.3V to V_{DD}+0.3V

Operating Ambient Temperature . . . . . 0°C to +60°C

Storage Temperature . . . . . -55°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V_{DD} = 3.0V, GND = 0V, T_A = 25°C, F_{OSC} = 32.768KHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	2.2	3	3.4	V	
Operating Current	I_{OP}		5	10	μA	All output pins unload execute NOP instruction
Standby Current	I_{SB1}		1.5	2.5	μA	All output pins unload (HALT mode) exclude LCD current
Standby Current	I_{SB2}			1	μA	All output pins unload (STOP mode) LCD off, no current
Input High Voltage	V_{IH}	0.7 × V_{DD}		V_{DD} + 0.3	V	PORTA, PORTB, PORTC, PORTD
Input Low Voltage	V_{IL}	GND - 0.3		0.2 × V_{DD}	V	PORTA, PORTB, PORTC, PORTD
Output High Voltage	V_{OH1}	2.3			V	PORTA, PORTB, PORTC (I_{OH} = 15μA)
Output Low Voltage	V_{OL1}			0.2	V	PORTA, PORTB, PORTC (I_{OL}= 300μA)
Output High Voltage	V_{OH2}	2.1			V	BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), I_{OH} = 2mA
Output Low Voltage	V_{OL2}			0.9	V	BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), I_{OL} = 2mA
Output High Voltage	V_{OH3}	2.8			V	SEGx, I_{OH} = 3μA , SEG1 - 4 to be output port (for reference only)
Output Low Voltage	V_{OL3}			0.2	V	SEGx, I_{OL} = 3μA , SEG1 - 4 to be output port (for reference only)
Output High Voltage	V_{OH4}	2.8			V	COMx, I_{OH} = 8μA (for reference only)
Output Low Voltage	V_{OL4}			0.2	V	COMx, I_{OL} = 8μA (for reference only)
LCD Lighting	I_{LCD}		6.5	7.5	μA	HALT mode

DC Electrical Characteristics (V_{DD} = 5.0V, GND = 0V, T_A = 25°C, F_{OSC} = 32.768KHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	4.5	5.0	5.4	V	PORTA, PORTB, PORTC (I_{OH} = 15μA)
Operating Voltage	I_{OP}		15	30	μA	PORTA, PORTB, PORTC (I_{OL}= 300μA)
Standby Current	I_{SB1}		4.5	7.5	μA	BD/$\overline{BD}$ (set PA.1 and PA.2 to be ALARM output), I_{OH} = 2mA
Standby Current	I_{SB2}			1	μA	All output pins unload (STOP mode) LCD off, no current
Input High Voltage	V_{IH}	0.7 × V_{DD}		V_{DD} + 0.3	V	PORTA, PORTB, PORTC, PORTD
Input Low Voltage	V_{IL}	GND - 0.3		0.2 × V_{DD}	V	PORTA, PORTB, PORTC, PORTD
Output High Voltage	V_{OH1}	4.3			V	SEGx, I_{OH} = 3μA , SEG1 - 4 to be output port (for reference only)
Output Low Voltage	V_{OL1}			0.3	V	SEGx, I_{OL} = 3μA , SEG1 - 4 to be output port (for reference only)
Output High Voltage	V_{OH2}	4.1			V	COMx, I_{OH} = 8μA (for reference only)
Output Low Voltage	V_{OL2}			1.0	V	COMx, I_{OL} = 8μA (for reference only)
Output Low Voltage	V_{OH3}	4.8				
Output Low Voltage	V_{OL3}			0.3		
Output Low Voltage	V_{OH4}	4.8				
Output Low Voltage	V_{OL4}			0.3		
LCD Lighting	I_{LCD}		19.5	23	μA	HALT mode

Note:

1. Operation frequency vs. I_{SB1}

   I_{SB1x} = (Frequency/32.768KHz) ×I_{SB1}×0.8

2. Operation frequency vs. I_{op}

   I_{opx} = (Frequency/32.768KHz) × I_{op}×0.8

3. HLM vs. Iop, I_{sb1} and I_{sb2}

   If HLM = 1, I_{opx} = I_{op}×2, I_{SB1x} = I_{SB1}×2, I_{SB2x} = I_{SB1}×2

AC Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25°C, F_{OSC} = 32.768KHz , unless otherwise specified)

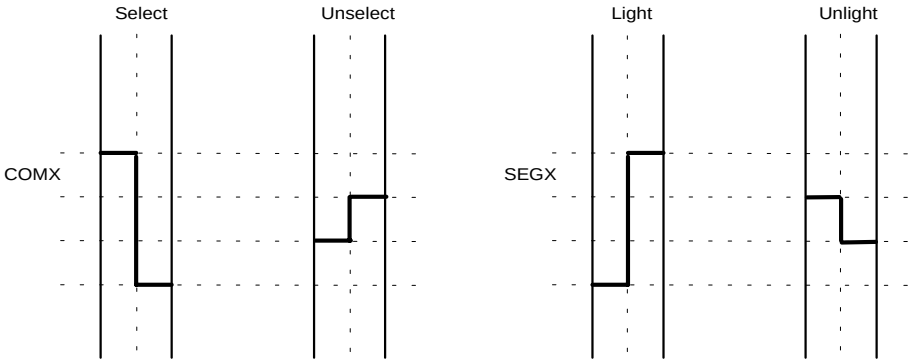
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillation Start Time	T_{STT}		2	5	s	
Halt Time	T_{HTT}		0		s	I_{DD} reduces to Isb1 after instruction executing
Stop Time	T_{SPT}		0		s	I_{DD} reduces to Isb2 after instruction executing
Frequency Stability	Δ F/F			1	PPM	[F(3.0)-F(2.4)]/F(3.0), crystal oscillator (for reference only)
Frequency Variation	Δ F/F			10	PPM	C1 = 5 - 25P (for reference only)

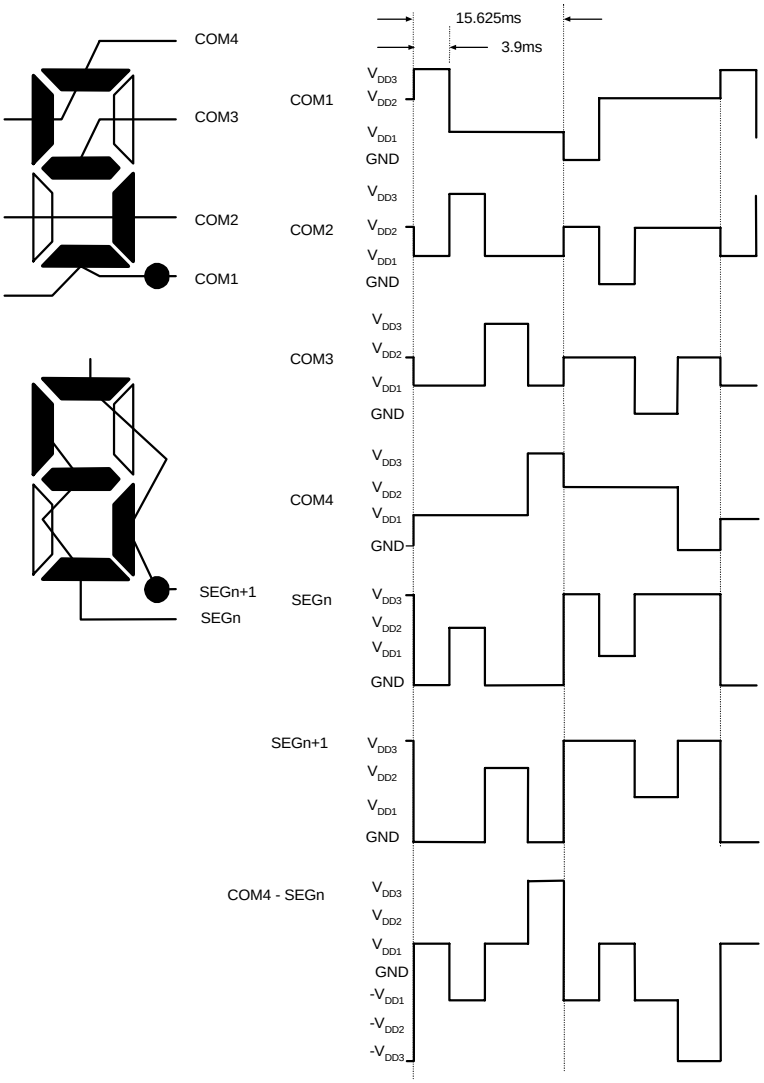
AC Characteristics (V_{DD} = 3.0V, GND = 0V, T_A= 25°C, F_{OSC}= 262KHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillation Start Time	T_{STT}			2	ms	
Halt Time	T_{HTT}		0		s	I_{DD} reduces to Isb1 after instruction executing
Stop Time	T_{SPT}		0		s	I_{DD} reduces to Isb3 after instruction executing
Frequency Stability	|Δ F|/F			10	%	|F(3.0)-F(2.4)|/F(3.0), RC oscillator (for reference only)
Frequency Variation	|Δ F|/F			15	%	variation caused by process variation (for reference only)

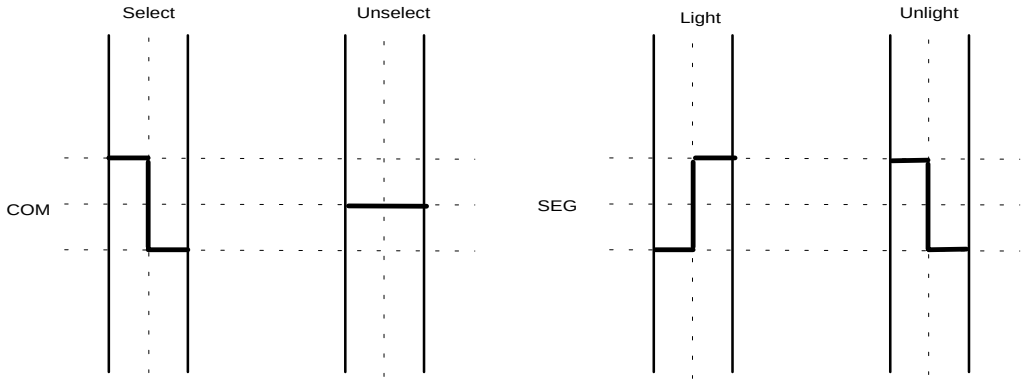
Timing Waveform

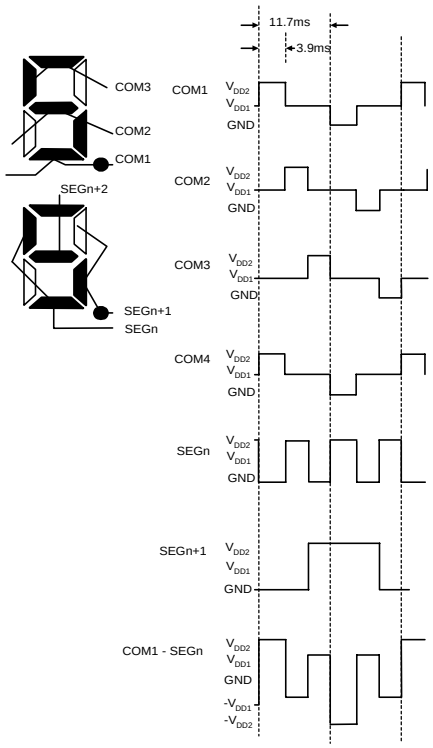
1/4 duty, 1/3 bias LCD waveform



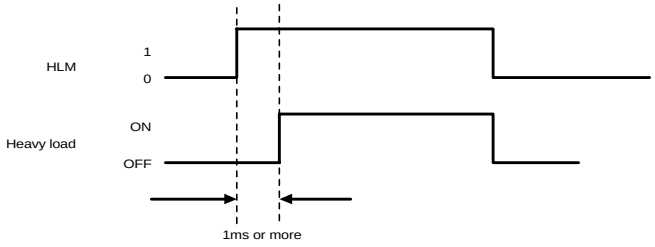


1/3 duty, 1/2 bias LCD waveform





HLM waveform

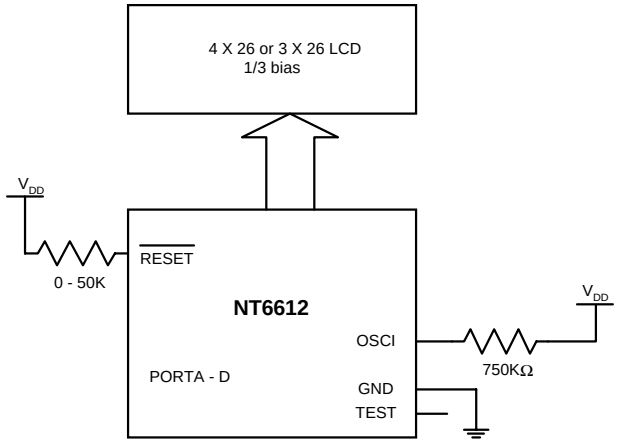


Application Circuits (for reference only)

NT6612 chip substrate connects to system ground.

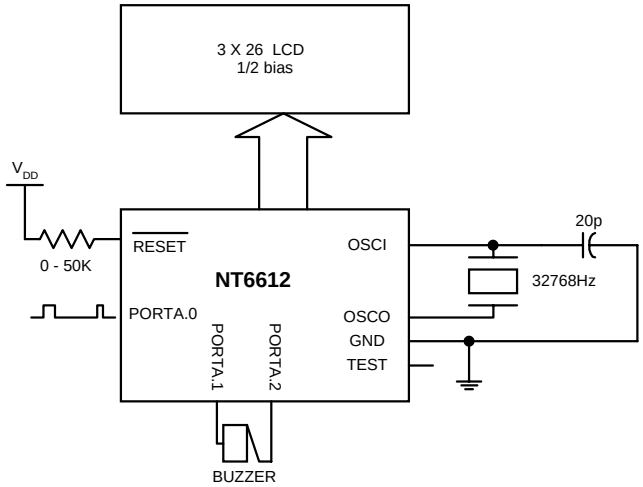
AP1

OSC : RC: 262K (code option)
LCD Panel: 1/4 duty, 1/3 bias; (S/W select 1/4 duty, auto 1/3 bias)
LCD Panel: 1/3 duty, 1/3 bias; (S/W select 1/4 duty, auto 1/3 bias; ignore duty 4 segments)
PORTA - D : I/O



AP2

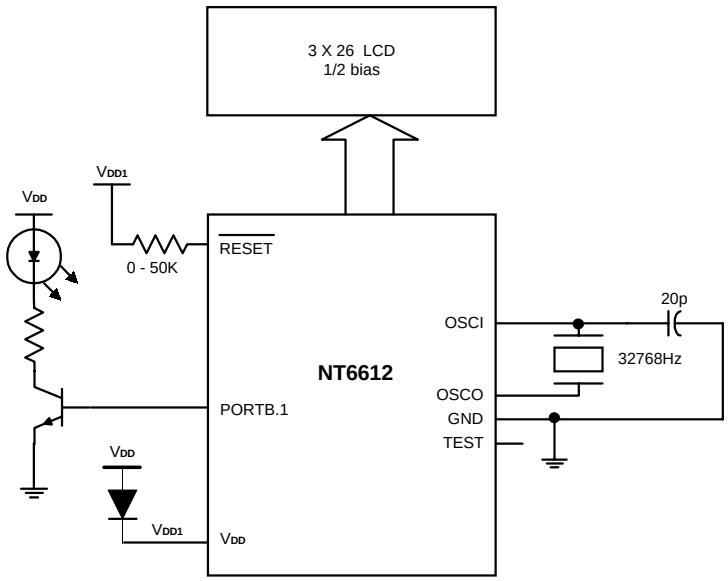
OSC: 32.768KHz crystal (code option)
LCD: 1/3 duty, 1/2 bias
PORTB - D: I/O
PORTA.0: external interrupt
PORTA.1, PORTA.2: ALARM output (carrier frequency: 2KHz or 4KHz code option) (code option)



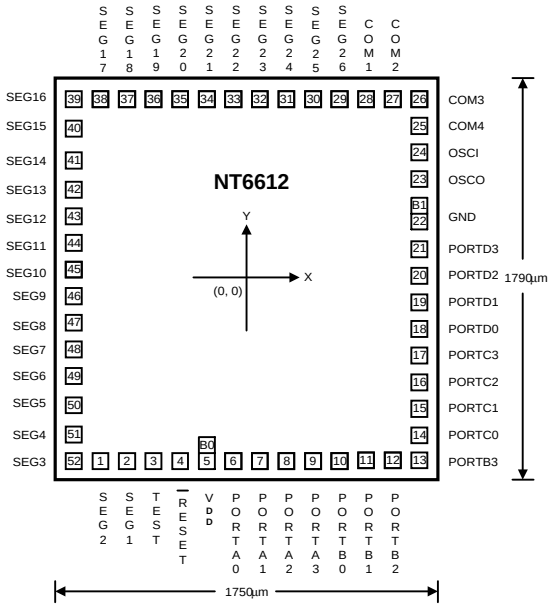
Application Circuits (continued)

AP3

OSC: 32.768KHz
LCD: 1/3 duty, 1/2 bias
PORTB.1 = Output
When V_{DD} is higher than V_{LCD}, reducing V_{DD} to V_{DD1} can regulate the voltage.



Bonding Diagram



* Substrate connects to GND.
The bonding wire with diameter of 1.0mil is recommended.

unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	SEG2	-627	-770	26	COM3	747	770
2	SEG1	-517	-770	27	COM2	625	770
3	TEST	-407	-770	28	COM1	505	770
4	$\overline{\text{RESET}}$	-297	-770	29	SEG26	385	770
5	V_{DD}	-164	-770	30	SEG25	275	770
	B0	-I64	-673	31	SEG24	165	770
6	PORTA0	-54	-770	32	SEG23	55	770
7	PORTA1	55	-770	33	SEG22	-54	770
8	PORTA2	165	-770	34	SEG21	-164	770
9	PORTA3	275	-770	35	SEG20	-274	770
10	PORTB0	385	-770	36	SEG19	-392	770
11	PORTB1	505	-770	37	SEG18	-515	770
12	PORTB2	625	-770	38	SEG17	-625	770
13	PORTB3	749	-768	39	SEG16	-747	770
14	PORTC0	747	-650	40	SEG15	-747	641
15	PORTC1	747	-530	41	SEG14	-747	513
16	PORTC2	747	-421	42	SEG13	-747	385
17	PORTC3	747	-309	43	SEG12	-747	275
18	PORTD0	747	-200	44	SEG11	-747	165
19	PORTD1	747	-90	45	SEG10	-747	55
20	PORTD2	747	19	46	SEG9	-747	-55
21	PORTD3	747	129	47	SEG8	-747	-165
22	GND	747	240	48	SEG7	-747	-275
	B1	747	309	49	SEG6	-747	-385
23	OSCO	747	419	50	SEG5	-747	-513
24	OSCI	747	530	51	SEG4	-747	-641
25	COM4	747	650	52	SEG3	-747	-770

Ordering Information

Part No.	Package
NT6612H	CHIP FORM