




Battery Protect Solution IC

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DATA SHEET

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Battery Protect Solution IC

EL1501

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■ Features

1. The protection IC and The Dual-Nch MOSFET to use common Drain are integrated into One-packaging IC.
2. Reduced Pin-Count by fully connecting internally.

3. Application Part

1) Protection IC

- ① Uses high withstand voltage CMOS process.
 - The charger section can be connected up to absolute maximum rating 20V.
- ② Detection voltage precision
 - Overcharge detection voltage $\pm 60\text{mV}$ (Ta=25°C)
 - Overdischarge detection voltage $\pm 110\text{mV}$ (Ta=25°C)
 - Discharging overcurrent detection voltage $\pm 35\text{mV}$ (Ta=25°C)
- ③ Built-in detection delay times
 - Overcharge detection delay time Typ 0.08s / Max 0.20s (Ta=25°C)
 - Overdischarge detection delay time) Typ 40ms / Max 100ms (Ta=25°C)
 - Discharging overcurrent detection delay time) Typ 10ms / Max 30ms (Ta=25°C)
 - Short detection delay time) Typ 5 μs / Max 50 μs (Ta=25°C)
- ④ With abnormal charger has an ability to detect function
- ⑤ 0V charge function allowed

2) FET

- ① Using advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltage as low as 2.5V while retaining a 12V $V_{GS(MAX)}$.
- ② The protection for ESD
- ③ Common drain configuration
- ④ General characteristics
 - V_{DS} (V) = 20V
 - I_D (A) = 6A
 - $R_{SS(ON)} < 60\text{m}\Omega$ ($V_{GS} = 4.5\text{V}$, $I_D = 5\text{A}$)
 - ESD Rating : 2000V HBM

Battery Protect Solution IC**ELI501****■ Outline**

This is a battery protect solution IC which is integrated with built-in the protection IC to use a lithium ion/lithium polymer secondary batteries developed for 1-cell series and Dual-Nch MOSFET. It functions to protect the battery by detecting overcharge, overdischarge, discharge overcurrent, charge overcurrent and other abnormalities as turning off internal Nch MOSFET. The protection IC is composed of four voltage detectors, short detection circuit, reference voltage sources, oscillator, counter circuit and logical circuits.

The C_{OUT} pin (charge FET control pin) and D_{OUT} pin (discharge FET control pin) outputs are CMOS output, and can drive the internal Nch MOSFET directly. The C_{OUT} output becomes low level after delay time fixed in the IC if overcharge is detected. The D_{OUT} output becomes low level after delay time fixed in the IC if overdischarge, discharge overcurrent or short is detected.

On overcharge state, if the V_{DD} voltage is less than the overcharge release voltage, the C_{OUT} output becomes high level after delay time fixed in the IC. On overdischarge state, if the voltage of the battery rises more than the overdischarge detection voltage with connecting the charger, the D_{OUT} output becomes high level after delay time fixed in the IC. Charging current can be supplied to the battery discharged up to 0V.

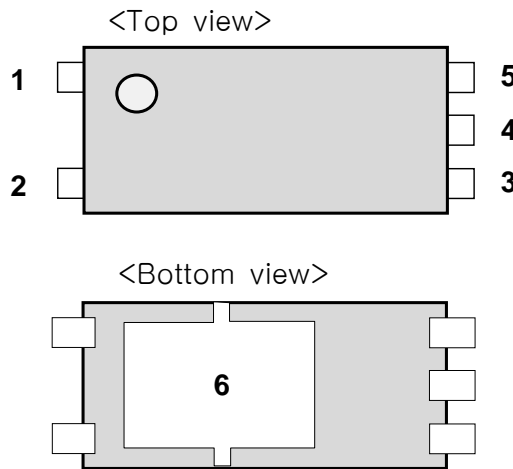
Once discharge overcurrent or short have been detected, if the state of discharge overcurrent or short is released by opening the loads, the D_{OUT} output becomes high level after delay time fixed in the IC. On overdischarge state, the supply current is reduced as less as possible. Once charge overcurrent has been detected, the state of charge overcurrent is released by opening the charger and setting the load.

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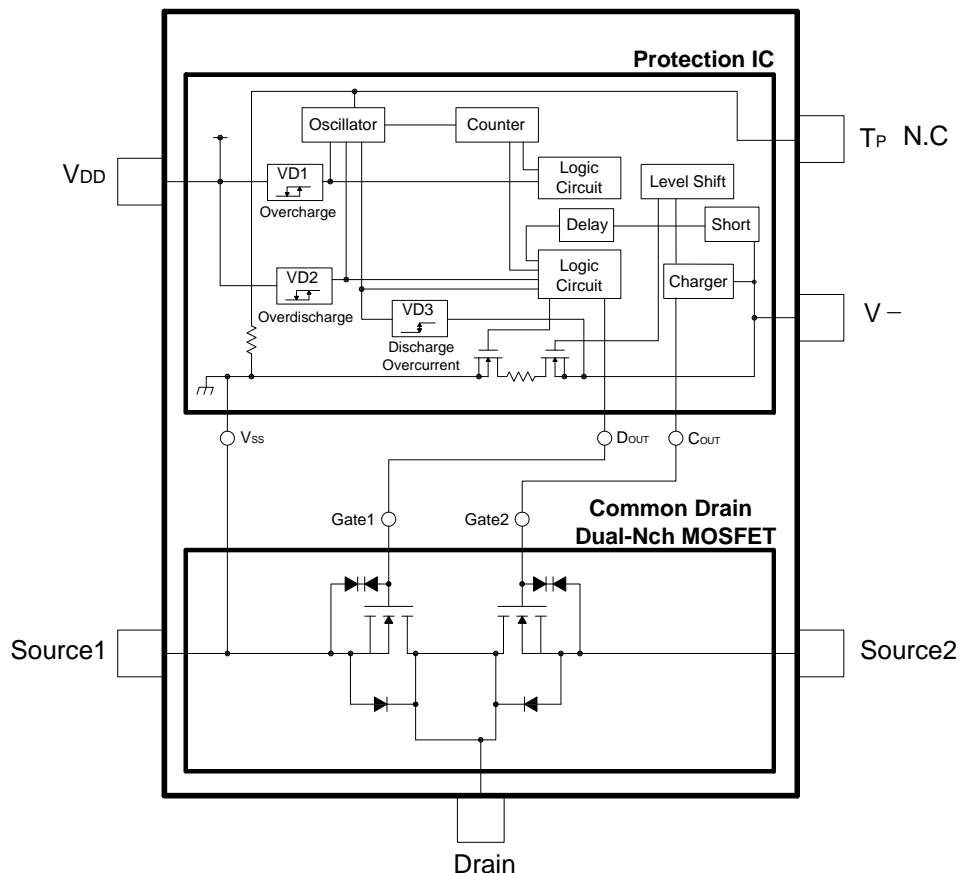
Pin Assignment

[Package: TEP-5L]



1	T_P (N.C)
2	Source 1(same as V_{SS})
3	Source 2
4	V_{DD}
5	V_-
6	Drain

Block Diagram



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Absolute Maximum Rating

※ $T_{OPR}=25^{\circ}\text{C}$, Source1(V_{SS})=0V

Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	-0.3 ~ 10	V
V- Terminal Input Voltage	V-	$V_{DD}-24 \sim V_{DD}+0.3$	V
C _{OUT} Terminal Output Voltage	V_{COUT}	$V_{DD}-24 \sim V_{DD}+0.3$	V
D _{OUT} Terminal Output Voltage	V_{DOUT}	$V_{SS}-0.3 \sim V_{DD}+0.3$	V
Operation Temperature	T_{OPR}	-40 ~ 85	°C
Storage Temperature	T_{STG}	-40 ~ 125	°C
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±12	V

Electrical Characteristics

※ $T_{OPR}=25^{\circ}\text{C}$

Item	Symbol	Measure Condition	Min.	Typ.	Max.	Unit	*1
Operating Input Voltage	V_{DD1}	$V_{DD} - V_{SS}$	1.5	-	8.0	V	A
Minimum Operating Voltage for 0V Charging	V_{ST}	$V_{DD} - V-$, $V_{DD} - V_{SS}=0V$	-	-	1.5	V	A
C _{OUT} Pin Nch ON Voltage	V_{OL1}	-	-	0.1	0.5	V	-
C _{OUT} Pin Pch ON Voltage	V_{OH1}	-	$V_{DD}-0.1$	$V_{DD}-0.02$	-	V	-
D _{OUT} Pin Nch ON Voltage	V_{OL2}	-	-	0.1	0.5	V	-
D _{OUT} Pin Pch ON Voltage	V_{OH2}	-	$V_{DD}-0.1$	$V_{DD}-0.02$	-	V	-
Current Consumption	I_{DD}	$V_{DD}=3.9V$, $V-=0V$	-	3.0	6.0	μA	L
Current Consumption at Stand-By	I_S	$V_{DD}=2.0V$	-	-	0.1	μA	L
Overcharge Detection Voltage	V_{DET1}	$R1=100\Omega$	4.240	4.300	4.360	V	B
Overcharge Release Voltage	V_{REL1}	$R1=100\Omega$	4.040	4.100	4.160	V	B
Overdischarge Detection Voltage	V_{DET2}	$V-=0V$, $R1=100\Omega$	2.290	2.400	2.510	V	D
Overdischarge Release Voltage	V_{REL2}	$R1=100\Omega$	2.890	3.000	3.110	V	D
Discharging Overcurrent Detection Voltage	V_{DET3}	$V_{DD}=3.5V$, $R2=1.0k\Omega$	0.115	0.150	0.185	V	F
Short Detection Voltage	V_{SHORT}	$V_{DD}=3.6V$	1.00	1.35	1.70	V	F
Charger Detection Threshold Voltage	V_{CHA}	-	-1.2	-0.7	-0.2	V	G

Note : *1 The test circuit symbols.

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※ T_{OPR}=25℃

Item	Symbol	Measure Condition	Min.	Typ.	Max.	Unit	*1
Overcharge Detection Delay Time	t _{DET1}	V _{DD} =3.6V→4.5V	–	0.08	0.20	s	B
Overdischarge Detection Delay Time	t _{DET2}	V _{DD} =3.6V→2.0V	–	40	100	ms	D
Discharging Overcurrent Detection Delay Time	t _{DET3}	V _{DD} =3.5V, V ₋ =0V→1V	–	10	30	ms	F
Short Detection Delay Time	t _{SHORT}	V _{DD} =3.0V, V ₋ =0V→3V	–	5	50	μs	F
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	20	–	–	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V, V _{GS} =0V	–	–	1	μA	
Gate-Body Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±12V	–	–	±100	nA	
Gate-Source Breakdown Voltage	BV _{GSO}	V _{DS} =0V, I _G =±250μA	±12	–	–	V	
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.4	–	0.9	V	
Static Source-Source ON-Resistance	R _{SS(ON)}	V _{GS} =10V, I _O =5A	–	42	50	mΩ	
		V _{GS} =4.5V, I _O =5A	–	50	60	mΩ	
		V _{GS} =2.5V, I _O =3A	–	62	76	mΩ	
Diode Forward Voltage	V _{SD}	I _S =1.7A, V _{GS} =0V	–	0.74	1.20	V	

Note : *1 The test circuit symbols.

*2 The parameter is guaranteed by design.

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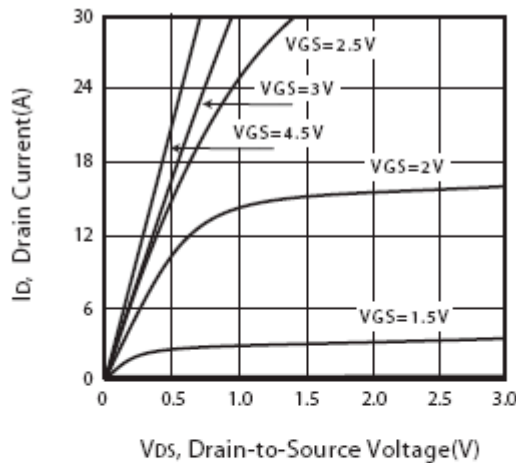


Figure 1. Output Characteristics

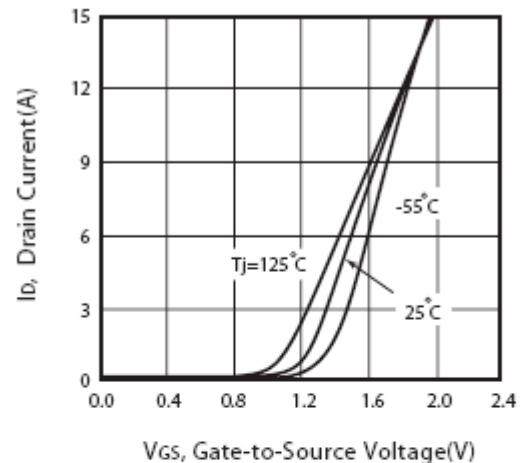


Figure 2. Transfer Characteristics

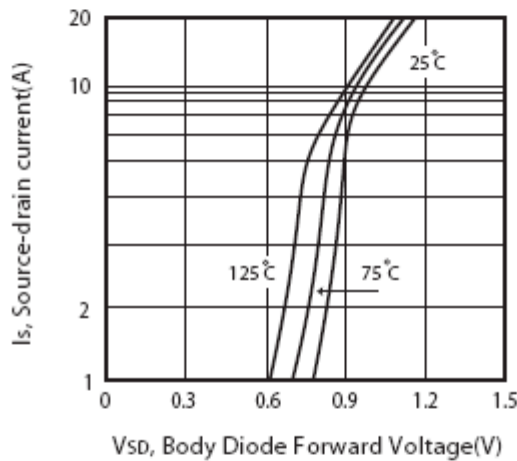


Figure 3. Body Diode Forward Voltage Variation with Source Current

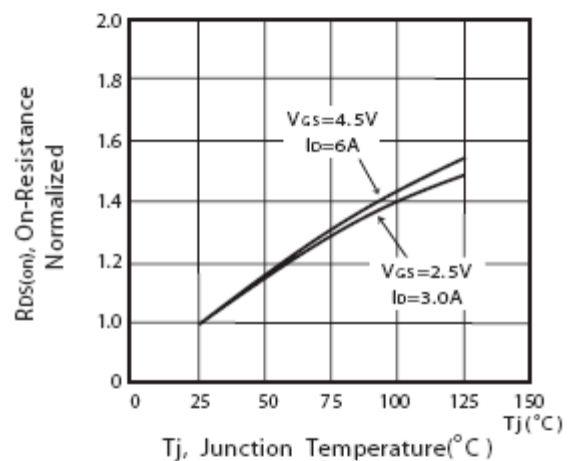


Figure 4. On-Resistance Variation with Drain Current and Temperature

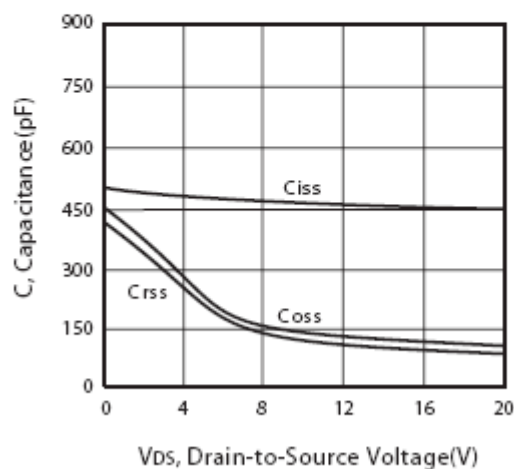


Figure 5. Capacitance

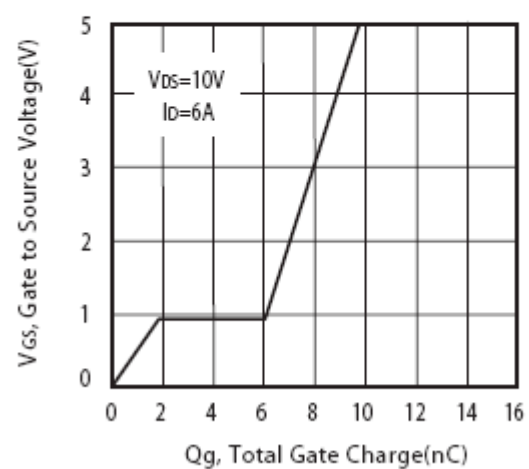


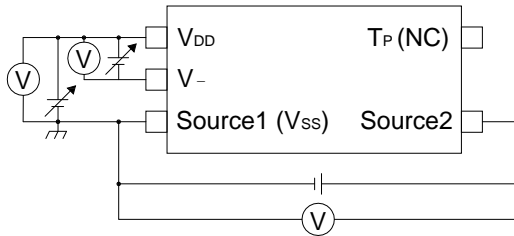
Figure 9. Gate Charge

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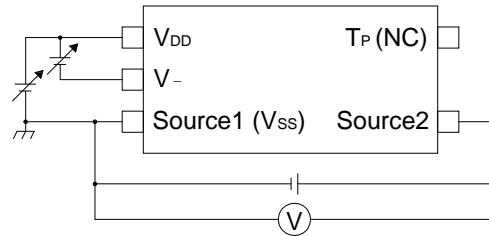
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■ Measuring Circuit

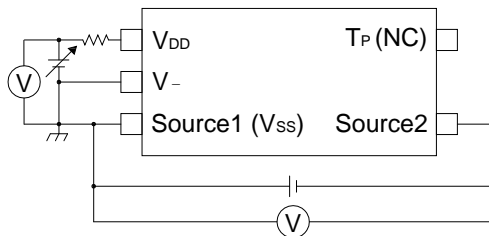
A.



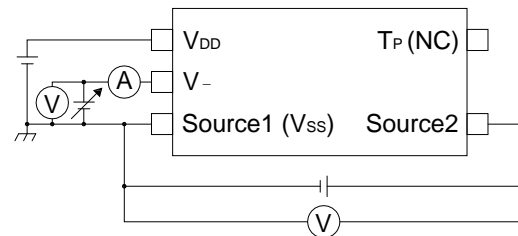
E.



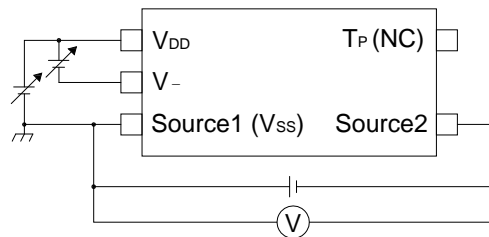
B.



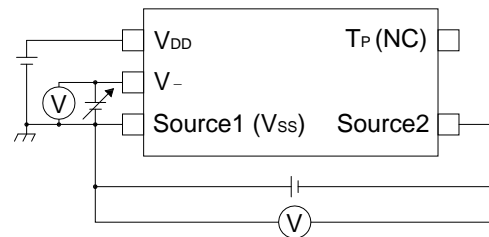
F.



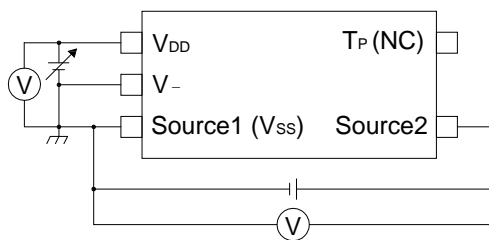
C.



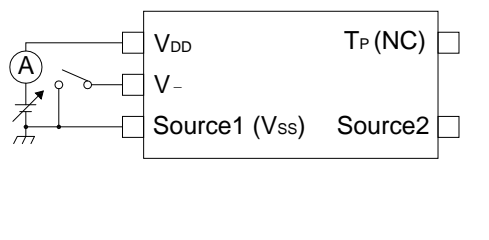
G.



D.



H.



Battery Protect Solution IC**ELI501****■ Operation****1. Overcharge detector (VD1)**

The VD1 monitors V_{DD} pin voltage during charge. In the state of charging the battery, it will detect the overcharge state of the battery if the V_{DD} terminal voltage becomes higher than the overcharge detection voltage(Typ. 4.300V). And then the C_{OUT} terminal turns to low level, so the internal charging control Nch MOSFET turns OFF and it forbids to charge the battery.

After detecting overcharge, it will release the overcharge state if the V_{DD} terminal voltage becomes lower than the overcharge release voltage(Typ.4.100V). And then the C_{OUT} terminal turns to high level, so the internal charging control Nch MOSFET turns ON, and it accepts to charge the battery.

When the V_{DD} terminal voltage is higher than the overcharge detection voltage, to disconnect the charger and connect the load, leave the C_{OUT} terminal low level, but it accepts to conduct load current via the paracritical body diode of the internal Nch MOSFET. And then if the V_{DD} terminal voltage becomes lower than the overcharge detection voltage, the C_{OUT} terminal turns to high level, so the internal Nch MOSFET turn ON, and it accepts to charge the battery.

The overcharge detection and release have delay time decided internally. When the V_{DD} terminal voltage becomes higher than the overcharge detection voltage, if the V_{DD} terminal voltage becomes lower than the overcharge detection voltage again within the overcharge detection delay time(Typ. 0.08s), it will not detect overcharge. And in the state of overcharge, when the V_{DD} terminal voltage becomes lower than the overcharge release voltage, if the V_{DD} terminal voltage backs higher than the overcharge release voltage again within the overcharge release delay time, it will not release overcharge.

The output driver stage of the C_{OUT} terminal includes a level shifter, so it will output the V_- terminal voltage as low level. The output type of the C_{OUT} terminal is CMOS output between V_{DD} and V_- terminal voltage.

2. Overdischarge detector (VD2)

The VD1 monitors V_{DD} pin voltage during discharge. In the state of discharging the battery, it will detect the overdischarge state of the battery if the V_{DD} terminal becomes lower than the overdischarge detection voltage (Typ. 2.400V). And then the D_{OUT} terminal turns to low level, so the internal discharging control Nch MOSFET turn OFF and it forbids to discharge the battery.

The release from the overdischarge state is done by connecting the charger. If the charger is connected and the V_{DD} terminal voltage is lower than the overdischarge detection voltage, it accepts to conduct charge current via the paracritical body diode of the internal Nch MOSFET. And then if the V_{DD} terminal voltage becomes higher than the overdischarge detection voltage, the D_{OUT} terminal turns to high level, so the external Nch MOSFET turns ON, and it accepts to discharge the battery. If the charger is connected and the V_{DD} terminal voltage is higher than the overdischarge detection voltage, the D_{OUT} terminal will turn to high level with the delay time.

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When the battery voltage is about 0V, if the charger voltage is higher than the minimum operating voltage for 0V charging (Max. 1.5V), the C_{OUT} terminal outputs high level and it accepts to conduct charging current.

The overdischarge detection have delay time decided internally. When the V_{DD} terminal voltage becomes lower than the overdischarge detection voltage, if the V_{DD} terminal voltage becomes higher than the overdischarge detection voltage again within the overdischarge detection delay time (Typ. 40ms), it will not detect overdischarge. Moreover, the overdischarge release delay time exists, too.

All the circuits are stopped, and after the overdischarge is detected, it is assumed the state of the standby, and decreases the current (standby current) which IC consumes as much as possible. (When V_{DD}=2V, Max. 0.1uA).

The output type of the D_{OUT} terminal is CMOS output between V_{DD} and V_{SS} terminal voltage.

3. Discharge overcurrent detector, Short detector (VD3, Short Detector)

In the state of chargeable and discharge, VD3 monitors the voltage level of V₋ pin. If the V₋ terminal voltage becomes higher than the discharging overcurrent detection voltage (Typ. 0.150V) by short of loads, etc., it will detect discharging overcurrent state. If the V₋ terminal voltage becomes higher than short detection voltage (Typ. 1.35V), it will detect discharging overcurrent state, too. And then the D_{OUT} terminal outputs low level, so the internal discharging control Nch MOSFET turns OFF, and it protects from large current discharging.

The discharging overcurrent detection has delay time decided internally. When the V₋ terminal voltage becomes higher than the discharging overcurrent detection voltage, if the V₋ terminal voltage becomes lower than the discharging overcurrent detection voltage within the discharging overcurrent detection delay time (Typ. 10ms), it will not detect discharging overcurrent. Moreover, the discharging overcurrent release delay time exists, too.

The short detection delay time (Typ. 5us) decided internally exists, too.

4. DS (Delay Shortening) function

The delay time of overcharge, overdischarge, discharging overcurrent, charging overcurrent detection and release can be shortened by making the DS terminal to V_{DD} level voltage.

The overcharge detection delay time can be adjusted to several 100us by making the DS terminal to middle level voltage, so test time of protection module can be shortened.

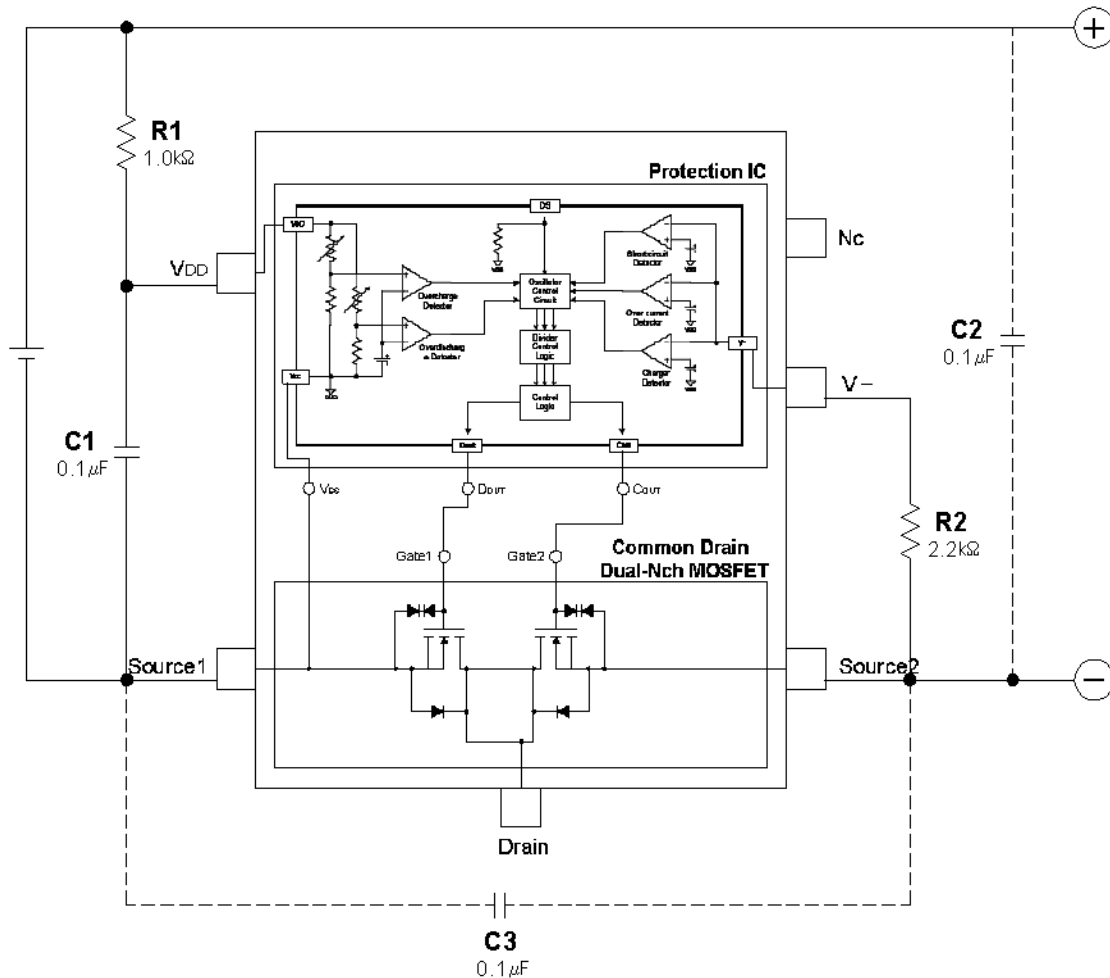
In the DS terminal, the pull-down resistance of 13kohm is connected between V_{SS}.

Please short the DS terminal and V_{SS} terminal when using usually.

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■ Application Circuit (Example)



※ Application Hint

R1 and C1 stabilize a supply voltage ripple. However, the detection voltage rises by the current of penetration in IC of the voltage detection when R1 is enlarged, so the value of R1 is adjusted to 100Ω or less. Moreover, adjust the value of C1 to 0.1uF or more to do the stability operation, please.

R1 and R2 resistors are current limit resistance if a charger is connected reversibly or a highvoltage charger that exceeds the absolute maximum rating is connected. R1 and R2 may cause a power consumption will be over rating of power dissipation, therefore the 'R1+R2' should be more than 1kohm. Moreover, if R2 is too enlarged, the charger connection release cannot be occasionally done after the overdischarge is detected, so adjust the value of R2 to 5kohm or less, please.

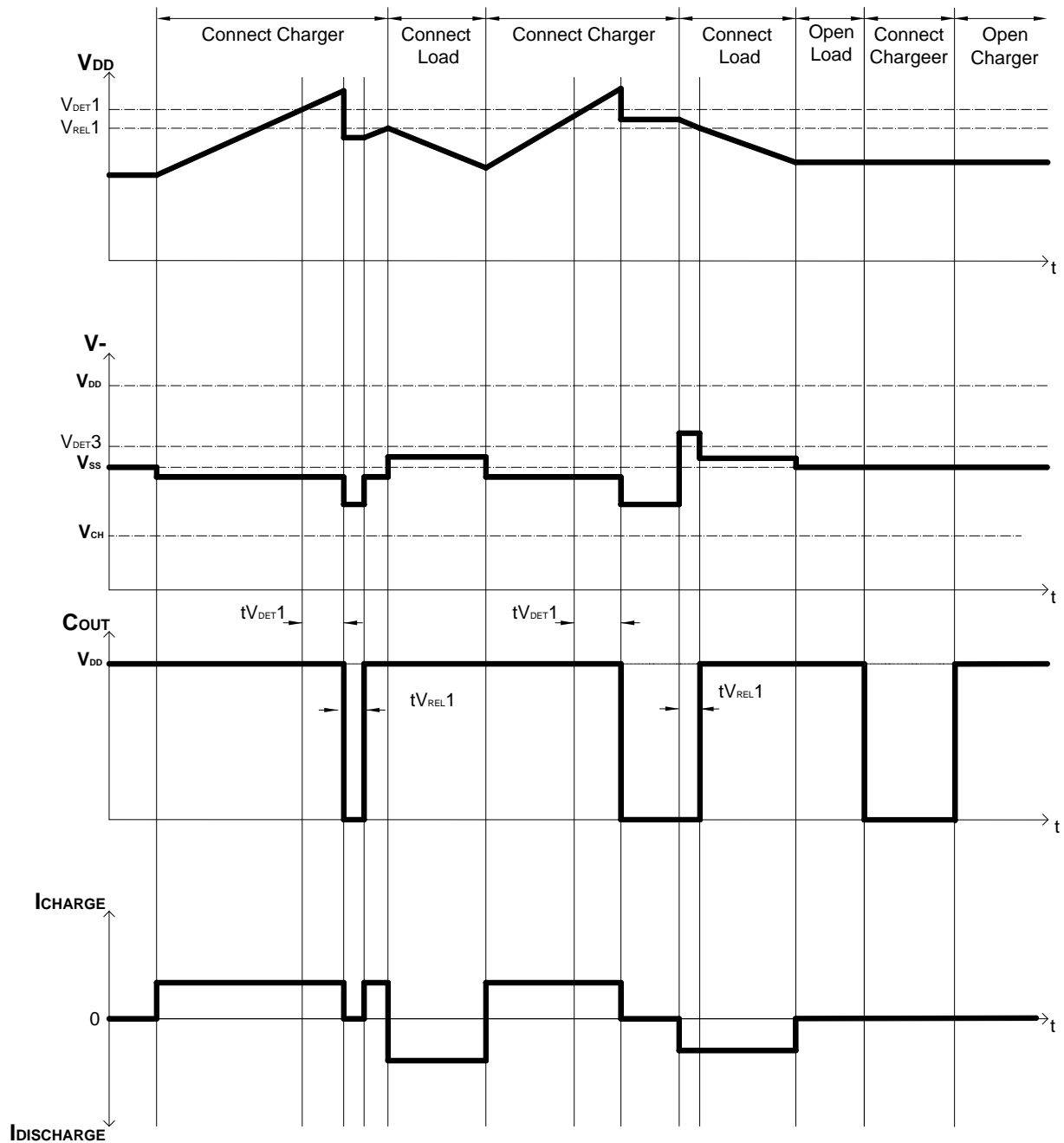
C2 and C3 capacitors have effect that the system stability about voltage ripple or imported noise. After check characteristics, decide that these capacitors should be inserted or not, where should be inserted, and capacitance value, please.

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■ Timing Chart

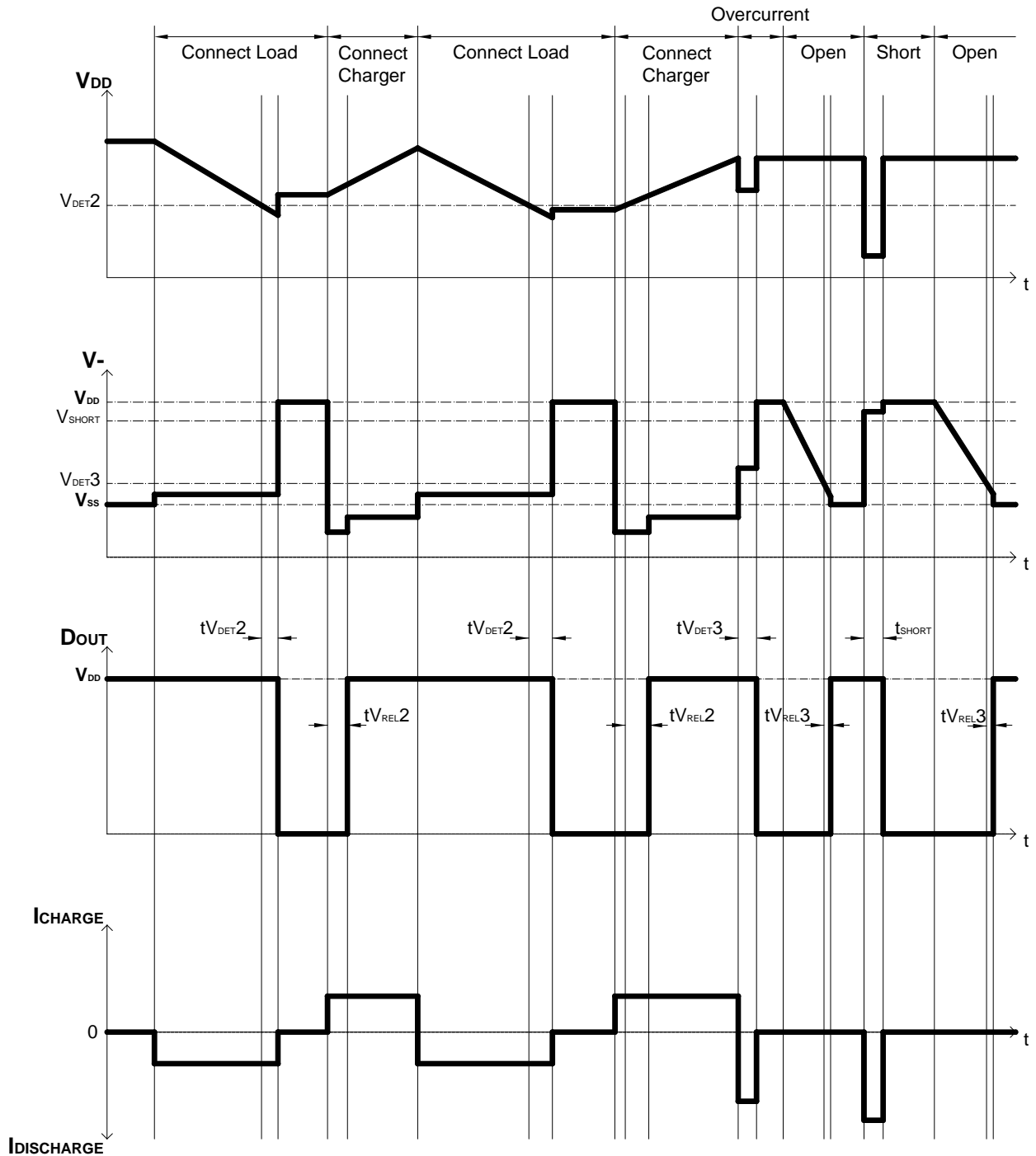
1. Overcharge, Overvoltage charger operations



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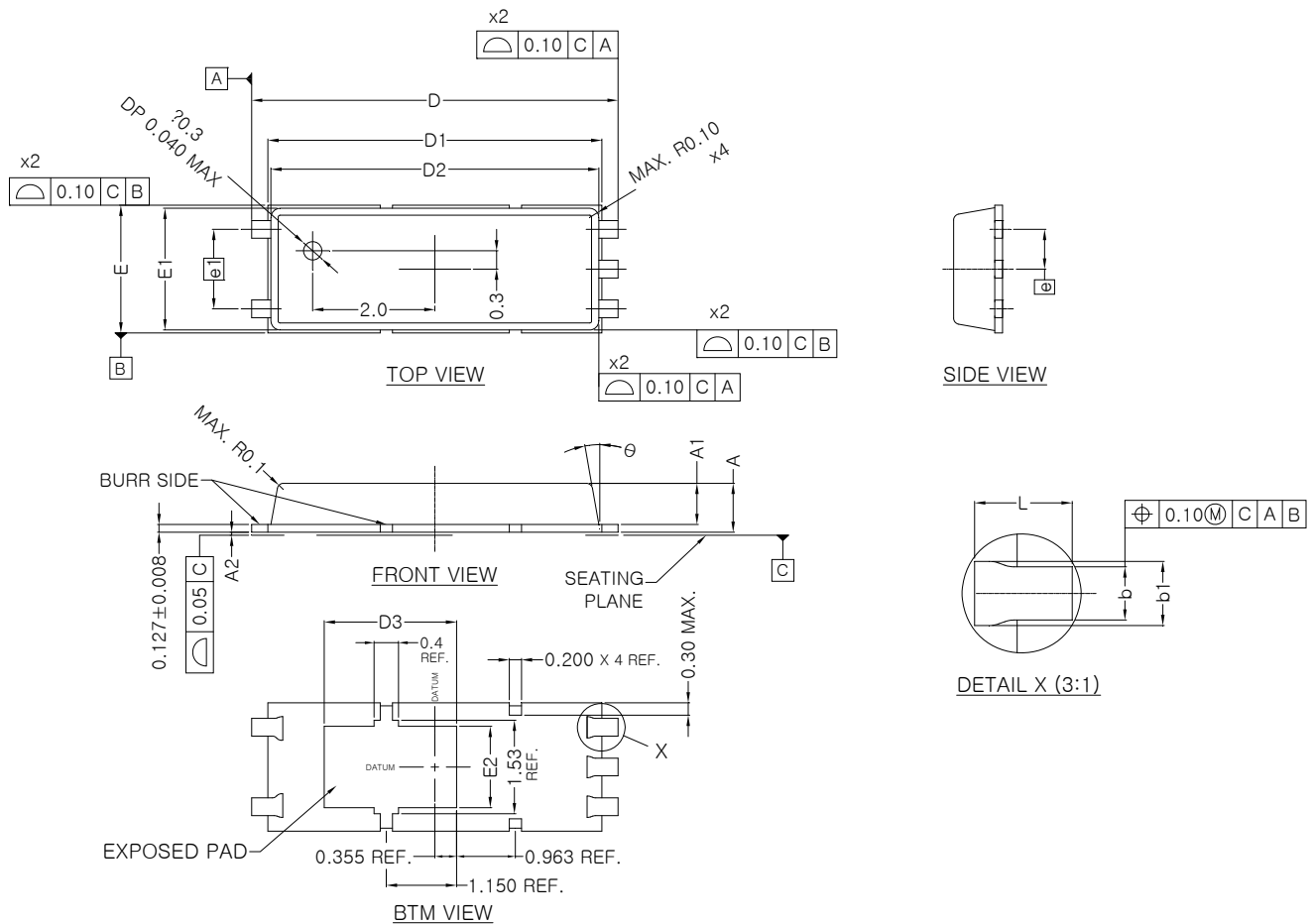
2. Overdischarge, Discharging Overcurrent and Short operations



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■ Package Description



SYMBOL	DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.750	0.800	0.850	
A1	0.623	0.673	0.723	
A2	—	—	0.050	
D	5.900	6.000	6.100	
D1	5.320	5.370	5.420	
D2	5.270	5.320	5.370	
D3	2.220 REF.			
E	2.000	2.100	2.200	
E1	1.950	2.000	2.050	
E2	1.330 REF.			
Θ	—	—	10 °	
e	0.650 BSC			
e 1	1.300 BSC			
L	0.410	—	—	
b	0.240	0.290	0.340	
b1	0.300	0.350	0.400	

NOTE

1. LEAD BURR : VERTICAL MAX 0.025
HORIZONTAL MAX 0.025
BURR SIDE : ALL TOP SIDE
2. MOLD BURR & FLASH : PACKAGE OUT LINE BURR MAX 0.100
EXPPOSED PAD FLASH MAX 0.200
3. PACKAGE WARPAGE MAX 0.025
4. LEAD AND EXPOSED PAD PLATING : PURE TIN
THICKNESS> 7.62~25.4um

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■ Marking Contents

