Change Summary

CHANGES

No.	Applicable Section	Description	Page(s)
1	Block Diagram, Application Circuit	CHG and DSG swapped in block diagram and application circuit	2, 4
2	DC Characteristics	Removed ESD rating	5
3	Electrical Characteristics	FET driver circuit table changed from VAV to VCC; Also VBAT1 changed to VCC	7
4	Register Information	VAV changed to VCC	15
5	Register Information	Reg. 0Dh address change to Reg.0Eh	15
6	Application	Precharge FET Mode changed to External Precharge FET Mode	20, 21
7	Application	FET precharge Mode changed to Main FET precharge Mode	20, 21
8	SBS Register Function	The word “big” changed to “bit”	23
9	Application Circuit	Removed the secondary protection IC MM1373	4
10	Pin description	TCLK pin changed from I/O to I (input only)	3
11	Electrical characteristics	V_{OH} changed from V3V – 0.5 to V3V – 0.7 Removed PBI pin from driving capability table Changed PBO driving capability from 4mA to 1mA	5
12	Functional description	Added related Control Register to the function description Changed “battery pole” to “battery terminal”	9, 11
13	Register Information	Added Control Register map	12 – 22
14	Register Information	Added Internal register access methodology	31

REVISION HISTORY

Revision No.	Description of change	Release Date
0.5	Initial release	01/20/05
0.51	Change items 1 to 8	01/31/05
0.60	Change items 9 to 14	09/09/05

SBS Compliant Battery Gauge and Protection IC

FEATURES

- Single chip LiIon and Li-Polymer Battery Management
- Fully integrated high accuracy battery gauge with protection function for 3 and 4 cell Li-Ion and Li-Polymer batteries
- Smart Battery Specification (SBS) v 1.1 compliant
- Measures charge/discharge current with a dedicated 16-bit ADC:
  - Resolution down to 0.14nVhr
  - Auto Calibration to improve accuracy
- Monitors individual cell voltages and terminal voltage, with resolution of up to 15-bit.
- Integrated cell balancing circuits
- Integrated temperature sensor
- Multiple uncommitted 16 bit ADC channels available for custom applications
- Integrated Cell Protection includes:
  - Over voltage Protection
  - Under voltage Protection
  - Over current Protection
  - Short circuit Protection
- Embedded flash program and data storage allows flexible support of changing battery characteristics.
- Integrated 3.3V and 2.5V voltage regulators
- Integrated Charge and Discharge FET drivers
- Integrated patent pending *Trickle Driver* allows the main charge FET to perform current limited precharge without additional components
- Single 48 pin QFN package

APPLICATIONS

- Notebook computer battery packs
- Portable Devices
- Test equipment

GENERAL DESCRIPTION

OZ930 is a highly integrated SBS v1.1 compliant gas gauge and protection IC that measures the general state of health of a Li-Ion or Li-Polymer battery pack and its individual cells through a highly accurate, low power, battery gauge function. The measured voltage, current, temperature and capacity along with other essential parameters are then reported to the SMBus host and/or Smart Battery charger via the SMBus protocol

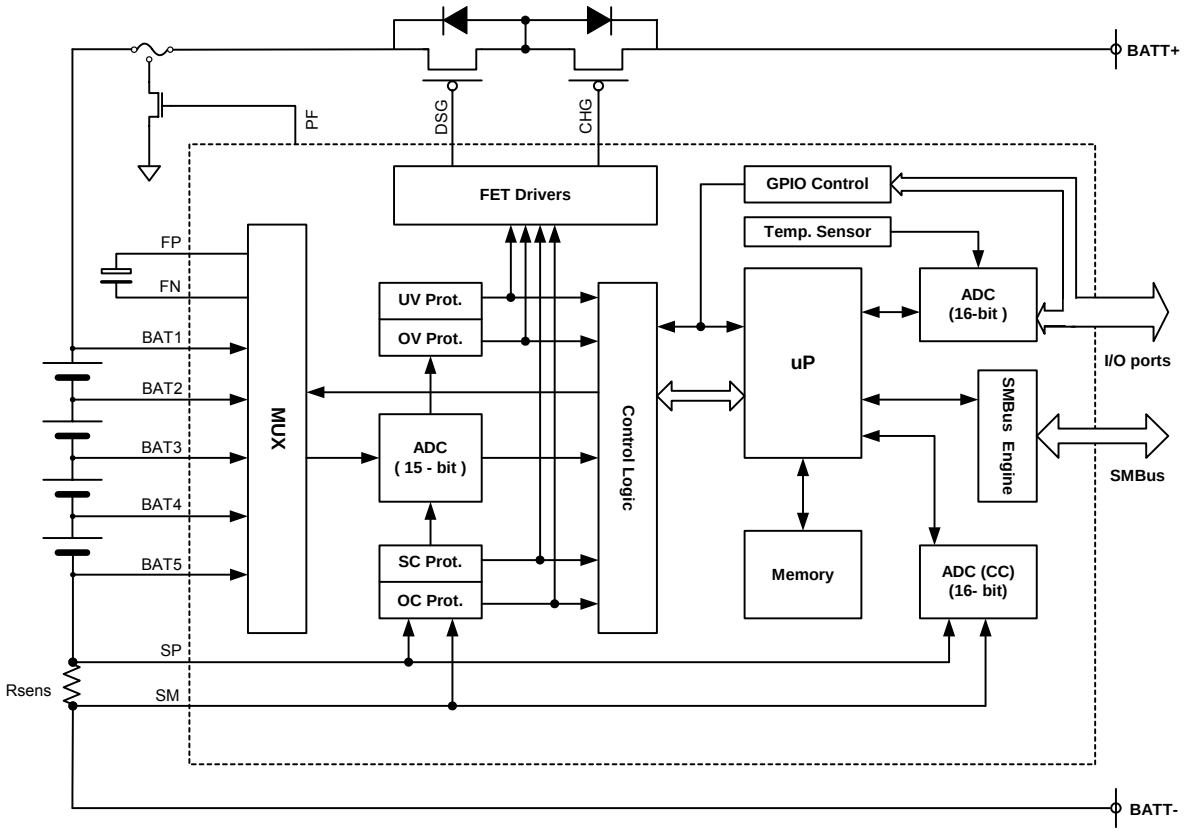
The Battery Gauge Software (BGS) calibrates itself automatically and continuously without waiting for a full charge and discharge cycle to occur, significantly increasing the reliability and accuracy of the battery pack.

The integrated digital Battery Protection Engine (BPE) works independently of the BGS to constantly monitor each cell to provide over-current, short circuit, over-voltage, and under-voltage safety protection. Working with embedded FET driver circuits, the protection circuit will independently shut off the FETs if necessary. If shutting off the FETs fails to resolve the protection condition, the BPE can then automatically assert the Permanent Fail (PF) signal to blow an external fuse. All over-current, short-circuit, over-voltage and under-voltage thresholds and their related delay times are register programmable for different battery types and manufacturers.

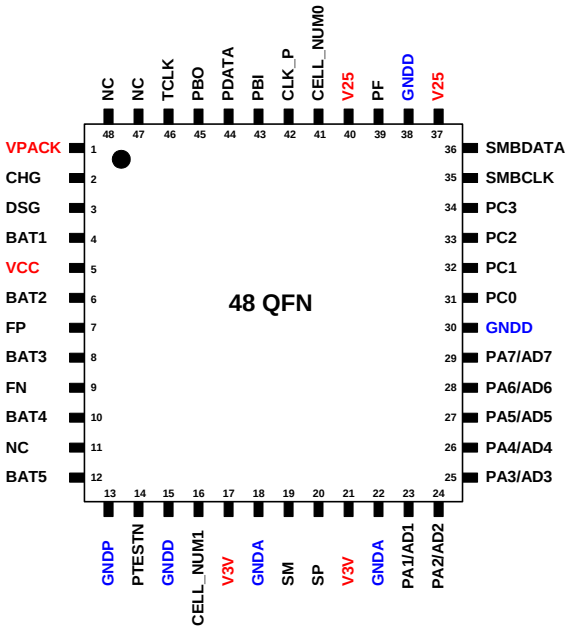
The integrated cell balancing circuits perform cell balancing during charge state under the control of BGS. Longer battery pack life can be achieved.

OZ930 supports the SBS Data Specification v1.1 (See section on *SBS v1.1 Functions* for detailed information) and can be easily modified to support additional optional manufacturer functions, protocol extensions, and gauge functionality.

BLOCK DIAGRAM



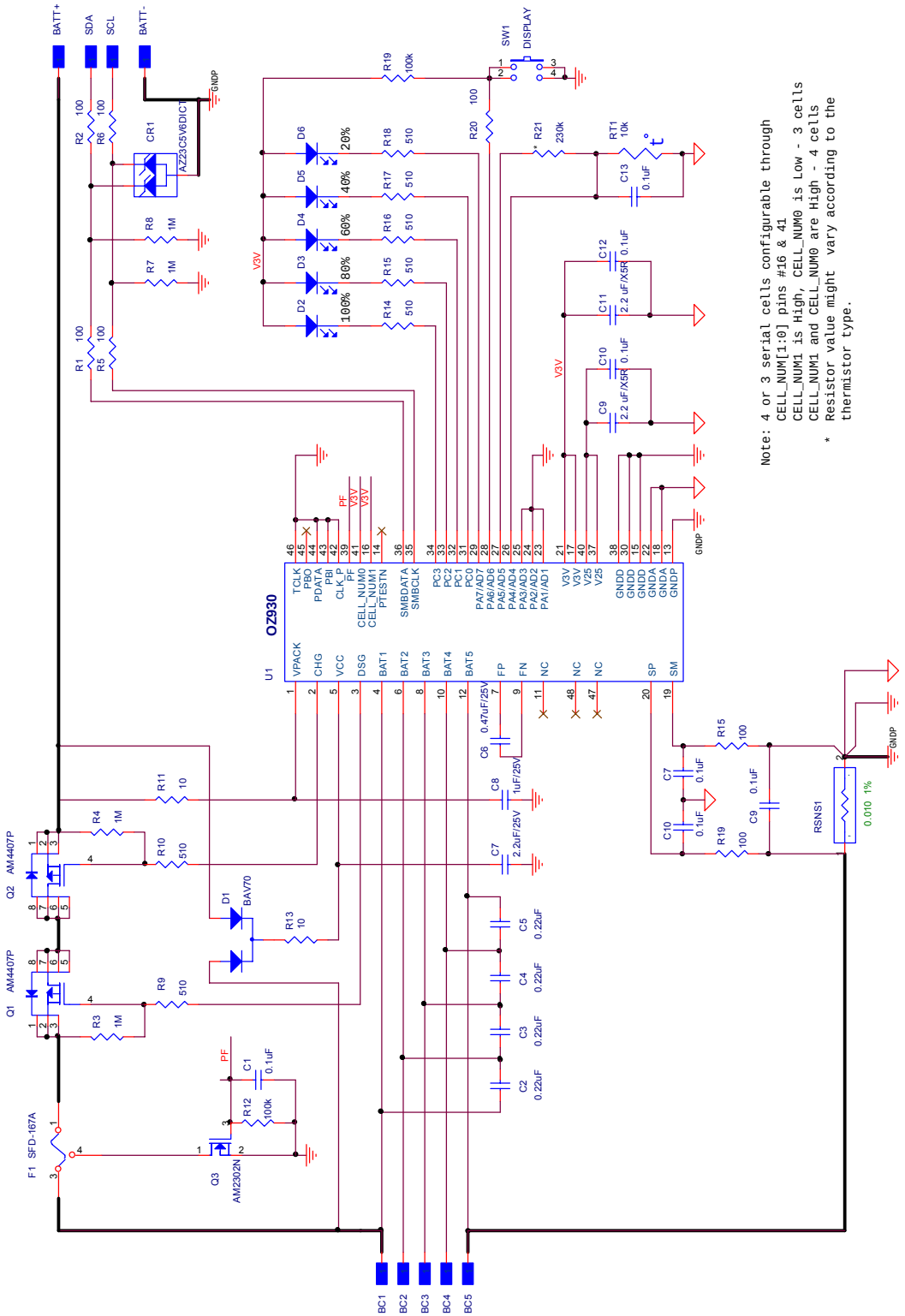
PIN DIAGRAM



PIN DESCRIPTION

No.	Name	I/O	Type	Description
1	VPACK	I	HV	Pack positive terminal or external power source
2	CHG	O	HV	Charge FET control. Active low.
3	DSG	O	HV	Discharge FET control. Active low.
4	BAT1	I	Analog	Connect to most positive cell (cell 1) plus pole. Short to BAT2 in 3-cell case.
5	VCC	I	HV	High voltage input either from battery (BAT1) or VPACK. Primary power supply for the chip.
6	BAT2	I	Analog	Connect to cell 1 negative pole.
7	FP	I/O	Analog	Positive of the sampling capacitor.
8	BAT3	I	Analog	Connect to cell 2 negative pole.
9	FN	I/O	Analog	Negative of the sampling capacitor.
10	BAT4	I	Analog	Connect to cell 3 negative pole.
12	BAT5	I	Analog	Connect to cell 4 negative pole.
13	GNDP	GND	Ground	Power ground.
14	PTESTN	I	Digital	Test pin. Leave floating.
15	GNDD	GND	Ground	Digital ground.
16	CELL_NUM1	I	Digital	4- or 3-cell select pin. Together with CELL_NUM0. CELL_NUM1:0 = 10 → 3-cell pack CELL_NUM1:0 = 11 → 4-cell pack
17	V3V	Power	Power	Internal 3.3V LDO output
18	GNDA	GND	Ground	Analog ground
19	SM	I	Analog	External small sense resistor negative terminal
20	SP	I	Analog	External small sense resistor positive terminal
21	V3V	Power	Power	3.3V power supply, short with Pin 17.
22	GNDA	GND	Ground	Analog ground
23	PA1/AD1	I/O	Ana/Dig	Port A.1 GPIO / ADC channel 1 input pin
24	PA2/AD2	I/O	Ana/Dig	Port A.2 GPIO / ADC channel 2 input pin
25	PA3/AD3	I/O	Ana/Dig	Port A.3 GPIO / ADC channel 3 input pin
26	PA4/AD4	I/O	Ana/Dig	Port A.4 GPIO / ADC channel 4 input pin
27	PA5/AD5	I/O	Ana/Dig	Port A.5 GPIO / ADC channel 5 input pin
28	PA6/AD6	I/O	Ana/Dig	Port A.6 GPIO / ADC channel 6 input pin
29	PA7/AD7	I/O	Ana/Dig	Port A.7 GPIO / ADC channel 7 input pin
30	GNDD	GND	Ground	Digital ground
31	PC0	I/O	Digital	Port C.0 GPIO
32	PC1	I/O	Digital	Port C.1 GPIO
33	PC2	I/O	Digital	Port C.2 GPIO
34	PC3	I/O	Digital	Port C.3 GPIO
35	SMBCLK	I/O	Digital	SMBus clock
36	SMBDATA	I/O	Digital	SMBus data
37	V25	Power	Power	2.5V power supply, short with Pin 40.
38	GNDD	GND	Ground	Digital Ground
39	PF	O	Digital	Permanent failure output. Active high. Should have a 5k ~ 10k ohm pull down resistor.
40	V25	Power	Power	Internal 2.5V LDO output
41	CELL_NUM0	I	Digital	4- or 3-cell select pin. Together with CELL_NUM1. CELL_NUM1:0 = 10 → 3-cell pack CELL_NUM1:0 = 11 → 4-cell pack
42	CLK_P	I	Digital	Test pin. Tie to ground.
43	PBI	I	Digital	Port B digital input pin.
44	PDATA	I/O	Digital	Test pin. Leave floating.
45	PBO	O	Digital	Port B digital output pin.
46	TCLK	I	Digital	Test pin. Tie to ground.
47	NC			No Connection.
48	NC			No Connection.

APPLICATION DIAGRAM



DC CHARACTERISTICS

Absolute Maximum Ratings

Supply voltage range	VCC, V PACK	-0.5V to 30V
Input voltage range	BAT1, BAT2, BAT3, BAT4, FP, FN	-0.5V to 30V
	BAT5, SM, SP	-0.5V to 0.5V
	BAT1 to BAT2, BAT2 to BAT3, BAT3 to BAT4, BAT4 to BAT5	-0.5V to 6V
	All other input pins	-0.5V to V3V + 0.3V
Output voltage range	DSG, CHG	-0.5V to VCC
	All other output pins	-0.5V to 6V
Operating free-air temperature range, TA		-20 °C to 70 °C
Storage temperature range, Tstg		-55 °C to 150 °C
Lead temperature (soldering, 10 sec)		300 °C

Note 1: All voltages are with respect to ground of this device except BATn – BAT(n+1), where n = 1,2,3,4 cell voltage
Note 2: Ground refers to common node of GNDA, GNDD, GNDP

Electrical Characteristics

Power supply

Parameter	Test Conditions	MIN	TYP	MAX	Unit
Supply voltage (VPACK or VCC)		6.6		25	V
3.3V regulator output voltage	V3V output voltage	3.0	3.3	3.6	V
2.5V regulator output voltage	V25 output voltage	2.25	2.5	2.75	V
Power on reset voltage			1.9		V
Supply Current	Normal mode; no load at V3V, V25, no flash programming(1)		750 *		µA
	Sleep mode (2)		65 *		µA
	Ship mode (3)		1 *		µA

Note 1: The exact power consumption number depends on the current, cell voltage data acquisition frequency.
Note 2: uP, Coulomb counter halted, Charge FET & Discharge FET off. Over-current & short-circuit detector off.
Note 3: Charger-on-wakeup active. All others are off.

General purpose digital inputs and outputs

Parameter	Test Conditions	MIN	TYP	MAX	Unit
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{OH} Output voltage high	Iload = -0.5mA	V3V – 0.7			V
V_{OL} Output voltage low	Iload = 0.5mA			0.4	V
Current drive capability	PC0 ~ PC3		8		mA
	PA1 ~ PA7		4		mA
	PBO		1		mA

Charger-on-wakeup

Parameter	Test Conditions	MIN	TYP	MAX	Unit
External charger wakeup IC voltage (Applied to VPACK)	VCC = 16V		5		V
	VCC = 6.6V	2			V

* Estimated value, final data TBD

Power-on-reset [1]

Parameter	Test Conditions	MIN	TYP	MAX	Unit
V25 voltage threshold	2.5V regulator output voltage decreasing		1.9		V
Hysteresis			100		mV

Note 1: Power-on-reset circuit monitors the 2.5V regulator output voltage. If the V25 output is lower than the threshold, it will generate a reset signal to the whole chip.

3.3V Regulator

Parameter	Test Conditions	MIN	TYP	MAX	Unit
Regulator output voltage	Io < 30mA		3.3		V
Line regulation	5.5V ≤ VCC ≤ 20V, Io = 20mA		10 *		mV
Load regulation	0.1mA ≤ Io ≤ 30mA, VCC = 12V		80 *		mV

2.5V Regulator

Parameter	Test Conditions	MIN	TYP	MAX	Unit
Regulator output voltage	Io < 30mA		2.5		V
Line regulation	5.5 V ≤ VDD ≤ 20V, Io = 20mA		10 *		mV
Load regulation	0.1mA ≤ Io ≤ 30mA, VCC = 12V		120 *		mV

Cell Voltage Monitor ADC (Referred to as Voltage ADC)

Parameter	Test Conditions	MIN	TYP	MAX	Unit
Input voltage range		-0.3		4.8	V
Resolution[1]		10		15	Bit
Conversion Time[1]	Single conversion	7.8125		250	ms

Note 1: Resolution is selectable by register setup. The higher the resolution, the longer the conversion time.

Coulomb counter (Referred to as Coulomb Counting ADC or ADC1)

Parameter	Test Conditions	MIN	TYP	MAX	Unit
Input voltage range		-256		256	mV
Resolution			16		Bit
Conversion Time	Single conversion	62.5		32000	ms
Offset error[1]			1		μV

Note 1: After calibration

Multi-channel ADC[1] (Referred to as ADC2)

Parameter	Test Conditions	MIN	TYP	MAX	Unit
Input voltage range		-300		1024	mV
Resolution[2]		11		16	Bit
Conversion Time[2]	Single conversion	1.953		62.5	ms

Note 1: Each channel is selectable by register setup.
Note 2: Resolution is selectable by register setup. The higher the resolution, the longer is the conversion time.

Internal Oscillator[1]

Parameter	Test Conditions	MIN	TYP	MAX	Unit
Frequency error from 256kHz	TA = 0°C to 75°C	-1%	±0.5%	+1%	

Note 1: Internal digital circuit is running at 256kHz frequency

Over-current (OC) and Short-circuit (SC) Detection[1]

Parameter	Test Conditions		MIN	TYP	MAX	Unit
OC detection threshold range[2]	Charge		50		180	mV
	Discharge		-50		-180	mV
OC detection threshold program step[2]	Charge			5		mV
	Discharge			-5		mV
SC detection threshold range[3]	Discharge		80		405	mV
SC detection threshold program step[3]	Discharge			25		mV
OC detection threshold accuracy	Charge and discharge	Voc = 50 mV (min)	TBD	50	TBD	mV
		Voc = 100 mV	TBD	100	TBD	mV
		Voc = 180 mV (max)	TBD	180	TBD	mV
SC detection threshold accuracy	Discharge	Vsc = 100 mV (min)	TBD	100	TBD	mV
		Vsc = 200 mV	TBD	200	TBD	mV
		Vsc = 405 mV (max)	TBD	405	TBD	mV

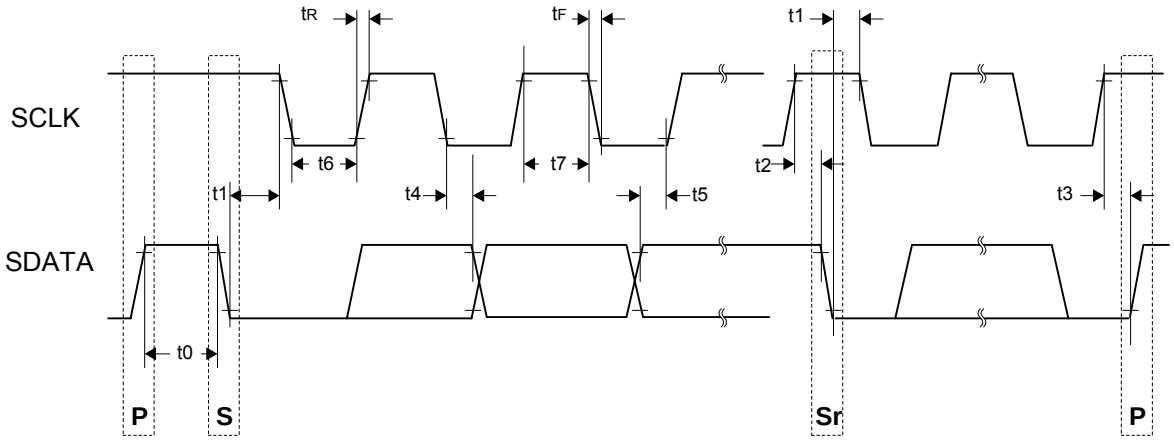
Note 1: The actual current threshold = the relative voltage threshold / Rsens
Note 2: The OC detection threshold is adjusted by a 5-bit register
Note 3: The SC detection threshold is adjusted by a 4-bit register

FET Driver Circuit

Parameter	Test Conditions	MIN	TYP	MAX	Unit
CHG high level	Charge FET off		VCC		V
CHG low level	Charge FET on		VCC – 9		V
DSG high level	Discharge FET off		VCC		V
DSG low level	Discharge FET on		VCC – 9		V
Rise time	C_L = 5000 pF, 10% to 90%		5	TBD	µs
Fall time	C_L = 5000 pF, 90% to 10%		5	TBD	µs

AC TIMING

SMBus Timing



Symbol	Parameter	Limits		Units	Note
		Min	Max		
FSMB	SMBus Operating Frequency	10	100	KHz	
t0	Bus free time between Stop and Start condition	4.7	-	µs	
t1	Hold time after (Repeated) Start condition. After this period, the first clock is generated	4.0	-	µs	
t2	Repeated Start condition set up time	4.7	--	µs	
t3	Stop Condition setup time	4.0	-	µs	
t4	Data hold time	150	-	ns	
t5	Data setup time	250	-	ns	
TIMOUT		25	35	ms	See **Note 1**
t6	Clock low period	4.7	-	µs	
t7	Clock high period	4.0	50	µs	See **Note 2**
TLOW:SEXT	Cumulative clock low extend time (slave device)	-	25	ms	See **Note 3**
TLOW:MEXT	Cumulative clock low extend time (master dvice)	-	10	ms	See **Note 4**
tF	Clock/Data Fall time	-	300	ns	See **Note 5**
tR	Clock/Data Rise Time	-	1000	ns	See **Note 5**

Note 1: A device will timeout when any clock low exceeds this value
Note 2: t5 Max provides a simple guaranteed method for devices to detect bus idle conditions.
Note 3: TLOW:SEXT is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to the stop. If a slave device exceeds this time, it is expected to release both its clock and data lines and reset itself.
Note 4: TLOW:MEXT is the cumulative time a master device is allowed to extend its clock cycles within one byte of a message as defined from start-to-ack, ack-to-ack, or ack-to-stop.
Note 5: Rise and Fall times are measured between 10% to 90% of the signal amplitude.

FUNCTIONAL DESCRIPTION

General Operation

OZ930 constantly measures the state of health of a battery pack, including the charge/discharge current, each individual cell voltage, and the temperature of the pack. The Battery Gauge Software (BGS) combines this measured data with calculated corrections for self discharge, capacity loss, and other second order effects to compute the true capacity of the battery pack.

OZ930 also protects the battery pack from over charging, over discharging, and over heating by setting various protection thresholds including over-voltage, under-voltage, over-current, short-circuit current thresholds and relative delay timers and over-temperature limits.

To support non-balanced or slightly off balanced battery cells in a pack, integrated cell balancing circuits optionally allows each cell to be balanced effectively during both the charging and idle status.

Measurements

OZ930 includes three independent analog to digital converters: (ADCs)

i. Current

OZ930 has a dedicated 16-bit sigma-delta ADC (ADC1) for Coulomb counting measurements of the current across a sense resistor (1mΩ to 50mΩ), pin 19 and 20, during charging and discharging of a battery pack. The resolution of the coulomb counter is 0.14nVh, with an input voltage range of –256mV to +256mV. The measurement period is programmable from 62.5ms to 32 seconds. The current ADC can be controlled by Internal Control Register 10h ~ 15h.

ii. Voltage

Cell voltages are measured by an 11 to 15 bit cell voltage ADC, which is shared by both the BPE (Battery Protection Engine) and the BGS (Battery Gauge Software). The BPE reads each cell voltage sequentially with 10-bit resolution for over-voltage (OV) and under-voltage (UV) checking. The protection circuit scan rate may be programmed from 250ms to 32 seconds. The BGS also uses the cell voltage ADC to monitor cell voltages, using 11 to 15 bit resolution. The voltage ADC is controlled by Protection register 12h ~ 14h.

iii. Multi-channel ADC

OZ930 includes a third general purpose 16-bit ADC (ADC2) with 8-channel multiplexer for temperature measurement and functional extensions. Channel 0 is fixed for internal temperature sensor. Channel 1 to 7 (pin PA1 ~ PA7) can be configured by BGS (Battery Gauge Software) through internal Control Register. All channels of this ADC resolution also can be configured from 11-bit to 16-bit for different applications by Internal Control Register 18h ~ 1Ch.

Temperature

OZ930 includes a temperature sensor, which can monitor the die temperature from –20 °C to 120°C. This internal temperature sensor is accessible through Multi-channel ADC (ADC2) channel 0. External or battery pack temperature also can be monitored by using an external thermistor. Temperature measurements are used for thermal protection and battery capacity compensation.

Computing Capacity

With coulomb counting, the amount of charges added to or removed from the battery pack can be properly accounted for. However, calibration is necessary to continually re-adjust the battery gauge to the proper reference point. Calibration is performed automatically when necessary.

The self-discharge rate of a rechargeable battery depends on the capacity and the temperature of the battery. This factor is taken into account when computing the overall capacity of the battery pack.

Protection Circuits

OZ930 includes a digital Battery Protection Engine (BPE), which operates independently from the Battery Gauge Software (BGS). The BPE constantly monitors data from the protection ADC and other circuits described below. If a protection error condition is detected and persists, the BPE will force the charge and/or discharge FET off. If the protection error condition still persists, the BPE will assert the Permanent Fail (PF) signal to instruct an optional external fuse circuit to permanently disable the battery.

i. Over-current (OC)

OZ930 includes an independent hardware over-current detector (separate from the Coulomb counting ADC) that monitors the sense resistor to detect over-current in either charge or discharge. If the over-current condition continues for a programmable delay, the protection circuit will turn off the charge or discharge FET, depending on direction of current flow. The charge and discharge over-current thresholds are set in Protection register 06h and 07h:

ChargeOC: 50mV (default) to 180mV, 5mV steps.
DischargeOC: -50mV(default) to -180mv, -5mV steps

The over-current delay allows the system to momentarily accept a high current condition. The default OC delay is 500ms. This delay time can be programmed from 250ms to 4 seconds in 250ms steps in Protection register 04h. Charge and discharge OC share the same delay time.

ii. Short circuit (SC)

Short circuit detection is very similar to over-current detection but only applies to discharge. When short circuit condition is detected, OZ930 will turn off both charge FET and discharge FET. Short circuit threshold can be programmed from 80mV to 405mV in 25mV steps in Protection register 06h. Short circuit delay time can be programmed from 31.25us to 64ms with 250us as default. The Short circuit delay time is configured by Protection register 03h.

iii. Over-voltage (OV)

The protection engine performs over-voltage detection by comparing 10 bit values from the protection ADC to an OV threshold, which is programmable from 2.4V to 4.79V in 9.375mV steps. The default is 4.2V. The threshold is setup in Protection register 01h. When over-voltage condition is detected, OZ930 will turn off the charge FET after a delay time. This delay time is programmed in Protection register 04h as a multiple of the ADC scan cell voltage rate. Default value equals to 2.

iv. Under-voltage (UV)

Under-voltage detection operates in the same way as over-voltage detection. Its threshold varies from 1.8V to 4.19V in 9.375mV steps. The default value is 3.0V. The threshold is setup in Protection register 02h.
Under-voltage protection has the same delay time as the over-voltage protection.

The above mentioned OC, SC, OV and UV protection each has an independent hardware circuit, and does not rely on Battery Gauge Software (BGS). Normally, BGS also has those protection functions and their relative thresholds are lower, so Battery Gauge OC, SC, OV and UV protections act as the first level protection. The OC, SC, OV and UV protection circuits in the BPE (Battery Protection Engine) act as a second level protection.

v. Thermal protection

Thermal protection is performed by the BGS, based on inputs from both the internal temperature sensor and the (optional) external temperature sensor. Thermal information may be used to temporarily interrupt the charge cycle, or to disable discharge, or even assert PF in the case of extreme sustained over temperature

Charge and Discharge FET Control

The charge and discharge FET enables are controlled by the Battery Gauge Software (BGS) through Protection register 0Ch, subject to override by the Battery Protection Engine (BPE). The charge (CHG) FET and discharge (DSG) FET drive gate-to-source voltage is clamped to 9V (typical). The default state of the FET drive is off. The charge FET employs the Trickle Driver circuit (patent pending). When cell voltage is below a threshold, such as 2.4V, the BGS can program the Trickle Driver to enter trickle charge (pre-charge) mode. In this mode, the charge FET gate-to-source voltage is not clamped to 9V but to a much smaller programmable value. This way, the charge FET acts as a variable resistor to control the trickle charge current. Trickle charge current can be programmed from 10mA to 150mA by Protection registers 10h and 11h. When cell voltage exceeds the trickle charge threshold, the BGS will program the Trickle Driver back to normal charge mode and the charge FET gate-to-source voltage will be clamped to 9V. The detail information about trickle charge will be described in “0-V Precharge Support” section.

Power Management

OZ930’s modular and register programmable design makes it very flexible for power management. The Coulomb Counting ADC’s conversion rate can be programmed from 62.5ms to 32 seconds. The slower the rate, the more power will be saved. When the battery is being charged or discharged, the conversion rate should be fast to get more accurate capacity information. When battery is idle or out of the system, the conversion rate can be set slower. Both the resolution and scan rate of the cell voltage ADC are programmable, and are varied dynamically by the BGS depending upon battery status. The general purpose ADC is only powered on when the BGS requests a conversion: when the conversion is finished, it automatically powers off. The OC and SC detector and FET drivers can be independently turned off to save power

SMBus Communication

OZ930 has an SBS v1.1 compatible SMBus port to communicate with the SMBus host and charger. In this way a system can efficiently monitor and manage the battery. The SMBus interface is a command-based protocol. A processor acting as the bus master initiates a communication to OZ930 by generating a start condition. A start condition consists of a high-to-low transition of the SMBDATA line while the SMBCLK is high. The processor completes the access with a stop condition. A stop condition consists of a low-to-high transition of the SMBDATA

line while the SMBCLK is high. With SMBus, the most-significant bit (MSB) of a data byte is transmitted first. In some instances, OZ930 acts as the bus master. This occurs when OZ930 broadcasts charging requirements and alarm conditions to device addresses 0x12 (SBS Smart Charger) and 0x10 (SBS Host Controller).

OZ930 supports the following SMBus protocols:

- Read Word
- Write Word
- Block read

A processor acting as the bus master uses the three protocols to communicate with OZ930. The OZ930 acting as the bus master, uses the write word protocol. The SMBDATA and SMBCLK pins are open drain and require external pull-up resistors. OZ930 supports packet error checking (PEC) as a mechanism to confirm proper communication between it and another SMBus device. Packet error checking requires that both the transmitter and receiver calculate a packet error code (PEC) for each communication message. The device that supplies the last byte in the communication message appends the PEC to the message. The receiver compares the transmitted PEC to its PEC results to determine if there is a communication error.

LEDs

OZ930 has 11 GPIO pins (PA1 ~ PA7, PC0 ~ PC3) that can be configured as LED drivers. Normally, 4 or 5 LEDs are used for bar-graph display, with each LED representing 25% or 20% capacity. The displayed remaining capacity can be relative or absolute based on customer's design requirements.

Note: During assembly, it is recommended to connect the cells in the following order: negative terminal of the 4th cell, BAT5; positive terminal of the 1st cell, BAT1; negative terminal of the 3rd cell, BAT4, negative terminal of the 2nd cell, BAT3; and negative terminal of the 1st cell, BAT2.

INTERNAL REGISTER INFORMATION

OZ930 has three sets of different internal registers:

- Control Register ---- for I/O ports, coulomb counting ADC, multi-channel ADC, EFlash memory control
- Protection register ---- for voltage ADC, hardware protection function control
- SBS v1.1 function register ---- for SBS v1.1 function support

CONTROL REGISTER MAP

OZ930 has 64 addressable Control Registers. These registers control coulomb counting ADC (ADC1), multi-channel ADC(ADC2), EFlash memory management, and SMBus communication, etc. OZ930 internal uP can directly access these Control Registers.

After reset, bits in Control Register are cleared to zeroes except as otherwise noted.

Control Register Address Range	Function Description
00h – 03h	Interrupt Control
04h – 07h	EFlash Erase Control
08h – 0Fh	Timers control
10h – 15h	ADC1 (Coulomb Counting ADC) related
16h – 17h	uP reset Control
18h – 1Ch	ADC2 (Multi-Channel ADC) related Control
1Dh	EFlash access security Control
1Eh – 20h	SMBus activities
21h – 27h	SBS v1.1 Function Access
28h – 2Ch	SMBus command support
2Dh – 2Fh	SMBus master support
30h – 37h	GPIO (PA1~PA7, PC0~PC3) Control
38h – 3Ah	Protection Register Access
3Bh	Chip ID/Version
3Ch – 3Eh	Hardware Configuration
3F	Permanent Fail Control

Note: All the registers in shadow are fully controlled by Battery Gauge Software (BGS), not accessible to the end user

Detailed Control Register information

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Enb GPIO in int.	Enb SMB cmd int.	Enb SBS Fun. Int.	Enb SMB active int.	Reserved		Enb ADC2 int.	Enb Timer int.
01h	GPIO in event	SMB cmd event	SBS Fun. Event	SMB active event	Reserved		ADC2 event	Timer event
02h	Enb EFlash fault int.	Enb I/O fault int.	Enb Memory fault int.	Reserved				Enb ADC1 int.
03h	EFlash fault event	I/O fault event	Memory fault event	Reserved				ADC1 event

Register 00h

Bit0 : Enable timer interrupt. (OZ930 has 4 hardware timers. Refer to Control Register 08h – 0Fh for more detailed information)
Bit1 : Enable ADC2 interrupt.
Bit3 – Bit2 : Reserved
Bit4 : Enable SMBus activity interrupt.
Bit5 : Enable SBS function interrupt
Bit6 : Enable SMBus command interrupt.
Bit7 : Enable GPIO input interrupt. Each GPIO input has its own enable bit in Control Register 32h and 33h, this bit serves as a global interrupt enable for all enabled GPIO input events.

Register 01h
- Bit0 : Timer event. This is a logical OR of all timer event bits in Control Register 0Fh.
- Bit1 : ADC2 event. Write "1" to clear. This event is set when an ADC2 read request is finished.
- Bit3 – Bit2 : Reserved
- Bit4 : SMBus activity event. This event is set whenever activity is detected on the SMBus.
- Bit5 : SBS Function event. This bit can be set based on SMBus reads/writes accessing SBS function registers. Refer Control Register 1Eh and 1Fh for more information.
- Bit6 : SMBus command event. Write "1" to clear.
- Bit7 : GPIO input event. This bit is a logical OR of all key event bits in Control Register 34h.

Register 02h
- Bit0 : Enable ADC1 interrupt.
- Bit4 – Bit1 : Reserved.
- Bit5 : Enable memory fault interrupt.
- Bit6 : Enable I/O fault interrupt.
- Bit7 : Enable EFlash fault interrupt.

Register 03h
- Bit0 : ADC1 timer event.
- Bit4 – Bit1 : Reserved.
- Bit5 : Memory fault event. This bit is set in response to any attempted access to a reserved area in the memory map.
- Bit6 : I/O fault event. This event is set when any Control Registers access is attempted when interrupts are enabled on the uP. In that case, the attempted Control Register access doesn't complete.
- Bit7 : EFlash fault event. This event is set when an EFlash access is attempted when uP interrupts are enabled, or when the access violates the limits set in Control Register 04h.

****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04h	Reserved							
05h	EFlash Page erase command (80h = erase information area, 81h = erase data)							
06h	EFlash page erase address, low byte							
07h	EFlash page erase address, high byte							

Register 04h
- Bit7 – Bit0: Reserved

Register 05h
- Bit7 – Bit0: EFlash Page erase command
  OZ930 embedded 64kByte EFlash, which has 128 byte information area and 128 pages with 512 byte/page.
  Command code 80h = erase EFlash 128 byte information area;
  Command code 81h = erase EFlash page
  Other command code is ignored for Control Register 05h

Register 06h
- Bit7 – Bit0: EFlash address (low byte) for page erase. EFlash address is 0000h – FFFFh.

Register 07h
- Bit7 – Bit0: EFlash address (high byte) for page erase. EFlash address is 0000h – FFFFh.

In order to erase EFlash page correctly, uP has to send the EFlash address to Control Register 06h & 07h first, then send the erase command to Control Register 05h. The EFlash page including the specified address will be erased.

****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h	Write reload	Read reload	Read timer	Reserved			Timer Select	
09h	Timer buffer (low byte)							

0Ah	Timer buffer (high byte)								
0Bh	Reset Enable	Reserved	Output Option		Reserved	Input Option			
0Ch	Reserved					Timebase			
0Dh	Start	Stop	Pause	Repeat	Reserved	Timer state			
0Eh	Reserved								
0Fh	Reserved				Timer 3 Event	Timer 2 Event	Timer 1 Event	Timer 0 Event	

OZ930 has four 16-bit internal hardware timers, Timer0 ~ Timer3. All timers will increment from 1 to the pre-defined "Reload" value if enabled. The timer with 0 in it means stopped (disabled). When the timer reach the reload value, it will generate an event or a reset signal (depends on the Control Register 0Bh, bit 7), after that, it will start again at 1 or stop at 0 (depends on Control Register 0Dh, bit 4).

Timer1, Timer2 and Timer3 also associated with two GPIO pins, one for input and one for output.

Timer	Input	Output
1	PA3	PA2
2	PA5	PA4
3	PA7	PA6

All the timers have different input mode and output mode. Refer to Control Register 0Bh for detail. All timers also can use different timebase for counting, determined by Control Register 0Ch.

Register 08h

Bit1 – Bit0 : Select timer.
- 00 = Timer0
- 01 = Timer1
- 10 = Timer2
- 11 = Timer3

Bit4 – Bit2 : Reserved

Bit5 : Set this bit will cause the selected timer count to be copied to the timer buffer (Control Register 09h & 0Ah).

Bit6 : Set this bit will cause the selected timer's reload value to be copied to the timer buffer.

Bit7 : Set this bit will cause the value in timer buffer to be written to the selected timer's reload latch as reload value.

Register 09h

Bit7 – Bit0 : Timer buffer low byte

Register 0Ah

Bit7 – Bit0 : Timer buffer high byte

Register 0Bh

Bit2 – Bit0 : Timer input option
- 000 = Software trigger, input pin has no effect.
- 001 = The same as 000.
- 010 = Trigger on low input. Start counting when input pin is low, continue counting regardless of the input until count is equal the reload value. Then reload or stop based on repeat bit (Control Register 0Dh, bit4)
- 011 = Trigger on high input. Start counting when input pin is high, continue counting regardless of the input until count is equal the reload value. Then reload or stop based on repeat bit (Control Register 0Dh, bit4)
- 100 = Trigger on the input falling edge. Start counting when the input is low, continue counting until the input goes high again, then stop and set the timer event. (Note: In this option, the reload value should set larger than the input pulse width, like FFFFh)
- 101 = Trigger on the input rising edge. Start counting when the input is high, continue counting until the input goes low again, then stop and set the timer event. (Note: In this option, the reload value should set larger than the input pulse width, like FFFFh)

110 = Trigger on the input falling edge. Start counting at the input falling edge, continue counting until the subsequent falling edge, then stop and set the timer event. (Note: In this option, the reload value should set larger than the input period, like FFFFh)
111 = Trigger on the input rising edge. Start counting at the input rising edge, continue counting until the subsequent rising edge, then stop and set the timer event. (Note: In this option, the reload value should set larger than the input period, like FFFFh)

Bit3 : Reserved
Bit5 – Bit4 : Timer output option
00 = No output
01 = Level output. When the timer start counting, the associated output pin goes high and will keep high until the timer stops. (Note: If the repeat bit is set, the output will keep high all the way, until the timer is forced to stop)
10 = Pulse output. The associated output pin will generate a pulse every time the timer event happens (either the timer equal the reload value or input pin changes the state). The pulse width depends on the timebase option, equals to one timebase clock period.
11 =Toggle output. The associated output pin will toggle every timer event.
Bit6 : Reserved
Bit7 : Reset enable. If this bit Is set, a timer event will cause uP reset instead of an event for interrupt. Using this function can implementing a deadman timer.

Register 0Ch
Bit2 – Bit0 : Timebase selection
000 = system clock /8 (256khz / 8 = 32khz)
001 = 16khz
010 = 1khz
011 = 32hz
100 = 1hz
101 = 1/32 hz
110 = ADC1 scan rate (16hz ~ 1/32 hz, dependent on Control Register 10h, bit3 – bit0).
111 = Input pin rising edge.
Bit7 – Bit3 : Reserved

Register 0Dh
Bit2 – Bit0 : Timer state. This give all relevant information about the timer's current condition.
000 = Idle, timer value is 0
001 = Timer stopped by input signal. The timer value is unchanged from its contents at the last significant ijnput pin event.
010 = Timer stopped by terminal count. The timer value equals the reload latch value.
011 = Timer stopped by software. The timer value is unchanged from the time software stopped it.
100 = Waiting for trigger. Timer value equals 0 and output is in normal state.
101 = Timer running.
110 = Reserved.
111 = Reserved.
Bit3 : Reserved
Bit4 : Repeat enable. When set, a running timer will start over at 1 after the timer value reaches its reload value. If this bit is not set, the timer stops counting after reach its reload value.
Bit5 : Pause. When set, timer incrementing is disabled, any input edges will not be noticed during pause.
Bit6 : Write a 1 to this bit will cause the timer to be stopped and the timer state set to 3'b011. The bit remains set during any timer delay before the timer actually stops.
Bit7 : Start or restart timer. If the timer is in a state less than 3'b100, writing a 1 to this bit will cause the timer goes to state 3'b100 or 3'b101 depending on input options and the state of the associated input pin. If the timer is in state 3'b101, writing a 1 to this bit will cause the timer to be restarted at 1, extending its period like a retriggerable one-shot. The bit remains set until the timer is actually started or restarted.

Register 0Eh
Bit7 – Bit0 : Reserved.

Register 0Fh
Bit0 : Timer0 event. Write a 1 to clear.
Bit1 : Timer1 event. Write a 1 to clear.
Bit2 : Timer2 event. Write a 1 to clear.

Bit3 : Timer3 event. Write a 1 to clear.
Bit7 – Bit4 : Reserved.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10h	ADC1 disable	Calibration	Reserved		ADC1 scan rate			
11h	Reserved							
12h	ADC1 result (Low Byte)							
13h	ADC1 result (High Byte)							
14h	Reserved							
15h	ADC1 cycle count (counts 1/16 second intervals since previous ADC1 timer event)							

Register 10h
Bit3 – Bit0 : ADC1 scan rate. The actual scan rate is $16/(2^N)$.
0000 = 16hz (convert every 62.5ms)
0001 = 8hz (convert every 125ms)
……
1001 = 1/32hz (convert every 32 seconds)
1010 ~ 1111 = reserved, no use.
Bit5 – Bit4 : Reserved.
Bit6 : Calibration. When this bit is set, ADC1 inputs are shorted together to make calibration readings for ADC1. Otherwise, ADC1 readings use the current sense resistor inputs.
Bit7 : ADC1 disable. When this bit is set, ADC1 is disabled to save power. But the ADC1 timer event (Control Register 03h bit0) will continue at the programmed scan rate.

Register 11h
Bit7 – Bit0 : Reserved.

Register 12h
Bit7 – Bit0: ADC1 result (low byte). The value remains valid after each reading until the next reading completes.

Register 13h
Bit7 – Bit0: ADC1 result (high byte). The value remains valid after each reading until the next reading completes.

Register 14h
Bit7 – Bit0 : Reserved.

Register 15h
Bit7 – Bit0 : Count indicates numbers of 1/16 seconds (62.5ms) intervals since the previous ADC1 timer event. This time interval is used for Coulomb counting calculation.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
16h	Reserved							
17h	SMBus reset	Reserved	Scratchpad register					

Register 16h
Bit7 – Bit0 : Reserved

Register 17h
Bit5 – Bit0 : Scratchpad register. Can be used as temporary register to store some intermediate results.
Bit6 : Reserved
Bit7 : SMBus reset. High to indicate the most recent reset was caused by a command from SMBus.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
18h	ADC2 voltage source selection				Reserved	ADC2 resolution		
19h	Reserved							

1Ah	ADC2 result (Low Byte)
1Bh	ADC2 result (High Byte)
1Ch	Reserved

Register 18h
Bit2 – Bit0 : ADC2 resolution select.
000 = 11-bit
001 = 12-bit
……
101 = 16-bit
110 ~ 111 = reserved, no use.
Bit3 : Reserved.
Bit7 – Bit4 : ADC2 voltage source selection. Any write to this register requests an ADC2 conversion.
0000 = Internal temperature sensor
0001 = PA1 input (PA1 has to be configured as analog pin. Refer to Control Register 30h ~ 37h)
0010 = PA2 input (PA2 has to be configured as analog pin. Refer to Control Register 30h ~ 37h)
0011 = PA3 input (PA3 has to be configured as analog pin. Refer to Control Register 30h ~ 37h)
0100 = PA4 input (PA4 has to be configured as analog pin. Refer to Control Register 30h ~ 37h)
0101 = PA5 input (PA5 has to be configured as analog pin. Refer to Control Register 30h ~ 37h)
0110 = PA6 input (PA6 has to be configured as analog pin. Refer to Control Register 30h ~ 37h)
0111 = PA7 input (PA7 has to be configured as analog pin. Refer to Control Register 30h ~ 37h)
1000 = Inputs shorted for calibration
1001 ~ 1111 = Reserved.

Register 19h
Bit7 – Bit0 : Reserved.

Register 1Ah
Bit7 – Bit0: ADC2 result (low byte). The value remains valid after each reading until the next reading completes. The results are always left justified, with 0's appended to the lower bit as needed.

Register 1Bh
Bit7 – Bit0: ADC2 result (high byte). The value remains valid after each reading until the next reading completes. The results are always left justified, with 0's appended to the lower bit as needed.

Register 1Ch
Bit7 – Bit0 : Reserved.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1Dh	Disable EFlash Write	Enable EFlash Write	Disable EFlash Read	Enable EFlash Read	Reserved			

Register 1Dh
Bit3 – Bit0 : Reserved.
Bit4 : Write "1" to this bit to enable EFlash read through SMBus.
Bit5 : Write "1" to this bit to disable EFlash read through SMBus.
Bit6 : Write "1" to this bit to enable EFlash write through SMBus.
Bit7 : Write "1" to this bit to disable EFlash write through SMBus.
When reading from this register, one of the two bits in each pair will always be set. Following reset, the default value for this register will be 51h.
****

Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Eh	Enb SBS Fun. Write event	Enb SBS Fun. Read event	SMBus Clock	SMBus Data	Reserved			
1Fh	SMB written	Reserved	Most recently accessed SBS Function register					

20h	SMBus reset	OZ930 SMBus address

Register 1Eh
Bit3 – Bit0 : Reserved
Bit4 : Copy SMBus data (Pin 36) to here for software monitor
Bit5 : Copy SMBus clock (Pin 35) to here for software monitor
Bit6 : Enable SBS Function read event (Also refer to Control Register 01h bit5)
Bit7 : Enable SBS Function write event (Also refer to Control Register 01h bit5)

Register 1Fh
Bit5 – Bit0 : SBS Function register accessed by the most recent SMBus access.
Bit6 : Reserved.
Bit7 : Set high to indicate the most recent SMBus access was a write (Also refer to Control Register 01h bit5).

Register 20h
Bit6 – Bit0 : OZ930 SMBus address.
OZ930 default SMBus address is 30h. For Smart Battery application, this register will be set to 16h.
Bit7 : Returns state of SMBus reset during read if SMBus engine generate a reset. Write has no effect.
****

Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
21h	Disable SMBus	Disable PEC	SBS Function register address (00h ~ 3Fh)					
22h	SBS Function register data (low byte)							
23h	SBS Function register data (high byte)							
24h	All SBS Fun. Busy	Selected Fun. Busy	Reserved					
25h	Reserved		Busy SBS Function register #1					
26h	Reserved		Busy SBS Function register #2					
27h	Reserved		Busy SBS Function register #3					

Register 21h
Bit5 – Bit0 : SBS Function register address (00h ~ 3Fh). Refer to “SBS v1.1 Functions” section.
Bit6 : Set to disable PEC (Packet Error Checking). Default is 0, enable PEC.
Bit7 : Set to disable internal SMBus controller. Default is 0, enable SMBus.

Register 22h
Bit7 – Bit0 : Read or write SBS Function register data (low byte)

Register 23h
Bit7 – Bit0 : Read or write SBS Function register data (high byte)
Because SBS Function registers may access by internal uP and external SMBus host, OZ930 internal logic has to guarantee the synchronization of the Control Register 22h and 23h. When reading from Control Register 22h, the value for register 23h is sampled from the SBS Function register at the same instant. So, when the end user read from Control Register 23h next time, he will receive the value that matches the latest value read from Control Register 22h. Vice versa, when Control Register 22h is written, the data is saved but it’s not put into SBS Function register. When Control Register 23h is written, the saved value from the most recent register 22h write will be copied to the SBS Function register at the same instant the Control Register 23h value is written.
So, the following is the correct sequence for reading SBS Function register:
a) Write the SBS Function register number into Control Register 21h, bit5 – bit0;
b) Read Control Register 22h to get the SBS Function value low byte;
c) Read Control Register 23h to get the SBS Function value high byte;
The following is the correct sequence for writing SBS Function register:
a) Write the SBS Function register number into Control Register 21h, bit5 – bit0;
b) Write the SBS Function value low byte to Control Register 22h;
c) Read the SBS Function value high byte to Control Register 23h;

Register 24h
Bit5 – Bit0 : Reserved.

Bit6 : Bit set to indicate that the SBS Function specified in Control Registers 25h ~ 27h are busy. This bit is set by any external SMBus host write to a writeable SBS Function and cleared by uP write a "1" to this bit.
Bit7 : Bit set to indicate that all SBS Functions (except the SBS status function register 16h) are busy. This bit is set by any external SMBus host write to a writeable SBS Function and cleared by uP write a "1" to this bit.

Register 25h ~ 27h
Each of these Control Registers corresponds to one SBS Function register, or 00h to disable. When bit 6 in Control Register 24h is set, the selected SBS Function register is busy. Typically, these 3 registers select the three SBS Functions 05h, 06h & 07h that are updated as a result of a change in SBS Function 04h "AtRate".
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
28h	Address for SMBus command, low byte							
29h	Address for SMBus command, high byte							
2Ah	Data for SMBus command, low byte							
2Bh	Data for SMBus command, high byte							
2Ch	SMBus command code							

These Control Registers 28h ~ 2Ch provide an interface for uP to respond to external host SMBus command that need uP support. When the "SMBus command interrupt" bit (Control Register 01h, bit 6) is set to get the uP attention, the uP can then read these above Control Registers to figure out what it is being requested to do. When the uP has completed the request, it should clear the "SMBus command interrupt" bit.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2Dh	Master Error	Master PEC Error	Cmd PEC missing	Cmd PEC Error	SMBus EFlash write prot.	Critical host write	Critical charger write	SBS Fun. Write to charger
2Eh				SBS Function register for master transfer				
2Fh					Retry Counter for master			

OZ930 also can be act as SMBus master to send critical information to Smart Battery charger or other SMBus device. Please refer to "Smart Battery Data Specification, Revision 1.1" section 6.1, section 6.2, section 6.3 for detailed protocol information.

Register 2Dh
Bit0 : Request a SMBus master write to the battery charger.
Bit1 : Request a "critical" SMbus master write to the battery charger.
Bit2 : Request a "critical" SMBus master write to the host.
Bit3 : High when EFlash is write-protection to SMBus accesses.
Bit4 : When a command code is pass to uP, this bit will be set if a PEC error was found on the command code or other related registers.
Bit5 : "PEC byte missing" status bit set to respond to a command code.
Bit6 : After a master write is completed, this bit indicates a PEC error happened. It may be caused by real PEC error or the slave doesn't support PEC.
Bit7 : After a master write is completed, this bit indicates an error happened (except PEC).

Register 2Eh
Bit4 – Bit0 : SBS Function register number (00h ~ 1Fh) for transfer.
Bit7 – Bit5 : Reserved.

Register 2Fh
Bit3 – Bit0 : Retry counter for master block. 0 = immediately retry, 1 = 4 32khz clocks, 2 = 8 32khz clocks, etc.
Bit7 – Bit4 : Reserved.

Setting one of bits in Control Register 2Dh will cause an SMBus master write to take place. If bit 0 is set, the SBS Function register number is copied in the second byte of the write word transfer. If bit1 or bit 2 is set, the second byte will contain OZ930's SMBus address (normally is 16h). Once one of these bit is set, hardware will clear it after the write operation has finished.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
30h	GPIO output enable (Bank switched between PA group and PC group)							
31h	GPIO open-drain enable (Bank switched between PA group and PC group)							
32h	GPIO negative-edge trigger enable							
33h	GPIO positive-edge trigger enable							
34h	GPIO pin event (write 1 to clear)							
35h	GPIO pin data (Bank switched between PA group and PC group)							
36h	Analog input enable (only for PA7 ~ PA1)							
37h	Reserved							Select PC group

OZ930 has three groups of GPIO. PA group (PA7 ~ PA1) and PC group (PC3 ~ PC0) are controlled by Control Register 30h – 37h. PB group (PBO and PBI) are controlled by Protection Register 1Bh.

Register 30h

Output enable bits for PA group or PC group. If any bit set to 1, the associated pin is configured as output pin. If any bit is 0, the associated pin is not driven.

Bit	Associated Pin (Control Register 37h bit0 = 0)	Associated Pin (Control Register 37h bit0 = 1)
Bit0	Reserved	PC0
Bit1	PA1	PC1
Bit2	PA2	PC2
Bit3	PA3	PC3
Bit4	PA4	Reserved
Bit5	PA5	Reserved
Bit6	PA6	Reserved
Bit7	PA7	Reserved

Register 31h

Open-drain enable bits. If any pin is enabled as an output (controlled by Control Register 30h), an “1” bit in this register will specify an open-drain output function (data = 1 selects tri-state, data = 0 selects low). If open-drain enable bit is clear, the output pin will be push-pull (normal output).

Bit	Associated Pin (Control Register 37h bit0 = 0)	Associated Pin (Control Register 37h bit0 = 1)
Bit0	Reserved	PC0
Bit1	PA1	PC1
Bit2	PA2	PC2
Bit3	PA3	PC3
Bit4	PA4	Reserved
Bit5	PA5	Reserved
Bit6	PA6	Reserved
Bit7	PA7	Reserved

Register 32h

Negative-edge triggered event enabled.

Bit	Associated Pin (Control Register 37h bit0 = 0)	Associated Pin (Control Register 37h bit0 = 1)
Bit0	Reserved	PC0
Bit1	PA1	PC1
Bit2	PA2	PC2
Bit3	PA3	PC3
Bit4	PA4	Reserved
Bit5	PA5	Reserved
Bit6	PA6	Reserved
Bit7	PA7	Reserved

Register 33h

Positive-edge triggered event enabled.

Bit	Associated Pin (Control Register 37h bit0 = 0)	Associated Pin (Control Register 37h bit0 = 1)
Bit0	Reserved	PC0
Bit1	PA1	PC1
Bit2	PA2	PC2
Bit3	PA3	PC3
Bit4	PA4	Reserved
Bit5	PA5	Reserved
Bit6	PA6	Reserved
Bit7	PA7	Reserved

Register 34h

GPIO pin event bits, write "1" to clear.

Bit	Associated Pin (Control Register 37h bit0 = 0)	Associated Pin (Control Register 37h bit0 = 1)
Bit0	Reserved	PC0
Bit1	PA1	PC1
Bit2	PA2	PC2
Bit3	PA3	PC3
Bit4	PA4	Reserved
Bit5	PA5	Reserved
Bit6	PA6	Reserved
Bit7	PA7	Reserved

Register 35h

GPIO pin data. If GPIO pin is configured as input pin, the input data is mapped to this register. If GPIO pin is configured as output pin, the data in this register will be passed to the related pin.

Bit	Associated Pin (Control Register 37h bit0 = 0)	Associated Pin (Control Register 37h bit0 = 1)
Bit0	Reserved	PC0
Bit1	PA1	PC1
Bit2	PA2	PC2
Bit3	PA3	PC3
Bit4	PA4	Reserved
Bit5	PA5	Reserved
Bit6	PA6	Reserved
Bit7	PA7	Reserved

Register 36h

Analog input enable bits. When the bit is set, the associated pin is configured as an analog input pin and its digital buffers are powered down. Only PA group (PA7 ~ PA1) can be configured as analog inputs.

Bit0 : Reserved
Bit1 : Associated PA1 pin
Bit2 : Associated PA2 pin
Bit3 : Associated PA3 pin
Bit4 : Associated PA4 pin
Bit5 : Associated PA5 pin
Bit6 : Associated PA6 pin
Bit7 : Associated PA7 pin

Register 37h

Bit0 : When set, select PC group (PC3 ~ PC0).
Bit7 – Bit1 : Reserved

****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
38h	Reserved							
39h	Protection Register address							RD/WR#
3Ah	Protection Register Data							

Register 38h
Bit7 – Bit0 : Reserved

Register 39h
Bit0 : Read/Write indication. 1 = Read; 0 = Write
Bit7 – Bit1 : Protection Register address (00h – 1Ch) for transfer.

Register 3Ah
Bit7 – Bit0 : Protection Register Data.

For write operation to Protection Register:
a) Write the data to Control Register 3Ah;
b) Write the Protection register address to Control Register 39h, with bit 0 clear to indicate a write;
For read operation from Protection Register:
a) Write the Protection register address to Control Register 39h, with bit 0 set to indicate a read;
b) Read the data from Control Register 3Ah.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3Bh	Chip ID/Version register							

Register 3Bh
Bit7 – Bit0 : Read-only register to identify OZ930 chip ID/version.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3Ch	Hardware Configuration data low byte							
3Dh	Hardware Configuration data mid byte							
3Eh	Hardware Configuration data high byte							

Register 3Ch – Register 3Eh total 3 bytes, 24 bits are used for hardware configuration, such as trimming, calibration, etc.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3Fh	Permanent Fail (PF) output (fuse blow)							

This register is used to blow the fuse (raise PF signal). Since this is an unrecoverable condition, an extra measure of security is built in. To blow the fuse, read from this register first, invert the bits read and write the result back. If the written value matches the expected value, the fuse will be blown, otherwise, the write will be ignored.
****

PROTECTION REGISTER MAP

OZ930 has 28 addressable protection registers. These registers provide battery pack control, configuration and status information for protection purpose. OZ930 internal uP can indirect access these 28 Protection Registers through Control Registers 39h & 3Ah.

Protection register Address	Type	Description
00h	R	Reserved for internal usage
01h	R/W	Over voltage threshold
02h	R/W	Under voltage threshold
03h	R/W	Short circuit delay time
04h	R/W	Over/Under voltage delay time and Over current delay time
05h	R/W	Reserved for internal usage
06h	R/W	Over current for discharge threshold and short circuit current threshold
07h	R/W	Over current for charge/discharge threshold
08h	R/W	Battery cell voltage scan rate and permanent fail control
09h – 0Bh	R	Reserved for internal usage
0Ch	R/W	Charge/Discharge FET control and Protection status
0Dh	R	Reserved for internal usage
0Eh	R/W	Cell balance control
0Fh	R	Reserved for internal usage
10h – 11h	R/W	Trickle charge current control
12h	R/W	Battery cell selection for voltage measurement
13h -14h	R	Battery cell voltage data
15h	R/W	Dead-man timer enable
16h	R	Dead-man timer
17h	R/W	Event interrupt enable register
18h	R	Event register
19h	R/W	Reserved for internal usage
1Ah	R/W	Status register
1Bh	R/W	GPIO pin PBI and PBO control
1Ch	R/W	Main clock speed control

Note: All the registers in shadow are fully controlled by Battery Gauge Software (BGS), not accessible to the end user

Detailed Protection Register information

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h	OV7	OV6	OV5	OV4	OV3	OV2	OV1	OV0

This register sets the battery over voltage protection threshold.
This 8-bit register adds an offset to the over-voltage protection threshold base value. Total 256 steps with each step being 9.375mV. The threshold base value is 2400mV. So, the final over-voltage protection threshold is:

OV threshold = 2400mV + 9.375mV * N, where N is register value

The default register value is 192 (C0h), that means the over-voltage threshold is 4200mV. (2400mV + 9.375mV * 192 = 4200mV).
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02h	UV7	UV6	UV5	UV4	UV3	UV2	UV1	UV0

This register sets the battery under voltage protection threshold.
This 8-bit register adds an offset to the under-voltage protection threshold base value. Totally there are 256 steps with each step being 9.375mV. The threshold base value is 1800mV. So, the final under-voltage protection threshold is:

UV threshold = 1800mV + 9.375mV * N, where N is register value

The default register value is 128 (80h), that means the over-voltage threshold is 3000mV. (1800mV + 9.375mV * 128 = 3000mV).
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
03h	SCTN3	SCTN2	SCTN1	SCTN0	N/A	SCTP2	SCTP1	SCTP0

This register sets the short-circuit delay time.
Bit2 – Bit0 (SCTP2 – SCTP0): These 3 bits set the short circuit delay timer prescale M with M=2 as the default.
Bit7 – Bit4 (SCTN3 – SCTN0): These 4 bits set the short circuit delay clock cycles N with N=2 as the default.
The short circuit delay time is calculated as follows:

SC delay time = $N*2^{(M+2)}$ cycles of 128kHz clock = 7.8μs * $N*2^{(M+2)}$

So, the default short circuit delay time is N=2, M=2, SC delay time = 7.8μs * 2 * $2^{(2+2)}$ ≈ 250 μs
The minimum short circuit delay time is N=1, M=0, SC delay time = 7.8μs * 1 * 2^2 ≈ 32 μs
The maximum short circuit delay time is N=0, M=7, SC delay time = 7.8μs * 16 * $2^{(7+2)}$ ≈ 64 ms
Note here SCTN4 – SCTN0 = 0h interpreted as 16.
For more accuracy, keep M as low as possible.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04h	OUVT3	OUVT2	OUVT1	OUVT0	OCT3	OCT2	OCT1	OCT0

This register sets the over/under voltage delay time and over current delay time.
Bit3 – Bit0 (OCT3 – OCT0): These 4 bits set the over current delay time N with N=2 as the default.
The over current delay time is calculated as follows:

OC delay time = 250ms * N

The default over current delay time is N=2, OC delay time = 250ms * 2 = 500ms
The minimum over current delay time is N=1, OC delay time = 250ms
The maximum over current delay time is N=0, OC delay time = 250ms * 16 = 4 seconds
Note here OCT3 – OCT0 = 0h interpreted as 16, and the over current for charge and over current for discharge share the same delay time.

Bit7 – Bit4 (OUVT3 – OUVT0): These 4 bits set the over/under voltage delay time N with N=2 as the default.
The over/under voltage share the same time delay and the delay relies on the Battery Protection Engine (BPE) cell voltage scan speed. (Refer to Protection register 08h for cell voltage scan speed definition).
The over/under voltage delay time is calculated as follows:

OV/UV delay time = N * (cell voltage scan period)

The default over/under voltage delay time is N=2, OV/UV delay time = 2 * (default cell voltage scan period) = 500ms (the default cell voltage scan period is 250ms).
The minimum over/under voltage delay time is N=1, OV/UV delay time = 1 * (the minimum cell voltage scan period) = 250ms (the minimum cell voltage scan period is 250ms).
The maximum over/under voltage delay time is N=0, OV/UV delay time = 16 * (the maximum cell voltage scan period) = 16 * 32 second = 512 second. (the maximum cell voltage scan period is 32 seconds). Note here OUVT3 – OUVT0 = 0h interpreted as 16.

The cell voltage scan speed is controlled by Protection register 08h bit2-bit0, with fastest speed 250ms, slowest speed 32 seconds. The scan speed is fully controlled by Battery Gauge Software (BGS) based on the battery pack's operation status. In this case, the over/under voltage delay time also varies with battery pack operation status. When battery pack is in under charging/discharging status, voltage scan speed is at fastest speed (250ms), and only in this state, we care about the over/under voltage safety checking. For this reason, customer's selection of the over/under voltage delay time will only be based on the fastest cell voltage scan speed.

OV/UV delay time = N * 250ms

The minimum over/under voltage delay time is N=1, OV/UV delay time = 1 * 250ms = 250ms.
The maximum over/under voltage delay time is N=0, OV/UV delay time = 16 * 250ms = 4 second.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h	OCD3	OCD2	OCD1	OCD0	SC3	SC2	SC1	SC0
07h	Reserved	reserved	OCC4	OCC3	OCC2	OCC1	OCC0	OCD4

SC3 – SC0: These 4 bits set up the short circuit current threshold voltage.
The short circuit current threshold voltage is calculated as follows:

SC current threshold voltage = 80mV + N * 25mV, where 0 ≤ N ≤ 13.
Here N is the SC3 – SC0 value with N=0 as the default.

The minimum short circuit current threshold voltage is N=0, SC current threshold voltage = 80mV.
The maximum short circuit current threshold voltage is N=13, SC current threshold voltage = 80mV + 13 * 25mV = 405mV.
The final short circuit current threshold depends on the external sense resistor value. For example, if external sense resistor is 10mohm, then the default short circuit current threshold = 80mV/10mohm = 8 Amps.

OCD4 – OCD0: These 5 bits set up the discharge over current threshold voltage.
The discharge over current threshold voltage calculated as follows:

OCD current threshold voltage = 50mV + N * 5mV, where 0 ≤ N ≤ 26.
Here N is the OCD4 – OCD0 value with N=0 as the default.

The minimum discharge over current threshold voltage is N=0, OCD current threshold voltage = 50mV.
The maximum discharge over current threshold voltage is N=26, OCD current threshold voltage = 50mV + 26 * 5mV = 180mV.
The final discharge over current threshold depends on the external sense resistor value. For example, if external sense resistor is 10mohm, then the default discharge over current threshold = 50mV/10mohm = 5 Amps.

OCC4 – OCC0: These 5 bits set up the charge over current threshold voltage.
The charge over current threshold voltage is calculated as follows:

OCC current threshold voltage = 50mV + N * 5mV, where 0 ≤ N ≤ 26.
Here N is the OCC4 – OCC0 value with N=0 as the default.

The minimum charge over current threshold voltage is N=0, OCC current threshold voltage = 50mV.
The maximum charge over current threshold voltage is N=26, OCC current threshold voltage = 50mV + 26 * 5mV = 180mV.
The final charge over current threshold depends on the external sense resistor value. For example, if external sense resistor is 10mohm, then the default charge over current threshold = 50mV/10mohm = 5 Amps.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h	DISP	EFUSE	Reserved			CVS2	CVS1	CVS0

Bit2 – Bit0 (CVS2 – CVS0): These 3 bits set the Battery Protection Engine (BPE) scan cell voltage speed. When the scan speed is set, BPE will measure each individual cell voltage (3 cells or 4 cells depends on the battery pack configuration) and check for over-voltage or under-voltage condition. Remember, BPE cell voltage checking according to CVS2 – CVS0 predefined scan speed is fully independent of Battery Gauge Software (BGS).
The cell voltage scan speed is calculated as follows:

Cell voltage scan speed = $2^{(N-2)}$ second, where N is the CVS2 – CVS0 value with N=0 as the default.

The fastest scan speed is N=0, CVS scan speed = 2^{-2} = 250 ms.
The slowest scan speed is N=7, CVS scan speed = 2^{5} = 32 second.

Bit6 (EFUSE): This bit enables the fuse blow function after turning off the charge/discharge FET.

EFUSE = 0 (default): Disable fuse blow function. When some abnormal condition happens, such as OV, UV, OCC, OCD, SC, OZ930 only turns off charge/discharge FET.
EFUSE = 1: Enable fuse blow function. When some abnormal condition happens, such as OV, UV, OCC, OCD, SC, OZ930 turns off charge/discharge FET first. After the FET is off, if the abnormal condition is still there, then after the second delay time, OZ930 raises the PF signal pin.

Bit7 (DISP): This bit disables over current and short circuit protection circuits after charge/discharge FETs are off.
DISP = 0 (default): Over current and short circuit protection circuits are always alive
DISP = 1: Over current and short circuit protection circuits automatically shut down when both charge and discharge FETs are off. This way, the system can save some power.
Note: When Bit6 (EFUSE) is set, Bit7(DISP) should be kept in the cleared state. This way, OZ930 sends the command to turn off the charge/discharge FETs, but protection circuits are still monitoring the abnormal case and preparing to raise the PF signal if the abnormal case is still there.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ch	ECHG	EPCHG	EDSG	Reserved	SC	OC	UV	OV

Bit3 – Bit0: These 4 bits are abnormal condition status bits for FET control, which is set by the Battery Protection Engine (BPE).
Bit0 (OV): Over voltage condition, when this bit is set by BPE, OZ930 will automatically turn off the charge FET (even though Bit7 or Bit6 may be enabled).
Bit1 (UV): Under voltage condition, when this bit is set by BPE, OZ930 will automatically turn off the discharge FET (even though Bit5 may be enabled).
Bit2 (OC): Over current condition (over current in either charge or discharge), when this bit is set by BPE, OZ930 will automatically turn off both the charge and discharge FET.
Bit3 (SC): Short circuit condition, when this bit is set by BPE, OZ930 will automatically turn off both charge and discharge FET.
All the Bit3 – Bit0 can be cleared by writing "1" to them when the related abnormal condition is gone or under control.

Bit7 – Bit5: These 3 bits are charge and discharge FET control bit.
Bit5 (EDSG): Enable discharge FET.
EDSG = 0 (default): Disable discharge FET (discharge FET turned off).
EDSG = 1: Enable discharge FET. When this bit is set, if no abnormal conditions exist, discharge FET will turn on.
Bit6 (EPCHG): Enable pre-charge.
EPCHG = 0 (default): Disable pre-charge.
EPCHG = 1: Enable pre-charge. When this bit is set, OZ930 will drive charge FET as variable resistor to limit the charge current. The pre-charge current value is controlled by Protection register 10h & 11h.
Bit7(ECHG): Enable charge FET.
ECHG = 0 (default): Disable charge FET (charge FET turned off).
ECHG = 1: Enable charge FET. When this bit is set, if no abnormal conditions exist, charge FET will turn on.
Note: ECHG bit will overwrite EPCHG bit, that means when both ECHG bit and EPCHG bits are set, OZ930 will fully turn on charge FET. So, to set pre-charge mode, only EPCHG bit needs to be set.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Eh	Reserved					ECB	CB1	CB0

This register sets up the cell balancing mode.
Bit 2 (ECB): When this bit is set, the cell balancing function is enabled.
Bit1 – Bit0 (CB1 – CB0): Select which cell to be balanced, enable the related bypass path.
00 – Selects the highest cell (BAT1 – BAT2) for cell balancing.
01 – Selects the second highest cell (BAT2 – BAT3) for cell balancing.
10 – Selects the second lowest cell (BAT3 – BAT4) for cell balancing.
11 – Selects the lowest cell (BAT4 – BAT5) for cell balancing.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10h	PCHG7	PCHG6	PCHG5	PCHG4	PCHG3	PCHG2	PCHG1	PCHG0
11h	Reserved						PCHG9	PCHG8

PCHG9 – PCHG0: These 10 bits set up the charge FET Vgs voltage in pre-charge mode (EPCHG = 1).
PCHG9 – PCHG0 set the charge FET Vgs voltage as follows:
0000000000 → Vgs = VCC – 0.5V
……
1111111111 → Vgs = VCC – 4.0V
The charge FET turn on resistance relies on the Vgs voltage, which limits the pre-charge current. But the relationship between Vgs voltage and pre-charge current fully depends on the charge FET characteristics.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12h	CSEL3	CSEL2	CSEL1	CSEL0	Reserved	CRES2	CRES1	CRES0

This register selects the cell for voltage measurement and set the voltage measurement resolution.
Bit2 – Bit0 (CRES2 – CRES0): Set the voltage measurement resolution as shown in the following table:

CRES2 – CRES0	Resolution
000 (default)	10-bit
001	11-bit
010	12-bit
011	13-bit
100	14-bit
101	15-bit
110 – 111	Reserved

Bit7 – Bit4 (CSEL3 – CSEL0): Select the cell for voltage measurement:

CSEL3 – CSEL0	Selected Cell
0000	Highest cell
0001	Second highest cell
0010	Second lowest cell
0011	Lowest cell
0100	Internal 3.3V reference voltage
0101	Internal 1.5V reference voltage
0110	ADC offset
0111	3.3V regulator voltage
1000	VPACK/4
1001 – 1111	Reserved

****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
13h	CADC6	CADC5	CADC4	CADC3	CADC2	CADC1	CADC0	BUSY
14h	CADC14	CADC13	CADC12	CADC11	CADC10	CADC9	CADC8	CADC7

Bit0 (BUSY): This bit indicates that the voltage measurement is not finished yet. ADC is busy.
BUSY = 1: ADC is busy, the voltage measurement not finished yet
BUSY = 0: ADC is not busy, the voltage measurement is finished. Only when BUSY=0, it will get the correct recent cell voltage measurement data.
CADC14 – CADC0: The recent cell voltage measurement data.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
15h	Reserved						DT1	DT0
16h	Reserved				DTIMER3	DTIMER2	DTIMER1	DTIMER0

These two registers enable the dead-man timer function.
DT1 – DT0: Enable the dead-man timer and set the dead-man timer length.

DT1 – DT0	Dead-man timer length
00 (default)	Disabled. Infinite length
01	3 * cell voltage scan period
10	7 * cell voltage scan period
11	15 * cell voltage scan period

DTIMER3 – DTIMER0: Running dead-man timer.
When dead-man timer is enabled (DT1-DT0 set value > zero), DTIMER3 – DTIMER0 will keep increasing with the passage of time. If dead-man timer expires, OZ930 raises the PF signal pin to blow the fuse. So, it's the responsibility of the Battery Gauge Software (BGS) to do the following within the specified time period:

a) Read Protection register 16h (DTIMER3 – DTIMER0);
b) Decrement the value read;
c) Write the result back to register 16h

By doing the above steps, the dead-man timer never expires if BGS is working properly.

The dead-man timer adds a safety mechanism for checking the BGS running status. If BGS hangs or enters into some dead loop, then the dead-man loop will raise the PF signal pin to blow the fuse.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
17h	Reserved			ECADCI	ESCI	EOCI	EUVI	EOVI
18h	Reserved			CADCE	SCE	OCE	UVE	OVE

Protection register 17h is the interrupt control register. When individual bit is set, when the related event happens, Battery Protection Engine (BPE) will generate an interrupt to uP.
Bit 0 (EOVI): Enable over voltage event interrupt
EOVI = 0 (default): Over voltage event interrupt disabled
EOVI = 1: Over voltage event interrupt enabled
Bit 1 (EUVI): Enable under voltage event interrupt
EUVI = 0 (default): Under voltage event interrupt disabled
EUVI = 1: Under voltage event interrupt enabled
Bit 2 (EOCI): Enable over current event interrupt
EOCI = 0 (default): Over current event interrupt disabled
EOCI = 1: Over current event interrupt enabled
Bit 3 (ESCI): Enable short circuit event interrupt
ESCI = 0 (default): Short circuit event interrupt disabled
ESCI = 1: Short circuit event interrupt enabled
Bit 4 (ECADCI): Enable cell voltage ADC event interrupt
ECADCI = 0 (default): Cell voltage ADC event interrupt disabled
ECADCI = 1: Cell voltage ADC event interrupt enabled

Protection register 18h is the event register. This register contains a latched bit for each individual event. When any one of these bits is set, along with the corresponding event interrupt enable bit set in the Protection register 17h, BPE will generate an interrupt to the uP. The event bits, once set, can only be cleared by writing a "1" to the bit.
Bit 0 (OVE): Over voltage event.
Bit 1 (UVE): Under voltage event.
Bit 2 (OCE): Over current event.
Bit 3 (SCE): Short circuit event.
Bit 4 (CADCE): Cell voltage ADC event.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1Ah	SHUTDN	PBB	CHGR	CFGLOCK	Reserved	VCCLOW	CNUM1	CNUM0

This register is the status register.
Bit1 – Bit0 (CNUM1 – CNUM0) (Read only): These two bits reflect the two external pin (CELL_NUM1 and CELL_NUM0) set up and indicate the number of cells in series.

CNUM1 – CNUM0	Cells in series
00	Reserved
01	Reserved
10	3 cells
11	4 cells

Bit 2 (VCCLOW): This bit indicates that the OZ930 power supply (VCC) is lower than 6.5V.
VCCLOW = 0: VCC is higher than 6.5V
VCCLOW = 1: VCC is lower than 6.5V.
OZ930 power supply (VCC) voltage is either from the battery pack or from the charger. If VCC is too low, system may not work properly. This bit informs the Battery Gauge Software (BGS) that system voltage is too low and should prepare to enter into shutdown (ship) mode.
Bit 4 (CFGLOCK): This is the configuration lock bit.
CFGLOCK = 0: The configuration is not locked. Protection registers 01h – 07h can be changed.
CFGLOCK = 1: The configuration is locked. Protection registers 01h – 07h can't be changed. Also this bit once set, can't be cleared again until a shutdown causes a reset.
Bit 5 (CHGR) (Read only): This bit indicates that a charger is attached or not.
CHGR = 0: No charger is attached.
CHGR = 1: Charger is attached.
Bit 6 (PBB): System power by battery request.
PBB = 0: System can only be powered by charger, when charger is removed, system shutdown happens again.
PBB =1: System can also be powered by battery. When this bit is set, system can still stay alive and be powered by battery, even when the charger is removed.
Bit 7(SHUTDN): Shutdown request.
SHUTDN = 0: System works normally.
SHUTDN =1: System shutdown request. When this bit is set. OZ930 shuts down itself and enters the ultra low power status (< 1uA) –-- ship mode. Only when a charger is attached, the system wakes up again.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1Bh	Reserved			PBO_EN	Reserved	PBO_OUT	Reserved	PBI_IN

This register controls the GPIO pin PBI and PBO
Bit0 (PBI_IN) (Read only): This bit mirrors the general purpose input pin PBI (pin 43) value. We can read this bit to monitor PBI pin input value
Bit2 (PBO_OUT): This bit controls the general purpose output pin PBO (pin 45). When set to 1, PBO will output 1; when set to 0, PBO will output 0.
Bit4 (PBO_EN): This bit enable PBO pin output.
PBO_EN = 0: PBO output disabled, PBO is in high impedance state
PBO_EN = 1: PBO output enabled.
****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1Ch	Reserved							CLK/4

This register controls OZ930 system clock frequency.
Bit0 (CLK/4): When this bit is set, the system main clock speed slow down 4 times.
CLK/4 = 0: system clock frequency = 256kHz
CLK/4 = 1: system clock frequency = 256kHz/4 = 64kHz
This bit is used for power management. When Battery Gauge Software (BGS) enters sleep mode, set this bit to slow down the system clock to save power.

SBS v1.1 FUNCTIONS

OZ930 fully supports "Smart Battery Data Specification, revision 1.1" (SBS v1.1). There are up to 64 functions defined by SBS v1.1, so there are 64 registers that correspond to 64 SBS v1.1 functions in OZ930. Most of them are 16-bit (word) wide, only a few (SBS Function 20h ~ 23h) are strings. OZ930 internal uP can indirectly access SBS Function registers through Control Registers 21h, 22h & 23h. End user can directly access SBS v1.1 Functions through SMBus (Pin 35 SMBCLK & Pin 36 SMBDATA)

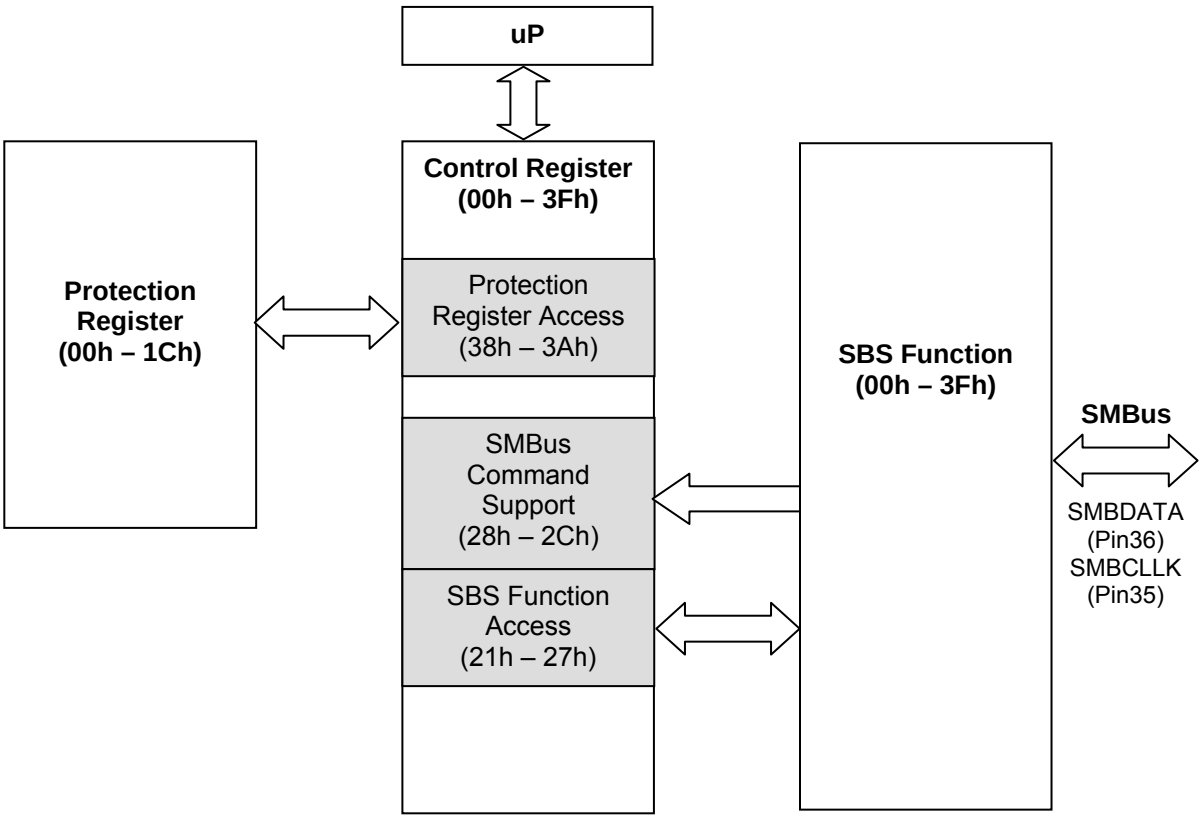
FUNCTION	Code	Access	Units
Manufacturer Access	0x00	r/w	word
RemainingCapacityAlarm	0x01	r/w	mAh or 10mWh
RemainingTimeAlarm	0x02	r/w	minutes
Battery Mode	0x03	r/w	bit flags
AtRate	0x04	r/w	mA or 10mW
AtRateTimeToFull	0x05	r/w	minutes
AtRateTimeToEmpty	0x06	r	minutes
AtRateOK	0x07	r	Boolean
Temperature	0x08	r	0.1°K
Voltage	0x09	r	mV
Current	0x0a	r	mA
AverageCurrent	0x0b	r	mA
MaxError	0x0c	r	percent
RelativeStateOfCharge	0x0d	r	percent
AbsoluteStateOfCharge	0x0e	r	percent
RemainingCapacity	0x0f	r	mAh or 10mWh
FullChargeCapacity	0x10	r	mAH or 10mWh
RunTimeToEmpty	0x11	r	minutes
AverageTimeToEmpty	0x12	r	minutes
AverageTimeToFull	0x13	r	minutes
ChargingCurrent	0x14	r	mA
ChargingVoltage	0x15	r	mV
BatteryStatus	0x16	r	bit flags
CycleCount	0x17	r	count
DesignCapacity	0x18	r	mAh or 10mWh
DesignVoltage	0x19	r	mV
SpecificationInfo	0x1a	r	unsigned int
ManufactureDate	0x1b	r	unsigned int
SerialNumber	0x1c	r	number
Reserved	0x1d – 0x1f	r	
ManufacturerName	0x20	r	string
DeviceName	0x21	r	string
DeviceChemistry	0x22	r	string
ManufacturerData	0x23	r	data
Reserved	0x25 – 0x2e	r	
Manufacturer Access	0x00	r/w	Reserved for O_2Micro use
Optional Mfg Fuction5	ox2f	r/w	Reserved for O_2Micro use
Optional Mfg Function4	0x3c-0x3f	r	Individual cell voltages

INTERNAL REGISTER ACCESS METHODOLOGY

Among the three sets of registers, OZ930's internal uP can only directly access the Control Registers. But OZ930 provides a mechanism for uP to indirectly acess the Protection Registers and SBS Function registers.

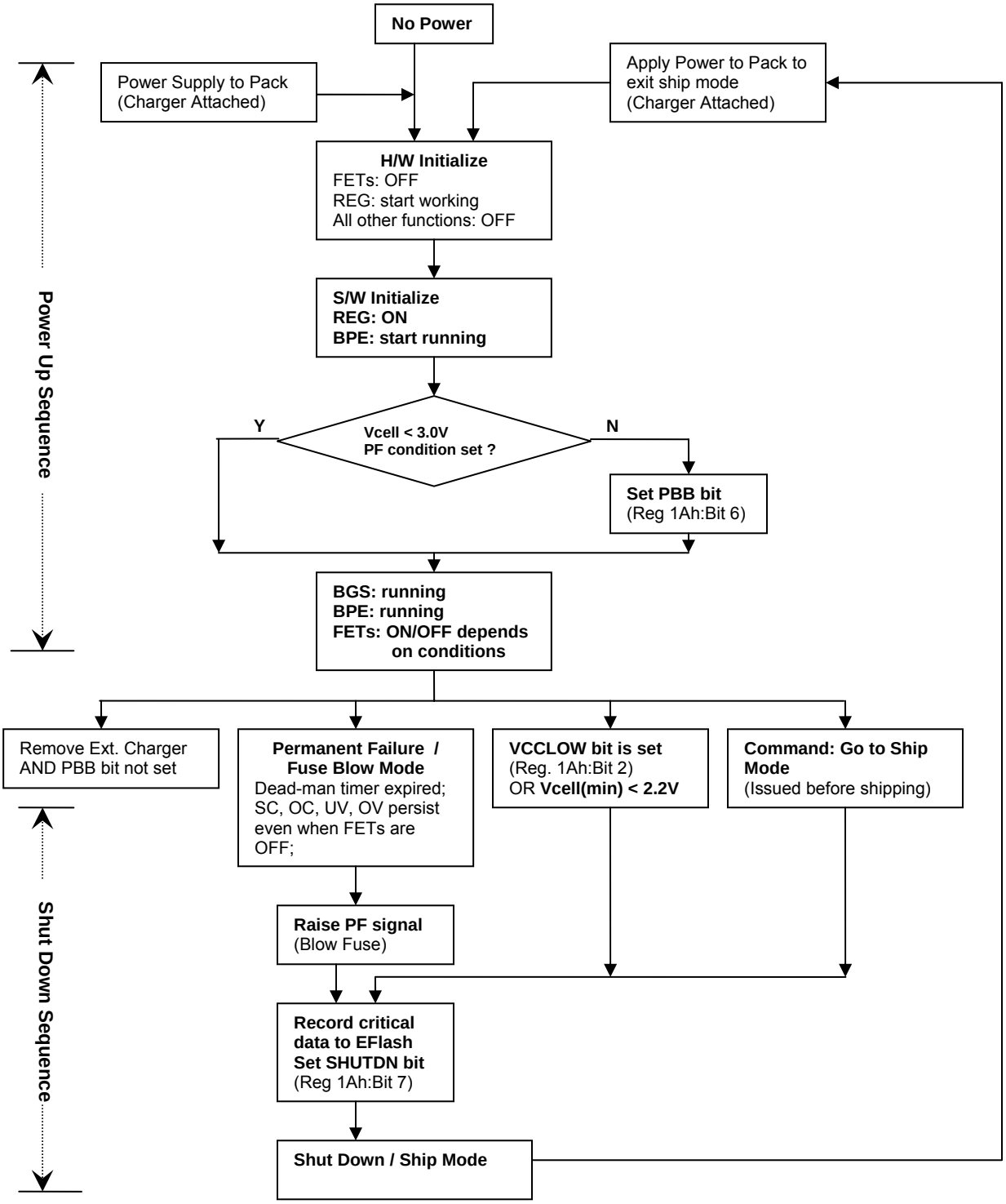
Shown in the following diagram, through Control Register 38h ~ 3Ah, uP can access Protection Registers, though Control Register 21h ~ 27h, uP can access SBS Functions. Still, through Control Register 28h ~ 2Ch, uP can support SMBus command.

External SMBus host can directly access SBS Function Registers by SMBus.



APPLICATION

Power up and Shut down sequence



Precharge Circuits to support 0-V charging

When the battery pack voltage drops low, even down to 0V, if the charge FET is simply turned ON to charge the battery, the VPACK is as low as the battery voltage. In this case, the supply voltage for the OZ930 and other devices on the board is too low to operate. OZ930 provides 2 precharge circuits to support 0-V charge. They are Main FET Precharge Mode and External Precharge FET Mode.

- External Precharge FET Mode – Use PBO pin to drive an external FET (in series with a current limiting resistor) to provide a precharge current path. The charger doesn't provide any precharge function.
- Main FET Precharge Mode – OZ930 drives the charge FET to saturation region to limit the precharge current. The charger may or may not provide precharge function.

External Precharge FET Mode

Fig. 1 shows the EXternal Precharge FET mode circuit. In this mode, an output pin PBO drives an extra FET (PCHG FET) to provide a Precharge current path. The charger doesn't have the Precharge function.

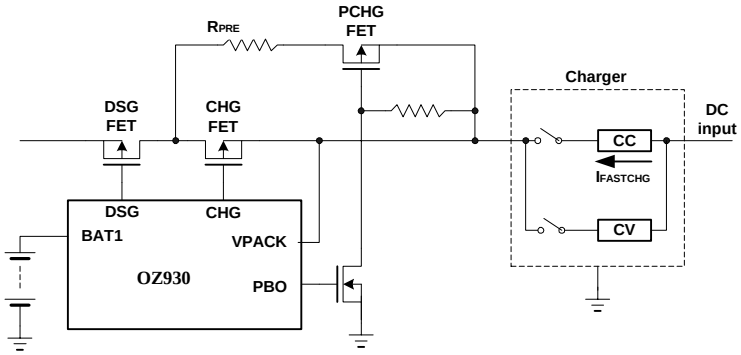


Fig. 1 EXternal Precharge FET Mode circuit

The PCHG FET is in series with the resistor R_{PRE} to limit the precharge current. When PBO is high, the external NMOS is turned on to pull the PCHG FET gate level to low and turn on the PCHG FET. The precharge current is expressed as:

$$I_{PCHG} = (VPACK - VBAT - V_{DS}) / R_{PRE}$$

Since V_{GS} is high enough, PCHG FET is driven to linear region and its resistance is very low. By approximating V_{DS} to 0V, the precharge current expression can be simplified as:

$$I_{PCHG} = (VPACK - VBAT) / R_{PRE}$$

When the charger is connected, OZ930 powers up and it's 3.3V and 2.5V regulator start .The DSG FET, CHG FET and PCHG FET are in OFF state (default state). Then the Battery Gauge Software (BGS) will check the battery voltage and enter the EXternal Precharge FET mode, drive the PBO pin to high and enable the precharge path.

In this mode, attention has to be paid to the high power consumption in PCHG FET and the series resistor R_{PRE} . The highest power is consumed when VBAT = 0V, where the highest voltage difference exists between the VPACK and BAT1 pin. For example, when VPACK = 17V for 4 series cell fast charge voltage, R_{PRE} = 300 ohm, then:

$$I_{PCHG} = (17.0V - 0.0V) / 300 \text{ ohm} = 56.6 \text{ mA}$$

$$17.0V \times 56.6 \text{ mA} = 0.963 \text{ W}$$

So, when the PCHG FET and R_{PRE} component are selected, it is necessary to check their power tolerance.

During the precharge mode, when all the cell voltage measured by BGS reaches the fast charge threshold (for example, 3.0V), BGS turns on the CHG FET and turns off the PCHG FET. It is also appropriate to turn on the DSG FET during switching from precharge mode to normal charge mode, to efficiently supply fast charging current (at precharge mode, DSG FET is automatically OFF because of the under-voltage protection mechanism).

Main FET Precharge Mode

Fig. 2 shows the Main FET Precharge mode circuit. In this mode, CHG FET provides the pre-charge current path, also acting as a current limiting resistor. The charger may or may not have the pre-charge function.

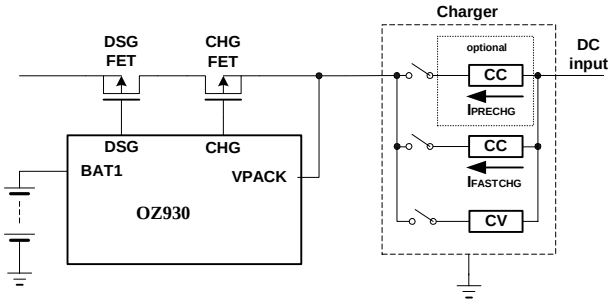


Fig. 2 Main FET Precharge mode circuit

When the charger is connected, OZ930 powers up and its 3.3V and 2.5V regulators start. The DSG FET, CHG FET and PCHG FET are in OFF state (default state). Then the Battery Gauge Software (BGS) checks the battery voltage and enters the Main FET Precharge mode by setting the appropriate pre-charge current value to Protection register 10h and 11h and enables the EPCHG bit (Protection 0Ch, bit 6). Then CHG FET acts as a current limiting resistor and provides the pre-charge path.

In this mode, OZ930 drives CHG FET to saturation region, and uses CHG FET as a current limiting resistor. The pre-charge current can be calculated as follows (CHG FET in saturation region):

$$I_{PCHG} = K * (V_{GS} - Vth)^2 * \{1 + \lambda *[V_{DS} - (V_{GS} - Vth)]\}$$

$$V_{DS} = VPACK - VBAT$$

Where K, Vth and λ are CHG FET parameters. OZ930 can control the V_{GS} to control the pre-charge current I_{PCHG}.

In Main FET Precharge mode, the voltage drop is in the CHG FET. The power consumption of the CHG FET has to be taken into consideration.

$$P_{CHG\_FET} = (VPACK - VBAT) * I_{PCHG}$$

When the I_{PCHG} is fixed, the worst case happens at VBAT = 0V. For example, VPACK = 17V for four series cell fast charge, I_{PCHG} = 30mA, then:

$$P_{CHG\_FET} = (17V - 0V) * 30mA = 0.51\ W$$

Also it should be noted that during the pre-charge procedure, cell voltage increases, VBAT increases, then according to the pre-charge current, I_{PCHG} equation and CHG FET power consumption, P_{CHG_FET} equation, both of them will decrease. This gives us a chance to increase the pre-charge current I_{PCHG} along with the VBAT increase. This speeds up the pre-charge procedure and prevents any harm to the battery cell. It is also important to keep the CHG FET power consumption in the safety range.

Based on OZ930's CHG FET drive control flexibility, Battery Gauge Software (BGS) will dynamically adjust the pre-charge current according to cell voltage and CHG FET power consumption as Fig. 3 shows.

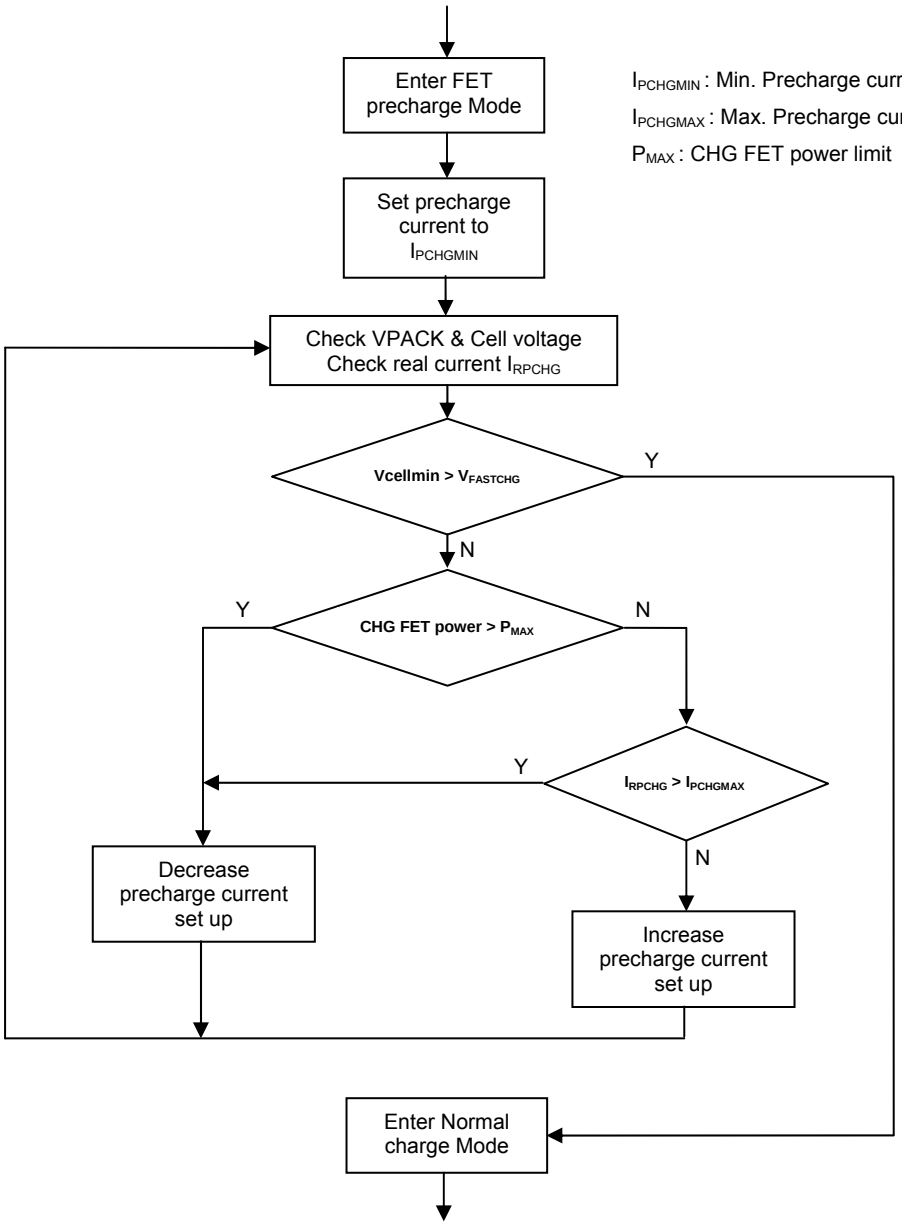
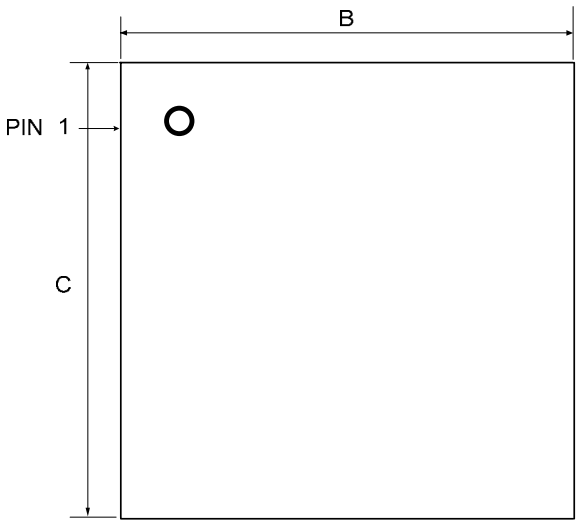


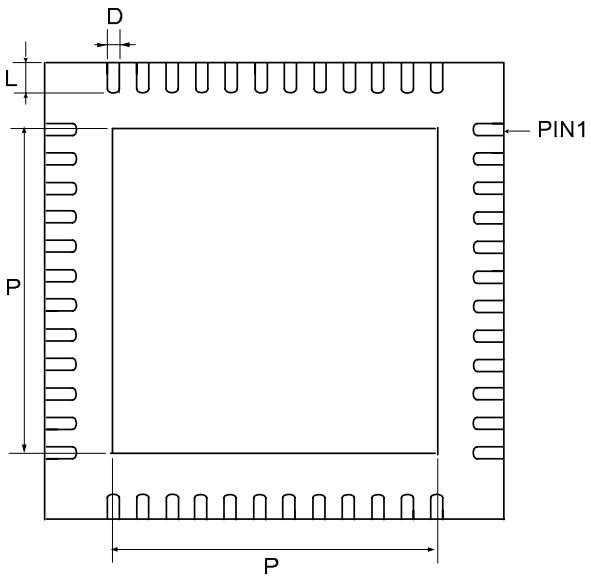
Fig. 3 OZ930 Main FET Precharge mode control flow

QFN 48 PACKAGE INFORMATION

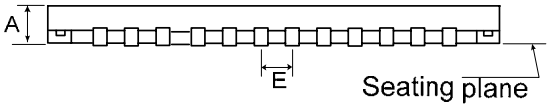
7x7mm 48Ld QFN Package Outline Drawing



Top View



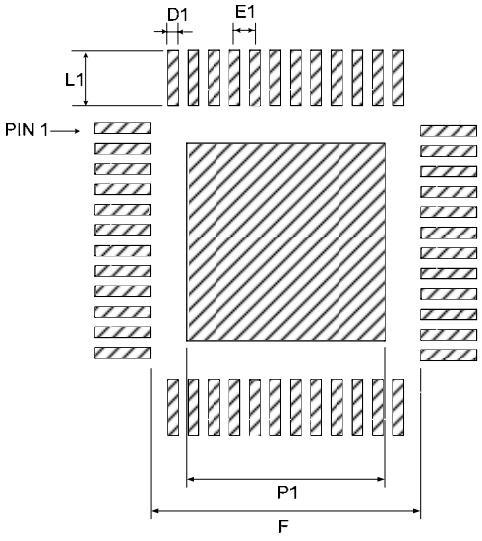
Bottom View



Side View

O2Micro Dimension Table			
SYMBOL	SPECIFICATION IN mm		
Pitch 0.50	Min	Nom	Max
A			1.00
B		7.00	
C		7.00	
D	0.18	.25	.30
E		.50	
L	0.30	0.40	0.50
P	4.90	5.05	5.80
D1		0.25	
E1		0.50	
L1		0.80	
P1		5.00	
F		5.80	

Landing Pattern



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