NT53101

Preliminary

65×132 RAM-MAP LCD Controller/Driver

Features

- Direct RAM data display using the display RAM. When RAM data bit is 0, it is not displayed. When RAM data bit is 1, it is displayed. (At normal display)
- RAM capacity: 65 × 132 = 8580 bits
- Many command functions: Read/Write Display Data. Display ON/OFF. Normal/Reverse Display. Page Address Set. Set Display Start Line. Set LCD Bias, Electronic contrast Controls, Read Modify Write, Select Segment Driver Direction, Power Save
- High-speed 8-bit microprocessor interface allowing direct connection to 6502.
- Single supply operation, 2.4 – 5.1V
- Maximum 12V LCD driving output voltage
- 2X / 3X / 4X / 5X on chip DC-DC converter
- Voltage regulator
- Voltage follower
- On chip oscillator

General Description

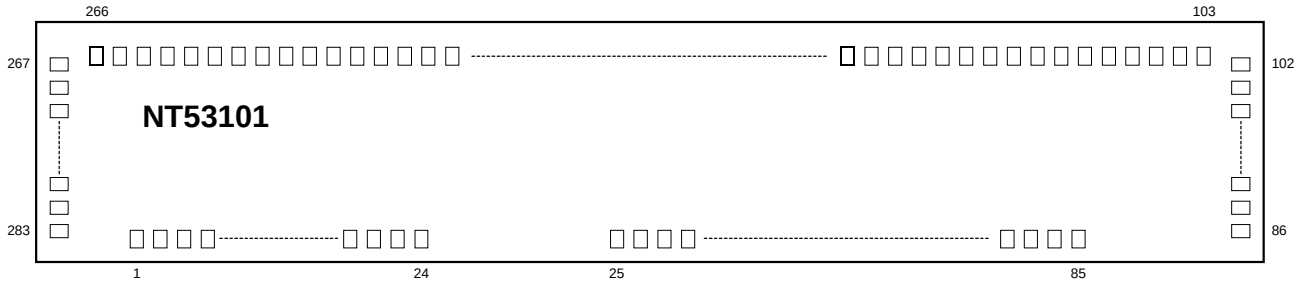
The NT53101 is a single-chip LCD driver for dot-matrix liquid crystal displays, which is directly connectable to a microcomputer bus. It accepts 8-bit parallel display data directly sent from a microcomputer and stores it in an on-chip display RAM. It generates a LCD drive signal independent of microprocessor clock.

The set of the on-chip display RAM of 65 × 132 bits and a one-to-one correspondence between LCD panel pixel dots and on-chip RAM bits permits implementation of displays with a high degree of freedom.

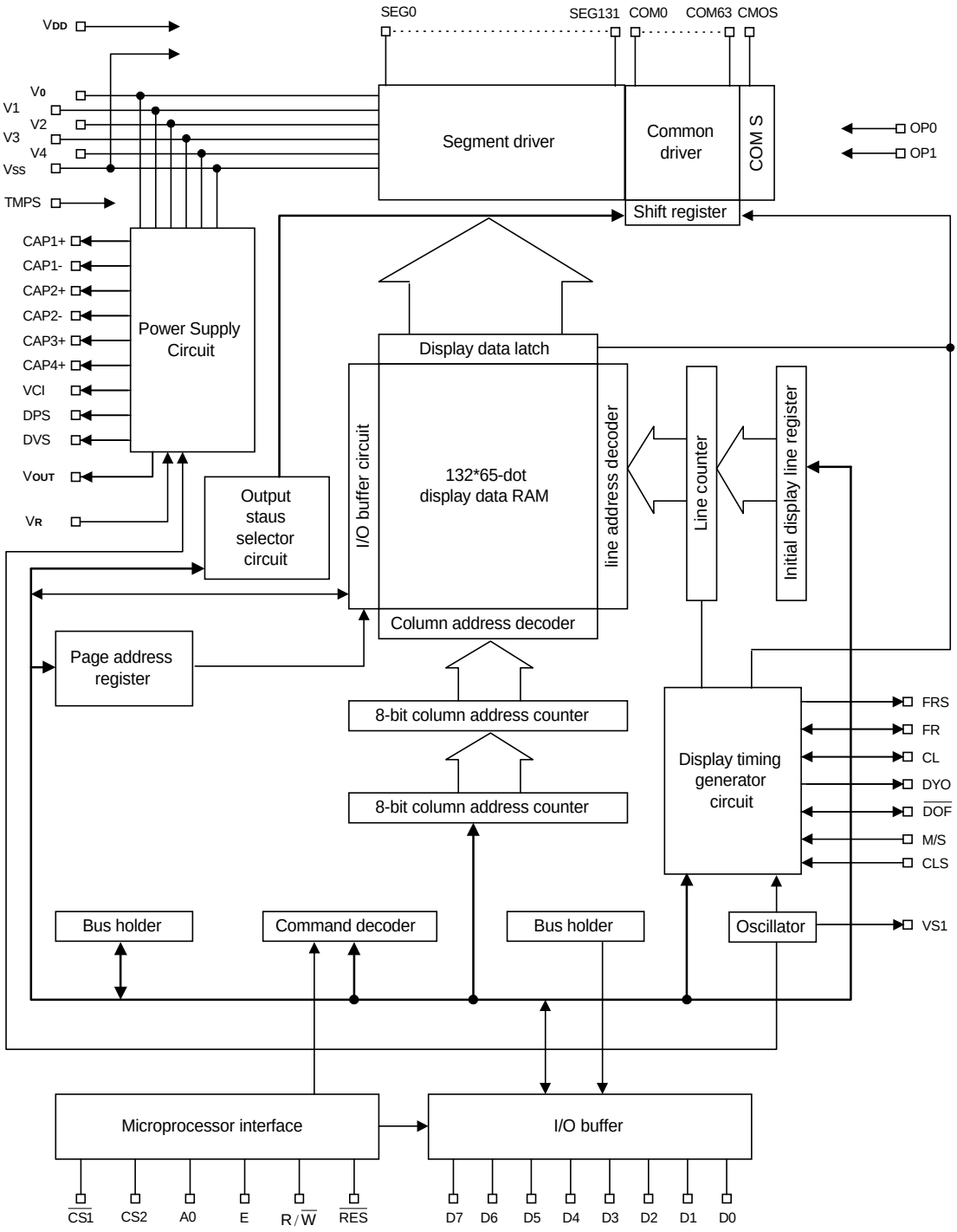
a single chip of NT53101 can make 65 x 132, 55 x132, 49x132 and 33 x 132 dots displays with pad option (OP1, OP0)

No external operation clock is required for RAM read/write operations. Accordingly, this driver can be operated with a minimum current consumption and its on-board low-current-consumption liquid crystal power supply can implement a high-performance handy display system with a minimum current consumption and a smallest LSI configuration.

Pad Configuration



Block Diagram



Pad Description

Power Supply

Pad No.	Symbol	I/O	Description
25~28	V_{DD}	Supply	2.4 – 5.1V power supply for digital circuit. Connect to microprocessor power supply pin V_{CC} These pads must be connected each other.
35~38	V_{SS}	Supply	Ground for digital circuit. These pads must be connected each other.
29~32	V_{DD}	Supply	2.4 – 5.1V power supply for analog circuit. Connect to microprocessor power supply pin V_{CC} These pads must be connected each other.
39~42	V_{SS}	Supply	Ground for analog circuit. These pads must be connected each other.
11, 65~66, 80, 85	V_{DD}	Supply	2.4 – 5.1V power supply. These pads were connected to digital or analog V_{DD} internally.
9, 13, 63~64, 77~78, 82	V_{SS}	Supply	Ground. These pads were connected to digital or analog V_{SS} internally.
59~60, 67~68	V_0	Supply	LCD driver supply voltages. The voltage determined by LCD cell is impedance-converted by a resistive driver or an operation amplifier for application. Voltages should be the following relationship: $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$ When the on-chip operating power circuit is on, the following voltages are given to V_1 to V_4 by the on-chip power circuit. Voltage selection is performed by the Set LCD Bias command.
69~70	V_1		
71~72	V_2		
73~74	V_3		
75~76	V_4		

LCD Driver Supplies

Pad No.	Symbol	I/O	Description
51~52	CAP1+	O	Capacitor 1+ pad for DC/DC voltage converter.
49~50	CAP1-	O	Capacitor 1- pad for DC/DC voltage converter.
55~56	CAP2+	O	Capacitor 2+ pad for DC/DC voltage converter.
53~54	CAP2-	O	Capacitor 2- pad for DC/DC voltage converter.
47~48	CAP3+	O	Capacitor 3+ pad for DC/DC voltage converter.
45~46	CAP4+	O	Capacitor 4+ pad for DC/DC voltage converter.
43~44	VCI	O	Internal power supply voltage for DC/DC voltage converter.
33	DPS	I	Select the power of DC/DC converter DPS = 0: Select VCI = 2.7V or 2.2V (depend on DVS = 0 or 1) DPS = 1: Select VCI = VDD
34	DVS	I	Select the VCI output voltage DVS = 0: 2.7V (when V_{DD} >2.7V); V_{DD} (when $V_{DD} \leq$ 2.7V) DVS = 1: 2.2V
57~58	V_{OUT}	O	DC/DC voltage converter output
61~62	V_R	I	Voltage adjustment pad. Applies voltage between V_0 and V_{SS} using a resistive divider.
79	TMPS	I	Selects temperature coefficient of the reference voltage TMPS = 0: -0.01% / °C TMPS = 1: -0.2 % / °C

System Bus Connection Terminals

Pad No.	Symbol	I/O	Description
17~24	D0 – D7	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit standard MPU data bus. When the chip select is inactive, D0 to D7 are set to high impedance.
14	A0	I	This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0="H": Indicate that D0 to D7 are display data. A0="L": Indicates that D0 to D7 are control data.
8	$\overline{RES}$	I	When $\overline{RES}$ is set to "L", the settings are initialized. The reset operation is performed by the $\overline{RES}$ signal level.
10, 12	$\overline{CS1}$, CS2	I	This is the chip select signal. When $\overline{CS1}$="L", CS2=1 then the chip select becomes active,and data/command I/O is enabled
16	E	I	When connected to a 6502 Series MPU , this is active HIGH. This is the 6502 series MPU enable clock input terminal.
15	R/$\overline{W}$	I	When connected to a 6502 series MPU: This is the read/write control signal input terminal. When R/$\overline{W}$ ="H": Read; When R/$\overline{W}$ ="L": Write.
7	M/S	I	This terminal selects the master/slave operation for the NT53101 chips. Master operation outputs the timing signals that are required for the LCD display, while slave operation inputs the timing signals require for the liquid crystal display, synchronizing the liquid crystal display system.
4	CL	I/O	This is the display clock input terminal When the NT53101 chips are used in master/slave mode, the various CL terminals must be connected
81	CLS	I	Select whether enable or disable the display clock internal oscillator circuit. CLS="H": Internal oscillator circuit is enabled CLS="L": Internal oscillator circuit is disabled (requires external input) When CLS="L", input the display clock through the CL pad
2	FR	I/O	This is the liquid crystal alternating current signal I/O terminal. M/S="H": Output M/S="L": Input When the NT53101 chip is used in master/slave mode, the various FR terminals must be connected.
3	DYO	O	Common drive signal output. This output is enabled for only at master operation and connects to the common driver DIO pad. It becomes HZ at slave operation.
6	VS1	O	Internal power supply voltage monitor output.
5	$\overline{DOF}$	I/O	This is the liquid crystal display blanking control terminal. M/S="H": Output M/S="L": Input When the NT53101 chip is used in master/slave mode, the various $\overline{DOF}$ terminals must be connected
1	FRS	O	This is the output terminal for the static drive. This terminal is only enabled when the static indicator display is ON when in master operation mode, and is used in conjunction with the FR terminal.

Liquid Crystal Drive Pins

Pad No.	Symbol	I/O	Description
119-250	SEG0 - 131	O	Segment signal output for LCD display
117~86 251-282	COM0~31 COM32 - 63	O	Common signal output for LCD display. When in master/slave mode, the same signal is output by both master and slave.
118, 283	COMS	O	Common signal output for LCD display. When in master/slave mode, the same signal is output by both master and slave.

Configuration Pin

Pad No.	Symbol	I/O	Description
83, 84	OP0, OP1	I	Configuration Setting, select the output as 65, 55, 49, 32 duty

Functional Description

Microprocessor Interface

The NT53101 identifies the data bus signal according to A0, E, R / $\overline{W}$ signals.

A0	R / $\overline{W}$	Function
1	1	Reads display data.
1	0	Writes display data.
0	1	Reads status.
0	0	Writes control data in internal register. (Command)

Chip Select Inputs

The NT53101 has two chip select pads, $\overline{CS1}$ and CS2 can interface to a microprocessor when $\overline{CS1}$ is low and CS2 is high. When these pads are set to any other combination. D0 to D7 are in high impedance and A0, E and R / $\overline{W}$ inputs are disabled.

Access to Display Data RAM and Internal Registers

The NT53101 can perform a series of pipeline processing between LSI's using bus holder of internal data bus in order to match the operating frequency of display RAM and internal registers with the microprocessor. For example, the microprocessor reads data from display RAM in the first read (dummy) cycle, stores it in bus holder, and outputs it onto system bus in the next data read cycle.
Also, the microprocessor temporarily stores display data in bus holder, and stores it in display RAM until the next data write cycle starts.
When viewed from the microprocessor, the NT53101 access speed greatly depends on the cycle time rather than access time to the display RAM (t_{ACC}). It shows the data transfer speed to/from the microprocessor can increase. If the cycle time is inappropriate, the microprocessor can insert the NOP instruction that is equivalent to the wait cycle setup. However, there is a restriction in the display RAM read sequence. When an address is set, the specified address data is NOT output at the immediately following read instruction. The address data is output during second data read. A single dummy read must be inserted after address setup and after write cycle (refer to Figure1).

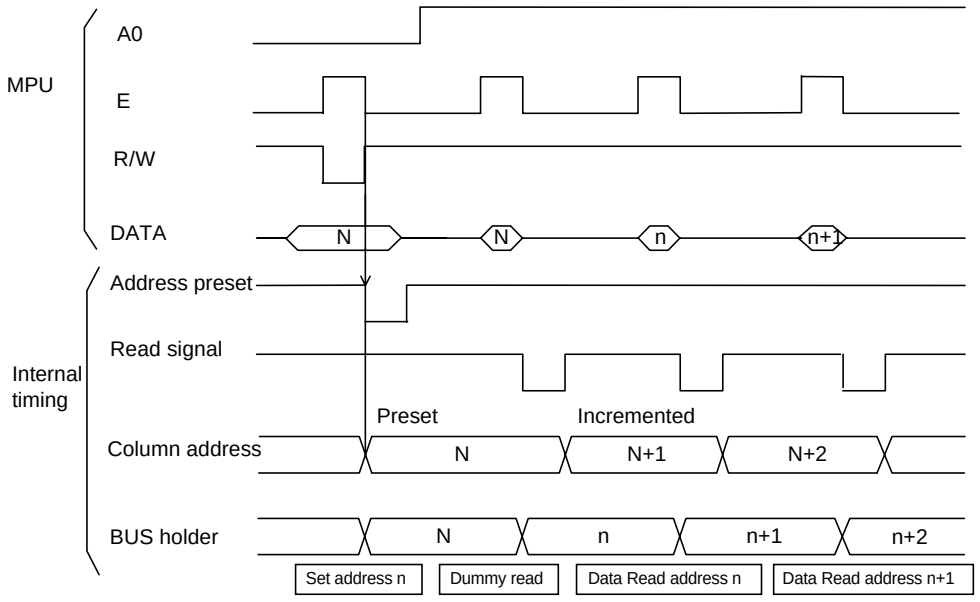


Figure 1

Busy Flag

The Busy flag is set when the NT53101 starts to operate. During operating, it accepts Read Status instruction only. The busy flag signal is output at pin D7 when Read Status is issued. If the cycle time (t_{CYC}) is correct, the microprocessor needs not to check the flag before issuing a command. This can greatly improve the microprocessor performance.

Initial Display Line Register

When the display RAM data is read, the display line according to COM0 (usually, the top line of screen) is determined using register data. The register is also used for screen scrolling and page switching.
The set Display Start Line command sets the 6-bit display start address in this register. The register data is preset on the line counter each time FR signal status changes. The line counter is incremental by CL signal and it generates a line address to allow 132 bit.

Column Address Counter

This is a 8 bit presettable counter that provides column address to the display RAM (refer to Figure2). It is incremental by 1 when a Read/Write command is entered. However, the counter is not incremental but locked if a non-existing address above 84H is specified. It is unlocked when a column address is set again. The Column Address counter is independent of Page Address register.
When ADC Select command is issued to display inverse display, the column address decoder inverts the relationship between RAM column address and display segment output.

Page Address Register

This is a 4-bit page address register that provides page address to the display RAM (refer to Figure 2). The microprocessor issues Set Page Address command to change the page and access to another page. Page address 8 (D3 is high, but D2,D1 and D0 are low) is RAM area dedicate to the indicator, and display data D0 is only valid.

Relationship between display data RAM and address (if initial display line is 21H)

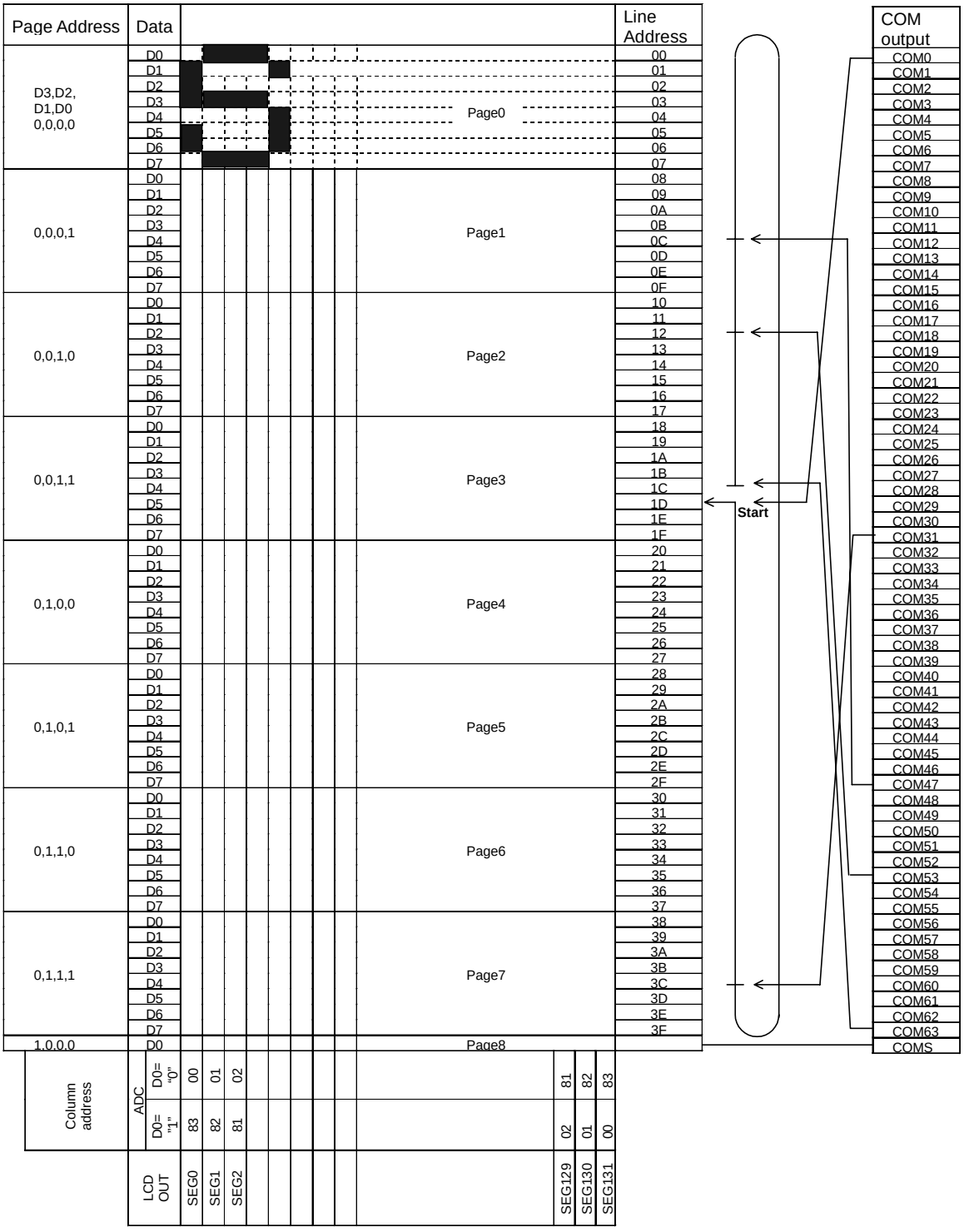


Figure 2

Display Data RAM

The display data RAM stores pixel data for LCD. It is a 65-column by 132-row (8-page by 8 bit+1) addressable array. Each pixel can be selected when page and column addresses are specified.
The time required to transfer data is very short because the microprocessor enters D0 to D7 corresponding to LCD common lines as shown in Figure 3. Therefore, multiple NT53101's can easily configure a large display having the high flexibility with very few data transmission restriction.
The microprocessor writes and reads data to/from the RAM through I/O buffer. As LCD controller operates independently, data can be written into RAM at the same time as data is being displayed, without causing the LCD to flicker.

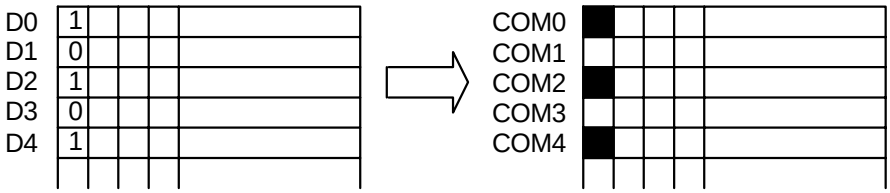


Figure 3

Display Timing Generator

This section explains how the display timing generator circuit operates.

Signal generation to line counter and display data latch circuit

The display clock (CL) generates a clock to the line counter and a latch signal to the display data latch circuit.
The line address of the display RAM is generated in synchronization with the display clock. 132-bit display data is latched by the display data latch circuit in synchronization with the display clock and output to the segment LCD drive output pin.
The display data is read to the LCD drive circuit completely independent of access to the display data RAM from the microprocessor.

LCD AC signal (FR) generation

The display clock generates an LCD AC signal (FR). The FR causes the LCD drive circuit to generate a AC drive waveform. It generates a 2-frame AC drive waveform.
When the NT53101 is operated in slave mode on the assumption of multi-chip, the FR pin and CL pin become input pins.

Common timing signal generation

The display clock generates an internal common timing signal and a start signal (DYO) to the common driver. A display clock resulting from frequency division of an oscillation clock is output from the CL pin.
When an AC signal (FR) is switched, a high pulse is output as a DYO output at the training edge of the previous display clock. Refer to Fig.6. The DYO output is output only in master mode.
When the NT53101 is used for multi-chip, the slave requires to receive the FR, CL, $\overline{DOF}$ signals from the master.

Operating Mode		FR	CL	$\overline{DOF}$
Master (M/S="H")	The internal oscillator circuit is enabled (CLS="H")	Output	Output	Output
	The internal oscillator circuit is disabled (CLS="L")	Output	Input	Output
Slave (M/S="L")	The internal oscillator circuit is disabled (CLS="H")	Input	Input	Input
	The internal oscillator circuit is disabled (CLS="L")	Input	Input	Input

The relationship between oscillation frequency and frame frequency

Duty	Item	f_{CL}	f_{FR}
1/65	On-chip oscillator is used	fosc/6	$f_{CL}/(2\times65)$
	On-chip oscillator is not used	External input f_{CL}	$f_{CL}/(2\times65)$
1/55	On-chip oscillator is used	fosc/8	$f_{CL}/(2\times55)$
	On-chip oscillator is not used	External input f_{CL}	$f_{CL}/(2\times55)$
1/49	On-chip oscillator is used	fosc/8	$f_{CL}/(2\times49)$
	On-chip oscillator is not used	External input f_{CL}	$f_{CL}/(2\times49)$
1/33	On-chip oscillator is used	fosc/12	$f_{CL}/(2\times33)$
	On-chip oscillator is not used	External input f_{CL}	$f_{CL}/(2\times33)$

Example of NT53101 1/65 duty (Dual-frame AC driver waveforms)

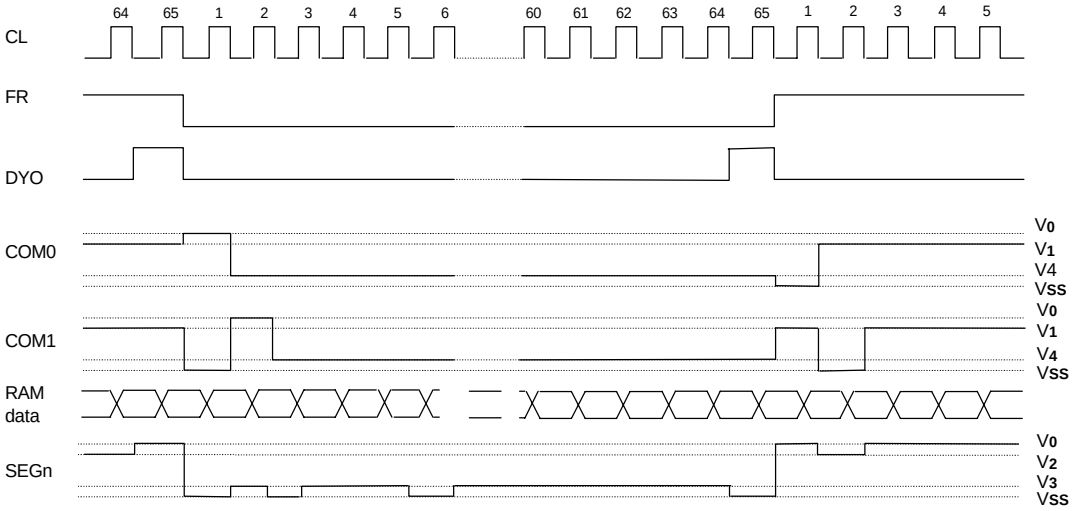


Figure 4

Display Data Latch Circuit

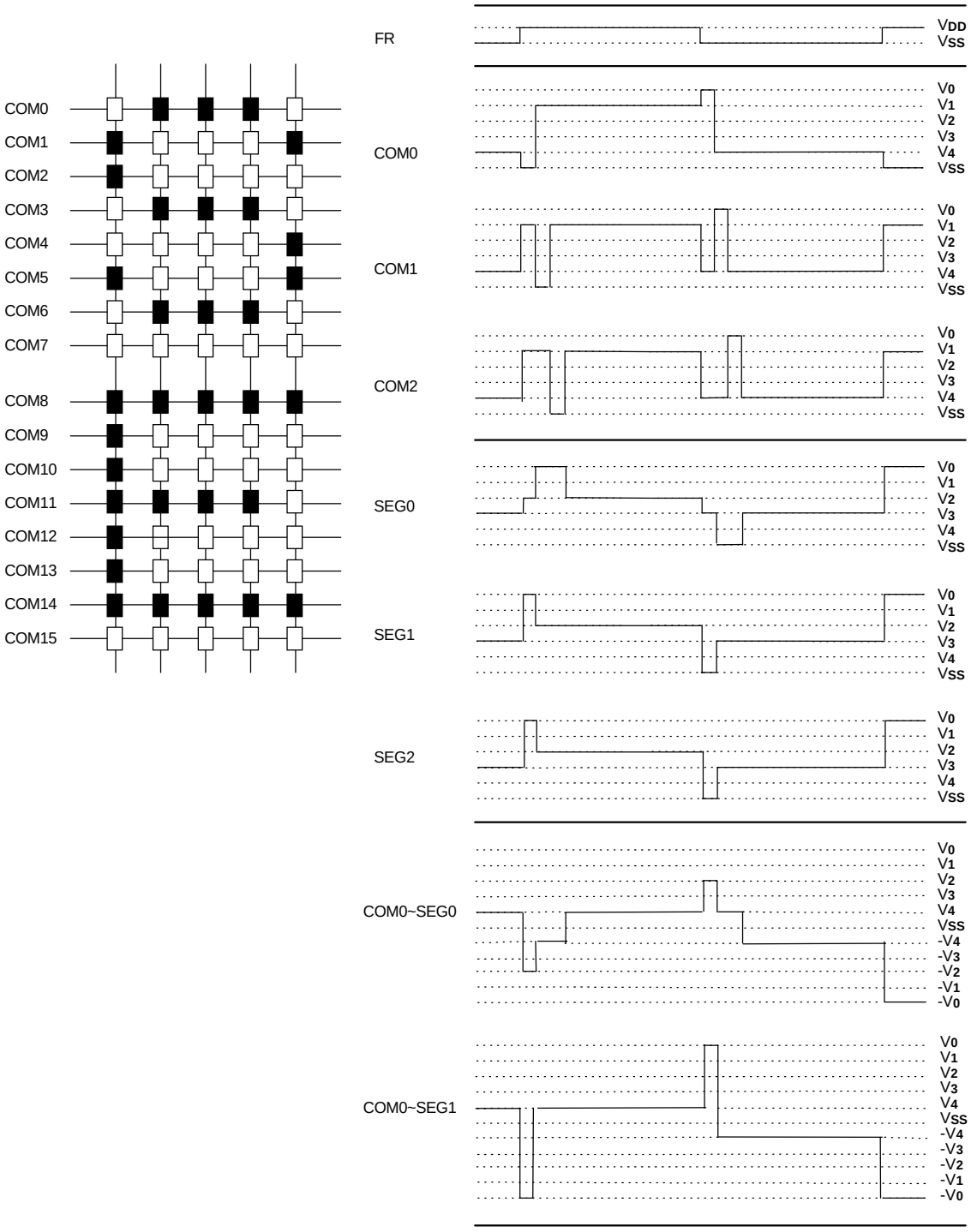
This circuit temporarily stores (or latches) display data (during a single common signal period) when it is output from display RAM to LCD panel driver circuit. This latch is controlled by Display in normal/reverse Display ON/OFF and Entire display on commands. These commands do not alter the data.

LCD Driver

This is a multiplexer circuit consisting of 132 segment outputs to generate four-level LCD panel drive signals. The LCD panel drive voltage is generated by a specific combination of display data, COM scan signal, and FR signal. Figure 5 gives an example of SEG and COM output waveform.

Oscillator Circuit

This is an oscillator having a complete built-in type CR, and its output is used as the display timing signal source or as the clock for voltage booster circuit of the LCD power supply.
The oscillator circuit is available in master mode only.
The oscillator signal is divided and output as display clock at CL pad


COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
FR
VDD
VSS
COM0
V0
V1
V2
V3
V4
VSS
COM1
V0
V1
V2
V3
V4
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COM0~SEG0
V0
V1
V2
V3
V4
VSS
-V4
-V3
-V2
-V1
-V0
COM0~SEG1
V0
V1
V2
V3
V4
VSS
-V4
-V3
-V2
-V1
-V0

Figure 5

Configuration Setting

The NT53101 can be optional into two configuration by OP1, OP0

OP1, OP0	Duty	V1	V2	V3	V4
0, 0	65	8/9V0, 6/7V0	7/9V0, 5/7V0	2/9V0, 2/7 V0	1/9V0, 1/7V0
0, 1	55	7/8V0, 5/6V0	6/8V0, 4/6V0	2/8V0, 2/6 V0	1/8V0, 1/6V0
1, 0	49	7/8V0, 5/6V0	6/8V0, 4/6V0	2/8V0, 2/6 V0	1/8V0, 1/6V0
1, 1	33	5/6V0, 4/5V0	4/6V0, 3/5V0	2/6 V0, 2/5V0	1/6V0, 1/5V0

Common Output Control Circuit

This circuit controls the relationship between the number of common output and specified duty ratio. Common output mode select instruction specifies the scanning direction of the common output pads.

Duty	**Status**	**Common output pads**							
		COM [0-15]	**COM [16-23]**	**COM [24-26]**	**COM [27-36]**	**COM [37-39]**	**COM [40-47]**	**COM [48-63]**	**COMS**
1/33	Normal	COM[0-15]	NC					COM[16-31]	COMS
	Reverse	COM[31-16]	NC					COM[15-0]	
1/49	Normal	COM[0-23]		NC			COM[24-47]		COMS
	Reverse	COM[47-24]		NC			COM[23-0]		
1/55	Normal	COM[0-26]			NC	COM[27-53]			COMS
	Reverse	COM[53-27]			NC	COM[26-0]			
1/65	Normal	COM[0-63]							COMS
	Reverse	COM[63-0]							

Power Supply Circuit

The power supply circuit generates voltage to drive the LCD panel at low power consumption, and is available in NT53101 master mode only. The power supply circuit consists of a voltage booster, voltage regulator and LCD drive voltage follower.
The power supply circuit built in the NT53101 is set for a small-scale LCD panel and is inappropriate to a large-pixel panel and a large-display-capacity LCD panel using multiple chips. As the large LCD panel has the dropped display quality due to a large load capacity, it must use an external power source.
The power circuit is controlled by Set Power Control command. This command sets a three-bit data in Power Control register to select one of eight power circuit functions. The external power supply and part of internal power circuit functions can be used simultaneously. The following explains how the Set Power Control command works.

[Control by Set Power Control command]
D2 turns on when voltage booster control bit goes high, and D2 turns off when this bit goes low.
D1 turns on when voltage regulator control bit goes high, and D1 turns off when this bit goes low.
D0 turns on when voltage follower control bit goes high, and D0 turns off when this bit goes low.

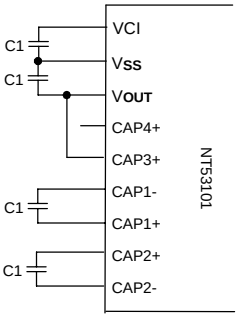
[Practical combination examples]
Status 1: To use only the internal power supply.
Status 2: To use only the voltage regulator and voltage follower
Status 3: To use only the voltage follower, input the external voltage as $V_0=V_{OUT}$
Status 4: To use only an external power supply because the internal power supply does not operate.

	D2	D1	D0	Voltage booster	Voltage regulator	Voltage follower	External voltage input	Voltage booster terminal	Voltage regulator terminal
1	1	1	1	ON	ON	ON	-	Used	Used
2	0	1	1	OFF	ON	ON	VOUT	OPEN	Used
3	0	0	1	OFF	OFF	ON	V0	OPEN	OPEN
4	0	0	0	OFF	OFF	OFF	V0 to V4	OPEN	OPEN

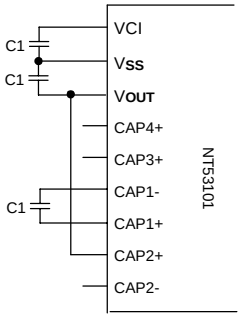
*The voltage booster terminals are CAP1+, CAP1-, CAP2+, CAP2-, CAP3+ and CAP4+
*Combinations other than those shown in the above table are possible but impractical.

Booster circuit

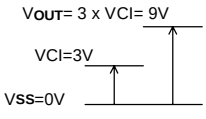
These circuits boost up the electric potential between VCI and Vss to 2, 3, 4, 5 times toward positive side and boosted voltage is outputted from VOUT pad.
* The VCI voltage range must be set so that the VOUT voltage does not exceed the absolute maximum rated value.
As the booster circuit uses signals from the oscillator circuit, the oscillator circuit must operate.



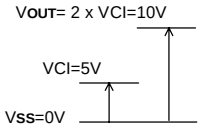
3x step-up voltage circuit



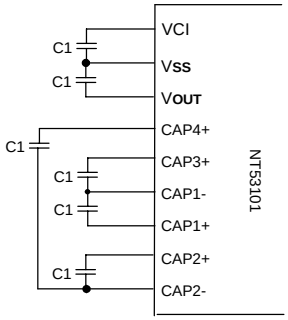
2x step-up voltage circuit



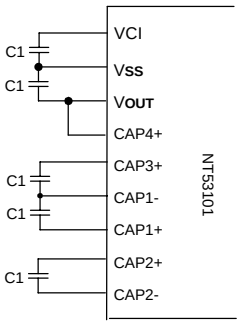
3x step-up voltage relationships



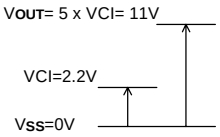
2x step-up voltage relationships



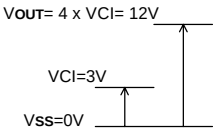
5x step-up voltage circuit



4x step-up voltage circuit



5x step-up voltage relationships



4x step-up voltage relationships

C1 = 1.0 to 4.7 μF

Figure 6

Voltage regulator circuit

The function of the internal voltage regulator circuits is to determine liquid crystal operating voltage V_0 by adjusting resistors R_a and R_b, within the range of $V_0 < V_{OUT}$. VOUT is the operating voltage of operational amplifier circuits shown in figure 7.

Feedback gain control for initial LCD voltage. External resistors are connected between V_0 and V_R, and between V_R and V_{SS}. These resistors are chosen to give the desired V_0 according to the following equation:

$$V_0 = (1+ R_b/R_a) \times V_{REG} + R_b \times I_{ref}$$

Voltage regulator using the Electronic Volume Control Function

The Electronic Volume Control Function can adjust the intensity (brightness level) of LCD screen by electronic control command.

Software control of 32 voltage levels of V_0. It gives the following equation:

$$V_0 = (1+ R_b/R_a) \times V_{REG} + R_b \times I_{ref}$$

Where I_{ref} = 0 to 6.5μA ± 40% depending on the 5-bit data set by the electronic control command.

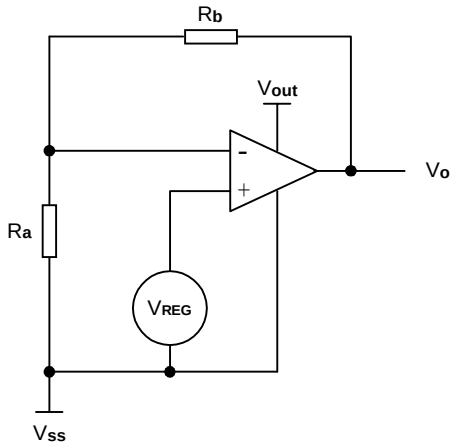


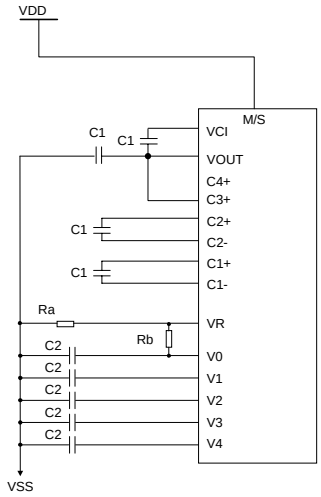
Figure 7

Reference power supply circuit for driving LCD panel

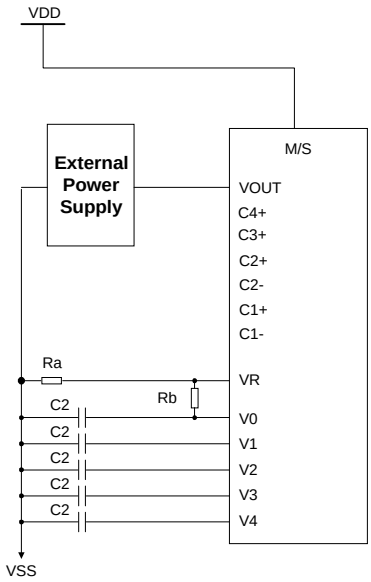
-When using all LCD power circuits

(Voltage converter regulator and follower)

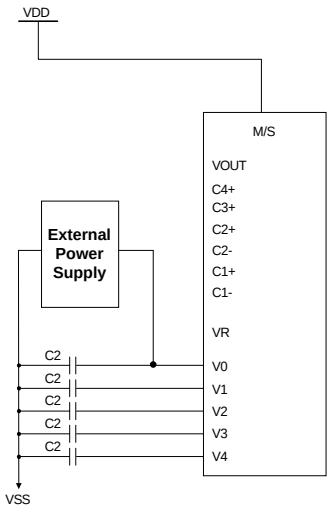
(In case of 3X boosting circuit)



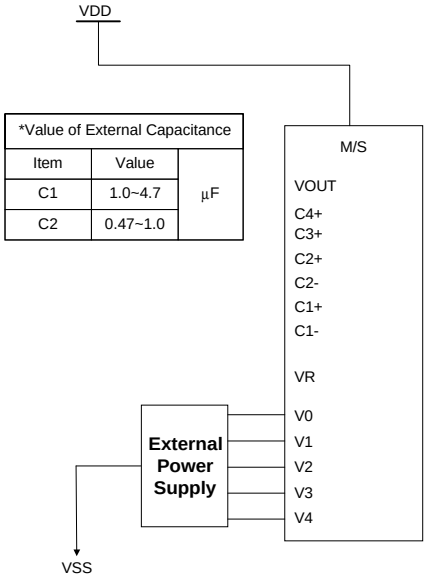
-When not using voltage booster circuits



When only using voltage follower

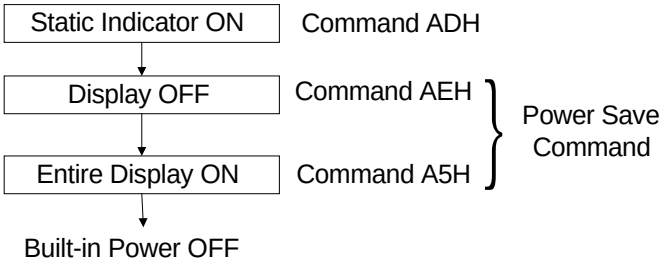


When not using internal LCD power supply circuits



Command Sequence when Built-in Power Supply is Turned OFF

To turn off the built-in power supply, follow the command sequence as shown below to turn it off after making the system into the standby mode.



Reset Circuit

When the RES input goes low, this LSI is initialized.

Initialized status

1. Display OFF
2. Normal display
3. ADC select: Normal display (ADC command D0 = 0)
4. Read modify write OFF
5. Power control register (D2, D1, D0)=(0, 0, 0,)
6. LCD power supply bias ratio 1/9 (1/65duty); 1/8 (1/55duty), 1/8 (1/49duty); 1/6 (1/33duty)
7. Static indicator: OFF
8. Display start line register set at first line
9. Column address counter set at address0
10. Page address register set at page 0
11. Output status register (D3)=(0)
12. Electronic control register set at 0
13. Test command OFF

As seen in Microprocessor Interface (Reference Example). Connect the $\overline{RES}$ pad to the reset pin of the microprocessor and initialize the microprocessor at the same time.

In case the NT53101 does not use the internal LCD power supply circuit, the $\overline{RES}$ must be low when the external LCD power supply is turned on.

When $\overline{RES}$ goes low, each register is cleared and set to the above initialized status. However, it has no effect on the oscillator circuit and output pads (FR, CL, DYO, D0 to D7)

The initialization by $\overline{RES}$ pad signal is always required during power-on. If the control signal from the MPU is HZ, an overcurrent may flow through the IC. A protection is required to prevent the HZ signal at the input pads during power-on.

Be sure to initialize it by $\overline{RES}$ pad when turning on the power supply. When the reset command is used, only parameters 7 to 13 in the above initialization are executed.

COMMANDS

The NT53101 uses a combination of A0, E and $R/\overline{W}$ signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 6502 series microprocessor interface enters a read status when a high pulse is input to the $R/\overline{W}$ pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.). Accordingly, in the command explanation and command table, E and $R/\overline{W}$ becomes 1(high) when the 6502 series microprocessor interface reads status of display data.

Command set

1. Display ON/OFF

   Alternatively turns the display on and off.

A0	E	$R/\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

   The display turns off when D goes low and it turn on when D goes high.

2. Set Display Start Line

   Specifies line address (refer to Figure 2) to determine the initial display line, or COM0. The RAM display data becomes the top line of LCD screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

A0	E	$R/\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

← High-order bit

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
			:			:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

3. Set Page Address

Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed. Page address 8 is the display RAM area dedicate to the indicator, and only D0 is valid for data change.

A0	E	R / $\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Page address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

4. Set Column Address

Specifies column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them succession. When the microprocessor repeats to access to the display RAM, the column address counter is incremental by during each access until address 132 is accessed. The page address is not changed during this time.

	A0	E	R / $\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
Higher bits	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				:				:
1	0	0	0	0	0	1	1	131

5. Read Status

A0	E	R / $\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY: When high, the NT53101 is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

ADC: Indicates the relationship between RAM column address and segment drivers. When low, the display is reversed and column address “100-n” corresponds to segment driver n. When high, the display is normal and column address corresponds to segment driver n.

ON/OFF: Indicates whether the display is on or off. When goes low the display turns on. When goes high, the display turns off. This is the opposite of Display ON/OFF command

RESET: Indicates the initialization is in progress by $\overline{RES}$ signal or by reset command. When low, the chip is in operating state. When high, the chip is being reset.

6. Write Display Data

Write 8-bit data in display RAM. As the column address is incremental by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	E	R / $\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

7. Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address is increment by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details.

A0	E	R / $\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	Read data							

8. ADC Select

Changes the relationship between RAM column address and segment driver. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of Figure2. When display data is written or read, the column address is incremental by 1 as shown in Figure2.

A0	E	R / $\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

D = 0: Normal direction D = 1: Reverse direction

9. Normal/ Reverse Display

Reverses the Display ON/OFF status without rewriting the contents of the display data RAM.

A0	E	R / $\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

D = 0: Normal display D = 1: Reverse display

10. Entire Display ON

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.
This command has priority over the Normal/Reverse Display command. When D is low, the normal display status is provided.

A0	E	R / $\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D is high, the entire display ON status is provided. If the Entire Display ON command is executed in the display OFF status, the LCD panel enters Power Save mode. Refer to the Power Save section for details.

11. Set LCD Bias

Selects a bias ratio of the voltage required for driving the LCD. This command is enabled when the voltage follower in the power supply circuit operates.

A0	E	R / $\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	1	D

The potential V0 is resistively divided inside the IC to produce potentials V1, V2, V3 and V4 which are necessary to drive the LCD. The bias ratio can be selected using the LCD bias setting command.
Moreover, the potentials V1, V2, V3 and V4 are converted in the impedance and supplied to the LCD drive circuit.

Bias ratio of LCD power supply	Duty			
	65	55	49	33
D = 0	1/9 bias	1/8 bias	1/8 bias	1/6 bias
D = 1	1/7 bias	1/6 bias	1/6 bias	1/5 bias

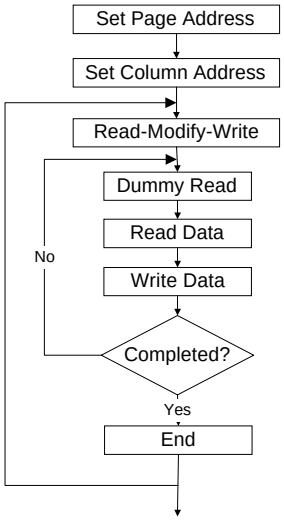
12. Read-Modify-Write

A pair of Read-Modify-Write and End commands must always be used. Once Read-Modity-Write is issued, column address is not incremental by Read Display Data command but incremental by Write Display Data command only. It continues until End command is issued. When the End is issued, column address returns to the address when Read-Modify-Write was issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	E	R / $\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note: Any command except Read/Write Display Data and Set Column Address can be issued during Read-Modify-Write mode.

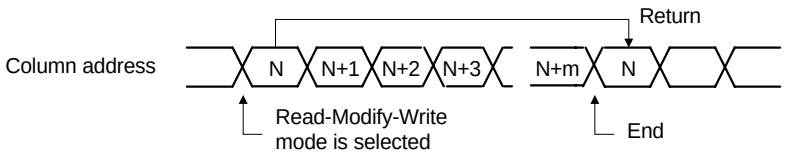
Cursor display sequence



13. End

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write was issued.)

A0	E	R / $\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



14. Reset

Resets the Initial Display Line register, Column Address counter, Page Address register, and output status selector circuit to their initial status. The Reset command does not affect on the contents of display RAM. Refer to the Reset circuit section of FUNCTIONAL DESCRIPTION.

A0	E	R / $\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The Reset command cannot initialize LCD power supply. Only the Reset signal to the $\overline{RES}$ pad can initialize the supplies.

15. Output Status Select Register

Applicable to the NT53101. When D is high or low, the scan direction of the COM output pad is selectable. Refer to Output Status Selector Circuit in Function Description for details.

A0	E	R / $\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

D : Selects the scan direction of COM output pad
D=0: Normal (COM0 → COM64/54/47/33) D=1: Reverse (COM64/55/47/33 → COM0)
*: Invalid bit

16. Set Power Control

Selects one of eight power circuit functions using 3-bit register. An external power supply and part of on-chip power circuit can be used simultaneously. Refer to Power Supply Circuit section of FUNCTIONAL DESCRIPTION for details.

A0	E	R / $\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	A2	A1	A0

When A0 goes low, voltage follower turns off. When A0 goes high, it turns on.
When A1 goes low, voltage regulator turns off. When A1 goes high, it turns on
When A2 goes low, voltage booster turns off. When A2 goes high, it turns on.

17. Set Electronic Control

Adjusts the contrast of LCD panel display by changing V_0 LCD drive voltage that is output by voltage regulator of on-board power supply.
This command selects one of 32 V_0 LCD drive voltages by storing data in 5-bit register. The V_0 voltage adjusting range should be determined depending on the external resistance. Refer to the Voltage Regulator section of FUNCTIONAL DESCRIPTION for details.

A0	E	R / $\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	A4	A3	A2	A1	A0

A4	A3	A2	A1	A0	I V0 I
0	0	0	0	0	LOW
0	0	0	0	1	
0	0	0	1	0	
		:			↓
1	1	1	0	1	
1	1	1	1	0	
1	1	1	1	1	High

Set register to (D4, D3, D2, D1,D0)=(0, 0, 0, 0, 0) to suppress electronic control function.

18. Static Indicator

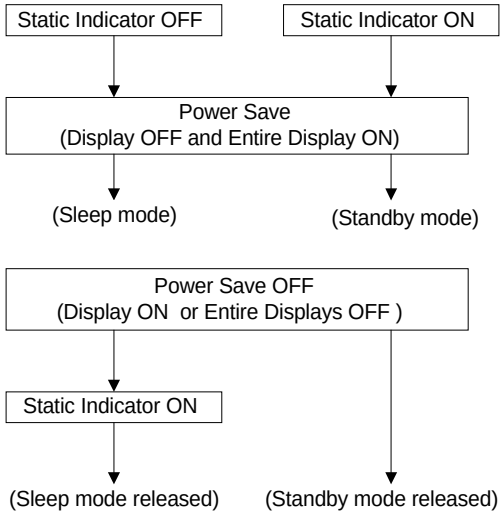
This command turns on or off static drive indicators. The indicator display is controlled by this command only, and it is not affected by the other display control commands.
Either FR or FRS terminal is connected to either of static indicator LCD drive electrodes, and the remaining terminal is connected to another electrode. When the indicator is turned on, the static drive operates and the indicator blinks at an interval of approximately one second. The pattern separation between indicator electrodes are dynamic drive electrodes is recommended. A closer pattern may cause an LCD and electrode deterioration.

A0	E	$R/\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	D

D = 0: Static indicator OFF
D = 1: Static indicator ON

19. Power Save (Compound Command)

When all displays are turned on during display off, the Power Save command is issued to greatly reduce the current consumption.
If the static indicators are off, the Power Save command sleeps the system. If on, this command stands by the system.
Release the Sleep mode using the both Power Save OFF command (Display ON command or Entire Display OFF command) and Static Indicator ON command.
Release the Sleep mode using the Power Save OFF command (Display ON command or Entire Displays OFF command) and Static Indicator ON command.
Release the Standby mode using the Power Save OFF command (Display ON command or Entire Displays OFF command).



Sleep mode
This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:
(1) Stops the oscillator circuit and LCD power supply circuit.
(2) Stops the LCD drive and outputs the Vss as the segment/common driver output.
(3) Holds the display data and operation mode provided before the start of the sleep mode.
(4) The MPU can access to the built-in display RAM.

Standby mode
Stops the operation of the duty LCD display system and turns on only the static drive system to reduce current consumption to the minimum level required for static drive.
The ON operation of the static drive system indicates that the NT53101 is in the standby mode. The internal status in the standby mode is as follows:
(1) Stop the LCD power supply circuit.

(2) Stop the LCD drive and outputs the V**ss** as the segment/common driver output. However, the static drive system operates.
(3) Holds the display data and operation mode provided before the start of the standby mode.
(4) The MPU can access to the built-in display RAM.
When the RESET command is issued in the standby mode, the sleep mode is set.

When the LCD drive voltage level is given by an external resistive driver, the current of this resistor must be cut so that it may be fixed to floating or V**ss**, prior to or concurrently with causing the NT53101 to go to the sleep mode or standby mode. When an external power supply is used, likewise, the function of this external power supply must be stopped so that it may be fixed to floating or V**ss**, prior to or concurrently with causing the NT53101 to go to the sleep mode or standby mode.

20. Test Command

This is the dedicate IC chip test command. It must not be used for normal operation. If the Test command is issued unconsciously, set the $\overline{RES}$ input to low or issue the Reset command to release the test mode.

A0	E	R / $\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

*: Invalid bit

Cautions: The NT53101 holds an operation status specified by each command. However, the internal operation status may be changed by a high level of ambient noise. It must be considered to suppress the noise on the its package and system or to prevent an ambient noise insertion. To prevent a spike noise, a built-in software for periodical status refreshment is recommended to use.
The test command can be inserted in an unexpected place. Therefore it is recommended to enter the test mode reset command F0h during the refresh sequence.

Command	Code											Function
	A0	E	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	D	Turns on LCD panel when goes high, and turns off when goes low
(2) Initial Display Line	0	1	0	0	1	Display start address						Specifies RAM display line for COM0
(3) Set Page Address	0	1	0	1	0	1	1	Page address				Sets the display RAM page in Page Address register
(4) Set Column Address 4 higher bits	0	1	0	0	0	0	1	Higher column address				Sets 4 higher bits of column address of display RAM in register
(4) Set column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register
(5) Read Status	0	1	1	Status				0	0	0	0	Reads the status information
(6) Write Display Data	1	1	0	Write data								Writes data in display RAM
(7) Read Display Data	1	1	1	Read data								Reads data from display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	D	Sets normal relationship between RAM column address and segment driver when low, but reverses the relationship when high
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	D	Normal indication when low, but full indication when high
(10) Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Selects normal display (0) or Entire Display ON (1)
(11) Set LCD Bias	0	1	0	1	0	1	0	0	0	1	D	Sets LCD drive voltage bias ratio
(12) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Increments Column Address counter during each write when high and during each read when low
(13) End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read-Modify-Write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Resets internal functions
(15) Set Output Status Register	0	1	0	1	1	0	0	D	*	*	*	Selects COM output scan direction. * Invalid data
(16) Set Power Control	0	1	0	0	0	1	0	1	Operation status			Selects the power circuit operation mode
(17) Set Electronic Control Register	0	1	0	1	0	0	Electronic control value					Sets V0 output voltage to Electronic Control register
(18) Set static indicator On/Off	0	1	0	1	0	1	0	1	1	0	D	Set static indicator On/Off 0: OFF 1: ON
(19) Power Save	-	-	-	-	-	-	-	-	-	-	-	Compound command of display OFF and entire display ON
(20) Test Command	0	1	0	1	1	1	1	*	*	*	*	IC Test command. Do not use!
(21) Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	Command of test mode reset

Note: Do not use any other command, or the system malfunction may result.

Absolute Maximum Rating*

DC Supple Voltage (V_{DD}) . . . . . -0.3V to +6.0V

DC Supple Voltage (V_{OUT}) . . . . . -0.3V to +12V

Input Voltage . . . . . -0.3V to V_{DD}+0.3V

Operating Ambient Temperature . . . . -40°C to +85°C

Storage Temperature . . . . . -55°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{SS}= 0V, V_{DD} = 2.4 – 5.1V T_A = -40 to 85°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating Voltage	2.4		5.1	V	
VCI	Internal power supply for DC/DC voltage converter	2.2		5.1	V	
		2.2		4.0	V	3X boosting
		2.2		3.0	V	4X boosting
		2.2		2.4	V	5X boosting
V_{OUT}	Booster output voltage	6.0		12.0	V	
V_0	Voltage regulator operation voltage	4.5		11.5	V	
V_{REG}	Reference voltage	2.2	2.4	2.6	V	T_A=25°C
I_{DD1}	Dynamic current consumption 1	-	40	80	μA	V_{DD} = 3V, V_0 = 8V, build-in power supply off, display on, display data = checker and no access, T_A = 25°C
I_{DD2}	Dynamic current consumption 2	-	200	400	μA	3X boosting, V_{DD}=3V, V_0 = 8V, build-in power supply on, display on, display data = checker and no access, T_A = 25°C
I_{DD3}	Dynamic current consumption 3	-	400	600	μA	4X boosting, V_{DD}=3V, V_0 =11V, build-in power supply on, display on, display data = checker and no access, T_A = 25°C
I_{SP}	Sleep mode current consumption		0.02	2	μA	During sleep, T_A = 25°C
I_{SB}	Standby mode current consumption		20	40	μA	During standby, T_A = 25°C
V_{IHC}	High-level input voltage	0.8×V_{DD}		V_{DD}	V	A0, D0 - D7, E, R/$\overline{W}$, $\overline{CSI}$, CS2, FR, M/S, and $\overline{DOF}$
V_{ILC}	Low-level input voltage	V_{SS}		0.2×V_{DD}	V	A0, D0 - D7, E, R/$\overline{W}$, $\overline{CSI}$, CS2, FR, M/S, and $\overline{DOF}$
V_{OHC}	High-level output voltage	0.8×V_{DD}		V_{DD}	V	I_{OH}=-0.5mA (D0 – D7, FR, FRS, DYO, $\overline{DOF}$ and CL)
V_{OLC}	Low -level output voltage	V_{SS}		0.2×V_{DD}		I_{OL}=0.5mA (D0 – D7, FR, FRS, DYO, $\overline{DOF}$ and CL)
V_{IHS}	High-level input voltage	0.85×V_{DD}		V_{DD}	V	Schmitt trigger input (CL, TMPS, OP1, OP0, CLS and $\overline{RES}$)
V_{ILS}	Low-level input voltage	V_{SS}		0.15×V_{DD}	V	Schmitt trigger input (CL, TMPS, OP1, OP0, CLS and $\overline{RES}$)

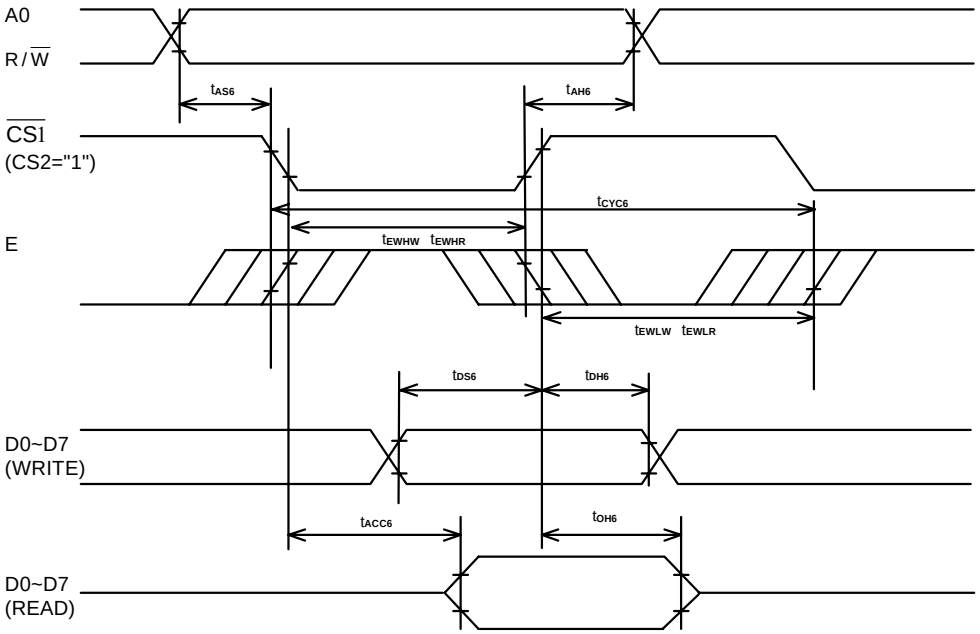
DC Characteristics (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
I_{LI}	Input leakage current	-1.0		1.0	μA	V_{IN}=V_{DD} or V_{SS} (A0, E, R / $\overline{W}$, $\overline{CSI}$, CS2, M/S, TMPS, OP1, OP0 and $\overline{RES}$)	
I_{HZ}	HZ leakage current	-3.0		3.0	μA	When the D0 - D7, FR, CL, DYO and $\overline{DOF}$ are in high impedance	
R_{ON1}	LCD driver ON resistance	-	-	1.3	kΩ	V_0= 11.0V	T_A=25°C, These are the resistance values for when a 0.1V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V1, V2, V3, V4).
R_{ON2}	LCD driver ON resistance	-	-	1.5	kΩ	V_0= 8.0V	
C_{IN}	Input pad capacity	-	5.0	8.0	pF	f=1MHz	
f_{OSC}	Oscillation frequency	27	33	39	kHZ	T_A=25°C, V_{DD} = 3.0V	

Notes: 1. Voltages $V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{SS}$ must always be satisfied.

AC Characteristics

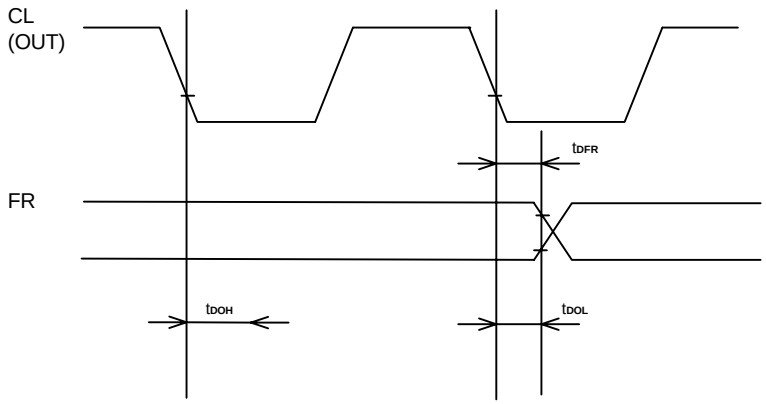
(1) System buses



(V_{DD}=2.4 – 5.1V, T_A = -40 - 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CYC}	System cycle time	400			nS	
T_{AS}	Address setup time	13			nS	
T_{AH}	Address hold time	10			nS	
T_{DS}	Data setup time	35			nS	
T_{DH}	Data hold time	10			nS	
T_{OH}	Output disable time	10		90	nS	C_L=100pF
T_{ACC}	Access time			125	nS	C_L=100pF
T_{EWHR}	Enable	125			nS	
T_{EWHW}	Low pulse width	55			nS	
T_{EWLR}	Enable	125			nS	
T_{EWLW}	Low pulse width	180			nS	

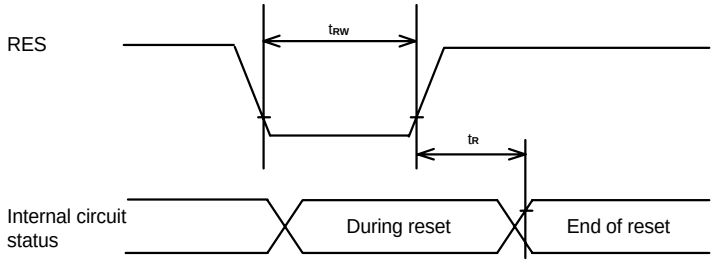
(2) Display control timing



(V_{DD}=2.4 – 5.1V, T_A = -40 - 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{DFR}	FR delay time		13	70	nS	C_L=50pF

(3) Reset timing

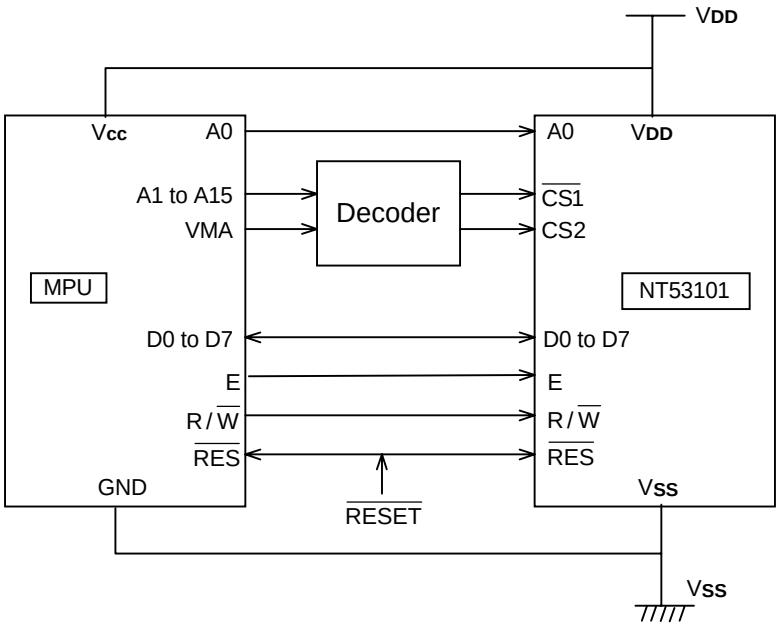


(V_{DD}=2.4 – 5.1V, T_A = -40 - 85°C)

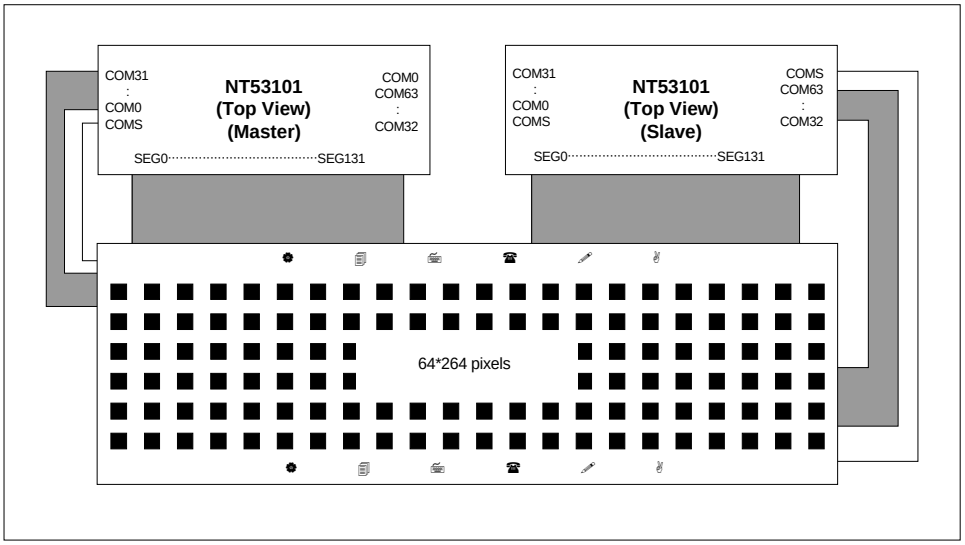
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_R	Reset time	1.0			µS	
T_W	Reset low pulse width	1.0			µS	

MICROPROCESSOR INTERFACE (for reference only)

6502-series microprocessors

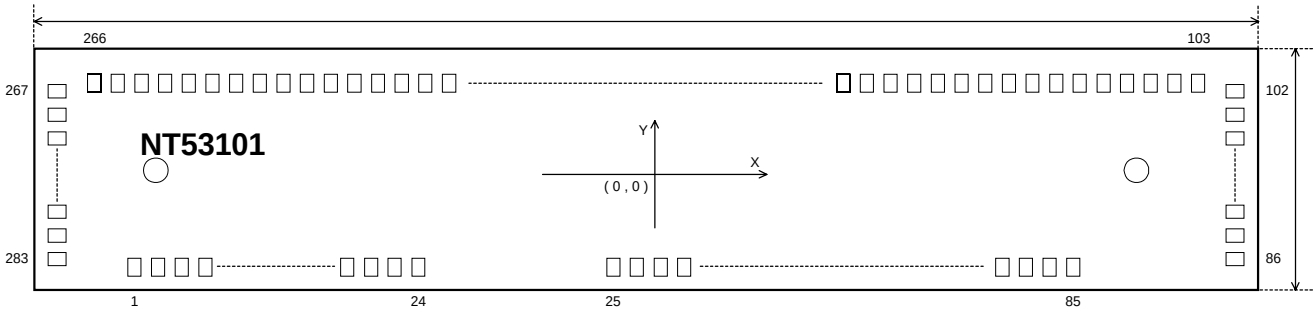


Application example (for reference only)



Connect the following pads of two chips each other:
Display clock pads: CL, FR
Display control pad: $\overline{DOF}$
LCD power pads: V0 V1, V2, V3, V4

Bonding Diagram



Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	FRS	-5109.95	-550	31	VDD	91.65	-550
2	FR	-5019.95	-550	32	VDD	181.65	-550
3	DYO	-4929.95	-550	33	DPS	271.65	-550
4	CL	-4839.95	-550	34	DVS	361.65	-550
5	$\overline{DOF}$	-4749.95	-550	35	VSS	451.65	-550
6	VS1	-4659.95	-550	36	VSS	541.65	-550
7	M/S	-4569.95	-550	37	VSS	631.65	-550
8	$\overline{RES}$	-4479.95	-550	38	VSS	721.65	-550
9	VSS	-4389.95	-550	39	VSS	811.65	-550
10	$\overline{CS1}$	-4299.95	-550	40	VSS	901.65	-550
11	VDD	-4209.95	-550	41	VSS	991.65	-550
12	CS2	-4119.95	-550	42	VSS	1081.65	-550
13	VSS	-4029.95	-550	43	VCI	1171.65	-550
14	A0	-3939.95	-550	44	VCI	1261.65	-550
15	R/W	-3849.95	-550	45	CAP4+	1351.65	-550
16	E	-3759.95	-550	46	CAP4+	1441.65	-550
17	D0	-3669.95	-550	47	CAP3+	1531.65	-550
18	D1	-3579.95	-550	48	CAP3+	1621.65	-550
19	D2	-3489.95	-550	49	CAP1-	1711.65	-550
20	D3	-3399.95	-550	50	CAP1-	1801.65	-550
21	D4	-3309.95	-550	51	CAP1+	1891.65	-550
22	D5	-3219.95	-550	52	CAP1+	1981.65	-550
23	D6	-3129.95	-550	53	CAP2-	2071.65	-550
24	D7	-3039.95	-550	54	CAP2-	2161.65	-550
25	VDD	-448.35	-550	55	CAP2+	2251.65	-550
26	VDD	-358.35	-550	56	CAP2+	2341.65	-550
27	VDD	-268.35	-550	57	VOUT	2431.65	-550
28	VDD	-178.35	-550	58	VOUT	2521.65	-550
29	VDD	-88.35	-550	59	V0	2611.65	-550
30	VDD	1.65	-550	60	V0	2701.65	-550

Bonding Diagram (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
61	VR	2791.65	-550	101	COM16	5856.95	483.65
62	VR	2881.65	-550	102	COM15	5856.95	553.65
63	VSS	2971.65	-550	103	COM14	5705	549.2
64	VSS	3061.65	-550	104	COM13	5635	549.2
65	VDD	3151.65	-550	105	COM12	5565	549.2
66	VDD	3241.65	-550	106	COM11	5495	549.2
67	V0	3331.65	-550	107	COM10	5425	549.2
68	V0	3421.65	-550	108	COM9	5355	549.2
69	V1	3511.65	-550	109	COM8	5285	549.2
70	V1	3601.65	-550	110	COM7	5215	549.2
71	V2	3691.65	-550	111	COM6	5145	549.2
72	V2	3781.65	-550	112	COM5	5075	549.2
73	V3	3871.65	-550	113	COM4	5005	549.2
74	V3	3961.65	-550	114	COM3	4935	549.2
75	V4	4051.65	-550	115	COM2	4865	549.2
76	V4	4141.65	-550	116	COM1	4795	549.2
77	VSS	4231.65	-550	117	COM0	4725	549.2
78	VSS	4321.65	-550	118	COMS	4655	549.2
79	TMPS	4411.65	-550	119	SEG0	4585	549.2
80	VDD	4501.65	-550	120	SEG1	4515	549.2
81	CLS	4591.65	-550	121	SEG2	4445	549.2
82	VSS	4681.65	-550	122	SEG3	4375	549.2
83	OP0	4771.65	-550	123	SEG4	4305	549.2
84	OP1	4861.65	-550	124	SEG5	4235	549.2
85	VDD	4951.65	-550	125	SEG6	4165	549.2
86	COM31	5856.95	-566.35	126	SEG7	4095	549.2
87	COM30	5856.95	-496.35	127	SEG8	4025	549.2
88	COM29	5856.95	-426.35	128	SEG9	3955	549.2
89	COM28	5856.95	-356.35	129	SEG10	3885	549.2
90	COM27	5856.95	-286.35	130	SEG11	3815	549.2
91	COM26	5856.95	-216.35	131	SEG12	3745	549.2
92	COM25	5856.95	-146.35	132	SEG13	3675	549.2
93	COM24	5856.95	-76.35	133	SEG14	3605	549.2
94	COM23	5856.95	-6.35	134	SEG15	3535	549.2
95	COM22	5856.95	63.65	135	SEG16	3465	549.2
96	COM21	5856.95	133.65	136	SEG17	3395	549.2
97	COM20	5856.95	203.65	137	SEG18	3325	549.2
98	COM19	5856.95	273.65	139	SEG19	3255	549.2
99	COM18	5856.95	343.65	139	SEG20	3185	549.2
100	COM17	5856.95	413.65	140	SEG21	3115	549.2

Bonding Diagram (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
141	SEG22	3045	549.2	181	SEG62	245	549.2
142	SEG23	2975	549.2	182	SEG63	175	549.2
143	SEG24	2905	549.2	183	SEG64	105	549.2
144	SEG25	2835	549.2	184	SEG65	35	549.2
145	SEG26	2765	549.2	185	SEG66	-35	549.2
146	SEG27	2695	549.2	186	SEG67	-105	549.2
147	SEG28	2625	549.2	187	SEG68	-175	549.2
148	SEG29	2555	549.2	188	SEG69	-245	549.2
149	SEG30	2485	549.2	189	SEG70	-315	549.2
150	SEG31	2415	549.2	190	SEG71	-385	549.2
151	SEG32	2345	549.2	191	SEG72	-455	549.2
152	SEG33	2275	549.2	192	SEG73	-525	549.2
153	SEG34	2205	549.2	193	SEG74	-595	549.2
154	SEG35	2135	549.2	194	SEG75	-665	549.2
155	SEG36	2065	549.2	195	SEG76	-735	549.2
156	SEG37	1995	549.2	196	SEG77	-805	549.2
157	SEG38	1925	549.2	197	SEG78	-875	549.2
158	SEG39	1855	549.2	198	SEG79	-945	549.2
159	SEG40	1785	549.2	199	SEG80	-1015	549.2
160	SEG41	1715	549.2	200	SEG81	-1085	549.2
161	SEG42	1645	549.2	201	SEG82	-1155	549.2
162	SEG43	1575	549.2	202	SEG83	-1225	549.2
163	SEG44	1505	549.2	203	SEG84	-1295	549.2
164	SEG45	1435	549.2	204	SEG85	-1365	549.2
165	SEG46	1365	549.2	205	SEG86	-1435	549.2
166	SEG47	1295	549.2	206	SEG87	-1505	549.2
167	SEG48	1225	549.2	207	SEG88	-1575	549.2
168	SEG49	1155	549.2	208	SEG89	-1645	549.2
169	SEG50	1085	549.2	209	SEG90	-1715	549.2
170	SEG51	1015	549.2	210	SEG91	-1785	549.2
171	SEG52	945	549.2	211	SEG92	-1855	549.2
172	SEG53	875	549.2	212	SEG93	-1925	549.2
173	SEG54	805	549.2	213	SEG94	-1995	549.2
174	SEG55	735	549.2	214	SEG95	-2065	549.2
175	SEG56	665	549.2	215	SEG96	-2135	549.2
176	SEG57	595	549.2	216	SEG97	-2205	549.2
177	SEG58	525	549.2	217	SEG98	-2275	549.2
178	SEG59	455	549.2	218	SEG99	-2345	549.2
179	SEG60	385	549.2	219	SEG100	-2415	549.2
180	SEG61	315	549.2	220	SEG101	-2485	549.2

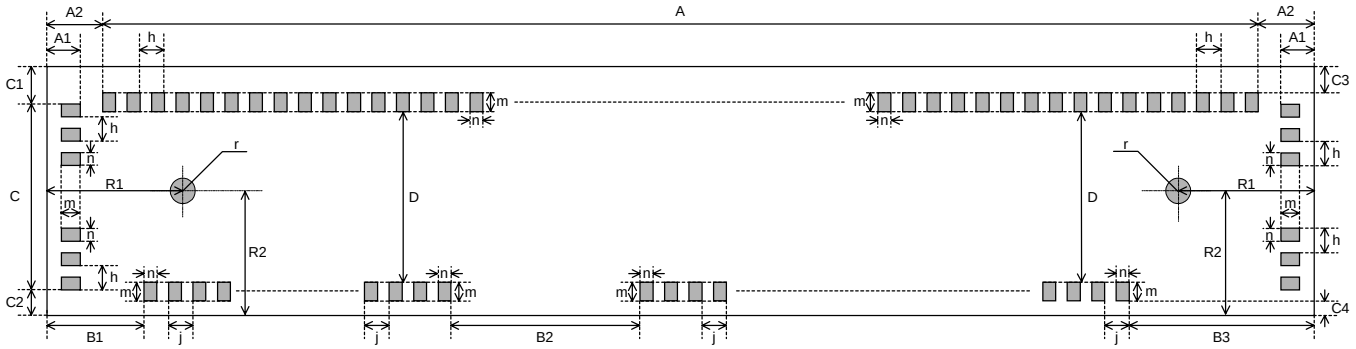
Bonding Diagram (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
221	SEG102	-2555	549.2	254	COM35	-4865	549.2
222	SEG103	-2625	549.2	255	COM36	-4935	549.2
223	SEG104	-2695	549.2	256	COM37	-5005	549.2
224	SEG105	-2765	549.2	257	COM38	-5075	549.2
225	SEG106	-2835	549.2	258	COM39	-5145	549.2
226	SEG107	-2905	549.2	259	COM40	-5215	549.2
227	SEG108	-2975	549.2	260	COM41	-5285	549.2
228	SEG109	-3045	549.2	261	COM42	-5355	549.2
229	SEG110	-3115	549.2	262	COM43	-5425	549.2
230	SEG111	-3185	549.2	263	COM44	-5495	549.2
231	SEG112	-3255	549.2	264	COM45	-5565	549.2
232	SEG113	-3325	549.2	265	COM46	-5635	549.2
233	SEG114	-3395	549.2	266	COM47	-5705	549.2
234	SEG115	-3465	549.2	267	COM48	-5856.95	553.65
235	SEG116	-3535	549.2	268	COM49	-5856.95	483.65
236	SEG117	-3605	549.2	269	COM50	-5856.95	413.65
237	SEG118	-3675	549.2	270	COM51	-5856.95	343.65
238	SEG119	-3745	549.2	271	COM52	-5856.95	273.65
239	SEG120	-3815	549.2	272	COM53	-5856.95	203.65
240	SEG121	-3885	549.2	273	COM54	-5856.95	133.65
241	SEG122	-3955	549.2	274	COM55	-5856.95	63.65
242	SEG123	-4025	549.2	275	COM56	-5856.95	-6.35
243	SEG124	-4095	549.2	276	COM57	-5856.95	-76.35
244	SEG125	-4165	549.2	277	COM58	-5856.95	-146.35
245	SEG126	-4235	549.2	278	COM59	-5856.95	-216.35
246	SEG127	-4305	549.2	279	COM60	-5856.95	-286.35
247	SEG128	-4375	549.2	280	COM61	-5856.95	-356.35
248	SEG129	-4445	549.2	281	COM62	-5856.95	-426.35
249	SEG130	-4515	549.2	282	COM63	-5856.95	-496.35
250	SEG131	-4585	549.2	283	COMS	-5856.95	-566.35
251	COM32	-4655	549.2				
252	COM33	-4725	549.2				
253	COM34	-4795	549.2				

Package Information

Chip Outline Dimensions

unit: inches/mm



Symbol	Dimensions in μm	Symbol	Dimensions in μm
A	11452	C4	20
A1	113.05	D	1009.2
A2	199	m	90
B1	794.05	n	42
B2	2549.6	h	70
B3	952.35	j	90
C	1162	R1	605
C1	40.35	R2	555
C2	27.65	r	30
C3	20.8		