NT58200

Data Bank Micro-controller with expansible LCD and Memory

Preliminary

Date: 1999/7/26

Features

- 65C02 based single chip 8 bit micro-controller
- Operation voltage:2.4V~5.1V (standard : 3.0V or 4.5V)
- Dual oscillation circuits:
  - System oscillator, 3.58MHz ceramic /4MHz Crystal / 4MHz RC by pin options in 3V operating.
    And, 8MHz Crystal /RC Oscillation in 4.5V operating
  - 32.768KHz Crystal for real time clock
- MCU High/Low operating speed software programmable
  - Source clock /1, /2, /4, /8 mode
  - 32.678KHz (Crystal)
- RAM: Built-in 4K x 8bits (incl. Program variable & stack)
- ROM: Built-in 512K x 8bits (incl. Program and Data ROM)
  - External ROM expansible
  - Internal and external ROM Co-existed (Max. 4M bytes)
- Dual-channel voice and melody output
- Software selectable compression structures for various sound quality and duration requirements:
  - 4-bit ADPCM, 5-bit *u*-Law or 8-bit PCM
- Programmable PWM output or current DAC output
- Two I/O ports--PA & PB (16 I/O pins)
- One O/P port--PC (8 O/P pins)
- Standard LCD drivers interface (16 ports)
- Three 8-bit timers----timer0, timer1, timer2.
- One 16-bit sample rate counters (SR1)
- Two interrupt levels and various interrupt sources:
  - NMI and IRQ
  - NMI source
    PA, SR1 Sample rate clock
  - IRQ source
    PA&PB (falling edge), timer0, timer1, timer2, wake-up timer
- Power saving mode and wake-up function
- Programmable watchdog timer
- Programmable wake-up timer
- Low Power detector
- Built-in remote control carrier synthesizer – software programmable
- Powerful functions:
  - Programmable voice sample rate
  - Programmable envelope generator
  - Selectable melody basic waveform
  - Programmable digital volume control

General Description

The NT58200 is a powerful audio control chip with external LCD drivers interface. It integrates a 65C02 8-bit core CPU, SRAM, ROM, and complicated logic blocks, such as timers, dual-tone PSG, software selectable output structure for PWM or DAC. The standby/wakeup function, which can be used to stop/wakeup the oscillator, facilitates the low power dissipation of the system. This chip offers several compression structures, so the speech sources can be coded as PCM, *u*-Law or ADPCM format through NOVATEK's tools.

Voice duration depends on the compression structure. Lower compression rate gains higher sound quality and shorter duration. Normally, ADPCM can meet most requirements especially the sound frequency varies not so violent.

Each one of dual-channel PSG contains a programmable envelope generator, selectable tone basic waveform function.

NT58200 also offers total 16 I/O and 8 O/P pins, which can be used for keyboard scan or other high I/O pins needed applications. Using the LCD and external-memory interfaces, it's suitable to be a LCD ELA product control engine. Furthermore, the electrical DATA BANK, personal digital assistance (PDA) equipment, talking instrument and general speech synthesizer are also applicable.

Blocks Diagram

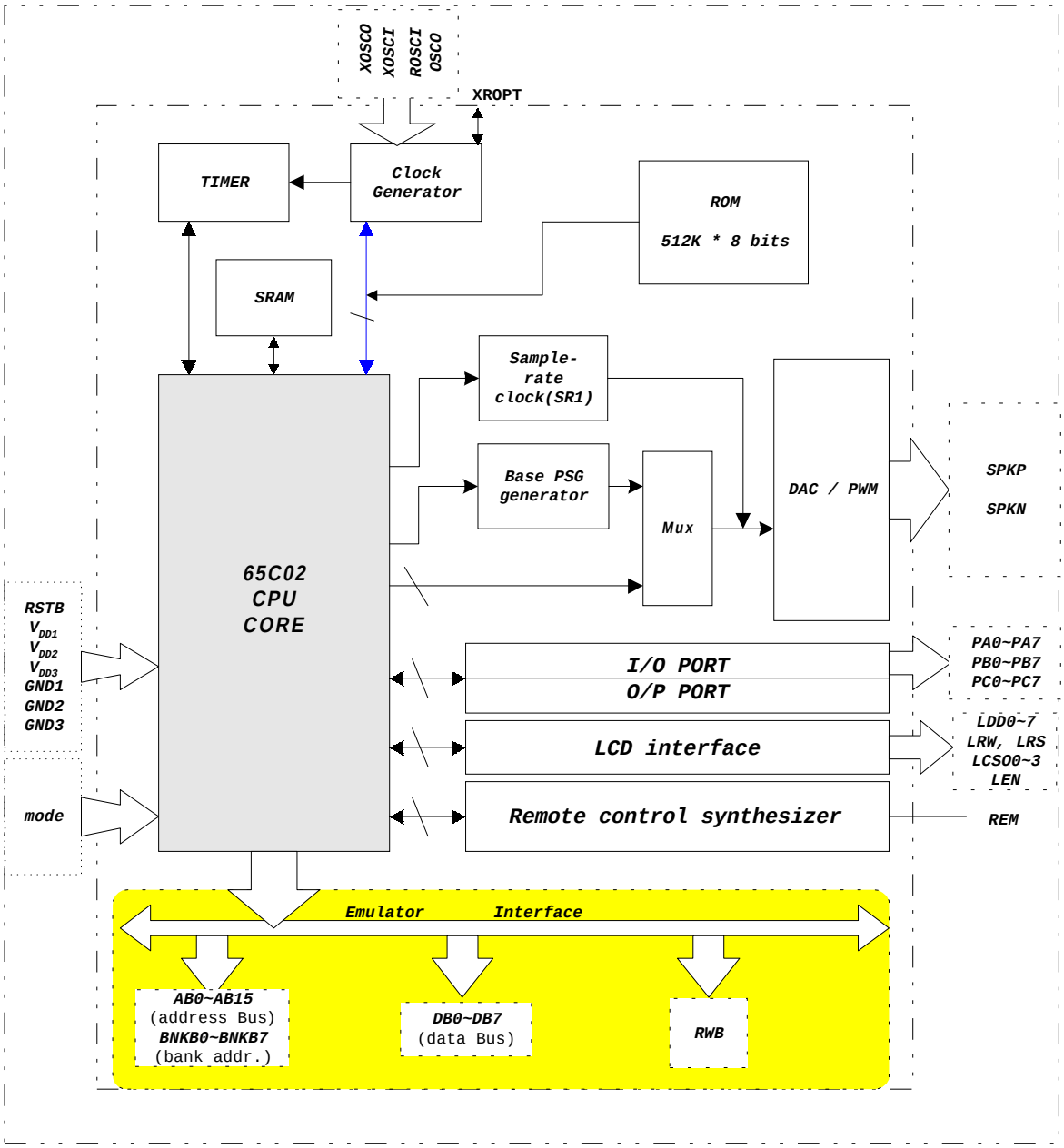
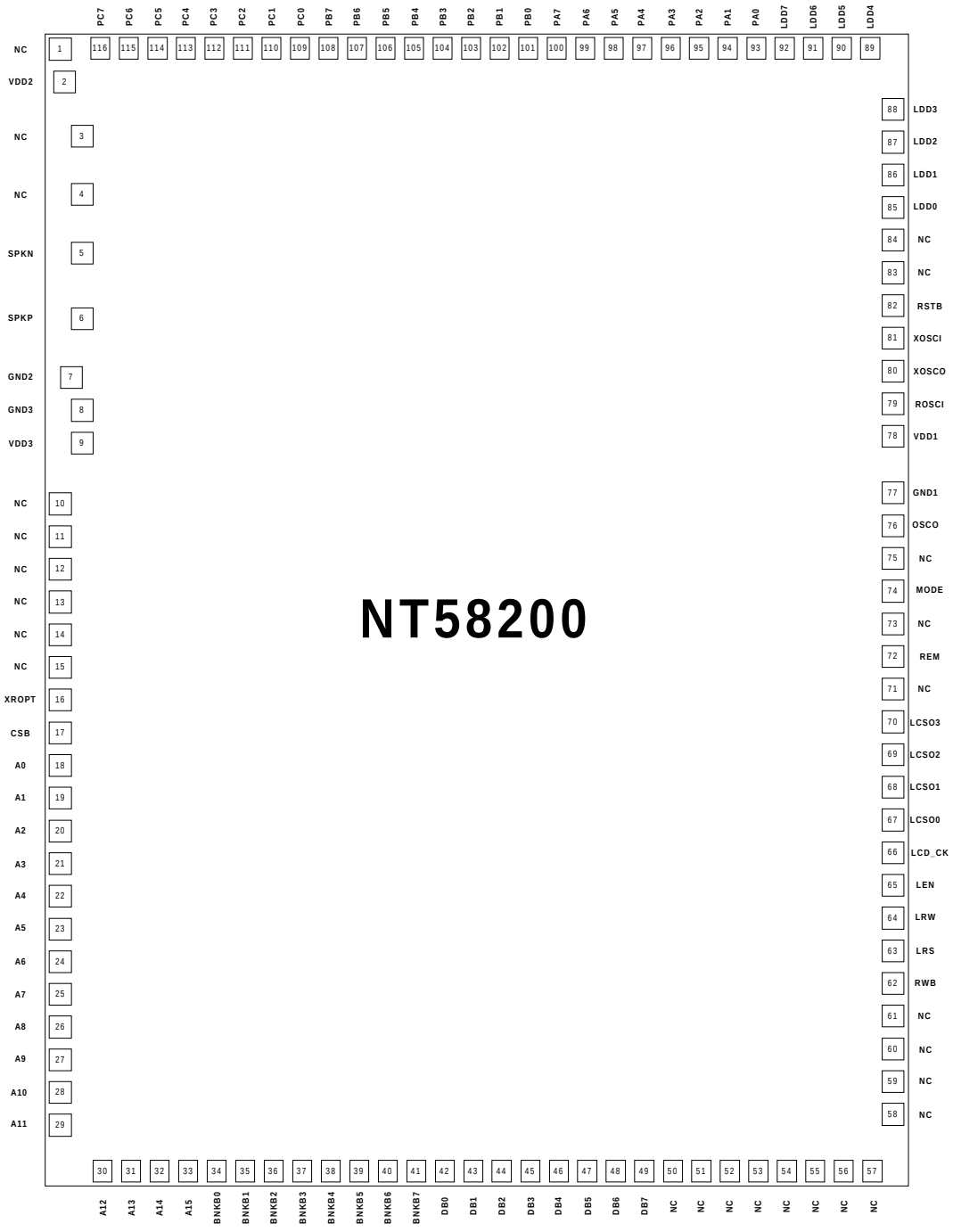


Fig.1 NT58200 Blocks Diagram

Pads Configuration



Pads Description

Pin No.	Pad No	Designation	I/O	Description
	81	XOSCI	I	32768Hz crystal oscillator input pin
	80	XOSCO	O	32768Hz crystal oscillator output pin
	79	ROSCI	I	System oscillator (RC or Crystal) input pin
	76	OSCO	O	System oscillator (crystal) output pin (mask option)
	72	REM	O	Remote data output pin
	6	SPKP	O	Positive terminal of PWM output pin (Also can be used as DAC output pin by software option)
	5	SPKN	O	Negative terminal of PWM output pin
	82	RSTB	I	Reset pin
	78, 2, 9	V_{DD1}, V_{DD2}, V_{DD3}	P	Positive power pin
	77, 7, 8	GND1, GND2, GND3	P	Ground pin
	93 ~ 100	PA0~PA7	I/O	Bi-directional I/O ports (all bit programmable)
	101 ~ 108	PB0~PB7	I/O	Bi-directional I/O ports (high /low nibble programmable)
	109 ~ 116	PC0~PC7	O	Output only ports
	16	XROPT	I	System oscillator selection pin for Crystal / resonator or RC type, 0 = RC type; 1 = Crystal / Resonator type
	85 ~ 92	LDD0~~LDD7	O	LCD interface (for data bus)
	63	LRS	I/O	LCD interface (for register select, choose Command/Data mode)
	67 ~ 70	LCSO0~LCSO3	O	LCD interface (for chip selection in the multi-chip mode)
	66	LCD_CK	O	LCD interface (for external LCD clock input)
	64	LRW	O	LCD interface (read / write signal)
	65	LEN	O	LCD interface (read/write enable signal)
	17	CSB	I	External Memory chip select
	74	MODE	I	Internal or External ROM selection, 0:Internal (default:Floating)
	42 ~ 49	DB0~DB7	I/O	Data bus
	18 ~ 33	A0~A15	I/O	Address bus
	34 ~ 41	BNKB0~BNKB7	I/O	Address bus for bank switch
	62	RWB	I/O	Read or write control signal
	58 ~ 61	NC	-	Not carried
	71, 73, 75	NC	-	Not carried
	83 ~ 84	NC	-	Not carried
	1	NC	-	Not carried
	3 ~ 4	NC	-	Not carried
	10 ~ 15	NC	-	Not carried
	50 ~ 57	NC	-	Not carried
Total pin No. :116 pads				

SYSTEM REGISTER (a)

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W
◆ MEMORY										
$2000	ROM_BNK1	BNK1.7	BNK1.6	BNK1.5	BNK1.4	BNK1.3	BNK1.2	BNK1.1	BNK1.0	R/W
$2001	ROM_BNK2	BNK2.7	BNK2.6	BNK2.5	BNK2.4	BNK2.3	BNK2.2	BNK2.1	BNK2.0	R/W
◆ SYSTEM CONTROL										
$2006	SYS_CTRL	D.7	D.6	D.5	D.4	…	…	…	OPV	R/W
$2007	PWR_SAV	…	…	…	…	…	…	X32KEN	SPDUP	R/W
$2008	RESET	…	…	…	…	…	WT	WD	IPA	R
$2009	LPD_CTRL	LPDEN	…	…	…	…	…	…	LPD	R/W
◆ INTERRUPT										
$2010	NMI_IE	NMISR1	…	…	…	…	…	..	NMIPA	R/W
$2011	NMI_IF	NMISR1	…	…	…	…	…	…	NMIPA	R
$2012	IRQ_IE	…	IRQWT	…	IRQPB	IRQPA	IRQT2	IRQT1	IRQT0	R/W
$2013	IRQ_IF	…	IRQWT	…	IRQPB	IRQPA	IRQT2	IRQT1	IRQT0	R
◆ TIMER										
$2014	TM0_CTRL	…	…	…	…	TM0.3	TM0.2	TM0.1	TM0.0	W
$2015	TM0COUNT	T7	T6	T5	T4	T3	T2	T1	T0	R/W
$2016	TM1_CTRL	…	…	…	…	TM1.3	TM1.2	TM1.1	TM1.0	W
$2017	TM1_COUNT	T7	T6	T5	T4	T3	T2	T1	T0	R/W
$2018	TM2_CTRL	…	…	…	…	…	TM2.2	TM2.1	TM2.0	W
$2019	TM2_COUNT	T7	T6	T5	T4	T3	T2	T1	T0	R/W
$201a	WKT_CTRL	…	…	…	…	…	…	WKT.1	WKT.0	W
$201b	WDT_RST	…	…	…	…	…	…	…	…	W
◆ CARRIER SYNTHIZER										
$201c	RF_CTRL	enable	…	…	…	…	…	…	RFQ.0	W
$201d	RF_OUTPUT	…	…	…	…	…	…	…	DATA	R/W
◆ INPUT/OUTPUT PORT										
$2021	PA	PA.7	PA.6	PA.5	PA.4	PA.3	PA.2	PA.1	PA.0	R/W
$2022	PAC	PAC.7	PAC.6	PAC.5	PAC.4	PAC.3	PAC.2	PAC.1	PAC.0	R/W
$2023	PB	PB.7	PB.6	PB.5	PB.4	PB.3	PB.2	PB.1	PB.0	R/W
$2024	PBC	…	…	…	…	…	…	PBC.H	PBC.L	R/W
$2025	PC	PC.7	PC.6	PC.5	PC.4	PC.3	PC.2	PC.1	PC.0	W
◆ LCD Interface										
$2029	LCS	…	…	…	…	…	CSH/L	SEL1	SEL0	W
$202a	LRS	…	…	…	…	…	…	…	RS	W
$202b	RD_DATA	7	6	5	4	3	2	1	0	R
$202c	LCD0	7	6	5	4	3	2	1	0	R/W
$202d	LCD1	7	6	5	4	3	2	1	0	R/W
$202e	LCD2	7	6	5	4	3	2	1	0	R/W
$202f	LCD3	7	6	5	4	3	2	1	0	R/W

SYSTEM REGISTER (b)

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W
◆ SPEECH										
$2030	CH1_NODE	ND7	ND6	ND5	ND4	ND3	ND2	ND1	ND0	W
$2032	CH3_NODE	ND7	ND6	ND5	ND4	ND3	ND2	ND1	ND0	W
$2034	CH1_VOL	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0	W
$2036	CH3_VOL	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0	W
$2038	Global_VOL1	…	CH3E	…	CH1E	…	GVOL1.2	GVOL1.1	GVOL1.0	R/W
$2040	M1_CTRL	…	…	…	…	…	MODE1	BWS1.1	BWS1.0	W
$2041	M1_LENGTH	KEY1	M1L.6	M1L.5	M1L.4	M1L.3	M1L.2	M1L.1	M1L.0	W
$2042	M2_CTRL	…	…	…	…	…	MODE2	BWS2.1	BWS2.0	W
$2043	M2_LENGTH	KEY2	M2L.6	M2L.5	M2L.4	M2L.3	M2L.2	M2L.1	M2L.0	W
$2044	M1_BASE(L)	TG7	TG6	TG5	TG4	TG3	TG2	TG1	TG0	W
$2045	M1_BASE(H)	TG15	TG14	TG13	TG12	TG11	TG10	TG9	TG8	W
$2046	M2_BASE(L)	TG7	TG6	TG5	TG4	TG3	TG2	TG1	TG0	W
$2047	M2_BASE(H)	TG15	TG14	TG13	TG12	TG11	TG10	TG9	TG8	W
$2048	SD_CTRL	PWM/DAC	…	…	…	…	…	DAC1EN	PWM1EN	W
$2049	SR1_COUNT(L)	SR.7	SR.6	SR.5	SR.4	SR.3	SR.2	SR.1	SR.0	R/W
$204a	SR1_COUNT(H)	SR.15	SR.14	SR.13	SR.12	SR.11	SR.10	SR.9	SR.8	R/W
$204b	SR1_CTRL	enable	…	…	…	…	…	…	…	R/W

Functional Description

Memory Allocation

RAM allocation

NT58200 provides 4K x 8 bits RAM, it's used to store data memory, stack, program variable.

RAM ADDRESS	Description
$0000~$00FF	Zero page for program variable
$0100~$01FF	Stack Area
$0200~$0FFF	Working RAM
$1000~$1FFF	Reserved
$2000~$20FF	System register
$2100~$3FFF	Reserved

Memory mapping

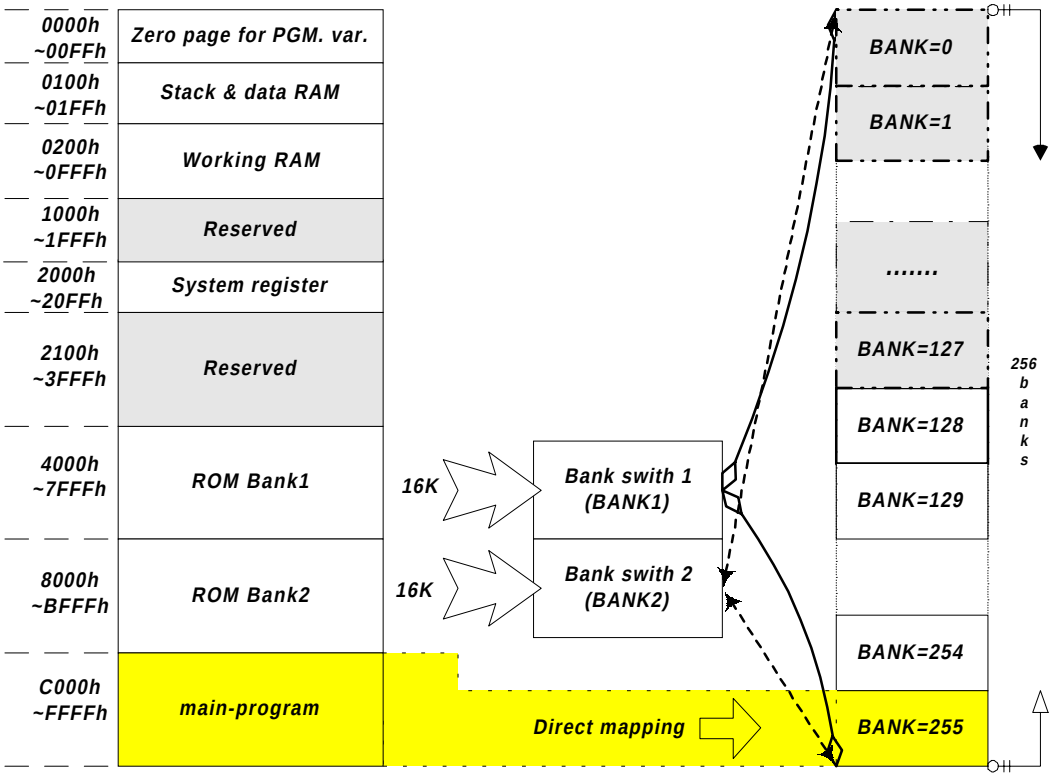


Fig.2 Memory Allocation map

Under 65C02 core structure, the program counter (16 bit) can only addresses 64K x 8 bits ROM space, hence, for the ROM size above 64K x 8 bits, the NT58200 offers the method of switching banks to extend the CPU address space. This chip offers 2 bank mapping areas, one is located at 4000h~7FFFh and the other is located at 8000h~BFFFh. There are 256 banks derived from each mapping area decoding, and every bank will indicate 16K x 8 bits. Therefore, the system can address max. up to 4096K x 8 bits (256 x 16Kx8bits).

Bank switch register

ADDRESS	*REGISTER*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*	*R/W*	Default
$2000	ROM_BNK1	BNK1.7	BNK1.6	BNK1.5	BNK1.4	BNK1.3	BNK1.2	BNK1.1	BNK1.0	R/W	11111111
$2001	ROM_BNK2	BNK2.7	BNK2.6	BNK2.5	BNK2.4	BNK2.3	BNK2.2	BNK2.1	BNK2.0	R/W	11111111

(A).The 16-bit program counter of 65C02 just can address 64K x 8 bits ROM space. Bank switch is used to extend the CPU address space. The two upper 16K bytes ROM blocks map to corresponding bank. (according to the BANK register, listed as follows.)

(B). The ROM mappings are:

ADDRESS	ROM_BNK1 ROM_BNK2 =0	ROM_BNK1 ROM_BNK2 =1	…….	ROM_BNK1 ROM_BNK2 =223	ROM_BNK1 ROM_BNK2 =224	…… ……	ROM_BNK1 ROM_BNK2 =254	ROM_BNK1 ROM_BNK2 =255
$C000h~$FFFFh	4080K~4M	4064~4080K	…….			……		
$4000h~$7FFFh	4080K~4M	4064~4080K	…….	512~528K	496~512K	……	16~32K	0K~16K
$8000h~$BFFFh	4080K~4M	4064~4080K		512~528K	496~512K	……	16~32K	0K~16K

Unit: byte

(C). Bank Switch:

(1). When the NT58200 is powered on, the ROM_BNK1, ROM_BNK2 are initially switched to bank FFh

(2). In order to linearize the ROM mapping, the address C000H~FFFFH will direct map to the bank255, listed in the figure-1, and it will meet the rule of the vector table for the 65C02 (the vector table should be located at FFFAH~FFFFH for 65C02)

(3). Wherever the ROM bank is, if the program counter read the C000H~FFFFH area, the bank must be switched to bank 255, thus, the program code and the vector table will not be lost in the bank switching.

(4). The NT58200 built-in 512K x 8 bits ROM, hence, In the Normal Mode (shown in the next page), ROM_BNK1 & ROM_BNK2 only can set in the following range: E0h~FFh.

(5). If user needs the ROM size over than 512K x 8 bit, the NT58200 also supply the External ROM access solution.

Chip Operating Modes Selection

(1). Users can use the MODE pin to choose Internal ROM or External ROM mode for operating.

(2). MODE = 0 , for Internal ROM mode; MODE = 1, for External ROM mode Default:Floating

(3). In the internal ROM mode, while the programmers access the address above 512K bytes, the NT58200's address will be decoded to the external ROM. That is, in the internal ROM mode, the internal ROM and external ROM could be coexistent.

(4). In the external ROM mode, the built -in ROM (512K bytes) will be disabled. That is, in the external ROM mode, the address will be decoded to the external ROM.

The NT58200 offers dual clock selection, one for system clock source by RC or Crystal oscillation (pin-option), the other is a time base clock source, 32.768KHz oscillator. The chip operating speed can also be programmed by software.

System control register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2006	SYS_CTRL	D.7	D.6	D.5	D.4	…	…	…	OPV	R/W	00000000

OPV	Operating Voltage selection bit, 1 = 4.5V and 0 = 3.0V
D.7	System Clock Source selection bit
0	Select system clock source from RC/Crystal
1	Select system clock source from time base clock (32,768Hz Crystal)
D.6	**When D7 = 0, this bit is used to select clock source frequency**
0	Clock Source =4MHz (or 3.58MHz)
1	Clock Source = 8MHz

D.5	D.4	Divisor of system clock
0	0	/8
0	1	/4
1	0	/2
1	1	/1

D[5:4]: the pre-scaler of Clock Source (Chosen by D.6)

Note:

(A). System oscillator component must be connected and it can be RC or crystal type according to the "XROPT" pin state (pin option). As to the time base clock, 32.768KHz, crystal oscillator may be connected or not that depends on the applications you need.

(B). When the 32.768KHz crystal is connected, user has to set X32KEN to "1" (see PWR_SAV register) to enable 32.768KHz crystal.

(C). The CPU clock is 32.768KHz when bit7 (D.7) is set to 1. Normally, this situation just happened at "STANDBY" mode to keep LCD display in regular.

(D). When 32.768KHz is used as system clock source, that is D.7=1, then D [6:4] are no more effective.

(E). D [7:4] = 00h (default). That means "Clock Source is not from 32.768KHz, Source Freq = 4MHz, and Pre-scaler = /8", so the system will work on 500KHz.

(F). In 3V operating, it is appropriate to set the system worked on 2MHz to process ADPCM and peripheral events.

LOW POWER DETECTION

The low power detection (LPD) is used to monitor the supply voltage and generate an internal flag to user for indicating the battery energy is much lower that may damage the operation status of system. The appearance of low voltage signal can remind user to replace battery.

(1). Different voltage operating, the various LPD voltage settings is needed. So, the bit0 (OPV) state of SYS_CTRL will determine the corresponding LPD voltage settings.

OPV = 0	V_{DD}=3.0V	→ then →	V_{LPD}:2.4V
OPV = 1	V_{DD}=4.5V	→ then →	V_{LPD}:3.6V

(2). Enable the LPD detection by set LPD_EN to 1, default LPD_EN = 0 (disabled)

(3). If LPD is enabled, the flag (LPD) will be set to 1 when the LPD circuit detects $V_{DD} \leqq V_{LPD}$. In this case, the programmer can use the flag to turn on LPD service subroutine to indicate users it's time to replace the supply battery.

LPD control register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2009	LPD_CTRL	LPD_EN	…	…	…	…	…	…	LPD	R/W	00000000

LPDEN	LPD	
	1	"1" means low voltage ($V_{DD} \leqq V_{LPD}$) detected; 0: $V_{DD} \geqq V_{LPD}$
1		LPD circuit enabled; 0: disabled

Power Saving control

User can get the system to reduce power consumption, by:

(1). STOP instruction (STP)

(2). Power saving register control

Power Saving Register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2007	PWR_SAV	…	…	…	…	…	…	X32KEN	SPDUP	R/W	111
$2008	RESET	…	…	…	…	…	WT	WD	IPA	R	000

(A). PWR_SAV register:

Control bit	Function description	Default
X32KEN	Turn ON/OFF 32.768K crystal--If CPU & Crystal is turned off at the same time, system will be shut down. That is, only the I/O port can wake up the chip.	1 (Turn-ON)
SPDUP	Speed up the 32K Oscillator in the CPU turn-on status.(1:turn on the function),it should be noticed that turnning off the function when the CPU is stable.	1 (Turn-ON)

Note: Turn off LCD display can reduce the power consumption much more.

(B). RESET register:

WT	WD	IPA	Description
		1	Wakeup by external port trigger (PORT A interrupt)
	1		System reset by Watchdog
1			System reset by wake up timer

Note:

(1). Once user read the reset status register, the 3-bit register will be immediately reset to 0 on the next ϕ0 pulse from low go high. Program can check what causes it to start running from reset vector through this register reading.

(2). If the 32.768KHz is turned off before STP instruction executed, there is only one way, port-A interrupt, to wake the CPU up. The port wake up is level trigger, hence, once the port data register is set to 00h, the CPU will be wake up.

(3). If the 32.768KHz is turned off before STP instruction executed, the CPU can be woken up by wake up timer, watchdog, and port-A interrupt.

INTERRUPT - NMI & IRQ

NMI enables

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2010	NMI_IE	NMISR1	…	…	…	…	…	…	NMIPA	R/W	00000000

(A). The register is used to decide what NMI sources can be activated. It's a Non-Maskable Interrupt.

(B). 0: Disable (default)
1: Enable (If the bit is set to 1, it means that the relative event can interrupt CPU.)

NMISR1: Interrupt of SR1 (sample rates counter 1)
NMIPA: Interrupt of port-A

NMI request flag

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2011	NMI_IF	NMISR1	…	…	…	…	…	…	NMIPA	R	00000000

(A). The register is used to record NMI request status. It means that the bit7 (NMISR1) will be set to 1 when the NMI source (SR1) counter overflows, from $FF to $00. In the meantime, if the corresponding bit on the NMI_IE register is set to 1 (enabled) then the NMI will be triggered. And, the program counter will point to the NMI vector. (6502 NMI vector is located at the FFFAh~FFFBh)

(B). After NMI occurs, program has to read this register to know which source triggering NMI and to re-enable the NMI. In other words, no any source can trigger NMI again before this register has been read after NMI occurs. This register will be cleared to zero after reading it.

0 = disable (the Counter don't count overflow yet…….Default)
1 = enable (the Counter counts overflow from $FF to $00, NMI flag activates)

NOTE:

(A). NT58200 can serve multi-level interrupt. However, 65C02 only has one NMI vector, therefore, it is necessary to reset the NMI_IF register if there are several (NMI) interrupt sources shared in the program. In this situation, users should store the value of NMI_IF into the program variable before reset NMI_IF flag for recording what NMI interrupt sources has happened.

(B). If the corresponding bit of NMI_IE register is set to 0, the bit of NMI_IF register won't be set to 1 while NMI source is coming up.

(C). Interrupt priority : NMI >> IRQ

IRQ enable

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2012	IRQ_IE	…	IRQWT	…	IRQPB	IRQPA	IRQT2	IRQT1	IRQT0	R/W	00000000

(A). The register is used to decide what IRQ sources can be activated.

(B). 0: Disable (default)
1: Enable (If the bit is set to 1, it means that the relative event can interrupt CPU.)

IRQWT	IRQPB	IRQPA	IRQT2	IRQT1	IRQT0	
					1	Timer0 count overflow
				1		Timer1 count overflow
			1			Timer2 count overflow
		1				Input PORTA trigger
	1					Input PORTB trigger
1						Wakeup timer overflow

IRQ request flag

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2013	IRQ_IF	…	IRQWT	…	IRQPB	IRQPA	IRQT2	IRQT1	IRQT0	R	00000000

After IRQ occurs, program has to read this register to know which source triggering IRQ and to clear it. In other words, CPU will be re-interrupted after instruction “RTI” or “CLI” executed unless the program read this register to clear it.

Note:

(A). The IRQ will be triggered when the bit of IRQ_IE enabled and the corresponding bit on IRQ_IF=1. At this time, IRQ will activate and start from the IRQ vector address. (65C02’s IRQ vector is defined on $FFFEh ~ $FFFFh).

(B). After IRQ occurred, the relative bit of IRQ request flag was set to 1, so, if the IRQ_IF flag didn’t be cleared to 0, the IRQ will be trigger immediately again (because the bit of IRQ_IE still enabled), the unpredicted thing will be happen, such as, stack overflow. Thus, the IRQ request (IRQ_IF) must be reset immediately by reading the IRQ_IF in the beginning of the IRQ interrupt service routine (ISR).

Timer / Counter

NT58200 has several timers: timer0, timer1, timer2, watchdog timer, and wake-up timer.

Timer0

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2014	TM0_CTRL	…	…	…	…	TM0.3	TM0.2	TM0.1	TM0.0	W	00000000
$2015	TM0COUNT	T7	T6	T5	T4	T3	T2	T1	T0	R/W	00000000

(A). Timer0 is an 8 bits up-count timer, when counter overflows from $FF to $00 will generate a timer IRQ request and set the IRQT0 (bit0) of IRQ request flag (IRQ_IF) to 1. If the corresponding bit of IRQ_IE is set to 1 then Timer0 interrupt will be activated.

(B). The clock source of timer0 can be system clock or external crystal(32.768KHz).

(C). Timer0 starts counting when the TM0COUNT is setting.

(1). Due to the asynchronous counting characteristics, the reading value may not be accurate! It must be careful for programmer to process the value accessed from timer0.

(2). This counter can be programmed as preload counter. Writing data to this register to set initial value for counting, thus we can prescale the timer again.

TM0_CTRL (timer0 control register):

TM0.3	For timer0 enable counting or disable
0	Disable
1	Enable

TM0.2	For automatic reload function
0	Disable
1	Enable

TM0.1	TM0.0	Description			TM0 divisor (TM0COUNT)	Frequency from TM0
		Timer 0 clock source from		Timer 0 clock input		
		System oscillator (assume 8MHz, and /2 mode)	Pre-scale			
0	0	System clock (4MHz)	**/65536**	61.04Hz	1(FF) ~ 255(00)	61.04~0.24Hz
0	1	System clock (4MHz)	**/2048**	1953.13Hz	1(FF) ~ 255(00)	1953.13~7.66Hz
1	0	System clock (4MHz)	**/2**	2MHz	1(FF) ~ 255(00)	2M~7843.14Hz
1	1	32.768KHz or 31.25KHz	**/8**	4096Hz or 3096.25Hz	1(FF) ~ 255(00)	4096.00~16.06Hz or 3096.25~12.14Hz

(A). TM0.0 and TM0.1 are used to decide the pre-scale values.

(B). If the external clock (32.768KHz) isn't connected to the system, then TM0.0=1 and TM0.1=1 will cause the timer0 to change the source from 32.768KHz to system clock, 31.25KHz.

Example:

If the clock source = system (4MHz), prescale = 65536 (TM0.1=0, TM0.0=0), TM0_COUNT=128, then
timer0 frequency = {4000000 / (65536)} / {256-128}=0.48Hz

Timer1

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2016	TM1_CTRL	…	…	…	…	TM1.3	TM1.2	TM1.1	TM1.0	W	00000000
$2017	TM1_COUNT	T7	T6	T5	T4	T3	T2	T1	T0	R/W	00000000

TM1_CTRL (timer1 control register):

TM1.3	For timer1 enable counting or disable
0	Disable
1	Enable

TM1.2	For automatic reload function
0	Disable
1	Enable

TM1.1	TM1.0	Description			TM1 divisor (TM1COUNT)	Frequency from TM1
		Timer1 clock source from	Pre-scale	Timer 1 clock input		
0	0	Timer0 overflow			1(FF) ~ 255(00)	
0	1	System clock (4MHz)	**/2048**	1953.13Hz	1(FF) ~ 255(00)	1953~7.66Hz
1	0	32.768K or 31.25K	**/16**	2048Hz or 1953.13Hz	1(FF) ~ 255(00)	2048 ~ 8.03Hz or 1935.13 ~ 7.66Hz
1	1	32.768K or 31.25K	**/2**	16384Hz or 15625Hz	1(FF) ~ 255(00)	16384 ~ 64.25Hz or 15625 ~ 61.27Hz

(A). If the clock source of timer1 comes from timer0, a new preload value of timer1 for getting various frequency won't be loaded into the counter until timer0 overflows. Actually, you also can change the contents of timer0 to get a desired frequency from TM1 without preload a new value into TM1.
(B). If the external clock (32.768KHz) isn't connected to the system, then the chosen clock source, 32.768KHz, will be changed to the system clock, 31.25KHz.

TM1_COUNT:
(A). Due to the asynchronous counting characteristics, the reading value may not be accurate! It must be careful for programmer to process the value accessed from timer0.
(B). This counter can be programmed as preload counter. Writing data to this register to set initial value for counting, thus we can prescale the timer again.

Example:
If the clock source = timer0, pre-scale = 2048 (TM0.1=0, TM0.0=1), TM0_COUNT=128, TM1_COUNT= 64, then timer1 frequency = {[4000000 / (2048)] / [256-128]} / [256-64] = 0.08Hz

Timer2

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2018	TM2_CTRL	…	…	…	…	…	TM2.2	TM2.1	TM2.0	W	00000000
$2019	TM2_COUNT	T7	T6	T5	T4	T3	T2	T1	T0	R/W	00000000

TM2_CTRL (timer2 control register):

TM2.2	For timer1 enable counting or disable
0	Disable
1	Enable
TM2.1	**For automatic reload function**
0	Disable
1	Enable

TM2.0	Description			TM2 divisor (TM2COUNT)	Frequency from TM2
	Timer2 clock source from	Pre-scale	Timer 2 clock input		
0	Timer1 overflow			1(FF) ~ 255(00)	
1	32.768K or 31.25K	**/16**	2048Hz or 1953.13Hz	1(FF) ~ 255(00)	2048~8.03Hz or 1953.13~7.66Hz

(A). If the clock source of timer2 comes from timer1, a new preload value of timer2 for getting various frequency won't be loaded into the counter until timer1 overflows. Actually, you also can change the contents of timer1 to get a desired frequency from TM2 without preload a new value into TM2.
(B). If the external clock (32.768KHz) isn't connected to the system, then the chosen clock source, 32.768KHz, will be changed to the system clock, 31.25KHz.

TM2_COUNT

The cascade block diagram of timer0, time1 and timer2 is as following:

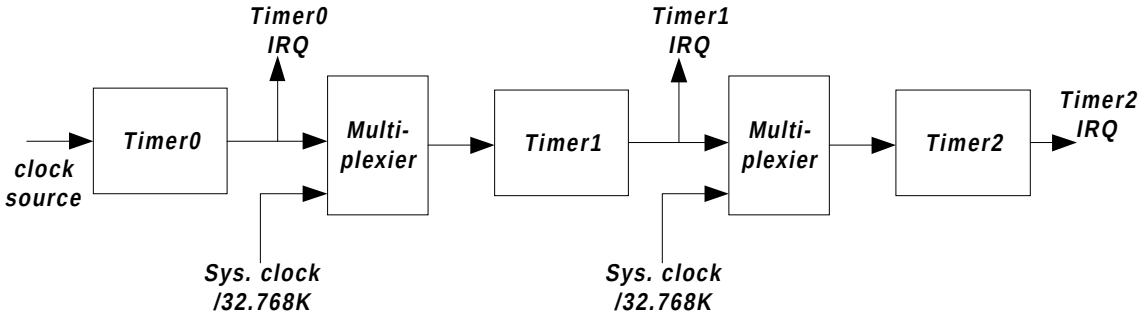


Fig.3 Timer cascade block diagram

Wakeup timer

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$201a	WKT_CTRL	…	…	…	…	…	…	WKT.1	WKT.0	W	00000000

(A). The clock source of wakeup timer is 32.768KHz. User can derive a different wake-up period by setting the WKT_CTRL register. If the associated bit of IRQ.IE (bit6) is set to 1 it will trigger the Interrupt of wakeup timer when it counts overflow.

WKT.1	WKT.0	Timer-out period
0	0	0.25(sec)
0	1	0.5(sec)
1	0	1(sec)
1	1	2(sec)

(B). If the external clock (32.768KHz) isn't connected to the system, the wakeup time will be useless.

Watch dog timer (WDT)

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W
$201b	WDT_RST	…	…	…	…	…	…	…	…	W

(A). The clock source of watchdog timer is cascaded from wakeup timer. The watchdog timer is designed for preventing a software malfunction or sequence jumping to an unknown state with unpredictable results.

(B). The period of watchdog timer is four times wakeup timer. Overflow happens during normal operation will initialize the chip to a **"RESET"** status, thus, before the WDT counts overflow, programmer should reset the WDT counter by writing any data to the WDT_RST.

The period of watchdog = 4 x (the period of wakeup timer)

(C). If the external clock (32.768KHz) isn't connected to the system, the watchdog time will be useless.

WDT_RS T (watchdog reset register):

(A). In order to prevent the chip from "RESET" status, before the WDT counts overflow, programmer should reset the WDT counter by writing any data to the WDT_RST.

Cascade blocks diagram of wakeup timer and watchdog:

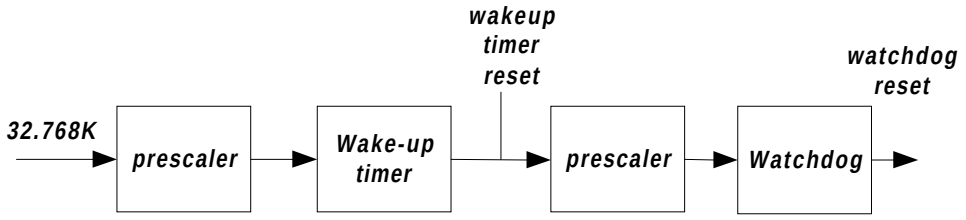


Fig.4 Timer cascade block diagram

I/O Port

The NT58200 provides 16 I/O ports (PA, PB) and 8 O/P ports (PC).

PORT pull up control

(1). The pull-up transistor is controlled by port data registers (PA and PB); hence, setting the corresponding bits or nibbles to turn ON / OFF the pull-up transistor individually.

(2). Internal pull-up transistor only used in the INPUT mode.

For example:

If bit7 and bit2 of PORTA is internal pull up, then

Step1: Setting #10000100b to the PORTA control-register (input port mode).

Step2: Setting #10000100b to the PORTA data register.

PORTA

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2021	PA	PA.7	PA.6	PA.5	PA.4	PA.3	PA.2	PA.1	PA.0	R/W	11111111
$2022	PAC	PAC.7	PAC.6	PAC.5	PAC.4	PAC.3	PAC.2	PAC.1	PAC.0	R/W	11111111

(A). PAC (PORTA control register):

PAC.[7~0]	Setting PA as Input /Output (all bits programmable)
1	Set that pin of PORTA as input (on initial setting)
0	set that pin of PORTA as output

(B). PA (PORTA data register): The output or input data buffers.

PORTB

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2023	PB	PB.7	PB.6	PB.5	PB.4	PB.3	PB.2	PB.1	PB.0	R/W	11111111
$2024	PBC	…	…	…	…	…	…	PBC.H	PBC.L	R/W	00000111

(A). PBC (PORTB control register):

PBC.H	PBC.L	Setting PB high nibbles and low nibbles as Input / Output
	1	Set low nibbles of PORTB as input ports (0: low nibbles as output ports)
1		Set high nibbles of PORTB as input ports (0: high nibbles as output ports)

(B). PB (PORTB data register): The output or input data buffers

PORTC (Output only)

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2025	PC	PC.7	PC.6	PC.5	PC.4	PC.3	PC.2	PC.1	PC.0	W	00000000

PC (PORTC data register): The output data buffers.

Port Interrupt

The PORTA (B) can be used as port interrupt sources. Since PORTA (B) is bi-directional I/O, thus,

(A). Only the input port status could generate interrupt.

(B). Any input pin of PORTA (B) transitions from high to low level would generate an interrupt request. No any other falling edge transitions of input pins can generate interrupt request again until all of the pins return to high level.

LCD Interface

The NT58200 provides 16 pins for the interface of external LCD drivers. The built-in LCD interface of the NT58200 is applicable for 8 bit parallel I/P structure. Ex: NT3881/NT3882 or NT3890/NT3891or NT53101 or KS107/KS108 or SED15xx or HDxx … and so on. The application blocks are shown as following:

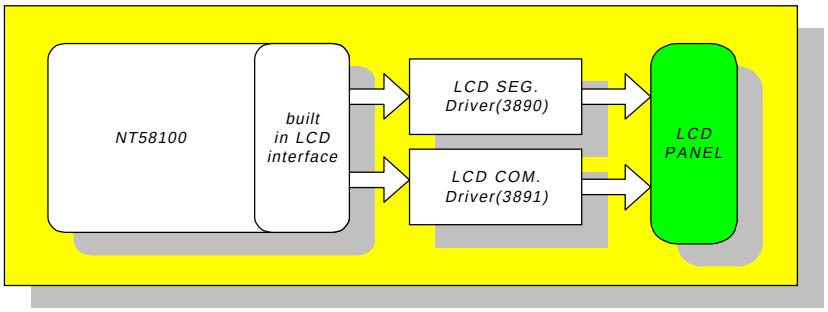


Fig.5 LCD Application

Control register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W
$2029	LCS	…	…	…	…	…	CSH/L	SEL1	SEL0	W
$202a	LRS	…	…	…	…	…	…	…	RS	W
$202b	RD_DATA	7	6	5	4	3	2	1	0	R
$202c	LCD0	7	6	5	4	3	2	1	0	R/W
$202d	LCD1	7	6	5	4	3	2	1	0	R/W
$202e	LCD2	7	6	5	4	3	2	1	0	R/W
$202f	LCD3	7	6	5	4	3	2	1	0	R/W

(A). LCS:

(1). NT58200 supplies the LCD clock for external LCD drivers or modules. The user can use this register to fine-tune the LCD interface output frequency. Shown as following:

SEL1	SEL0	Clock division
0	0	NT58200 System clock /1
0	1	NT58200 System clock /2
1	0	NT58200 System clock /4
1	1	NT58200 System clock /8

CSH/L	Chip Select Trigger level
0	Active Low (Default)
1	Active High

(B). LRS:

This register is used to identify the data type in the data bus (LDD0~7). That is, programmer uses the register to indicate the external LCD drivers what the data type (the instruction or pure data) is used.

RS	Data mode
0	Instruction mode
1	Data mode

(C). RD_DATA:

This register is used to store the input transition data. When user using the READ data/status instruction, the data will be stored to the RD_DATA register.

For example, if the programmer wants to read data from the LCD driver (here assume driver 0 is selected), the program flows are needed:

```
Lda     $202C   ; load LCD0 data into LCD buffers
Lda     $202b   ; load LCD buffer data into $202b register (RD_DATA)
Sta     var     ; store the contents of RD_DATA register to a variable that is defined on zero page
```

(D). LCD0:

This register is used to store the data that will be written out. LCD0 is used for the driver0. NT58200 supplies maximum up to 4 LCD drivers and the data access relies on the individual LCD drivers. (That is, LCD1 is used for the driver1, LCD2 is used for the driver2, and LCD3 is used for the Driver3.)

Interface pin

(1). LDD0~7:
Data bus between NT58200 and external LCD drivers.

(2). LRS:
This pin is mapped from the inner register “LRS” state to indicate the bus data type for external LCD drivers.

(3). LCSO0~LCSO3:
Chip selection control pins for external LCD drivers.

(4). LRW:
Read / Write control signal pin between NT58200 and external LCD drivers.

(5). LEN:
Enable signal for external LCD drivers.

(6). LCD_CK:
The clock output for the external LCD drivers. This pin will generate a clock source for the external LCD drivers.

LCD Timing Waveform

Item	Symbol		Condition	Max.	Min.	Unit
Address setup time	LRS LRW	Tad (set)				ns
Address hold time		Tad (hold)				
Data setup time	LDD0 ∫ LDD7	Td (set)				
Data hold time		Td (hold)				
RD access time		Tr (access)				
Output disable time		To (dis)				
Input signal falling time		Tf				
Input signal rising time		Tr				
Enable High pulse width (Read)	LEN	Tenh (R)				
Enable High pulse width (Write)		Tenh (W)				

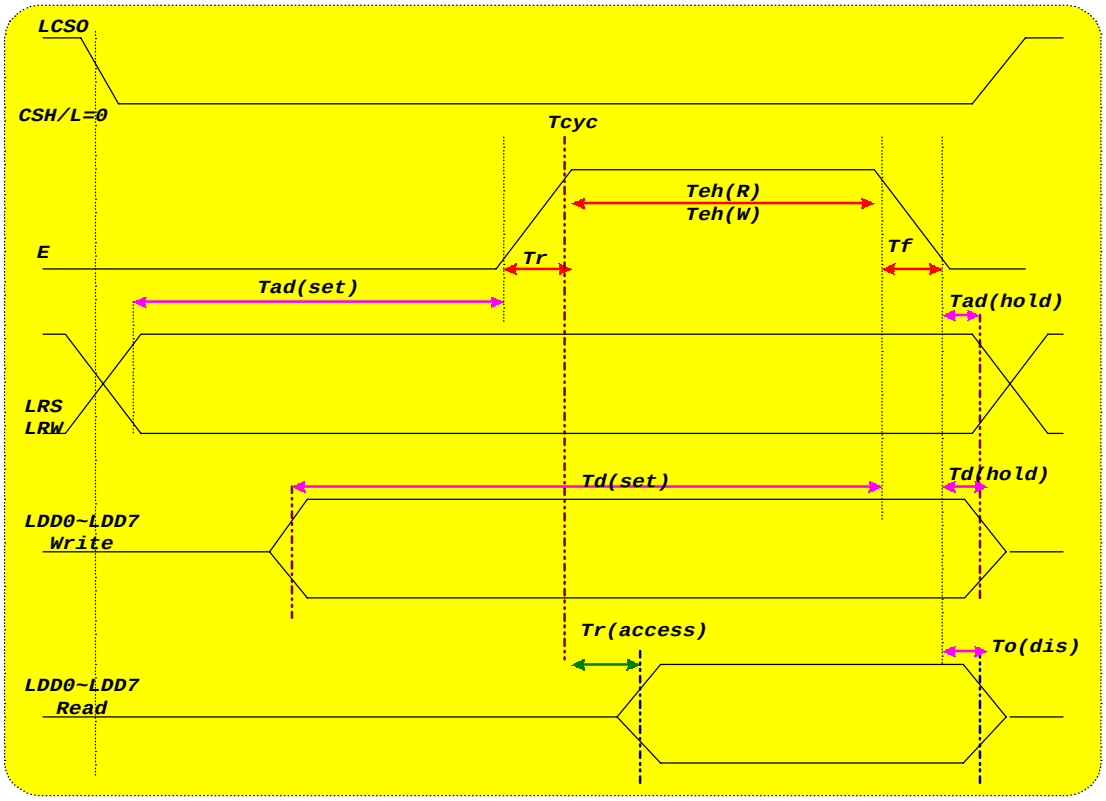


Fig.6 LCD Read /Write Timing

PSG GENERATOR

PSG (Programmable Sound Generator) includes a tone generator and an envelope generator:
(A). Tone generator: Generating a basic frequency of tone by the tone control register and base counter.
(B). Envelope generator: Generating a decayed envelope or a sustained envelope by tone length and tone volume registers.

PSG1
Tone1 base counter and control register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2044	M1_BASE(L)	TG7	TG6	TG5	TG4	TG3	TG2	TG1	TG0	W	00000000
$2045	M1_BASE(H)	TG15	TG14	TG13	TG12	TG11	TG10	TG9	TG8	W	00000000
$2040	M1_CTRL	…	…	…	…	…	MODE	BWS1.1	BWS1.0	W	00000000

(A). Tone generator, M1_BASE (L) and M1_BASE (H) registers, are used for tone base frequency generation. They generate specific frequencies of tone. They also can be used as general counters, just like timer 1. The counter overflow frequency is illustrated below:

Tone Base frequency = f / [integer of (65536 / register value)+1], if remainder >0
Tone Base frequency = f / [integer of (65536 / register value)], if remainder =0
Note: f = 31.25KHz, if system freq. = 2MHz

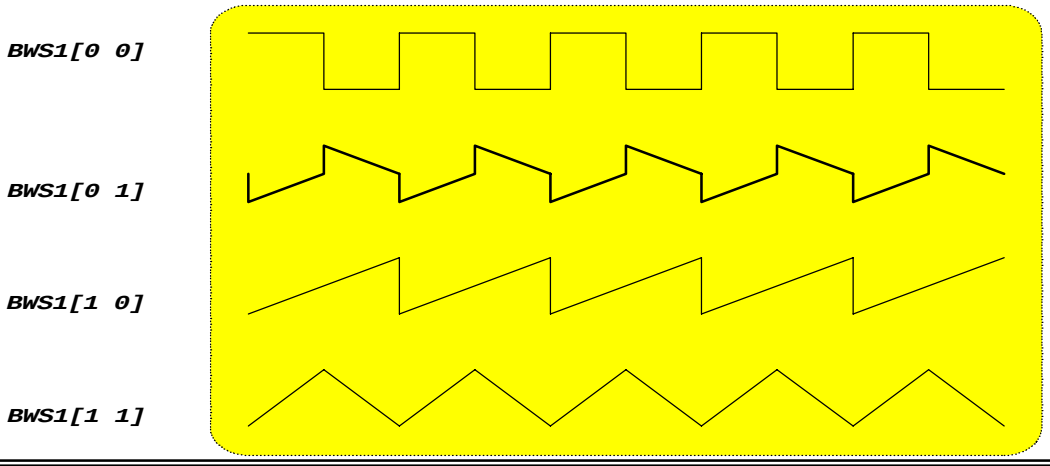
Example: (ref. APPENDIX A in detail)

Tone	Ideal Tone (Hz)	M1_BASE (H)	M1_BASE (L)	Base Freq. (Hz)	Error (db)
C3	130.81	01h	13h	130.75	-0.05
C3#	138.59	01h	24h	138.89	0.22
D3	146.83	01h	34h	146.71	-0.08
D3#	155.56	01h	47h	155.47	-0.06
:	:	:	:	:	:
G6	1567.98	0Ch	CEh	1562.5	-0.35
A6	1760.00	0Eh	3Ah	1736.11	-1.36
B6	1975.53	10h	02h	1953.12	-1.13
C7	2093.00	11h	13h	2083.33	-0.46
C7#	2217.46	12h	4Bh	2232.14	0.66
D7	2349.32	13h	B3h	2403.85	2.32
D7#	2489.02	13h	B3h	2403.85	-3.42

(B). Tone1 control register:

BWS1.1	BWS1.0	Basic Waveform Selection bits.
0/1	0/1	Shown as following

Fig.7 Tone base waveform



MODE	Mode selection bit.
0	Melody mode, the value of tone base counter will directly output to node register.
1	This channel will be used as voice channel.

Envelop Generator

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2034	CH1_VOL	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0	W	00000000
$2041	M1_LENGTH	KEY1	M1L.6	M1L.5	M1L.4	M1L.3	M1L.2	M1L.1	M1L.0	W	00000000

(A). This register is used for tone length counting and envelope controlling. If user's program enables hardware melody, the register can generate a decayed envelope waveform as figure 8.

KEY1	Key control, it is used for key-on and key-off control.
0 1	Key-off mode - the envelope will decay to zero. Key-on mode – envelope will be set to the volume value (don't decay)
M1L[6:0] :	**Tone length, it is used to control envelope decay rate.**
	Listed below: (Fig.8)

(B). The effects of tone length and volume controls are shown below.

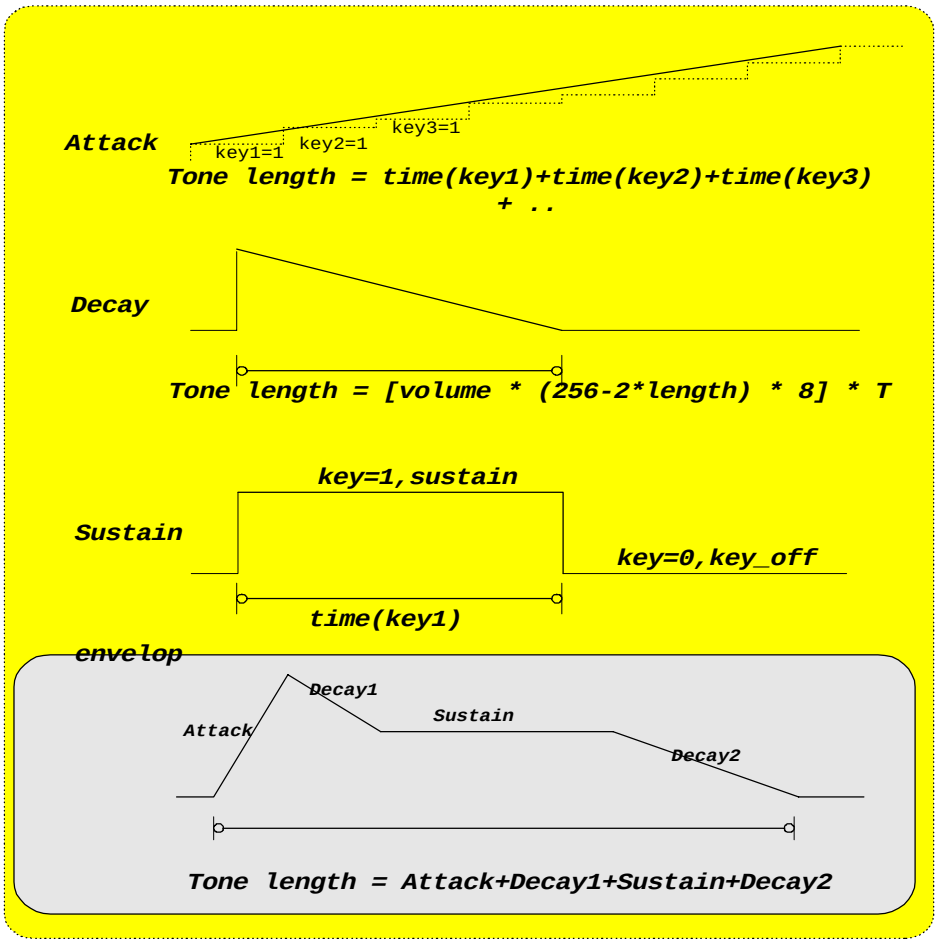


Fig.8 PSG envelop generator

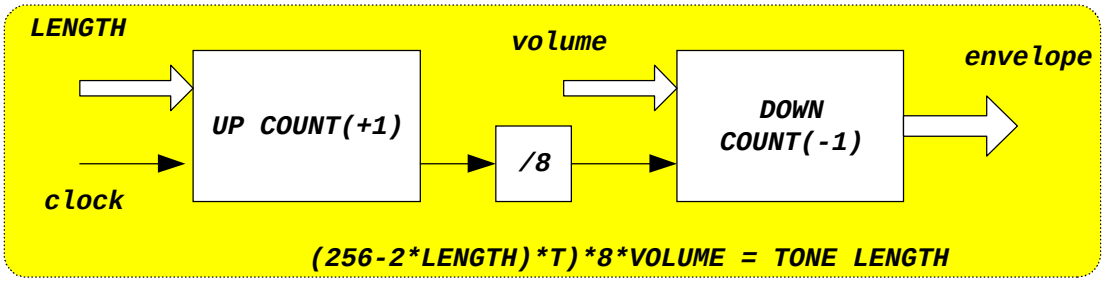


Fig.9 PSG Tone Length diagram

PSG2 (same as PSG1)

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2046	M2_BASE(L)	TG7	TG6	TG5	TG4	TG3	TG2	TG1	TG0	W	00000000
$2047	M2_BASE(H)	TG15	TG14	TG13	TG12	TG11	TG10	TG9	TG8	W	00000000
$2042	M2_CTRL	…	…	…	…	…	MODE2	BWS2.1	BWS2.0	W	00000000
$2036	CH3_VOL	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0	W	00000000
$2043	M2_LENGTH	KEY2	M2L.6	M2L.5	M2L.4	M2L.3	M2L.2	M2L.1	M2L.0	W	00000000

The definition and usage of those registers about tone and envelope tone generation of PSG2 are same as that of PSG1.
How to score melody? Tone length is the time period from tone start to tone ending. It must match the rule:

Tone_Length = volume x [256 – (2 x length)] x 8 x T

Ex. If the volume = FFh, then what's the tone length?

Assume the system frequency = 2MHz then f = 31.25K Hz, and T = 1/f = 32 usec
We can get the tone length value: Tone_Length = 2^8 x (256 – 2 x length) x 2^3 x 32 (us) = (256-2 x length) x 65.536 (ms)
So, If length (M1L [6:0])= 0 Tone length = 16.78 sec
If length (M1L [6:0])= 64 Tone length = 8.39 sec
If length (M1L [6:0])= 96 Tone length = 4.19 sec
If length (M1L [6:0])= 112 Tone length =112.00 sec

NT58200 also has a wave table ROM space to enhance the extra melody variable beside the basic waveform. The following register controls it:

Node Register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2030	CH1_NODE	ND7	ND6	ND5	ND4	ND3	ND2	ND1	ND0	W	00000000
$2032	CH3_NODE	ND7	ND6	ND5	ND4	ND3	ND2	ND1	ND0	W	00000000

Note: Node value of voice data is an 8-bit 2'complement data format. (Signed data)

Volume Register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2034	CH1_VOL	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0	W	00000000
$2036	CH3_VOL	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0	W	00000000

Volume values are of unsigned 8-bit codes. The voice and volume data are loaded into a hardware multiplier that generates an 8-bit voice output. If a channel operates in hardware-melody mode, the volume values are not only volume parameters but also tone length parameters.

Sample rate clock (SR1)

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2049	SR1_COUNT(L)	SR.7	SR.6	SR.5	SR.4	SR.3	SR.2	SR.1	SR.0	R/W	00000000
$204a	SR1_COUNT(H)	SR.15	SR.14	SR.13	SR.12	SR.11	SR.10	SR.9	SR.8	R/W	00000000
$204b	SR1_CTRL	enable	…	…	…	…	…	…	…	R/W	00000000

(A). This chip offers a 16-bit up counter for sample rates clock generated from system clock.

(B). The counter will be re-loaded with the new values and start counting as long as programmer writes data into the SR1_COUNT (H) register regardless of the SR1_COUNT (L). That is, if some data was written into the SR1_COUNT (L) and nothing was written into SR1_COUNT (H), this counter won't be loaded any data and start counting. And, even if some data was written into the SR1_COUNT (L) during SR1 counting, the counter will still count the past values until the counter overflows. After the overflow, the new values will be immediately loaded into the counter.

(C). Sample rate clock:

The frequency of sample rate = system clock / {2^{16} -[SR1_COUNT (H), SR1_COUNT (L)]}

(D). SR1_CTRL (sample rate control register):

0:disable 1:enable counter

Global Volume Register

Sound output control

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2048	SD_CTRL	PWM/DAC	…	…	…	…	…	DAC1EN	PWM1EN	W	00000000

(A). NT58200 provides 2 types of audio output, one is current DAC type for driving external speaker through an external NPN transistor (8050); the other is PWM type for directly driving speaker or buzzer without any buffer or AMP circuit needed. In current DAC type, it provides a louder sound, but also brings more power consumption. (DAC output signal is send to the SPKP)

PWM/DAC	PWM or DAC Output
0	**DAC Output**
1	**PWM Output**
DAC1EN	**DAC1 output control**
0	DAC1 output Disable
1	DAC1 output Enable
PWM1EN	**PWM1 output control**
0	PWM1 output Disable
1	PWM1 output enable

Glorbal1 & Glorbal2 volume control

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$2038	Global_VOL1	…	CH3E	…	CH1E	…	GVOL1.2	GVOL1.1	GVOL1.0	R/W	00000000

(A). The output of NT58200 will mix the 2 channels outputs into one signal at a time, user can choose the volume source individually by bit7~ bit4 of volume register.

CH3E	CH1E	Description
	1	CH1 enable (0: CH1 disable)
1		CH3 enable (0: CH3 disable)

(C). Bit [2:0] are used to control each speaker output volume, shown as following:

GVOL1.2	GVOL1.1	GVOL1.0	Description
0	0	0	Min. volume
0	0	1	…
…	…	…	…
1	1	1	Max. Volume

Carrier synthesizer

This chip is built-in a carrier synthesizer for infrared or RF remote control circuit.

Remote control

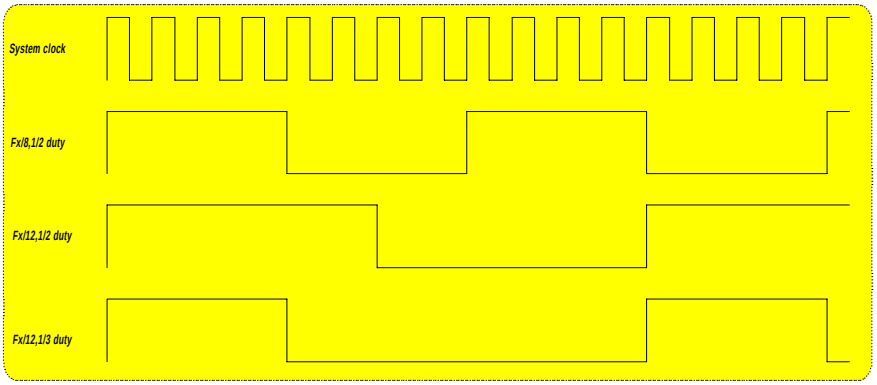
ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$201c	RF_CTRL	enable	…	…	…	…	…	…	RFQ.0	W	00000000
$201d	RF_OUTPUT	…	…	…	…	…	…	…	DATA	R/W	00000000

RFQ.0	Carrier frequency
0	Frequency=56K,1/2 duty
1	Frequency=38K,1/2 duty

enable	Enable output pin data control
1	Enable data output
0	Disable data output(default)

DATA	Carrier data output control
1	Carrier Output
0	Disable carrier(default)

Fig.10 Carrier generator



Absolute Maximum Rating

DC Supply Voltage……-0.3V to +7V

Input / Output Voltage……GND-0.3V to V_{DD}+03.V

Operating Ambient Temperature…-10^{0}C to +60^{0}C

Storage Temperature……-55^{0}C to +125^{0}C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (1)

(GND = 0V，Temp = 25^{0}C，F_{RC} = 4MHz, System clock=2MHz, Standard Operating Voltage=3V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD}	Operating Voltage	2.4	3.0	3.3	Volt	3V operates
V_{IH}	Input High Voltage	0.7*V_{DD}	---	V_{DD}+0.3	Volt	
V_{IL}	Input Low Voltage	GND-0.3	---	0.3*V_{DD}	Volt	
I_{OP}	Operating Current	---	1.5	---	mA	output floating，V_{DD}=3V
I_{STB1}	Standby Current1	---	1	2	uA	CPU off, 32K off, No load, V_{DD}=3V
I_{STB2}	Standby Current2	---	3	6	uA	CPU off, 32K On, No load, V_{DD}=3V
I_{OH}	Port A driving current	0.5	1.5	---	mA	V_{OH} = 2.7V，V_{DD}=3V
I_{OL}	Port A sink current	1	3	---	mA	V_{OL} = 0.4V，V_{DD}=3V

DC Electrical Characteristics (2)

(GND = 0V，Temp = 25^{0}C，F_{RC} = 4MHz, System Clock =2MHz, Standard Operating Voltage=4.5V)

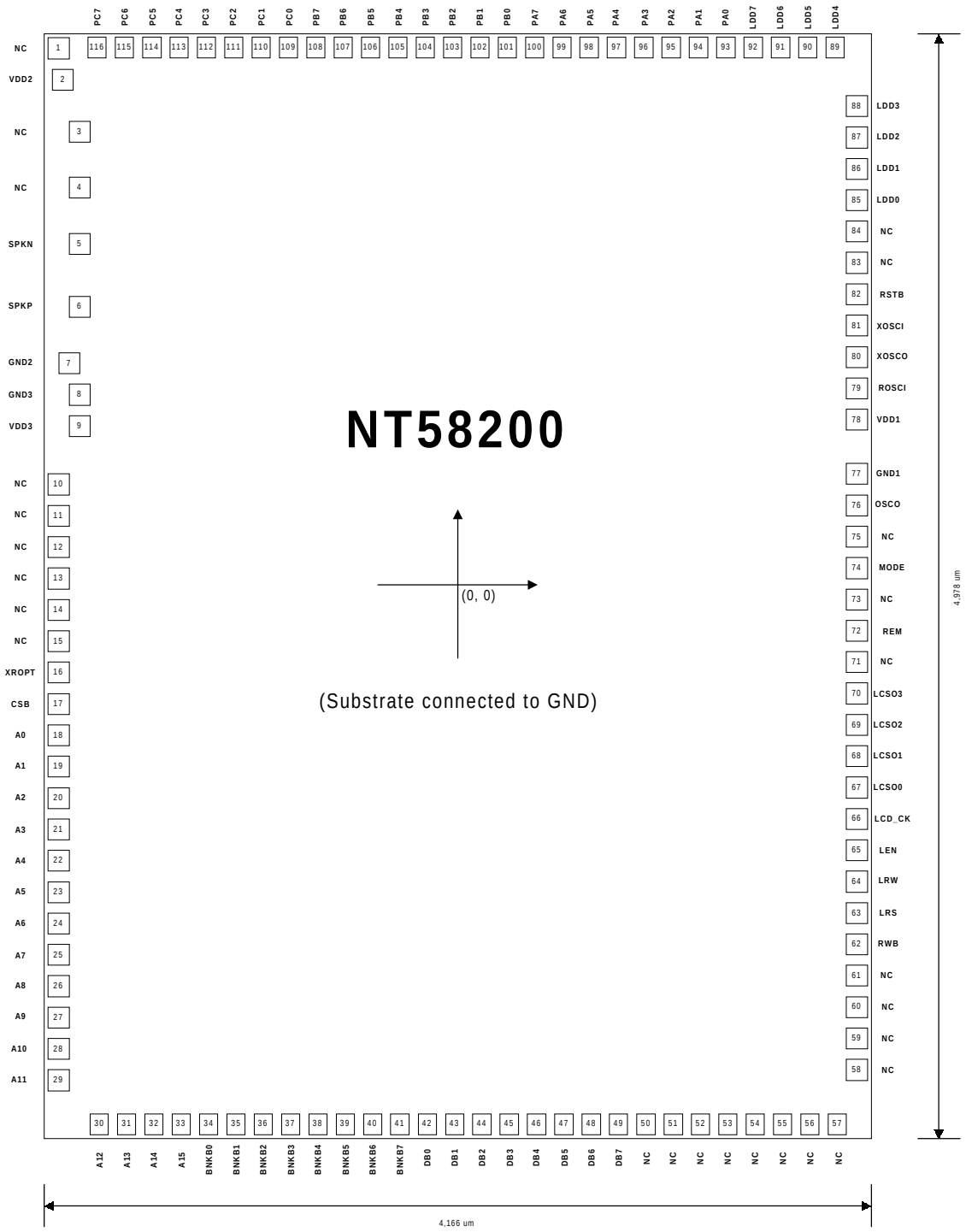
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD}	Operating Voltage	3.6	4.5	5.1	Volt	4.5V operates
V_{IH}	Input High Voltage	0.7*V_{DD}	---	V_{DD}+0.3	Volt	
V_{IL}	Input Low Voltage	GND-0.3	---	0.3*V_{DD}	Volt	
I_{OP}	Operating Current	---	3	---	mA	Output floating，V_{DD}=4.5V
I_{STB1}	Standby Current	---	1	2	uA	CPU off, 32k off, No load,V_{DD}=4.5V
I_{STB2}	Standby Current	---	6	8	uA	CPU off, 32k On, No load,V_{DD}=4.5V
I_{OH}	Port A driving current	1	3	…	mA	V_{OH} =3.6V，V_{DD}=4.5V
I_{OL}	Port A sink current	2	6	…	mA	V_{OL} =0.9 V，V_{DD}=4.5V

AC Electrical Characteristics

(GND = 0V，Temp = 25^{0}C，F_{RC} = 4MHz)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_{PWM}	PWM output driving current	---	25	---	mA	
I_{DAC}	current DAC output current	---	2.6	---	mA	
$\Delta F_{RC}/F_{RC}$	RC Frequency Stability	---	7 5 5 4	10 7 7 6	%	[F(3.0V)-F(2.5V)] / F(3.0V), F_{OSC}=8M [F(4.5V)-F(3.5V)] / F(4.5V), F_{OSC}=8M [F(3.0V)-F(2.5V)] / F(3.0V), F_{OSC}=4M [F(4.5V)-F(3.5V)] / F(4.5V), F_{OSC}=4M
F_{CPU}	CPU working frequency	0.5 0.5	2 2	4.5 6.5	MHz	V_{DD}=3.0V V_{DD}=4.5V

Pads Diagram



Pad	Designation	X	Y
1	NC	-1941.40	2342.95
2	VDD2	-1921.85	2204.25
3	NC	-1869.60	1952.35
4	NC	-1869.60	1687.35
5	SPKN	-1869.60	1351.15
6	SPKP	-1869.60	1086.15
7	GND2	-1900.45	851.20
8	GND3	-1868.80	718.15
9	VDD3	-1872.70	588.10
10	NC	-1957.45	386.65
11	NC	-1957.45	256.65
12	NC	-1957.45	126.65
13	NC	-1957.45	-3.35
14	NC	-1957.45	-133.35
15	NC	-1957.45	-263.35
16	XROPT	-1957.45	-393.35
17	CSB	-1957.45	-523.35
18	A0	-1957.45	-653.35
19	A1	-1957.45	-783.35
20	A2	-1955.60	-915.00
21	A3	-1957.45	-1043.35
22	A4	-1957.45	-1173.35
23	A5	-1957.45	-1303.35
24	A6	-1957.45	-1433.35
25	A7	-1957.45	-1563.35
26	A8	-1957.45	-1693.35
27	A9	-1957.45	-1823.35
28	A10	-1957.45	-1953.35
29	A11	-1957.40	-2083.35
30	A12	-1753.00	-2360.50
31	A13	-1623.00	-2360.50
32	A14	-1493.00	-2360.50
33	A15	-1363.00	-2360.50
34	BNKB0	-1233.00	-2360.50
35	BNKB1	-1103.00	-2360.50
36	BNKB2	-973.00	-2360.50
37	BNKB3	-843.00	-2360.50
38	BNKB4	-713.00	-2360.50
39	BNKB5	-583.00	-2360.50
40	BNKB6	-453.00	-2360.50
41	BNKB7	-323.00	-2360.50
42	DB0	-193.00	-2360.50
43	DB1	-63.00	-2360.50
44	DB2	67.00	-2360.50
45	DB3	197.00	-2360.50
46	DB4	327.00	-2360.50
47	DB5	457.00	-2360.50
48	DB6	587.00	-2360.50
49	DB7	717.00	-2360.50
50	NC	847.00	-2360.50
51	NC	977.00	-2360.50
52	NC	1017.00	-2360.50
53	NC	1237.00	-2360.50
54	NC	1367.00	-2360.50
55	NC	1497.00	-2360.50
56	NC	1627.00	-2360.50
57	NC	1757.00	-2360.50
58	NC	1957.65	-2069.35
59	NC	1957.65	-1928.35
60	NC	1957.65	-1787.35
61	NC	1957.65	-1646.35
62	RWB	1957.65	-1516.35
63	LRS	1957.65	-1386.35
64	LRW	1957.65	-1256.35
65	LEN	1957.65	-1126.35
66	LCD_CK	1957.65	-996.35
67	LCSO0	1957.65	-866.35
68	LCSO1	1957.65	-736.35
69	LCSO2	1957.65	-606.35
70	LCSO3	1957.65	-476.35
71	NC	1957.65	-346.35
72	REM	1957.65	-216.35
73	NC	1957.65	-86.35
74	MODE	1957.65	43.65
75	NC	1957.65	173.65
76	OSCO	1957.65	303.65
77	GND1	1959.00	443.65
78	VDD1	1958.80	704.45
79	ROSCI	1957.65	849.95
80	XOSCO	1957.65	979.95
81	XOSCI	1957.65	1109.95
82	RSTB	1957.65	1239.95
83	NC	1957.65	1369.95
84	NC	1957.65	1499.95
85	LDD0	1957.65	1629.95
86	LDD1	1957.65	1759.95
87	LDD2	1957.65	1900.95
88	LDD3	1957.65	2041.95
89	LDD4	1832.90	2360.35
90	LDD5	1702.90	2360.35
91	LDD6	1572.90	2360.35
92	LDD7	1442.90	2360.35
93	PA0	1312.90	2360.35
94	PA1	1182.90	2360.35
95	PA2	1052.90	2360.35
96	PA3	922.90	2360.35
97	PA4	792.90	2360.35
98	PA5	662.90	2360.35
99	PA6	532.90	2360.35
100	PA7	402.90	2360.35
101	PB0	272.90	2360.35
102	PB1	142.90	2360.35
103	PB2	12.90	2360.35
104	PB3	-117.10	2360.35
105	PB4	-247.10	2360.35
106	PB5	-377.10	2360.35
107	PB6	-507.10	2360.35
108	PB7	-637.10	2360.35
109	PC0	-767.10	2360.35
110	PC1	-897.10	2360.35
111	PC2	-1027.10	2360.35
112	PC3	-1157.10	2360.35
113	PC4	-1287.10	2360.35
114	PC5	-1417.10	2360.35
115	PC6	-1547.10	2360.35
116	PC7	-1677.10	2360.35

(unit: um)

Chip size: 164 X 196 mil²

Application Circuit (for reference only) (a)

(Without IR application; used in the RC mode; LCD interface with the LCD COMMON, SEGMENT driver)

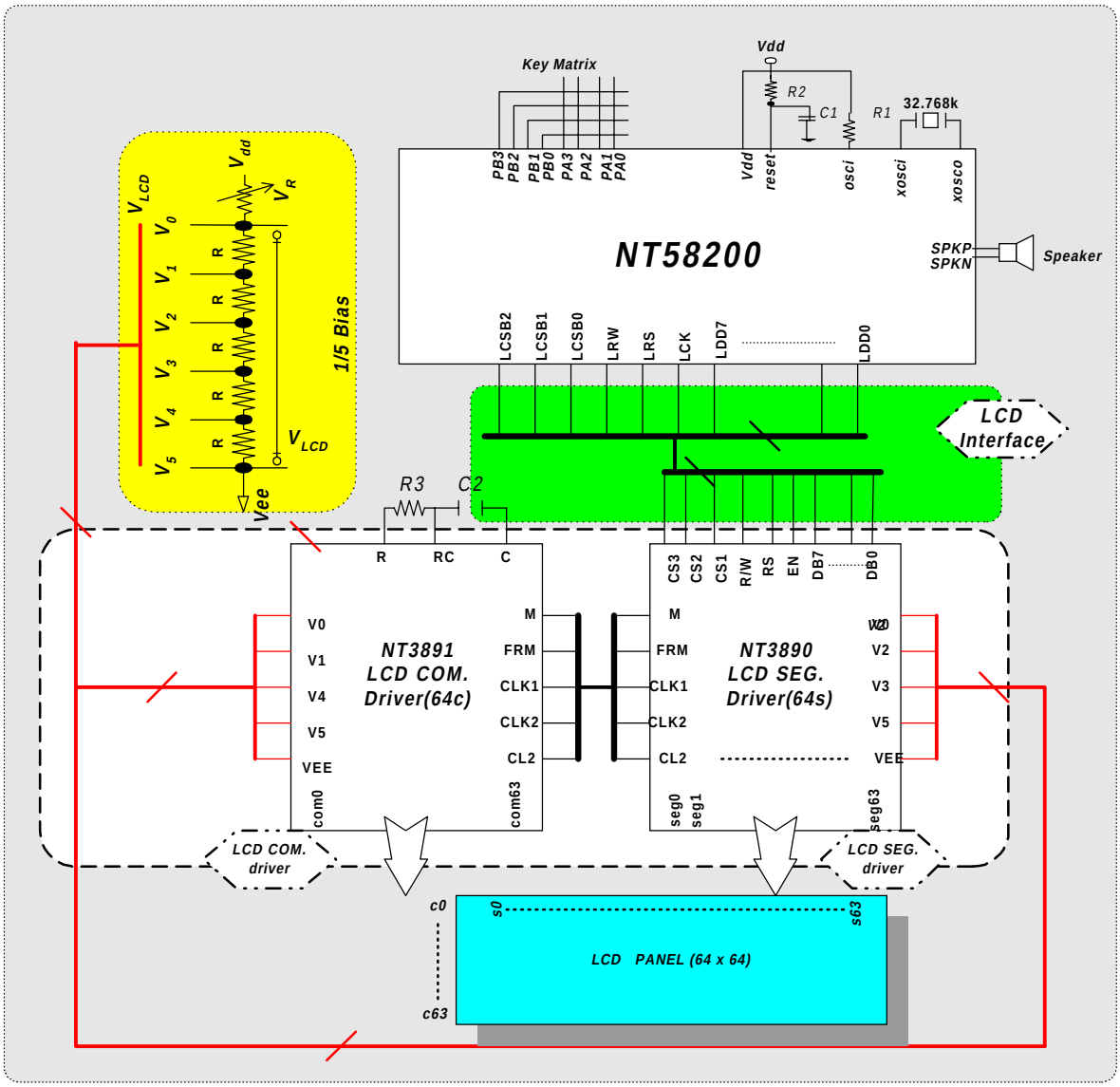


Fig.11 Application circuit (1)

Application Circuit (for reference only)(b)

(X'tal mode; LCD interface with the multi-chip LCD drivers)

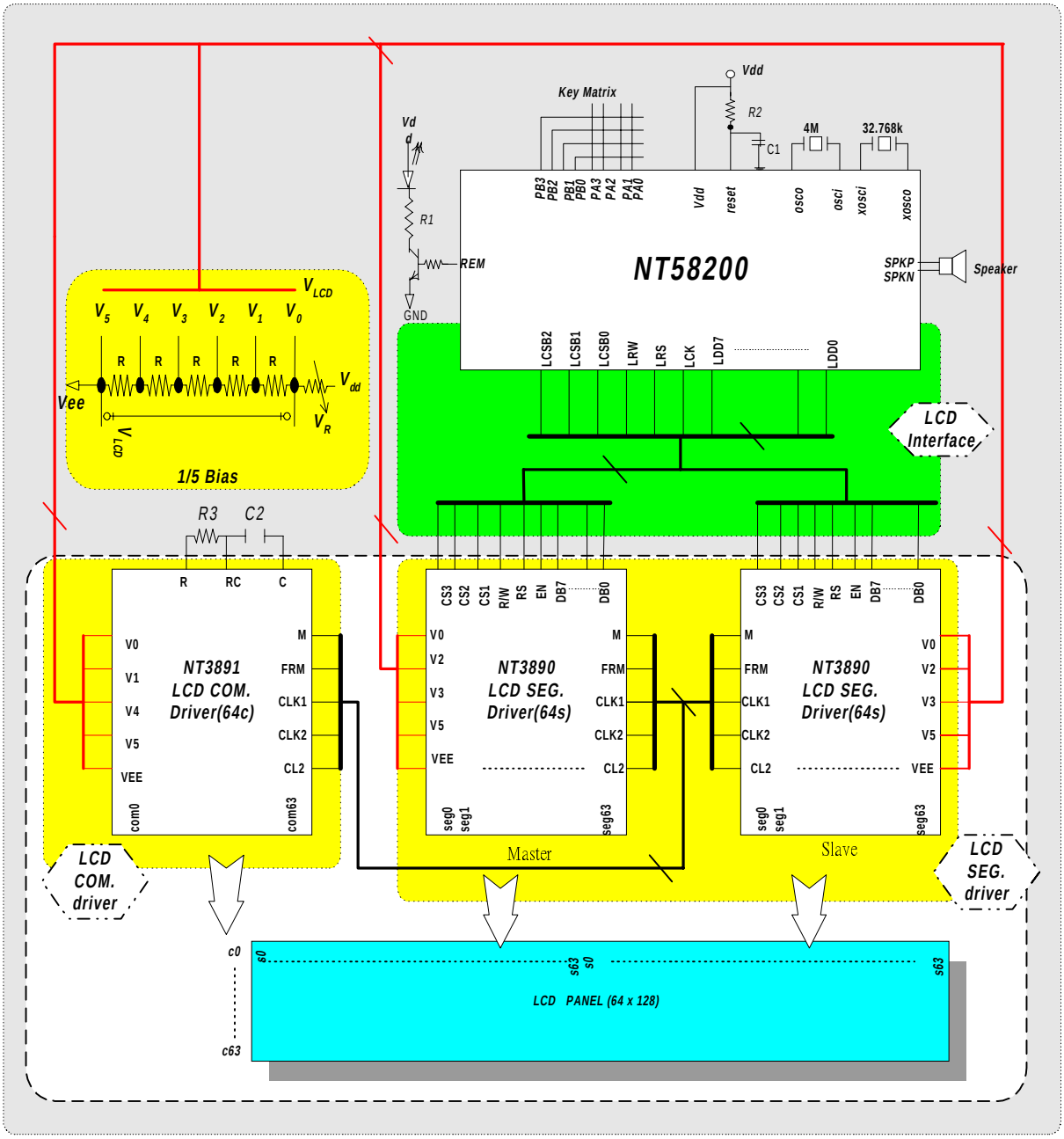


Fig.12 Application circuit (2)

APPENDIX A (tone base frequency)

	FREQ.(ideal)	M1BASE	FREQ.(real)	(Dn-Bn)/Bn%	(Dn-Bn)/(Bn-Bn-1)%	M1BASE(Hex)
A2#	116.54	245	116.60	0.05	0.05	F5
B2	123.47	260	123.51	0.03	0.58	104
C3	130.81	275	130.75	-0.05	-0.82	113
C3#	138.59	292	138.89	0.22	3.86	124
D3	146.83	308	146.71	-0.08	-1.46	134
D3#	155.56	327	155.47	-0.06	-1.03	147
E3	164.81	346	164.47	-0.21	-3.68	15A
F3	174.61	368	174.58	-0.02	-0.31	170
F3#	185.00	389	184.91	-0.05	-0.87	185
G3	196.00	414	196.54	0.28	4.91	19E
G3#	207.65	436	206.95	-0.34	-6.01	1B4
A3	220.00	463	220.07	0.03	0.57	1CF
A3#	233.08	491	233.21	0.06	0.99	1EB
B3	246.94	518	246.06	-0.36	-6.35	206
C4	261.31	548	260.42	-0.34	-6.19	224
C4#	277.18	581	276.55	-0.23	-3.97	245
D4	293.66	620	294.81	0.39	6.98	26C
D4#	311.13	657	312.50	0.44	7.84	291
E4	329.63	691	328.94	-0.21	-3.73	2B3
F4	349.23	738	351.12	0.54	9.64	2E2
F4#	369.99	782	372.03	0.55	9.83	30E
G4	392.00	821	390.63	-0.35	-6.22	335
G4#	415.30	875	416.66	0.33	5.84	36B
A4	440.00	925	440.14	0.03	0.57	39D
A4#	466.16	980	466.42	0.06	0.99	3D4
B4	493.88	1042	496.03	0.44	7.76	412
C5	523.25	1094	520.83	-0.46	-8.24	446
C5#	554.37	1172	558.04	0.66	11.79	494
D5	587.33	1238	589.62	0.39	6.95	4D6
D5#	622.25	1312	625.00	0.44	7.88	520
E5	659.26	1396	664.89	0.85	15.21	574
F5	698.46	1458	694.44	-0.58	-10.26	5B2
F5#	739.99	1562	744.04	0.55	9.75	61A
G5	783.99	1640	781.25	-0.35	-6.23	668
G5#	830.61	1726	822.36	-0.99	-17.70	6BE
A5	880.00	1822	868.05	-1.36	-24.20	71E
A5#	932.33	1929	919.12	-1.42	-25.24	789
B5	987.77	2050	976.56	-1.13	-20.22	802
C6	1046.50	2186	1041.66	-0.46	-8.24	88A
C6#	1108.73	2342	1116.00	0.66	11.68	926
D6	1174.66	2434	1157.40	-1.47	-26.18	982
D6#	1244.51	2623	1250.00	0.44	7.86	A3F
E6	1318.51	2732	1302.08	-1.25	-22.20	AAC
F6	1396.91	2980	1420.00	1.65	29.45	BA4
F6#	1479.98	3122	1488.09	0.55	9.76	C32
G6	1567.98	3278	1562.50	-0.35	-6.23	CCE
G6#	1661.22	3451	1644.74	-0.99	-17.67	D7B
A6	1760.00	3642	1736.11	-1.36	-24.19	E3A
A6#	1864.66	3857	1838.00	-1.43	-25.47	F11
B6	1975.53	4098	1953.12	-1.13	-20.21	1002