Document No. : 031-MP29A-02

DATA SHEET

Product	Battery Protect Solution IC
Product code	**MP29A** (001-MP29A-00)
Production Form	TEP - 5L,BD44
Date of Registration	May. 15. 2006

Issued	Checked	Approved
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4/4	4/4	4/4

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■ Contents

■ Features

1. Protection IC and Common Drain Dual-Nch MOSFET are integrated into One-packaging IC.

2. Reduced Pin-Count by fully connecting internally.

3. Protection IC (MITSUMI社)

① Uses high withstand voltage CMOS process
- Charger connection section absolute maximum rating 32V.

② Detection voltage precision
- Overcharge detection voltage
  ±25 ㎷ (Ta=25℃), ±45 ㎷ (Ta=-30~75℃)
- Overdischarge detection voltage
  ±35 ㎷ (Ta=25℃), ±75 ㎷ (Ta=-30~75℃)
- Discharge overcurrent detection voltage
  ±10 ㎷ (Ta=25℃), ±20 ㎷ (Ta=-30~75℃)
- Charging overcurrent detection voltage
  ±20 ㎷ (Ta=25℃), ±40 ㎷ (Ta=-30~75℃)

③ Built-in detection delay times (timer circuit)
- Overcharge detection delay time
  ±0.2 s (Ta=25℃), +0.5s, −0.4 s (Ta=-30~75℃)
- Overdischarge detection delay time
  ±4 ㎳ (Ta=25℃), +10㎳, −8㎳ (Ta=-30~75℃)
- Discharge overcurrent detection delay time
  ±1.2 ㎳ (Ta=25℃), +3.0㎳, −2.4㎳ (Ta=-30~75℃)
- Charging overcurrent detection delay time
  ±1.6 ㎳ (Ta=25℃), +4㎳ −3.2㎳ (Ta=-30~75℃)
- Short detection delay time
  +160㎲, −120㎲ (Ta=25℃), +400㎲, −200㎲ (Ta=-30~75℃)

④ With abnormal charger detection function

⑤ 0V charge function allowed

4. Common Drain Dual-Nch MOSFET (AOS社)

① Using advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltage as low as 2.5V while retaining a 12V $V_{GS(MAX)}$.

② ESD protected

③ Common drain configuration

④ General characteristics
- V_{DS} (V) = 30V
- I_D (A) = 8A
- $R_{SS(ON)}$ < 46mΩ (V_{GS} = 4.5V , I_D = 5A)
- ESD Rating : 2000V HBM

■ Outline

This is a battery protect solution IC which is integrated the protection IC developed for 1-cell series use in lithium ion/lithium polymer secondary batteries and Dual-Nch MOSFET. It functions to protect the battery by detecting overcharge, overdischarge, discharge overcurrent and other abnormalities and turning off internal Nch MOSFET. The protection IC is composed of four voltage detectors, short detection circuit, reference voltage sources, oscillator, counter circuit and logical circuits.

The C_{OUT} pin (charge FET control pin) and D_{OUT} pin (discharge FET control pin) outputs are CMOS output, and can drive the internal Nch MOSFET directly. The C_{OUT} output becomes low level after delay time fixed in the IC if overcharge is detected. The D_{OUT} output becomes low level after delay time fixed in the IC if overdischarge, discharge overcurrent or short is detected.
On overcharge state, if the V_{DD} voltage is less than the overcharge release voltage, the C_{OUT} output becomes high level after delay time fixed in the IC.

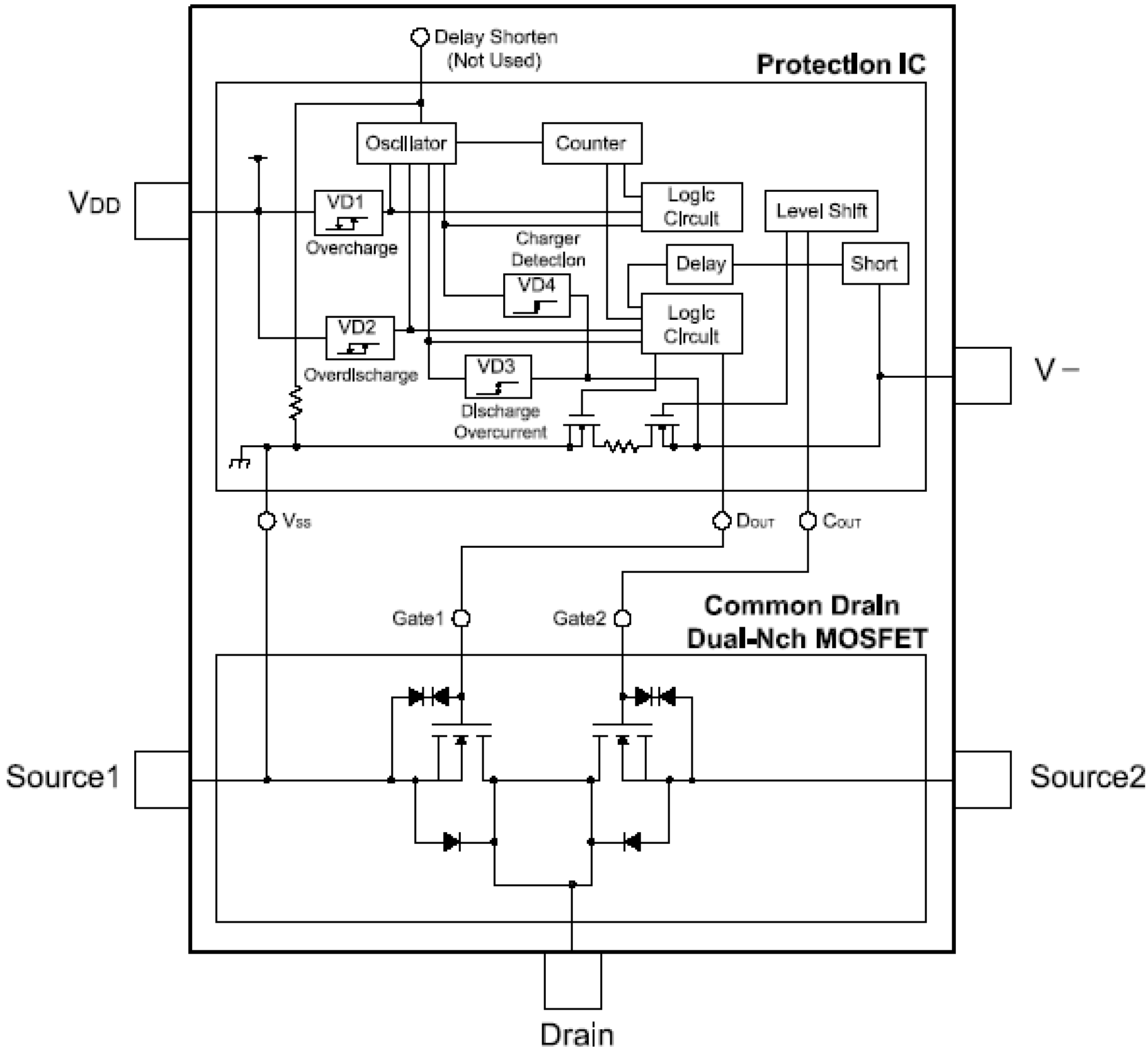
Once overdischarge has been detected, overdischarge is released and the D_{OUT} output becomes high level after delay time fixed in the IC, if the voltage of the battery rises more than the overdischarge detection voltage with connecting the charger, or more than the overdischarge release voltage without connecting the charger. Charging current can be supplied to the battery discharged up to 0V. Once discharge overcurrent or short has been detected, the state of discharge overcurrent or short is released by opening the loads, and the D_{OUT} output becomes high level after delay time fixed in the IC. On overdischarge state, the supply current is reduced as less as possible.

■ Pin Assignment

TEP-5L
<TOP VIEW>

1	T_P (NC)
2	Source 1
3	Source 2
4	V_{DD}
5	V−

■ Block Diagram



■ Absolute Maximum Rating

※ T_{OPR}=25℃, Source1(V_{SS})=0V

Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	-0.3 ~ 12	V
V- Terminal Input Voltage	V-	V_{DD}-32 ~ V_{DD}+0.3	V
C_{OUT} Terminal Output Voltage	V_{COUT}	V_{DD}-32 ~ V_{DD}+0.3	V
D_{OUT} Terminal Output Voltage	V_{DOUT}	V_{SS}-0.3 ~ V_{DD}+0.3	V
Operation Temperature	T_{OPR}	-40 ~ +85	℃
Storage Temperature	T_{STG}	-55 ~ +125	℃
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±12	V

■ Electrical Characteristics

※ T_{OPR}=25℃

Item	Symbol	Measure Condition	Min.	Typ.	Max.	Unit	*1
Operating Input Voltage	$V_{DD}1$	V_{DD} - V_{SS}	1.5	-	10.0	V	A
Current Consumption	I_{DD}	V_{DD} = 3.9V, V- = 0V	-	3.0	6.0	㎂	H
Current Consumption at Stand-By	I_S	V_{DD} = 2.0V	-	0.2	0.5	㎂	H
Overcharge Detection Voltage	$V_{DET}1$	R1 = 1㏀	4.250	4.275	4.300	V	B
Overdischarge Detection Voltage	$V_{DET}2$	V- = 0V R1 = 1㏀	2.765	2.800	2.835	V	D
Overdischarge Release Voltage	$V_{REL}2$	R1 = 1㏀	2.930	3.000	3.070	V	D
Discharging Overcurrent Detection Voltage	$V_{DET}3$	V_{DD} = 3V R2 = 2.2㏀	0.040	0.050	0.060	V	F
Discharging Overcurrent Detection Current	-	V_{DD} = 3V R2 = 2.2㏀	0.77	1.13	1.76	A	F
Charging Overcurrent Detection Voltage	$V_{DET}4$	V_{DD} = 3V R2 = 2.2㏀	-0.095	-0.075	-0.055	V	G
Charging Overcurrent Detection Current	-	V_{DD} = 3V R2 = 2.2㏀	-2.94	-1.70	-0.96	A	G
Short Detection Voltage	V_{SHORT}	V_{DD} = 3V	V_{DD}-1.2	V_{DD}-0.9	V_{DD}-0.6	V	F

※ T_{OPR}=25℃

Item	Symbol	Measure Condition	Min.	Typ.	Max.	Unit	*1
Overcharge Detection Delay Time	$tV_{DET}1$	V_{DD} = 3.6V → 4.6V	0.8	1.0	1.2	s	B
Overdischarge Detection Delay Time	$tV_{DET}2$	V_{DD} = 3.6V → 2.2V	16.0	20.0	24.0	㎳	D
Discharging Overcurrent Detection Delay Time	$tV_{DET}3$	V_{DD} = 3V, V- = 0V → 1V	4.8	6.0	7.2	㎳	D
Charging Overcurrent Detection Delay Time	$tV_{DET}4$	V_{DD} = 3V, V- = 0V → -1V	6.4	8.0	9.6	㎳	F
Short Detection Delay Time	t_{SHORT}	V_{DD} = 3V, V- = 0V → 3V	280	400	560	㎲	F
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250㎂, V_{GS}=0V	30	-	-	V	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=24V, V_{GS}=0V T_J=55℃	-	-	1 5	㎂	
Gate-Body Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±10V	-	-	10	㎂	
Gate-Source Breakdown Voltage	BV_{GSO}	V_{DS}=0V, I_G=±250㎂	±12	-	-	V	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250㎂	0.6	1.0	1.5	V	
Static Source-Source ON-Resistance	$R_{SS(ON)}$	V_{GS}=10V, I_D=5A T_J=125℃	-	34 52	40 62	mΩ	
		V_{GS}=4.5V, I_D=5A	-	40	46	mΩ	
		V_{GS}=2.5V, I_D=3A	-	52	66	mΩ	
Diode Forward Voltage	V_{SD}	I_S=1A, V_{GS}=0V	0.50	0.76	0.90	V	
Maximum Body-Diode Continuous Current	I_S		-	-	4.5	A	

Note : *1 The test circuit symbols.

※ T_{OPR}=-30~75℃

Item	Symbol	Measure Condition	Min.	Typ.	Max.	Unit	*1
Overcharge Detection Voltage	$V_{DET}1$	R1 = 1kΩ	4.230	4.275	4.320	V	B
Overdischarge Detection Voltage	$V_{DET}2$	V- = 0V R1 = 1kΩ	2.725	2.800	2.875	V	D
Overdischarge Release Voltage	$V_{REL}2$	V- = 0V R1 = 1kΩ	2.910	3.000	3.090	V	D
Discharging Overcurrent Detection Voltage	$V_{DET}3$	V_{DD} = 3V R2 = 2.2kΩ	0.030	0.050	0.070	V	F
Charging Overcurrent Detection Voltage	$V_{DET}4$	V_{DD} = 3V R2 = 2.2kΩ	-0.115	-0.075	-0.035	V	G
Short Detection Voltage	V_{SHORT}	V_{DD} = 3V	V_{DD}-1.2	V_{DD}-0.9	V_{DD}-0.6	V	F
Overcharge Detection Delay Time	$tV_{DET}1$	V_{DD} = 3.6V → 4.6V	0.6	1.0	1.5	s	B
Overdischarge Detection Delay Time	$tV_{DET}2$	V_{DD} = 3.6V → 2.2V	12.0	20.0	30.0	ms	D
Discharging Overcurrent Detection Delay Time	$tV_{DET}3$	V_{DD} = 3V, V- = 0V → 1V	3.6	6.0	9.0	ms	D
Charging Overcurrent Detection Delay Time	$tV_{DET}4$	V_{DD} = 3V, V- = 0V → -1V	4.8	8.0	12.0	ms	F
Short Detection Delay Time	t_{SHORT}	V_{DD} = 3V, V- = 0V → 3V	200	400	800	µs	F

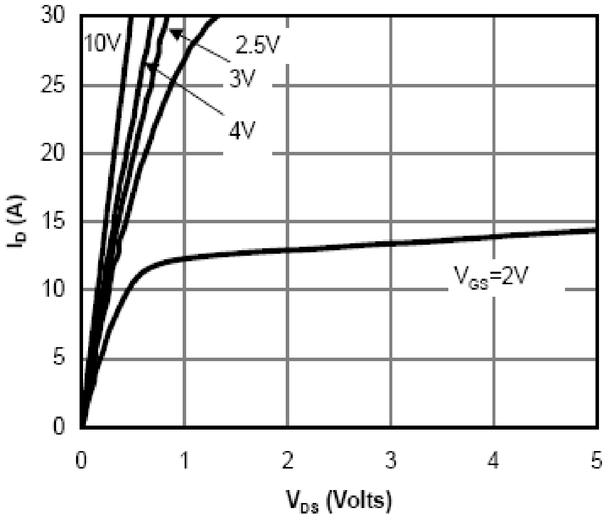


Figure 1 : On-Regin Characteristics

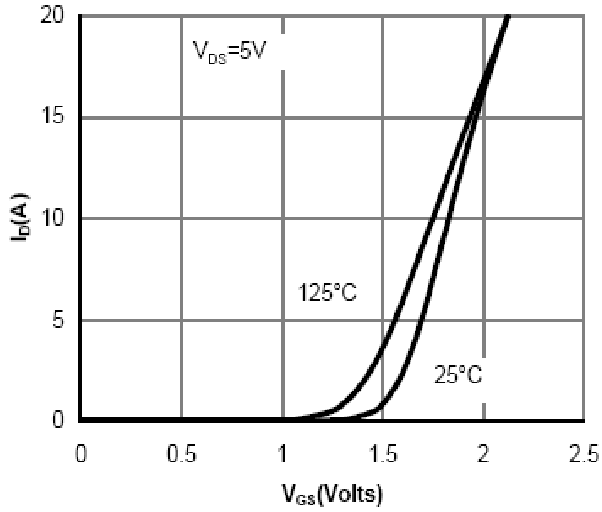


Figure 2: Transfer Characteristics

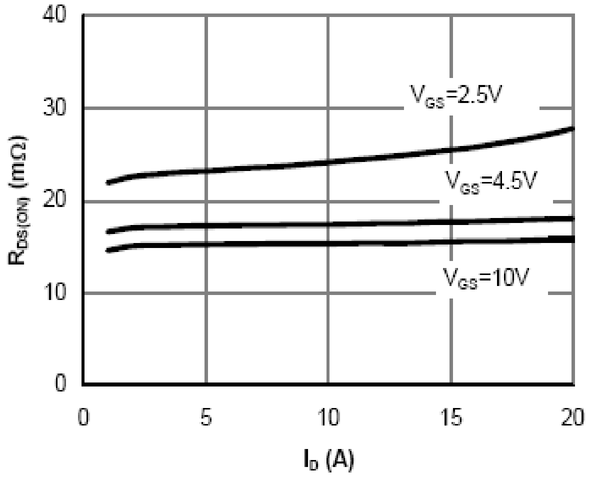


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

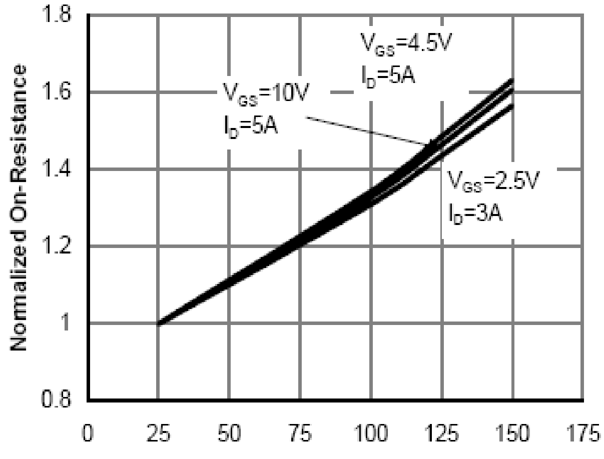


Figure 4: On-Resistance vs. Junction Temperature

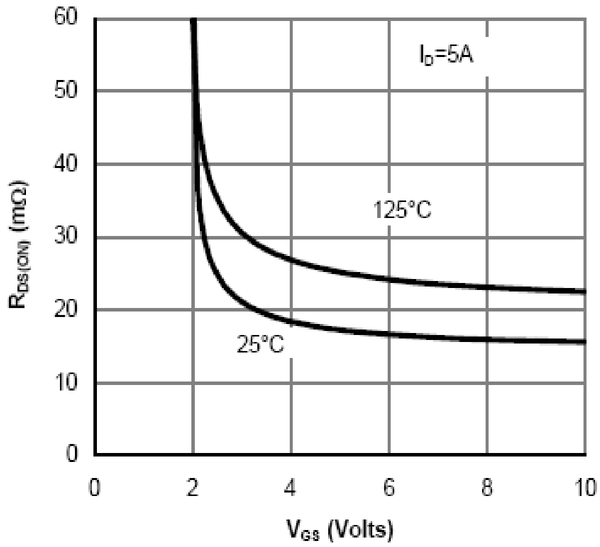


Figure 5: On-Resistance vs. Gate-Source Voltage

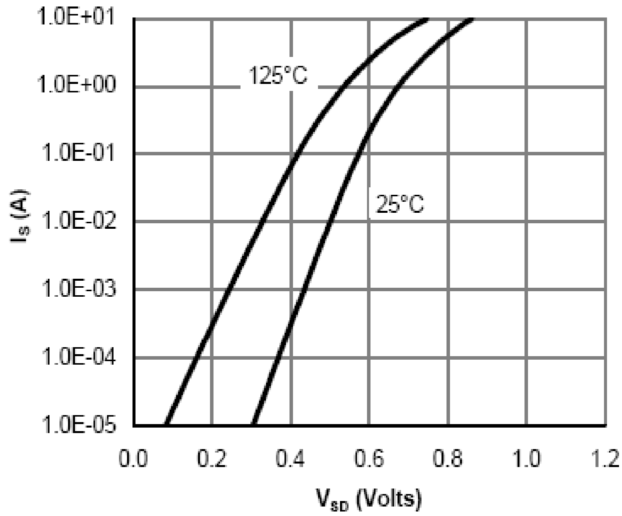


Figure 6: Body-Diode Characteristics

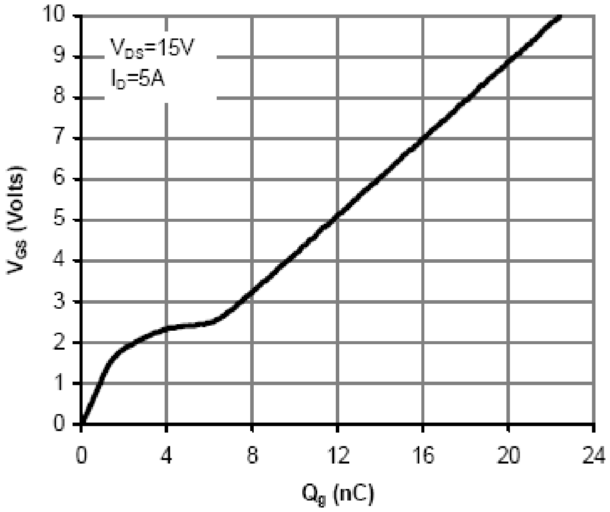


Figure 7: Gate-Charge Characteristics

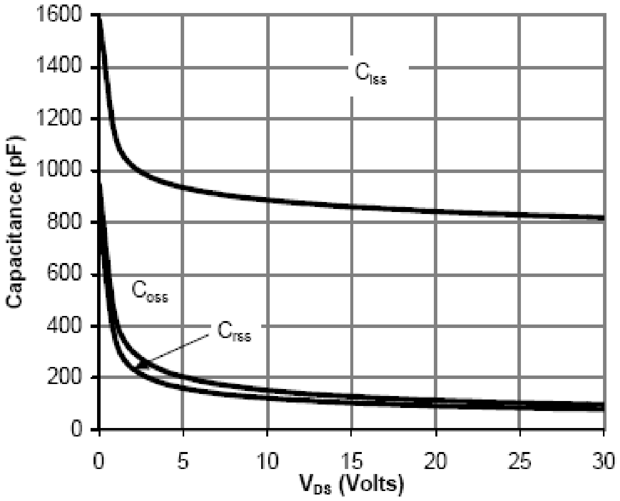
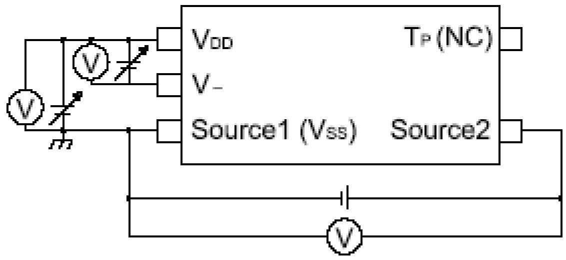


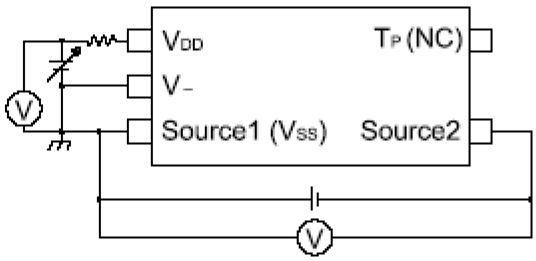
Figure 8: Capacitance Characteristics

■ Measuring Circuit

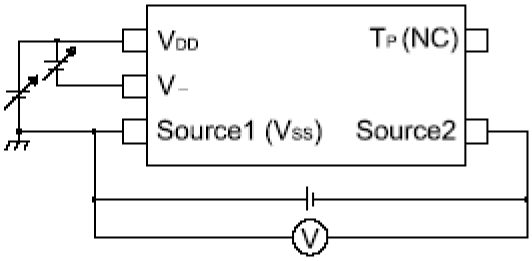
A.



B.



C.



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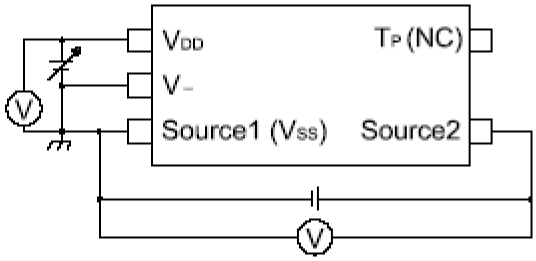

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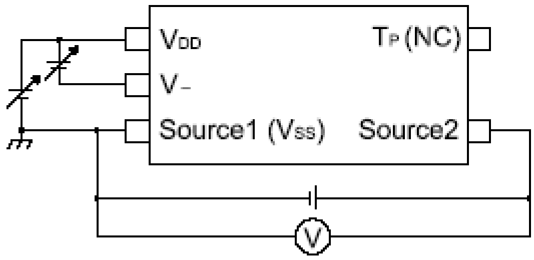

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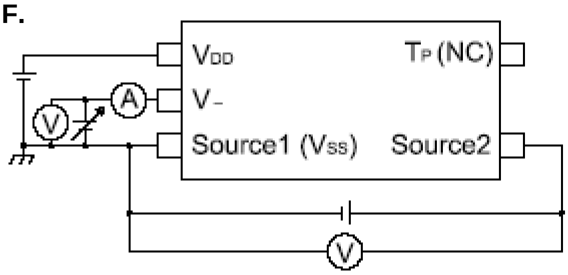
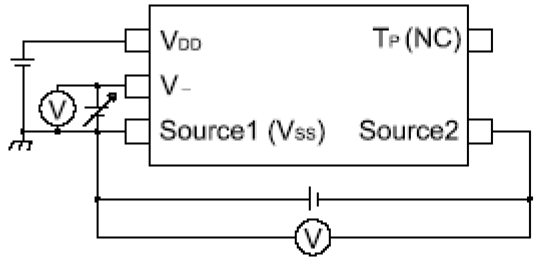
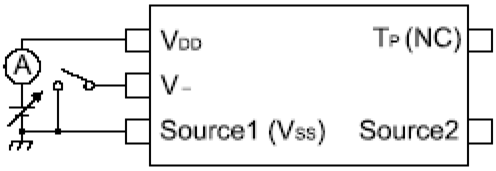


G.



H.



■ Operation

1. Overcharge detector (VD1)

VD1 monitors V_{DD} terminal voltage, and when the voltage of V_{DD} terminal crosses overcharge detection voltage (Typ. 4.275V) from the low value to the value higher than the overcharge detection voltage, VD1 sense a overcharging and an internal charging control Nch MOSFET turns to OFF with C_{OUT} terminal being low level.

After detecting overcharge when the V_{DD} terminal voltage is coming down to a level lower than overcharge release voltage, internal charging control Nch MOSFET turns to ON with C_{OUT} terminal being high level.

After detecting overcharge in the V_{DD} terminal voltage, connecting system load to the battery charger side makes load current allowable supplied to parasitic diode of charging control FET. The C_{OUT} terminal level would be high when the V_{DD} terminal level is lower than the overcharge detection voltage, so the internal Nch MOSFET turns ON, and it accepts to charge the battery.

There are delay time set in the protection IC when the overcharge and the overcharge release are detected. When the V_{DD} level is going up to a level higher than overcharge detection voltage if the V_{DD} voltage would be back to a level lower than the overcharge detection voltage within a time period of the overcharge detection delay time (Typ. 1.0s). The overcharge detection does not release when returning to former state in the overcharge release delay time even if the load is connected after the charger is removed when the V_{DD} terminal voltage is lower than the overcharge release voltage with the overcharge detected.

A level shifter incorporated in a buffer drive for the C_{OUT} to the V- terminal voltage and the high level of C_{OUT} is set to V_{DD} voltage with CMOS buffer.

2. Overdischarge detector (VD2)

VD2 monitors V_{DD} terminal voltage, and when the voltage crosses the overdischarge detection voltage (Typ. 2.800V) from high value to a value lower than the overdischarge detection voltage, VD2 sense an overdischarge and an internal discharging control Nch MOSFET turns to OFF with D_{OUT} terminal being at low level.

Once overdischarge has been detected, overdischarge is released and the D_{OUT} output becomes high level, if the voltage of the battery rises more than the overdischarge detection voltage with connecting the charger, or more than the overdischarge release voltage without connecting the charger. Charging current is supplied through a parasitic diode of Nch MOSFET when the V_{DD} terminal voltage is below the overdischarge detection voltage to the connection of the charger, and the D_{OUT} terminal enters the state which can be discharged by becoming high level, and turning on Nch MOSFET when the V_{DD} terminal voltage rises more than the overdischarge detection voltage.

The C_{OUT} terminal becomes high level and charging current is supplied if the voltage of the charger is more than the maximum value of 0V charging lowest operating voltage when the voltage of the battery is 0V.

An output delay time (Typ. 20ms) for the overdischarge detection is fixed internally. When V_{DD} terminal voltage becomes lower the overdischarge detection voltage if V_{DD} terminal higher more than the over discharge detection voltage in delay time even does not enter the overdischarge detection mode. Moreover, when the overdischarge release, delay time is set.

All the circuits are stopped, and after the overdischarge is detected, it is assumed the state of the standby, and decreases the current (standby current) which IC consumes as much as possible.

Output type of D_{OUT} terminal is CMOS having high level of V_{DD} and low level of V_{SS}.

3. Overcurrent detector, Short detector (VD3, Short Detector)

When the V- terminal voltage is going up to a value during the short detection voltage (Typ. V_{DD}-0.9V) and overdischarge current detection voltage (Typ. 0.050V) is overdischarge current detection mode, when the V- terminal voltage higher than short detection voltage makes the short detection mode. This leads the internal discharge control Nch MOSFET turns to OFF with the D_{OUT} terminal being at low level.

An output delay time for the overdischarge current detection (Typ. 6ms) is fixed internally. When V- terminal voltage becomes during the overdischarge current detection voltage and the short circuit detection if V- terminal lowers more than the over discharge curent detection voltage in delay time even does not enter the over discharge current detection mode.

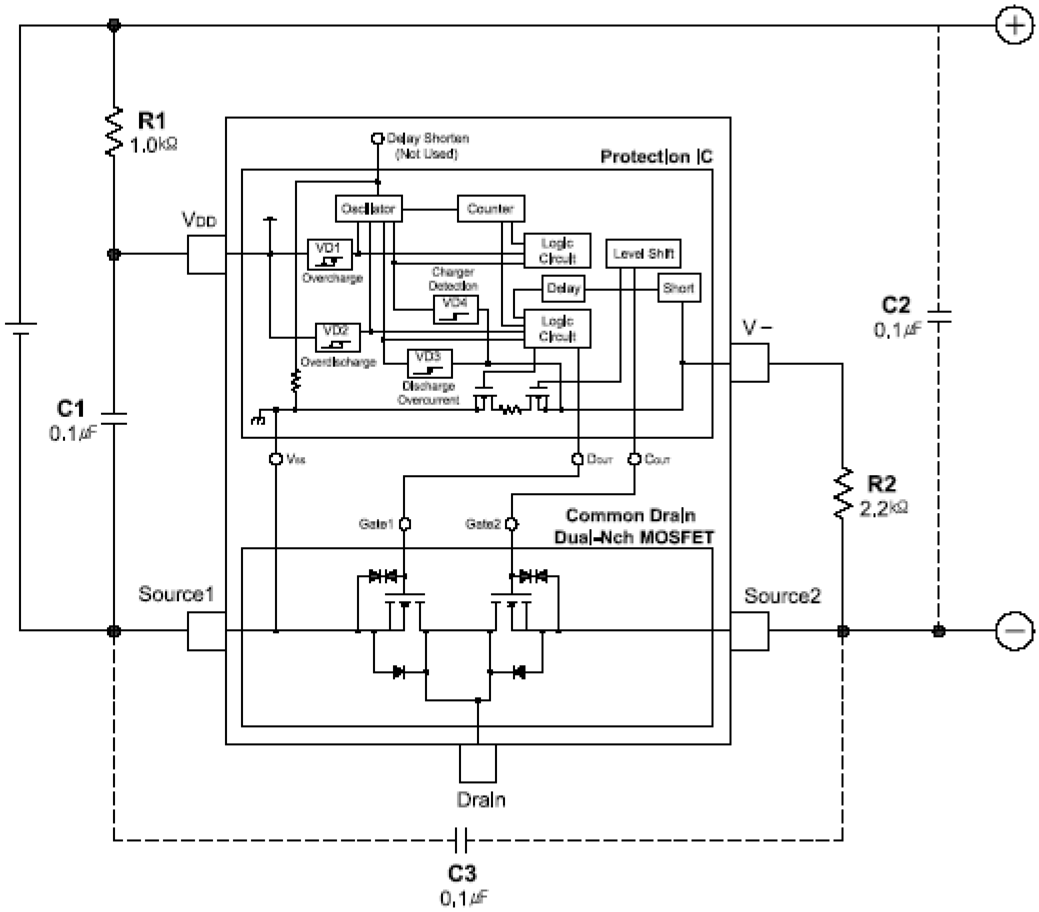
The delay time set in IC exists when the short circuit is detected (Typ. 400μs).

The overcurrent release resistance is built into between V- terminal and V_{SS} terminal. When the load opened after detecting the overdischarge current or the short circuit. V- terminal is pulled down to the V_{SS} through the overdischarge current release resistance, and IC returns automatically from the overdischarge current or the short circuit detection mode when V- terminal voltage becomes below the overdischarge current detection voltage. When the overdischarge current or the short circuit is detected, the overdischarge current release resistance is turned on. The overdischarge current release resistance is usually turned OFF on the normal state (chargable or dischargable state).

4. Charger detector (VD4)

VD4 monitors V- terminal voltage, when D_{OUT} output becomes high level, and V- terminal voltage is coming down to a level lower than the charger detection voltage. If excess current can flow, then the V- terminal voltage drops below the charger detection voltage. This prevents current flow into the circuit by turning OFF the internal Nch MOSFET with the C_{OUT} terminal being at low level. Charger detection releases when V- terminal is coming up to a high level than the charger detection voltage.

■ Application Circuit (Example)



Application Hint

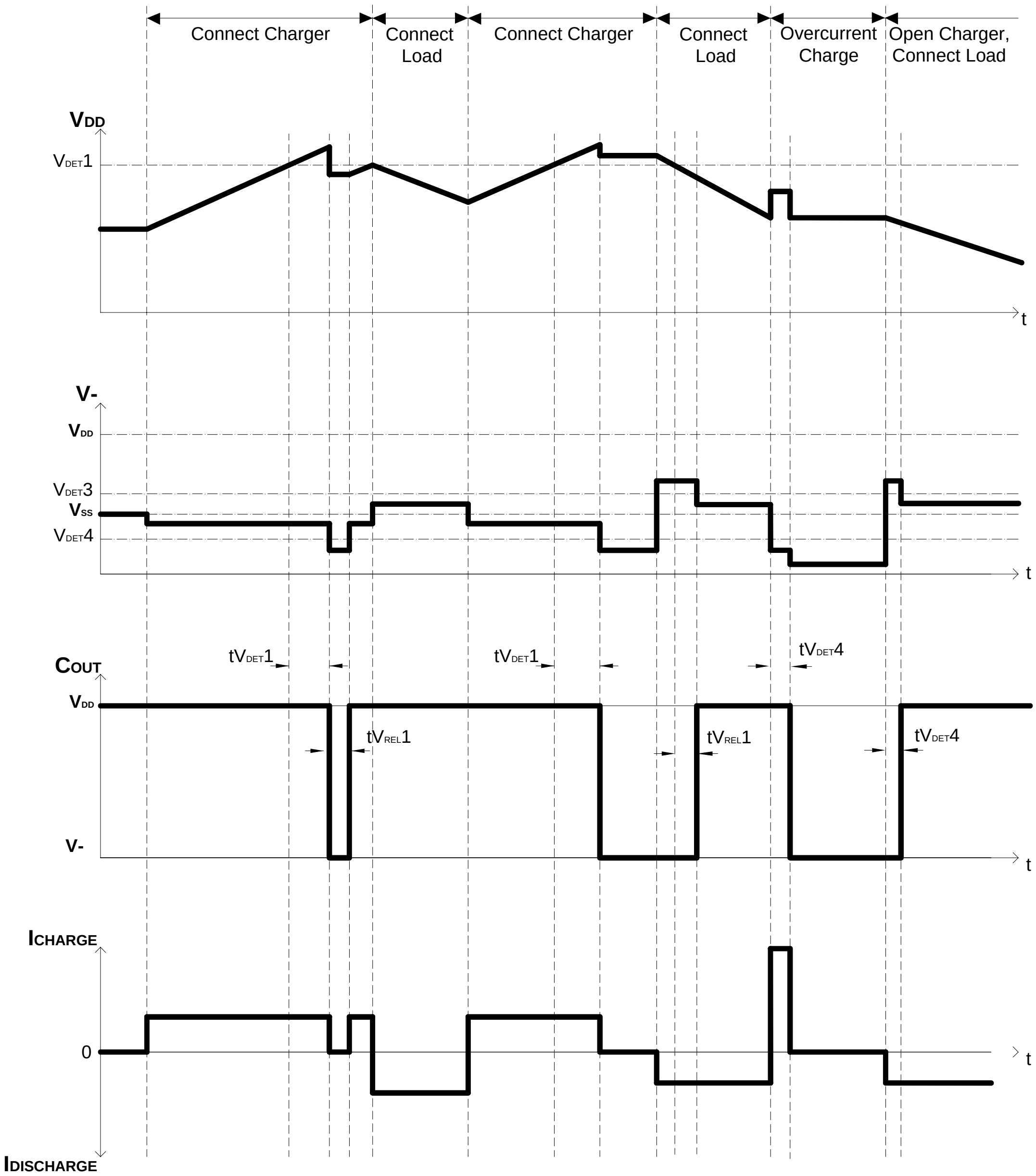
R1 and C1 stabilize a supply voltage ripple. However, the detection voltage rises by the current of penetration in IC of the voltage detection when R1 is enlarged, and the value of R1 is adjusted to 1kΩ. Moreover, adjust the value of C1 to 0.1µF or more to do the stability operation, please.

R1 and R2 resistors are current limit resistance if a charger is connected reversibly or a high-voltage charger that exceeds the absolute maximum ration is connected. R1 and R2 may cause a power consumption will be over rating of power dissipation, therefore the R1+R2 should be more than 1kΩ. Moreover, if R2 is too enlarged, the charger connection release cannot be occasionally done after the overdischarge is detected, so adjust the value of R2 to 10kΩ or less, please.

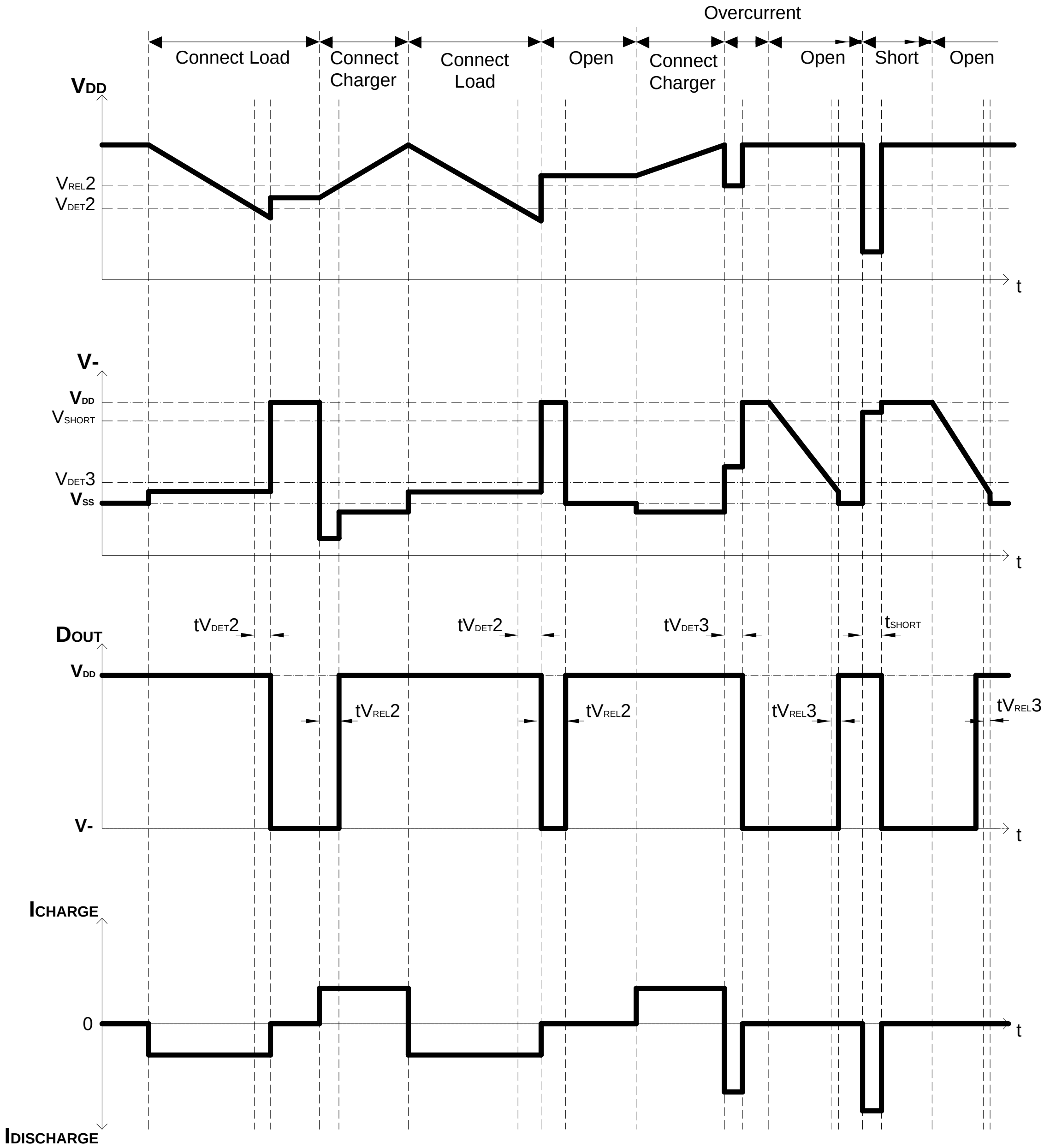
C2 and C3 capacitors have effect that the system stability about voltage ripple or imported noise. After check characteristics, decide that these capacitors should be inserted or not, where should be inserted, and capacitance value, please.

■ Timing Chart

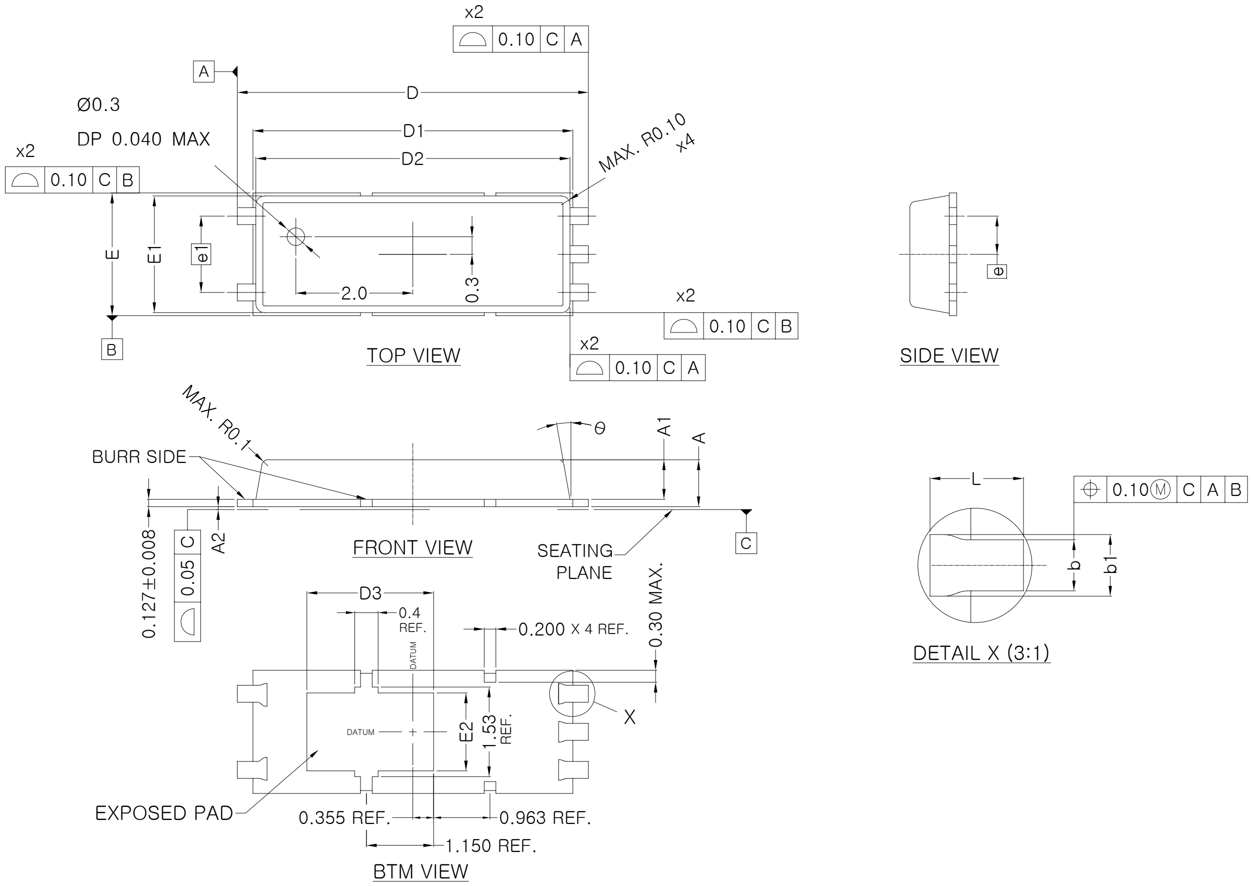
1. Overcharge, Abnormal Charger operations



2. Overdischarge, Discharging Overcurrent and Short operations



■ Package Description



SYMBOL	DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.750	0.800	0.850	
A1	0.623	0.673	0.723	
A2	–	–	0.050	
D	5.900	6.000	6.100	
D1	5.320	5.370	5.420	
D2	5.270	5.320	5.370	
D3	2.220 REF.			
E	2.000	2.100	2.200	
E1	1.950	2.000	2.050	
E2	1.330 REF.			
Θ	–	–	10 °	
e	0.650 BSC			
e1	1.300 BSC			
L	0.410	–	–	
b	0.240	0.290	0.340	
b1	0.300	0.350	0.400	

NOTE

1. LEAD BURR : VERTICAL MAX 0.025
   HORIZONTAL MAX 0.025
   BURR SIDE : ALL TOP SIDE
2. MOLD BURR & FLASH : PACKAGE OUT LINE BURR MAX 0.100
   EXPOSED PAD FLASH MAX 0.200
3. PACKAGE WARPAGE MAX 0.025
4. LEAD AND EXPOSED PAD PLATING : PURE TIN
   THICKNESS> 7.62~25.4um

■ Marking Contents