



AO4801H

Dual P-Channel Enhancement Mode Field Effect Transistor

General Description

The AO4801H uses advanced trench technology to provide excellent $R_{\text{DS(ON)}}$ with low gate charge. This device is suitable for use as a load switch or in PWM applications.

Features

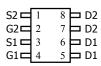
 $V_{DS}(V) = -30V$

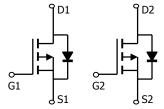
 $I_{\rm D} = -5 \, {\rm A}$

 $R_{DS(ON)}$ < 52m Ω (V_{GS} = -10V)

 $R_{DS(ON)}$ < 87m Ω (V_{GS} = -4.5V)

SOIC-8 Top View





Absolute Maximum Ratings T _A =25°C unless otherwise noted						
Parameter		Symbol	Maximum	Units		
Drain-Source Voltage		V_{DS}	-30	V		
Gate-Source Voltage		V_{GS}	±20	V		
Continuous Drain	T _A =25°C		-5			
Current ^A	T _A =70°C	I _D	-4.2	A		
Pulsed Drain Current ^B		I _{DM}	-20			
	T _A =25°C	В	2	14/		
Power Dissipation ^A	T _A =70°C	$-P_D$	1.4	W		
Junction and Storage Temperature Range		T _J , T _{STG}	-55 to 150	°C		

Thermal Characteristics						
Parameter	Symbol	Тур	Max	Units		
Maximum Junction-to-Ambient A	t ≤ 10s	$R_{\theta JA}$	48	62.5	°C/W	
Maximum Junction-to-Ambient A	Steady-State	$\kappa_{\theta JA}$	74	110	°C/W	
Maximum Junction-to-Lead ^C	Steady-State	$R_{\theta JL}$	35	40	°C/W	

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Тур	Max	Units	
STATIC F	PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D =-250 μ A, V_{GS} =0V		-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24V, V _{GS} =0V				-1	μА
-033	Zero Gato Venago Brain Garrent	T _J =55°C				-5	μ
I_{GSS}	Gate-Body leakage current	V_{DS} =0V, V_{GS} =±20V				±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ $I_{D}=-250\mu A$		-1	-1.8	-3	V
$I_{D(ON)}$	On state drain current	V _{GS} =-4.5V, V _{DS} =-5V		-10			Α
		V _{GS} =-10V, I _D =5.0A			39	52	mΩ
$R_{DS(ON)}$	Static Drain-Source On-Resistance	-	T _J =125°C		54	70	11122
		V_{GS} =-4.5V, I_D =-4A			67	87	mΩ
g FS	Forward Transconductance	V _{DS} =-5V, I _D =-5A		6	8.6		S
V_{SD}	Diode Forward Voltage	I _S =-1A,V _{GS} =0V			-0.77	-1	V
I_S	Maximum Body-Diode Continuous Current					-2.8	Α
DYNAMIC	PARAMETERS						
C_{iss}	Input Capacitance				700		pF
C _{oss}	Output Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz			120		pF
C _{rss}	Reverse Transfer Capacitance				75		pF
R_g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz			10		Ω
SWITCHI	NG PARAMETERS						
Q _g (10V)	Total Gate Charge (10V)	-V _{GS} =-10V, V _{DS} =-15V, I _D =-5A			14.7		nC
Q _g (4.5V)	Total Gate Charge (4.5V)				7.6		nC
Q_{gs}	Gate Source Charge				2		nC
Q_{gd}	Gate Drain Charge				3.8		nC
t _{D(on)}	Turn-On DelayTime				8.3		ns
t _r	Turn-On Rise Time	V_{GS} =-10V, V_{DS} =-15V, R_L =3 Ω , R_{GEN} =3 Ω			5		ns
t _{D(off)}	Turn-Off DelayTime				29	_	ns
t _f	Turn-Off Fall Time				14		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-5A, dI/dt=100A/μs			23.5		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-5A, dI/dt=100A/μs	_	_	13.4		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any a given application depends on the user's specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

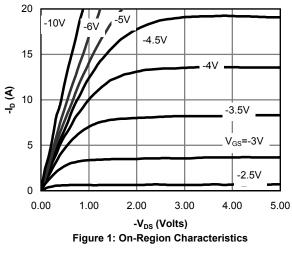
B: Repetitive rating, pulse width limited by junction temperature.

C. The R $_{\theta JA}$ is the sum of the thermal impedence from junction to lead R $_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using $80\,\mu s$ pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



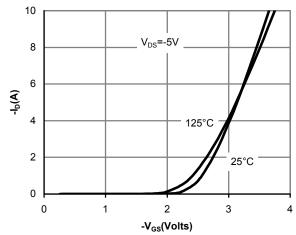


Figure 2: Transfer Characteristics

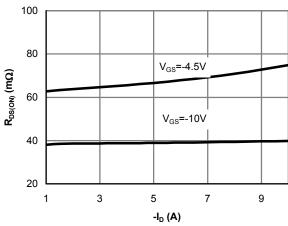


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

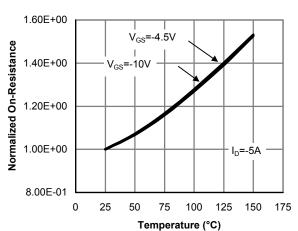


Figure 4: On-Resistance vs. Junction Temperature

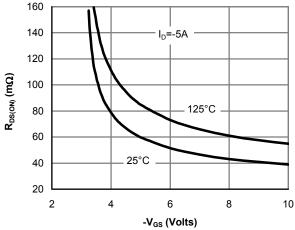


Figure 5: On-Resistance vs. Gate-Source Voltage

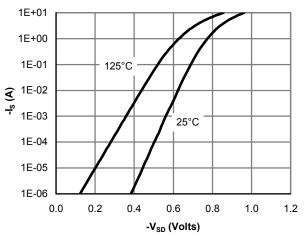


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

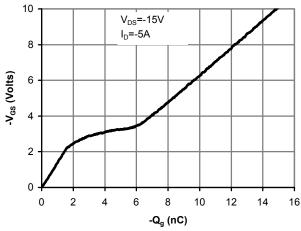


Figure 7: Gate-Charge Characteristics

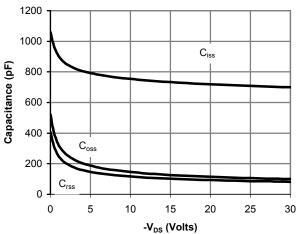


Figure 8: Capacitance Characteristics

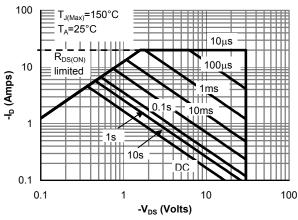


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

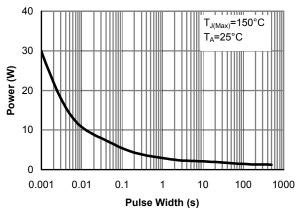


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

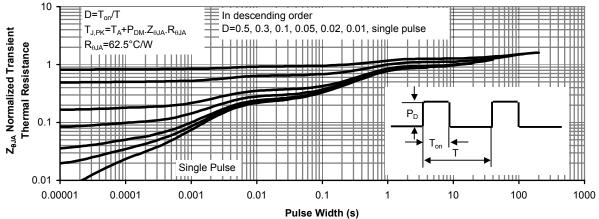
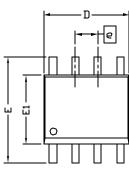
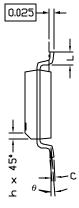


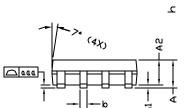
Figure 11: Normalized Maximum Transient Thermal Impedance



SO-8 Package Data







SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES			
	MIN	NOM	MAX	MIN	NOM	MAX	
A	1.45	1.50	1.55	0.057	0.059	0.061	
A1	0.00		0.10	0.000		0.004	
A2		1.45			0.057		
b	0.33		0.51	0.013		0.020	
С	0.19		0.25	0.007		0.010	
D	4.80		5.00	0.189		0.197	
E1	3.80		4.00	0.150		0.157	
e	1.27 BSC			0.050 BSC			
E	5.80		6.20	0.228		0.244	
h	0.25		0.50	0.010		0.020	
L	0.40		1.27	0.016		0.050	
aaa			0.10			0.004	
θ	0°		8°	0°		8°	

- NOTE: 1. LEAD FINISH: 150 MICROINCHES (3.8 um) MIN. THICKNESS OF Tin/Lead (SOLDER) PLATED ON LEAD 2. TOLERANCE ±0.10 mm (4 mil) UNLESS OTHERWISE SPECIFIED

- 3. COPLANARITY : 0.10 mm 4. DIMENSION L IS MEASURED IN GAGE PLANE

PACKAGE MARKING DESCRIPTION



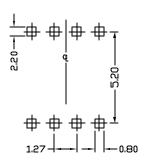
NOTE:

LOGO - AOS LOGO

4801H - PART NUMBER CODE.
F - FAB LOCATION
A - ASSEMBLY LOCATION
Y - YEAR CODE
W - WEEK CODE.

- ASSEMBLY LOT CODE LC

RECOMMENDED LAND PATTERN



UNIT: mm

SOP-8 PART NO. CODE

PART NO.	CODE
AO4801H	4801H

