Powerking Electronics (ShenZhen) Co., LTD.
深圳市柏健電子有限公司
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承认书

SPCEIFICATION FOR APPROVER

客户名称 (Customer Name)	迈科科技有限公司
日　　期 (Date)	2008-04-10
品　　牌(Brand)	BCD
型　　号(Parts No)	AZ7500CM-E1

客户签章(Customer' s Signature)

全部承认(Pull Approved)	
日　　期(Date)	17/4-08

General Description

The AZ7500B/C is a voltage mode pulse width modulation switching regulator control circuit designed primarily for power supply control.

The AZ7500B/C consists of a reference voltage circuit, two error amplifiers, an on-chip adjustable oscillator, a dead-time control (DTC) comparator, a pulse-steering control flip-flop, and an output control circuit. The precision of voltage reference (V_{REF}) is improved up to ± 1% through trimming and this provides a better output voltage regulation. The AZ7500B/C provides for push-pull or single-ended output operation, which can be selected through the output control.

The difference between AZ7500B and AZ7500C is that they have 4.95V and 5V reference voltage respectively.

The AZ7500B/C is available in standard packages of DIP-16 and SOIC-16.

Features

- Stable 4.95V/5V Reference Voltage Trimmed to ±1.0% Accuracy
- Uncommitted Output TR for 200mA Sink or Source Current
- Single-End or Push-Pull Operation Selected by Output Control
- Internal Circuitry Prohibits Double Pulse at Either Output
- Complete PWM Control Circuit with Variable Duty Cycle
- On-Chip Oscillator with Master or Slave Operation

Applications

- SMPS
- Back Light Inverter
- Charger

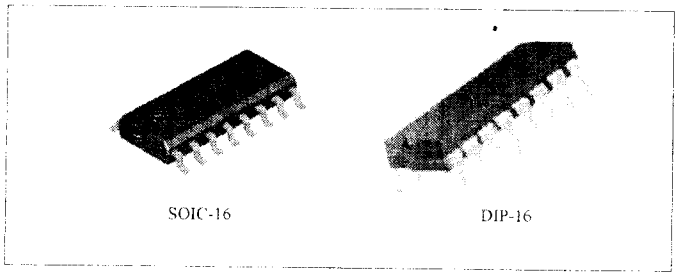


Figure 1. Package Types of AZ7500B/C

Advanced Analog Circuits

Data Sheet

PULSE-WIDTH-MODULATION CONTROL CIRCUITS AZ7500B/C

Pin Configuration

M/P Package
(SOIC-16/DIP-16)

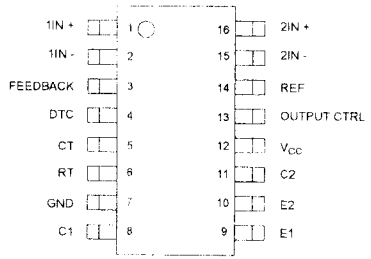


Figure 2. Pin Configuration of AZ7500B/C (Top View)

Output Function Control Table

Signal for Output Control	Output Function
V_I = GND	Single-ended or parallel output
V_I = V_{REF}	Normal push-pull operation

Functional Block Diagram

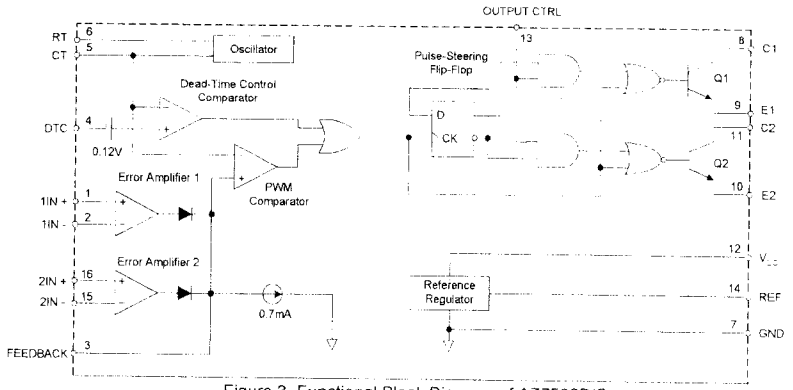
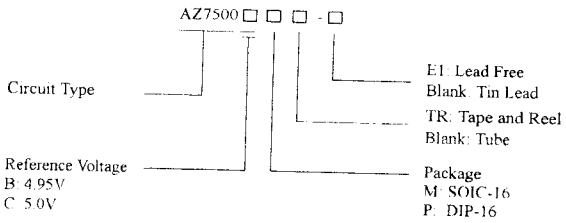


Figure 3. Functional Block Diagram of AZ7500B/C

Ordering Information



Package	Temperature Range	Part Number		Marking ID		Packing Type
		Tin Lead	Lead Free	Tin Lead	Lead Free	
SOIC-16	-40 to 85°C	AZ7500BM	AZ7500BM-E1	AZ7500BM	AZ7500BM-E1	Tube
		AZ7500BMTR	AZ7500BMTR-E1	AZ7500BM	AZ7500BM-E1	Tape & Reel
		AZ7500CM	AZ7500CM-E1	AZ7500CM	AZ7500CM-E1	Tube
		AZ7500CMTR	AZ7500CMTR-E1	AZ7500CM	AZ7500CM-E1	Tape & Reel
DIP-16		AZ7500BP	AZ7500BP-E1	AZ7500BP	AZ7500BP-E1	Tube
		AZ7500CP	AZ7500CP-E1	AZ7500CP	AZ7500CP-E1	Tube

BCD Semiconductor's Pb-free products, as designated with "E1" suffix in the part number, are RoHS compliant

Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Value		Unit
Supply Voltage (Note 2)	V_{CC}	40		V
Amplifier Input Voltage	V_I	-0.3 to V_{CC} + 0.3		V
Collector Output Voltage	V_O	40		V
Collector Output Current	I_O	250		mA
Package Thermal Impedance (Note 3)	$R_{\theta JA}$	M Package	73	°C/W
		P Package	67	
Lead Temperature 1.6mm from case for 10 seconds		260		°C
Storage Temperature Range	T_{STG}	-65 to 150		°C
ESD rating (Machine Model)		200		V

Note 1: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

Note 2: All voltage values are with respect to the network ground terminal.

Note 3: Maximum power dissipation is a function of $T_J(max)$, $R_{\theta JA}$ and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	7	15	36	V
Collector Output Voltage	V_{C1}, V_{C2}		30	36	V
Collector Output Current (Each Transistor)	I_{C1}, I_{C2}			200	mA
Amplifier Input Voltage	V_I	0.3		V_{CC} - 2	V
Current Into Feedback Terminal	I_{FB}			0.3	mA
Reference Output Current	I_{REF}			10	mA
Timing Capacitor	C_T	0.00047	0.001	10	μF
Timing Resistor	R_T	1.8	30	500	KΩ
Oscillator Frequency	f_{osc}	1.0	40	200	KHz
PWM Input Voltage (Pin 3, 4, 14)		0.3		5.3	V
Operating Free-Air Temperature	T_A	-40		85	°C

Electrical Characteristics

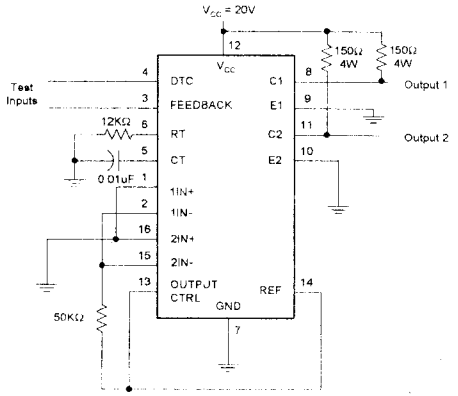
T_A = 25°C, V_{CC}=20V, f=10KHz unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reference Section						
Output Reference Voltage for AZ7500B	V_{REF}	I_{REF}=1mA	4.90	4.95	5.0	V
		I_{REF}=1mA, T_A= -40 to 85°C	4.85	4.95	5.05	V
Output Reference Voltage for AZ7500C	V_{REF}	I_{REF}=1mA	4.95	5.0	5.05	V
		I_{REF}=1mA, T_A= -40 to 85°C	4.9	5.0	5.1	V
Line Regulation	R_{LINE}	V_{CC} = 7V to 36V		2	25	mV
Load Regulation	R_{LOAD}	I_{REF}=1mA to 10mA		1	15	mV
Short-Circuit Output Current	I_{SC}	V_{REF} = 0V	10	35	50	mA
Oscillator Section						
Oscillator Frequency	f_{OSC}	C_T=0.001μF, R_T=30KΩ		40		KHz
		C_T=0.01μF, R_T=12KΩ	9.2	10	10.8	
		C_T=0.01μF, R_T=12KΩ, T_A= -40 to 85°C	9.0		12	
Frequency Change with Temperature	Δf/ΔT	C_T=0.01μF, R_T=12KΩ, T_A= -40 to 85°C			1	%
Dead-Time Control Section						
Input Bias Current	I_{BIAS}	V_{CC}=15V, V4= 0 to 5.25V		-2	-10	μA
Maximum Duty Cycle	D(MAX)	V_{CC}=15V, V4= 0V, Pin 13= V_{REF}	45			%
Input Threshold Voltage	V_{ITH}	Zero Duty Cycle		3	3.3	V
		Maximum Duty Cycle	0			
Error-Amplifier Section						
Input Offset Voltage	V_{IO}	V3 = 2.5V		2	10	mV
Input Offset Current	I_{IO}	V3 = 2.5V		25	250	nA
Input Bias Current	I_{BIAS}	V3 = 2.5V		0.2	1	μA
Common-Mode Input Voltage Range	V_{CM}	V_{CC}=7V to 36V	-0.3		V_{CC}-2	V
Open-Loop Voltage Gain	G_{VO}	V_O=0.5V to 3.5V	70	95		dB
Unity-Gain Bandwidth	BW			650		KHz
Common-Mode Rejection Ratio	CMRR		65	80		dB
Output Sink Current (Feedback)	I_{SINK}	V_{ID} = -15mV to -5V, V3 = 0.7V	-0.3	-0.7		mA
Output Source Current (Feedback)	I_{SOURCE}	V_{ID}=15mV to 5V V3 = 3.5V	2			mA

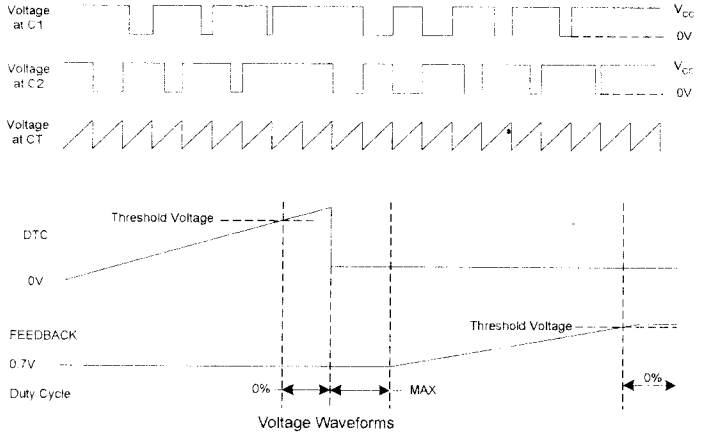
Electrical Characteristics (Continued)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
PWM Comparator Section							
Input Threshold Voltage		V_{ITH}	Zero duty cycle		4	4.5	V
Input Sink Current		I_{SINK}	V3 = 0.7V	-0.3	-0.7		mA
Output Section							
Output Saturation Voltage	Common Emitter	V_{CE} (SAT)	V_E = 0V, I_C =200mA		1.1	1.3	V
	Emitter Follower	V_{CC} (SAT)	V_{CC} = 15V, I_E = -200mA		1.5	2.5	
Collector Off-State Current		I_C (OFF)	V_{CE} = 36V, V_{CC}=36V		2	100	μA
Emitter Off-State Current		I_E(OFF)	V_{CC} = V_C = 36V, V_E = 0			-100	μA
Total Device							
Supply Current		I_{CC}	Pin 6 = V_{REF}, V_{CC}=15V		6	10	mA
Output Switching Characteristics							
Rise Time		t_R	Common Emitter Common Collector		100	200	ns
Fall Time		t_F	Common Emitter Common Collector		25	100	ns

Parametr Measurement information



Test Circuit



Voltage Waveforms

Figure 4. Operational Test Circuit and Waveforms

Parametr Measurement information (Continued)

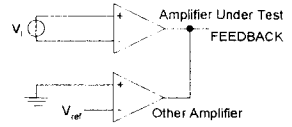
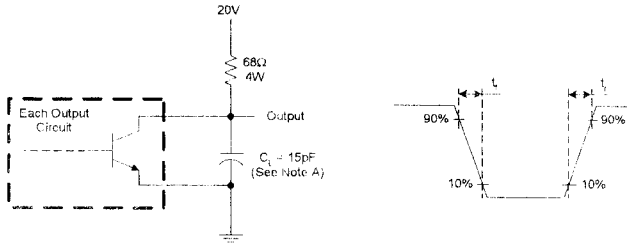
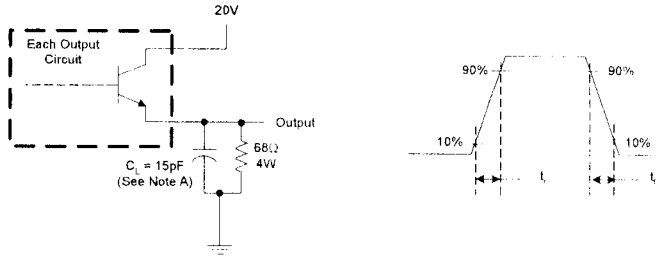


Figure 5. Error Amplifier Characteristics



Note A: C_L includes probe and jig capacitance.

Figure 6. Common-Emitter Configuration



Note A: C_L includes probe and jig capacitance.

Figure 7. Emitter-Follower Configuration

Typical Performance Characteristics

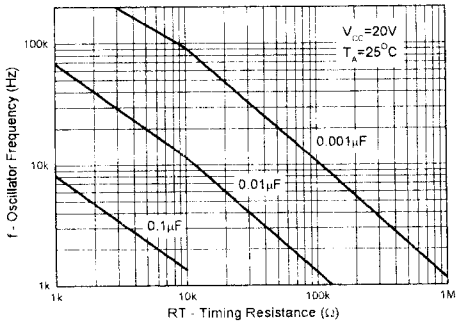


Figure 8. Oscillator Frequency vs. RT and CT

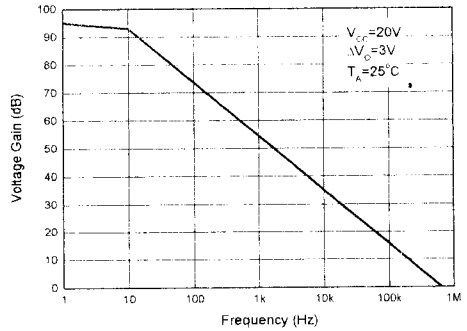


Figure 9. Error Amplifier Small-Signal Voltage Gain vs. Frequency

Typical Applications

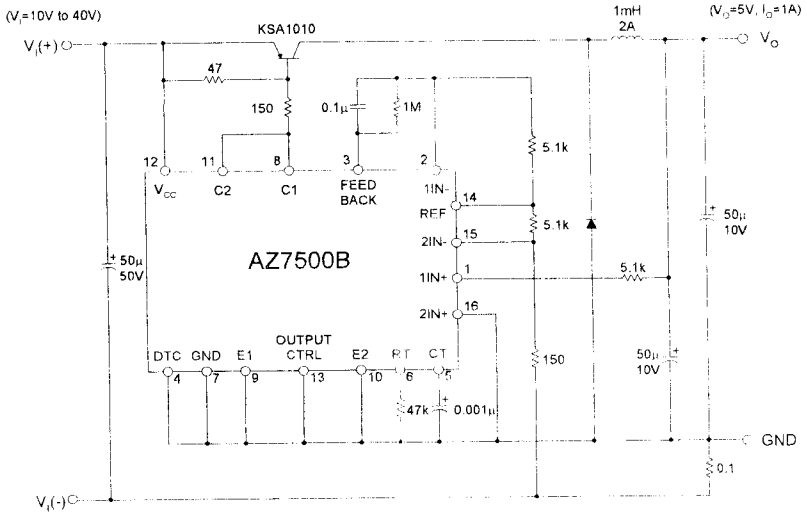
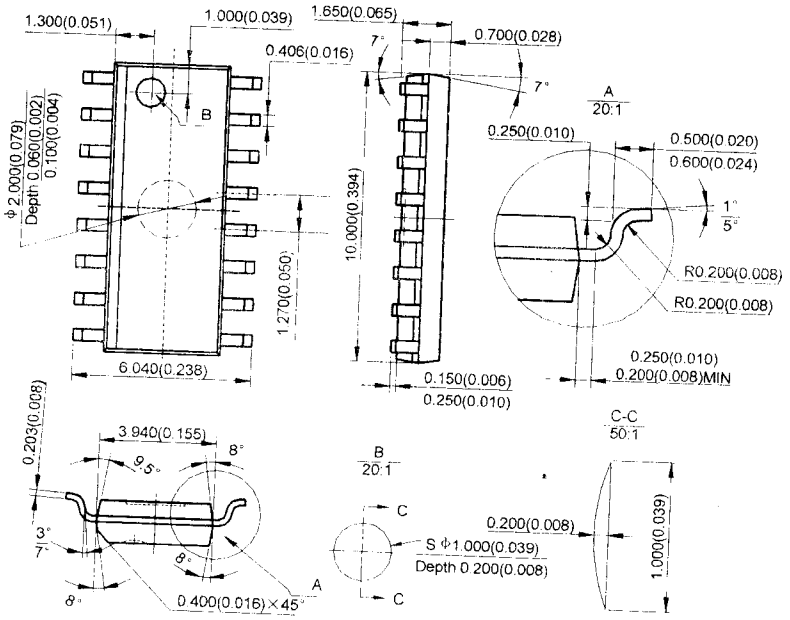


Figure 10. Pulse Width Modulated Step-Down Converter

Mechanical Dimensions

SOIC-16

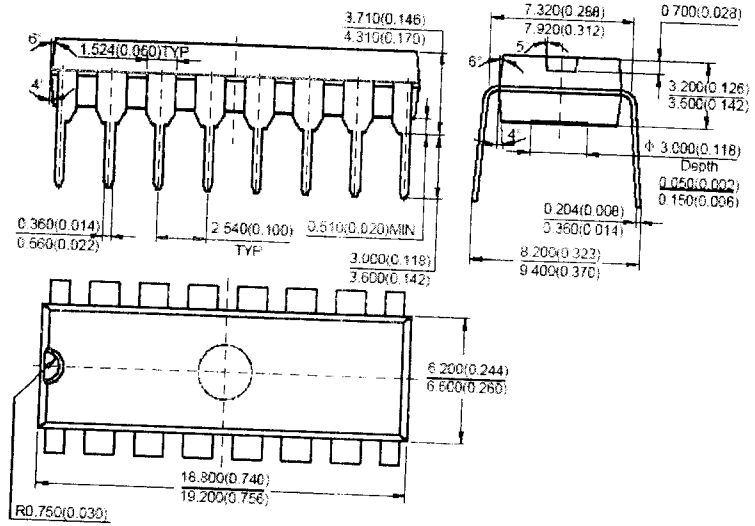
Unit: mm(inch)



Mechanical Dimensions (Continued)

DIP-16

Unit: mm(inch)



SGS

Test Report

No. SH7042944/CHEM Date: Apr. 27, 2007

JIANGSU CHANGJIANG ELECTRONIC TECHNOLOGY CO., LTD
78, CHANGSHAN RD, JIANGYIN, JIANGSU CHINA

The following sample(s) was/were submitted and identified by/on behalf of the client as:

Sample Name : SOP PACKAGE PART (INCLUDE SOP16/28)
SGS Ref No. : 10333677-7
Model : SOP (INCLUDE SOP16/28)

Sample Receiving Date : Apr.24, 2007
Testing Period : Apr.24 – Apr.27, 2007

Test Requested : (1) In accordance with the RoHS Directive 2002/95/EC, and its amendment directives
(2) To determine the PCBs (Polychlorinated Biphenyls) content of the submitted sample.
(3) To determine the Polychlorinated Naphthalene content of the submitted sample.
(4) To determine the Short Chain Chlorinated Paraffin content of the submitted sample.

Test Method : (1-1) With reference to IEC 62321 Ed.1 111/54/CDV for Cadmium content. Analysis was performed by ICP.
(1-2) With reference to IEC 62321 Ed.1 111/54/CDV for Lead content. Analysis was performed by ICP.
(1-3) With reference to IEC 62321 Ed.1 111/54/CDV for Mercury content. Analysis was performed by ICP.
(1-4) With reference to IEC 62321 Ed.1 111/54/CDV for Hexavalent Chromium by Colorimetric Method.
(1-5) With reference to IEC 62321 Ed.1 111/54/CDV for PBBs / PBDEs content. Analysis was performed by GC/MS.
(2) With reference to US EPA 8082, Analysis was performed by GC-MS.
(3) With reference to US EPA 8081, Analysis was performed by GC-MS.
(4) With reference to US EPA 8081, Analysis was performed by GC/MS.

Test Results : Please refer to next pages

Signed for and on behalf of
SGS-CSTC Chemical Laboratory

Ella Zhang
Sr. Section Head

Signed for and on behalf of
SGS-CSTC Chemical Laboratory

Sandy Hao
Lab Manager

Test results by chemical method

(1) Cadmium, Lead, Mercury, Hexavalent Chromium, PBBs(Polybrominated biphenyls) PBBEs(PBDEs) (Polybrominated biphenyl ethers) content(Unit: mg/kg)

Test Item(s):	Method (refer to)	1*	MDL	RoHS Limit
Cadmium(Cd)	(1-1)	ND	2	100
Lead (Pb)	(1-2)	11	2	1000
Mercury (Hg)	(1-3)	ND	2	1000
Hexavalent Chromium (CrVI)	(1-4)	ND	2	1000
Sum of PBBs	(1-5)	ND	-	1000
Monobromobiphenyl		ND	5	-
Dibromobiphenyl		ND	5	-
Tribromobiphenyl		ND	5	-
Tetrabromobiphenyl		ND	5	-
Hexabromobiphenyl		ND	5	-
Pentabromobiphenyl		ND	5	-
Heptabromobiphenyl		ND	5	-
Octabromobiphenyl		ND	5	-
Nonabromobiphenyl		ND	5	-
Decabromobiphenyl		ND	5	-
Sum of PBDEs (Note 4)		ND	-	1000
Monobromodiphenyl ether		ND	5	-
Dibromodiphenyl ether		ND	5	-
Tribromodiphenyl ether		ND	5	-
Tetrabromodiphenyl ether		ND	5	-
Pentabromodiphenyl ether		ND	5	-
Hexabromodiphenyl ether		ND	5	-
Heptabromodiphenyl ether		ND	5	-
Octabromodiphenyl ether		ND	5	-
Nonabromodiphenyl ether		ND	5	-
Decabromodiphenyl ether		ND	5	-
Sum of PBDEs (Mono to Deca)		ND	-	-

(2)~(4) PCBs (Polychlorinated Biphenyls) content ,Polychlorinated Naphthalene content and Short Chain Chlorinated Paraffin content (Unit: mg/kg)

Test Item(s):	Method (refer to)	1*	MDL
PCBs (Polychlorinated Biphenyls) content	(2)	-	-
2.4.4'-Trichlorobiphenyl (PCB 28) CAS 7012-37-5		ND	0.5
2.2'.5.5'-Tetrachloro-biphenyl (PCB 52) CAS 35693-99-3		ND	0.5
2.2'.4.5.5'-Pentachloro-biphenyl (PCB 101) CAS 37680-73-2		ND	0.5
2.3'.4.4'.5-Pentachlorobiphenyl (PCB 118) CAS 31508-00-6		ND	0.5
2.2'3.4.4'.5'-Hexachloro-biphenyl (PCB 138) CAS 35065-28-2		ND	0.5
2.2'.4.4'.5.5'-Hexachloro-biphenyl (PCB 153) CAS 35065-27-1		ND	0.5
2.2'.3.4.4'.5.5'-Heptachlorobiphenyl (PCB 180) CAS 35065-29-3		ND	0.5
Polychlorinated Naphthalene content	(3)	-	-
2-Chlorinated Naphthalene		ND	5
1,4-Dichlorinated Naphthalene		ND	5
1,5-Dichlorinated Naphthalene		ND	5
1,2-Dichlorinated Naphthalene		ND	5
1,8-Dichlorinated Naphthalene		ND	5
1,2,3,4-Tetrachlorinated Naphthalene		ND	5
Octa-chlorinaed Naphthalene		ND	5
Short Chain Chlorinated Paraffin	(4)	ND	30

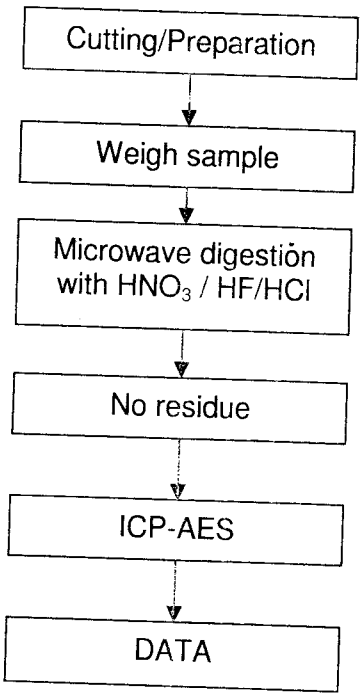
Test Part Description:
1. Black body part (mix all)

Note:

(1) mg/kg = ppm
(2) ND = Not Detected
(3) MDL = Method Detection Limit
(4) Sum of Mono to NonaBDE & according to 2005/717/EC DecaBDE is exempt.
(5) "-" = Not Regulated
(6) The maximum permissible limit is quoted from the document 2005/618/EC amending RoHS directive 2002/95/EC
(7) * The sample(s) was analyzed on behalf of the applicant as mixing whole/part sample in one testing. The result(s) in report means average of whole sample. The result(s) will be different obviously if the sample(s) was tested as requirement of RoHS, and result(s) may be higher than that of report. The applicant will take the responsibility of all discrepancy and risk.

ATTACHMENTS

Cd and Pb Measurement Flowchart



The samples were dissolved totally by pre-conditioning method according to above flow chart.

Tested by : Chaven Lian
Checked by : Terry Wang

Sample photo:

SGS authenticate the photo on original report only

*** End of Report ***