Dual slope ADC with low battery detector

Feature

- Operating Voltage: 2.4 V ~ 5.2 V
- Operation Current: 300 uA @ VDD=3V
- Standby current: 0.01 uA @ VDD=3V
- Low Battery Detect
- Sensor Signal Buffer
- Operation Amplifier
- Comparator
- Transmission Gates
- Power On/Off Control

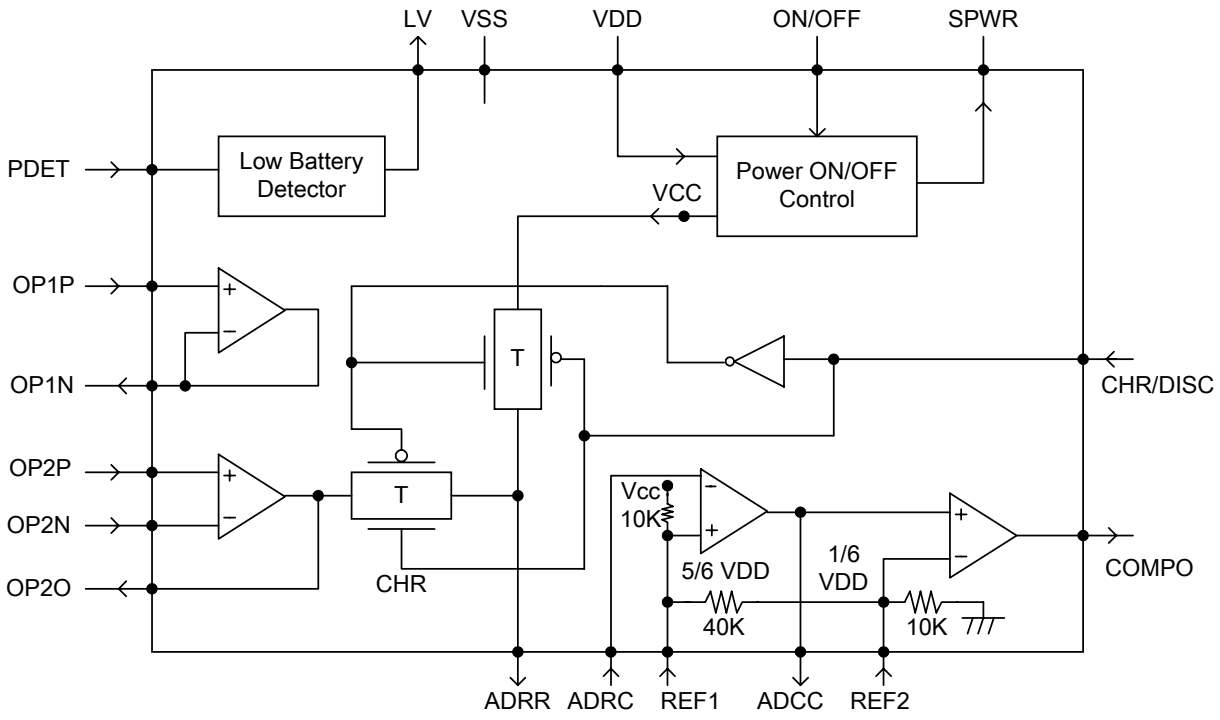
General Description

The JA32020 offers very high accuracy A/D conversion at low cost by using Dual Slope integration. It incorporates operational amplifiers, comparators, low battery detector, power on/off control circuit and charge/discharge control circuit inside to achieve high performance for application.

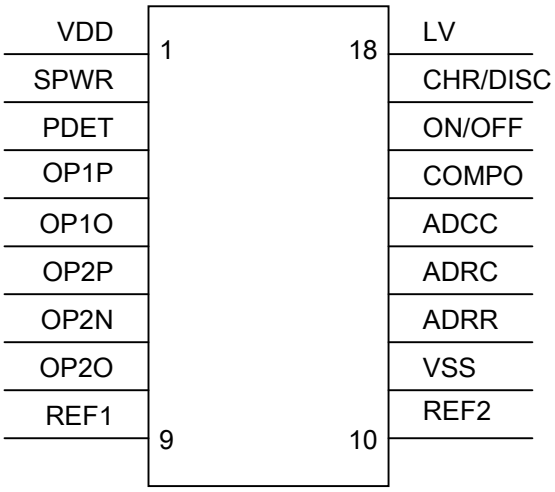
A voltage follower was used as buffer for sensor signal input. Because of the buffer's great isolating characteristic, the signal from sensor will be precisely duplicated and sent out at output pin without any distortion.

An operational amplifier was designed for user to properly amplify the sensor signal from buffer. Inside the chip, a current accurately proportional to the amplified signal level will be generated to charge an external RC network for a fixed time interval. After being charged for this interval, the capacitor is discharged by a constant current until the voltage reaches 1/6 VDD. This discharging time is proportional to the input signal level and is used by external controller to enable a counter; the final count is proportional to the input level and can be converted to digital output. Because the charge cycle and discharge cycle go through the same RC network, using a high quality capacitor is recommended.

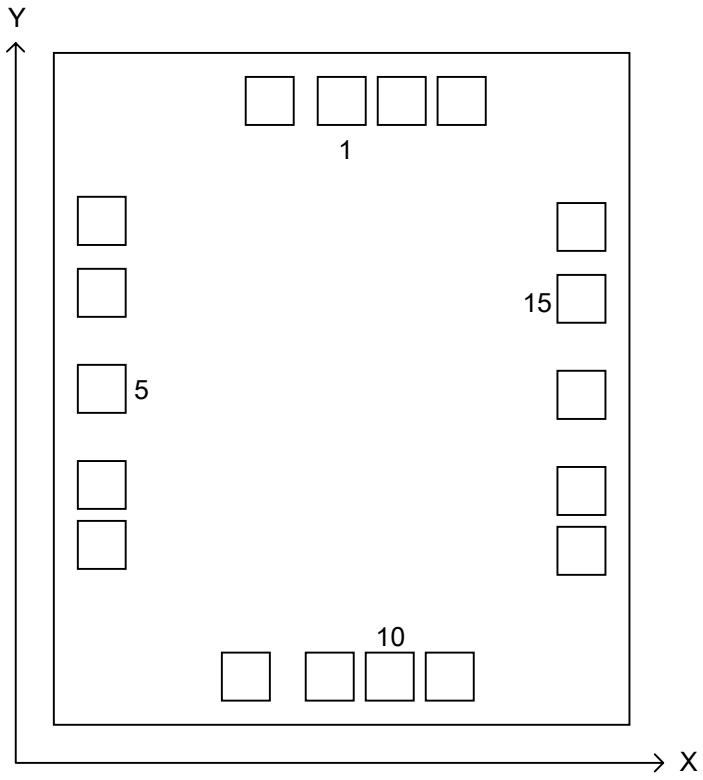
Block Diagram



Pin Assignment



Pad Assignment



Chip Size: 1150 X 1260 (uM^2)

Pad Coordinates

Pad No.	Name	X	Y	Pad No.	Name	X	Y
1	VDD	455.8	1077.0	10	REF2	617.2	53.4
2	PSWR	330.3	1077.0	11	VSS	728	53.9
3	PDET	52.1	840.2	12	ADRR	965.7	289.8
4	OP1P	46.5	719.2	13	ADRC	966.9	406.9
5	OP1O	56.7	579.2	14	ADCC	963.3	552.7
6	OP2P	56.8	403.0	15	COMPO	962.6	700.4
7	OP2N	52.3	286.4	16	ON/OFF	962.4	822.3
8	OP2O	335.2	53.0	17	CHR/DISC	683.4	1078.4
9	REF1	508.7	58.1	18	LV	572.6	1074.7

Pad Description

Pad No	Pad Name	I/O	Description
1	VDD	—	Positive power supply
2	SPWR	O	Sensor power supply
3	PDET	I	Low battery detect input
4	OP1P	I	Sensor input " — " end, the 1st OPA positive input end
5	OP1O	I/O	The 1st stage of OPA voltage follow end
6	OP2P	I	Sensor input " + " end, the 2nd OPA positive input end
7	OP2N	I	The 2nd stage of OPA negative input end
8	OP2O	I	The 2nd stage of OPA output end.
9	REF1	I	The 3rd stage of OPA positive input end
12	REF2	I	The compare stage of OPA positive input end
13	VSS	—	Negative power supply
14	ADRR	I	Charge and discharge input source, the R terminal of RC network
15	ADRC	I	The 3rd stage of OPA negative input end, the R-C terminal of RC network
16	ADCC	O	The 3rd stage of OPA output end, the C terminal of RC network
17	COMPO	O	The compare stage of OPA output end
18	ON/OFF	I	The internal OPA power supply control; Hi=ON, Low=OFF
19	CHR/DISC	I	The ADC charge and discharge control; Hi=Charge, Low=Discharge
20	LV	O	Low battery detect output; if battery low, then output low level.

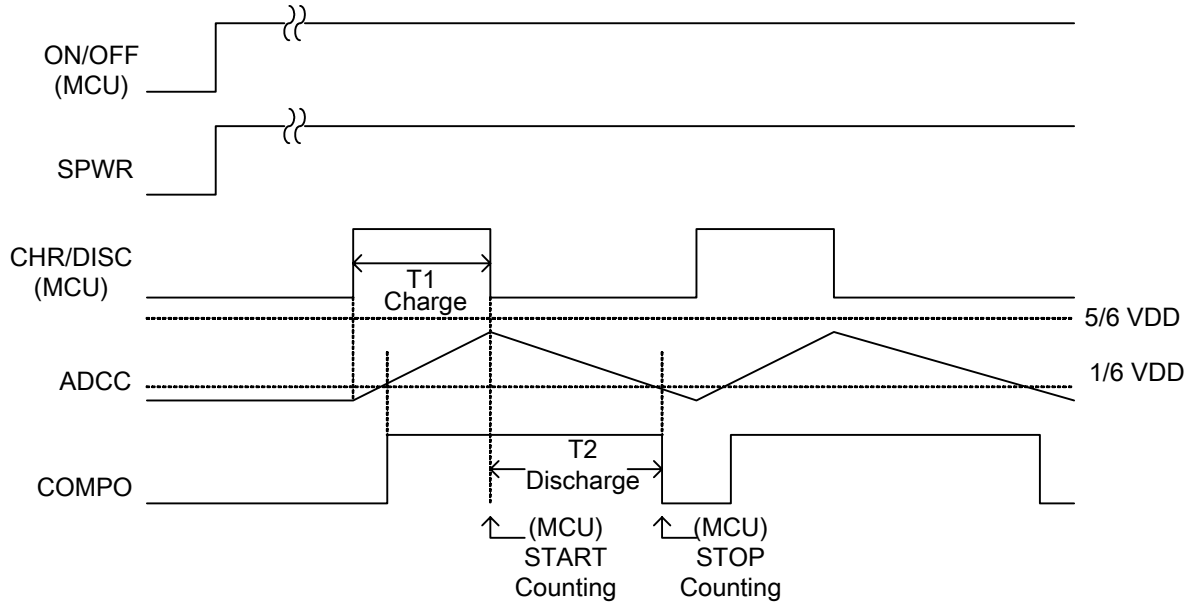
Electrical Characteristics

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		VDD	Condition				
VDD	Operation Voltage			2.4	3.0	5.2	V
IDD	Operation Current	3V	With Loading	-	300	500	uA
ISTB	Standby Current	3V	On/Off pin:off	-	0.01	1	uA

Functional Descriptions

1. Low Battery Detector
   When the input voltage below the setting voltage (by adjusting the external resistor), the LV level goes low (Refer to Application Diagram).
2. OP1
   OP1 was a voltage follower. It receives sensor signal and amplify the signal with unit gain. The output was sent to pin 2 for OP2 further use.
3. OP2
   OP2 was designed for signal amplification. By adjusting the external resistors, user can properly decide the gain of the amplifier.
4. Transmission gates & Integrator
   Transmission gate provides a signal accurately proportional to the OP2 amplified signal level. This signal will be used to charge an external RC network at a fixed time interval (See the Timing Diagram T1). Another transmission gate can generate a constant signal to discharge the capacitor. This discharging time is proportional to the input signal level.
5. Comparators
   The comparators were used to generate a data (T2) for controller. When the input signal is charged on integrator after a time interval T1, the controller shall control the CHR/DISC pin to discharge (See the Timing Diagram), and then controller shall enable the internal counter to start counting. When the voltage on ADCC is lower than 1/6 VDD (after discharge a time interval T2), the COMPO pin will transfer from High to Low. At this time the controller shall stop the internal counter. The discharge time T2 is proportional to the input level, the final count of counter can be converted to digital data by controller.
6. Power on/off control
   The power on/off control circuit was designed for power saving. The SPWR (Sensor Power Supply) won't be available unless the On/Off actives (High).

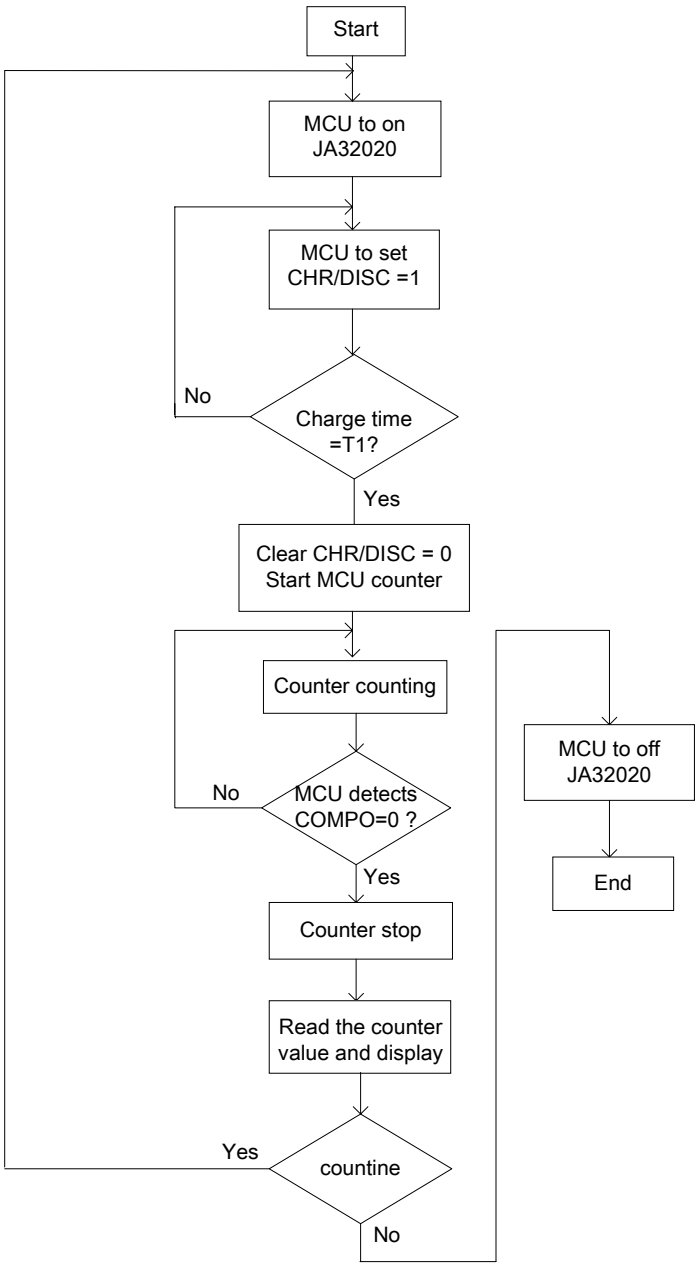
Timing Diagram



T1(Charge): The fixed charge time control by controller(MCU).
T2 (Discharge): The discharge time provide to controller(MCU).

Programming Flow Chart

The following flow chart is the illustration for JA32020 programming.



a. MCU asserts high signal on JA32020 ON/OFF pin to activate JA32020.
b. JA32020 provides power to sensor from SPWR pin.
c. MCU asserts high signal on JA32020 CHR/DISC pin to informJA32020 start charging.
d. After a fixed time interval (decided by MCU program), MCU asserts low signal on JA32020 CHR/DISC pin to informJA32020 start discharging.
e. MCU enable internal counter start counting.
f. When ADCC of JA32020 below 1/6 VDD (The COMPO pin transfer from High to Low), MCU disable counter.
g. MCU converts counter count value to digital output. The count value is proportional to the input signal.

Application Diagram