NT6512

16K 4-Bit Microcontroller with 16x33 LCD Driver

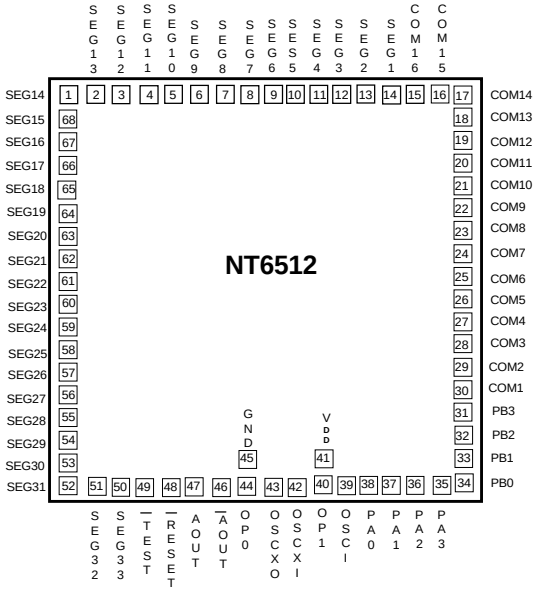
Features

- NT6610C-based single-chip 4-bit microcontroller with LCD driver
- ROM: 16 K × 16 bits (bank switched)
- RAM: 512 × 4 bits (system control register & data memory)
- Operating Voltage Range: 2.4V - 5.5V
- 8 CMOS I/O ports
- 4 level subroutine nesting including interrupts
- One 8-bit timer with pre-divider circuit
- Warm-up timer for power-on reset
- Powerful interrupt sources:
  - Timer0 interrupt
  - Base timer interrupt
  - Port B interrupt (falling edge)
- Base timer clock: 32.768KHz X'tal oscillator.
- System clock 2M~500KHz single-pin voltage-controlled oscillator
- Table Branch and Return Constant Instructions for Table Data Generation
- Data pointer with special system register control
- Two low power operating modes - HALT and STOP
- Instruction cycle time: 2 μs for 2 MHz voltage-controlled oscillator
- Built-in 2-channel PSG for sound effects, switchable to noise channel
- Directly drives speaker
- Type B LCD drive circuit
- LCD driver: 33 × 16 (1/16 duty cycle, 1/5 bias)
- LCD off by programming LCDOFF register
- Available in CHIP FORM

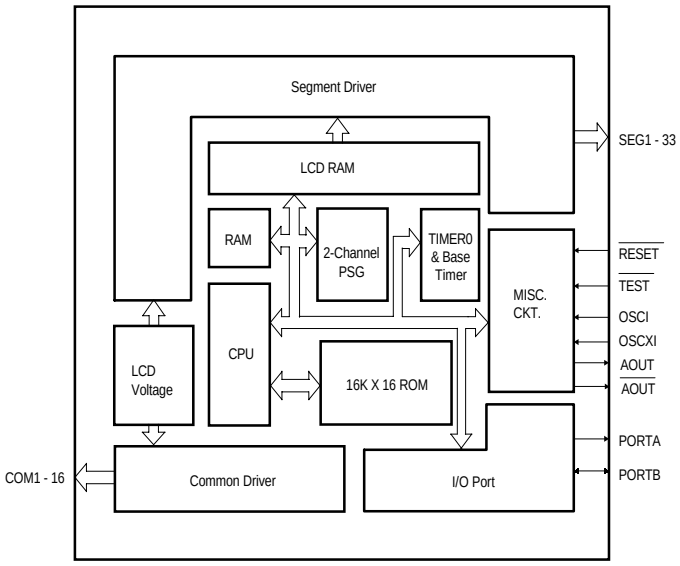
General Description

NT6512 is a single chip 4 bit μC dedicated chip for handheld games. This device integrates a NT6610C 4-bit CPU core with RAM, ROM, timer, 2-channel PSG, and dot matrix LCD driver.

Pad Configuration



Block Diagram



Pad Description

Pad No.	Symbol	I/O	Shared by	Reset	Description
14 - 1, 68 - 50	SEG1 - 33	O			Segment signal output for LCD display
15 - 30	COM16 - 1	O			Common signal output for LCD display
31 - 34	PB3 - PB0	I/O	PORT INT.	0FH	Bit programmable I/O, Vector Interrupt
35 - 38	PA3 - PA0	O		0	Output ports
40, 44	OP1, OP0	I			Bonding option
41	V_{DD}				Power supply
39	OSCI	I			OSC input
45	GND				Ground
46, 47	$\overline{AOUT}$ AOUT	O			Audio output
48	$\overline{RESET}$	I			Reset input (active low)
49	$\overline{TEST}$	I			TEST (No connect for user)
42	OSCXI	I/O			32.768Khz X'tal OSC input
43	OSCXO	I/O			32.768Khz X'tal OSC output

Functional Description

1. CPU

The CPU core contains the following function blocks: Program Counter, ALU, Carry Flag, Accumulator, Table Branch Register (TBR), Data Pointer (INX, DPH, DPM and DPL), and Stack.

(a) PC (Program Counter)

The PC is used for ROM addressing consisting of 12-bits: Page Register (PC11),
and Ripple Carry Counter (PC10 - PC0).

The program counter normally increases by one (+1) with each execution of an instruction except in the following cases:

1) When executing a jump instruction (such as JMP, BA0, BAC);

2) When executing a subroutine call instruction (CALL);

3) When an interrupt occurs;

4) When the chip is at INITIAL RESET. The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

Program Counter can only address a 4K program ROM. To address 16K program ROM, use bank switch (Refer to the ROM description in Section 3 for details).

(b) ALU and CY

ALU performs arithmetic and logic operations.

The ALU provides the following functions:

Binary addition/subtraction
(ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjustment for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDI, EORI, ORI)
Decision (BA0, BA1, BA2, BA3, BAZ, BAC)
The Carry Flag (CY) holds the arithmetic operation ALU overflow.

During interrupt or call instruction, carry is pushed onto stack and restored from stack by RTNI. It is unaffected by an RTNW instruction.

(c) Accumulator

Accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with ALU, data transfers between the accumulator and system register, LCD RAM, or data memory can be performed.

(d) Stack

A group of registers used to save the contents of CY & PC (10-0) sequentially with each subroutine call or interrupt. It is organized 13 bits × 4 levels. The MSB is saved for CY. 4 levels are the maximum allowed for subroutine calls and interrupts.

The contents of Stack are returned sequentially to the PC with the return instructions (RTNI/RTNW). Stack is operated on a first-in, last-out basis. This 4-level nesting includes both subroutine calls and interrupt requests. Note that program execution may enter an abnormal state if the number of calls and interrupt requests exceeds 4, and the bottom of stack will be shifted out.

2. RAM

RAM consists of general purpose data memory, LCD RAM, and system registers.

(a) RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. Following is the memory allocation map:

$000 - $01F : System register and I/O (32 × 4 bits)
$020 - $1FF : Data Memory (480 × 4 bits)
$200 - $2FF : Reserved
$300 - $383 : LCD RAM space (132 × 4 bits)

(b) Data Memory

Data memory is organized as 480 × 4 bits ($020 - $1FF). Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT.

(c) System Registers

The configuration of system registers is as follows:

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEBT	IET0	-	IEP	R/W	Interrupt enable flags
$01	IRQBT	IRQT0	-	IRQP	R/W	Interrupt request flags
$02	-	TM0.2	TM0.1	TM0.0	R/W	Timer0 mode register (TM0)
$03	HVL	BTM.2	BTM.1	BTM.0	W	HVL: Switch Base Timer into heavy load mode Base timer mode register (BTM)
$04	TL.3	TL.2	TL.1	TL.0	R/W	Timer0 load/counter register low digit
$05	TH.3	TH.2	TH.1	TH.0	R/W	Timer0 load/counter register high digit
$06	BTL.3	BTL.2	BTL.1	BTL.0	R/W	Base timer load/counter register low digit
$07	BTH.3	BTH.2	BTH.1	BTH.0	R/W	Base timer load/counter register high digit
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A~0B	-	-	-	-	-	Reserved
$0C	-	-	OP1	OP0	R	Bonding Option
$0D	-	-	-	-	-	Reserved
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register (TBR)
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo Index Register (INX)
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data Pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data Pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data Pointer for INX high nibble
$13	C1.3	C1.2	C1.1	C1.0	W	PSG Channel 1 low digit
$14	C1M	C1.6	C1.5	C1.4	W	PSG Channel 1 high digit
$15	C2.3	C2.2	C2.1	C2.0	W	PSG Channel 2 low digit
$16	C2.7	C2.6	C2.5	C2.4	W	PSG Channel 2
$17	C2.11	C2.10.	C2.9	C2.8	W	PSG Channel 2
$18	C2M	C2.14	C2.13	C2.12	W	PSG Channel 2 high digit
$19	VOL1	VOL0	CH2 EN	CH1 EN	W	Bit 0: PSG Channel 1 enable Bit 1: PSG Channel 2 enable Bit 2, Bit 3: Volume Control (Initially 0, no sound)
$1A	-	-	P1.1	P1.0	W	PSG 1 Prescaler
$1B	-	-	P2.1	P2.0	W	PSG 2 Prescaler
$1C	-	TM.2	TM.1	LCDOFF	W	Bit 0: LCD Power Control Bit 2, Bit 1: Reserved for TEST Mode (TMR)
$1D	-	-	-	-	-	Reserved for ICE
$1E	-	-	-	-	-	Reserved
$1F	-	BNK2	BNK1	BNK0	W	Bank Register for ROM (BNK), bit 3 reserved for ICE

(d) Data Pointer

Data memory can be indirectly addressed by the Data Pointer. Pointer address is located in register DPM (3-bits) and DPL (4-bits). The addressing range can have 128 locations. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9-bit0 comes from DPH, DPM and DPL.

3. ROM

NT6512 can address up to 16K × 16 bits of program area from $000 to $3FFF.
ROM SPACE in the system is 16384 × 16 bits.

(a) Vector Address Area ($000 to $004)

The program is sequentially executed. An area from address $000 through $004 is reserved for special interrupt service routines as starting execution of a vector address.

Address	Instruction	Remarks
$000	JMP	Jump to RESET
$001	JMP	Jump to Base Timer
$002	JMP	Jump to TIMER0
$003	-	Reserved
$004	JMP	Jump to PB (port B)

* JMP can be replaced by any other instruction.

(b) Table Data Reference

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The Table Branch Register (TBR) and Accumulator (A) is placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) ×(2^8) + (TBR, A)). The address is determined by RTNW to return look-up value into (TBR, A). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into A.

(c) Bank Switch Mapping

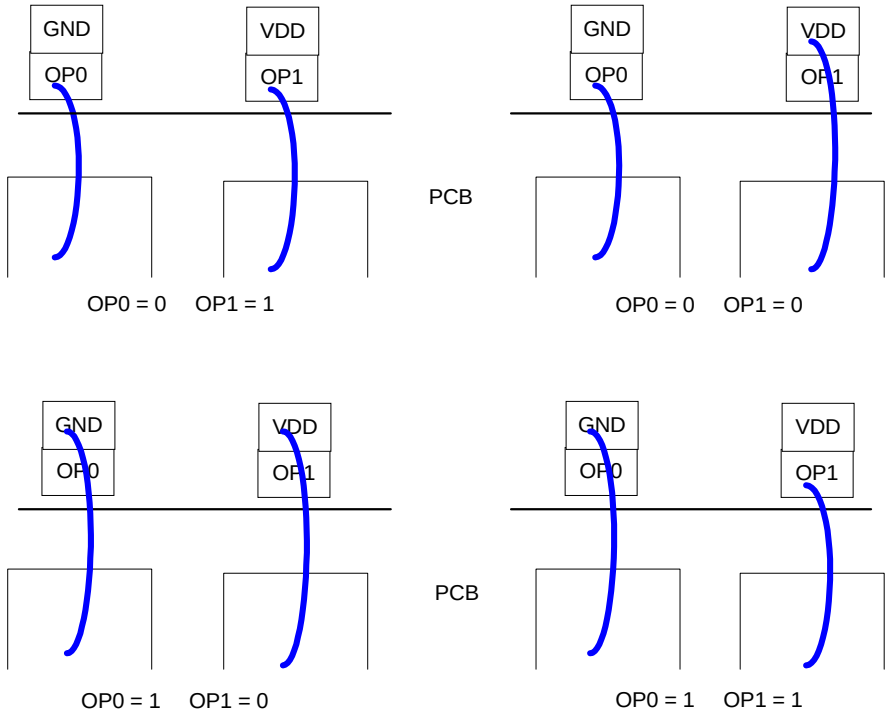
Program Counter (PC11 - PC0) can only address 4K ROM space. Bank switch technique is used to extend the CPU address space. The lower 2K of the CPU addressing space maps to lower 2K of ROM space (BANK0). The upper 2K of the CPU addressing space maps to one of the seven banks (BANK 1, 2, 3, 4, 5, 6, 7) of the upper 14K of ROM. (according to the Bank Register)

The bank switch mapping is as follows:

CPU Address	ROM Space, BNK = 0	ROM Space, BNK = 1	ROM Space, BNK = 2	ROM Space, BNK = 3	ROM Space, BNK = 4	ROM Space, BNK = 5	ROM Space, BNK = 6
000-7FF	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)
800 - FFF	0800-0FFF (BANK 1)	1000 -17FF (BANK 2)	1800 -1FFF (BANK 3)	2000 -27FF (BANK 4)	2800 -2FFF (BANK 5)	3000 -37FF (BANK 6)	3800 -3FFF (BANK 7)

System Register 0CH

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power-on
$0C	-	-	OP1	OP0	R	Bit0: Bonding option 0, internal weak drive Bit1: Bonding option 1, internal weak drive	Pull high Pull low
	X	X	0	1			Yes
	X	X	0	0		OP0 bond to GND	
	X	X	1	1		OP1 bond to V_{DD}	
	X	X	1	0		OP0 bond to GND and OP1 bond to V_{DD}	



NT6512 Bonding Option

Up to 4 different bonding options are possible for the user's needs. The chip's program has 4 different program flows that will vary depending on which bonding option is used. The readable contents of OP1 and OP0 will differ depending on bonding.

4. Timer

NT6512 has one 8-bit timer for count-up, consisting of an 8-bit counter and an 8-bit pre-loaded register. Beside, the other base timer provides real time clock function for time-keeper.

Timer0 provides the following functions:

* Programmable interval timer
* Read counter value

(a) Timer0 Configuration and Operation:

Timer-0 is an 8-bit write-only timer load register (TL0L, TL0H), and an 8-bit read-only timer counter (TC0L, TC0H). Each low order digits and high order digits. Timer counter is initialized by writing data into the timer load register (TL0L, TL0H).

First write the low-order digit, then the high-order digit. Timer counter is automatically loaded with the contents of the loaded register when the high order digit is written or count overflows occurs. Timer overflow will result in a interrupt if the interrupt enable flag is set.

Timer can be programmed in several different clock sources by setting Timer Mode Register (TM0).

(b) Timer0 Mode Register:

Timer Mode Registers (TM0) are 4-bit registers used for timer control as shown in Table 1. Mode Register selects input pulse sources to the timer.

Table 1. Timer0 Mode Registers ($02)

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

(c) Base timer Configuration and Operation:

Base timer generates the different frequency interrupt for real time clock based on the value of BTM, shown as Table 2. The heavy load register, HVL, is used to switch 32.769K Hz X'tal oscillator into heavy load mode that makes the oscillation easier in the startup period but more current is needed.

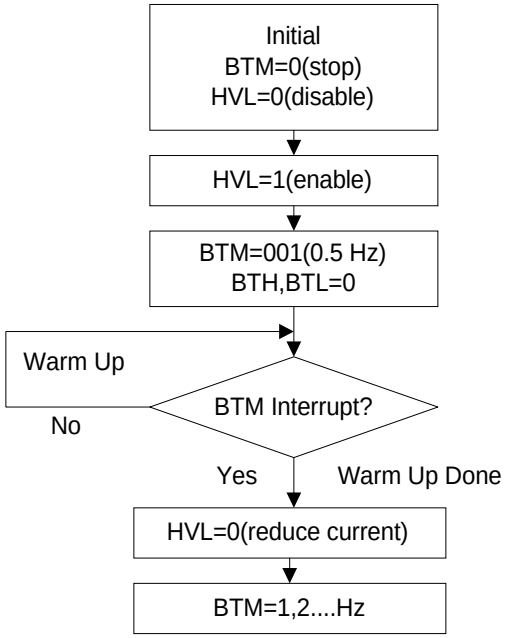
Table 2. Base Timer Mode Registers ($03)

BTM.2	BTM.1	BTM.0	Interrupt Period	Clock Source
0	0	0	Stop(default)	32K Hz
0	0	1	0.5 Hz	32K Hz
0	1	0	1 Hz	32K Hz
0	1	1	2 Hz	32K Hz
1	0	0	4 Hz	32K Hz
1	0	1	8 Hz	32K Hz
1	1	0	16 Hz	32K Hz
1	1	1	Inhibit	

To achieve the above interrupt periods, system register $06 and $07, BTL and BTH, must be set to 00H for both.

Note: Please enable 32.768K oscillator before turning LCD on , since LCD clock comes from basetimer.

The example of using Base Timer:

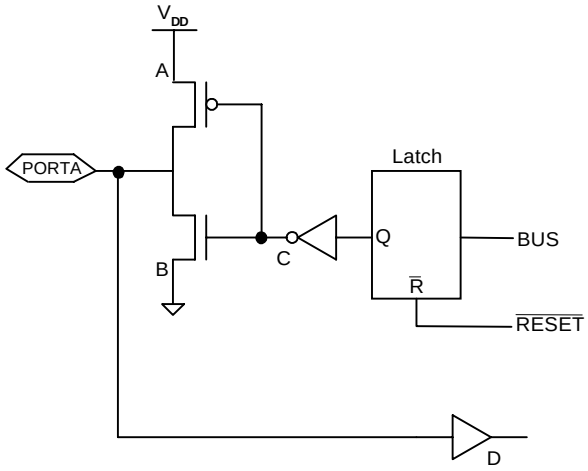


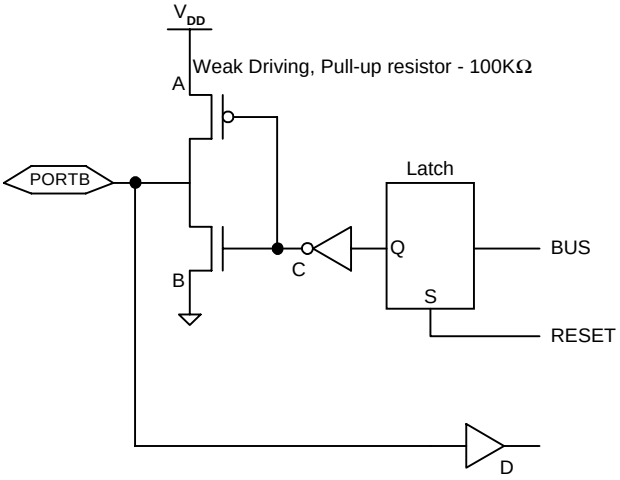
5. I/O Ports

(a) Functional Description

- CMOS type output port
- PMOS as pull-up for Input on PortB
- Output low initially for PortA
- Output high initially for PortB
- Operates same as data memory for arithmetic and logic instructions

(b) Circuit Diagrams (PORT A and PORT B)





(c) Programming

- I/O ports can be accessed with the read/write system register.
- Memory-mapped addresses are listed as follows:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	-	-	-	-	-	Reserved
$0B	-	-	-	-	-	Reserved
$0C	-	-	OP1	OP0	R	Optional Register

- Users can output any value to any I/O port bit at any time.
- Before reading PORTB I/O bits, the user needs to output "1" to the same bit.

6. Programmable Sound Generator (PSG)

2-Channel PSG is provided. Channel 1 is a 7-bit pseudo random counter. Channel 2 is a 15-bit pseudo random counter. Mode bits CH1M, CH2M determine which of each pseudo random counter will be a noise or a tone generator. To reduce power consumption, disable the sound effect generator during both STOP and HALT.

Note: Don't enable two PSG channels together to produce one tone, or it will produce some unpredicted errors. If it is necessary to use 2 channels together (EX. To play two channel melody), don't let the score always be the same tones as we can do, then the unpredicted errors will not occur or it will be ignore through user hearing

Channel 2 TONE mode is same as Channel 1. (7-bit pseudo-random counter). This eliminates some programming codes.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	C1.3	C1.2	C1.1	C1.0	W	PSG Channel 1 low digit
$14	C1M	C1.6	C1.5	C1.4	W	PSG Channel 1 high digit
$15	C2.3	C2.2	C2.1	C2.0	W	PSG Channel 2 low digit
$16	C2.7	C2.6	C2.5	C2.4	W	PSG Channel 2
$17	C2.11	C2.10.	C2.9	C2.8	W	PSG Channel 2
$18	C2M	C2.14	C2.13	C2.12	W	PSG Channel 2 high digit
$19	VOL1	VOL0	CH2EN	CH1EN	W	Bit 0: PSG Channel 1 enable Bit 1: PSG Channel 2 enable Bit 2, Bit 3: Volume Control (Initially 0, no sound)
$1A	-	-	P1.1	P1.0	W	PSG 1 Prescaler
$1B	-	-	P2.1	P2.0	W	PSG 2 Prescaler

P.1	P.0	Prescaler Divide Ratio	Clock Source	Actual Clock
0	0	1	32 KHz	32 KHz
0	1	2	32 KHz	16 KHz
1	0	4	32 KHz	8 KHz
1	1	8	32 KHz	4 KHz

Music Table1:

Following is the music scale reference table for channel 1 (or channel 2) under Actual Clock=32KHz.

Note	Ideal freq.	N	LSFR (C1.6~C1.0) (C2.14~C2.8)	Real freq.	Error %	Note	Ideal freq.	N	LSFR (C1.6~C1.0) (C2.14~C2.8)	Real freq.	Error %
C3	130.81	122	20	131.15	0.26%	**G4**	392.0	41	58	390.24	-0.44%
D3	146.83	109	51	146.79	-0.03%	**A4**	440.0	36	1A	444.44	1.01%
E3	164.81	97	45	164.95	0.08%	**B4**	493.9	32	25	500.00	1.24%
F3	174.61	92	33	173.91	-0.40%	**C5**	523.2	31	4B	516.13	-1.36%
G3	195.99	82	27	195.12	-0.44%	**D5**	587.3	27	3B	592.59	0.90%
A3	220.00	73	21	219.18	-0.37%	**E5**	659.2	24	5C	666.67	1.13%
B3	246.94	65	44	246.15	-0.32%	**F5**	698.4	23	39	695.65	-0.40%
C4	261.62	61	49	262.30	0.26%	**G5**	784.0	20	4C	800.00	2.04%
D4	293.66	54	5A	296.30	0.90%	**A5**	880.0	18	32	888.89	1.01%
E4	329.62	49	5B	326.53	-0.94%	**B5**	987.7	16	4A	1000.00	1.24%
F4	349.22	46	5E	347.83	-0.40%	**C6**	1046.5	15	15	1066.67	1.93%

Music Table2:

Following is the music scale reference table for channel 1 (or channel 2) under Actual Clock=16KHz.

Note	Ideal freq.	N	LSFR (C1.6~C1.0) (C2.14~C2.8)	Real freq.	Error %	Note	Ideal freq.	N	LSFR (C1.6~C1.0) (C2.14~C2.8)	Real freq.	Error %
C2	65.41	122	20	65.57	0.26%	**G3**	195.99	41	58	195.12	-0.44%
D2	73.41	109	51	73.39	-0.03%	**A3**	220.00	36	1A	222.22	1.01%
E2	82.41	97	45	82.47	0.08%	**B3**	246.94	32	25	250.00	1.24%
F2	87.31	92	33	86.96	-0.40%	**C4**	261.62	31	4B	258.06	-1.36%
G2	98.00	82	27	97.56	-0.44%	**D4**	293.66	27	3B	296.30	0.90%
A2	110.00	73	21	109.59	-0.37%	**E4**	329.62	24	5C	333.33	1.13%
B2	123.47	65	44	123.08	-0.32%	**F4**	349.22	23	39	347.83	-0.40%
C3	130.81	61	49	131.15	0.26%	**G4**	391.99	20	4C	400.00	2.04%
D3	146.83	54	5A	148.15	0.90%	**A4**	439.99	18	32	444.44	1.01%
E3	164.81	49	5B	163.27	-0.94%	**B4**	493.87	16	4A	500.00	1.24%
F3	174.61	46	5E	173.91	-0.40%	**C5**	523.24	15	15	533.33	1.93%

Music Table3:

Following is the music scale reference table for channel 1 (or channel 2) under Actual Clock=8KHz.

Note	Ideal freq.	N	LSFR (C1.6~C1.0) (C2.14~C2.8)	Real freq.	Error %	Note	Ideal freq.	N	LSFR (C1.6~C1.0) (C2.14~C2.8)	Real freq.	Error %
C1	32.70	122	20	32.79	0.26%	**G2**	98.00	41	58	97.56	-0.44%
D1	36.71	109	51	36.70	-0.03%	**A2**	110.00	36	1A	111.11	1.01%
E1	41.20	97	45	41.24	0.08%	**B2**	123.47	32	25	125.00	1.24%
F1	43.65	92	33	43.48	-0.40%	**C3**	130.81	31	4B	129.03	-1.36%
G1	49.00	82	27	48.78	-0.44%	**D3**	146.83	27	3B	148.15	0.90%
A1	55.00	73	21	54.79	-0.37%	**E3**	164.81	24	5C	166.67	1.13%
B1	61.73	65	44	61.54	-0.32%	**F3**	174.61	23	39	173.91	-0.40%
C2	65.41	61	49	65.57	0.26%	**G3**	195.99	20	4C	200.00	2.04%
D2	73.41	54	5A	74.07	0.90%	**A3**	220.00	18	32	222.22	1.01%
E2	82.41	49	5B	81.63	-0.94%	**B3**	246.94	16	4A	250.00	1.24%
F2	87.31	46	5E	86.96	-0.40%	**C4**	261.62	15	15	266.67	1.93%

Music Table4:

Following is the music scale reference table for channel 1 (or channel 2) under Actual Clock=4KHz.

Note	Ideal freq.	N	LSFR (C1.6~C1.0) (C2.14~C2.8)	Real freq.	Error %	Note	Ideal freq.	N	LSFR (C1.6~C1.0) (C2.14~C2.8)	Real freq.	Error %
C0	16.35	122	20	16.39	0.26%	**G1**	49.00	41	58	48.78	-0.44%
D0	18.35	109	51	18.35	-0.03%	**A1**	55.00	36	1A	55.56	1.01%
E0	20.60	97	45	20.62	0.08%	**B1**	61.73	32	25	62.50	1.24%
F0	21.83	92	33	21.74	-0.40%	**C2**	65.41	31	4B	64.52	-1.36%
G0	24.50	82	27	24.39	-0.44%	**D2**	73.41	27	3B	74.07	0.90%
A0	27.50	73	21	27.40	-0.37%	**E2**	82.41	24	5C	83.33	1.13%
B0	30.87	65	44	30.77	-0.32%	**F2**	87.31	23	39	86.96	-0.40%
C1	32.70	61	49	32.79	0.26%	**G2**	98.00	20	4C	100.00	2.04%
D1	36.71	54	5A	37.04	0.90%	**A2**	110.00	18	32	111.11	1.01%
E1	41.20	49	5B	40.82	-0.94%	**B2**	123.47	16	4A	125.00	1.24%
F1	43.65	46	5E	43.48	-0.40%	**C3**	130.81	15	15	133.33	1.93%

7. LCD

The LCD has 16 common signal pads, a controller, an LCD voltage generator, and 33 segment driver pads. The controller consists of display data RAM and a duty generator. LCD is 1/16 duty, and 1/5 bias. The LCD data RAM is a dual port RAM that automatically transfers data to segment. The LCD can be turned off with the internal LCDOFF register.

LCD frame frequency is controlled by 32.768KHz clock. Therefore, 32.768KHz clock must be enabled before LCD is turned on. To save power, the main clock can be stopped and keep the 32.768KHz running that can keep LCD on.

Note: Please enable 32.768K oscillator before turning LCD on.

(a) LCD RAM Area Configuration:

Address	Bit3	Bit2	Bit1	Bit0
$300	SEG1	SEG1	SEG1	SEG1
$301	SEG2	SEG2	SEG2	SEG2
$302	SEG3	SEG3	SEG3	SEG3
$303	SEG4	SEG4	SEG4	SEG4
$304	SEG5	SEG5	SEG5	SEG5
$305	SEG6	SEG6	SEG6	SEG6
$306	SEG7	SEG7	SEG7	SEG7
$307	SEG8	SEG8	SEG8	SEG8
$308	SEG9	SEG9	SEG9	SEG9
$309	SEG10	SEG10	SEG10	SEG10
$30A	SEG11	SEG11	SEG11	SEG11
$30B	SEG12	SEG12	SEG12	SEG12
$30C	SEG13	SEG13	SEG13	SEG13
$30D	SEG14	SEG14	SEG14	SEG14
$30E	SEG15	SEG15	SEG15	SEG15
$30F	SEG16	SEG16	SEG16	SEG16
$310	SEG17	SEG17	SEG17	SEG17
$311	SEG18	SEG18	SEG18	SEG18
$312	SEG19	SEG19	SEG19	SEG19
$313	SEG20	SEG20	SEG20	SEG20
$314	SEG21	SEG21	SEG21	SEG21
$315	SEG22	SEG22	SEG22	SEG22
$316	SEG23	SEG23	SEG23	SEG23
$317	SEG24	SEG24	SEG24	SEG24
$318	SEG25	SEG25	SEG25	SEG25
$319	SEG26	SEG26	SEG26	SEG26
$31A	SEG27	SEG27	SEG27	SEG27
$31B	SEG28	SEG28	SEG28	SEG28
$31C	SEG29	SEG29	SEG29	SEG29
$31D	SEG30	SEG30	SEG30	SEG30
$31E	SEG31	SEG31	SEG31	SEG31
$31F	SEG32	SEG32	SEG32	SEG32
Duty	**COM4**	**COM3**	**COM2**	**COM1**

LCD RAM Area Configuration (continued):

Address	Bit 3	Bit 2	Bit 1	Bit 0
$320	SEG1	SEG1	SEG1	SEG1
$321	SEG2	SEG2	SEG2	SEG2
$322	SEG3	SEG3	SEG3	SEG3
$323	SEG4	SEG4	SEG4	SEG4
$324	SEG5	SEG5	SEG5	SEG5
$325	SEG6	SEG6	SEG6	SEG6
$326	SEG7	SEG7	SEG7	SEG7
$327	SEG8	SEG8	SEG8	SEG8
$328	SEG9	SEG9	SEG9	SEG9
$329	SEG10	SEG10	SEG10	SEG10
$32A	SEG11	SEG11	SEG11	SEG11
$32B	SEG12	SEG12	SEG12	SEG12
$32C	SEG13	SEG13	SEG13	SEG13
$32D	SEG14	SEG14	SEG14	SEG14
$32E	SEG15	SEG15	SEG15	SEG15
$32F	SEG16	SEG16	SEG16	SEG16
$330	SEG17	SEG17	SEG17	SEG17
$331	SEG18	SEG18	SEG18	SEG18
$332	SEG19	SEG19	SEG19	SEG19
$333	SEG20	SEG20	SEG20	SEG20
$334	SEG21	SEG21	SEG21	SEG21
$335	SEG22	SEG22	SEG22	SEG22
$336	SEG23	SEG23	SEG23	SEG23
$337	SEG24	SEG24	SEG24	SEG24
$338	SEG25	SEG25	SEG25	SEG25
$339	SEG26	SEG26	SEG26	SEG26
$33A	SEG27	SEG27	SEG27	SEG27
$33B	SEG28	SEG28	SEG28	SEG28
$33C	SEG29	SEG29	SEG29	SEG29
$33D	SEG30	SEG30	SEG30	SEG30
$33E	SEG31	SEG31	SEG31	SEG31
$33F	SEG32	SEG32	SEG32	SEG32
Duty	**COM8**	**COM7**	**COM6**	**COM5**

LCD RAM Area Configuration (continued):

Address	Bit3	Bit2	Bit1	Bit0
$340	SEG1	SEG1	SEG1	SEG1
$341	SEG2	SEG2	SEG2	SEG2
$342	SEG3	SEG3	SEG3	SEG3
$343	SEG4	SEG4	SEG4	SEG4
$344	SEG5	SEG5	SEG5	SEG5
$345	SEG6	SEG6	SEG6	SEG6
$346	SEG7	SEG7	SEG7	SEG7
$347	SEG8	SEG8	SEG8	SEG8
$348	SEG9	SEG9	SEG9	SEG9
$349	SEG10	SEG10	SEG10	SEG10
$34A	SEG11	SEG11	SEG11	SEG11
$34B	SEG12	SEG12	SEG12	SEG12
$34C	SEG13	SEG13	SEG13	SEG13
$34D	SEG14	SEG14	SEG14	SEG14
$34E	SEG15	SEG15	SEG15	SEG15
$34F	SEG16	SEG16	SEG16	SEG16
$350	SEG17	SEG17	SEG17	SEG17
$351	SEG18	SEG18	SEG18	SEG18
$352	SEG19	SEG19	SEG19	SEG19
$353	SEG20	SEG20	SEG20	SEG20
$354	SEG21	SEG21	SEG21	SEG21
$355	SEG22	SEG22	SEG22	SEG22
$356	SEG23	SEG23	SEG23	SEG23
$357	SEG24	SEG24	SEG24	SEG24
$358	SEG25	SEG25	SEG25	SEG25
$359	SEG26	SEG26	SEG26	SEG26
$35A	SEG27	SEG27	SEG27	SEG27
$35B	SEG28	SEG28	SEG28	SEG28
$35C	SEG29	SEG29	SEG29	SEG29
$35D	SEG30	SEG30	SEG30	SEG30
$35E	SEG31	SEG31	SEG31	SEG31
$35F	SEG32	SEG32	SEG32	SEG32
Duty	**COM12**	**COM11**	**COM10**	**COM9**

LCD RAM Area Configuration (continued):

Address	Bit3	Bit2	Bit1	Bit0
$360	SEG1	SEG1	SEG1	SEG1
$361	SEG2	SEG2	SEG2	SEG2
$362	SEG3	SEG3	SEG3	SEG3
$363	SEG4	SEG4	SEG4	SEG4
$364	SEG5	SEG5	SEG5	SEG5
$365	SEG6	SEG6	SEG6	SEG6
$366	SEG7	SEG7	SEG7	SEG7
$367	SEG8	SEG8	SEG8	SEG8
$368	SEG9	SEG9	SEG9	SEG9
$369	SEG10	SEG10	SEG10	SEG10
$36A	SEG11	SEG11	SEG11	SEG11
$36B	SEG12	SEG12	SEG12	SEG12
$36C	SEG13	SEG13	SEG13	SEG13
$36D	SEG14	SEG14	SEG14	SEG14
$36E	SEG15	SEG15	SEG15	SEG15
$36F	SEG16	SEG16	SEG16	SEG16
$370	SEG17	SEG17	SEG17	SEG17
$371	SEG18	SEG18	SEG18	SEG18
$372	SEG19	SEG19	SEG19	SEG19
$373	SEG20	SEG20	SEG20	SEG20
$374	SEG21	SEG21	SEG21	SEG21
$375	SEG22	SEG22	SEG22	SEG22
$376	SEG23	SEG23	SEG23	SEG23
$377	SEG24	SEG24	SEG24	SEG24
$378	SEG25	SEG25	SEG25	SEG25
$379	SEG26	SEG26	SEG26	SEG26
$37A	SEG27	SEG27	SEG27	SEG27
$37B	SEG28	SEG28	SEG28	SEG28
$37C	SEG29	SEG29	SEG29	SEG29
$37D	SEG30	SEG30	SEG30	SEG30
$37E	SEG31	SEG31	SEG31	SEG31
$37F	SEG32	SEG32	SEG32	SEG32
Duty	**COM16**	**COM15**	**COM14**	**COM13**

Address	Bit3	Bit2	Bit1	Bit0
$380	SEG33	SEG33	SEG33	SEG33
Duty	**COM4**	**COM3**	**COM2**	**COM1**

Address	Bit3	Bit2	Bit1	Bit0
$381	SEG33	SEG33	SEG33	SEG33
Duty	**COM8**	**COM7**	**COM6**	**COM5**

LCD RAM Area Configuration (continued):

Address	Bit3	Bit2	Bit1	Bit0
$382	SEG33	SEG33	SEG33	SEG33
Duty	**COM12**	**COM11**	**COM10**	**COM9**

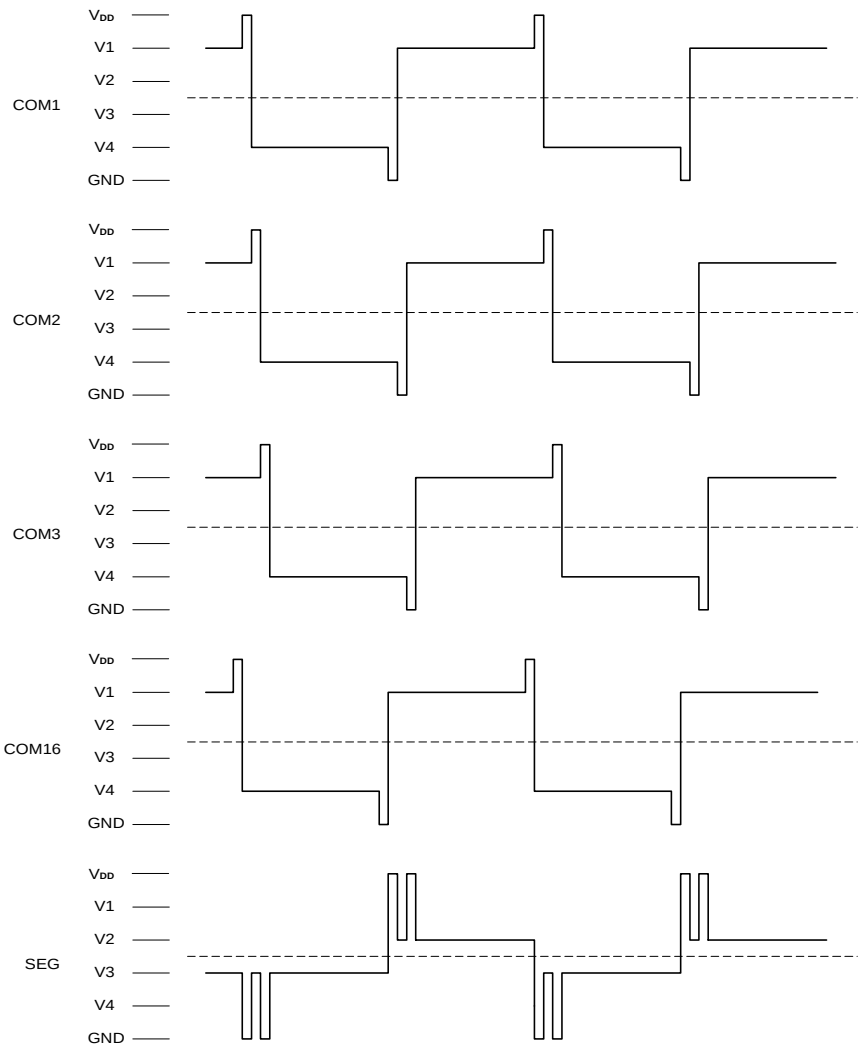
Address	Bit3	Bit2	Bit1	Bit0
$383	SEG33	SEG33	SEG33	SEG33
Duty	**COM16**	**COM15**	**COM14**	**COM13**

(b) LCD Voltage Generator

LCD voltages V1, V2, V3, V4 are obtained using resistor divider network. The LCD can be turned off by with the LCDOFF register.

(c) LCD Waveform

The output waveform of 1/16 duty and 1/5 bias is shown below.



8. Interrupt

Three interrupt sources are available on the NT6512:

- Base Timer interrupt (BTMR)
- Timer0 interrupt (TMR0)
- Port falling edge detection interrupt ($\overline{PB}$)

(a) Interrupt Control Bits and Interrupt Service:

- Interrupt control flags are mapped on $00 through $01 of the system register. They can be accessed or tested by the program. These flags are cleared to 0 at initialization.

	Bit 3	Bit 2	Bit 1	Bit 0	Remarks
$00	IEBT	IET0	-	IEP	Interrupt enable flags
$01	IRQBT	IRQT0	-	IRQP	Interrupt request flags

- Interrupt request begins when IRQx is set to 1 and IEx is 1. At this time, interrupt will activate and vector address will commence from the priority PLA corresponding to the interrupt source. When an interrupt occurs, the PC and CY flags will be saved in stack memory and jump to an interrupt service vector address. After interrupt occurs, all interrupt enable flags (IEx) are automatically reset to 0, so any interrupt is disabled. The IRQx, which caused interrupt, must be reset by software in the interrupt service routine. When IEx is set to 1 again, NT6512 can service multi-level interrupts.

(b) Vector Address and Interrupt Priority

Priority	Interrupt source
1 (Most)	RESET
2	BTM
3	TMR0
4	Reserved
5 (Least)	PB

9. System Clock and Oscillation Circuit

The system clock generator produces clock pulses supplied to the CPU and on-chip peripherals.

- Instruction cycle time
  2 μs for 2 MHz clock

10. HALT or STOP

- After execution of HALT, NT6512 will enter HALT. In HALT, the CPU will stop operating, but the peripheral circuit (timer) will operate.

- After execution of STOP, NT6512 will enter STOP. In STOP, the entire chip (including RC oscillator) will stop operating. If 32.768Khz clock is activated by setting BTM.2-BTM.0, the Base Timer keeps running even in STOP mode. In the same manner, LCD outputs waveform if 32.768Khz LCD clock source is choosed in STOP mode.

- In HALT, NT6512 will wake up if an interrupt occurs.
- In STOP, NT6512 will wake up if port interrupt occurs or BTM interrupt occurs.

11. Warm-up Timer

The warm-up timer eliminates an initial oscillation instability in the following two cases: 1) power-on reset, and 2) wake-up from STOP. Software warm-up is needed for Base Timer startup.

The warm-up time interval is 32 clock cycles.

12. System Reset

- Hardware reset input
- Warm-up timer for power-on reset

(a) Initial State

Hardware	After Power-on Reset
Program Counter	$000
CY	Undefined
Data Memory	Undefined
System Register	Undefined
AC	Undefined
Timer Counter	Undefined
Timer Load Register	Undefined
Interrupt Enable Flags	0
Interrupt Request Flags	0
DPH, DPM, DPL	Undefined
TBR	Undefined
LCD Driver Output	active
Base Timer	stop
PORT A	$0
PORT B	$F
Bank bit 2, 1, 0	$0

13. Instruction Set

All instructions are one cycle, one word.

Arithmetic and Logical Instruction

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X(,B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X(,B)	00000 1bbb xxx xxxx	AC,Mx ← Mx + AC + CY	CY
ADD X(,B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X(,B)	00001 1bbb xxx xxxx	AC,Mx ← Mx + AC	CY
SBC X(,B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X(,B)	00010 1bbb xxx xxxx	AC,Mx ← Mx + -AC + CY	CY
SUB X(,B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X(,B)	00011 1bbb xxx xxxx	AC,Mx ← Mx + -AC +1	CY
EOR X(,B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X(,B)	00100 1bbb xxx xxxx	AC,Mx ← Mx ⊕ AC	
OR X(,B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X(,B)	00101 1bbb xxx xxxx	AC,Mx ← Mx | AC	
AND X(,B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X(,B)	00110 1bbb xxx xxxx	AC,Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3]; AC[0] → CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X,I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X,I	01001 iiii xxx xxxx	AC,Mx ← Mx + I	CY
SBI X,I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X,I	01011 iiii xxx xxxx	AC,Mx ← Mx + -I + 1	CY
EORIM X,I	01100 iiii xxx xxxx	AC,Mx ← Mx ⊕ I	
ORIM X,I	01101 iiii xxx xxxx	AC,Mx ← Mx | I	
ANDIM X,I	01110 iiii xxx xxxx	AC,Mx ← Mx & I	

* In the assembler ASM66 V1.0, EORIM memonic is EORI. However, EORI has the same operation identical with EORIM. Same for the ORIM with respect to ORI, and ANDIM with respect to ANDI.

Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC;Mx ← Decimal adjust for add.	CY
DAS X	11001 1010 xxx xxxx	AC;Mx ← Decimal adjust for sub.	CY

Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X(,B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X(,B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X,I	01111 iiii xxx xxxx	AC,Mx ← I	

Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC=0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC≠0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY=1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY≠1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC(0)=1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC(1)=1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC(2)=1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC(3)=1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC +1 PC ← X(Not include p)	
RTNW H;L	11010 000h hhh llll	PC ←ST; TBR ← hhhh; A ← llll	
RTNI	11010 1000 000 0000	CY;PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X(Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (A)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank=000
p	ROM page =0		
ST	Stack	TBR	Table Branch Register

There are 3 new instruction added: SHR, BNZ, and BNC. They are available on development system which uses NT6610C emulation chip only.

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3Vto +7V

Input Voltage . . . . . .-0.3V to V_{DD} +0.3V

Operating Ambient Temperature . . . . . .-10°C to +60°C

Storage Temperature . . . . . -55°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 4.5V, GND = 0V, T_A = 25°C, F_{OSC} = 2 MHz, unless otherwise specified)

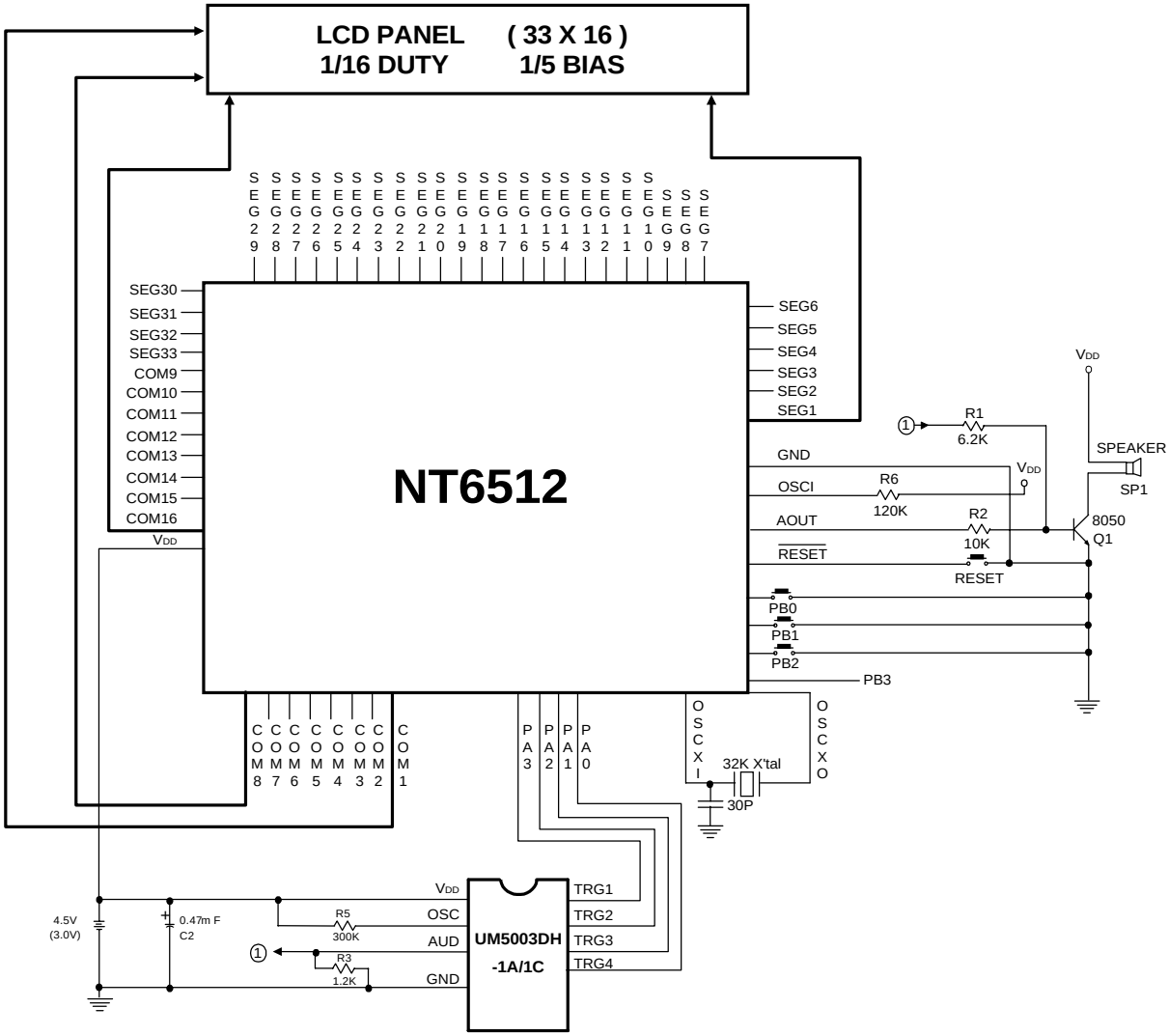
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD}	Operating Voltage	3.6	4.5	5.5	V	
I_{OP}	Operating Current		0.5	0.8	mA	V_{DD} = 4.5V, no load
I_{SB1}	Standby Current (Stop, Base Timer on, LCD off)		4.5	7.5	μA	V_{DD} = 4.5V, RC OSC stop, all outputs unloaded
I_{SB2}	Standby Current(Stop)		0.7	1.2	μA	V_{DD} = 4.5V, OSC and Base timer stop, all outputs unloaded
I_I	Input Current		10	50	μA	V_{DD} = 4.5V V(input) = 4.5V
V_{IH}	Input High Voltage	V_{DD}-0.5		V_{DD}+0.3	V	
V_{IL}	Input Low Voltage	-0.3		GND+0.5	V	
I_{OL}	Output Low Drive Current	3.5			mA	PORTA and PORTB, V_{OL} = 0.8V
I_{OH}	Output High Drive Current	500			μA	PORTA, V_{OL} = V_{DD} -0.5V
I_{OH} I_{OL}	AOUT, $\overline{AOUT}$ Output Current	2 2			mA mA	V_{OUT} = V_{DD} -1V V_{OUT} = 0.5V
I_{LCD}	LCD Lighting		25.0	35.0	μA	V_{DD} = 4.5V, LCD on current
R_{PU}	Pull-up Resistance		20	100	KΩ	PORTB

DC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25°C, F_{OSC} = 2 MHz, unless otherwise specified)

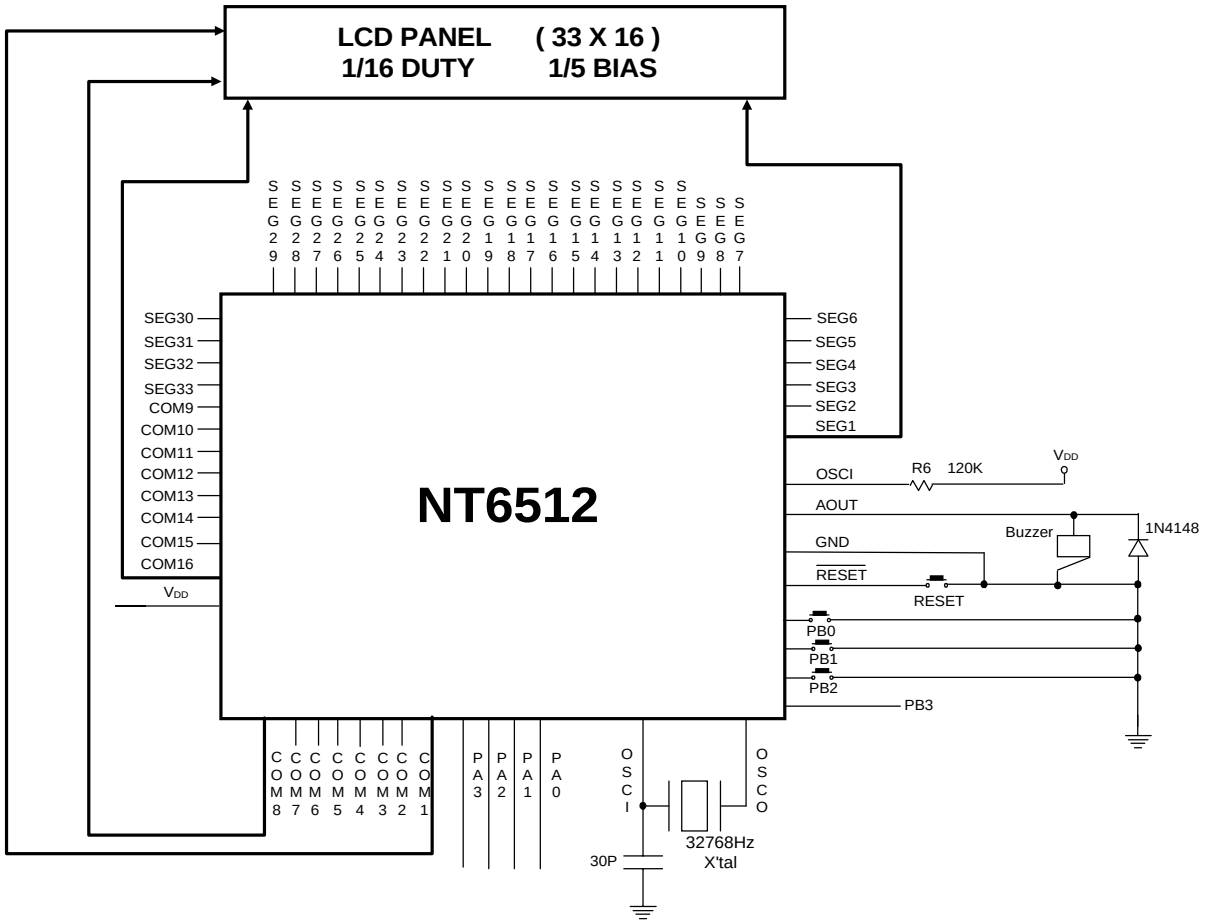
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD}	Operating Voltage	2.4	3.0	3.4	V	
I_{OP}	Operating Current		0.26	0.3	mA	V_{DD} = 3.0V, no load, 32.768KHz OSC off
I_{SB1}	Standby Current (Stop, Base Timer on, LCD off)		1.5	2.5	μA	V_{DD} = 3.0V, RC OSC stop, all outputs unloaded
I_{SB2}	Standby Current(Stop)		0.7	1.2	μA	V_{DD} = 3.0V, OSC and Base timer stop, all outputs unloaded
I_I	Input Current		6	35	μA	V_{DD} = 3.0V V(input) = 3.0V
V_{IH}	Input High Voltage	V_{DD}-0.5		V_{DD}+0.3	V	
V_{IL}	Input Low Voltage	-0.3		GND+0.5	V	
I_{OL}	Output Low Drive Current	1.2			mA	PORTA and PORTB, V_{OL} = 0.5V
I_{OH}	Output High Drive Current	250			μA	PORTA, V_{OL} = V_{DD} -0.5V
I_{OH} I_{OL}	AOUT, $\overline{AOUT}$ Output Current	1.2 1.2			mA mA	V_{OUT} = V_{DD} -0.6V V_{OUT} = 0.5V
I_{LCD}	LCD Lighting		15.0	17.0	μA	V_{DD} = 3.0V, LCD on current
R_{PU}	Pull-up Resistance		20	100	KΩ	PORTB

Application Circuit (for reference only)

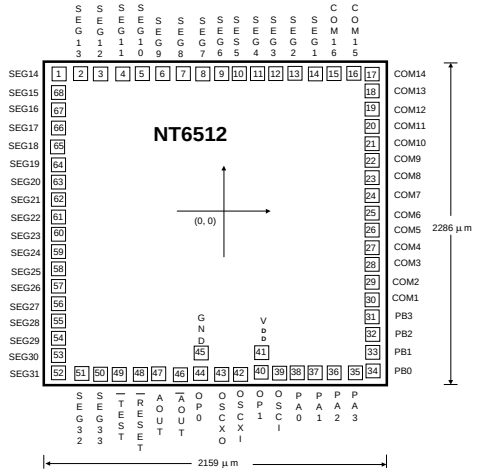
AP1:



AP2:


LCD PANEL (33 X 16)
1/16 DUTY 1/5 BIAS
NT6512
SEG30
SEG31
SEG32
SEG33
COM9
COM10
COM11
COM12
COM13
COM14
COM15
COM16
VDD
SEG6
SEG5
SEG4
SEG3
SEG2
SEG1
OSCI
R6 120K
VDD
AOUT
Buzzer
1N4148
GND
RESET
RESET
PB0
PB1
PB2
PB3
PA3
PA2
PA1
PA0
OSCI
OSCO
30P
32768Hz
X'tal

Bonding Diagram



* Substrate connect to GND

unit: µm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	SEG14	-959	1017	35	PA3	830	-1017
2	SEG13	-829	1017	36	PA2	700	-1017
3	SEG12	-699	1017	37	PA1	580	-1017
4	SEG11	-579	1017	38	PA0	460	-1017
5	SEG10	-459	1017	39	OSCI	345	-1017
6	SEG9	-344	1017	40	OP1	230	-1017
7	SEG8	-229	1017	41	V_{DD}	230	-923
8	SEG7	-114	1017	42	OSCXI	115	-1017
9	SEG6	0	1017	43	OSCXO	0	-1017
10	SEG5	115	1017	44	OP0	-115	-1017
11	SEG4	230	1017	45	GND	-114	-920
12	SEG3	345	1017	46	$\overline{AOUT}$	-230	-1017
13	SEG2	460	1017	47	AOUT	-345	-1017
14	SEG1	580	1017	48	$\overline{RESET}$	-459	-1017
15	COM16	700	1017	49	$\overline{TEST}$	-579	-1017
16	COM15	830	1017	50	SEG33	-699	-1017
17	COM14	960	1017	51	SEG32	-829	-1017
18	COM13	960	887	52	SEG31	-959	-1017
19	COM12	960	757	53	SEG30	-959	-887
20	COM11	960	637	54	SEG29	-959	-757
21	COM10	960	517	55	SEG28	-959	-637
22	COM9	960	402	56	SEG27	-959	-517
23	COM8	960	287	57	SEG26	-959	-402
24	COM7	960	172	58	SEG25	-959	-287
25	COM6	960	57	59	SEG24	-959	-172
26	COM5	960	-57	60	SEG23	-959	-57
27	COM4	960	-172	61	SEG22	-959	57
28	COM3	960	-287	62	SEG21	-959	172
29	COM2	960	-402	63	SEG20	-959	287
30	COM1	960	-517	64	SEG19	-959	402
31	PB3	960	-637	65	SEG18	-959	517
32	PB2	960	-757	66	SEG17	-959	637
33	PB1	960	-887	67	SEG16	-959	757
34	PB0	960	-1017	68	SEG15	-959	887

Ordering Information

Part No.	Package
NT6512H-AXX XX	CHIP FORM