Stereo 10W (4W) Class-T Digital Audio Amplifier using Digital Power Processing™ Technology

TA1101B

June 1999

General Description

The TA1101B is a two-channel Class-T (Tripath™) Digital Audio Power Amplifier IC using Tripath's proprietary Digital Power Processing™ technology. Class-T amplifiers offer both the audio fidelity of Class-AB and the power efficiency of Class-D amplifiers.

Applications

- Computer/PC Multimedia
- Video CD Players
- Cable Set-Top Products
- Televisions
- DVD Players
- Battery Powered Systems

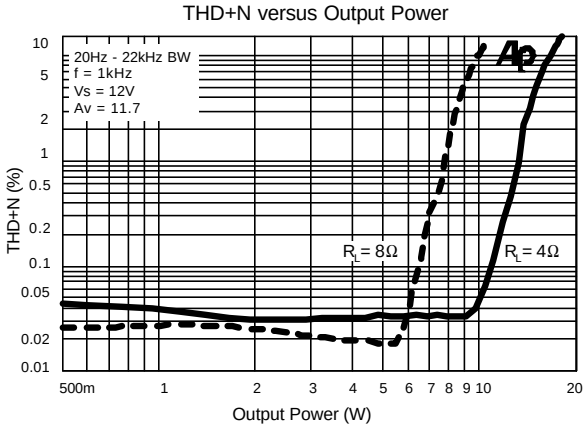
Benefits

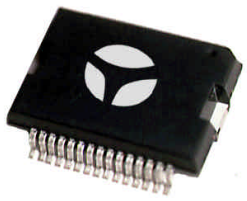
- Fully integrated solution with FETs
- Easier to design-in than Class-D
- Reduced system cost with no heat sink
- Dramatically improves efficiency versus Class-AB
- Signal fidelity equal to high quality linear amplifiers
- High dynamic range compatible with digital media such as CD, DVD, and Internet audio

Features

- Class-T architecture
- Proprietary Digital Power Processing
- Single Supply Operation
- "Audiophile" Quality Sound
  - 0.04% THD+N @ 9Wrms, 4Ω
  - 0.18% IHF-IM @ 1Wrms, 4Ω
  - 6Wrms @ 8Ω, 0.1% THD+N
  - 10Wrms @ 4Ω, 0.1% THD+N
- High Power
  - 10Wrms @ 8Ω, 10% THD+N
  - 15Wrms @ 4Ω, 10% THD+N
- High Efficiency
  - 88% @ 10Wrms, 8Ω
  - 81% @ 15Wrms, 4Ω
- Dynamic Range = 102 dB
- Mute and Sleep inputs
- Turn-on & turn-off pop suppression
- Over-current protection
- Over-temperature protection
- Bridged outputs
- Supports 100kHz BW Super Audio CD and DVD-Audio (See App Note for specifics)
- 30-pin Power SOP package

Typical Performance





Absolute Maximum Ratings[Note 1]

SYMBOL	PARAMETER	Value	UNITS
V_{DD}	Supply Voltage	16	V
T_{STORE}	Storage Temperature Range	-40 to 150	ºC
T_A	Operating Free-air Temperature Range	0 to 70	ºC
P_{DISS}	Continuous Total Power Dissipation	Note 2	W

Notes 1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
2) See Power Dissipation Derating section in Applications Information.

Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{DD}	Supply Voltage	8.5	12	13.2	V
V_{IH}	High-level Input Voltage (MUTE, SLEEP)	3.5			V
V_{IL}	Low-level Input Voltage (MUTE, SLEEP)			1	V

Note: Recommended Operating Conditions indicate conditions for which the device is functional. See Electrical Characteristics for guaranteed specific performance limits.

Electrical Characteristics

See Test/Application Circuit. Unless otherwise specified, V_{DD} = 12V, f = 1kHz, Measurement Bandwidth = 22kHz, R_L = 4Ω, T_A = 25 °C, Package heat slug soldered to 2.8 square-inch PC pad.

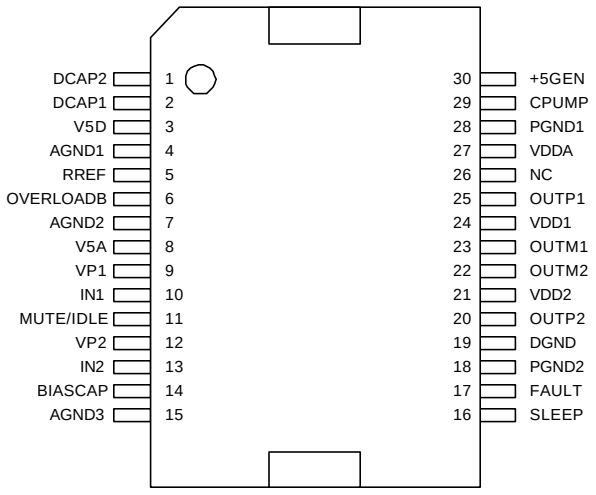
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
P_O	Output Power (Continuous RMS/Channel)	THD+N = 0.1% R_L = 4Ω R_L = 8Ω THD+N = 10% R_L = 4Ω R_L = 8Ω	9 5.5 12 8	10 6 15 10		W W W W
$I_{DD,MUTE}$	Mute Supply Current	MUTE = V_{IH}		5.5	7	mA
$I_{DD, SLEEP}$	Sleep Supply Current	SLEEP = V_{IH}		0.25	2	mA
I_q	Quiescent Current	V_{IN} = 0 V		61	75	mA
THD + N	Total Harmonic Distortion Plus Noise	P_O = 9W/Channel		0.04		%
IHF-IM	IHF Intermodulation Distortion	19kHz, 20kHZ, 1:1 (IHF)		0.18	0.5	%
SNR	Signal-to-Noise Ratio	A Weighted, P_{OUT} = 1W, R_L = 8Ω		89		dB
CS	Channel Separation	30kHz Bandwidth	50	55		dB
PSRR	Power Supply Rejection Ratio	Vripple = 100mV. Input Referred	60	80		dB
η	Power Efficiency	P_{OUT} = 10W/Channel, R_L = 8Ω		88		%
V_{OFFSET}	Offset Voltage	No Load, MUTE/IDLE = Logic Low		50	150	mV
V_{OH}	High-level output voltage (FAULT & OVERLOAD)		3.5			V
V_{OL}	Low-level output voltage (FAULT & OVERLOAD)				1	V
e_{OUT}	Output Noise Voltage	A Weighted, no signal, input shorted, DC offset nulled to zero		100		µV

Minimum and maximum limits are guaranteed but may not be 100% tested.

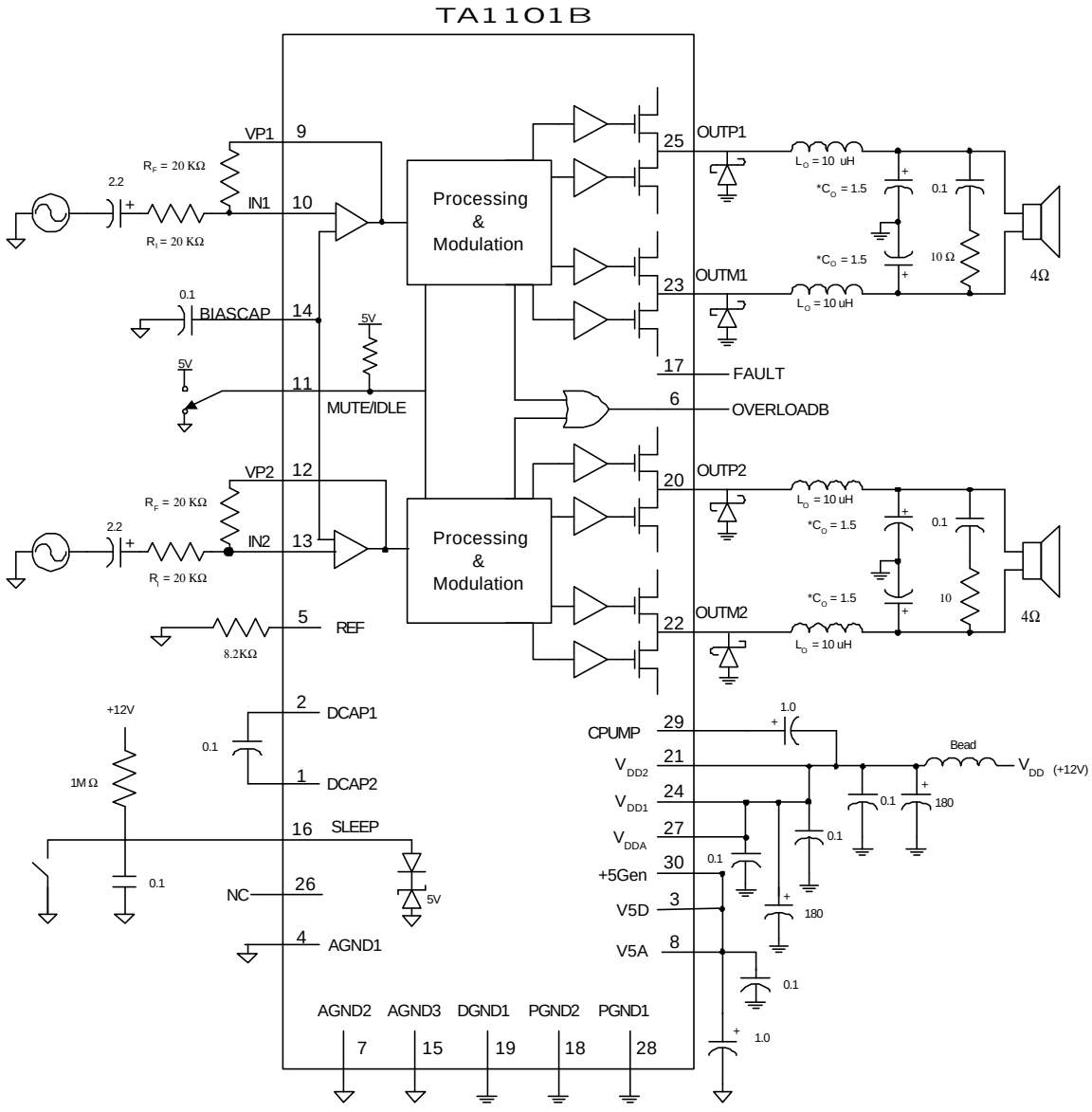
Pin Description

Pin	Function	Description
1, 2	DCAP2, DCAP1	Charge pump switching capacitor
3, 8	V5D, V5A	Digital +5V, Analog +5V
4, 7, 15	AGND1, AGND2, AGND3	Analog Ground
5	RREF	Reference resistor
6	OVERLOADB	A logic low output indicates the input signal has overloaded the amplifier.
9, 12	VP1, VP2	Input stage feedback drive
10, 13	IN1, IN2	Single-ended inputs
11	MUTE/IDLE	When set to logic high, both amplifiers are muted and in low power (idle) mode. When low (grounded), both amplifiers are fully operational. If left floating, the device stays in the mute mode. Ground if not used.
14	BIASCAP	Bias stabilization capacitor.
16	SLEEP	When set to logic high, device goes into low power mode. If not used this pin should be grounded
17	FAULT	A logic high output indicates thermal overload, or an output is shorted to ground or another output.
18, 28	PGND2, PGND1	Power Ground (High current)
19	DGND	Digital Ground
20, 22; 25, 23	OUTP2 & OUTM2; OUTP1 & OUTM1	Bridged outputs
21, 24	VDD2, VDD1	+12V Power (High Current)
26	NC	Not connected
27	VDDA	Analog +12V
29	CPUMP	Charge pump output capacitor
30	+5GEN	Regulated +5V source used to supply power to pins 3 & 8.

30-pin Power SOP Package
(Top View)



Test/Application Circuit



Analog Ground

Digital/Power Ground

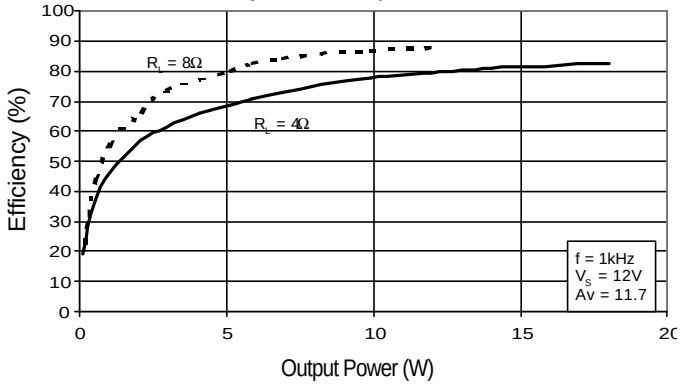
All Diodes Motorola MBRS130T3

All capacitance in uF

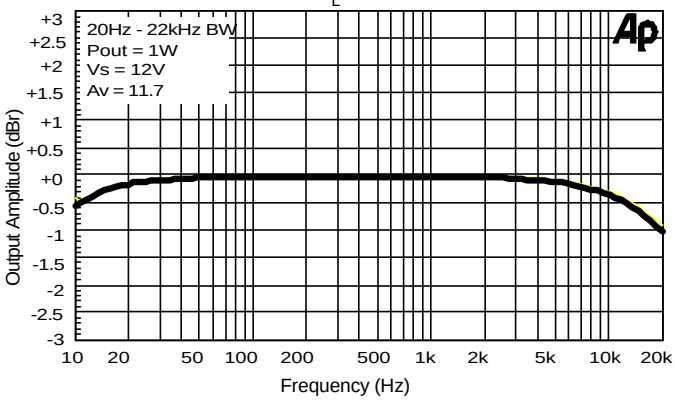
* Use C0 = .22uF for 8 Ohm loads

Typical Performance Characteristics

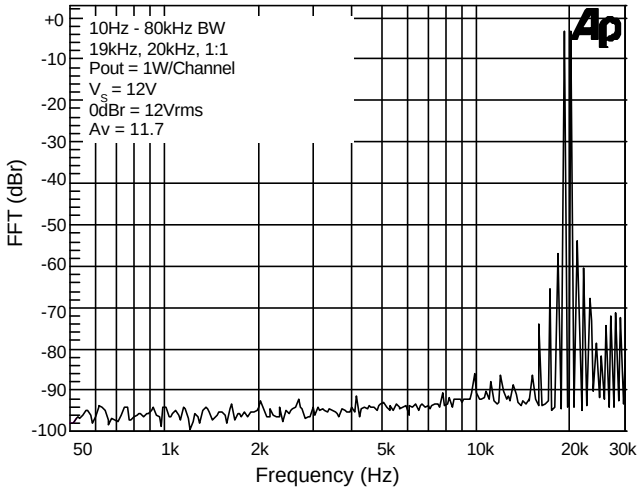
Efficiency versus Output Power



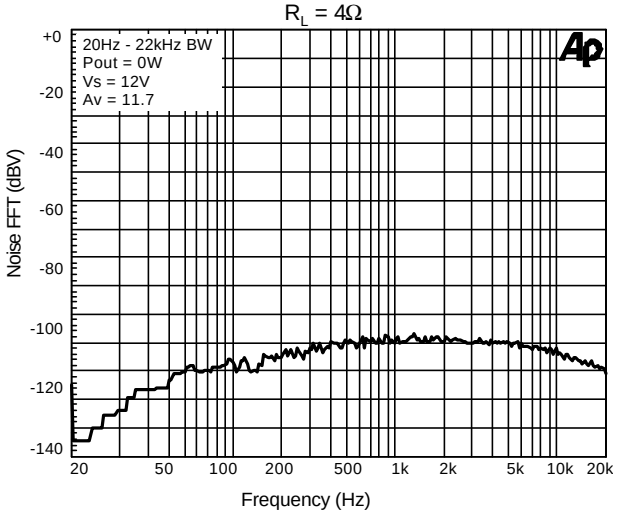
Frequency Response
R_L = 4 Ω



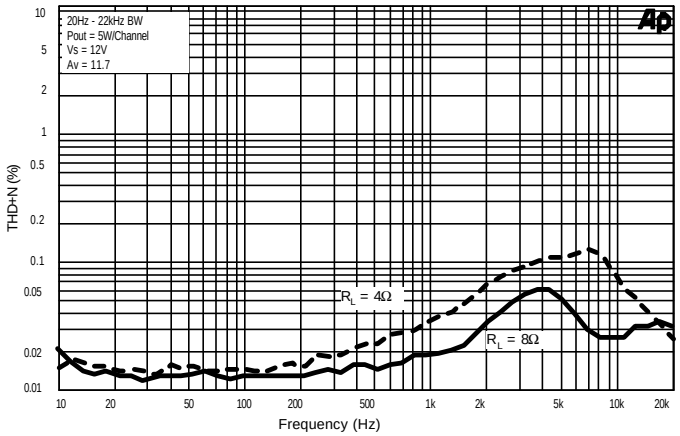
Intermodulation Performance
R_L = 4Ω



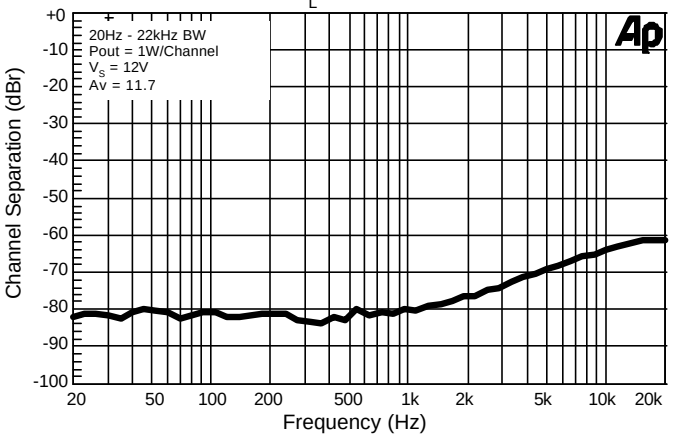
A-Weighted Noise FFT
R_L = 4Ω



THD+N versus Frequency



Channel Separation versus Frequency
R_L = 4Ω



Application Information

Amplifier Gain

The gain of the TA1101B is set by the ratio of two external resistors, R_I and R_F, and is given by the following formula:

$$V_O/V_I = 12R_F/R_I$$

Where V_I is the input signal level and V_O is the differential output signal level across the speaker.

9 watts of RMS output power results from an 8.485 V RMS signal across an eight-ohm speaker load. If $R_F = R_I$, then 9 Watts will be achieved with 0.707 V RMS of input signal.

$$8.485\text{V RMS} = (R_L * P_O)^{1/2} = (8\ \text{ohms} * 9\ \text{Watts})^{1/2}$$

Protection Circuits

The TA1101B is guarded against over-temperature and over-current conditions. When the device goes into an over-temperature or over-current state, the FAULT pin goes to a logic HIGH state indicating a fault condition. When this occurs, all amplifier outputs are TRI-STATED and will float to 1/2 of V_{DD}, thereby muting the amplifier.

Over-temperature Protection

An over-temperature fault occurs if the junction temperature of the part exceeds approximately 155°C. The thermal hysteresis of the part is approximately 45°C, therefore the fault will automatically clear when the junction temperature drops below 110°C.

Over-current Protection

An over-current fault occurs if more than approximately 7 amps of current flows from any of the amplifier output pins. This can occur if the speaker wires are shorted together or if one side of the speaker is shorted to ground. An over-current fault sets an internal latch that can only be cleared if the MUTE pin is toggled or if the part is powered down. Alternately, if the MUTE pin is connected to the FAULT pin, the HIGH output of the FAULT pin will toggle the MUTE pin and automatically reset the fault condition.

Overload

The OVERLOADB pin is a 5V logic output. When low, it indicates that the level of the input signal has overloaded the amplifier resulting in increased distortion at the output. The OVERLOADB signal can be used to control a distortion indicator light or LED through a simple buffer circuit.

Sleep Pin

The SLEEP pin is a 5V logic input that when pulled high (>3.5V) puts the part into a low quiescent current mode. This pin is internally clamped by a zener diode to approximately 6V thus allowing the pin to be pulled up through a large valued resistor (1MΩ recommended) to V_{DD}. To disable SLEEP mode, the sleep pin should be grounded.

Fault Pin

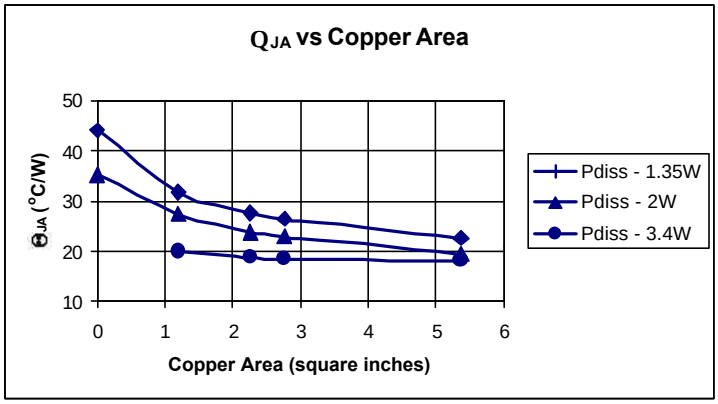
The FAULT pin is a 5V logic output that indicates various fault conditions within the device. These conditions include: low supply voltage, low charge pump voltage, low 5V regulator voltage, over current at any output, and junction temperature greater than approximately 155°C. The FAULT output is capable of directly driving an LED through a series 200-Ohm resistor. If the FAULT pin is connected directly to the MUTE input an automatic reset will occur in the event of an over-current condition.

Power Dissipation Derating

For operating at ambient temperatures above 25°C the device must be derated based on a 150°C maximum junction temperature, T_J(max) as given by the following equation:

$$P_{DISS} = (T_J(\text{max}) - T_A)/\theta_{JA}$$

Where θ_{JA} of the package is determined from the following graph:



In the above graph Copper Area is the size of the copper pad on the PC board to which the heat slug of the TA1101B is soldered.

Performance Measurements of the TA1101B

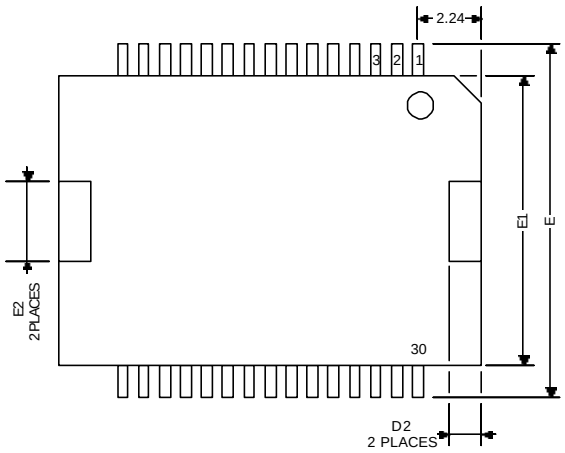
Tripath amplifiers operate by generating a high frequency switching pattern based on the input signal. This signal is sent through a low-pass filter (external to the Tripath amplifier) that recovers an amplified version of the audio input. The frequency of the switching pattern is spread spectrum and typically varies between 100kHz and 1.0MHz, which is well above the 20Hz – 20kHz audio band. The pattern itself does not alter or distort the audio input signal but it does introduce some inaudible components.

The measurements of certain performance parameters, particularly noise related specifications such as THD+N, are significantly affected by the design of the low-pass filter used on the output as well as the bandwidth setting of the measurement instrument used. Unless the filter has a very sharp roll-off just beyond the audio band or the bandwidth of the measurement instrument is limited, some of the inaudible noise components introduced by the Tripath amplifier switching pattern will degrade the measurement.

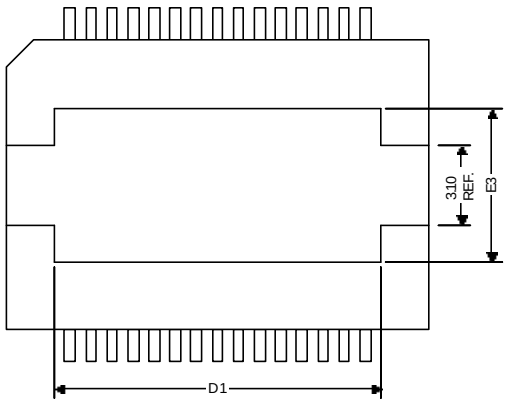
One feature of Tripath amplifiers is that they do not require large multi-pole filters to achieve excellent performance in listening tests, usually a more critical factor than performance measurements. Though using a multi-pole filter may remove high-frequency noise and improve THD+N type measurements (when they are made with wide-bandwidth measuring equipment), these same filters degrade frequency response. The TA1101B Evaluation Board uses the Test/Application Circuit of this data sheet, which has a simple two-pole output filter and excellent performance in listening tests. Measurements in this data sheet were taken using this same circuit with a limited bandwidth setting in the measurement instrument.

Package Information

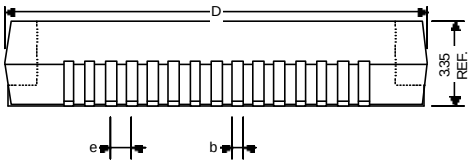
30-Lead Power Small Outline Package (PSOP),
compliant with JEDEC outline MO-166, variation AD:



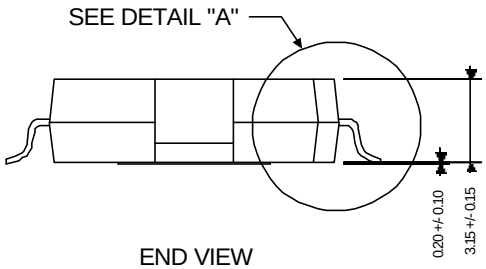
TOP VIEW



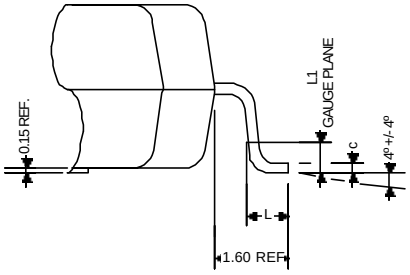
BOTTOM VIEW



SIDE VIEW



END VIEW



DETAIL "A"

Package Dimensions

Dimension	Min.	Nom.	Max.
b	0.35	---	0.48
c	0.23	---	0.32

D	15.80	15.90	16.00
D1	12.60	---	13.00
D2	---	---	1.10
E	13.90	14.20	14.50
E1	10.90	11.00	11.10
E2	---	---	2.90
E3	5.80	---	6.20
e	0.80 BSC.		
L1	0.25 BSC.		
L	0.70	---	1.00

Note: All dimensions are in millimeters.

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