NT66P22A

PRELIMINARY

OTP 4-bit Microcontroller

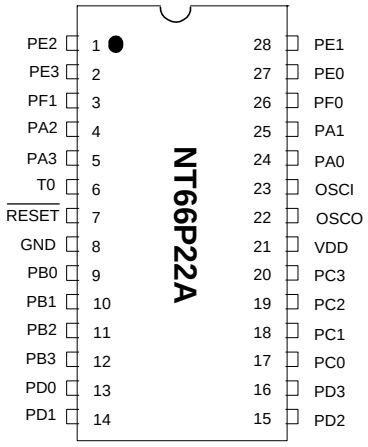
Features

- NT6610C-based single-chip 4-bit micro-controller.
- OTPROM: 4K × 16 bits.
- RAM: 160 × 4 bits (data memory)
- Operation voltage: 2.4V - 6.0V (typical 3.0V or 5.0V).
- 22 CMOS bi-directional I/O pins.
- 4-level subroutine nesting (including interrupts).
- One 8-bit auto re-load timer/counter.
- Warm-up timer for power on reset.
- Powerful interrupt sources:
  - Internal interrupt (Timer0).
  - External interrupts: PortB & PortC (falling edge).
- Oscillator (OTP option)
  - X`tal oscillator: 32.768KHz ~ 4MHz.
  - Ceramic resonator: 400K ~ 4MHz.
  - RC oscillator : 400K ~ 4MHz.
  - External clock: 30K ~ 4MHz.
- Instruction cycle time:
  - 4/32.768KHz(122us) for 32.768KHz OSC clock.
  - 4/4MHz (1us) for 4MHz OSC clock.
- Two low power operation modes: HALT and STOP.
- Built-in watch dog timer (OTP option)
- Built-in power on reset

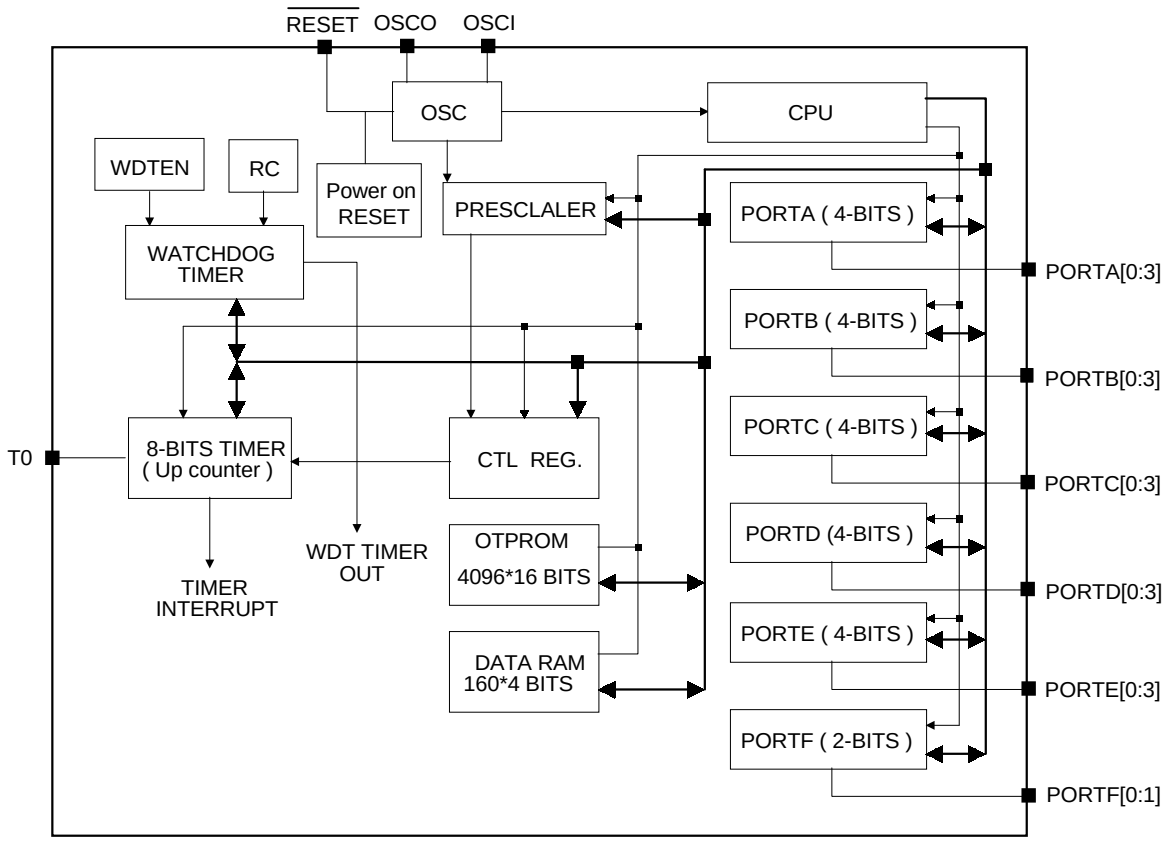
General Description

NT66P22A is a 4-bit micro controller. This chip integrates the NT6610C 4-bit CPU core with SRAM, 4K OTPROM, Timer and I/O Ports.

Pin Configuration



Block Diagram



Pin Description

Pin No.	Designation	I/O	Descriptions
27,28,1,2	PE.0 – PE.3	I/O	Bit programmable I/O.
26,3	PF.0 – PF.1	I/O	Bit programmable I/O.
24,25,4,5	PA.0 – PA.3	I/O	Bit programmable I/O.
6	T0	I	Timer Clock/Counter input pin. (schmitt trigger input).
7	$\overline{\text{RESET}}$	I	Reset input (active low, schmitt trigger input).
8	GND	P	Ground pin.
9 – 12	PB.0 – PB.3	I/O	Bit programmable I/O. Vector Interrupt (active falling edge).
13- 16	PD.0 – PD.3	I/O	Bit programmable I/O.
17 – 20	PC.0 – PC.3	I/O	Bit programmable I/O. Vector Interrupt (active falling edge).
21	VDD	P	Power supply pin.
22	OSCO	O	OSC output pin. Output a frequency of Fosc/4 for RC mode.
23	OSCI	I	OSC input pin, connected to crystal, ceramic or external resistor.

Function Description

1 CPU

The CPU contains the following function blocks: Program Counter, Arithmetic Logic Unit (ALU), Carry Flag, Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL), and Stack.

1.1 PC (Program Counter)

The Program Counter is used to address the 4K program ROM. It consists of 12-bits: Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter normally increases by one (+1) with every execution of an instruction except in the following cases:

1) When executing a jump instruction (such as JMP, BA0, BAC),
2) When executing a subroutine call instruction (CALL),
3) When an interrupt occurs,
4) When the chip is at the INITIAL RESET mode.

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

1.2 ALU and CY

ALU performs arithmetic and logic operations. The ALU provides the following functions:
Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjust for addition/subtraction (DAA, DAS) Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)
Decision (BA0, BA1, BA2, BA3, BAZ, BAC)
Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow, which the arithmetic operation generates. During an interrupt servicing or call instruction, the carry flag is pushed into the stack and restored back from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3 Accumulator

Accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with ALU, data transfer between the accumulator and system register, or data memory can be performed.

1.4 Stack

A group of registers are used to save the contents of CY & PC (10-0) sequentially with each subroutine call or interrupt. It is organized 13 bits X 4 levels. The MSB is saved for CY. 4 levels are the maximum allowed for subroutine calls and interrupts.

The contents of Stack are returned sequentially to the PC with the return instructions (RTNI/RTNW). Stack is operated on a first-in, last-out basis. This 4-level nesting includes both subroutine calls and interrupts requests. Note that program execution may enter an abnormal state if the number of calls and interrupt requests exceed 4, and the bottom of stack will be shifted out.

2 OTPROM

The NT66P22A can address up to 4096 × 16 bit words of program area from $000 to $FFF.
Service routine as starting vector address.

Address	Instruction	Remark
$000H	JMP instruction	Jump to RESET service routine.
$001H	NOP	Reserved.
$002H	JMP instruction	Jump to TIMER0 service routine.
$003H	NOP	Reserved.
$004H	JMP instruction	Jump to PBC service routine.

3 RAM

Built-in RAM consists of general-purpose data memory and system register. Direct addressing in one instruction can access data memory and system register.

The following is the memory allocation map:

$000 ~ $01F: System register and I/O.
$020 ~ $0BF: Data memory (160 × 4 bits, devide into 2 banks. $020 - $07F: bank0, $080 - $0BF: bank1).

The configuration of system Register

	Bit3	Bit2	Bit1	Bit0	R/W	Remark
$00	-	IET0	-	IEP	R/W	Interrupt enable flags.
$01	-	IRQT0	-	IRQP	R/W	Interrupt request flags.
$02	-	TM0.2	TM0.1	TM0.0	R/W	Timer0 Mode register(Prescaler)
$03	-	-	-	-	-	Reserved.
$04	TL0.3	TL0.2	TL0.1	TL0.0	R/W	Timer0 load/counter register low digit.
$05	TH0.3	TH0.2	TH0.1	TH0.0	R/W	Timer0 load/counter register high digit.
$06	-	-	-	-	-	Reserved.
$07	LPD3	LPD2	LPD1	LPD0	W	LPD Enable Control (LPD3~0): 1010: LPD Enable (Default); 0101: LPD Disable
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE
$0D	-	-	PF.1	PF.0	R/W	PORTF
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register.
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register.
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12		DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX HIGH nibble
$13 ~ $15	-	-	-	-	-	Reserved.
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	W	Set PORTA to be output port.
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	W	Set PORTB to be output port.
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	W	Set PORTC to be output port.
$19	PD3OUT	PD2OUT	PD1OUT	PD0OUT	W	Set PORTD to be output port.
$1A	PE3OUT	PE2OUT	PE1OUT	PE0OUT	W	Set PORTE to be output port.
$1B	-	-	PF1OUT	PF0OUT	W	Set PORTF to be output port.
$1C	-	-	T0S	T0E	W	Bit0:T0 signal edge; Bit1: T0 signal source.
$1D	-	-	-	-	-	Reserved.
$1E	WDT	-	-	-	W	Bit3: Watchdog timer reset. (write 1 to reset WDT)
$1F	-	-	-	-	-	Reserved.

*System Register $00~$12（except $07H） refer to "NT6610C User manual".

Low Power Detection（LPD）

The LPD function is to monitor the supply voltage and applies an internal reset in the micro-controller at the time of battery replacement. If the applied circuit satisfies the following conditions, the LPD can be incorporated by software control.

- High reliability is not required.
- Power supply voltage V_{DD}=2.4 to 6.0 V
- Operating ambient temperature T_A= -10℃ to +60℃

Functions of LPD Circuit

The LPD circuit has the following functions:

- Generates an internal reset signal when $V_{DD} \leq V_{LPD}$.
- Cancels the internal reset signal when $V_{DD} > V_{LPD}$.

Here, V_{DD}: power supply voltage, V_{LPD}: LPD detect voltage, about 1.6~1.7V and lower than $V_{DD\text{-}MIN}$ (2.4V).

LPD Control Register

The LPD circuit is controlled by software enable flag.

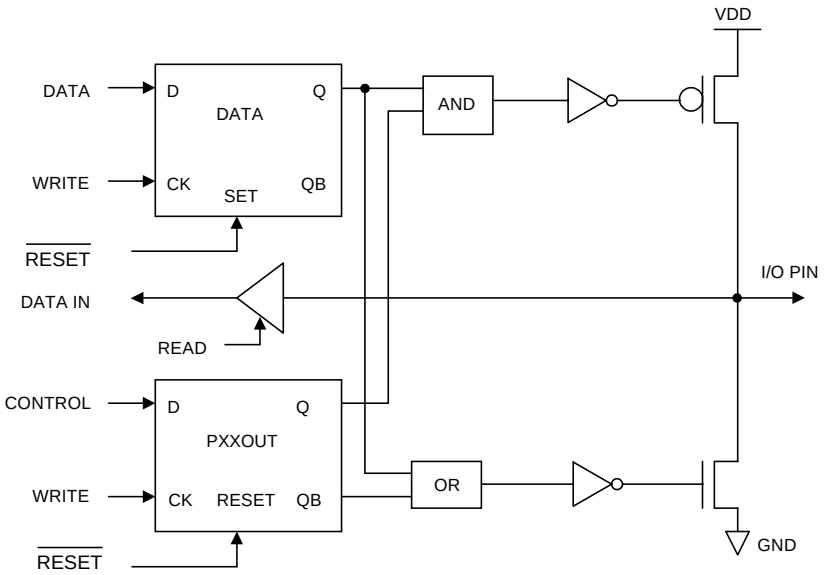
	Bit3	Bit2	Bit1	Bit0	R/W	Remark
$07	LPD3	LPD2	LPD1	LPD0	W	LPD Enable Control (LPD3~0): 1010: LPD Enable (Default); 0101: LPD Disable

LPD3、	LPD2、	LPD1、	LPD0：	LPD Enable/Disable flag．
1	0	1	0	Enable LPD circuit (Power-on initial)．
0	1	0	1	Disable LPD circuit．

System Register $16~$1B

	Bit3	Bit2	Bit1	Bit0	R/W	Remark
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	W	Set PORTA to be output port.
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	W	Set PORTB to be output port.
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	W	Set PORTC to be output port.
$19	PD3OUT	PD2OUT	PD1OUT	PD0OUT	W	Set PORTD to be output port.
$1A	PE3OUT	PE2OUT	PE1OUT	PE0OUT	W	Set PORTE to be output port.
$1B	-	-	PF1OUT	PF0OUT	W	Set PORTF to be output port.

Equivalent Circuit for a Single I/O Pin



PAXOUT, PBXOUT, PCXOUT, PDXOUT, PEXOUT (X=0,1,2,3), PFXOUT (X=0,1)

1: Use as output buffer.

0: Use as input buffer (Power on initial).

T0 & WDT

System Register $1C

	BIT3	BIT2	BIT1	BIT0	R/W	Remark
$1C	-	-	T0S	T0E	W	Bit0: T0 signal edge. Bit1: T0 signal source.

T0E: T0 signal edge.

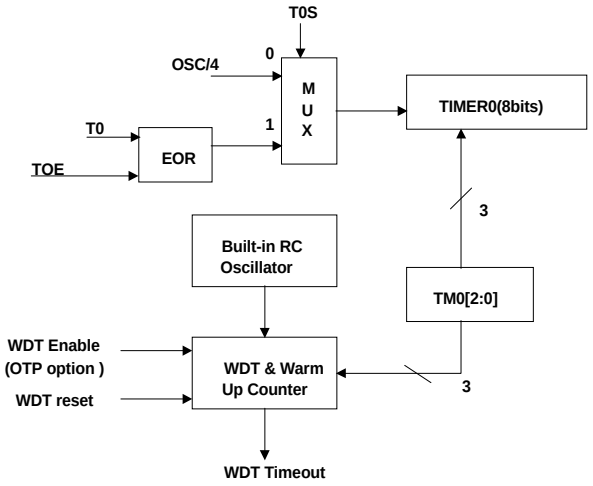
0: Increment on low-to-high transition T0 pin (Power on initial).

1: Increment on high-to-low transition T0 pin.

T0S: T0 signal source.

0: OSC 1/4 (Power on initial).

1: Transition on T0 pin.



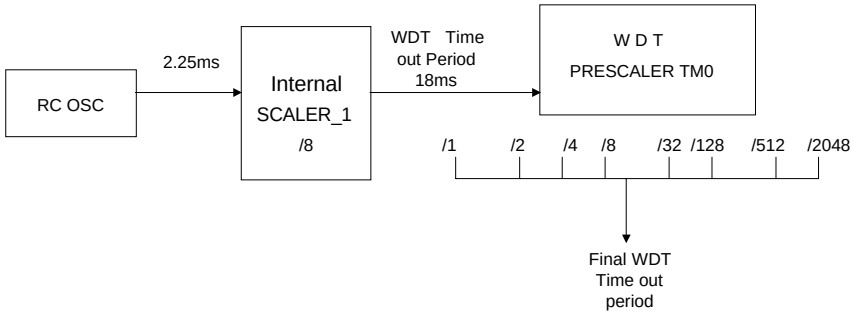
System Register $1E

	Bit3	Bit2	Bit1	Bit0	R/W	Remark
$1E	WDT	-	-	-	W	Bit3: Watchdog timer reset. (write 1 to reset WDT)

The input clock of watchdog timer is generated by a built-in RC oscillator. So the WDT will always run even in the STOP mode. NT66P22A generates a RESET condition when watch dog times-out. Watch dog can be enabled or disabled permanently by OTP option. To prevent it timing out and generating a device RESET condition, you should write this bit as "1" before timing-out. The WDT has a time-out period of approx. 18ms(V_{DD}=5V).If longer time-out periods are desired, a prescaler with a division ratio of up to 1:2048 can be assigned to the WDT under software controlled by writing to the TM0 register.

Prescaler divide ratio (valid for V_{DD}=5V):

TM0.2	TM0.1	TM0.0	Prescaler divide ratio	Timer-out period
1	1	1	1:1	18ms
1	1	0	1:2	36ms
1	0	1	1:4	72ms
1	0	0	1:8	144ms
0	1	1	1:32	576ms
0	1	0	1:128	2,304ms
0	0	1	1:512	9,216ms
0	0	0	1:2048 (Power on initial)	36,894ms

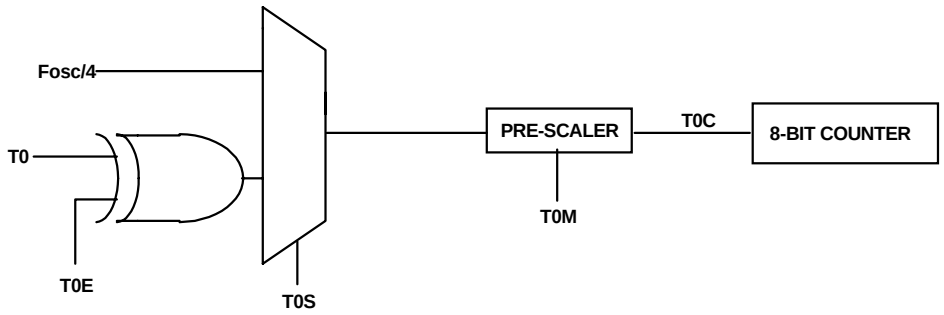


4 Timer0

NT66P22A has one 8-bit timer. The time/counter has the following features:

. 8-bit timer/counter
. Readable and writeable
. Automatic reloadable counter
. 8-prescaller scale is available
. Internal and external clock select
. Interrupt on overflow from $FF to $00
. Edge select for external event

Following is a simplified timer block diagram:



4.1 Configuration and Operation

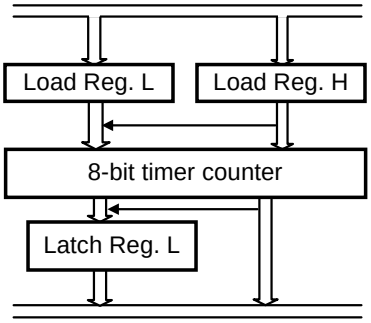
Timer-0 consists of an 8-bit write-only timer load register (TL0L, TL0H), and an 8-bit read-only timer counter (TC0L, TC0H). The counter and load register both have low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H) could initialize the timer counter. Load register programming: Write the low-order digit first and then the high-order digit. The timer counter is loaded with the content of load register automatically when the high order digit is written or counter counts overflow from $FF to $00.
Timer Load Register: Since the register H would control the physical READ and WRITE operation. Please follow these rules:

Write Operation:

First write Low nibble,
Then write High nibble to update the counter.

Read Operation:

High nibble first;
Low nibble followed.



4.2 Timer0 Interrupt

The timer overflow will generate an internal interrupt request, when the counter counts overflow from $FF to $00. If the interrupt enable flag is enabled, then a timer interrupt service routine will proceed. This can also be used to wake CPU from HALT mode.

4.3 Timer0 mode register

The timer can be programmed in several different prescaler ratio by setting Timer Mode register (TM0). The 8-bit counter counts prescaler overflow output pulses. The timer mode registers (TM0) are 3-bit registers used for timer control as shown in table1. These mode registers select the input pulse sources into the timer.

Table 1: Timer 0 Mode Register ($02)

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Ratio N
0	0	0	$/2^{11}$	2048（initial）
0	0	1	$/2^{9}$	512
0	1	0	$/2^{7}$	128
0	1	1	$/2^{5}$	32
1	0	0	$/2^{3}$	8
1	0	1	$/2^{4}$	4
1	1	0	$/2^{1}$	2
1	1	1	$/2^{0}$	1

4.4 External Clock/Event T0 as Timer0 Source

When external clock/event input is used for TM0, it is synchronized with CPU system clock. Therefor the external source must follow certain constrains. The output from T0M multiplex is T0C. It is sampled by system clock in instruction frame cycle. Therefore it is necessary for T0C to be high at least 2 t_{OSC} and low at least 2 t_{OSC}. When prescaler ratio selects $/2^0$, T0C is the same as the system clock input. Therefore the requirement is as follows

T0H = T0CH = T0 high time $\geq$ 2 t_{OSC} + ΔT

T0L = T0CL = T0 low time $\geq$ 2 t_{OSC} + ΔT

Note: ΔT = 40ns

When other prescaler ratio is selected, the TM0 is scaled by the asynchronous ripple counter and so the prescaler output is symmetrical.

Then:

$$\text{T0C high time} = \text{T0C low time} = \frac{N * T0}{2}$$

Where

T0 = Timer0 input period

N = prescaler value

The requirement is , therefore:

$$\frac{N * T0}{2} \geq 2\,t_{OSC} + \Delta T \text{ , or } T0 \geq \frac{4 * t_{OSC} + 2\Delta T}{N}$$

The limitation is applied for T0 period time only. The pulse width is not limited by this equation. It is summarized as follows:

$$\text{T0 = Timer0 period} \geq \frac{4 * t_{OSC} + 2\Delta T}{N}$$

5 Port Interrupt

PBC interrupt (PORTB & PORTC, 8bits) is falling edge active. It is means that if an interrupt request (IEx is set to 1 and one port bit is high go low) is been touched and that the condition is the other port bits are high level. Only input port bits could cause interrupt.

6 System Clock and Oscillator

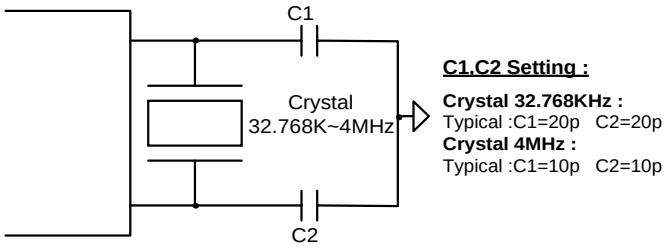
System clock generator produces the basic clock pulses that provide the system clock with CPU and peripherals.

Instruction cycle time

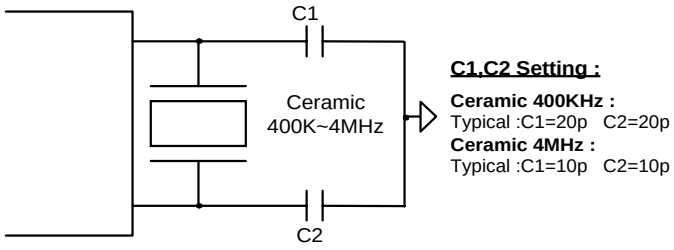
1) 4/32.768KHz (≈122us) for 32.768KHz system clock.
2) 4/4MHz(1us) for 4MHz system clock.

Oscillator

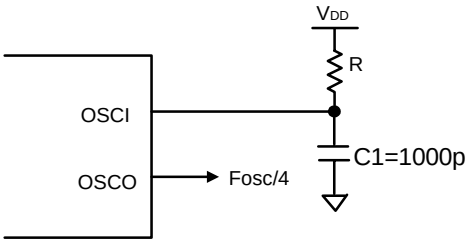
1) Crystal oscillator: 32.768KHz - 4MHz.



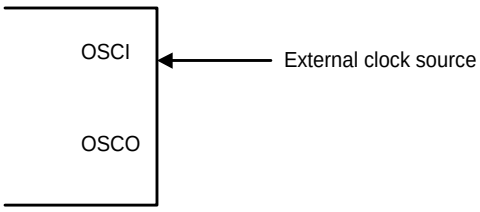
2) Ceramic resonator: 400KHz - 4MHz.



3) RC oscillator: 400KHz - 4MHz.



4) External input clock: 30KHz - 4MHz.



Initial State

Hardware	After power on reset
Program counter	$000
CY	Undefined
Data memory	Undefined
System register	Undefined
AC	Undefined
Pseudo index register	Undefined
DPL,DPM,DPH	Undefined
Table Branch Register	Undefined
Interrupt enable flag register	0
Interrupt request flag register	0
Timer mode register	0
Timer counter	0
Timer load register	0
WDT counter	0
WDT prescaler	0
I/O ports	Input
LPD3~0	1010（Enable LPD）

Instruction Set

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

Arithmetic and Logical Instruction

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X(,B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X(,B)	00000 1bbb xxx xxxx	AC,Mx ← Mx + AC + CY	CY
ADD X(,B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X(,B)	00001 1bbb xxx xxxx	AC,Mx ← Mx + AC	CY
SBC X(,B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X(,B)	00010 1bbb xxx xxxx	AC,Mx ← Mx + -AC + CY	CY
SUB X(,B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X(,B)	00011 1bbb xxx xxxx	AC,Mx ← Mx + -AC +1	CY
EOR X(,B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X(,B)	00100 1bbb xxx xxxx	AC,Mx ← Mx ⊕ AC	
OR X(,B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X(,B)	00101 1bbb xxx xxxx	AC,Mx ← Mx | AC	
AND X(,B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X(,B)	00110 1bbb xxx xxxx	AC,Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3]; AC[0] →CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X,I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X,I	01001 iiii xxx xxxx	AC,Mx ← Mx + I	CY
SBI X,I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X,I	01011 iiii xxx xxxx	AC,Mx ← Mx + -I + 1	CY
EORIM X,I	01100 iiii xxx xxxx	AC,Mx ← Mx ⊕ I	
ORIM X,I	01101 iiii xxx xxxx	AC,Mx ← Mx | I	
ANDIM X,I	01110 iiii xxx xxxx	AC,Mx ← Mx & I	

* In the assembler ASM66 V1.0, EORIM mnemonic is EORI. However, EORI has the same operation identical with EORIM. Same for the ORIM with respect to ORI, and ANDIM with respect to ANDI.

Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC; Mx ← Decimal adjustment for add.	CY
DAS X	11001 1010 xxx xxxx	AC; Mx ← Decimal adjustment for sub.	CY

Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X(,B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X(,B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X,I	01111 iiii xxx xxxx	AC,Mx ← I	

Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC=0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC≠0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY=1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY≠1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC(0)=1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC(1)=1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC(2)=1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC(3)=1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC +1 PC ← X(Not including p)	
RTNW H,L	11010 000h hhh llll	PC ←ST; TBR ← hhhh; AC← llll	
RTNI	11010 1000 000 0000	CY;PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X(Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (A)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page	B	RAM bank. Every $7F as one RAM bank.
ST	Stack	TBR	Table Branch Register

Absolute Maximum Rating*

DC Supple Voltage . . . . . -0.3V to +7.0V

Input Voltage . . . . . -0.3V to V_{DD}+0.3V

Operating Ambient Temperature . . . -10℃ to +60℃

Storage Temperature . . . . . .-55℃ to +125℃

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD}=5.0V GND=0V, T_A=25℃, F_{OSC}=4MHz, unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating voltage	V_{DD}	4.5		6	V	
Operating current	I_{OP}		1	2	mA	All output pins unloaded (Execute NOP instruction).
Stand by current (HALT)	I_{SB1}			0.5	mA	All output pins unloaded.
Stand by current (STOP)	I_{SB2}		1	2	μA	All output pins unloaded, LPD off (If LPD on, I_{SB2X}= I_{SB2}+3uA). WDT off (If WDT on, I_{SB2X}= I_{SB2}+15uA).
Input Low voltage	V_{IL1}	GND		0.2 × V_{DD}	V	I/O ports, pins tri-state.
Input Low voltage	V_{IL2}	GND		0.15 × V_{DD}	V	$\overline{\text{RESET}}$, T0.
Input Low voltage	V_{IL3}	GND		0.15× V_{DD}	V	OSCI (Driven by external clock).
Input High Voltage	V_{IH1}	0.8 × V_{DD}		V_{DD}	V	I/O ports, pins tri-state.
Input High Voltage	V_{IH2}	0.85 × V_{DD}		V_{DD}	V	$\overline{\text{RESET}}$,T0
Input High Voltage	V_{IH3}	0.85 × V_{DD}		V_{DD}	V	OSCI (Driven by external Clock).
Input Leakage Current	I_{IL1}	-1		1	μA	I/O ports, GND < $V_{I/O}$ < V_{DD}
Input Leakage Current	I_{IL2}	-5			μA	$V_{\overline{\text{RESET}}}$ = GND+0.25V
Input Leakage Current	I_{IL3}		1	5	μA	$V_{\overline{\text{RESET}}}$ = V_{DD}
Input Leakage Current	I_{IL4}	-3	1	3	μA	T0, GND < Vt0 < V_{DD}
Input Leakage Current	I_{IL5}	-3	1	3	μA	For OSCI
Output High Voltage	V_{OH}	V_{DD}-0.7			V	I/O ports,I_{OH}=-10mA OSCO$_{RC}$, I_{OH} =-0.7mA
Output Low Voltage	V_{OL}.			GND+0.6	V	I/O ports, I_{OL} =20mA OSCO$_{RC}$, I_{OL} =1.6mA

AC Electrical Characteristics (V_{DD}=5.0V GND=0V, T_A=25℃, unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Oscillator start time	T_{OSC1}			1	s	X'tal osc=32.768KHz
Oscillator start time	T_{OSC2}			20	ms	Ceramic osc=400KHz
Oscillator start time	T_{OSC3}			2	ms	RC Osc=400KHz
Oscillator start time	T_{OSC4}			2	ms	RC Osc=4MHz
WDT period	T_{WDT}	7	18		ms	V_{DD}=5.0V.
Frequency stability(crystal)	Δ F/F			1	ppm	Crystal oscillator: [F(5.0)-F(4.5)]/F(5.0)
Frequency variation(crystal)	Δ F/F			10	ppm	Crystal oscillator: C1=C2=5~30p
Frequency stability(ceramic)	Δ F/F			0.1	%	Ceramic resonator Osc: [F(5.0)-F(4.5)]/F(5.0)
Frequency Variation (RC)	Δ F/F			± 7.5	%	Chip to chip variation
Frequency Stability (RC)	Δ F/F			5	%	RC oscillator: [F(5.0)-F(4.5)]/F(5.0)

User Notice:

Max. Current into V_{DD}=50mA;
Max. Current out of V_{SS}=150mA
Max. Output current sunk by any I/O port=25mA;
Max. Output current sourced by any I/O port=20mA
Max. Output current sunk by all ports (A, B, C, D, E, F)=50mA;
Max. Output current sourced by all ports (A, B, C, D, E, F)=40mA

DC Electrical Characteristics (VDD=3.0V, GND=0V, T_A=25℃, F_{OSC}=4MHz,unless otherwise specified)

Parameter	Symbol	Min.	Typ	Max.	Unit	Condition
Operating voltage	V_{DD}	2.4		4.5	V	
Operating current	I_{OP}		0.7	1.3	mA	All output pins unloaded (Execute NOP instruction).
Stand by current(HALT)	I_{SB1}			0.2	mA	All output pins unloaded.
Stand by current(STOP)	I_{SB2}		1	2	μA	All output pins unloaded, LPD off (If LPD on, I_{SB2X}= I_{SB2}+3uA). WDT off (If WDT on, I_{SB2X}= I_{SB2}+5uA).
Input Low Voltage	V_{IL1}	GND		0.2 ×V_{DD}	V	I/O ports, pins tri-state.
Input Low Voltage	V_{IL2}	GND		0.15 ×V_{DD}	V	$\overline{\text{RESET}}$, T0.
Input Low Voltage	V_{IL3}	GND		0.15 ×V_{DD}	V	OSCI (Driven by external clock).
Input High Voltage	V_{IH1}	0.8 ×V_{DD}		V_{DD}	V	I/O ports, pins tri-state.
Input High Voltage	V_{IH2}	0.85 ×V_{DD}		V_{DD}	V	$\overline{\text{RESET}}$,T0
Input High Voltage	V_{IH3}	0.85 ×V_{DD}		V_{DD}	V	OSCI (Driven by external Clock).
Input Leakage Current	I_{IL1}	-1		1	μA	I/O ports, GND < Vi/o < V_{DD}
Input Leakage Current	I_{IL2}	-5			μA	$V_{\overline{\text{RESET}}}$ = GND+0.25V
Input Leakage Current	I_{IL3}		1	5	μA	$V_{\overline{\text{RESET}}}$ = V_{DD}
Input Leakage Current	I_{IL4}	-3	1	3	μA	T0, GND < Vt0 < V_{DD}
Input Leakage Current	I_{IL5}	-3	1	3	μA	For OSCI
Output High Voltage	V_{OH}	V_{DD}-0.7			V	I/O ports, I_{OH}=-7mA, V_{DD}=3V OSCO$_{RC}$, I_{OH}=-0.7mA, V_{DD}=3V
Output Low Voltage	V_{OL}.			GND+0.4	V	I/O ports, I_{OL}=8mA, V_{DD}=3V OSCO$_{RC}$, I_{OL}=1.0mA, V_{DD}=3V

AC Electrical Characteristics (VDD=3.0V, GND=0V, T_A=25℃, unless otherwise specified)

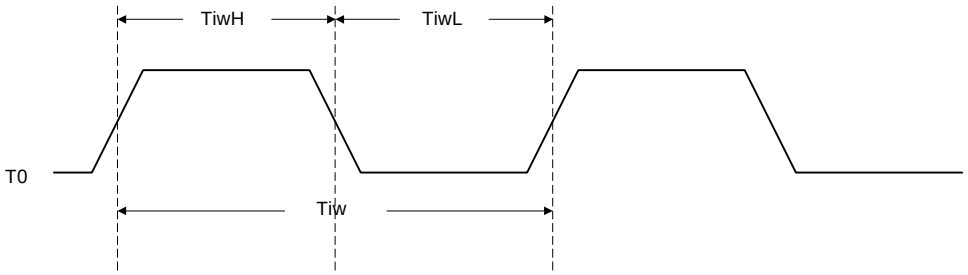
Parameter	Symbol	Min.	Typ	Max.	Unit	Condition
Oscillator start time	T_{OSC1}			1	s	Crystal Osc=32.768KHz, V_{DD}=3.0V.
Oscillator start time	T_{OSC2}			35	ms	Ceramic Osc=400KHz, V_{DD}=3.0V.
Oscillator start time	T_{OSC3}			5	ms	RC Osc=400KHz, V_{DD}=3.0V.
WDT period	T_{WDT}	7	18		ms	V_{DD}=3.0V
Frequency stability(crystal)	Δ F/F			1	PPM	Crystal oscillator: [F(3.0)-F(2.7)]/F(3.0)
Frequency variation(crystal)	Δ F/F			10	PPM	Crystal oscillator: C1=C2=5~30P
Frequency stability(ceramic)	Δ F/F			0.1	%	Ceramic resonator OSC:[F(3.0)-F(2.7)]/F(3.0)
Frequency Variation(RC)	Δ F/F			± 7.5	%	Chip to chip variation
Frequency stability(RC)	Δ F/F			5	%	RC oscillator (1MHz): [F(3.0)-F(2.7)]/F(3.0)

AC Characteristics

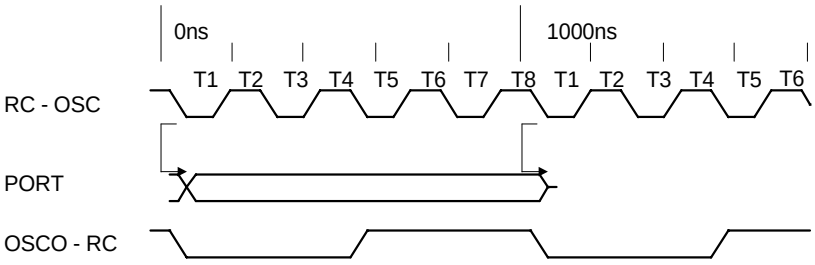
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CY}	Instruction cycle time	1		122	μs	
T_{IW}	T0 input width	$(T_{CY}+40)/N$			ns	N = Prescaler divide ratio.
T_{IWH}	High pulse width	1/2 t_{IW}			ns	
T_{IWL}	LOW pulse width	1/2 t_{IW}			ns	

Timing Waveform

T0 Input Waveform



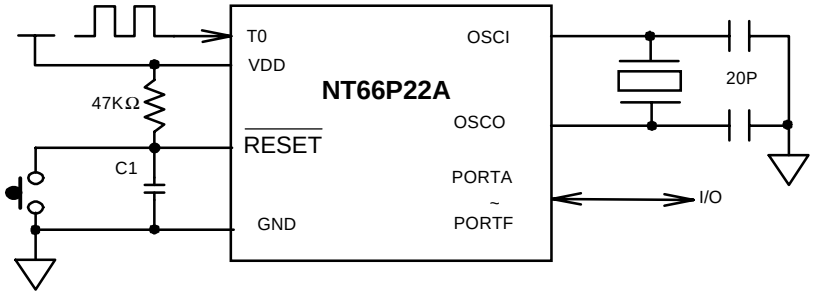
RC OSCO Timing Waveform



Application Circuit (for reference only)

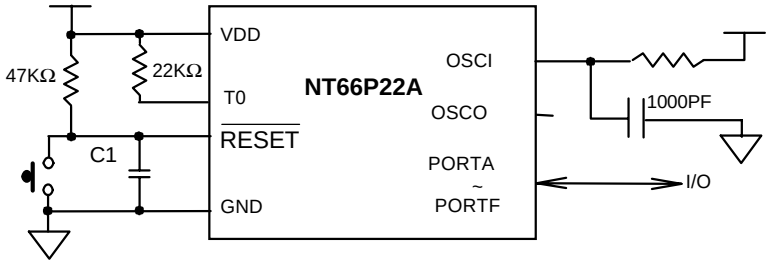
AP1

1) Operating voltage: 5.0V.
2) Oscillator: Ceramic resonator 400KHz.
3) T0 input timer clock / counter
4) PORTA ~ F: I/O



AP2

1) Operating voltage: 5.0V.
2) Oscillator: RC 400KHz.
3) PORTA~E: I/O



AP3

1) PORTA~C: as scan KEY BOARD (32 keys)
2) PORTD~F: I/O