

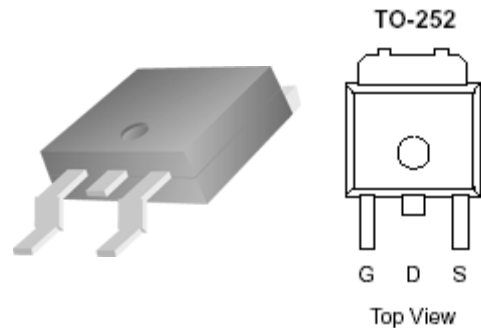
N-Channel 60-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology



PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
60	5.9 @ $V_{GS} = 10V$	76
	6.6 @ $V_{GS} = 4.5V$	72



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_C = 25^\circ\text{C}$	I_D	51	A
Pulsed Drain Current ^b		I_{DM}	100	
Continuous Source Current (Diode Conduction) ^a		I_S	50	A
Power Dissipation ^a	$T_C = 25^\circ\text{C}$	P_D	50	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ\text{C/W}$

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

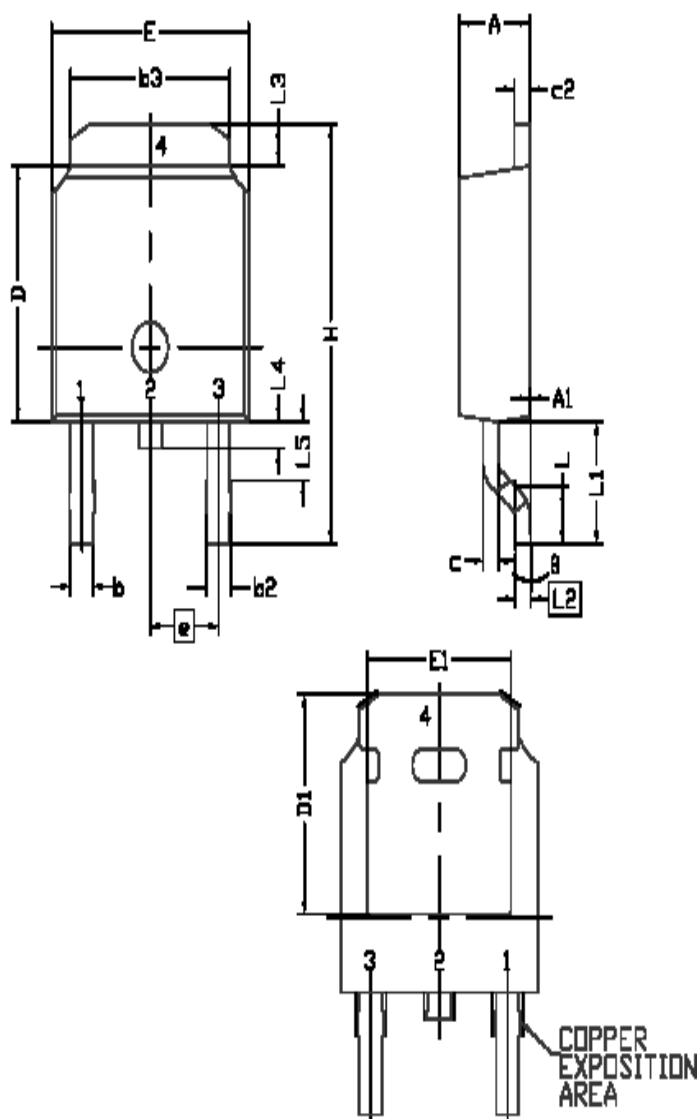
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 uA	1			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 48 V, V _{GS} = 0 V			1	uA
		V _{DS} = 48 V, V _{GS} = 0 V, T _J = 55°C			25	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	34			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 10 V, I _D = 2 A			5.9	mΩ
		V _{GS} = 4.5 V, I _D = 2 A			6.6	
Forward Tranconductance ^A	g _{fs}	V _{DS} = 15 V, I _D = 2 A		22		S
Diode Forward Voltage	V _{SD}	I _S = 2 A, V _{GS} = 0 V		1.1		V
Dynamic ^b						
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 2 A		70		nC
Gate-Source Charge	Q _{gs}			10		
Gate-Drain Charge	Q _{gd}			30		
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, = 1MHz	f	5000		pF
Output Capacitance	C _{oss}			500		
Reverse Transfer Capacitance	C _{rss}			300		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 25 V, R _L = 25 Ω , I _D = 30 A, V _{GEN} = 10 V		10		nS
Rise Time	t _r			20		
Turn-Off Delay Time	t _{d(off)}			200		
Fall-Time	t _f			80		

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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Package Information



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
E	6.40	6.60	6.731
L	1.40	1.52	1.77
L1	2.743 REF		
L2	0.508 BSC		
L3	0.89	—	1.27
L4	0.64	—	1.01
L5	—	—	—
D	6.00	6.10	6.223
H	9.40	10.00	10.40
b	0.64	0.76	0.88
b2	0.77	0.84	1.14
b3	3.21	3.34	5.46
e	2.286 BSC		
A	2.20	2.30	2.38
A1	0	—	0.127
c	0.45	0.50	0.60
c2	0.45	0.50	0.58
D1	5.30	—	—
E1	4.40	—	—
θ	0°	—	10°