
Protection IC for 4~7 Cells Li-ion Battery Pack

FEATURES

- High Accuracy Voltage Detection
 - Over-Voltage Protection
 - V_{OVP} : 3.6V~4.35V (50mV/step)
 - Accuracy: $\pm 25\text{mV}$
 - Hysteresis voltage: 0V or 0.1V to 0.3V in 50mV/step
 - Under-Voltage Protection
 - V_{UVP} : 2.0V~3.0V (100mV/step)
 - Accuracy: $\pm 80\text{mV}$
 - Hysteresis voltage: 0V to 1V in 100mV/step
- 3-Levels Over-Current Detection
 - Level-1 Over-Current Protection:
 - V_{OCP1} : 25mV~350mV (25mV/step)
 - Accuracy: $\pm 10\text{mV}$
 - Level-2 Over-Current Protection:
 - $V_{OCP2}=3 \times V_{OCP1}$
 - Accuracy: $\pm 30\text{mV}$
 - Short-Circuit Protection
 - $V_{SCP}=5 \times V_{OCP1}$
 - Accuracy: $\pm 50\text{mV}$
- OC/SC release conditions:
 - Charger-Connected **OR**
 - Load-Opened
- Built-in Over-Temperature Protection
- Built-in Under-Temperature Protection
- Delay times are set by external capacitors
- Switchable between 4-series to 7-series cell using the SEL1 and SEL2 pin
- Low-power Operating States:
 - Normal State: $< 35\mu\text{A}$
 - Power-down state: $< 1\mu\text{A}$
 - Hardware Shut-down state: $< 0.1\mu\text{A}$
- 24-Lead TSSOP Package

GENERAL DESCRIPTION

The FD881C is a protection IC which includes high-accuracy voltage detector and current detector to provide Over-Voltage (OV), Under-Voltage (UV), Over-Current (OC), Short-Circuit (SC), Over-Temperature (OT), Under-Temperature (UT) protection for 4-series to 7-series Li-ion/polymer battery pack used in power-tools, notebook PC applications etc. By cascade connection using this IC, it is also possible to protect 8-series or more cells Li-ion/polymer battery pack.

The FD881C provides CCTL and DCTL pins to control charging and discharging FET. It is possible for users to control the output voltages from the CFET pin and DFET pin independently.

The FD881C integrates MOSFET driver. The FD881C can drive the N-type charge FET and N-type discharge FET at the PACK- side directly.

The FD881C consumes less than 35uA in normal status from VCC, and it reduces to less than 1uA in Power-down state. Furthermore, the FD881C can be powered from a switched supply, providing a technique to reduce battery stack current draw to zero. This device is packaged in a 24-pin TSSOP package.

APPLICATIONS

- Power-Tools
- E-Bikes/E-Scooters/E-Motors
- Notebook PC/Tablet PC
- UPS Backup Battery Systems

PRODUCT ORDING INFORMATION

■ Product Name

FD881C XX XX

Package abbreviation
F: 24-pin TSSOP

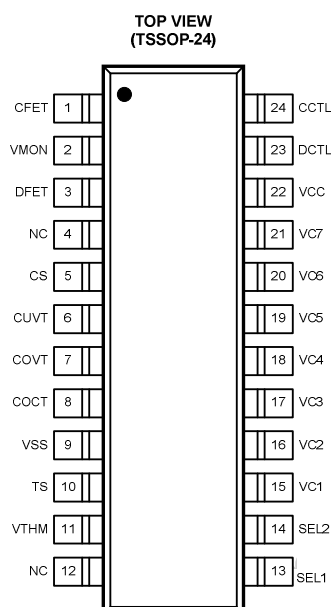
Additional number
Sequentially set from AA to ZZ

■ Product Name List

Product Name	OV Protection Voltage V_{OVP}	OV Release Voltage V_{OVR}	UV Protection Voltage V_{UVP}	UV Release Voltage V_{UVR}	Level-1 DOC Protection Voltage V_{DOCP1}	Power- down Function
FD881C AAF	4.25 $\pm 0.025V$	4.15 $\pm 0.025V$	2.7 $\pm 0.08V$	3.0 $\pm 0.08V$	0.1 $\pm 0.01V$	Yes
FD881C ABF	4.20 $\pm 0.025V$	4.10 $\pm 0.025V$	2.5 $\pm 0.08V$	3.0 $\pm 0.08V$	0.1 $\pm 0.01V$	Yes
FD881C ACF	4.20 $\pm 0.025V$	4.20 $\pm 0.025V$	2.5 $\pm 0.08V$	2.9 $\pm 0.08V$	0.1 $\pm 0.01V$	Yes
FD881C ADF	3.75 $\pm 0.025V$	3.55 $\pm 0.025V$	2.2 $\pm 0.08V$	2.7 $\pm 0.08V$	0.1 $\pm 0.01V$	Yes
FD881C AEF	3.85 $\pm 0.025V$	3.55 $\pm 0.025V$	2.2 $\pm 0.08V$	2.7 $\pm 0.08V$	0.1 $\pm 0.01V$	Yes
FD881C AFF	3.65 $\pm 0.025V$	3.65 $\pm 0.025V$	2.2 $\pm 0.08V$	2.7 $\pm 0.08V$	0.1 $\pm 0.01V$	Yes
FD881C AGF	4.25 $\pm 0.025V$	4.15 $\pm 0.025V$	2.7 $\pm 0.08V$	3.0 $\pm 0.08V$	0.1 $\pm 0.01V$	No
FD881C AHF	4.20 $\pm 0.025V$	4.10 $\pm 0.025V$	2.5 $\pm 0.08V$	3.0 $\pm 0.08V$	0.1 $\pm 0.01V$	No

Note: if a product with the required detection voltage does not appear in the above list, contact our sales office.

PIN CONFIGURATION



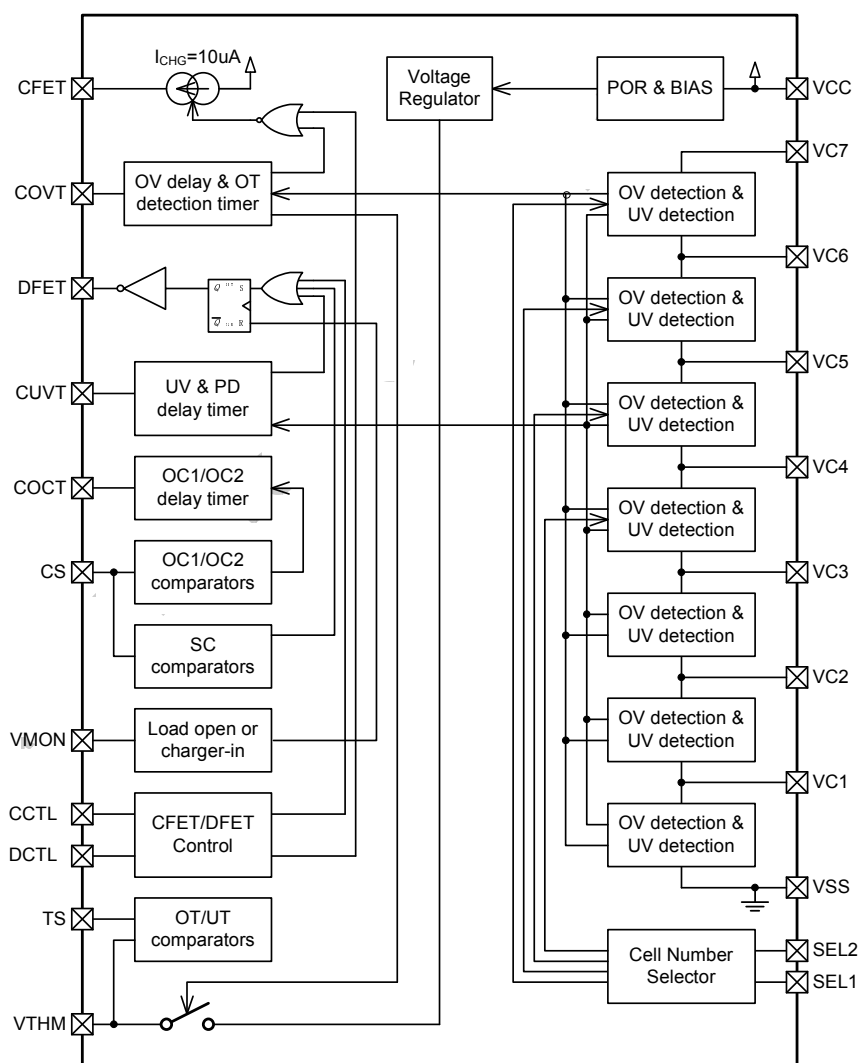
PIN DESCRIPTION

PIN	NAME	PIN DESCRIPTION															
1	CFET	Charge power FET control pin															
2	VMON	Voltage Monitor input pin to detect if the load is opened after over-current (OC) or short-circuit (SC) occurs															
3	DFET	Discharge power FET control pin															
4	NC	Not Connected															
5	CS	Connection pin for current sensing resistor															
6	CUVT	Capacitor connection pin for under-voltage detection timer															
7	COVT	Capacitor connection pin for over-voltage detection timer															
8	COCT	Capacitor connection pin for over-current detection timer															
9	VSS	Ground pin															
10	TS	Connection pin for thermistor															
11	VTHM	External Thermistor bias output pin. This is a switched connection for supplying a bias voltage from the internal voltage regulator to an external resistor network composed of resistor and an external NTC resistor for measuring the temperature of the battery module.															
12	NC	Not Connected															
13	SEL1	Pin for switching 4-series or 5-series cell or 6-series cell or 7-series cell. Do not leave SEL1/2 floating.															
14	SEL2	<table><tr><th>SEL2</th><th>SEL1</th><th>FUNCTION</th></tr><tr><td>V_{CC}</td><td>V_{CC}</td><td>7-series cell</td></tr><tr><td>V_{CC}</td><td>V_{SS}</td><td>6-series cell</td></tr><tr><td>V_{SS}</td><td>V_{CC}</td><td>5-series cell</td></tr><tr><td>V_{SS}</td><td>V_{SS}</td><td>4-series cell</td></tr></table>	SEL2	SEL1	FUNCTION	V _{CC}	V _{CC}	7-series cell	V _{CC}	V _{SS}	6-series cell	V _{SS}	V _{CC}	5-series cell	V _{SS}	V _{SS}	4-series cell
SEL2	SEL1	FUNCTION															
V _{CC}	V _{CC}	7-series cell															
V _{CC}	V _{SS}	6-series cell															
V _{SS}	V _{CC}	5-series cell															
V _{SS}	V _{SS}	4-series cell															

PIN DESCRIPTION (CONT.)

PIN	NAME	PIN DESCRIPTION
15	VC1	Connection for positive voltage of cell 1
16	VC2	Connection for positive voltage of cell 2
17	VC3	Connection for positive voltage of cell 3
18	VC4	Connection for positive voltage of cell 4
19	VC5	Connection for positive voltage of cell 5
20	VC6	Connection for positive voltage of cell 6
21	VC7	Connection for positive voltage of cell 7
22	VCC	Power supply pin. Connection for positive voltage of cell 5.
23	DCTL	Control pin for discharge FET
24	CCTL	Control pin for charge FET

BLOCK DIAGRAM



TYPICAL APPLICATION DIAGRAM

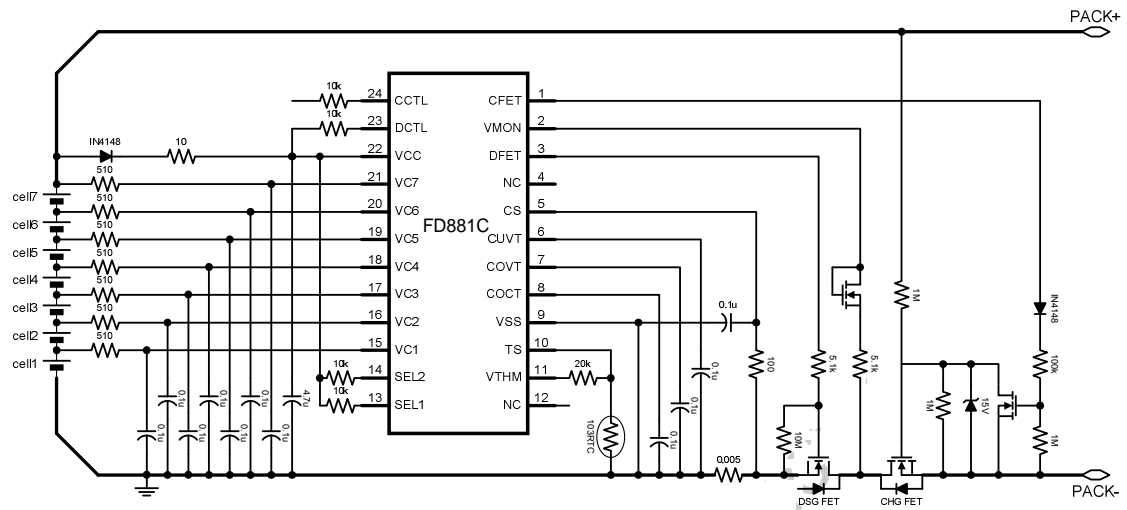


Figure 1, Typical Application Diagram for 7-series cell with N-type Charge FET & Discharge-FET

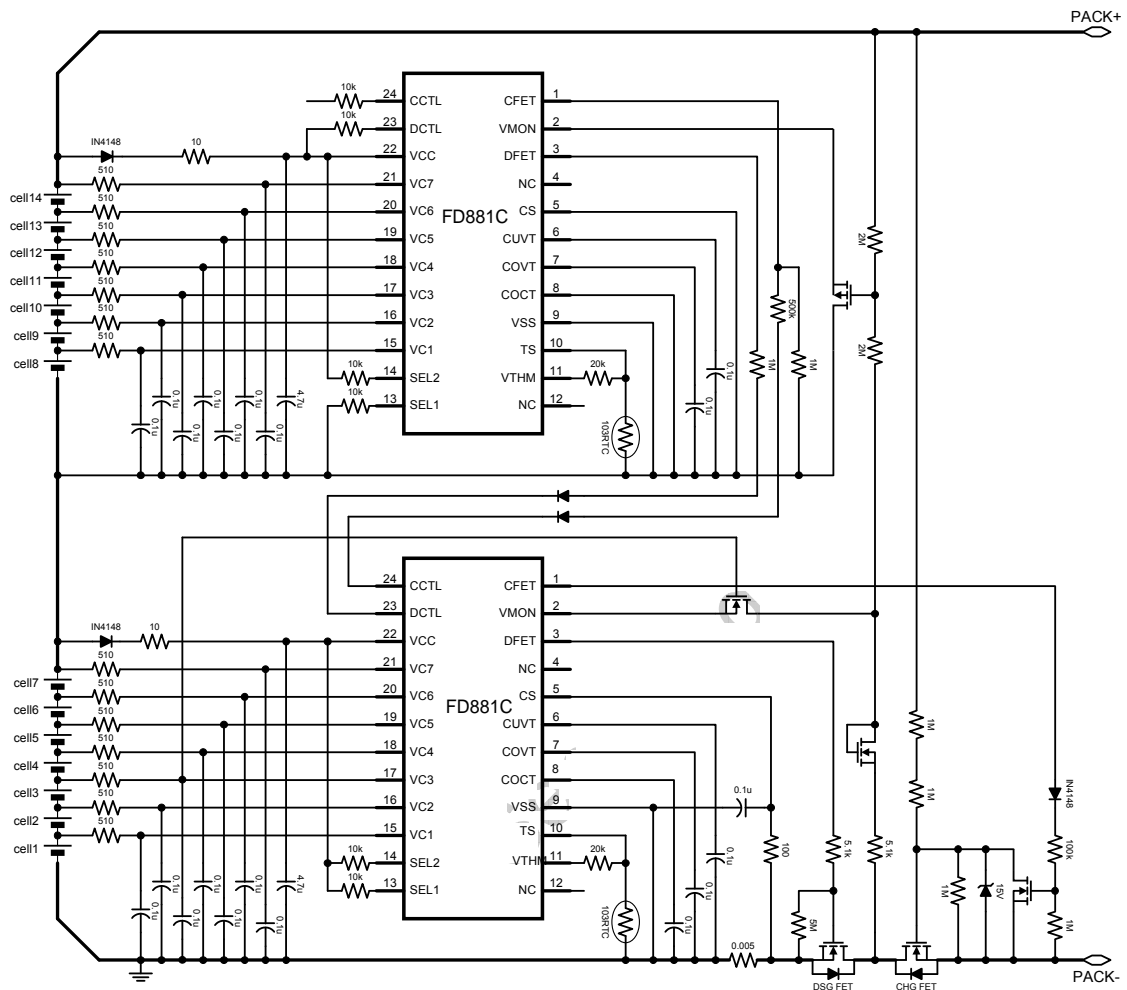


Figure 2, Typical Application Diagram for 13-series cell with N-type Charge FET & Discharge-FET

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)

PARAMETER	SYMBOL	APPLICABLE PIN	RATING
Input Voltage between VCC and VSS	V _{CC}	VCC	V _{SS} -0.3V to V _{SS} +35V
Low-Voltage Input pin voltage	V _{IN_LV}	CS, CUVT, COVT, COCT, TS, VTHM	V _{SS} -0.3V to V _{SS} +5.5V
High-voltage Input pin voltage	V _{IN_HV}	SEL1, SEL2, CCTL, DCTL	V _{SS} -0.3V to V _{SS} +35V
Rail-to-rail Input pin voltage	V _{IN_R2R}	VMON	V _{SS} -0.3V to V _{CC} +0.3V
Cell voltage input voltage: VC(n) to VC(n-1), n=2 to 7; VC1 to VSS	V _{CELL}	VC7, VC6, VC5, VC4, VC3, VC2, VC1	-0.3V to +7.0V
CFET pin output voltage	V _{CFET}	CFET	V _{CC} -35V to V _{CC} +0.3V
DFET pin output voltage	V _{DFET}	DFET	0.3V to +15V
HBM ESD rating			±2kV
Operating free-air temperature range	T _A		40°C to +85°C
Storage temperature range	T _{STG}		-40°C to +125°C
Package thermal resistance (TSSOP20)	θ _{JA}		48.7°C/W

Note 1: Human Body Model (HBM) to Specification MIL-STD-883 Method 3015.7

Note 2: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = +25°C, unless otherwise specified

Parameter	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Over-Voltage (OV) and Under-Voltage (UV) Protection						
Over-Voltage Protection Threshold	V _{OV} P	3.6V to 4.35V in 50mV/step	V _{OV} P -25	V _{OV} P	V _{OV} P +25	mV
Over-Voltage Release Hysteresis Voltage	V _{OV} P_HYS		0V or 0.1 to 0.3V in 50mV/step			mV
Over-Voltage Release Threshold	V _{OV} R	V _{OV} R = V _{OV} P - V _{OV} P_HYS	V _{OV} R -25	V _{OV} R	V _{OV} R +25	mV
Under-Voltage Protection Threshold	V _{UV} P	2.0V to 3.0V in 100mV/step	V _{UV} P -80	V _{UV} P	V _{UV} P +80	mV
Under-Voltage Release Hysteresis Voltage	V _{UV} P_HYS		0 to 1.0V in 100mV/step			mV
Under-Voltage Release Threshold	V _{UV} R	V _{UV} R = V _{UV} P + V _{UV} P_HYS	V _{OV} R -80	V _{OV} R	V _{OV} R +80	mV
Cell-Balance (CB) Protection						
Cell-Balance Protection Threshold	V _{CB}	3.55V to 4.30V in 50mV/step	V _{CB} -25	V _{CB}	V _{CB} +25	mV
Discharge Over-Current (DOC) and Short-Circuit (SC) and Charge Over-Current (COC) Protection						
Level-1 Discharge Over-Current Protection Threshold	V _{DO} CP1	50mV to 350mV in 25mV/step	V _{DO} CP1 -10	V _{DO} CP1	V _{DO} CP1 +10	mV
Level-2 Discharge Over-Current Protection Threshold	V _{DO} CP2	V _{DO} CP2=3*V _{DO} CP1	V _{DO} CP2 -30	V _{DO} CP2	V _{DO} CP2 +30	mV
Short-Circuit Protection Threshold	V _{SCP}	V _{SCP} =5*V _{DO} CP1	V _{SCP} -50	V _{SCP}	V _{SCP} +50	mV
Discharge state detection voltage	V _{IN_DSG}	V _{CS} >V _{IN_DSG} , it is considered as discharge state; otherwise, it is considered as charge state.	2.5	4	6	mV
Discharge Over-Temperature (DOT) and Charge Over-Temperature (COT) Protection						
Discharge Over-Temperature Protection Threshold	T _{DO} TP		T _{DO} TP -5	T _{DO} TP	T _{DO} TP +5	°C
Discharge Over-Temperature Release Hysteresis	T _{DO} TP_HYS			15		°C
Discharge Over-Temperature Release Threshold	T _{DO} TR	T _{DO} TR = T _{DO} TP - T _{DO} TP_HYS	T _{DO} TP -5	T _{DO} TP	T _{DO} TP +5	°C
Charge Over-Temperature Protection Threshold	T _{CO} TP		T _{CO} TP -5	T _{CO} TP	T _{CO} TP +5	°C
Charge Over-Temperature Release Hysteresis	T _{CO} TP_HYS			5		°C
Charge Over-Temperature Release Threshold	T _{CO} TR	T _{CO} TR = T _{CO} TP - T _{CO} TP_HYS	T _{CO} TP -5	T _{CO} TP	T _{CO} TP +5	°C

ELECTRICAL CHARACTERISTICS (CONT.)

T_A = +25°C, unless otherwise specified

Parameter	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Discharge Over-Temperature (DOT) and Charge Over-Temperature (COT) Protection						
Charge Under-Temperature Protection Threshold	T _{CUTP}		T _{CUTP} -5	T _{CUTP}	T _{CUTP} +5	°C
Charge Under-Temperature Release Hysteresis	T _{CUTP_HYS}			5		°C
Charge Under-Temperature Release Threshold	T _{CUTR}	T _{CUTR} = T _{CUTP} + T _{CUTP_HYS}	T _{CUTR} -5	T _{CUTR}	T _{CUTR} +5	°C
External Programmable Protection Delay and Release Delay Time						
Over-Voltage Protection Delay time	t _{OVP}	C _{COVT} =0.1uF	0.7	1.0	1.3	S
Under-Voltage Protection Delay time	t _{UVP}	C _{CUVT} =0.1uF	0.7	1.0	1.3	S
Under-Voltage Power-down Delay time	t _{UV_PD}	C _{CUVT} =0.1uF	3.5	5.5	7.5	S
Level-1 Discharge Over-Current Protection Delay time	t _{DOCP1}	C _{COCT} =0.1uF	0.7	1.0	1.3	S
Level-2 Discharge Over-Current Protection Delay time	t _{DOCP2}	C _{COCT} =0.1uF	0.07	0.1	0.13	S
Short-Circuit Protection Delay time	t _{SCP}	Internal fixed delay time, No RC filter in front of CS pin	100	250	500	μS
Temperature detection period time	t _{TDET}	C _{COVT} =0.1uF	0.5	1.0	1.5	S
POWER SUPPLY (VCC)						
Input voltage Range	V _{CC}		4.0		35	V
Supply Current	I _{VCC NOR}	Normal state, V _{CELL} =3.5V		45	55	μA
	I _{VCC PD}	Power-down state, V _{CELL} =1.8V		0.6	1.0	μA
Power-On-Reset Voltage	V _{POR}			4.8	6.0	V
Voltage regulator for discharge driver	V _{VREGH}	V _{CC} >V _{VREGH} +1V	9.0	10.5	12	V
		V _{CC} <V _{VREGH} +1V	V _{CC} -1.5	V _{CC} -1	V _{CC} -0.5	V
CELL INPUTS (VC7, VC6, VC5, VC4, VC3, VC2, VC1)						
VC7 sink current in normal state	I _{VC7}	V _{CELL} =3.5V		14.0	18.0	μA
VC(n) sink current in normal state, n=1 to 4	I _{VCX}	V _{CELL} =3.5V	-0.3		+0.3	μA
INPUT VOLTAGE (SEL1, SEL2, CCTL, DCTL)						
SEL1, SEL2 input voltage, High	V _{SELH}		V _{CC} -2.5			V
SEL1, SEL2 input voltage, Low	V _{SELL}				1.5	V
CCTL, DCTL input voltage, High	V _{CTRLH}		V _{CC} -1.0			V
CCTL, DCTL input voltage, Low	V _{CTRLL}				1.5	V

ELECTRICAL CHARACTERISTICS (CONT.)

T_A = +25°C, unless otherwise specified

Parameter	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DRIVER CIRCUIT (CFET, DFET)						
CFET pin source current	I _{CFET}	V _{CELL} =3.5V, V _{CFET} =V _{CC} -1V		Hi-Z		μA
		V _{CELL} =V _{OVP} +0.2V & V _{CFET} =V _{CC} -1V or V _{CELL} =3.5V, V _{CCTL} =V _{CC}	7.0	10.0	13.0	μA
DFET pin output voltage	V _{DFETH}	V _{CELL} =3.5V, V _{CS} =0V		= V _{VREGH}		V
	V _{DFETL}	V _{CELL} =3.5V, V _{CS} ≥V _{DOCP1}			0.4	V

FUNCTIONAL DESCRIPTION

Normal Status

When all of the battery voltages are in the range from V_{OVP} and V_{UVP}, the discharge current is lower than the specified value (the CS pin voltage is lower than V_{DOCP1}), the charge temperature is lower than T_{COTP}, and the discharge temperature is lower than T_{DOTP}, the FD881C works in normal status, the charging and discharging FETs are turned on.

Over-Voltage (OV) Status

When any one of the battery voltages becomes higher than V_{OVP} and the state continues for t_{OVP} or longer, the CFET pin becomes to source 10uA current, refer to figure 1/2/3, the source side and gate side of charging FET is shorted together, thus the charging FET is turned off to stop charging. This is called the over-voltage status. In over-voltage status, if a load is connected and the CS pin voltage is higher than discharging detection voltage V_{IN_DSG}, the FD881C will turn on charging FET immediately to avoid the over-heat of charging FET due to its body diode conduction. Before the over-voltage status is released, if the load is removed, the charging FET will be turned off again. The over-voltage status is released only when all battery voltages become V_{OVR} or lower.

Under-Voltage (UV) Status

When any one of the battery voltages becomes lower than V_{UVP} and the state continues for t_{UVP} or longer, the DFET pin voltage becomes V_{SS} level, and the discharging FET is turned off to stop discharging. This is called the under-voltage status. The under-voltage status is released when both of the following two conditions hold:

- All battery voltages become V_{UVR} and higher
- The VMON pin voltage is lower than 1.0V (Load is removed or charger is connected)

Power-Down (PD) Status

In under-voltage status, when the state continues for t_{UV_PD} or longer, the FD881C enters the power-down status (optional). In power-down status, the VMON pin voltage is pulled up to V_{CC} level by the internal pull-up resistor. In power-down status, almost all the circuits of the FD881C stop and the current consumption is I_{VCC_PD} or lower. The conditions of each output pin are listed as following:

- CFET pin: Hi-Z
- DFET pin: V_{SS}

The power-down status is released when the following condition holds:

- The VMON pin voltage is V_{CC}-3V (typ.) or lower (A charger is connected)

Over-Current (OC) Status

The FD881C has three over-current detection levels (V_{DOCP1}, V_{DOCP2} and V_{SCP}) and three over-current detection delay times (t_{DOCP1}, t_{DOCP2}, and t_{SCP}) corresponding to each over-current detection level. When the discharging current becomes higher than the specified value (the voltage on CS pin is greater than V_{DOCP1}) and the state continues for t_{DOCP1} or longer, the FD881C enters over-current status, in which the DFET pin voltage becomes V_{SS} level to turn off the discharging FET to stop discharging. Operation of over-current detection level-2 (V_{DOCP2}) and over-current detection delay time 2 (t_{DOCP2}) is the same as for V_{DOCP1} and t_{DOCP1}.

In over-current status, discharging FET is turned off, thus the VMON pin is pulled up to V_{CC} level by the load. The over-current status is released when the following conditions hold:

- The VMON pin voltage is lower than 1.0V (a charger is connected or the load is removed)

Over-Temperature (OT) or Under-Temperature Status

When the CS pin voltage is bigger than V_{IN_DSG} , the battery pack is regarded as in discharging status. Otherwise, the battery pack is regarded as in charging status.

In normal status, the FD881C will do the temperature detection every t_{TDET} , see figure 3 for temperature detection timing chart.

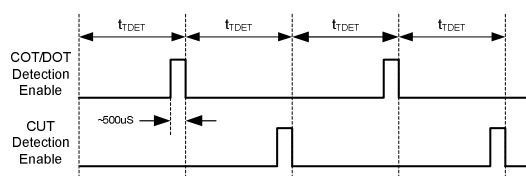


Figure 3, temperature detection timing

When the battery pack temperature becomes higher than T_{DOTP} in discharging status and the state continues for $4 \times t_{TDET}$ or longer, the DFET pin voltage becomes V_{SS} level and the CFET pin becomes to source 10uA current, both the charging and discharging FETs are turned off to stop charging and discharging. This is called the discharging over-temperature status. The discharging over-temperature status is released when both of the following two conditions hold:

- The battery pack temperature becomes T_{DOTR} or lower.
- The VMON pin voltage is lower than 1.0V (Load is removed or charger is connected)

When the battery pack temperature becomes higher than T_{COTP} in charging status and the state continues for $4 \times t_{TDET}$ or longer, the CFET pin becomes to source 10uA current, the charging FET is turned off to stop charging. This is called the charging over-temperature status. In charging over-temperature status, if a load is connected and the CS pin voltage is higher than discharging detection voltage V_{IN_DSG} , the FD881C will turn on charging FET immediately to avoid the over-heat of charging FET due to its body diode conduction. Before the charging over-temperature status is released, if the load is removed, the charging FET will be turned

off again. The charging over-temperature status is released only when the battery pack temperature becomes T_{COTR} or lower.

When the battery pack temperature becomes lower than T_{CUTP} in charging status and the state continues for $4 \times t_{TDET}$ or longer, the CFET pin becomes to source 10uA current, the charging FET is turned off to stop charging. This is called the charging under-temperature status. In charging under-temperature status, if a load is connected and the CS pin voltage is higher than discharging detection voltage V_{IN_DSG} , the FD881C will turn on charging FET immediately to avoid the over-heat of charging FET due to its body diode conduction. Before the charging under-temperature status is released, if the load is removed, the charging FET will be turned off again. The charging under-temperature status is released only when the battery pack temperature becomes T_{CUTR} or higher.

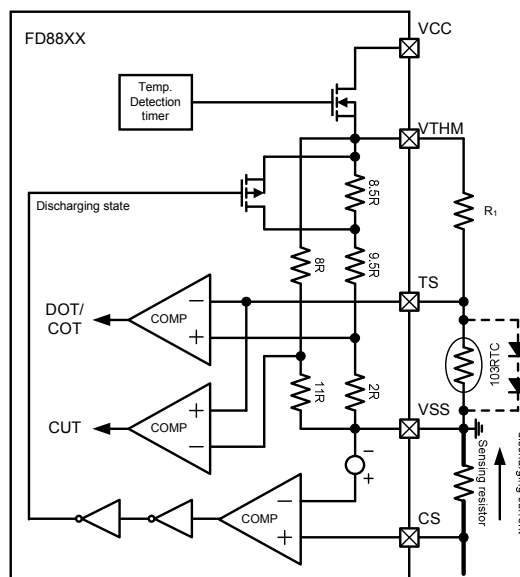


Figure 4, external temperature-sensing circuit

An example of external temperature-sensing circuit is shown in figure 4. In normal status, the FD881C continuously turns on VTHM output for 500uS every t_{TDET} . In this way, the external temperature is monitored. When the VTHM output turns on, the FD881C compares the external temperature voltage with two internal voltage dividers that are set to $1/10 \times V_{THM}$ (discharging state) or $2/11.5 \times V_{THM}$ (charging state). When the thermistor voltage is lower than $1/10 \times V_{THM}$ (discharging state) or $2/11.5 \times V_{THM}$ (charging state), the discharging over-temperature or charging over-temperature condition exists. When the thermistor voltage is bigger than $11/19 \times V_{THM}$, the charging under-

temperature condition exists. To set the external over-temperature limit, set the value of R_1 resistor to the 9 times the resistance of the thermistor at the discharging over-temperature threshold. For example, for 103-type NTC thermistor, set the R_1 to be 20k will set the DOT, COT and CUT thresholds to be 70°C, 50°C and 0°C. Set the R_1 to be 23k will set the DOT, COT and CUT thresholds to be 65°C, 45°C and -3°C.

Using a 10k resistor in place of thermistor will cause COT, DOT and CUT never occurs. Parallel the thermistor with two diodes (e.g. 1N4148) will cause CUT never occurs as shows in figure 4.

Delay time setting

The over-voltage protection delay time (t_{OVP}), temperature detection period time (t_{TDET}) are determined by the external capacitor connected to COVT pin. The under-voltage protection delay time (t_{UVP}), the under-voltage power-down delay time (t_{UV_PD}) are determined by the external capacitor connected to CUVT pin. Level-1 and Level-2 over-current protection delay time (t_{DOCP1} and t_{DOCP2}) are determined by the external capacitor connected to COCT pin. Short-Circuit detection delay time (t_{SCP}) is fixed internally to be 250uS (typical).

	Min.	Typ.	Max.
t_{OVP} [s] =	(7.00, 10.0, 13.0)	$\times C_{COVT}$ [uF]	
t_{TDET} [s] =	(5.00, 10.0, 15.0)	$\times C_{COVT}$ [uF]	
t_{UVP} [s] =	(7.00, 10.0, 13.0)	$\times C_{CUVT}$ [uF]	
t_{UV_PD} [s] =	(35.0, 55.0, 75.0)	$\times C_{CUVT}$ [uF]	
t_{DOCP1} [s] =	(7.00, 10.0, 13.0)	$\times C_{COCT}$ [uF]	
t_{DOCP2} [s] =	(0.70, 1.00, 1.30)	$\times C_{COCT}$ [uF]	

CCTL and DCTL pins

The FD881C has two control pins. The CCTL pin is used to control the CFET output voltage, while the DCTL is used to control DFET pin output voltage. Thus, it is possible for users to control the output voltages from the CFET pin and DFET pin independently. These control pins take precedence over the battery protection circuit.

Table 1, conditions set by CCTL pin

CCTL pin	CFET pin
High	Source 10uA
Open	Normal status* ¹
Low	Normal status* ¹

*1. The status is controlled by the voltage detector

Table 2, conditions set by DCTL pin

DCTL pin	DFET pin
High	Normal status* ¹
Open	V_{SS} level
Low	V_{SS} level

*1. The status is controlled by the voltage detector

SEL1 and SEL2 pin

The SEL1 and SEL2 pin are used to switch between 4-cell or 5-cell or 6-cell or 7-cell protection. The SEL1 and SEL2 pins take precedence over the battery protection circuit. Use the SEL1 and SEL2 pins at high level or low level, do not leave SEL1 and SEL2 floating.

Table 3, conditions set by SEL pin.

SEL2 pin	SEL1 pin	Condition
High	High	7-cell protection
High	Low	6-cell protection
Low	High	5-cell protection
Low	Low	4-cell protection

0V Battery Charge Function

The FD881C provides 0V battery charge function.

Hardware Shutdown

To completely shut down the FD881C, a PMOS switch can be connected to VCC, or VCC can be driven from an isolated power supply. Figure 5 shows an example of a switched VCC. If the switch is open, no current will flow through the stacked NPN transistor (i.e. MMBTA42s) and the 4.3M and 5.6M resistor, TP0610K will be completely shut off to reduce total supply current of FD881C to less than 1nA. If the switch is on, TP0610K will be turned on.

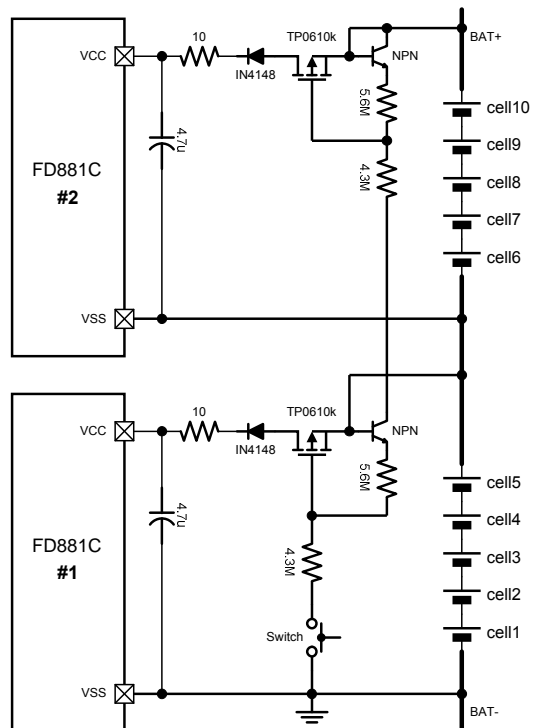


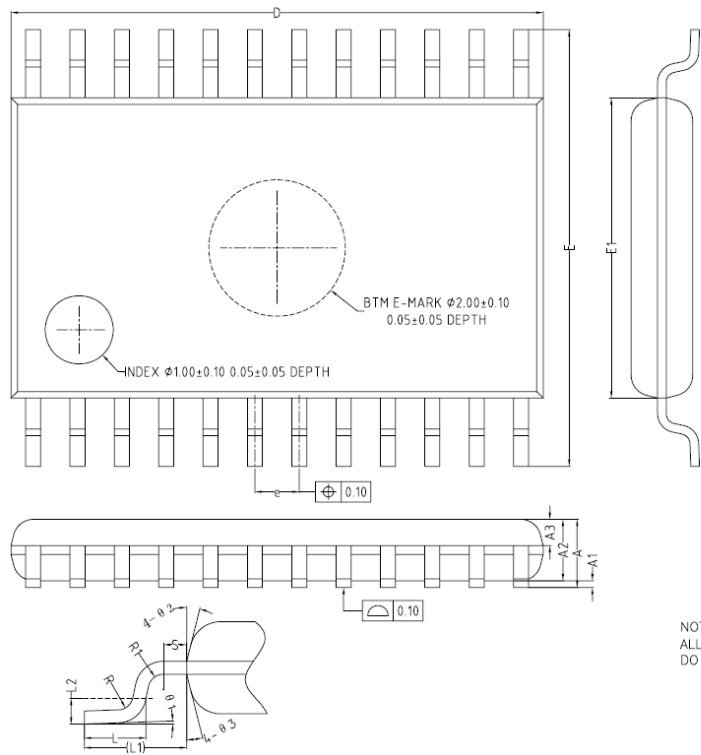
Figure 5, Hardware shutdown circuit

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	June/20/2013	Initial Release	--
1	Aug/12/2013	Second Release	--
2	April/10/2014	Add OT/UT protection	

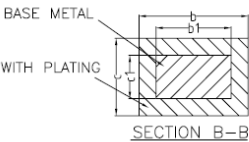
PACKAGE INFORMATION

24-Lead TSSOP Package Outline Diagram



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	0.90	1.00
A3	0.34	0.39	0.44
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.10	—	0.19
c1	0.10	0.13	0.15
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R	0.09	—	—
R1	0.09	—	—
S	0.20	—	—
θ_1	0°	—	8°
θ_2	12°	14°	16°
θ_3	12°	14°	16°



NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO-153 AD
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.