2 keys Touch Pad Detector IC

Outline

- The TTP224B-RO8N TonTouch™ IC is capacitive sensing design specifically for touch pad controls. The device built in regulator for touch sensor. Stable sensing method can cover diversity conditions. Human interfaces control panel links through non-conductive dielectric material. The main application is focused at replacing of the mechanical switch or button. The ASSP can independently handle the 2 touch pads with 2 direct output pins

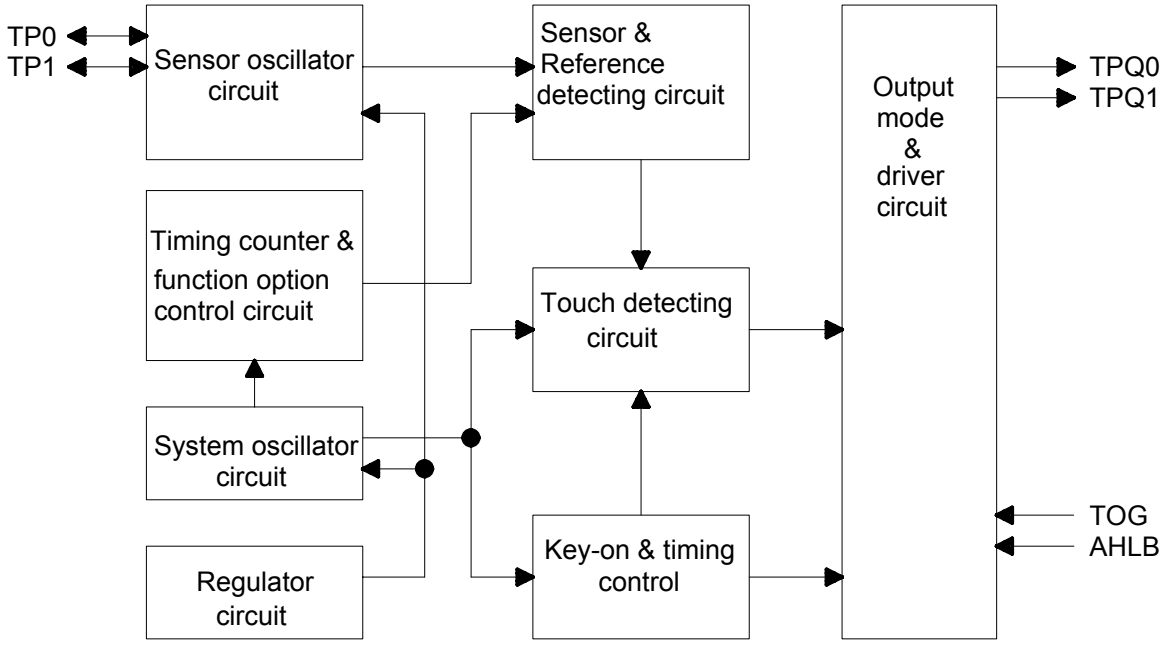
Characteristic

- Operating voltage 2.4V ~ 5.5V
- Built-in regulator
- Operating current, @VDD=3V no load
  At low power mode typical 2.5uA, At fast mode typical 13uA
- @VDD=3V operating voltage :
  The response time about 160mS at low power mode, 60mS at fast mode
- Sensitivity can adjust by the capacitance（1~50pF）outside for each touch pad
- Provides direct mode or toggle mode active high or active low by pad option (TOG/AHLB pin)
- After power-on have about 0.5sec stable-time, during the time do not touch the key pad, and the function is disabled
- Auto calibration for life
- The re-calibration period is about 1 sec within 8 sec after power-on. When key has been touched within 8 sec or key has not been touched more than 8 sec after power-on, then the re-calibration period change to 4 sec

Applications

- Wide consumer products
- Button key replacement

Block diagram



Pin Description

Pin NO	Pin Name	Type	Pad Description
1	TP0	I/O	Touch pad input pin
2	TP1	I/O	Touch pad input pin
3	AHLB	I-PL	Output active high or low option, default: 0
4	VDD	P	Positive power supply
5	TOG	I-PL	Output type option, default: 0
6	VSS	P	Negative power supply, ground
7	TPQ1	O	Direct output for TP1 touch input pin
8	TPQ0	O	Direct output for TP0 touch input pin

Pin Type

- I CMOS input only
- O CMOS push-pull output
- I／O CMOS I／O
- P Power／Ground
- I-PH CMOS input and pull-high resister
- I-PL CMOS input and pull-low resister
- OD Open drain output, have no Diode protective circuit

Electrical Characteristics

- **Absolute maximum ratings**

Parameter	Symbol	Conditions	Rating	Unit
Operating Temperature	T_{OP}	—	-40～+85	℃
Storage Temperature	T_{STG}	—	-50～+125	℃
Supply Voltage	VDD	Ta=25°C	VSS-0.3～VSS+5.5	V
Input Voltage	V_{IN}	Ta=25°C	VSS-0.3～VDD+0.3	V
Human Body Mode	ESD	—	5	KV
Note：VSS symbolizes for system ground				

- **DC / AC characteristics：（Test condition at room temperature = 25 ℃）**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	Internal regulator enable	2.4		5.5	V
Internal Regulator Output	VREG		2.2	2.3	2.4	V
Operating Current	I_{OPL}	VDD=3V, At low power mode(regulator enable)		2.5		uA
	I_{OPF}	VDD=3V, At fast mode (regulator enable)		13.0		uA
Input Ports	V_{IL}	Input Low Voltage	0		0.2	VDD
Input Ports	V_{IH}	Input High Voltage	0.8		1.0	VDD
Output Port Sink Current	I_{OL}	VDD=3V, V_{OL}=0.6V		8		mA
Output Port Source Current	I_{OH}	VDD=3V, V_{OH}=2.4V		-4		mA
Input Pin Pull-high Resistor	R_{PH}	VDD=3V		30K		ohm
Input Pin Pull-low Resistor	R_{PL}	VDD=3V		25K		ohm
Output Response Time	T_R	VDD=3V、At fast mode		60		mS
		VDD=3V、At low power mode		160		

Function Description

Ⅰ. Sensitivity adjustment

The total loading of electrode size and capacitance of connecting line on PCB can affect the sensitivity. So the sensitivity adjustment must according to the practical application on PCB. The TTP224B-RO8N offers some methods for adjusting the sensitivity outside

1. by the electrode size

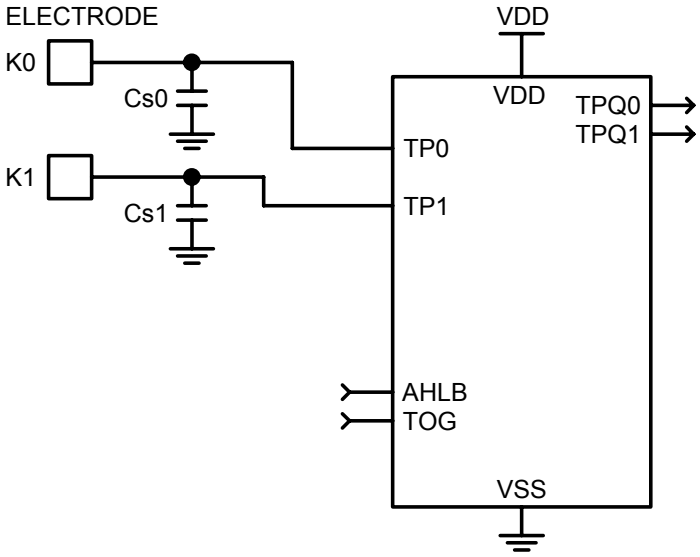
   Under other conditions are fixed. Using a larger electrode size can increase sensitivity. Otherwise it can decrease sensitivity. But the electrode size must use in the effective scope

2. by the panel thickness

   Under other conditions are fixed. Using a thinner panel can increase sensitivity. Otherwise it can decrease sensitivity. But the panel thickness must be below the maximum value

3. by the value of Cs0~Cs1（please see the down figure）

   Under other conditions are fixed. Add the capacitors Cs0~Cs1 can fine tune the sensitivity for single key, that lets all key's sensitivity identical. When do not use any capacitor to VSS, the sensitivity is most sensitive. When adding the values of Cs0~Cs1 will reduce sensitivity in the useful range（1≦Cs0~Cs1≦50pF）



Ⅱ. Output mode（By TOG、AHLB pad option）

The TTP224B-RO8N outputs（TPQ0~TPQ1）has direct mode active high or low by AHLB pad option, has toggle mode by TOG pad

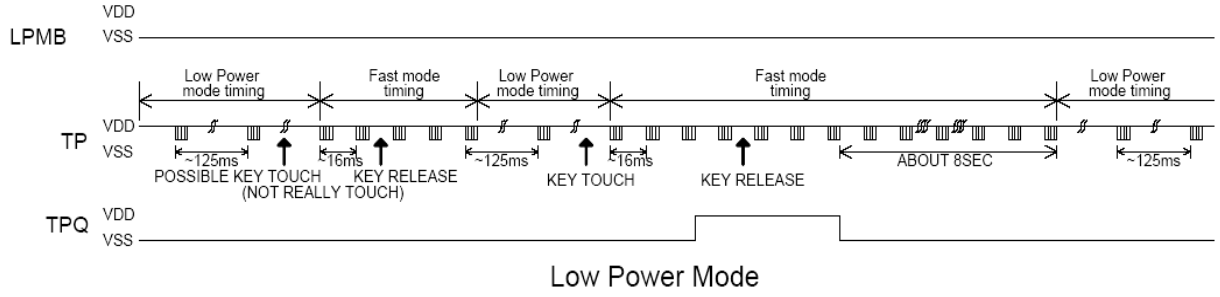
TOG	AHLB	Pad TPQ0 ～ TPQ1 option features	Remark
0	0	Direct mode, CMOS output active high	Default
0	1	Direct mode, CMOS output active low	
1	0	Toggle mode, CMOS output, Power on state=0	
1	1	Toggle mode, CMOS output, Power on state=1	

Ⅲ. Low power mode

The TTP224B-RO8N is Low Power mode. It will be saving power. When detecting key touch, it will switch to Fast mode. Until the key touch is released and will keep a time about 8sec. Then it returns to Low Power mode.

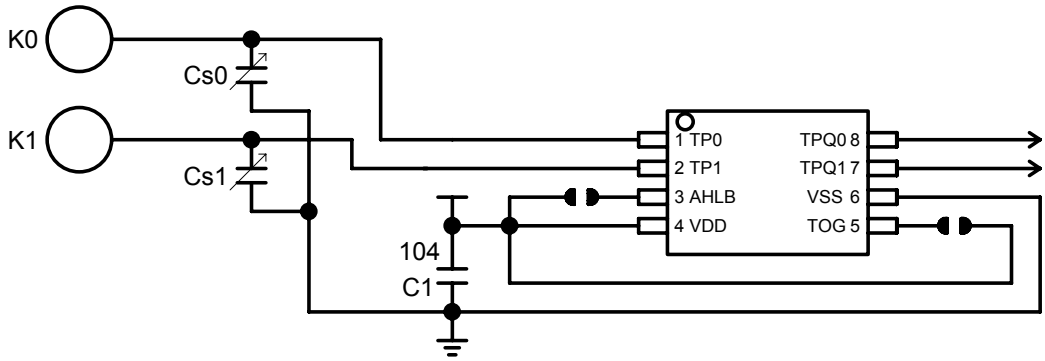
The states and timing please see below figure.

Low Power Mode timing diagram:



Low Power Mode

Application circuit



Option table:

Output Mode:

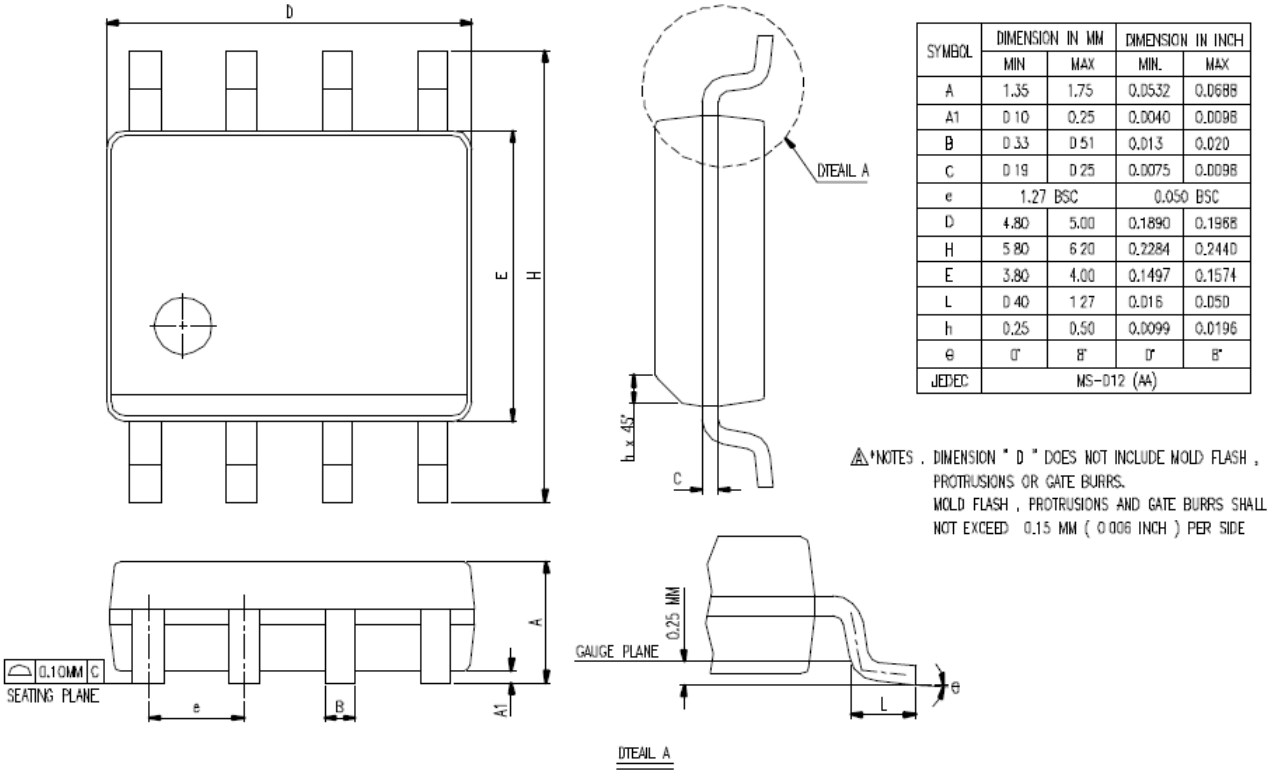
TOG	AHLB	Pad TPQ0~TP3 option features
OPEN	OPEN	Direct mode, CMOS active high output
OPEN	VDD	Direct mode, CMOS active low output
VDD	OPEN	Toggle mode, CMOS output, Power on state =0
VDD	VDD	Toggle mode, CMOS output, Power on state =1

P.S.：

1. On PCB, the length of lines from touch pad to IC pin shorter is better.
   And the lines do not parallel and cross with other lines.
2. The power supply must be stable. If the supply voltage drift or shift quickly, maybe causing sensitivity anomalies or false detections.
3. The material of panel covering on the PCB can not include the metal or the electric element. The paints on the surfaces are the same.
4. The C1 capacitor must be used between VDD and VSS; and should be routed with very short tracks to the device's VDD and VSS pins (TTP224B-RO8N).
5. The capacitance Cs0~Cs1 can be used to adjust the sensitivity. The value of Cs0~Cs1 use smaller, then the sensitivity will be better. The sensitivity adjustment must according to the practical application on PCB. The range of Cs0~Cs1 value are 1~50pF.
6. The sensitivity adjustment capacitors（Cs0~Cs1）must use smaller temperature coefficient and more stable capacitors. Such are X7R, NPO for example. So for touch application, recommend to use NPO capacitor, for reducing that the temperature varies to affect sensitivity.

Package outline

Package Type: SOP-8



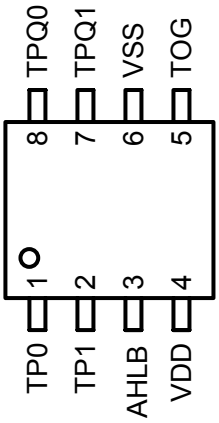
SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN	MAX	MIN.	MAX
A	1.35	1.75	0.0532	0.0688
A1	0.10	0.25	0.0040	0.0098
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.0075	0.0098
e	1.27 BSC		0.050 BSC	
D	4.80	5.00	0.1890	0.1968
H	5.80	6.20	0.2284	0.2440
E	3.80	4.00	0.1497	0.1574
L	0.40	1.27	0.016	0.050
h	0.25	0.50	0.0099	0.0196
θ	0°	8°	0°	8°
JEDEC	MS-012 (AA)			

⚠*NOTES . DIMENSION " D " DOES NOT INCLUDE MOLD FLASH , PROTRUSIONS OR GATE BURRS.
MOLD FLASH , PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE

Package configuration

TTP224B-RO8N

Package Type SOP-8



Ordering Information

TTP224B-RO8N

Package Type	Chip Type	Wafer Type
TTP224B-RO8N	No support	No support

REVISE HISTORY

1. 2016/01/18
   - Original version：V1.0