NOVATEK

PRELIMINARY

NT6616

16K 4-Bit Microcontroller with 16x33& 8x41 LCD Driver

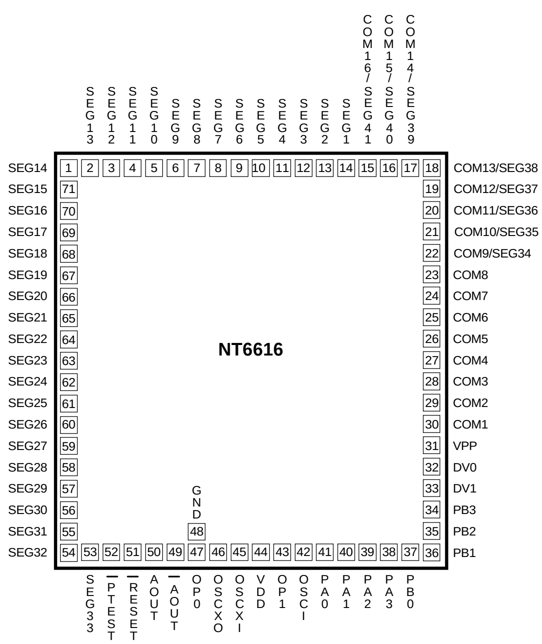
Features

- NT6610C-based single-chip with LCD driver
- 4-bit parallel processing ALU compatible with NT6610C
- ROM: 24K X 16 bit (bank switched)
- RAM: 512 X 4 bit (system control register & data memory)
- Operating Voltage Range: 2.4V - 5.5V
- 8 CMOS I/O ports
- 4 level subroutine nesting including interrupts
- One 8-bit timer with pre-divider circuit
- Warm-up timer for power-on reset
- Powerful interrupt sources:
  - Timer0 interrupt
  - Base timer interrupt
  - Port B interrupt (falling edge)
- Base timer clock: 32.768KHz X'tal oscillator.
- System clock: 2M~500KHz single-pin voltage-controlled oscillator
- Table Branch and Return Constant Instructions for Table Data Generation
- Data pointer with special system register control
- Two low power operation modes- HALT or STOP
- Instruction cycle time: 2µS for 2MHz voltage-controlled oscillator
- Built-in 2-channel PSG for sound effects, switchable to noise channel
- Directly driven speaker
- Type B LCD drive circuit , built-in voltage Pump
- LCD driver: 33 X 16 (1/16 duty cycle, 1/5 bias) or 41 X 8 (1/8 duty cycle, 1/4 bias)
- LCD off by programming LCDOFF register
- Available in CHIP FORM

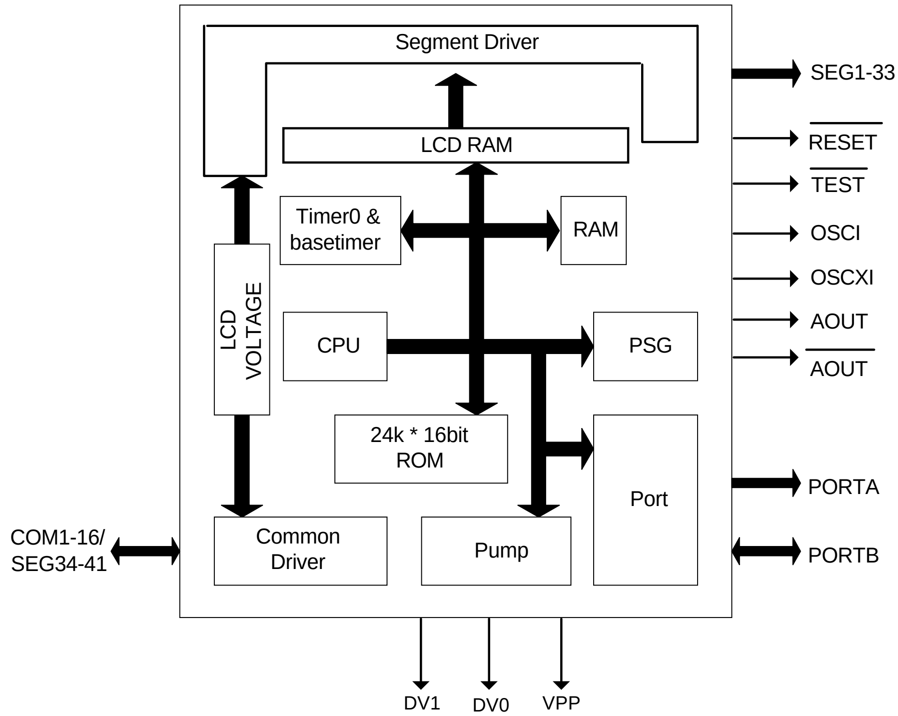
General Description

NT6616 Is a single chip 4 bit µC dedicated chip for hand-hold games. This device integrates a NT6610C 4-bit CPU core with RAM, ROM, 8 bit timer, 2-channel PSG, dot matrix LCD driver and pump circuit.

Pad Configuration



Block Diagram



Pad Description

Pad No.	Designation	I/O	Shared by	Description
14 -1, 71 - 53	SEG1 - 33	O		Segment signal output for LCD display
15 - 22	COM16 - 9	O	SEG41 - 34	Com/Seg signal output for LCD display
23 - 30	COM8 - 1	O		Common signal output for LCD display
31	V_{PP}	I		Capacity between V_{PP} and V_{CC} is expected for Pump
32, 33	DV0, DV1	O		Capacity between DV0 and DV1 is expected for Pump
34 - 37	PB3 - PB0	I/O	PORT INT.	Bit programmable I/O, Vector Interrupt
38 - 41	PA3 - PA0	O		Output ports
43, 47	OP1, OP0	I		Bonding option
44	V_{DD}			Power supply
42	OSCI	I		OSC input
48	GND			Ground
49, 50	$\overline{\text{AOUT}}$,AOUT	O		Audio output
51	$\overline{\text{RESET}}$	I		Reset input (active low, Internal pull-high).
52	$\overline{\text{TEST}}$	I		Test pin(Internal pull-high). No connect for user.
45, 46	OSCXI,OSCXO	I/O		32.768KHz X'tal OSC input, output

Functional Description

1. CPU

The CPU core contains the following function blocks: Program Counter, ALU, Carry Flag, Accumulator, Table Branch Register (TBR), Data Pointer (INX, DPH, DPM and DPL), and Stack.

1.1 PC (Program Counter)

The PC is used for ROM addressing consisting of 12-bits:
Page Register (PC11),
and Ripple Carry Counter (PC10 - PC0).

The program counter normally increases by one (+1) with each execution of an instruction except in the following cases:

1) When executing a jump instruction (such as JMP, BA0, BC);
2) When executing a subroutine call instruction (CALL);
3) When an interrupt occurs;
4) When the chip is at INITIAL RESET. The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can set an 1-bit page register for higher than 2K.

Program Counter can only address a 4K program ROM. To address 24K program ROM, use bank switch (Refer to the ROM description in Section 3 for details).

1.2 ALU and CY

ALU performs arithmetic and logic operations.

The ALU provides the following functions:

Binary addition/subtraction
(ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjustment for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR,OR, ANDI, EORI, ORI)
Decision (BA0, BA1, BA2, BA3, BAZ, BC)
The Carry Flag (CY) holds the arithmetic operation ALU overflow.

During interrupt or call instruction, carry flag is pushed into stack and restored from stack by RTNI. The carry flag is unaffected by an RTNW instruction.

1.3 Accumulator

Accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with ALU, data transfers between the accumulator and system registers, LCD RAM, or data memory can be performed.

1.4 Stack

A group of registers are used to save the contents of CY & PC (10-0) sequentially with each subroutine call or interrupt. It is organized as 13 bits X 4 levels. The MSB is saved for CY. 4 levels are the maximum allowed for subroutine calls and interrupts.

The contents of Stack are returned sequentially to the PC with the return instructions (RTNI/RTNW). Stack is operated on a first-in, last-out basis. This 4-level nesting includes both subroutine calls and interrupt requests. Note that program execution may enter an abnormal state if the number of calls and interrupt requests exceeds 4, and the bottom of stack will be shifted out.

2. RAM

RAM consists of general purpose data memory, LCD RAM, and system registers.

2.1 RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing.
Following is the memory allocation map:

$000 -- $01F : System register and I/O (32 x 4 bits)
$020 -- $1FF : Data Memory (480 x 4 bits)
$200 -- $2FF : Reserved
$300 -- $383 : LCD RAM space (132 x 4 bits)

2.2 Data Memory

Data memory is organized as 480 X 4 bits ($020 -- $1FF).
Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT.

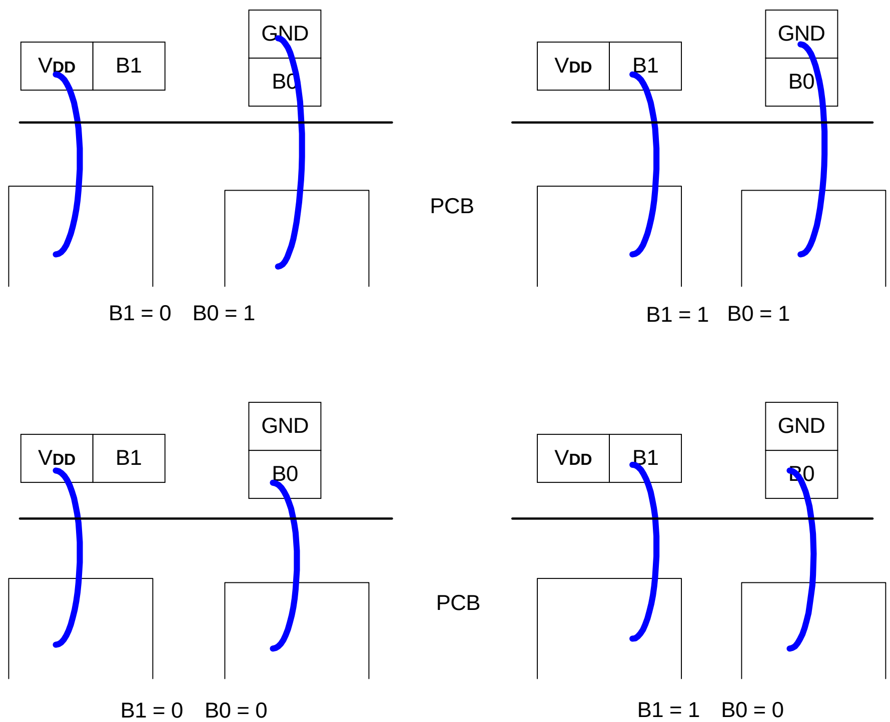
2.3 System Registers

The configuration of system registers is as follows:

	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W	Remarks
$00	IEBT	IET0	-	IEP	00	R/W	Interrupt enable flags
$01	IRQBT	IRQT0	-	IRQP	00	R/W	Interrupt request flags
$02	-	TM0.2	TM0.1	TM0.0	00	R/W	Timer0 mode register (TM0)
$03	HVL	BTM.2	BTM.1	BTM.0	00	R/W	HVL: Switch Base Timer into heavy load mode Base timer mode register (BTM)
$04	TL.3	TL.2	TL.1	TL.0	-	R/W	Timer0 load/counter register low digit
$05	TH.3	TH.2	TH.1	TH.0	-	R/W	Timer0 load/counter register high digit
$06	BTL.3	BTL.2	BTL.1	BTL.0	-	R/W	Base timer load/counter register low digit
$07	BTH.3	BTH.2	BTH.1	BTH.0	-	R/W	Base timer load/counter register high digit
$08	PA.3	PA.2	PA.1	PA.0	00	W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	0F	R/W	PORTB
$0A	-	-	-	-		-	-
$0B	-	-	-	-		-	-
$0C	-	-	OP1	OP0	01	R	Bonding Option
$0D	-	-	-	-	-	-	Reserved
$0E	TBR.3	TBR.2	TBR.1	TBR.0	-	R/W	Table Branch Register (TBR)
$0F	INX.3	INX.2	INX.1	INX.0	-	R/W	Pseudo Index Register (INX)
$10	DPL.3	DPL.2	DPL.1	DPL.0	-	R/W	Data Pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	-	R/W	Data Pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	-	R/W	Data Pointer for INX high nibble
$13	C1.3	C1.2	C1.1	C1.0	00	W	PSG Channel 1 low digit
$14	C1M	C1.6	C1.5	C1.4	00	W	PSG Channel 1 high digit
$15	C2.3	C2.2	C2.1	C2.0	00	W	PSG Channel 2 low digit
$16	C2.7	C2.6	C2.5	C2.4	00	W	PSG Channel 2
$17	C2.11	C2.10.	C2.9	C2.8	00	W	PSG Channel 2
$18	C2M	C2.14	C2.13	C2.12	00	W	PSG Channel 2 high digit
$19	VOL1	VOL0	CH2EN	CH1EN	00	W	Bit 0: PSG Channel 1 enable Bit 1: PSG Channel 2 enable Bit 2, Bit 3: Volume Control (Initially 0, no sound)
$1A	-	-	P1.1	P1.0	00	W	PSG 1 Prescaler
$1B	-	-	P2.1	P2.0	00	W	PSG 2 Prescaler
$1C	-	-	-	LCD OFF	00	R/W	Bit 0: LCD Power Control. 0 set LCD on, 1 set LCD off.
$1D	-	-	-	-		-	Reserved for ICE
$1E	COMSE	VDE	LCDI1	LCDI0	00	R/W	LCD Mode Control: Bit 0: LCD bias current control bit 0 Bit 1: LCD bias current control bit 1 Bit 2: Voltage Pump enable(Initially 0, disable VDE) Bit 3: 0 set 8 COM (Initially 0), 1 set 16 COM
$1F	BNK3	BNK2	BNK1	BNK0	00	R/W	Bank Register for ROM (BNK)

System Register 0CH

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power-on
$0CH	-	-	B1	B0	R	Bit0: Bonding option 0, internal weak drive Bit1: Bonding option 1, internal weak drive	Pull high Pull low
	X	X	1	0		B0 bond to GND and B1 bond to VDD	
	X	X	0	0		B0 bond to GND	
	X	X	1	1		B1 bond to VDD	
	X	X	0	1			Yes



NT6616 Bonding Option

Up to 4 different bonding options are possible for the user's needs. The chip's program has 4 different program flows that will vary depending on which bonding option is used. The readable contents of B1 and B0 will differ depending on bonding.

2.4 Data Pointer

Data memory can be indirectly addressed by the Data Pointer. Pointer address is located in register DPH(3-bits), DPM (3-bits) and DPL (4-bits). Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9-bit0 comes from DPH, DPM and DPL.

3.ROM

NT6616 can address up to 24K X 16 bit words of program area from $000 to $5FFF.

ROM SPACE in the system is 24576 X 16 bits.

3.1 Interrupt Vector Address Area ($000 to $004)

The program is sequentially executed. An area from address $000 through $004 is reserved for special interrupt service routines when starting execution of a vector address.

Address	Instruction	Remarks
$000	JMP	Jump to RESET
$001	JMP	Jump to Base Timer
$002	JMP	Jump to TIMER0
$003		Reserved
$004	JMP	Jump to PORTB

* JMP can be replaced by any other instruction.

3.2 Table Data Reference

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The Table Branch Register (TBR) and Accumulator (A) are placed by an offset address in program ROM . TJMP instruction branch is placed into address ((PC11 - PC8) X (2^8) + (TBR, A)). The address is determined by RTNW to return look-up value into (TBR, A). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into A.

3.3 Bank Switch Mapping

Program Counter (PC11 - PC0) can only address 4K ROM space. Bank switch technique is used to extend the CPU address space. The lower 2K of the CPU addressing space maps to lower 2K of ROM space (BANK0). The upper 2K of the CPU addressing space maps to one of the eleven banks (BANK 0 , 1 , 2 , 3 , 4 , 5 , 6 , 7 , 8 , 9 , A) of the upper 22K of ROM. (according to the Bank Register)

The bank switch mapping is as follows:

CPU Address	**ROM Space, $1FH = 0**	**ROM Space, $1FH = 1**	**ROM Space, $1FH = 2**	**ROM Space, $1FH = 3**	**ROM Space, $1FH = 4**	**ROM Space, $1FH = 5**	**ROM Space, $1FH = 6**
000-7FF	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)
800 - FFF	0800-0FFF (BANK 1)	1000 -17FF (BANK 2)	1800 -1FFF (BANK 3)	2000 -27FF (BANK 4)	2800 -2FFF (BANK 5)	3000 -37FF (BANK 6)	3800 -3FFF (BANK 7)

CPU Address	**ROM Space, $1FH = 7**	**ROM Space, $1FH = 8**	**ROM Space, $1FH = 9**	**ROM Space, $1FH = A**			
000-7FF	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)			
800 - FFF	4000 - 47FF (BANK 8)	4800 - 4FFF (BANK 9)	5000 - 57FF (BANK 10)	5800 - 5FFF (BANK 11)			

4. Timer

NT6616 has one 8-bit timer for count-up, consisting of an 8-bit counter and an 8-bit pre-loaded register. Besides, the other base timer provides real time clock function for time-keeper.

Timer0 provides the following functions:

* Programmable interval timer

* Read counter value

4.1 Timer0 Configuration and Operation:

Timer-0 is an 8-bit write-only timer load register (TL0L, TL0H), and an 8-bit read-only timer counter (TC0L, TC0H). Each consists of low order digits and high order digits. Timer counter is initialized by writing data into the timer load register (TL0L, TL0H).

First write the low-order digit, then the high-order digit. Timer counter is automatically loaded with the contents of the loaded register when the high order digit is written or count overflows occurs. Timer overflow will result in an interrupt if the interrupt enable flag is set.

Timer can be programmed in several different clock sources by setting Timer Mode Register (TM0).

4.2 Timer0 Mode Register:

Timer Mode Registers (TM0) are 4-bit registers used for timer control as shown in Table 1. Mode Register selects input pulse sources for the timer.

Table 1. Timer0 Mode Registers ($02)

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

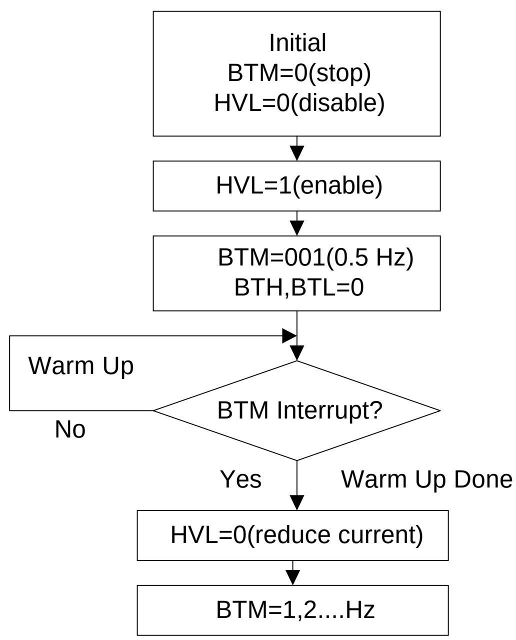
4.3 Base timer Configuration and Operation:

Base timer generates the different frequency interrupt for real time clock based on the value of BTM, shown as Table 2. The heavy load register, HVL, is used to switch 32.768K Hz X'tal oscillator into heavy load mode that makes the oscillation easier in the startup period but more current is needed.

Table 2. Base Timer Mode Registers ($03)

BTM.2	BTM.1	BTM.0	Interrupt Period	Clock Source
0	0	0	Stop(default)	32K Hz
0	0	1	0.5Hz	32K Hz
0	1	0	1 Hz	32K Hz
0	1	1	2 Hz	32K Hz
1	0	0	4 Hz	32K Hz
1	0	1	8 Hz	32K Hz
1	1	0	16 Hz	32K Hz
1	1	1	32 Hz	32K Hz

The example of using Base Timer:



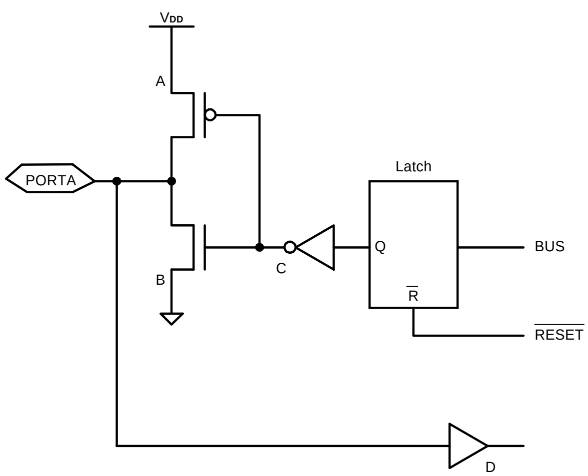
To achieve the above interrupt periods, system register $06 and $07, BTL and BTH, must be set to 00H for both.

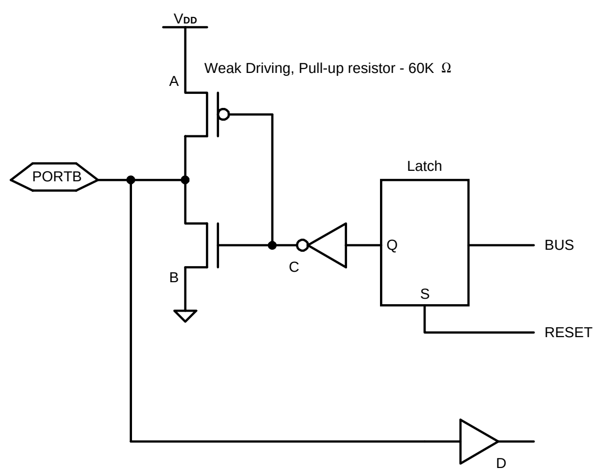
5. I/O Ports

5.1 Functional Description

- CMOS type output port
- PMOS as pull-up for Input on PortB
- Output low initially for PortA
- Output high initially for PortB
- Operates same as data memory for arithmetic and logic instructions

5.2 Circuit Diagrams (PORT A and PORT B)





5.3 Programming

- I/O ports can be accessed with the read/write system register.
- Memory-mapped addresses are listed as follows:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	-	-	-	-	-	Reserved
$0B	-	-	-	-	-	Reserved
$0C	-	-	OP1	OP0	R	Optional Register

- Before reading PORTB I/O bits, the user needs to output "1" to the same bit.

6. Programmable Sound Generator (PSG)

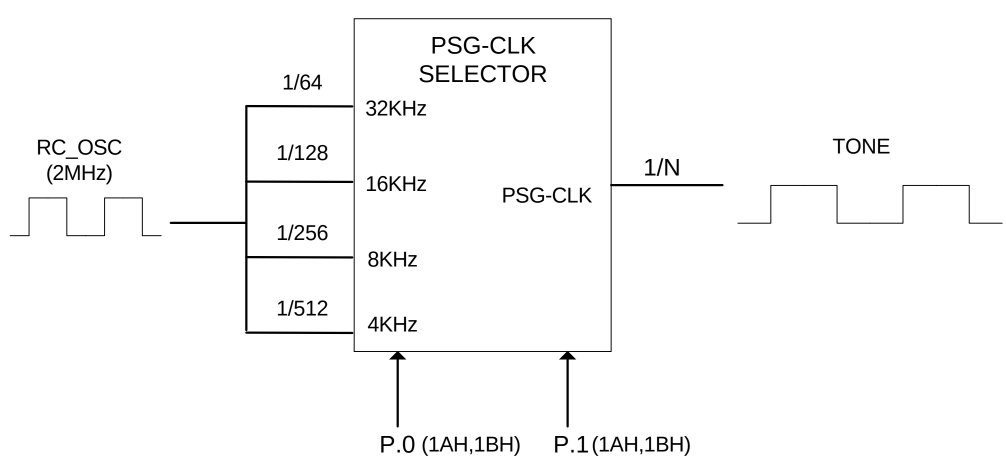
2-Channel PSG is provided. Channel 1 is a 7-bit pseudo random counter. Channel 2 is a 15-bit pseudo random counter. Mode bits C1M, C2M determine which of the two counters will be a noise or a tone generator. To reduce power consumption, disable the sound effect generator during both STOP and HALT.

Channel 2 TONE mode is same as Channel 1. (7-bit pseudo-random counter). This eliminates some programming codes.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	C1.3	C1.2	C1.1	C1.0	W	PSG Channel 1 low digit
$14	C1M	C1.6	C1.5	C1.4	W	PSG Channel 1 high digit
$15	C2.3	C2.2	C2.1	C2.0	W	PSG Channel 2 low digit
$16	C2.7	C2.6	C2.5	C2.4	W	PSG Channel 2
$17	C2.11	C2.10.	C2.9	C2.8	W	PSG Channel 2
$18	C2M	C2.14	C2.13	C2.12	W	PSG Channel 2 high digit
$19	VOL1	VOL0	CH2EN	CH1EN	W	Bit 0: PSG Channel 1 enable Bit 1: PSG Channel 2 enable Bit 2, Bit 3: Volume Control (Initially 0, no sound)
$1A	-	-	P1.1	P1.0	W	PSG 1 Prescaler
$1B	-	-	P2.1	P2.0	W	PSG 2 Prescaler

P.1	P.0	Prescaler Divide Ratio	Clock Source	Actual Clock
0	0	1	System Clock	32 KHz
0	1	2	System Clock	16 KHz
1	0	4	System Clock	8 KHz
1	1	8	System Clock	4 KHz

PSG subblock diagram



PSG clock can be selected by changing register $1AH and $1BH , as PSG-CLK is selected, the only way to get different tone is changing the value of N . The value of N is created by a group of counters (LSFR). Different initial data written to these counters, different N is created.

The value of N is corresponding to the REG C1.6~1.0 or REG C2.14~2.8 as shown in the following table

LSFR (C1.6~C1.0) (C2.14~C2.8)	**N**	**LSFR (C1.6~C1.0) (C2.14~C2.8)**	**N**	**LSFR (C1.6~C1.0) (C2.14~C2.8)**	**N**	**LSFR (C1.6~C1.0) (C2.14~C2.8)**	**N**
01	127	16	95	12	63	4B	31
02	126	2C	94	24	62	17	30
04	125	59	93	49	61	2E	29
08	124	33	92	13	60	5D	28
10	123	67	91	26	59	3B	27
20	122	4E	90	4D	58	77	26
41	121	1D	89	1B	57	6E	25
03	120	3A	88	36	56	5C	24
06	119	75	87	6D	55	39	23
0C	118	6A	86	5A	54	73	22
18	117	54	85	35	53	66	21
30	116	29	84	6B	52	4C	20
61	115	53	83	56	51	19	19
42	114	27	82	2D	50	32	18
05	113	4F	81	5B	49	65	17
0A	112	1F	80	37	48	4A	16
14	111	3E	79	6F	47	15	15
28	110	7D	78	5E	46	2A	14
51	109	7A	77	3D	45	55	13
23	108	74	76	7B	44	2B	12
47	107	68	75	76	43	57	11
0F	106	50	74	6C	42	2F	10
1E	105	21	73	58	41	5F	9
3C	104	43	72	31	40	3F	8
19	103	07	71	63	39	7F	7
72	102	0E	70	46	38	7E	6
64	101	1C	69	0D	37	7C	5
48	100	38	68	1A	36	78	4
11	99	71	67	34	35	70	3
22	98	62	66	69	34	60	2
45	97	44	65	52	33	40	1
0B	96	09	64	25	32		

Example:

A user uses 2MHz RC clock (RC OSC), and he wants to create a tone ‘C4’ whose frequency is 261.62Hz.

If he writes 00H to P.1 and P.0, then the PSG-CLK is 2M/64=32KHz, the value of N is 32K/261.62=122.3, look up 122 in the table, the corresponding initial data of LSFR is 20H.

If he writes 01H to P.1 and P.0, then the PSG-CLK is 2M/128=16KHz, the value of N is 16K/261.62=61.2, the initial data is 49H

If he writes 10H to P.1 and P.0, then the PSG-CLK is 2M/256=8KHz, the value of N is 8K/261.62=31, the initial data is 4BH.

If he writes 11H to P.1 and P.0, then the PSG-CLK is 2M/512=4KHz, the value of N is 4K/261.62=16, the initial data is 4AH.

When the tone frequency is too low, the wanted value of N maybe greater than 127, the counter cannot create this value, the better way is to select low PSG-CLK. For example, the frequency of tone ‘C1’ is 32.7Hz, if the PSG-CLK is greater than 8KHz, the wanted N is greater than 127, but the 4khz PSG-CLK can create this tone.

According to the illustration before, users can make a music table themselves, If user selects RC OSC as 2MHz, the music table is provided as following.

Music Table1:

Following is the music scale reference table for channel 1(or channel 2) under Actual Clock=32KHz.

Note	Ideal freq.	N	LSFR (C1.6~C1.0) (C2.14~C2.8)	Real freq.	Error %	Note	Ideal freq.	N	LSFR (C1.6~C1.0) (C2.14~C2.8)	Real freq.	Error %
C4	261.62	122	20	262.30	0.26%	**G5**	783.97	41	58	780.49	-0.44%
D4	293.66	109	51	293.58	-0.03%	**A5**	879.98	36	1A	888.89	1.01%
E4	329.62	97	45	329.90	0.08%	**B5**	987.75	32	25	1000.00	1.24%
F4	349.22	92	33	347.83	-0.40%	**C6**	1046.48	31	4B	1032.26	-1.36%
G4	391.99	82	27	390.24	-0.44%	**D6**	1174.63	27	3B	1185.19	0.90%
A4	439.99	73	21	438.36	-0.37%	**E6**	1318.48	24	5C	1333.33	1.13%
B4	493.87	65	44	492.31	-0.32%	**F6**	1396.88	23	39	1391.30	-0.40%
C5	523.24	61	49	524.59	0.26%	**G6**	1567.95	20	4C	1600.00	2.04%
D5	587.32	54	5A	592.59	0.90%	**A6**	1759.96	18	32	1777.78	1.01%
E5	659.24	49	5B	653.06	-0.94%	**B6**	1975.49	16	4A	2000.00	1.24%
F5	698.44	46	5E	695.65	-0.40%	**C7**	2092.96	15	15	2133.33	1.93%

Music Table2:

Following is the music scale reference table for channel 1(or channel 2) under Actual Clock=16KHz.

Note	Ideal freq.	N	LSFR (C1.6~C1.0) (C2.14~C2.8)	Real freq.	Error%	Note	Ideal freq.	N	LSFR (C1.6~C1.0) (C2.14~C2.8)	Real freq.	Error%
C3	130.81	122	20	131.15	0.26%	**G4**	391.99	41	58	390.24	-0.44%
D3	146.83	109	51	146.79	-0.03%	**A4**	439.99	36	1A	444.44	1.01%
E3	164.81	97	45	164.95	0.08%	**B4**	493.87	32	25	500.00	1.24%
F3	174.61	92	33	173.91	-0.40%	**C5**	523.24	31	4B	516.13	-1.36%
G3	195.99	82	27	195.12	-0.44%	**D5**	587.32	27	3B	592.59	0.90%
A3	220.00	73	21	219.18	-0.37%	**E5**	659.24	24	5C	666.67	1.13%
B3	246.94	65	44	246.15	-0.32%	**F5**	698.44	23	39	695.65	-0.40%
C4	261.62	61	49	262.30	0.26%	**G5**	783.97	20	4C	800.00	2.04%
D4	293.66	54	5A	296.30	0.90%	**A5**	879.98	18	32	888.89	1.01%
E4	329.62	49	5B	326.53	-0.94%	**B5**	987.75	16	4A	1000.00	1.24%
F4	349.22	46	5E	347.83	-0.40%	**C6**	1046.48	15	15	1066.67	1.93%

Music Table3:

Following is the music scale reference table for channel 1(or channel 2) under Actual Clock=8KHz.

Note	Ideal freq.	N	LSFR (C1.6~C1.0) (C2.14~C2.8)	Real freq.	Error%	Note	Ideal freq.	N	LSFR (C1.6~C1.0) (C2.14~C2.8)	Real freq.	Error%
C2	65.41	122	20	65.57	0.26%	**G3**	195.99	41	58	195.12	-0.44%
D2	73.41	109	51	73.39	-0.03%	**A3**	220.00	36	1A	222.22	1.01%
E2	82.41	97	45	82.47	0.08%	**B3**	246.94	32	25	250.00	1.24%
F2	87.31	92	33	86.96	-0.40%	**C4**	261.62	31	4B	258.06	-1.36%
G2	98.00	82	27	97.56	-0.44%	**D4**	293.66	27	3B	296.30	0.90%
A2	110.00	73	21	109.59	-0.37%	**E4**	329.62	24	5C	333.33	1.13%
B2	123.47	65	44	123.08	-0.32%	**F4**	349.22	23	39	347.83	-0.40%
C3	130.81	61	49	131.15	0.26%	**G4**	391.99	20	4C	400.00	2.04%
D3	146.83	54	5A	148.15	0.90%	**A4**	439.99	18	32	444.44	1.01%
E3	164.81	49	5B	163.27	-0.94%	**B4**	493.87	16	4A	500.00	1.24%
F3	174.61	46	5E	173.91	-0.40%	**C5**	523.24	15	15	533.33	1.93%

Music Table4:

Following is the music scale reference table for channel 1(or channel 2) under Actual Clock=4KHz.

Note	Ideal freq.	N	LSFR (C1.6~C1.0) (C2.14~C2.8)	Real freq.	Error%	Note	Ideal freq.	N	LSFR (C1.6~C1.0) (C2.14~C2.8)	Real freq.	Error%
C1	32.70	122	20	32.79	0.26%	**G2**	98.00	41	58	97.56	-0.44%
D1	36.71	109	51	36.70	-0.03%	**A2**	110.00	36	1A	111.11	1.01%
E1	41.20	97	45	41.24	0.08%	**B2**	123.47	32	25	125.00	1.24%
F1	43.65	92	33	43.48	-0.40%	**C3**	130.81	31	4B	129.03	-1.36%
G1	49.00	82	27	48.78	-0.44%	**D3**	146.83	27	3B	148.15	0.90%
A1	55.00	73	21	54.79	-0.37%	**E3**	164.81	24	5C	166.67	1.13%
B1	61.73	65	44	61.54	-0.32%	**F3**	174.61	23	39	173.91	-0.40%
C2	65.41	61	49	65.57	0.26%	**G3**	195.99	20	4C	200.00	2.04%
D2	73.41	54	5A	74.07	0.90%	**A3**	220.00	18	32	222.22	1.01%
E2	82.41	49	5B	81.63	-0.94%	**B3**	246.94	16	4A	250.00	1.24%
F2	87.31	46	5E	86.96	-0.40%	**C4**	261.62	15	15	266.67	1.93%

7. LCD

The LCD has 16 common signal pads and 33 segment driver pads, a controller, LCD voltage generator,. The controller consists of display data RAM and a duty generator. The LCD data RAM is a dual port RAM that automatically transfers data to segment. The LCD can be turned off with the internal LCDOFF register.

LCD frame frequency is controlled by 32.768KHz clock. Therefore, 32.768KHz clock must be enabled before LCD is turned on. To save power, the main clock can be stopped and the 32.768KHz enabled to keep LCD on.

After osc32k is steady, setting VDE can enable Voltage Pump circuit . LCD voltage is pumped to 4.5V if Pump is enabled and V_{DD} is 3.0V.

The LCD has two modes,1/16 duty and 1/8 duty

Table 1. LCD Mode Control Register $1EH:

$1EH.BIT3	0 set 8 duty(initially 0),1 set 16 duty
$1EH.BIT2	Voltage pump enable(initially 0,disable pump)
$1EH.BIT1	LCD bias current control bit1
$1EH.BIT0	LCD bias current control bit0

Table 2. LCDI1 and LCDI0 control the LCD driving current.

LCDI1	LCDI0	LCD Bias Current
0	0	Minimum (Default)
0	1	
1	0	
1	1	Maximum

7.1 1/16 duty (16 com x 33 seg)

7.1.1 LCD RAM Area Configuration for 1/16 duty:

Duty	COM4	COM3	COM2	COM1
Address	**Bit3**	**Bit2**	**Bit1**	**Bit0**
$300	SEG1	SEG1	SEG1	SEG1
$301	SEG2	SEG2	SEG2	SEG2
$302	SEG3	SEG3	SEG3	SEG3
$303	SEG4	SEG4	SEG4	SEG4
$304	SEG5	SEG5	SEG5	SEG5
$305	SEG6	SEG6	SEG6	SEG6
$306	SEG7	SEG7	SEG7	SEG7
$307	SEG8	SEG8	SEG8	SEG8
$308	SEG9	SEG9	SEG9	SEG9
$309	SEG10	SEG10	SEG10	SEG10
$30A	SEG11	SEG11	SEG11	SEG11
$30B	SEG12	SEG12	SEG12	SEG12
$30C	SEG13	SEG13	SEG13	SEG13
$30D	SEG14	SEG14	SEG14	SEG14
$30E	SEG15	SEG15	SEG15	SEG15
$30F	SEG16	SEG16	SEG16	SEG16
$310	SEG17	SEG17	SEG17	SEG17
$311	SEG18	SEG18	SEG18	SEG18
$312	SEG19	SEG19	SEG19	SEG19
$313	SEG20	SEG20	SEG20	SEG20
$314	SEG21	SEG21	SEG21	SEG21
$315	SEG22	SEG22	SEG22	SEG22
$316	SEG23	SEG23	SEG23	SEG23
$317	SEG24	SEG24	SEG24	SEG24
$318	SEG25	SEG25	SEG25	SEG25
$319	SEG26	SEG26	SEG26	SEG26
$31A	SEG27	SEG27	SEG27	SEG27
$31B	SEG28	SEG28	SEG28	SEG28
$31C	SEG29	SEG29	SEG29	SEG29
$31D	SEG30	SEG30	SEG30	SEG30
$31E	SEG31	SEG31	SEG31	SEG31
$31F	SEG32	SEG32	SEG32	SEG32
$380	SEG33	SEG33	SEG33	SEG33

LCD RAM Area Configuration (continued):

Duty	COM8	COM7	COM6	COM5
Address	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
$320	SEG1	SEG1	SEG1	SEG1
$321	SEG2	SEG2	SEG2	SEG2
$322	SEG3	SEG3	SEG3	SEG3
$323	SEG4	SEG4	SEG4	SEG4
$324	SEG5	SEG5	SEG5	SEG5
$325	SEG6	SEG6	SEG6	SEG6
$326	SEG7	SEG7	SEG7	SEG7
$327	SEG8	SEG8	SEG8	SEG8
$328	SEG9	SEG9	SEG9	SEG9
$329	SEG10	SEG10	SEG10	SEG10
$32A	SEG11	SEG11	SEG11	SEG11
$32B	SEG12	SEG12	SEG12	SEG12
$32C	SEG13	SEG13	SEG13	SEG13
$32D	SEG14	SEG14	SEG14	SEG14
$32E	SEG15	SEG15	SEG15	SEG15
$32F	SEG16	SEG16	SEG16	SEG16
$330	SEG17	SEG17	SEG17	SEG17
$331	SEG18	SEG18	SEG18	SEG18
$332	SEG19	SEG19	SEG19	SEG19
$333	SEG20	SEG20	SEG20	SEG20
$334	SEG21	SEG21	SEG21	SEG21
$335	SEG22	SEG22	SEG22	SEG22
$336	SEG23	SEG23	SEG23	SEG23
$337	SEG24	SEG24	SEG24	SEG24
$338	SEG25	SEG25	SEG25	SEG25
$339	SEG26	SEG26	SEG26	SEG26
$33A	SEG27	SEG27	SEG27	SEG27
$33B	SEG28	SEG28	SEG28	SEG28
$33C	SEG29	SEG29	SEG29	SEG29
$33D	SEG30	SEG30	SEG30	SEG30
$33E	SEG31	SEG31	SEG31	SEG31
$33F	SEG32	SEG32	SEG32	SEG32
$381	SEG33	SEG33	SEG33	SEG33

LCD RAM Area Configuration (continued):

Duty	COM12	COM11	COM10	COM9
Address	**Bit3**	**Bit2**	**Bit1**	**Bit0**
$340	SEG1	SEG1	SEG1	SEG1
$341	SEG2	SEG2	SEG2	SEG2
$342	SEG3	SEG3	SEG3	SEG3
$343	SEG4	SEG4	SEG4	SEG4
$344	SEG5	SEG5	SEG5	SEG5
$345	SEG6	SEG6	SEG6	SEG6
$346	SEG7	SEG7	SEG7	SEG7
$347	SEG8	SEG8	SEG8	SEG8
$348	SEG9	SEG9	SEG9	SEG9
$349	SEG10	SEG10	SEG10	SEG10
$34A	SEG11	SEG11	SEG11	SEG11
$34B	SEG12	SEG12	SEG12	SEG12
$34C	SEG13	SEG13	SEG13	SEG13
$34D	SEG14	SEG14	SEG14	SEG14
$34E	SEG15	SEG15	SEG15	SEG15
$34F	SEG16	SEG16	SEG16	SEG16
$350	SEG17	SEG17	SEG17	SEG17
$351	SEG18	SEG18	SEG18	SEG18
$352	SEG19	SEG19	SEG19	SEG19
$353	SEG20	SEG20	SEG20	SEG20
$354	SEG21	SEG21	SEG21	SEG21
$355	SEG22	SEG22	SEG22	SEG22
$356	SEG23	SEG23	SEG23	SEG23
$357	SEG24	SEG24	SEG24	SEG24
$358	SEG25	SEG25	SEG25	SEG25
$359	SEG26	SEG26	SEG26	SEG26
$35A	SEG27	SEG27	SEG27	SEG27
$35B	SEG28	SEG28	SEG28	SEG28
$35C	SEG29	SEG29	SEG29	SEG29
$35D	SEG30	SEG30	SEG30	SEG30
$35E	SEG31	SEG31	SEG31	SEG31
$35F	SEG32	SEG32	SEG32	SEG32
$382	SEG33	SEG33	SEG33	SEG33

LCD RAM Area Configuration (continued):

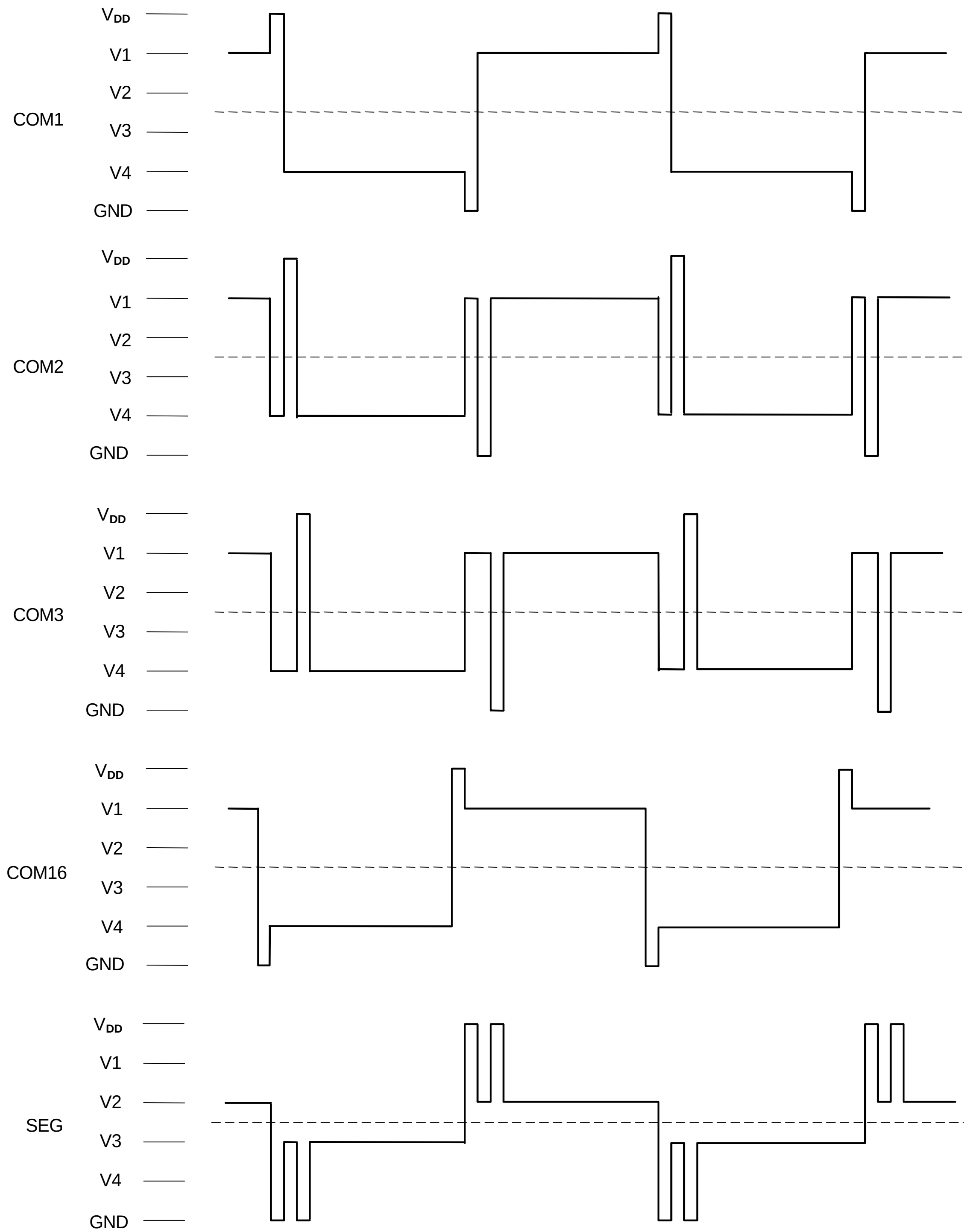
Duty	COM16	COM15	COM14	COM13
Address	**Bit3**	**Bit2**	**Bit1**	**Bit0**
$360	SEG1	SEG1	SEG1	SEG1
$361	SEG2	SEG2	SEG2	SEG2
$362	SEG3	SEG3	SEG3	SEG3
$363	SEG4	SEG4	SEG4	SEG4
$364	SEG5	SEG5	SEG5	SEG5
$365	SEG6	SEG6	SEG6	SEG6
$366	SEG7	SEG7	SEG7	SEG7
$367	SEG8	SEG8	SEG8	SEG8
$368	SEG9	SEG9	SEG9	SEG9
$369	SEG10	SEG10	SEG10	SEG10
$36A	SEG11	SEG11	SEG11	SEG11
$36B	SEG12	SEG12	SEG12	SEG12
$36C	SEG13	SEG13	SEG13	SEG13
$36D	SEG14	SEG14	SEG14	SEG14
$36E	SEG15	SEG15	SEG15	SEG15
$36F	SEG16	SEG16	SEG16	SEG16
$370	SEG17	SEG17	SEG17	SEG17
$371	SEG18	SEG18	SEG18	SEG18
$372	SEG19	SEG19	SEG19	SEG19
$373	SEG20	SEG20	SEG20	SEG20
$374	SEG21	SEG21	SEG21	SEG21
$375	SEG22	SEG22	SEG22	SEG22
$376	SEG23	SEG23	SEG23	SEG23
$377	SEG24	SEG24	SEG24	SEG24
$378	SEG25	SEG25	SEG25	SEG25
$379	SEG26	SEG26	SEG26	SEG26
$37A	SEG27	SEG27	SEG27	SEG27
$37B	SEG28	SEG28	SEG28	SEG28
$37C	SEG29	SEG29	SEG29	SEG29
$37D	SEG30	SEG30	SEG30	SEG30
$37E	SEG31	SEG31	SEG31	SEG31
$37F	SEG32	SEG32	SEG32	SEG32
$383	SEG33	SEG33	SEG33	SEG33

7.1.2 LCD Voltage Generator

LCD voltages V1, V2, V3, V4 are obtained using resistor divider network. The LCD can be turned off by writing the LCDOFF register.

7.1.3 LCD Waveform

The output waveform of 1/16 duty and 1/5 bias is shown below.



7.2 1/8 duty. (8com x 41 seg) (COM [9:16] are used as SEG[34:41]**)**

7.2.1 LCD RAM Area Configuration for 1/8 duty (power on default)

Duty	COM4	COM3	COM2	COM1
Address	**Bit3**	**Bit2**	**Bit1**	**Bit0**
$300	SEG1	SEG1	SEG1	SEG1
$301	SEG2	SEG2	SEG2	SEG2
$302	SEG3	SEG3	SEG3	SEG3
$303	SEG4	SEG4	SEG4	SEG4
$304	SEG5	SEG5	SEG5	SEG5
$305	SEG6	SEG6	SEG6	SEG6
$306	SEG7	SEG7	SEG7	SEG7
$307	SEG8	SEG8	SEG8	SEG8
$308	SEG9	SEG9	SEG9	SEG9
$309	SEG10	SEG10	SEG10	SEG10
$30A	SEG11	SEG11	SEG11	SEG11
$30B	SEG12	SEG12	SEG12	SEG12
$30C	SEG13	SEG13	SEG13	SEG13
$30D	SEG14	SEG14	SEG14	SEG14
$30E	SEG15	SEG15	SEG15	SEG15
$30F	SEG16	SEG16	SEG16	SEG16
$310	SEG17	SEG17	SEG17	SEG17
$311	SEG18	SEG18	SEG18	SEG18
$312	SEG19	SEG19	SEG19	SEG19
$313	SEG20	SEG20	SEG20	SEG20
$314	SEG21	SEG21	SEG21	SEG21
$315	SEG22	SEG22	SEG22	SEG22
$316	SEG23	SEG23	SEG23	SEG23
$317	SEG24	SEG24	SEG24	SEG24
$318	SEG25	SEG25	SEG25	SEG25
$319	SEG26	SEG26	SEG26	SEG26
$31A	SEG27	SEG27	SEG27	SEG27
$31B	SEG28	SEG28	SEG28	SEG28
$31C	SEG29	SEG29	SEG29	SEG29
$31D	SEG30	SEG30	SEG30	SEG30
$31E	SEG31	SEG31	SEG31	SEG31
$31F	SEG32	SEG32	SEG32	SEG32
$340	SEG33	SEG33	SEG33	SEG33
$341	SEG34	SEG34	SEG34	SEG34
$342	SEG35	SEG35	SEG35	SEG35
$343	SEG36	SEG36	SEG36	SEG36
$344	SEG37	SEG37	SEG37	SEG37
$345	SEG38	SEG38	SEG38	SEG38
$346	SEG39	SEG39	SEG39	SEG39
$347	SEG40	SEG40	SEG40	SEG40
$348	SEG41	SEG41	SEG41	SEG41

LCD RAM Area Configuration (continued):

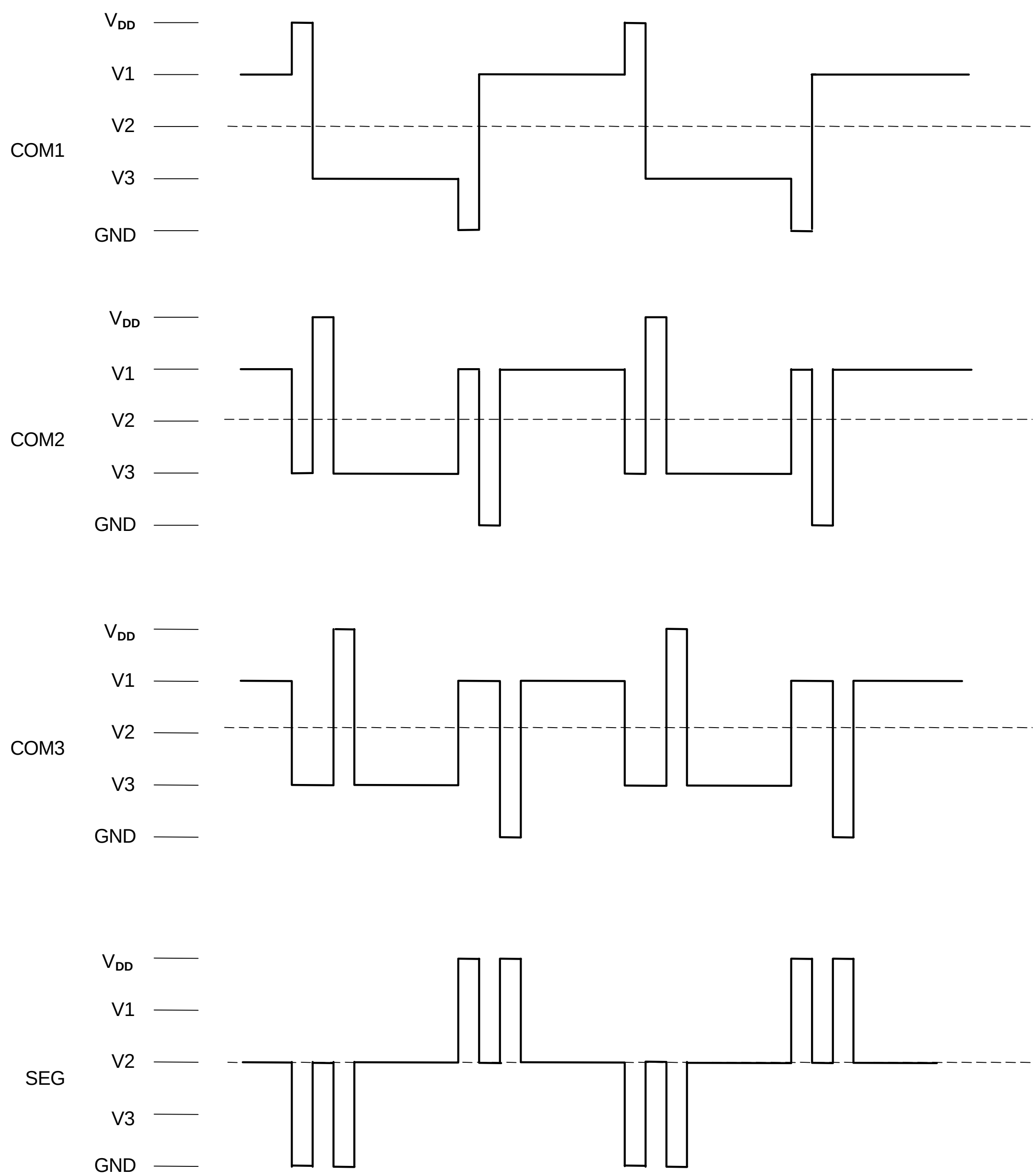
Duty	COM8	COM7	COM6	COM5
Address	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
$320	SEG1	SEG1	SEG1	SEG1
$321	SEG2	SEG2	SEG2	SEG2
$322	SEG3	SEG3	SEG3	SEG3
$323	SEG4	SEG4	SEG4	SEG4
$324	SEG5	SEG5	SEG5	SEG5
$325	SEG6	SEG6	SEG6	SEG6
$326	SEG7	SEG7	SEG7	SEG7
$327	SEG8	SEG8	SEG8	SEG8
$328	SEG9	SEG9	SEG9	SEG9
$329	SEG10	SEG10	SEG10	SEG10
$32A	SEG11	SEG11	SEG11	SEG11
$32B	SEG12	SEG12	SEG12	SEG12
$32C	SEG13	SEG13	SEG13	SEG13
$32D	SEG14	SEG14	SEG14	SEG14
$32E	SEG15	SEG15	SEG15	SEG15
$32F	SEG16	SEG16	SEG16	SEG16
$330	SEG17	SEG17	SEG17	SEG17
$331	SEG18	SEG18	SEG18	SEG18
$332	SEG19	SEG19	SEG19	SEG19
$333	SEG20	SEG20	SEG20	SEG20
$334	SEG21	SEG21	SEG21	SEG21
$335	SEG22	SEG22	SEG22	SEG22
$336	SEG23	SEG23	SEG23	SEG23
$337	SEG24	SEG24	SEG24	SEG24
$338	SEG25	SEG25	SEG25	SEG25
$339	SEG26	SEG26	SEG26	SEG26
$33A	SEG27	SEG27	SEG27	SEG27
$33B	SEG28	SEG28	SEG28	SEG28
$33C	SEG29	SEG29	SEG29	SEG29
$33D	SEG30	SEG30	SEG30	SEG30
$33E	SEG31	SEG31	SEG31	SEG31
$33F	SEG32	SEG32	SEG32	SEG32
$360	SEG33	SEG33	SEG33	SEG33
$361	SEG34	SEG34	SEG34	SEG34
$362	SEG35	SEG35	SEG35	SEG35
$363	SEG36	SEG36	SEG36	SEG36
$364	SEG37	SEG37	SEG37	SEG37
$365	SEG38	SEG38	SEG38	SEG38
$366	SEG39	SEG39	SEG39	SEG39
$367	SEG40	SEG40	SEG40	SEG40
$368	SEG41	SEG41	SEG41	SEG41

7.2.2 LCD Voltage Generator

LCD voltages V1, V2, V3 are obtained using resistor divider network. The LCD can be turned off by with the LCDOFF register.

7.2.3 LCD Waveform

The output waveform of 1/8 duty and 1/4 bias is shown below.



8. Interrupt

Three interrupt sources are available on the NT6616:

- Base Timer interrupt (BTMR)
- Timer0 interrupt (TMR0)
- Port falling edge detection interrupt ($\overline{PB}$)

8.1 Interrupt Control Bits and Interrupt Service:

- Interrupt control flags are mapped on $00 through $01 of the system register. They can be accessed or tested by the program. These flags are cleared to 0 at initialization.

	Bit 3	Bit 2	Bit 1	Bit 0	Remarks
$00	IEBT	IET0	-	IEP	Interrupt enable flags
$01	IRQBT	IRQT0	-	IRQP	Interrupt request flags

- Interrupt request begins when IRQx is set to 1 and IEx is 1. At this time, interrupt will activate and vector address will commence from the priority PLA corresponding to the interrupt source. When an interrupt occurs, the PC and CY flags will be saved in stack memory and jump to an interrupt service vector address. After an interrupt occurs, all interrupt enable flags (IEx) are automatically reset to 0, so any interrupt is disabled. The IRQx, which caused interrupt, must be reset by software in the interrupt service routine. When IEx is set to 1 again, NT6616 can supply multi-level interrupts.

8.2 Vector Address and Interrupt Priority

Priority	Interrupt source
1 (Most)	RESET
2	BTM
3	TMR0
4	Reserved
5 (Least)	$\overline{PB}$

9. System Clock and Oscillation Circuit

The system clock generator produces clock pulses supplied to the CPU and on-chip peripherals.
-Instruction cycle time : 2 µs for 2 MHz clock

10. HALT or STOP

- After execution of HALT, NT6616 will enter HALT state. In HALT state, the CPU will stop operating, but the peripheral circuit (timer) will operate.
- After execution of STOP, NT6616 will enter STOP. In STOP, the entire chip (including RC oscillator) will stop operating. If 32.768Khz clock is actived by setting BTM.2-BTM.0, the Base Timer keeps running even in STOP mode. In the same manner, LCD outputs waveform if 32.768Khz LCD clock source is chosen in STOP mode.
- In HALT, NT6616 will wake up if an interrupt occurs.
- In STOP, NT6616 will wake up if port interrupt occurs or BTM interrupt occurs.

11. Warm-up Timer

The warm-up timer eliminates an initial oscillation instability in the following two cases:
1) power-on reset;
2) wake-up from STOP.
Software warm-up is needed for Base Timer start-up.

The warm-up time interval is 32 clock cycles.

12. Pump

The Pump circuit needs OSC32KHz clock. When OSC32KHz clock is stopped, writing ‘1’ to VDE (bit2 of register $1EH) can not enable Pump. In order to get a steady clock, when the OSC32KHz clock begins to vibrate, Pump will not enable in the first one second even if VDE is set to ‘1’.

13. System Reset

- Hardware reset input
- Warm-up timer for power-on reset

Initial State

Hardware	After Power-on Reset
Program Counter	$000
CY	Undefined
Data Memory	Undefined
System Register	Undefined
AC	Undefined
Timer Counter	Undefined
Timer Load Register	Undefined
Interrupt Enable Flags	0
Interrupt Request Flags	0
DPH, DPM, DPL	Undefined
TBR	Undefined
LCD Driver Output	active
Base Timer	stop
PORT A	$0
PORT B	$F
COMSE	0
VDE	0
LCDI1, LCDI1	0
Bank	0

14 Instruction set

All instruction are one cycle and one word instruction. The characteristics is memory oriented operation.

1 Arithmetic and Logical Instruction

1.1Accumulator type

Mnemonic	Instruction Code	Function	Flag Change
ADC X(, B)	00000 0bbb xxx xxxx	AC $\leftarrow M_x + A_c + CY$	CY
ADCM X(, B)	00000 1bbb xxx xxxx	AC, $M_x \leftarrow M_x + A_c + CY$	CY
ADD X(, B)	00001 0bbb xxx xxxx	AC $\leftarrow M_x + A_c$	CY
ADDM X(, B)	00001 1bbb xxx xxxx	AC, $M_x \leftarrow M_x + A_c$	CY
SBC X(, B)	00010 0bbb xxx xxxx	AC $\leftarrow M_x + -A_c + CY$	CY
SBCM X(, B)	00010 1bbb xxx xxxx	AC, $M_x \leftarrow M_x + -A_c + CY$	CY
SUB X(, B)	00011 0bbb xxx xxxx	AC $\leftarrow M_x + -A_c + 1$	CY
SUBM X(, B)	00011 1bbb xxx xxxx	AC, $M_x \leftarrow M_x + -A_c + 1$	CY
EOR X(, B)	00100 0bbb xxx xxxx	AC $\leftarrow M_x \oplus A_c$	
EORM X(, B)	00100 1bbb xxx xxxx	AC, $M_x \leftarrow M_x \oplus A_c$	
OR X(, B)	00101 0bbb xxx xxxx	AC $\leftarrow M_x \mid A_c$	
ORM X(, B)	00101 1bbb xxx xxxx	AC, $M_x \leftarrow M_x \mid A_c$	
AND X(, B)	00110 0bbb xxx xxxx	AC $\leftarrow M_x \,\&\, A_c$	
ANDM X(, B)	00110 1bbb xxx xxxx	AC, $M_x \leftarrow M_x \,\&\, A_c$	
SHR	11110 0000 000 0000	$0 \rightarrow$ AC[3] ; AC[0] $\rightarrow$ CY ; AC shift right one bit	CY

1.2 Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X , I	01000 i i i i xxx xxxx	AC $\leftarrow M_x + I$	CY
ADIM X , I	01001 i i i i xxx xxxx	AC, $M_x \leftarrow M_x + I$	CY
SBI X , I	01010 i i i i xxx xxxx	AC $\leftarrow M_x + -I + 1$	CY
SBIM X , I	01011 i i i i xxx xxxx	AC, $M_x \leftarrow M_x + -I + 1$	CY
EORI X , I	01100 i i i i xxx xxxx	AC, $M_x \leftarrow M_x \oplus I$	
ORI X , I	01101 i i i i xxx xxxx	AC, $M_x \leftarrow M_x \vee I$	
ANDI X , I	01110 i i i i xxx xxxx	AC, $M_x \leftarrow M_x \wedge I$	

1.3 Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC; $M_x \leftarrow$Decimal adjust for add.	CY
DAS X	11001 1010 xxx xxxx	AC; $M_x \leftarrow$Decimal adjust for sub.	CY

2 Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X(, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X(, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X , I	01111 i i i i xxx xxxx	AC, Mx ← I	

3 Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC=0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC≠0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY=1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY≠1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC(0)=1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC(1)=1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC(2)=1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC(3)=1	
CALL X	11000 xxxx xxx xxxx	ST ← CY ; PC+1 PC ← X(Not include p)	
RTNW H , L	11010 000h hhh l 1 l l	PC← ST ; TBR← hhhh; A←l l l l	
RTNI	11010 1000 000 0000	CY ; PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X(Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-C8)(TBR)(A)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data	p	ROM page = 0
AC	Accumulator	⊕	Logical exclusive OR	ST	Stack
-AC	Complement of accumulator	|	Logical OR	TBR	Table Branch Register
CY	Carry flag	&	Logical AND		
Mx	Data memory	bbb	RAM bank=000		

Absolute Maximum Rating

DC Supply Voltage . . . . -0.3Vto +7V

Input Voltage . . . .-0.3V to V_{DD} +0.3V

Operating Ambient Temperature . . . .-10°C to +60°C

Storage Temperature . . . . -55°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V_{DD} = 4.5V, GND = 0V, T_A = 25°C, F_{OSC} = 2 MHz, unless otherwise specified)

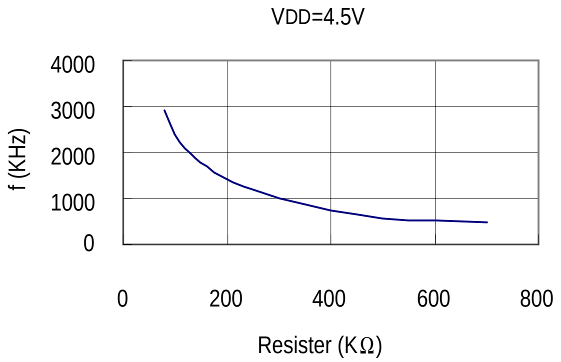
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	3.6	4.5	5.5	V	
Operating Current	I_{OP}		0.5	0.8	mA	V_{DD} = 4.5V, 32.768KHz OSC off, all outputs (ports AOUT, $\overline{AOUT}$) unloaded, execute NOP instruction
Standby Current	I_{SB1}		4.5	7.5	μA	V_{DD} = 4.5V, Stop (RC OSC stop, Base Timer on , LCD off , all outputs unloaded)
Standby Current	I_{SB2}		0.7	1.2	μA	V_{DD} = 4.5V, Stop (OSC and 32.768KHz OSC off, Base Timer stop, LCD off , all outputs unloaded)
Input Current	I_I		10	50	μA	V_{DD} = 4.5V V(input) = 4.5V
Input High Voltage	V_{IH}	V_{DD}-0.5		V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	-0.3		GND+0.5	V	
Output Low Drive Current	I_{OL}	3.5			mA	PORTA and PORTB, V_{OL} = 0.8V
Output High Drive Current	I_{OH}	500			μA	PORTA, V_{OH} = V_{DD} -0.5V
AOUT, $\overline{AOUT}$, Output Current	I_{OH} I_{OL}	2 2			mA mA	V_{OUT} = V_{DD} -1V V_{OUT} = 0.5V
LCD Lighting	I_{LCD}		25.0	35.0	μA	V_{DD} = 4.5V, LCD on current, (LCDI1, LCDI0) = (0,0). (For reference only)
Pull-up Resistance	R_{PU}		20	100	KΩ	PORTB

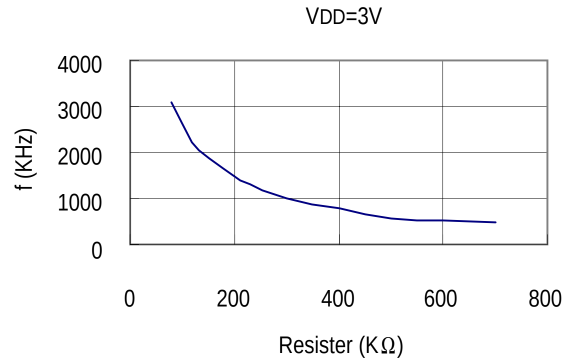
DC Electrical Characteristics

(V_{DD} = 3.0V, GND = 0V, T_A = 25°C, F_{OSC} = 2 MHz, unless otherwise specified)

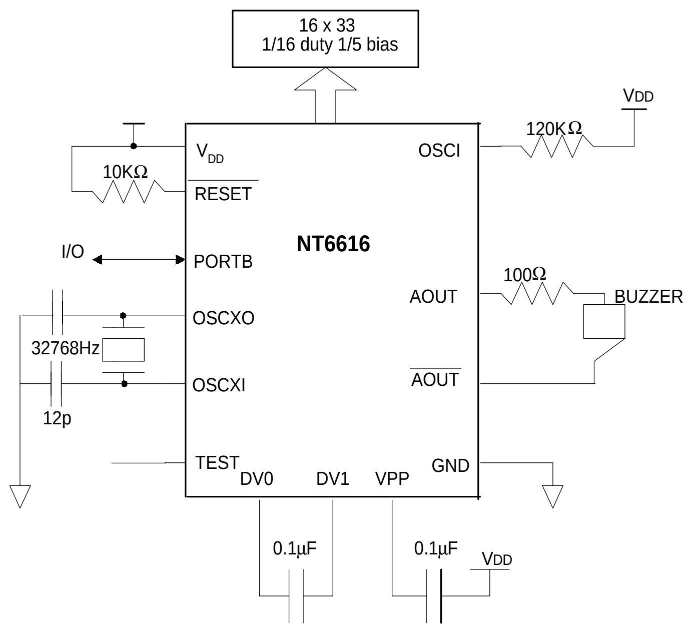
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	2.4	3.0	3.4	V	
Operating Current	I_{OP}		0.25	0.35	mA	V_{DD} = 3.0V, 32.768KHz OSC off, all output unloaded
Standby Current	I_{SB1}		1.5	2.5	µA	V_{DD} = 3.0V, Stop (RC OSC stop, Base Timer on , LCD off , all outputs unloaded)
Standby Current	I_{SB2}		0.7	1.2	µA	V_{DD} = 3.0V, Stop (OSC and 32.768KHz OSC off, Base Timer stop, LCD off , all outputs unloaded)
Input Current	I_I		6	35	µA	V_{DD} = 3.0V V(input) = 3.0V
Input High Voltage	V_{IH}	V_{DD}-0.5		V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	-0.3		GND+0.5	V	
Output Low Drive Current	I_{OL}	1.2			mA	PORTA and PORTB, V_{OL} = 0.5V
Output High Drive Current	I_{OH}	250			µA	PORTA, V_{OH} = V_{DD} -0.5V
AOUT, $\overline{AOUT}$ Output Current	I_{OH} I_{OL}	1.2 1.2			mA mA	V_{OUT} = V_{DD} -0.6V V_{OUT} = 0.5V
LCD Lighting	I_{LCD}		15.0	17.0	µA	V_{DD} = 3.0V, LCD on current, (LCDI1, LCDI0) = (0,0), no Pump. (For reference only)
LCD Lighting	I_{LCD}		25.0	35.0	µA	V_{DD} = 3.0V, LCD on current, (LCDI1, LCDI0) = (0,0), Pump enable. (For reference only)
Pull-up Resistance	R_{PU}		20	100	KΩ	PORTB

Typical RC oscillator Resistor vs. OSC frequence : (Reference only)

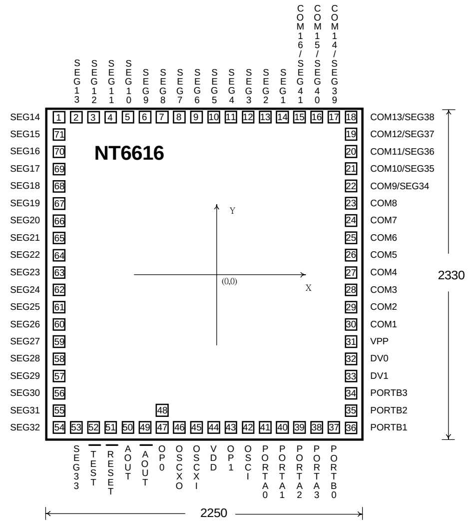




Application Circuit **(for reference only)**



Bonding Diagram



* Substrate connect to GND

unit: µm

Pad No	Designation	X	Y	Pad No	Designation	X	Y
1	SEG[14]	-1049.55	1092.60	37	PORTB0	908.05	-1092.60
2	SEG[13]	-908.05	1092.60	38	PORTA3	773.05	-1092.60
3	SEG[12]	-773.10	1092.60	39	PORTA2	648.05	-1092.60
4	SEG[11]	-648.10	1092.60	40	PORTA1	533.05	-1092.60
5	SEG[10]	-523.10	1092.60	41	PORTA0	413.05	-1092.60
6	SEG[9]	-397.60	1092.60	42	OSCI	293.05	-1092.60
7	SEG[8]	-281.95	1092.60	43	OP1	165.10	-1092.60
8	SEG[7]	-166.95	1092.60	44	VCC	65.05	-1092.60
9	SEG[6]	-51.95	1092.60	45	OSCXI	-49.95	-1092.60
10	SEG[5]	63.05	1092.60	46	OSCXO	-164.95	-1092.60
11	SEG[4]	178.05	1092.60	47	GND	-279.95	-992.60
12	SEG[3]	293.05	1092.60	48	OP0	-279.95	-1092.60
13	SEG[2]	408.05	1092.60	49	AOUT	-521.10	-1092.60
14	SEG[1]	528.05	1092.60	50	$\overline{\text{AOUT}}$	-395.60	-1092.60
15	COM[16]	648.05	1092.60	51	$\overline{\text{RESET}}$	-648.10	-1092.60
16	COM[15]	773.05	1092.60	52	$\overline{\text{TEST}}$	-773.10	-1092.60
17	COM[14]	908.05	1092.60	53	SEG[33]	-908.05	-1092.65
18	COM[13]	1049.05	1092.60	54	SEG[32]	-1049.55	-1092.60
19	COM[12]	1049.05	951.60	55	SEG[31]	-1049.55	-951.60
20	COM[11]	1049.05	816.55	56	SEG[30]	-1049.55	-818.45
21	COM[10]	1049.05	696.55	57	SEG[29]	-1049.55	-698.45
22	COM[9]	1049.05	576.55	58	SEG[28]	-1049.55	-578.45
23	COM[8]	1049.05	461.55	59	SEG[27]	-1049.55	-458.45
24	COM[7]	1049.05	346.55	60	SEG[26]	-1049.55	-343.45
25	COM[6]	1049.05	231.55	61	SEG[25]	-1049.55	-228.45
26	COM[5]	1049.05	116.55	62	SEG[24]	-1049.55	-113.45
27	COM[4]	1049.05	1.55	63	SEG[23]	-1049.55	1.55
28	COM[3]	1049.05	-113.45	64	SEG[22]	-1049.55	116.55
29	COM[2]	1049.05	-228.45	65	SEG[21]	-1049.55	231.55
30	COM[1]	1049.05	-343.45	66	SEG[20]	-1049.55	346.55
31	VPP	1049.05	-458.45	67	SEG[19]	-1049.55	461.55
32	DV0	1049.05	-578.45	68	SEG[18]	-1049.55	576.55
33	DV1	1049.05	-698.45	69	SEG[17]	-1049.55	696.55
34	PORTB3	1049.05	-818.45	70	SEG[16]	-1049.55	816.55
35	PORTB2	1049.05	-951.60	71	SEG[15]	-1049.55	951.55
36	PORTB1	1049.05	-1092.60				

Ordering Information

Part No.	Package
NT6616H	CHIP FORM