

MM3474 series application note

Outline

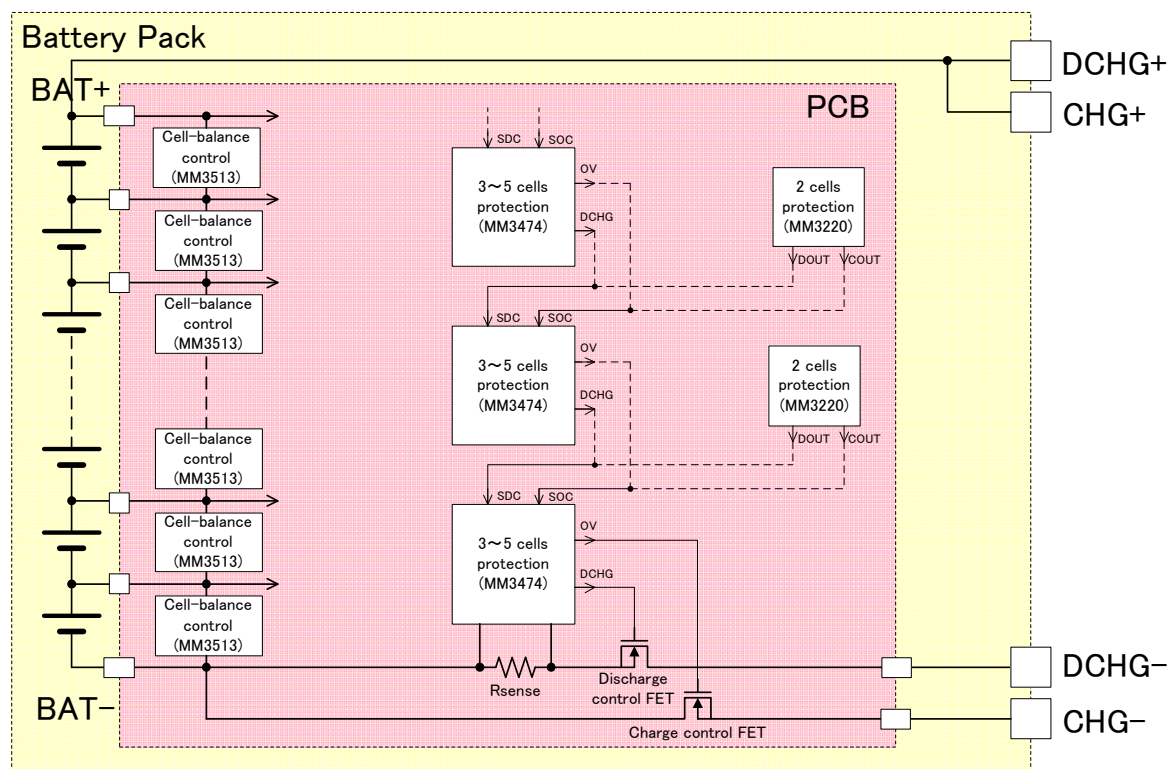
MM3474 series is an overcharge, overdischarge and overcurrent protection IC for a lithium-ion / lithium-polymer secondary battery. This supports 3 to 5 serial cells, and the number of cells can be switched over by inputting high / low signal to SEL terminal. MM3474 series can protect Lithium ion battery pack of 6-plus serial cells by connecting in cascade. This also provides the control terminals of output overdischarge detection (SDC) and output overcharge detection (SOC), which allows configuring an application with fewer external parts for 6 or more cells connected in series.

We provide many kinds of optional ICs of MM3474 series, which are customizable for the usage by selecting optional functions.

Low cost and small size configuration can be achieved when MM3474 series is combined with MM3220V series which is 2 cells protection IC and used for the applications of 6 cells or 7 cells, etc.

Cell balance control function can be added when MM3513 series which is cell balance control IC is used.

This application note is a reference material which describes representative examples of connection and cautions of designing for the applications which use MM3474 series, main characteristics and related products of MM3474 series. Please refer the data sheets for the details and specifications of this product.



Multi-cell protection circuit which uses MM3474 series and related products

Table of contents

Outline	-----	P1
Table of contents	-----	P2~4
1. Function outline of MM3474 series	-----	P5~6
1-1. Overcharge detection function	-----	P5
1-2. Overdischarge detection function	-----	P5
1-3. Overcurrent and short detection function	-----	P5
1-4. Switching function of 3 to 5 cells protection	-----	P6
1-5. Setting function of dead zone time	-----	P6
1-6. Communication function in cascade arrangement	-----	P6
2. Block diagram	-----	P7~8
2-1. Overdischarge release: "Voltage release" type	-----	P7
2-2. Overdischarge release: "Load release + voltage release" type	-----	P8
3. Explanation of PIN configuration and terminal	-----	P9
4. Package outline and recommended land pattern	-----	P10
5. Electric characteristics	-----	P11~12
6. Dead zone time characteristics	-----	P13
7. Temperature characteristics of main items	-----	P14~17
7-1. Current consumption	-----	P14
7-2. Overcharge detection voltage	-----	P15
7-3. Overdischarge detection voltage	-----	P16
7-4. Overcurrent detection voltage, short detection voltage and dead zone time of each detection	-----	P17
8. Timing chart	-----	P18~21
8-1. Overcharge detection and release operation	-----	P18
8-2. Overdischarge detection and release operation ... Overdischarge release: "Voltage release" type	-----	P19
8-3. Overdischarge detection and release operation ... Overdischarge release: "Load release+Voltage release" type	-----	P20
8-4. Overcurrent detection, short detection and release operation	-----	P21
9. Explanation of external parts	-----	P22
10. Examples of application circuit	-----	P23~48
* For the list of application circuit examples, please refer to the page 4.		
11. Selecting methods	-----	P49~51
12. Instruction and directions for use	-----	P52
13. Products line up list	-----	P53~54

Table of contents

14. Introduction of releted products ----- P55～56

14-1. MM3220V series :Overcharge and overdischarge protection IC ----- P55
for 2 cells lithium-ion battery

14-2. MM3513 series :Li-ion battery cell balance control IC ----- P56

15. Circuit examples which use related products ----- P57～66

* For the detail of application circuit examples, please refer to the list on page 4.

16. Line up list of related products ----- P67～68

17. Instruction and direction ----- P69

18. Related materials ----- P69

Table of contents

List of application circuit examples

Number of cells	Charge / discharge route	Over discharge release method *1	Configuration of protect IC	Optional function *2	Page
				cell balance	
3cells	separate	Non Latch	3cells protection	-	P23
	common	Non Latch	3cells protection	-	P24
4cells	separate	Non Latch	4cells protection	-	P25
	common	Non Latch	4cells protection	-	P26
5cells	separate	Non Latch	5cells protection	-	P27
	common	Non Latch	5cells protection	-	P28
	separate	Non Latch	5cells protection	○	P65
6cells	separate	Non Latch	3cells protection+3cells protection	-	P29
	separate	Latch	3cells protection+3cells protection	-	P30
	separate	Non Latch	4cells protection+2cells protection	-	P57
	separate	Latch	4cells protection+2cells protection	-	P58
7cells	separate	Non Latch	4cells protection+3cells protection	-	P31
	separate	Latch	4cells protection+3cells protection	-	P32
	separate	Non Latch	5cells protection+2cells protection	-	P59
	separate	Latch	5cells protection+2cells protection	-	P60
8cells	separate	Non Latch	4cells protection+4cells protection	-	P33
	separate	Latch	4cells protection+4cells protection	-	P34
9cells	separate	Non Latch	4cells protection+5cells protection	-	P35
	separate	Latch	4cells protection+5cells protection	-	P36
10cells	separate	Non Latch	5cells protection+5cells protection	-	P37
	common	Non Latch	5cells protection+5cells protection	-	P38
	separate	Latch	5cells protection+5cells protection	-	P39
	common	Latch	5cells protection+5cells protection	-	P40
	separate	Non Latch	5cells protection+5cells protection	○	P66
12cells	separate	Non Latch	4cells protection+4cells protection+4cells protection	-	P41
	separate	Latch	4cells protection+4cells protection+4cells protection	-	P42
	separate	Non Latch	5cells protection+5cells protection+2cells protection	-	P61
	separate	Latch	5cells protection+5cells protection+2cells protection	-	P62
13cells	separate	Non Latch	4cells protection+4cells protection+5cells protection	-	P43
	separate	Latch	4cells protection+4cells protection+5cells protection	-	P44
14cells	separate	Non Latch	4cells protection+5cells protection+5cells protection	-	P45
	separate	Latch	4cells protection+5cells protection+5cells protection	-	P46
16cells	separate	Non Latch	4cells protection+4cells protection+4cells protection+4cells protection	-	P47
	separate	Latch	4cells protection+4cells protection+4cells protection+4cells protection	-	P48
	separate	Non Latch	4cells protection+5cells protection+5cells protection+2cells protection	-	P63
	separate	Latch	4cells protection+5cells protection+5cells protection+2cells protection	-	P64

- ※1 Non Latch : Voltage release
Latch : Load release + Voltage release
※2 ○ : Equipped with the function
- : Not equipped with the function

1. Function outline of MM3474 series

1-1. Overcharge detection function

If any of the cells from V1 to V5 exceed the overcharge detection voltage, charging can be stopped by outputting "Hi impedance" from the OV output pin connecting an external pulldown resistor and turning off the charge control Nch MOS FET after the dead time set depending on values of the capacitor connecting to the COV pin. If all the cells from V1 to V5 drop below the overcharge release voltage, high level is output from the OV output pin and the overcharge detection state returns to the normal state.

Range and accuracy of detection/release voltage

- | | | |
|--------------------------------|--------------------------|--|
| • Overcharge detection voltage | 3.6V to 4.5V, 5mV steps | Accuracy±25mV (T _{opr} =±0~+50°C) |
| • Overcharge release voltage | 3.4V to 4.5V, 50mV steps | Accuracy±50mV |

1-2. Overdischarge detection function

If any of the cells from V1 to V5 drop below the overdischarge detection voltage, discharging can be stopped by outputting low level from the DCHG output pin and turning off the charge control Nch MOS FET after the dead time set depending on values of the capacitor connecting to the CDC pin.

As for the return methods from a overdischarge state to the normal state, choice is possible from two kinds of "voltage release" and "load release".

When all cells of the V1 cell - V5 cell become than the discharge reopening voltage with the IC of voltage release", output "H" level from DCHG output terminal and return to the normal state from the overdischarge detection state.

When all cells of load opening and V1 - V5 become than the discharge reopening voltage with the IC of "load release + voltage release", output "H" level from DCHG output terminal and usually return to the normal state from the overdischarge state.

Range and accuracy of detection/release voltage

- | | | |
|-----------------------------------|--------------------------|----------------|
| • Overdischarge detection voltage | 2.0V to 3.0V, 50mV steps | Accuracy±80mV |
| • Overdischarge release voltage | 2.0V to 3.4V, 50mV steps | Accuracy±100mV |

1-3. Discharge overcurrent / short detection function

In a dischargeable state, it becomes a overcurrent detection state if the CS pin voltage exceeds the overcurrent detection voltage and drops below the short detection voltage due to load short, etc. If the CS pin voltage exceeds the short detection voltage, it becomes a short detection state. If overcurrent and short are detected, discharging can be stopped by outputting low level from the DCHG output pin and turning off the charge control Nch MOS FET after the dead time set depending on values of the capacitor connecting to the COL1 pin. The release from the overcurrent and short detection states is done by load removal. After load removal, if the V- pin voltage drops below its threshold voltage due to pulldown resistance in the IC, high level is output from the DCHG output pin and the overcurrent and short detection state returns to the normal state.

Range and accuracy of detection

- | | | |
|------------------------------|--------------------------|----------------|
| • Overcurrent detect voltage | 50mV to 300mV, 5mV steps | Accuracy±15mV |
| • Short detection voltage | 0.2V to 1.0V, 50mV steps | Accuracy±100mV |

1. Function outline of MM3474 series

1-4. 3-, 4-, 5-cell protection switching function

The 3-, 4-, or 5-cell protection can be switched by connecting the SEL1 pin and SEL2 pin to the VDD or VSS2 via a protection resistor. At the time of 4-cell protection, the operation of the overcharge detection circuit and overdischarge detection circuit for the V1 cell is stopped. Therefore, short-circuit the V1 pin and VSS1 pin before use. At the time of 3-cell protection, the operation of overcharge detection circuit and overdischarge detection circuit for V1 and V2 Cell is stopped. Therefore, short-circuit the V2 pin, V1 pin and VSS1 pin before use.

SEL1 pin	SEL2 pin	MM3474 Setting
High (VDD)	High (VDD)	5 cell prptection
High (VDD)	Low (VSS2)	4 cell prptection
Low (VSS2)	High (VDD)	3 cell prptection
Low (VSS2)	Low (VSS2)	prohibite

1-5.Setting function of the dead time

The MM3474 series sets overcharge detection / release dead time,overdischarge detection / release dead time,overcurrent detection / release dead time with a value of the attaching externally capacity and can change dead time by changing the fixed number of the capacity.

Range of detection delay time

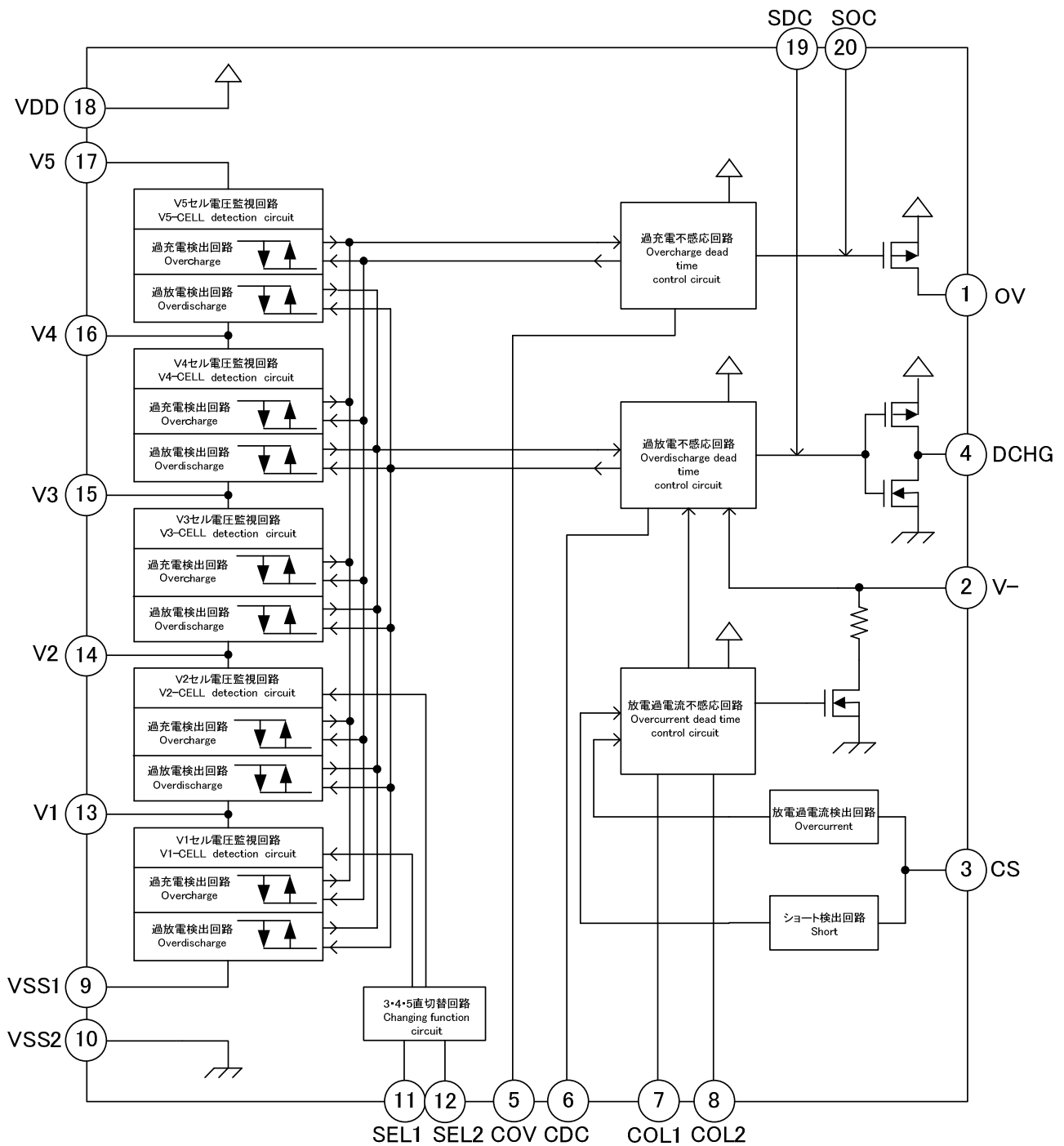
- | | |
|--|---|
| • Overcharge detection/release dead time | Setting by a capacitor of COV pin. Accuracy±50% |
| | Detection dead time : release dead time can be set from 1:10 to 10:1. |
| • Overdischarge detection voltage | Setting by a capacitor of CDC pin. Accuracy±50% |
| • Overdischarge release dead time | Max.15msec fixed |
| • Overcurrent dead time | Setting by a capacitor of COL1 pin. Accuracy±50% |
| • Overcurrent dead time | Setting by a capacitor of COL2 pin. Accuracy±50% |
| • Short detection dead time | 300usec fixed |

1-6.Communication function when cascade connected

When using a cascade-connected IC with 6 or more cell protection, an overdischarge detection signal can be transmitted by inputting the DCHG output pin signal to the SDC pin via a resistor. If the current input to the SDC pin exceeds the SDC release current, it is recognized as normal state. If it drops below the SDC detection current or if it is open, it is recognized as overdischarge detection state. In the same way, an overdischarge detection signal can be transmitted by inputting the OV output pin signal to the SOC pin via a resistor. In addition, charge / discharge is more controllable than inputting a signal into SDC terminal, SOC terminal from the outside independently

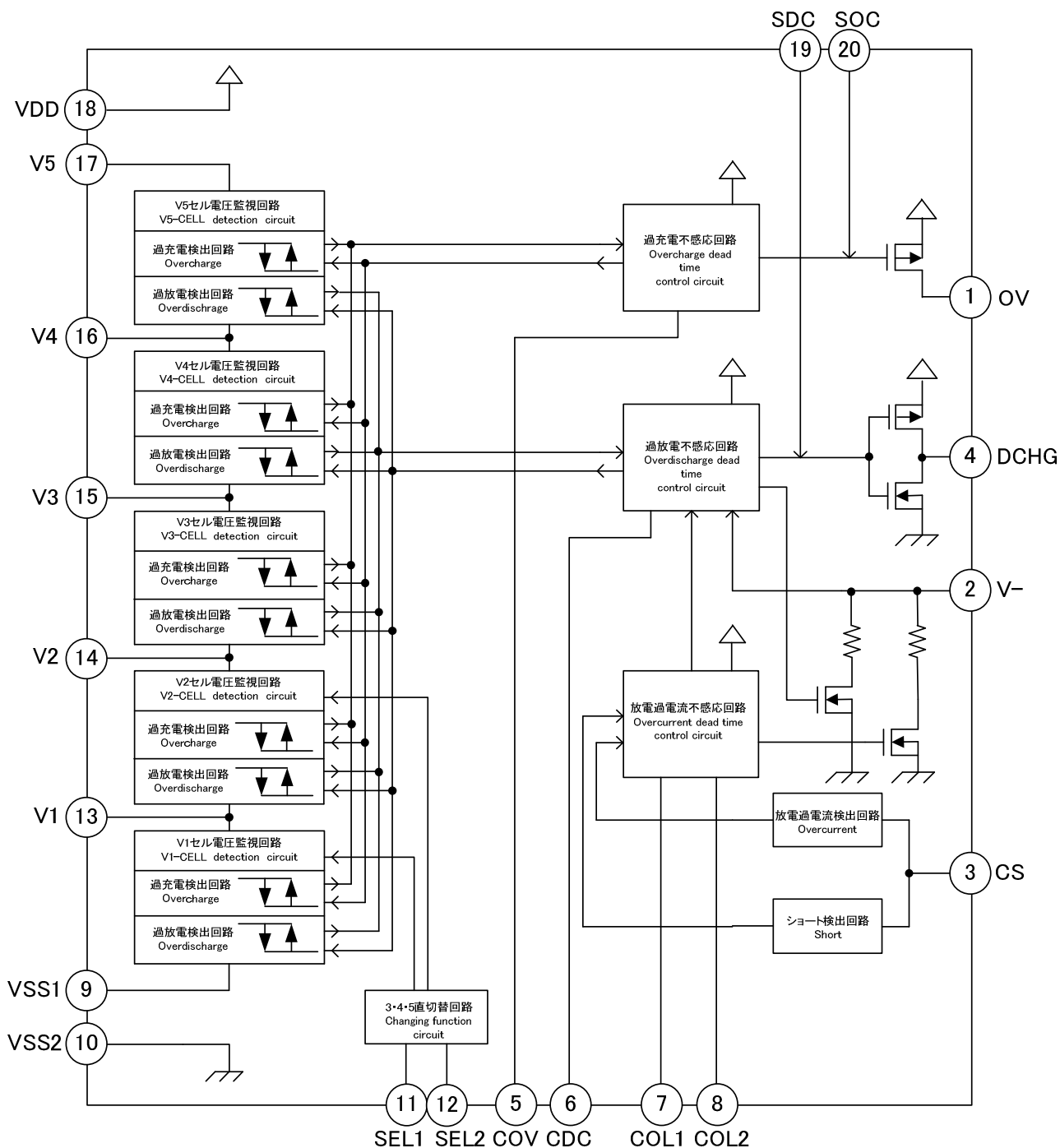
2. Block diagram

2-1. Overdischarge release : 「Voltage release」 type



2. Block diagram

2-2. Overdischarge release : 「Load release + Voltage release」 type



3. Explanation of PIN configuration and

Pin No.	Pin No.	Function
1	OV	Charge control output terminal. Output type is Pch open drain. Active "Hi impedance".
2	V-	Input terminal connected to charger negative voltage. Detected charger connection and load detection.
3	CS	Input of overcurrent detection. The voltage of the sense resistance is observed, and the overcurrent is detected.
4	DCHG	Discharge control output terminal. Output type is CMOS. Active "Low".
5	COV	This pin is dead time setting of overcharge detection and release.
6	CDC	This pin is dead time setting of overdischarge detection and release.
7	COL1	This pin is dead time setting of overcurrent detection.
8	COL2	This pin is dead time setting of overcurrent release.
9	VSS1	The input terminal of the negative voltage of V1 cell .
10	VSS2	The input terminal of the ground of IC.
11	SEL1	This pin is for changing function for 3cell in series or 4cell in series , 5cell in series. SEL1 = H , SEL2 = H → 5Cell protection SEL1 = H , SEL2 = L → 4Cell protection SEL1 = L , SEL2 = H → 3Cell protection (SEL1=SEL2=L setting is prohibited.)
12	SEL2	
13	V1	The input terminal of the positive voltage of V1 cell, and the negative voltage of V2 cell .
14	V2	The input terminal of the positive voltage of V2 cell, and the negative voltage of V3 cell .
15	V3	The input terminal of the positive voltage of V3 cell, and the negative voltage of V4 cell .
16	V4	The input terminal of the positive voltage of V4 cell, and the negative voltage of V5 cell .
17	V5	The input terminal of the positive voltage of V5 cell .
18	VDD	The input terminal of the power supply of IC.
19	SDC	The control terminal of output over discharge detection. $I_{SDC} < I_{SDCL} \rightarrow DCHG = Low$
20	SOC	The control terminal of output over charge detection. $I_{SOC} < I_{SOCL} \rightarrow OV = Hi\ impedance$

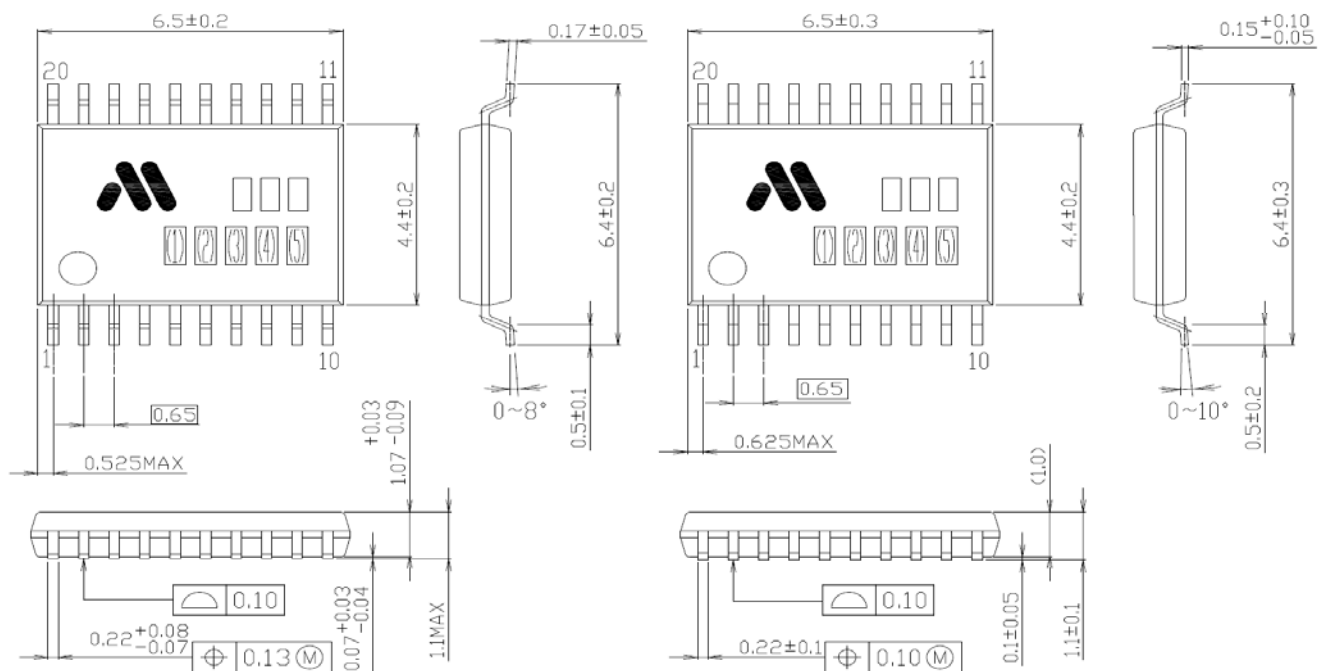
4. Package outline and recommended land

4-1. Package outline

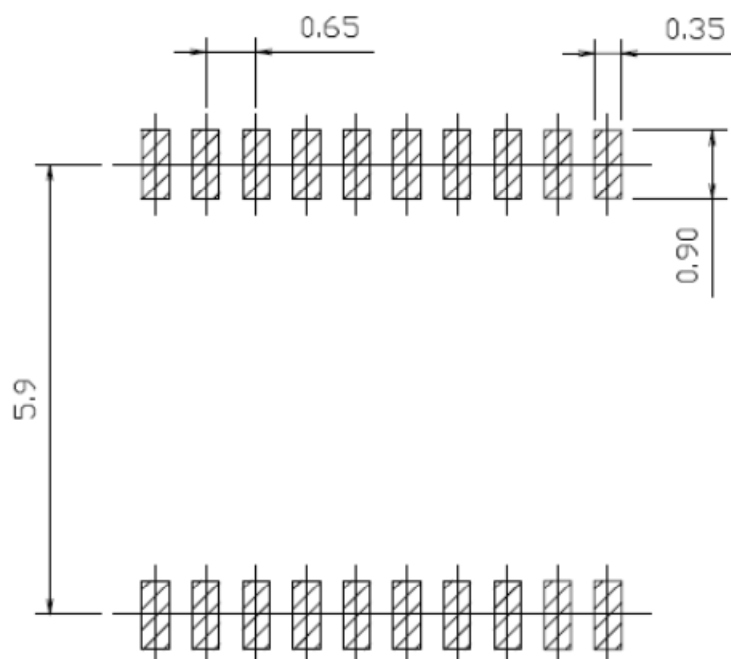
UNIT mm

TSOP-20C

TSOP-20D



4-2. Recommended land pattern



5. Electric characteristics

Unless otherwise specified, Topr=+25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	unit
ABSOLUTE MAXIMUM RATINGS						
VDD pin supply voltage	V_{VDDMAX}		VSS2-0.3	-	+30	V
V5 pin supply voltage	V_{V5MAX}		V4-0.3	-	VDD+0.3	V
Voltage between the input terminals of voltage of battery	$V_{CELLMAX}$		-0.3	-	+10	V
V- pin · OV pin supply voltage	$V_{V-MAX} \cdot V_{OVMAX}$		VDD-30	-	VDD+0.3	V
CS pin · DCHG pin supply voltage	$V_{CSMAX} \cdot V_{DCHGMAX}$		VSS2-0.3	-	VDD+0.3	V
SEL pin supply voltage	V_{SELMAX}		VSS2-0.3	-	VDD+0.3	V
SDC/SOCpin supply voltage	V_{SDCMAX}		VSS2-0.3	-	VDD+0.3	V
Storage temperature	Tstg		-55	-	+125	°C
Power dissipation	Pd		-	-	300	W
RECOMMENDED OPERATING CONDITIONS						
Operating Temperature	TOPR		-40.0	-	+85	°C
Supply Voltage	VOPR		VSS2+3.5	-	VSS2+22.5	V
CURRENT CONSUMPTION						
Consumption current1 (Vdd)	I_{DD1}	$V_{CELL}=4.4V$	-	10.0	20.0	uA
Consumption current2 (Vdd)	I_{DD2}	$V_{CELL}=3.5V$	-	5.0	10.0	uA
Consumption current3 (Vdd)	I_{DD3}	$V_{CELL}=1.8V$	-	1.5	3.0	uA
Consumption current1 (V5)	I_{1V5}	$V_{CELL}=4.4V$	-	4.0	8.0	uA
Consumption current2 (V5)	I_{2V5}	$V_{CELL}=3.5V$	-	3.0	6.0	uA
Consumption current3 (V5)	I_{3V5}	$V_{CELL}=1.8V$	-	1.5	3.0	uA
V4·V3·V2·V1 input current	$I_{V4} \cdot I_{V3} \cdot I_{V2} \cdot I_{V1}$	$V_{CELL}=3.5V$	-	-	±300	nA
SEL input current	I_{SEL}	$V_{CELL}=3.5V$, SEL=VDD	-	0.5	1.0	uA
SDC input current	I_{SDC}	$V_{CELL}=3.5V$, $R_{SDC}=1M\Omega$	-	0.8	1.6	uA
SOC input current	I_{SOC}	$V_{CELL}=3.5V$, $R_{SDC}=1M\Omega$	-	0.8	1.6	uA
DETECTION/RELEASE VOLTAGE/CURRENT						
Overcharge detection voltage	V_{CELLU}	Ta=±0°C~+50°C	Typ-0.025	V_{CELLU}	Typ+0.025	V
Overcharge release voltage	V_{CELLO}		Typ-0.050	V_{CELLO}	Typ+0.050	V
Overdischarge detection voltage	V_{CELLS}		Typ-0.080	V_{CELLS}	Typ+0.080	V
Overdischarge release voltage	V_{CELLD}		Typ-0.100	V_{CELLD}	Typ+0.100	V
Overcurrent detection voltage	V_{OC}		Typ-0.015	V_{OC}	Typ+0.015	V
V- pin overcurrent release voltage	V_{VM}		Typ-0.030	V_{VM}	Typ+0.030	V
Short detection voltage	V_{SHORT}		Typ-0.100	V_{SHORT}	Typ+0.100	V
SDC detection current	I_{SDCL}	$V_{CELL}=3.5V$	-	-	0.1	uA
SDC release current	I_{SDCH}	$V_{CELL}=3.5V$	0.5	-	-	uA
SOC detection current	$I_{SOC L}$	$V_{CELL}=3.5V$	-	-	0.1	uA
SOC release current	$I_{SOC H}$	$V_{CELL}=3.5V$	0.5	-	-	uA
DETECTION DEAD TIME						
※1 Overcharge detection dead time	t_{OV1}	$C_{COV}=0.1\mu F$	0.50	1.00	1.50	sec
※1 Overcharge release dead time	t_{OV2}	$C_{COV}=0.1\mu F$	0.05	0.10	0.15	sec
※1 Overdischarge detection dead time	t_{DC1}	$C_{CDC}=0.1\mu F$	0.50	1.00	1.50	sec
※1 Overdischarge release dead time	t_{DC2}	$C_{CDC}=0.1\mu F$	-	-	15.0	msec
※1 Overcurrent detection dead time	t_{OC1}	$C_{COL1}=0.001\mu F$	5.0	10.0	15.0	msec
※1 Overcurrent release dead time	t_{OC2}	$C_{COL2}=0.001\mu F$	5.0	10.0	15.0	msec
Short detection dead time	t_{SHORT}		100	300	600	usec

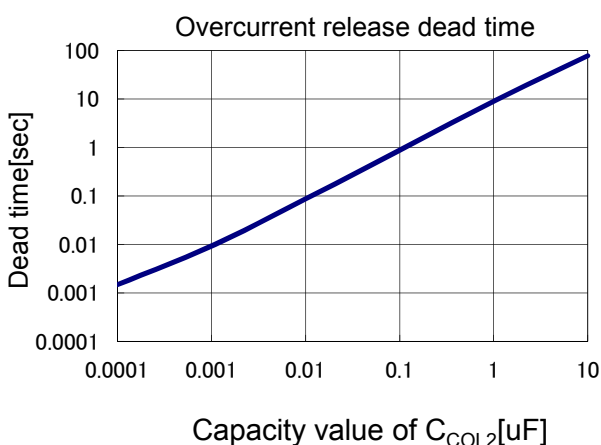
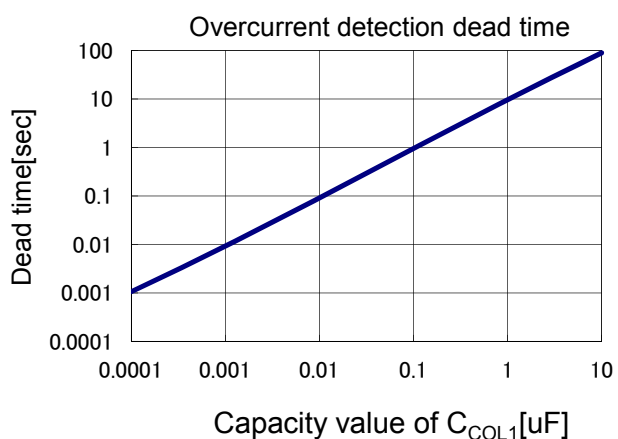
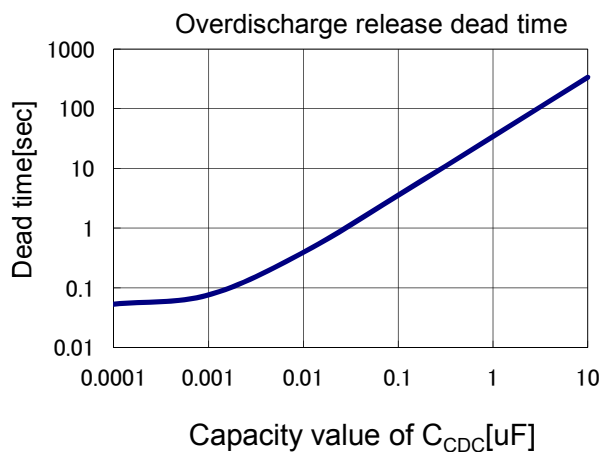
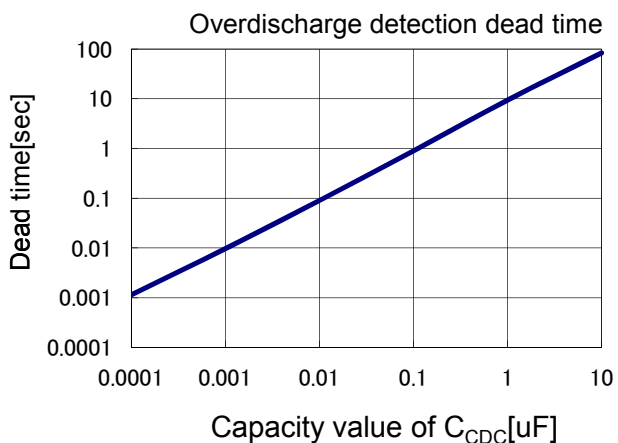
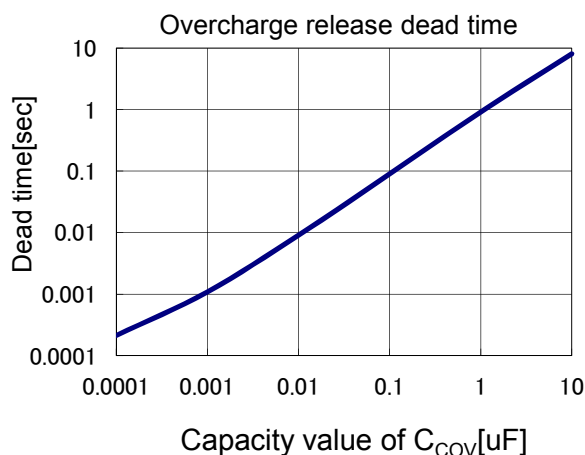
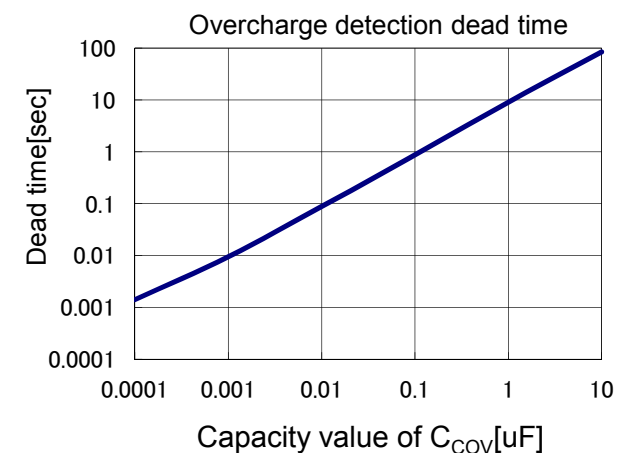
※1Dead time can be set by external capacitor.

5. Electric characteristics

Unless otherwise specified, Topr=+25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	unit
OUTPUT PIN / SEL PIN						
DCHG source current	$I_{SO}D_{CHG}$	$V_{DCHG}=VDD-0.5V$	-	-	-20	uA
DCHG sink current	$I_{SI}D_{CHG}$	$V_{DCHG}=0.5V$	20	-	-	uA
DCHG output voltage H	$V_{TH}D_{CH}$	$I_{SO}=-20uA$	VDD-0.5	-	-	V
DCHG output voltage L	$V_{TH}D_{CL}$	$I_{SI}=20uA$	-	-	0.5	V
OV source current	$I_{SO}O_V$	$V_{OV}=VDD-0.5V$	-	-	-20	uA
Ov leak current	$I_{LEAK}O_V$	$V_{OV}=VSS2$	-	-	0.1	uA
SEL input voltage L	$V_{SEL}L$		-	-	0.5	V
SEL input voltage H	$V_{SEL}H$		VDD-0.5	-	-	V
V- pin pulldown resistance	V_{PD}	$V_{CELL}=3.5v$, $V_{-}=1V$	15	30	60	kΩ

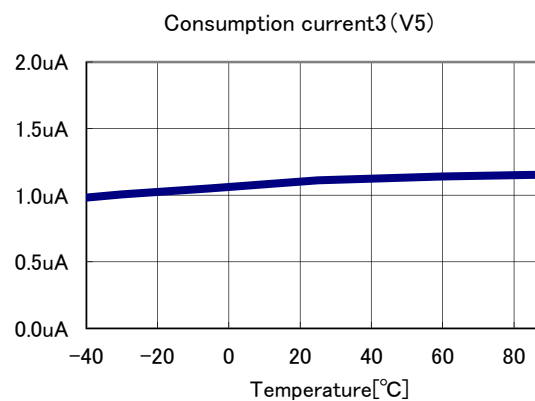
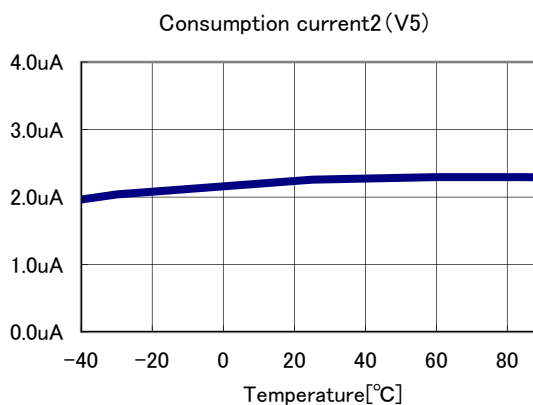
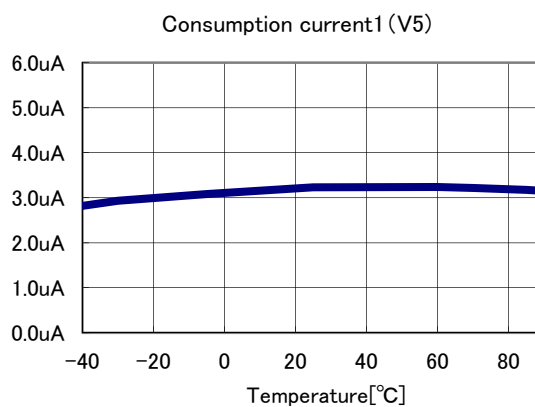
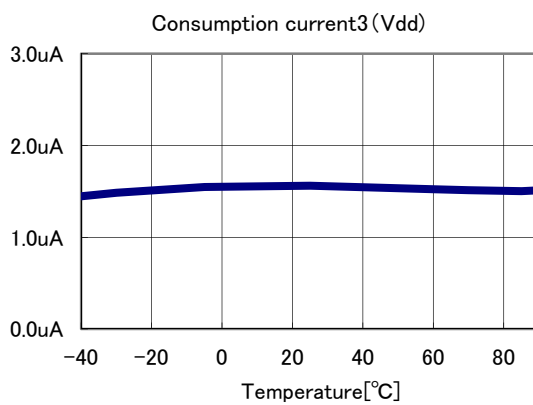
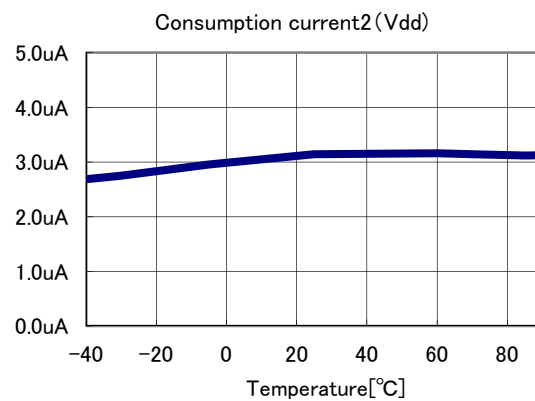
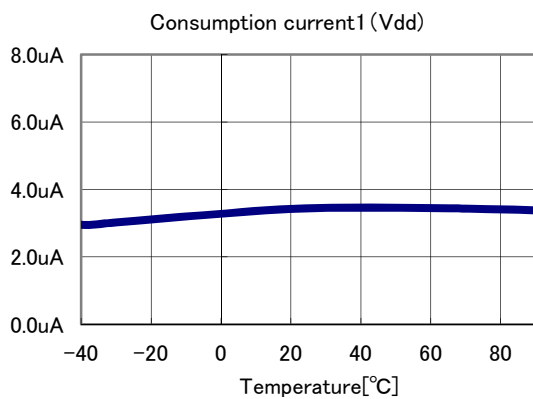
6. Dead time characteristic



Please refer to the matters that require attention listing in P45 - P46 [11.Instruction and directions for use].

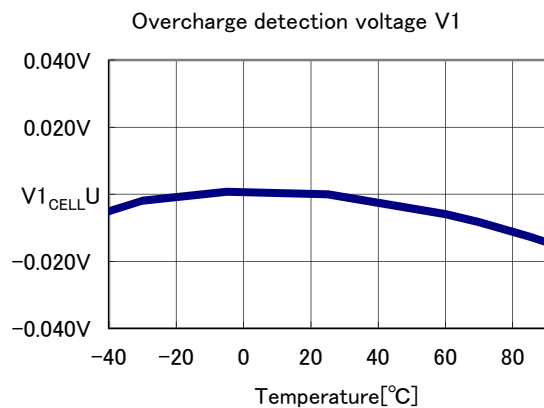
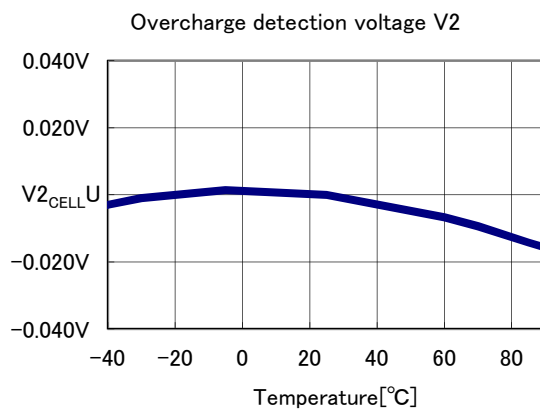
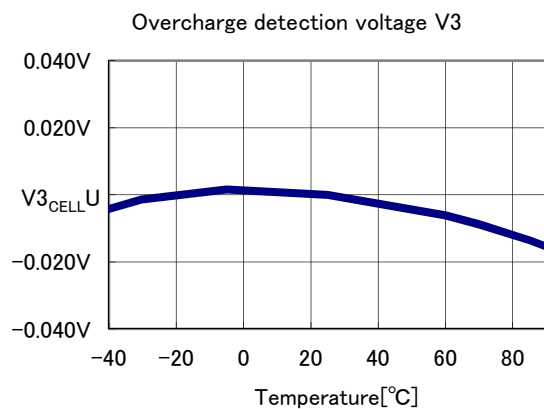
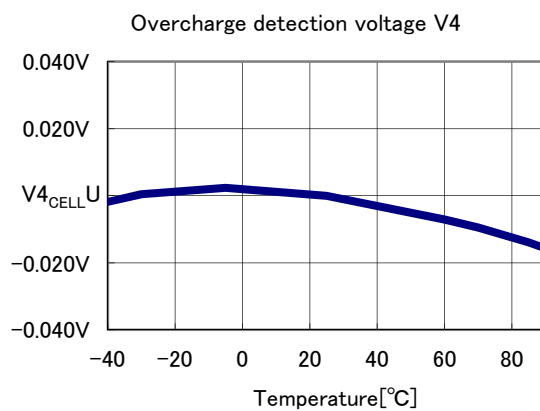
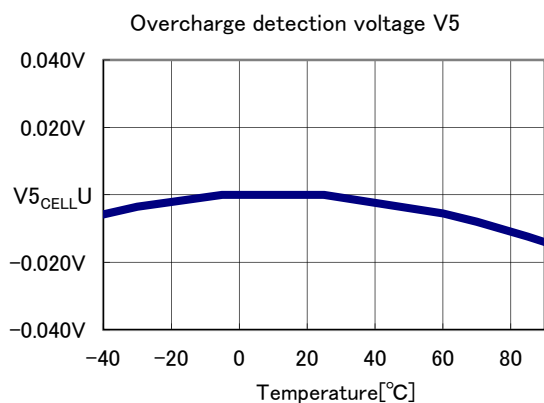
7. Temperature character of main parameter

7-1. Consumption current



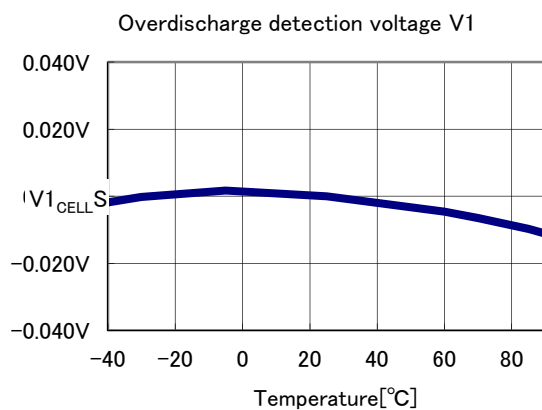
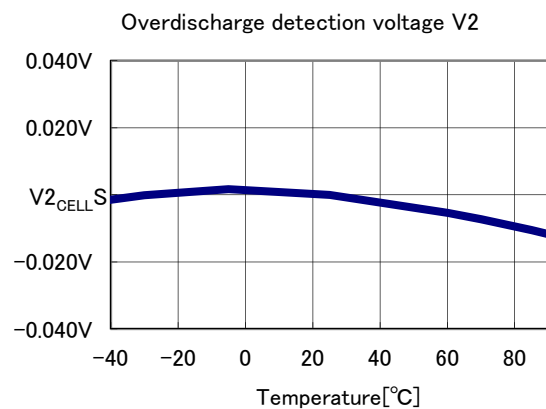
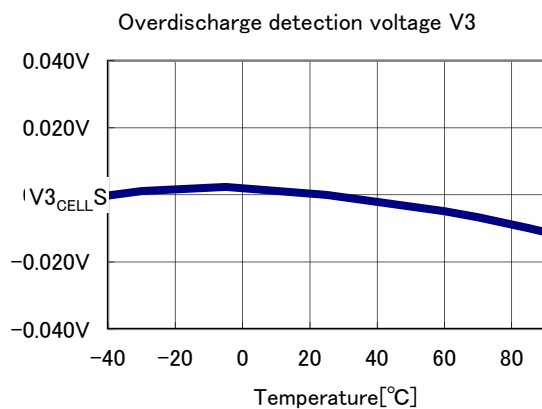
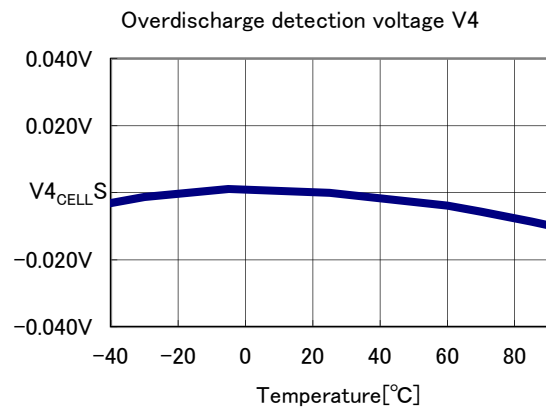
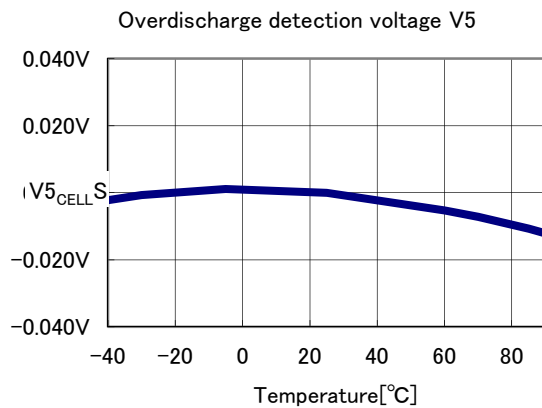
7. Temperature character of main parameter

7-2. Overcharge detection voltage



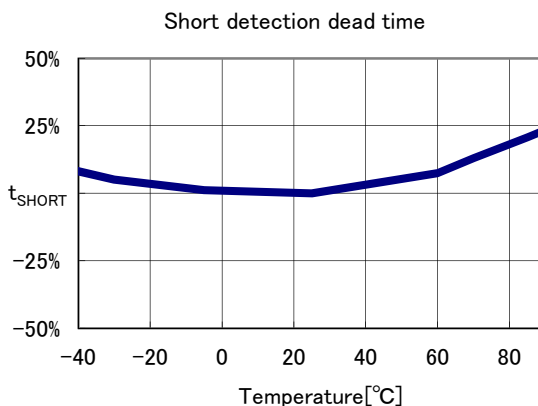
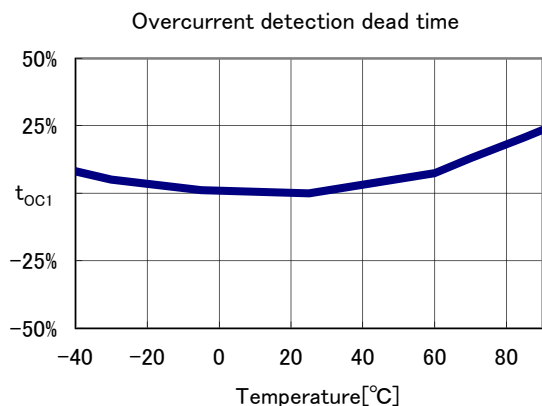
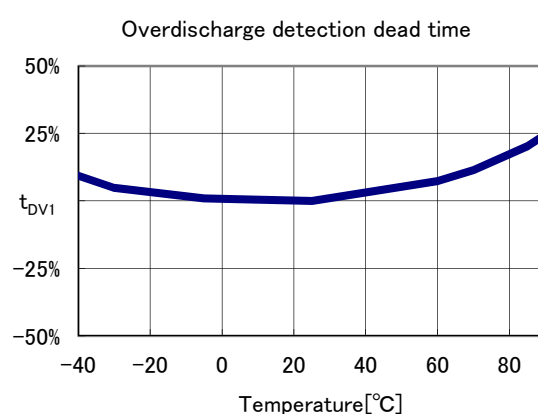
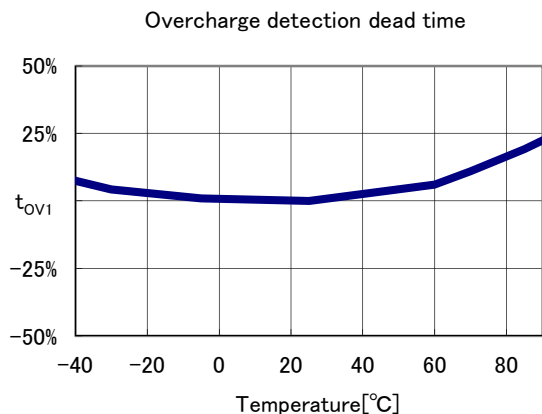
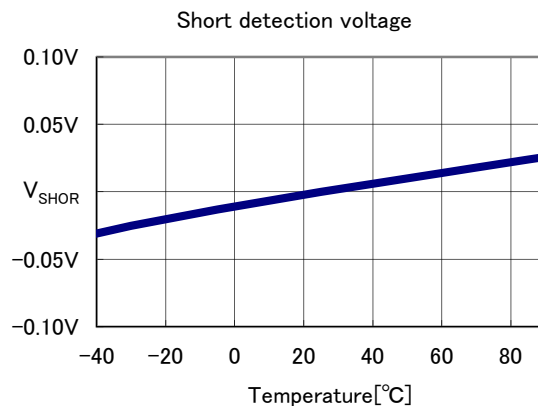
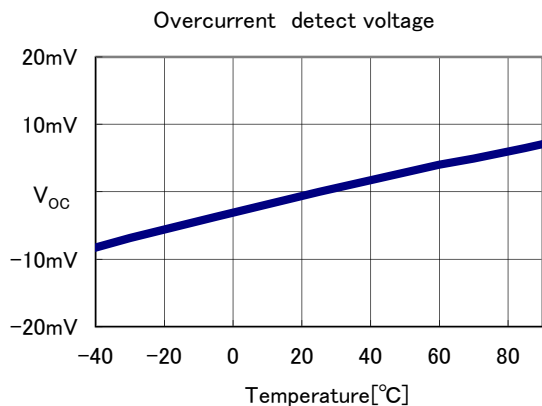
7. Temperature character of main parameter

7-3. Overdischarge detection voltage



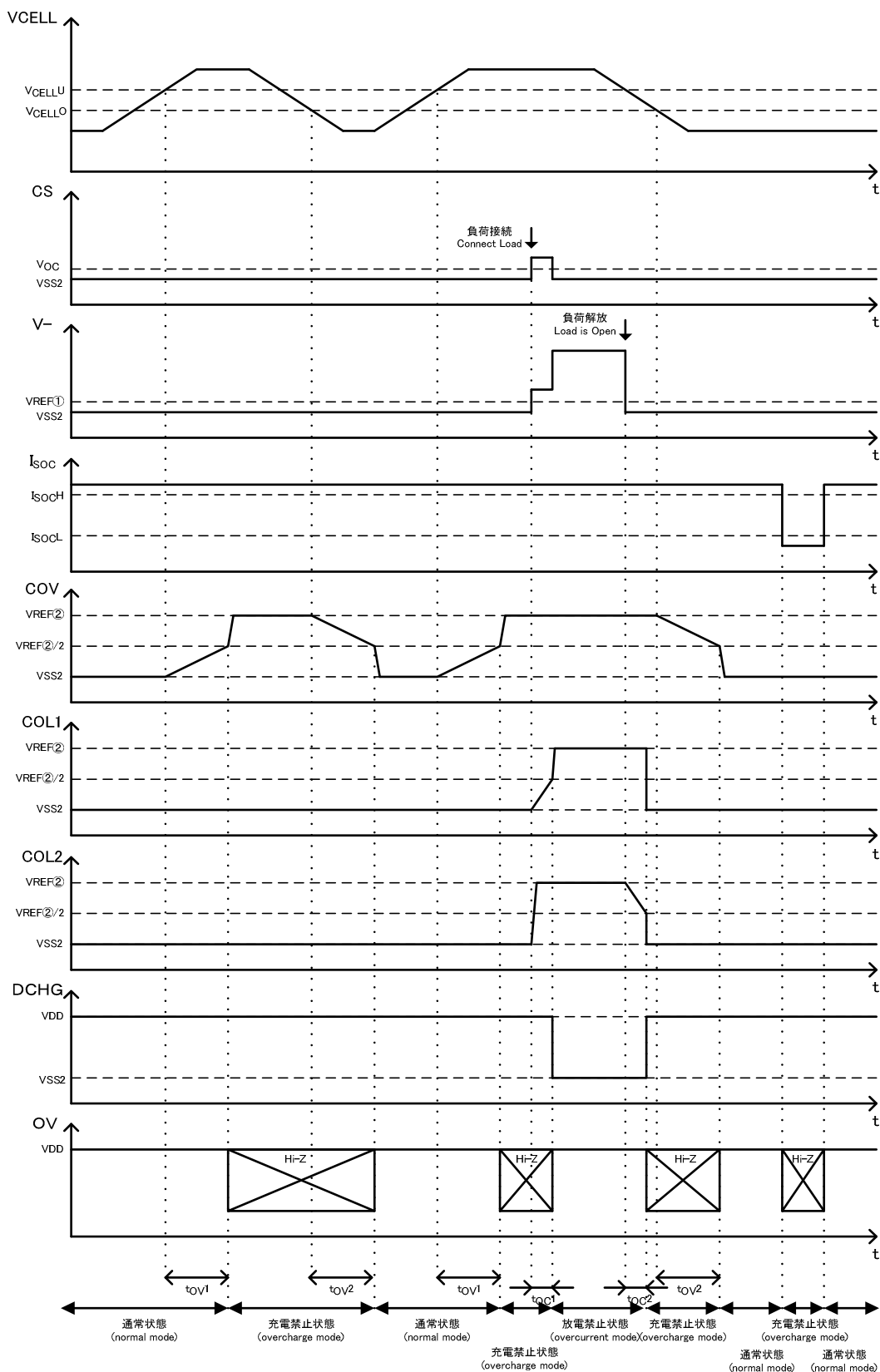
7. Temperature character of main parameter

7-4. Overcurrent detect voltage、Short detection voltage、Dead time



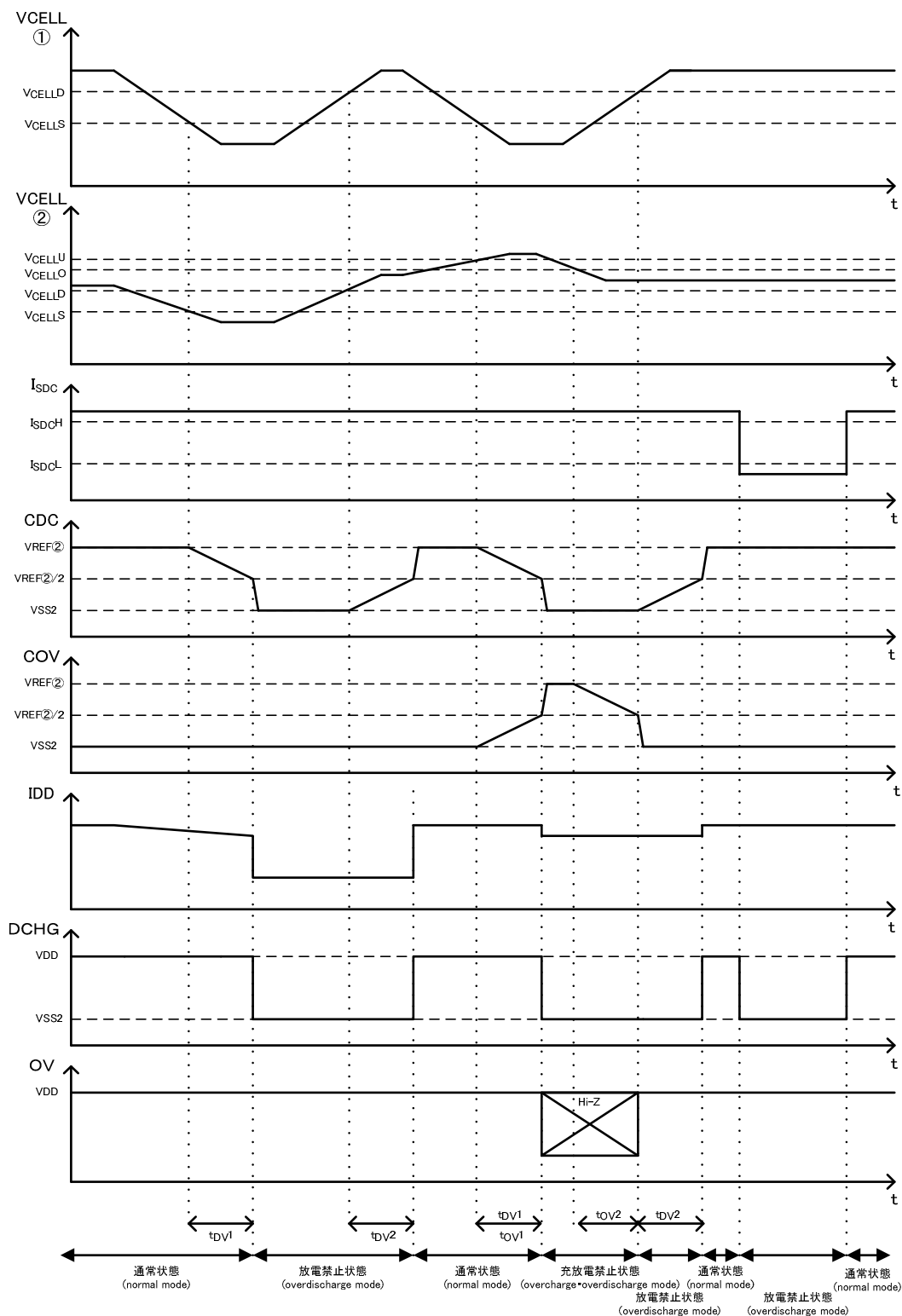
8. Timing chart

8-1. Overcurrent detection / release function



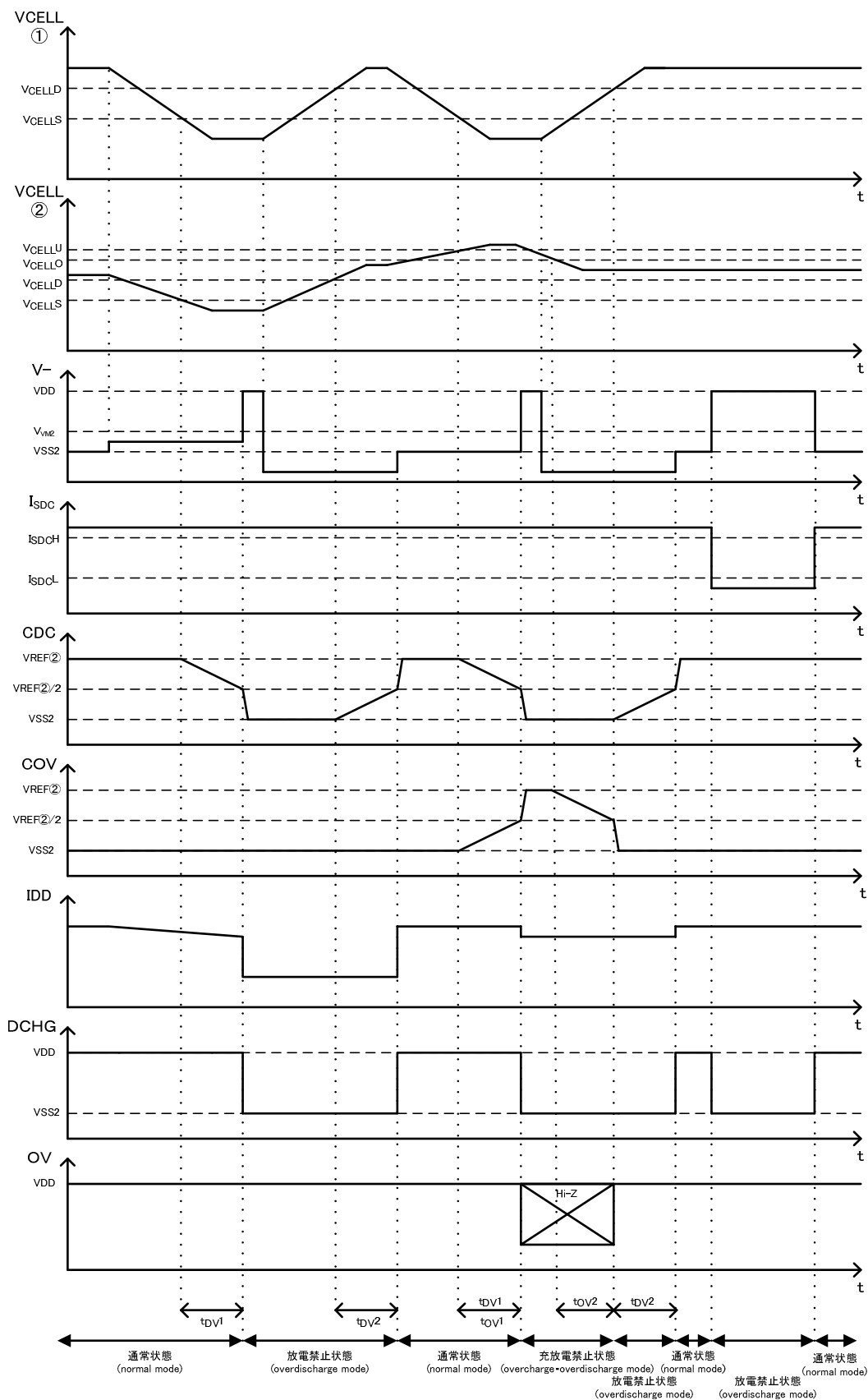
8. Timing chart

8-2. Overdischarge detection and release operation ... Overdischarge release: "Voltage release"



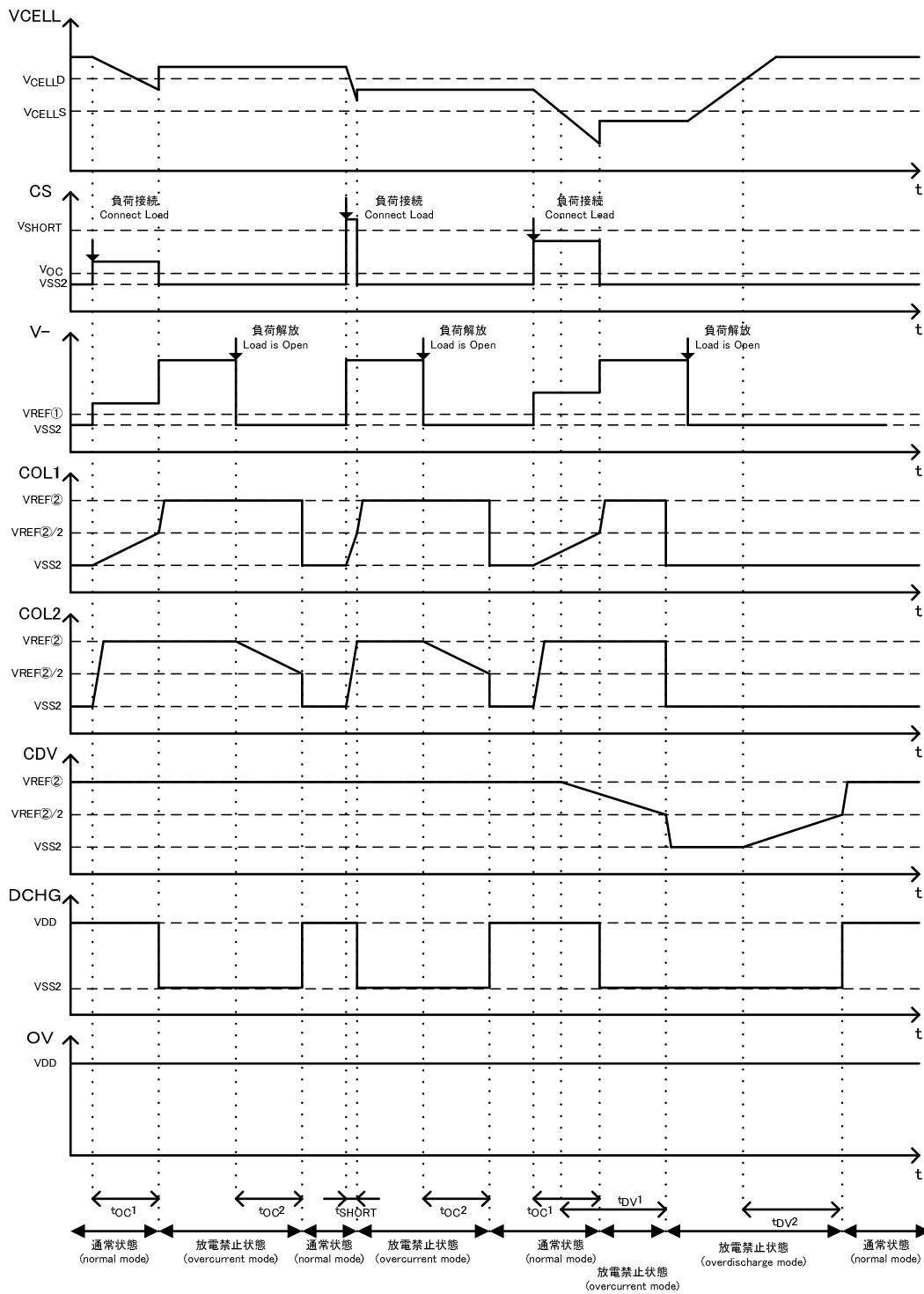
8. Timing chart

8-3.Overdischarge detection and release operation... Overdischarge release: "Load release+Voltage release" type

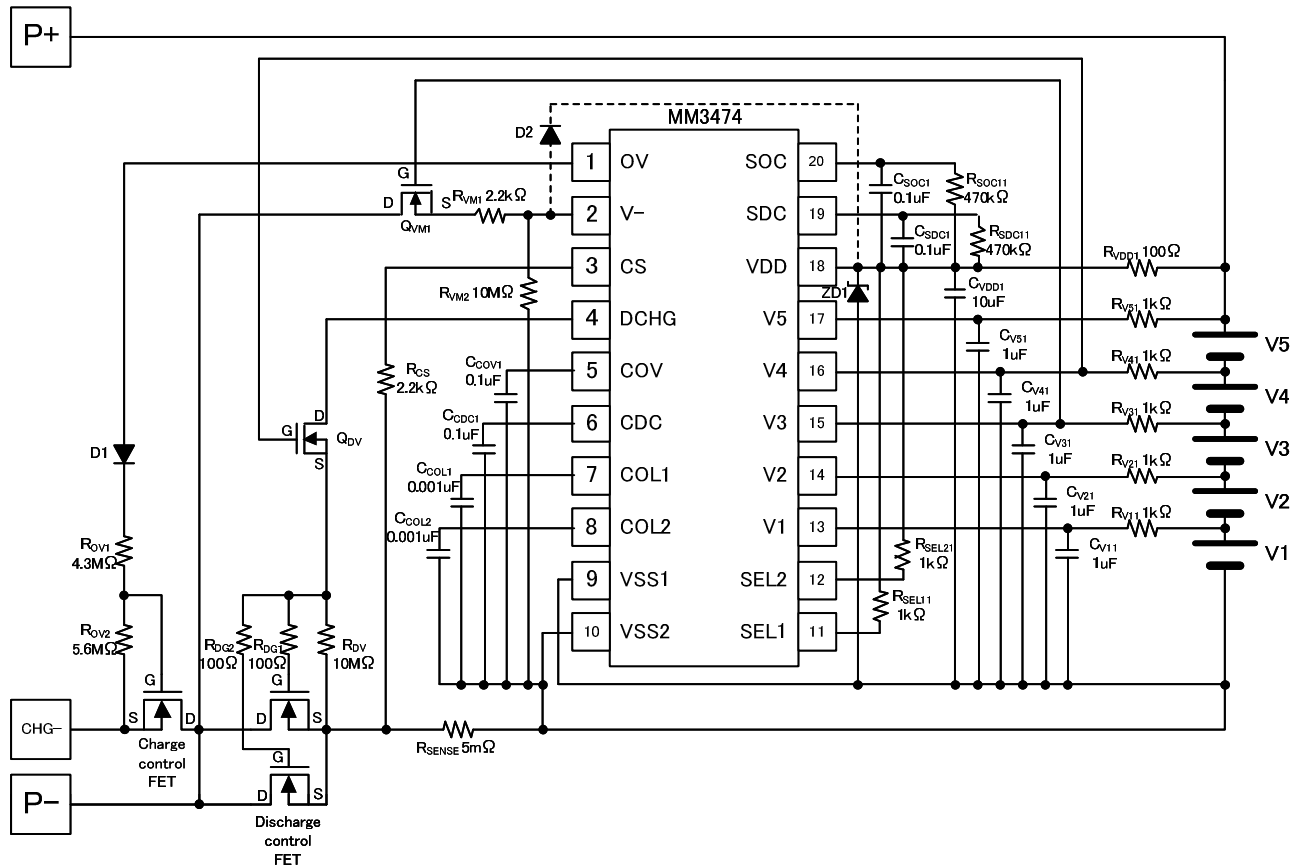


8. Timing chart

8-4. Overcurrent detection, short detection and release operation



9. Explanation of external parts



MM3474 5Cells protection typical application circuit

Parts name	Roles of parts
$R_{VDD1} \cdot R_{V51} \cdot R_{V41} \cdot R_{V31} \cdot R_{V21} \cdot R_{V11}$	CR low-pass filter to stabilize a supply ripple of VDD pin·V5pin·V4pin·V3pin·V2pin·V1pin.
$C_{VDD1} \cdot C_{V51} \cdot C_{V41} \cdot C_{V31} \cdot C_{V21} \cdot C_{V12}$	
$R_{SEL11} \cdot R_{SEL21}$	Resistor to protect terminal.
$R_{SDC11} \cdot R_{SOC11}$	Current limitation resistor. (The voltage signal is converted into the current signal by this resistor at the cascading connection.)
C_{COV1}	Capacitor to sets overcharge detection/release dead time.
C_{CDC1}	Capacitor to sets overdischarge detection/release dead time.
C_{COL1}	Capacitor to sets overcurrent detection dead time.
C_{COL2}	Capacitor to sets overcurrent release dead time.
R_{SENSE}	Sense resistance to observe discharging current.
R_{CS}	Resistor to protect terminal.
R_{VM1}	Resistor to protect terminal.
$R_{DG1} \cdot R_{DG2}$	Resistor for preventing the gate destruction due to parasitic oscillation.
$Q_{DV} \cdot R_{DV}$	The voltage between gate and source of FET must not exceed the absolute maximum rating. Therefore, The output voltage is clamped by FET or divided with a resistor.
$R_{OV1} \cdot R_{OV2}$	
$Q_{VM1} \cdot R_{VM2}$	FET to prevent voltage input to V-pin from rising more than voltage of VDD pin.
D1	Diode to turn off FET quickly by discharging charge of parasitic capacitance of FET.
D2	When a V-pin becomes more than it in VDD pin voltage, it is Schottky barrier diode to bypass the electric current so that an electric current does not flow through the IC inside.
ZD1	Zener diode to prevent destruction of IC by surge voltage.
Charge control FET	Nch MOS FET to control charging current.
Discharge control FET	Nch MOS FET to control discharging current.

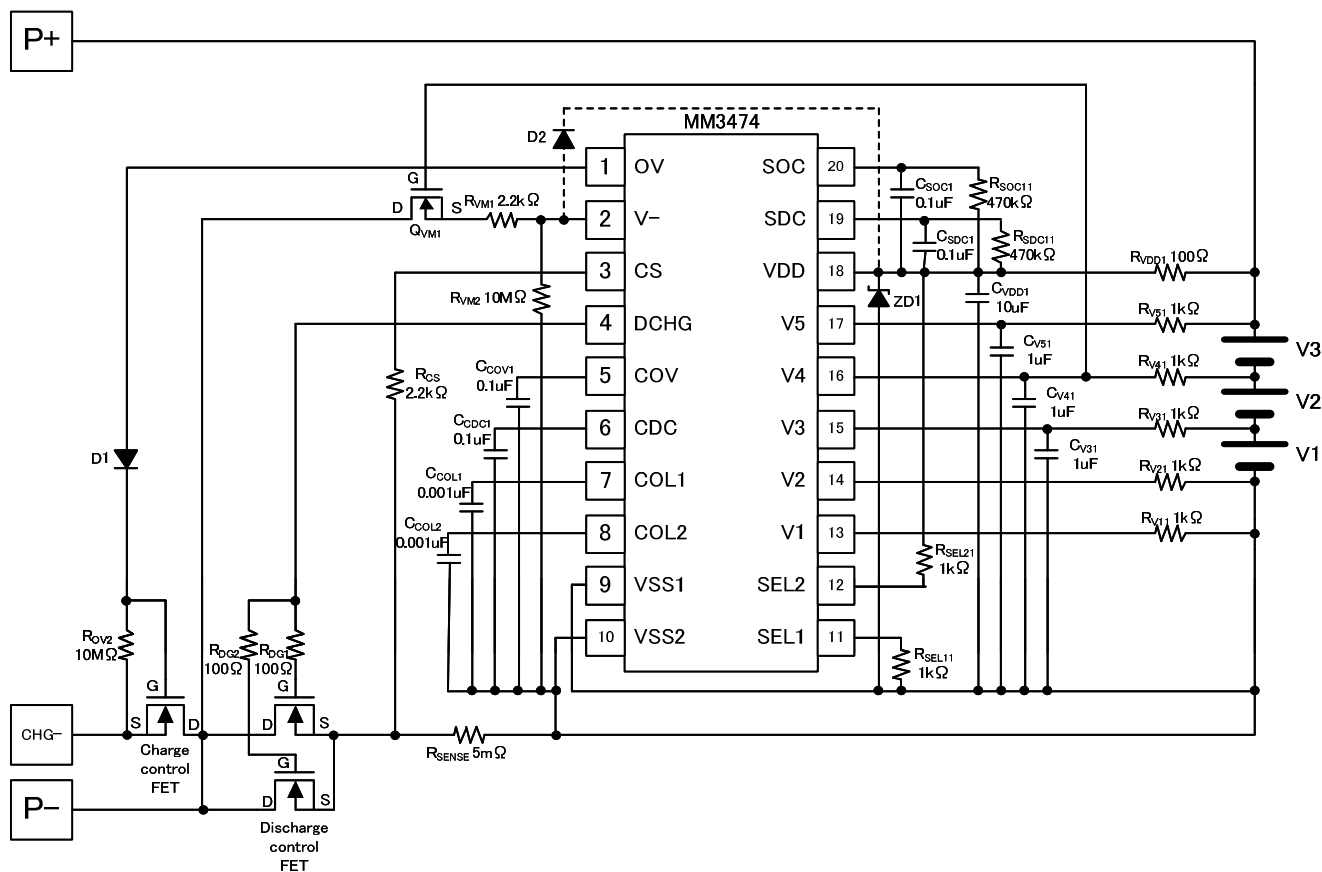
10. Examples of application circuit

10-1. Examples of 3 cells application circuit

10-1-1. Circuit condition 1

Circuit condition 1

- Number of cells : 3 cells
- Charge and discharge route : Separated
- Overdischarge release metho : Voltage release
- Optional functions : Nothing



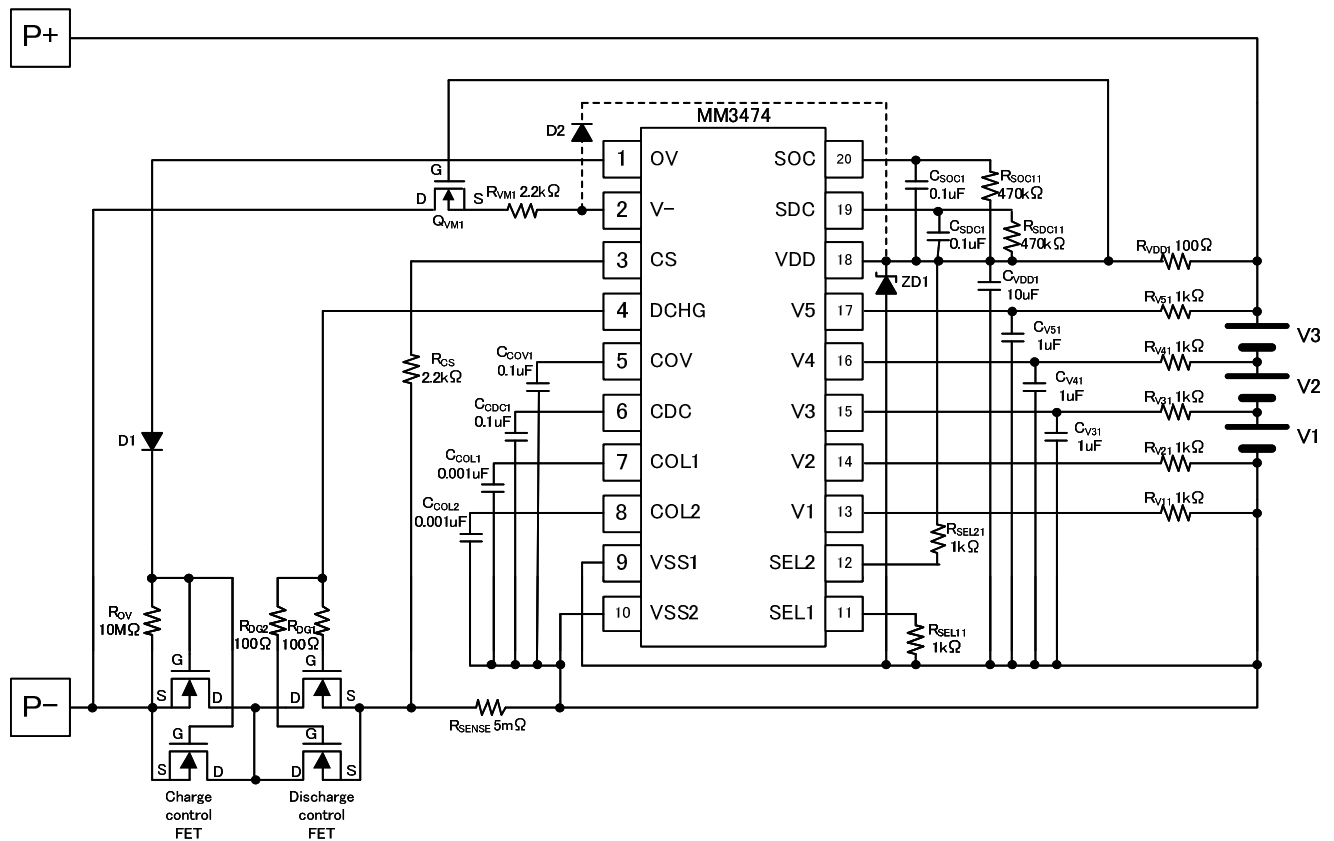
10. Examples of application circuit

10-1. Examples of 3 cells application circuit

10-1-2. Circuit condition 2

Circuit condition 2

- Number of cells : 3 cells
- Charge and discharge route : Common
- Overdischarge release metho : Voltage release
- Optional functions : Nothing



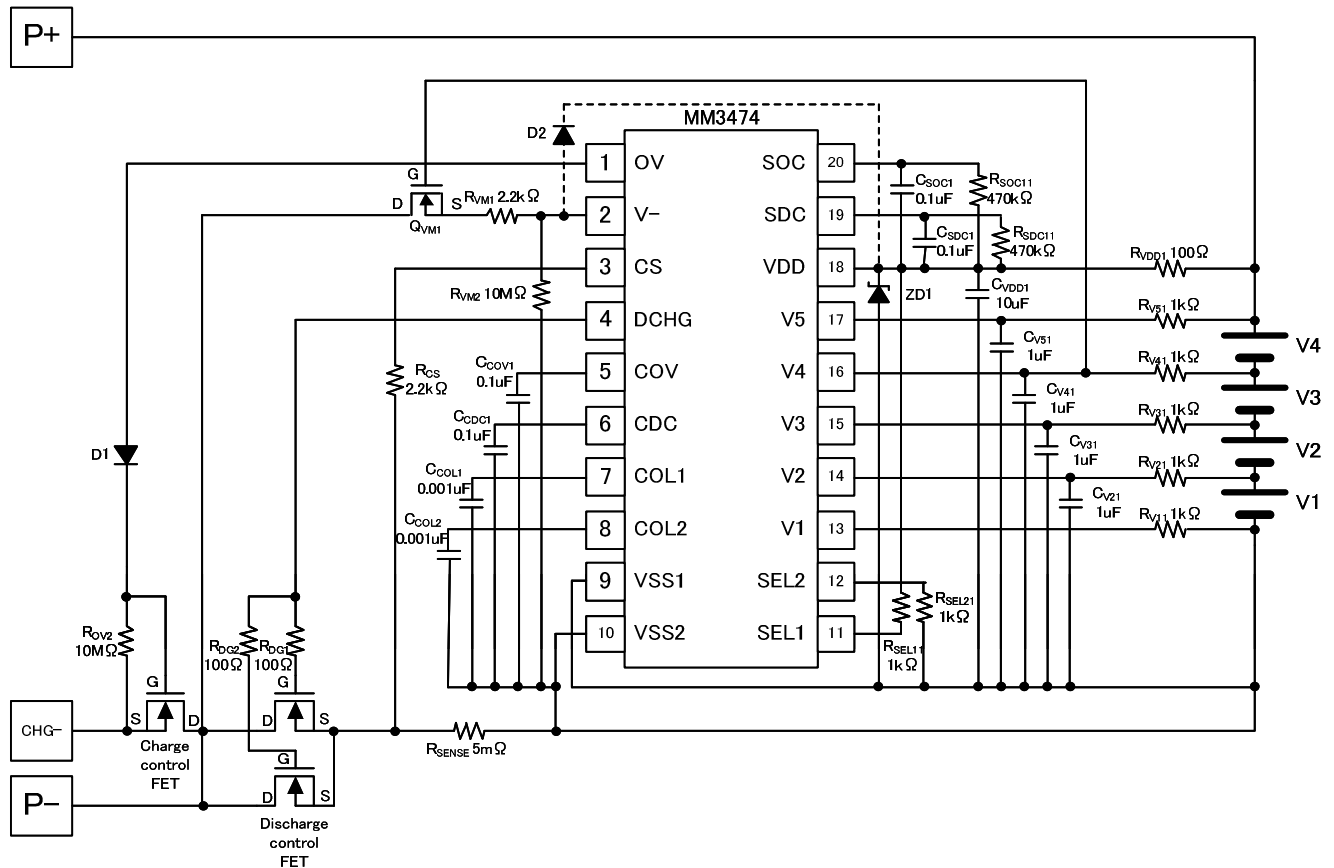
10. Examples of application circuit

10-2. Examples of 4 cells application circuit

10-2-1. Circuit condition 1

Circuit condition 1

- Number of cells : 4 cells
- Charge and discharge route : Separated
- Overdischarge release metho : Voltage release
- Optional functions : Nothing



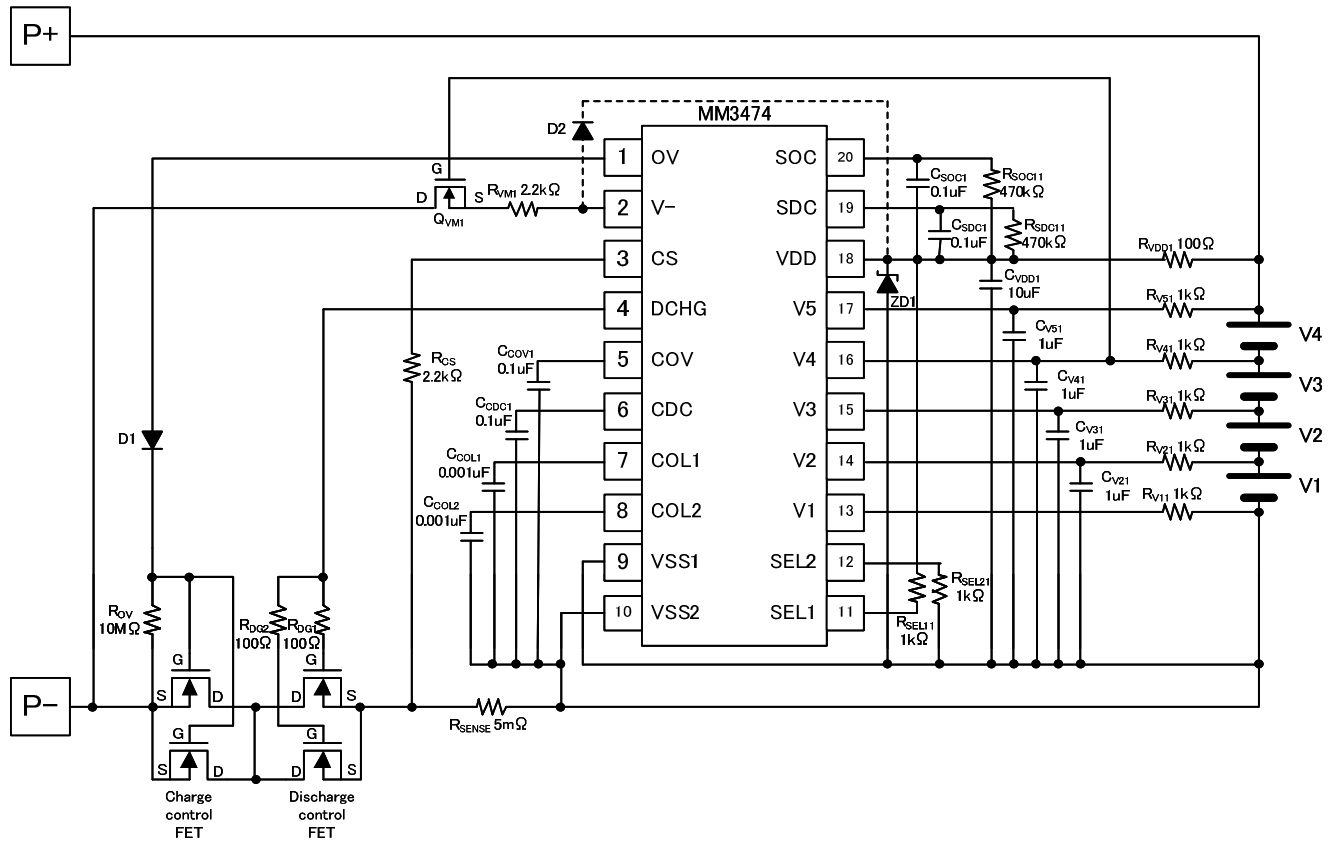
10. Examples of application circuit

10-2. Examples of 4 cells application circuit

10-2-2. Circuit condition 2

Circuit condition 2

- Number of cells : 4 cells
- Charge and discharge route : Common
- Overdischarge release metho : Voltage release
- Optional functions : Nothing



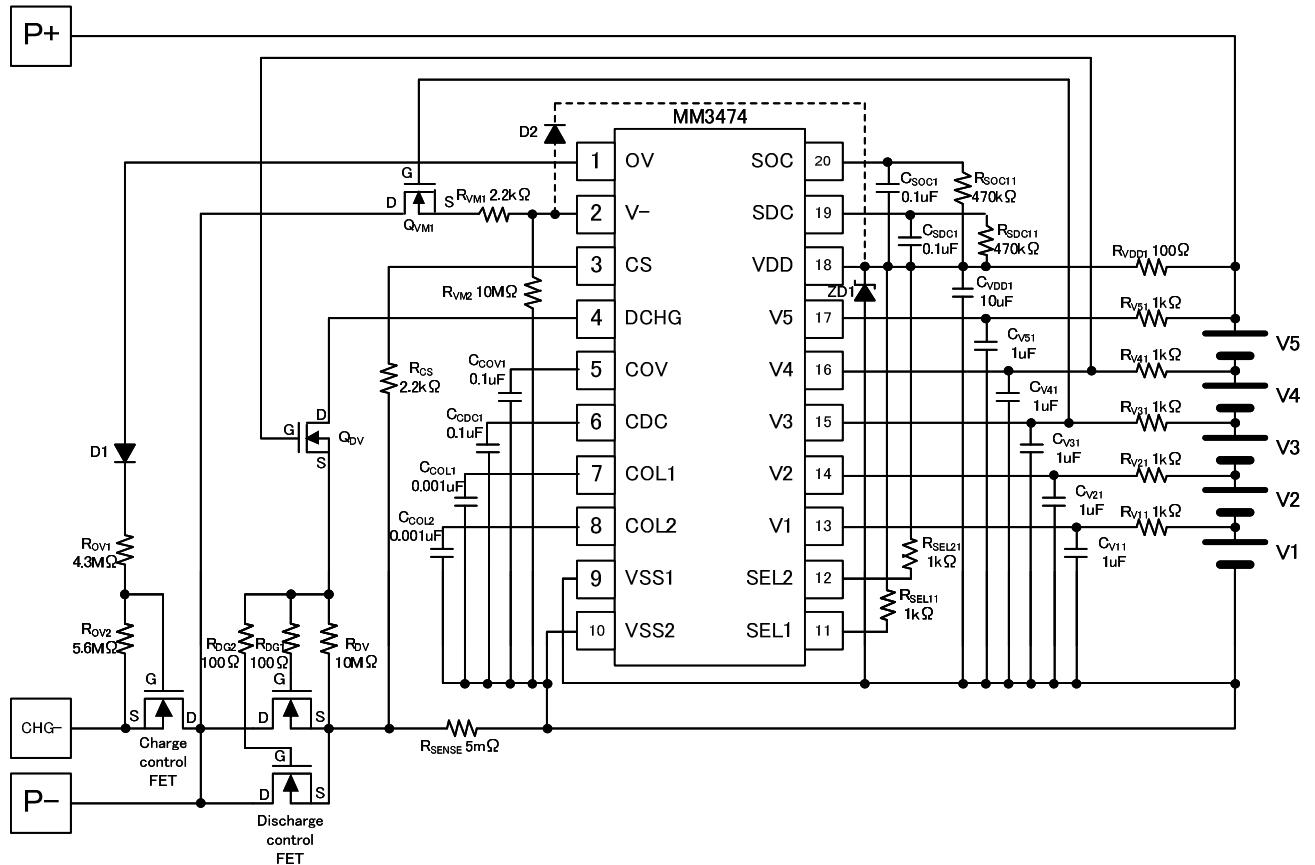
10. Examples of application circuit

10-3. Examples of 5 cells application circuit

10-3-1. Circuit condition 1

Circuit condition 1

- Number of cells : 5 cells
- Charge and discharge route : Separated
- Overdischarge release metho : Voltage release
- Optional functions : Nothing



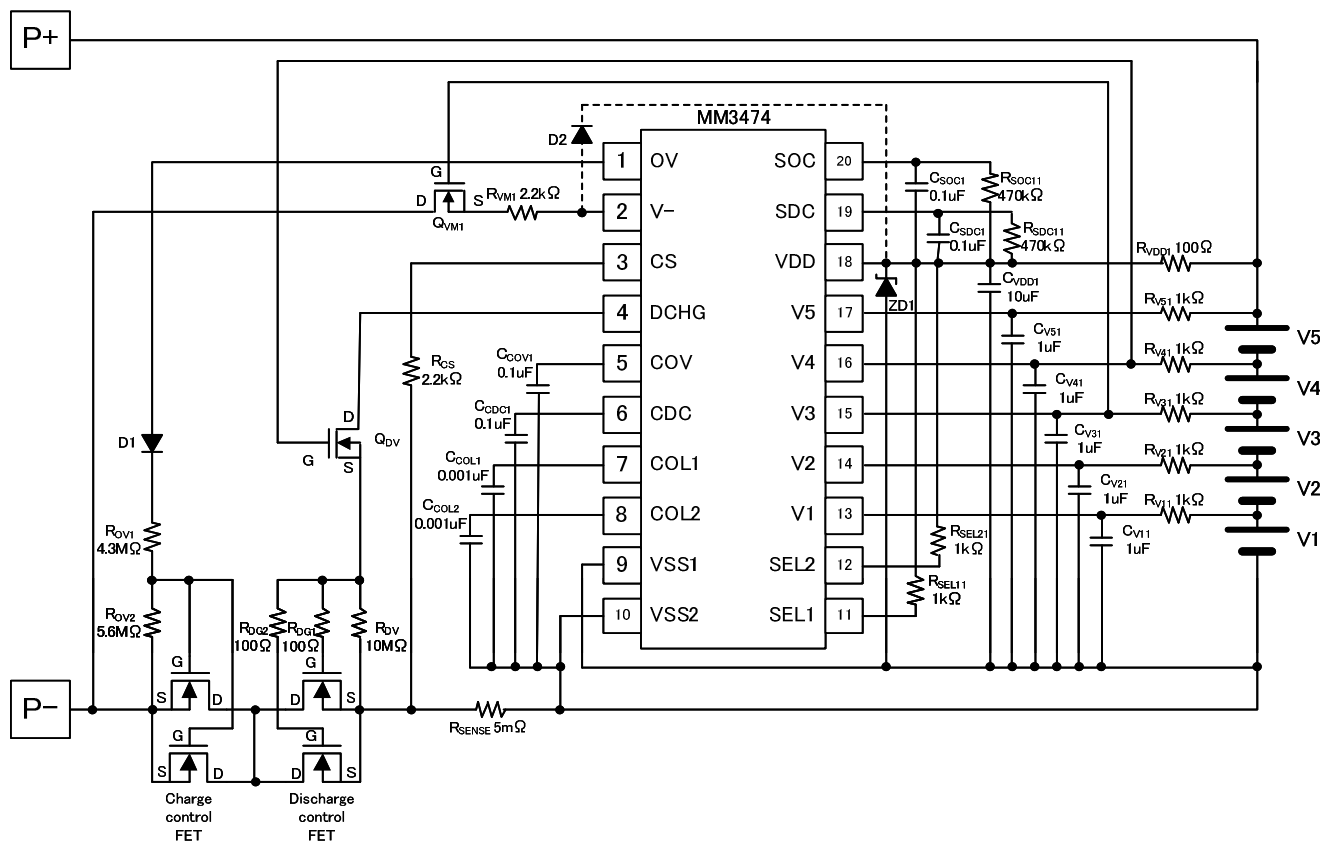
10. Examples of application circuit

10-3. Examples of 5 cells application circuit

10-3-2. Circuit condition 2

Circuit condition 2

- Number of cells : 5 cells
- Charge and discharge route : Common
- Overdischarge release metho : Voltage release
- Optional functions : Nothing

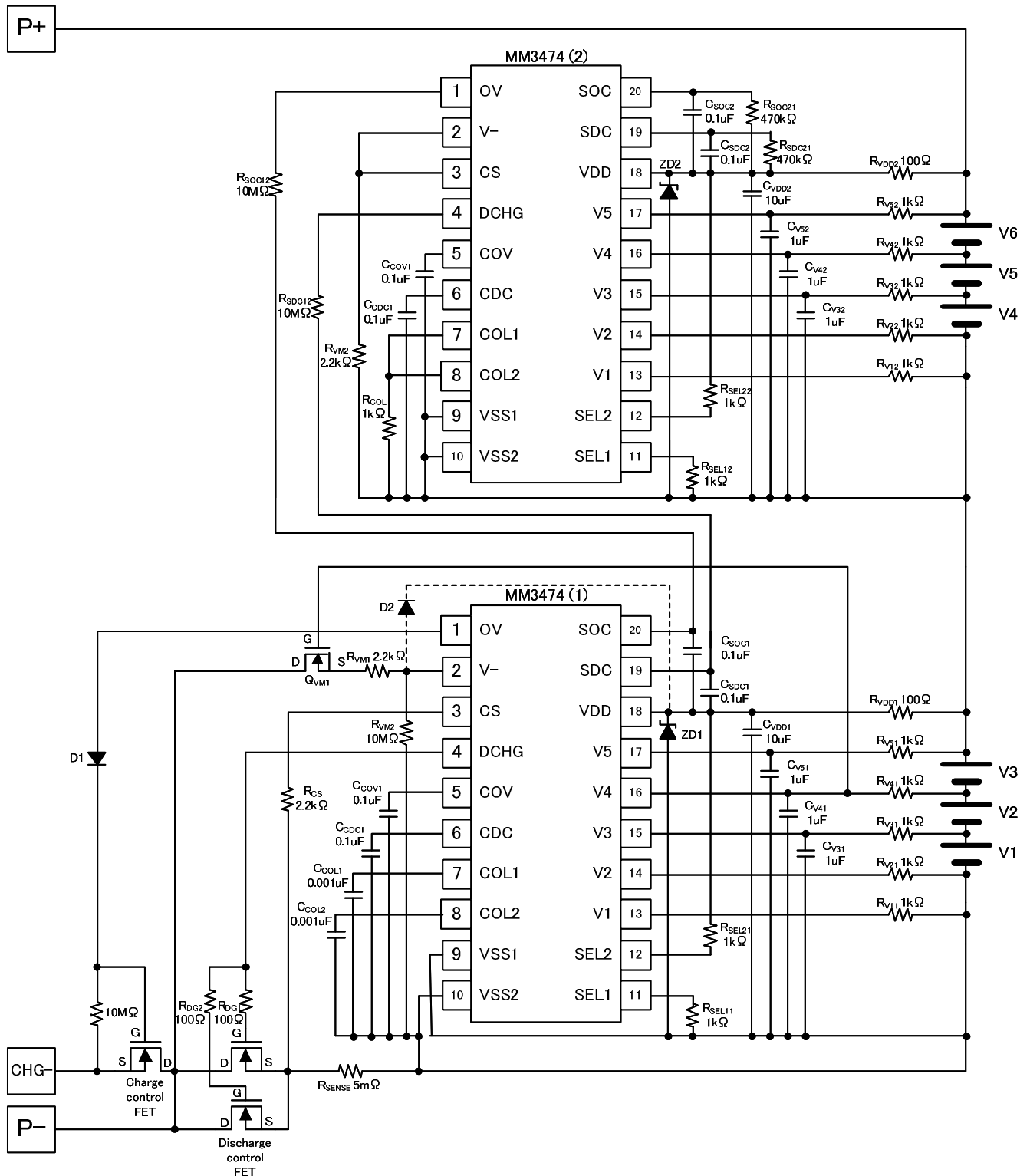


10. Examples of application circuit

10-4. Examples of 6 cells application circuit

10-4-1. Circuit condition 1

- Number of cells : 6 cells (3cells + 3cells)
- Charge and discharge route : Separated
- Overdischarge release metho : Voltage release
- Optional functions : Nothing

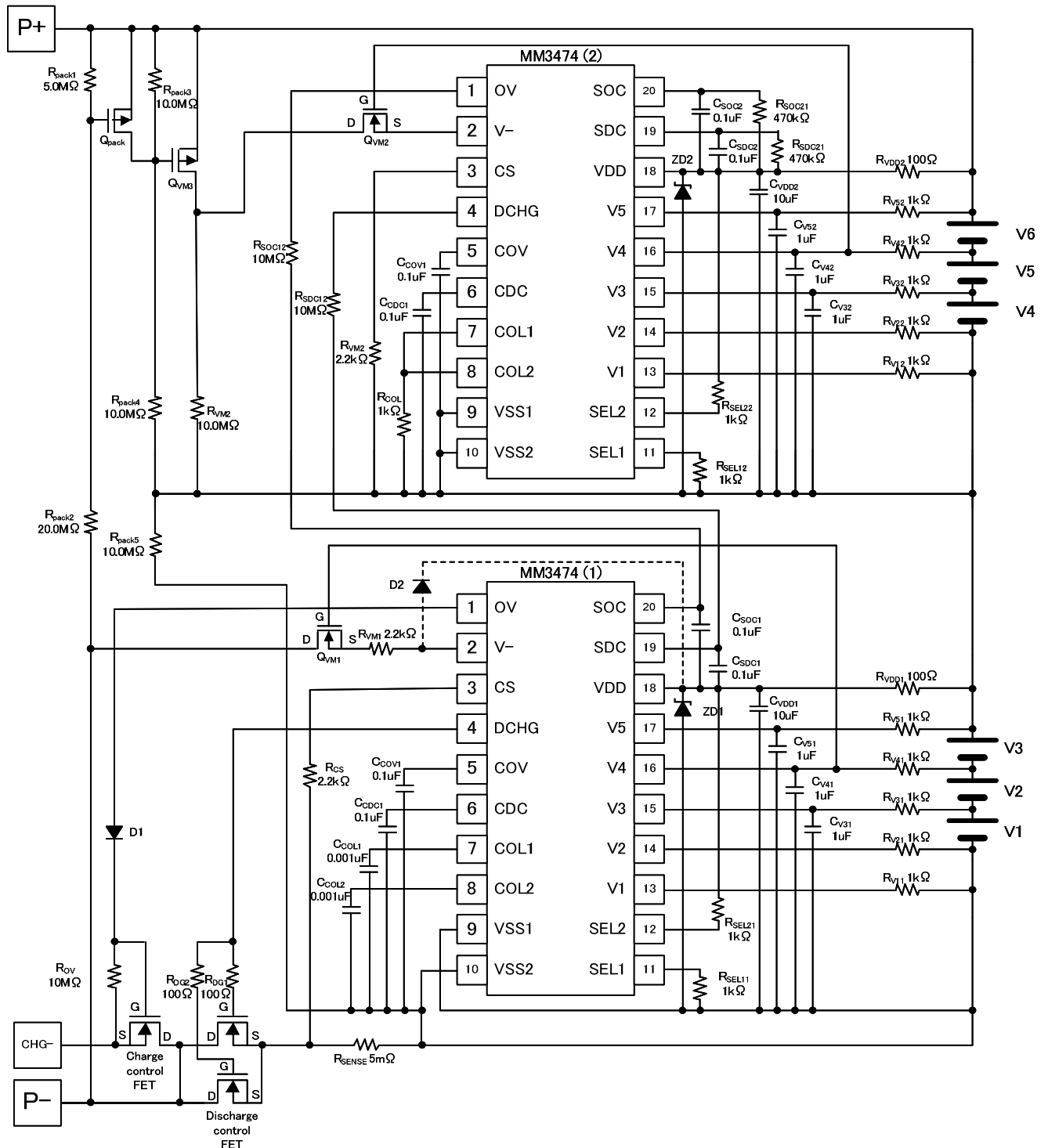


10. Examples of application circuit

10-4. Examples of 6 cells application circuit. Circuit condition 2

10-4-2. Circuit condition 2

- Number of cells : 6 cells (3cells + 3cells)
- Charge and discharge route : Separated
- Overdischarge release metho : Load release + Voltage release
- Optional functions : Nothing

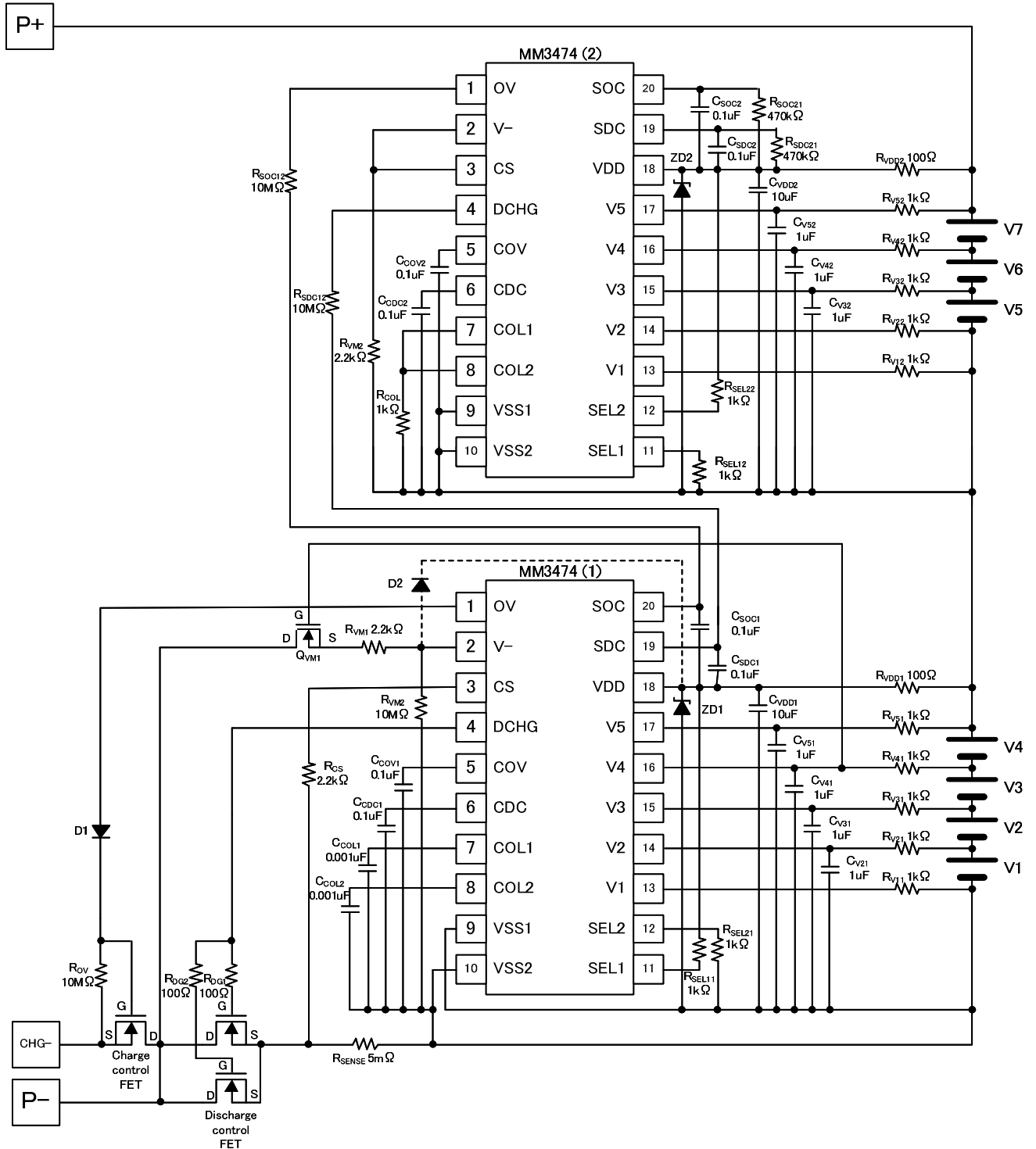


10. Examples of application circuit

10-5. Examples of 7 cells application circuit condition 1

10-5-1. Circuit condition 1

- Number of cells : 7 cells (4cells + 3cells)
- Charge and discharge route : Separated
- Overdischarge release metho : Voltage release
- Optional functions : Nothing

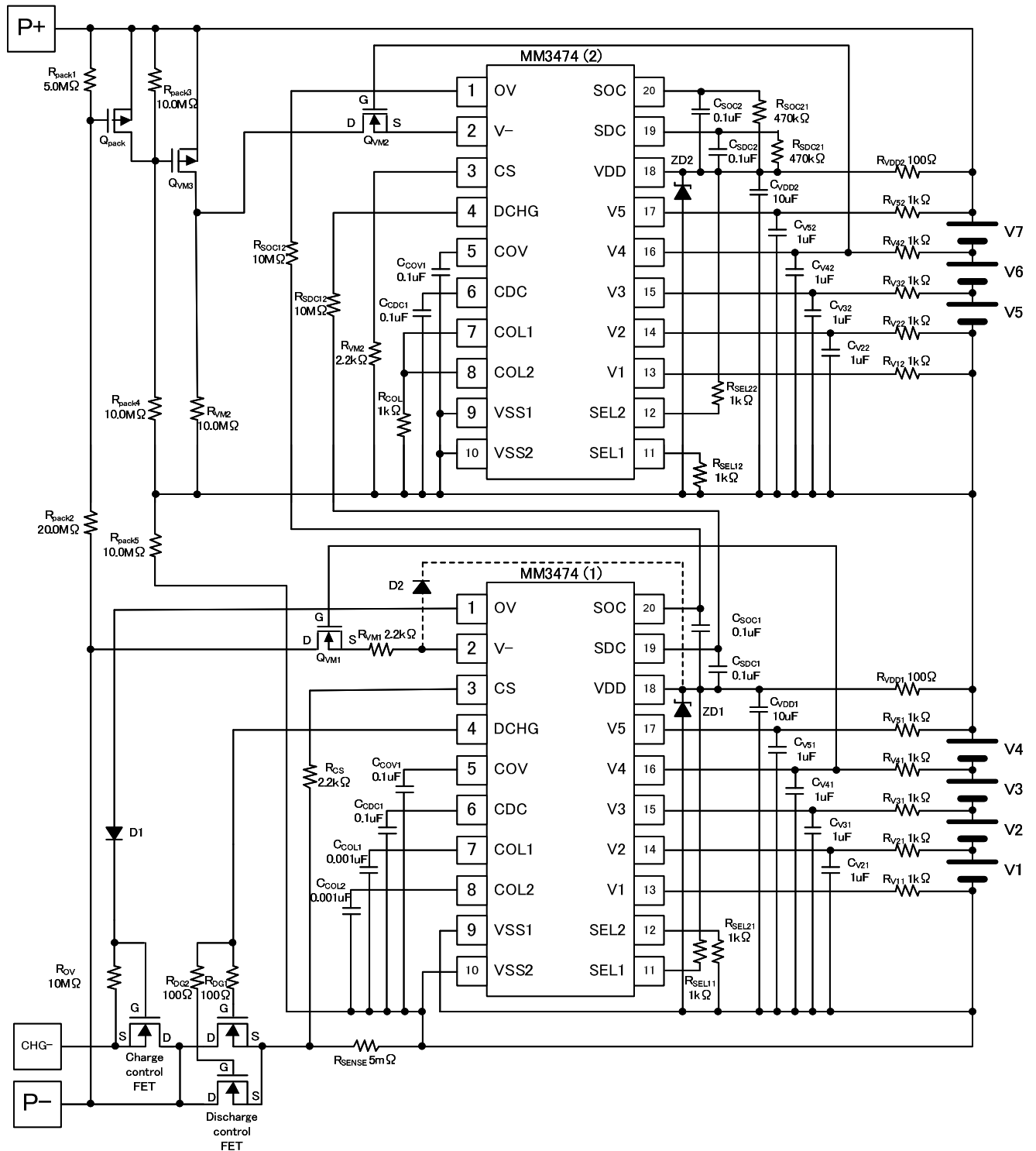


10. Examples of application circuit

10-5. Examples of 7 cells application circuit. Circuit condition 2

10-5-2. Circuit condition 2

- Number of cells : 7 cells (4cells + 3cells)
- Charge and discharge route : Separated
- Overdischarge release metho : Load release + Voltage release
- Optional functions : Nothing

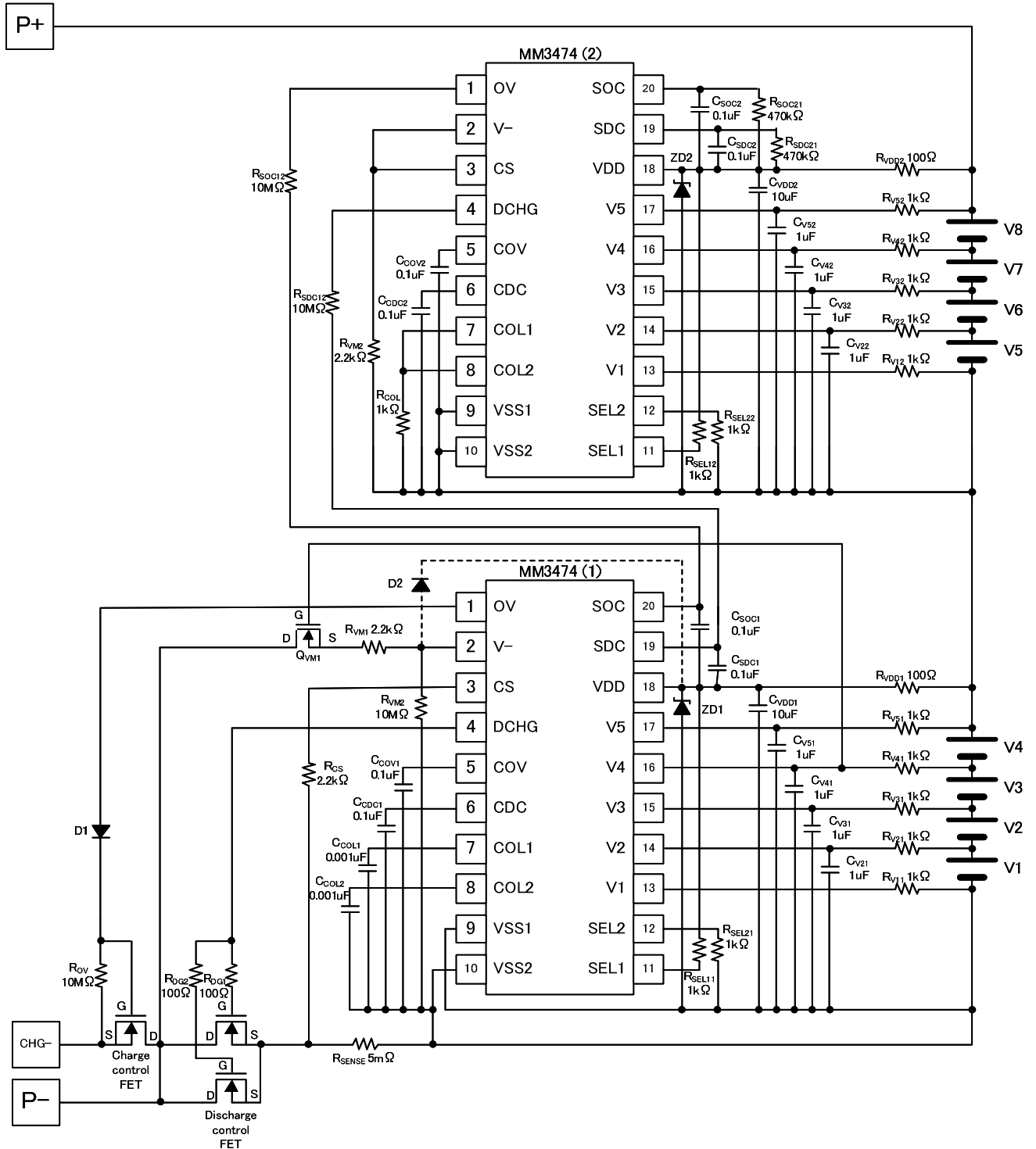


10. Examples of application circuit

10-6. Examples of 8 cells application circuit condition 1

10-6-1. Circuit condition 1

- Number of cells : 8 cells (4cells + 4cells)
- Charge and discharge route : Separated
- Overdischarge release metho : Voltage release
- Optional functions : Nothing

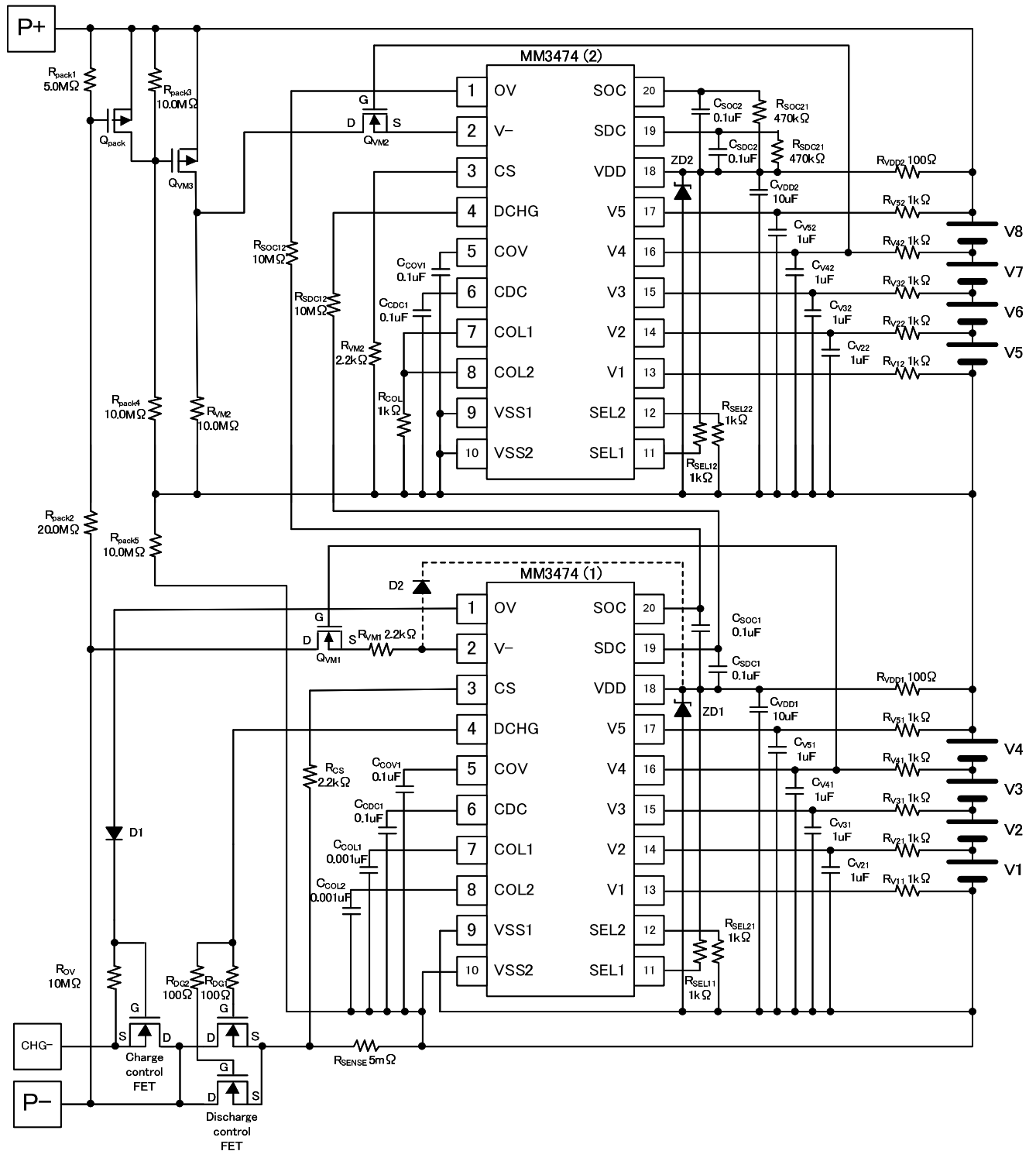


10. Examples of application circuit

10-6. Examples of 8 cells application circuit. Circuit condition 2

10-6-2. Circuit condition 2

- Number of cells : 8 cells (4cells + 4cells)
- Charge and discharge route : Separated
- Overdischarge release metho : Load release + Voltage release
- Optional functions : Nothing

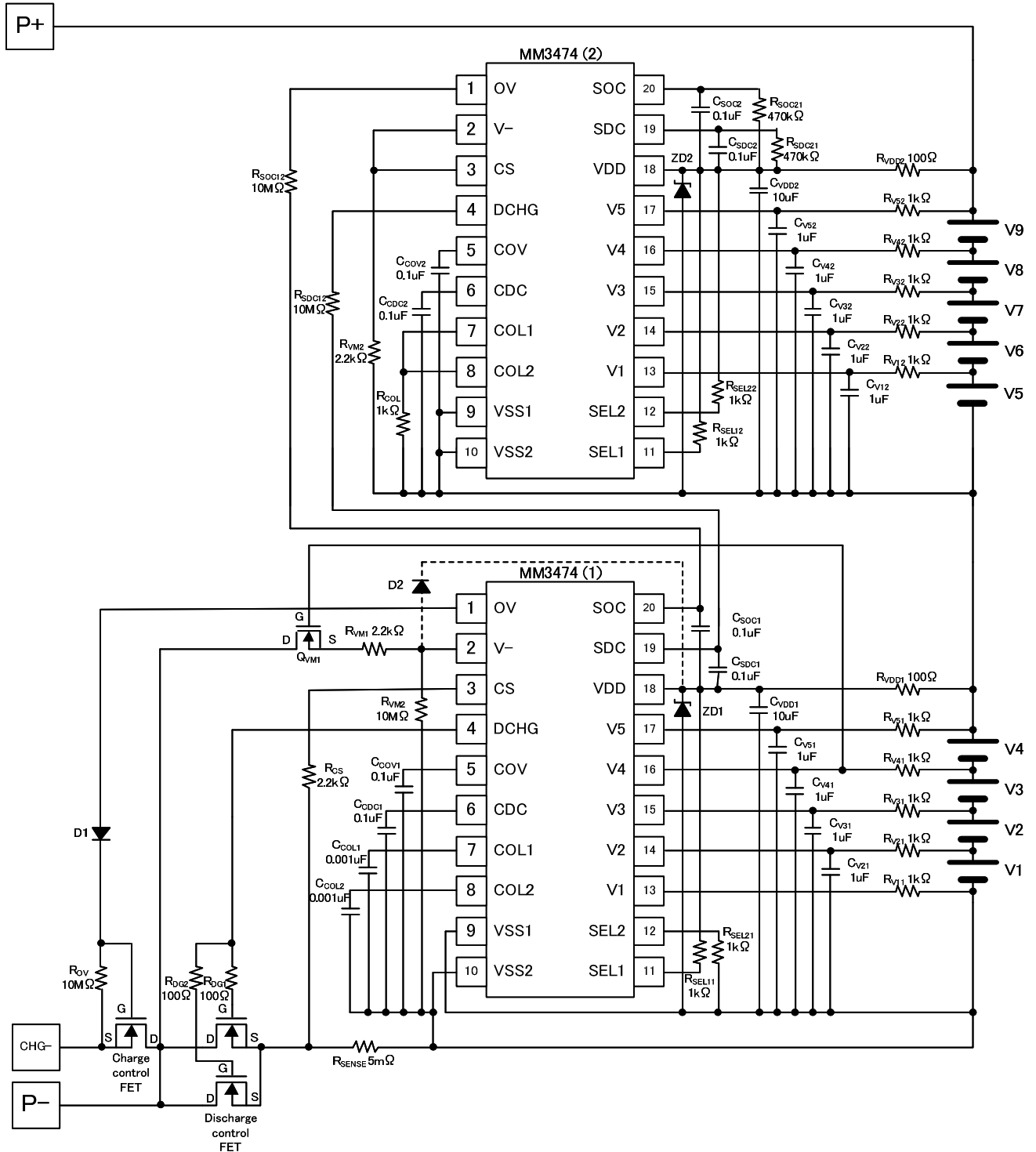


10. Examples of application circuit

10-7. Examples of 9 cells application circuit condition 1

10-7-1. Circuit condition 1

- Number of cells : 9 cells (4cells + 5cells)
- Charge and discharge route : Separated
- Overdischarge release method : Voltage release
- Optional functions : Nothing

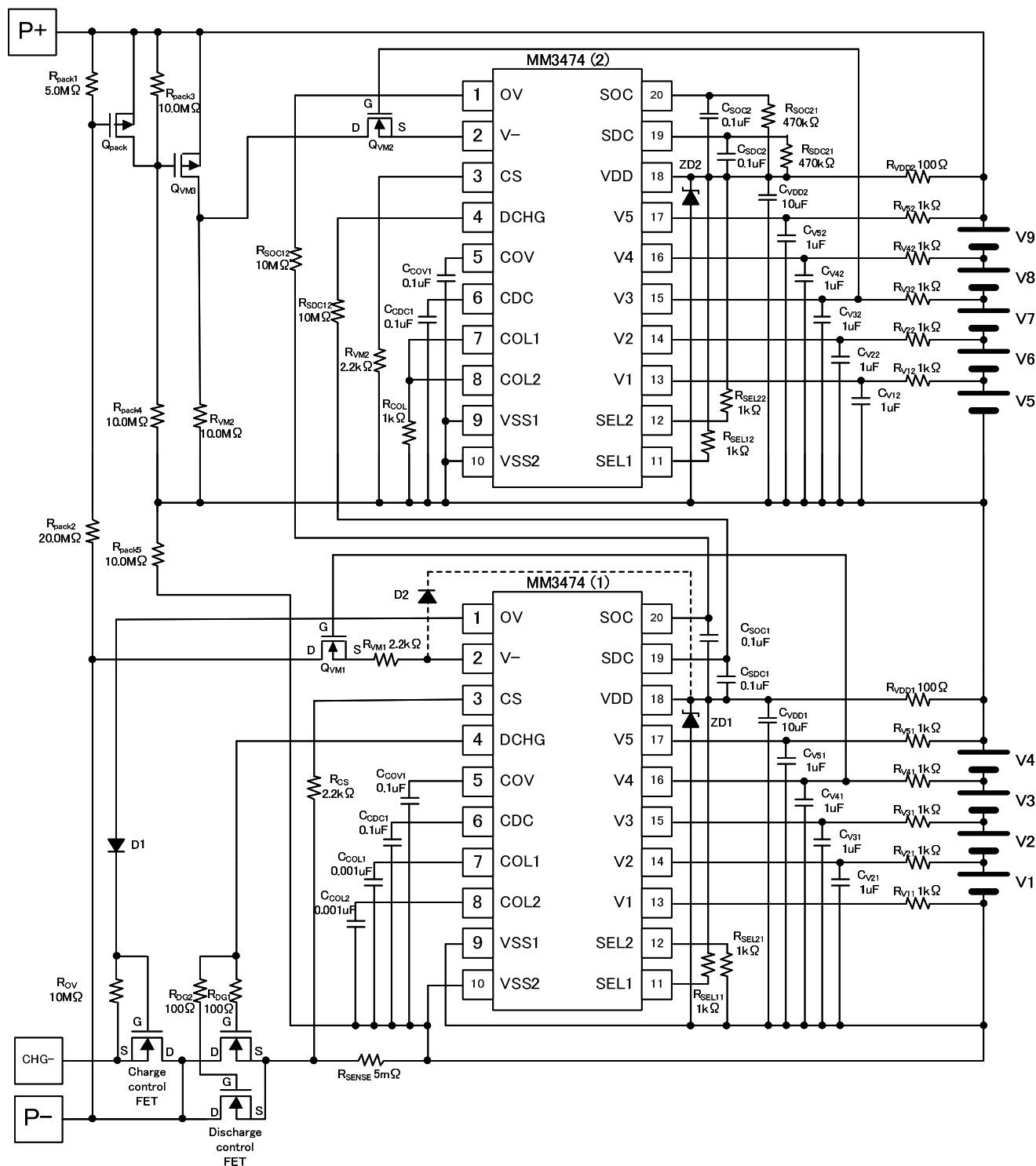


10. Examples of application circuit

10-7. Examples of 9 cells application circ Circuit condition 2

10-7-2. Circuit condition 2

- Number of cells : 9 cells (4cells + 5cells)
- Charge and discharge route : Separated
- Overdischarge release metho : Load release + Voltage release
- Optional functions : Nothing

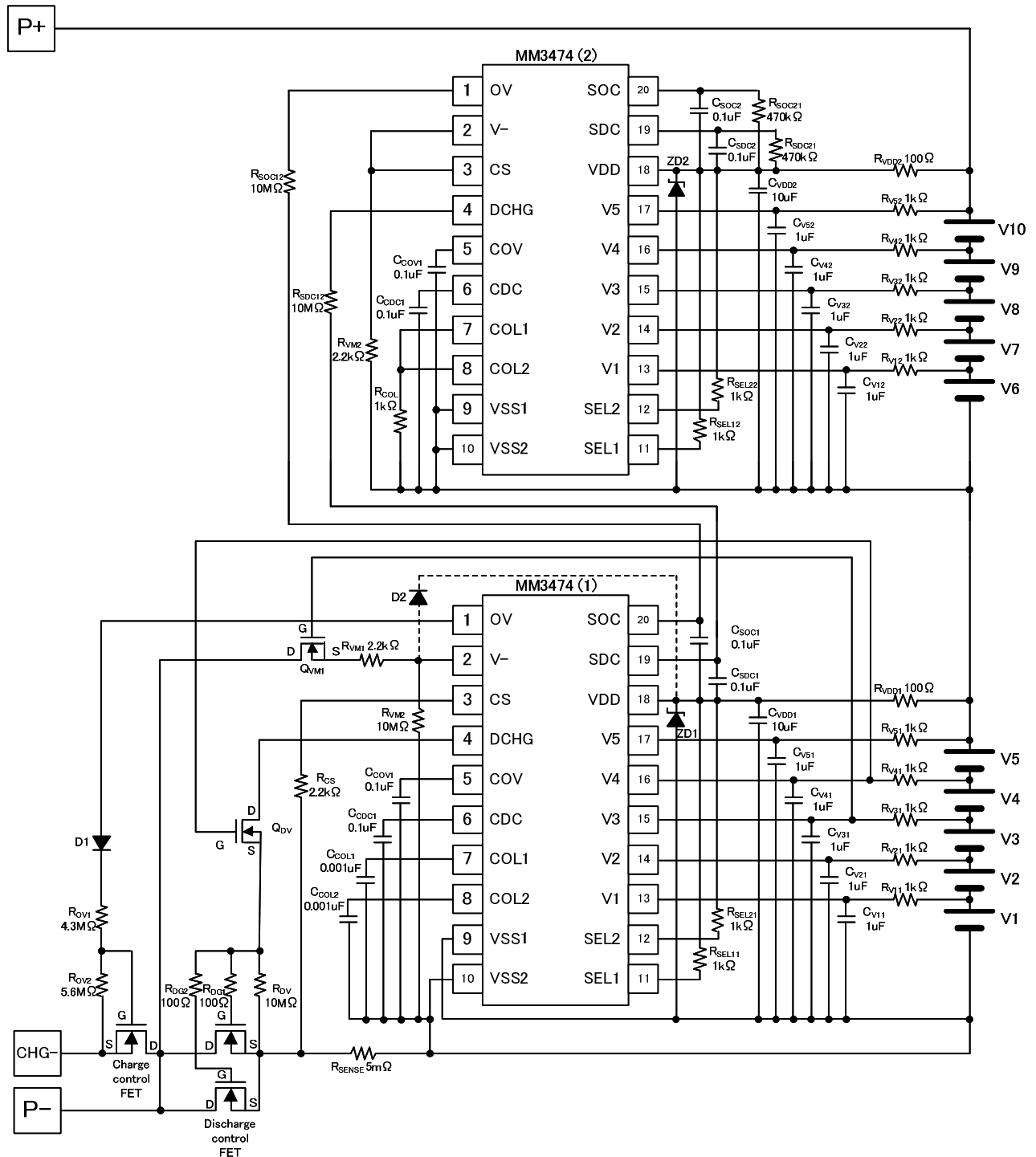


10. Examples of application circuit

10-8. Examples of 10 cells application circ Circuit condition 1

10-8-1. Circuit condition 1

- Number of cells : 10 cells (5cells + 5cells)
- Charge and discharge route : Separated
- Overdischarge release metho : Voltage release
- Optional functions : Nothing

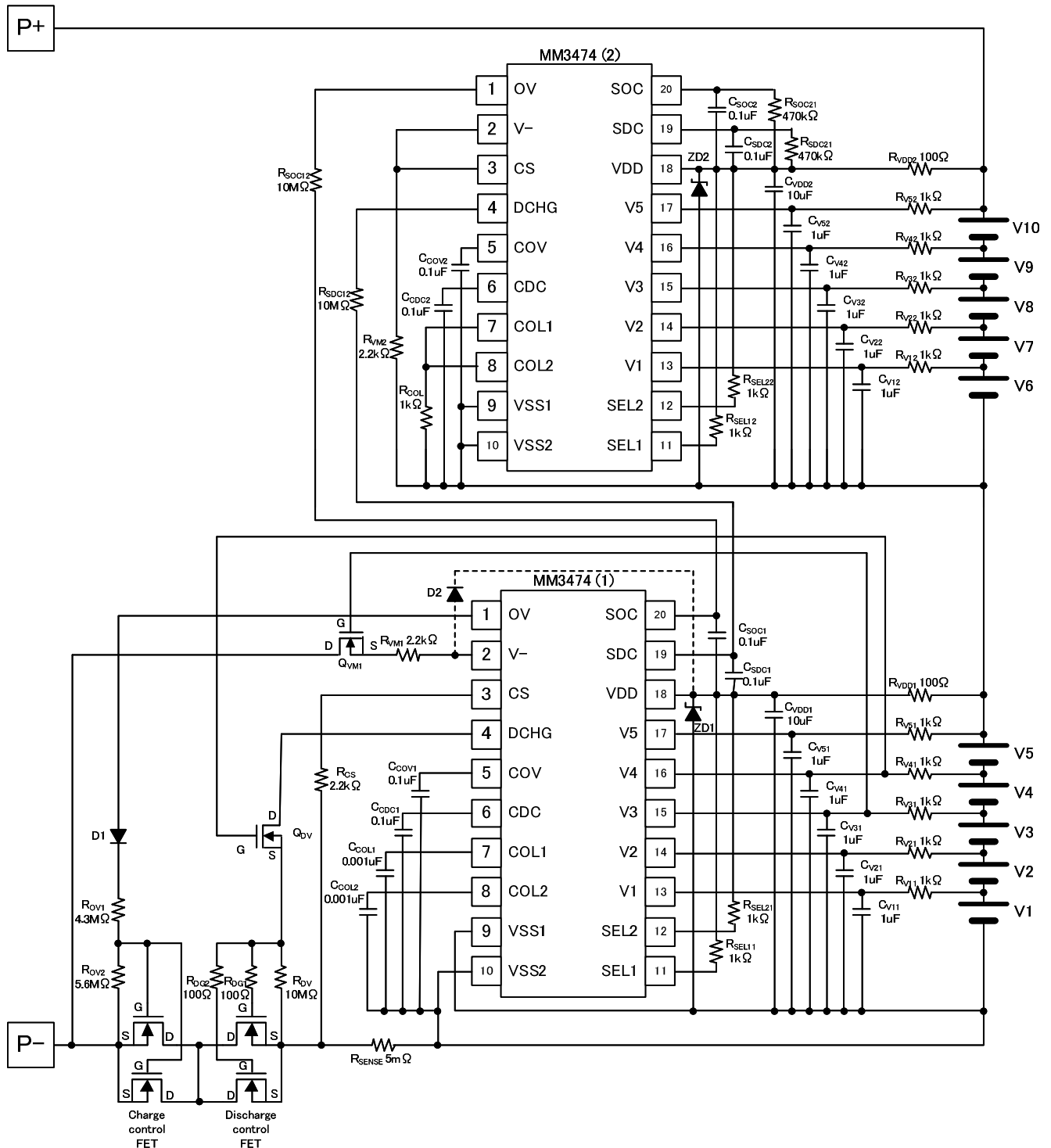


10. Examples of application circuit

10-8. Examples of 10 cells application circ Circuit condition 2

10-8-2. Circuit condition 2

- Number of cells : 10 cells (5cells + 5cells)
- Charge and discharge route : Common
- Overdischarge release metho : Voltage release
- Optional functions : Nothing

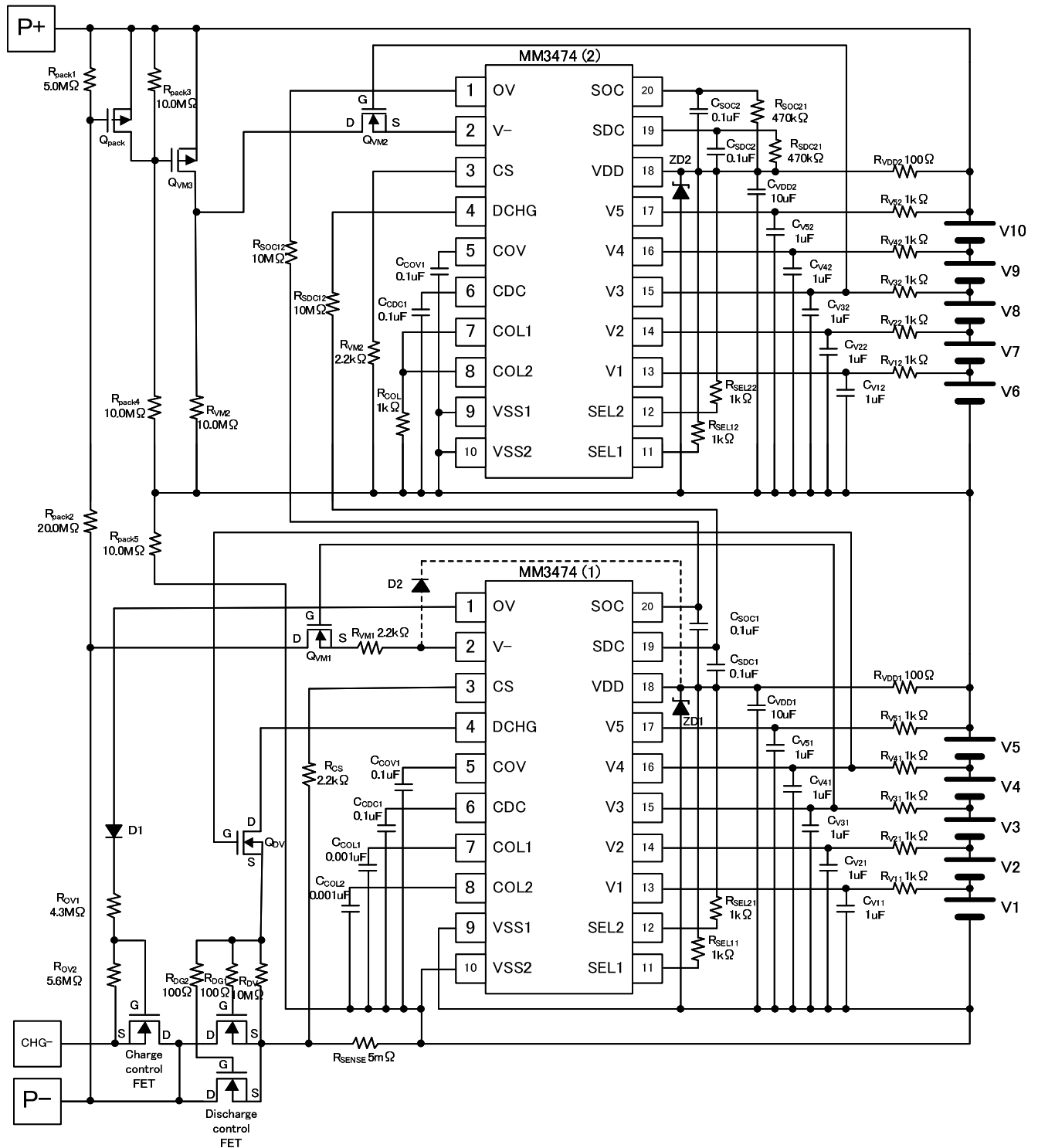


10. Examples of application circuit

10-8. Examples of 10 cells application circ Circuit condition 3

10-8-3. Circuit condition 3

- Number of cells : 10 cells (5cells + 5cells)
- Charge and discharge route : Separated
- Overdischarge release metho : Load release + Voltage release
- Optional functions : Nothing



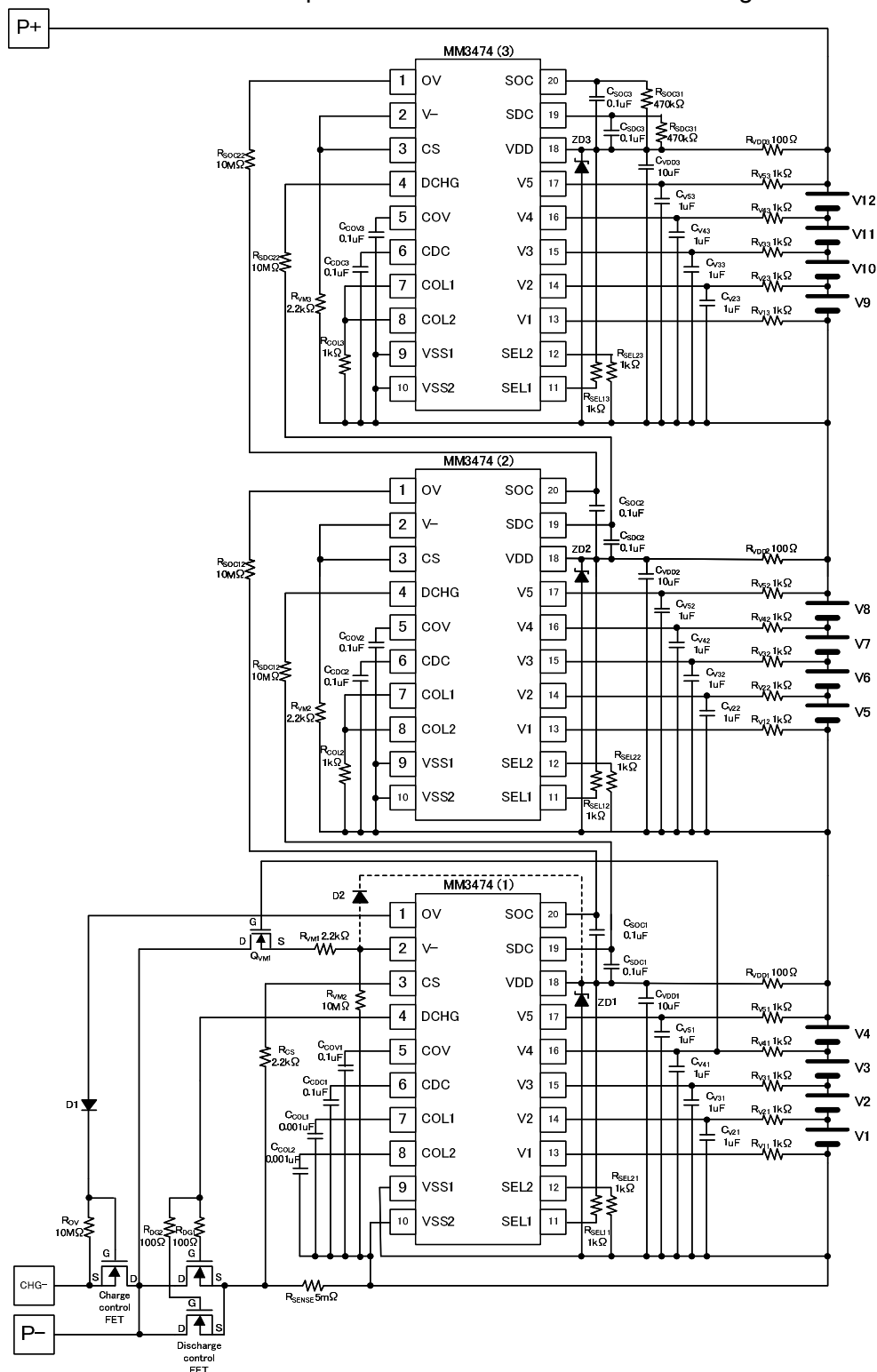
10. Examples of application circuit

10-9. Examples of 12 cells application circuit

10-9-1. Circuit condition 1

Circuit condition 1

- Number of cells : 12 cells (4cells + 4cells + 4 cells)
- Charge and discharge route : Separated
- Overdischarge release metho : Voltage release
- Optional functions : Nothing



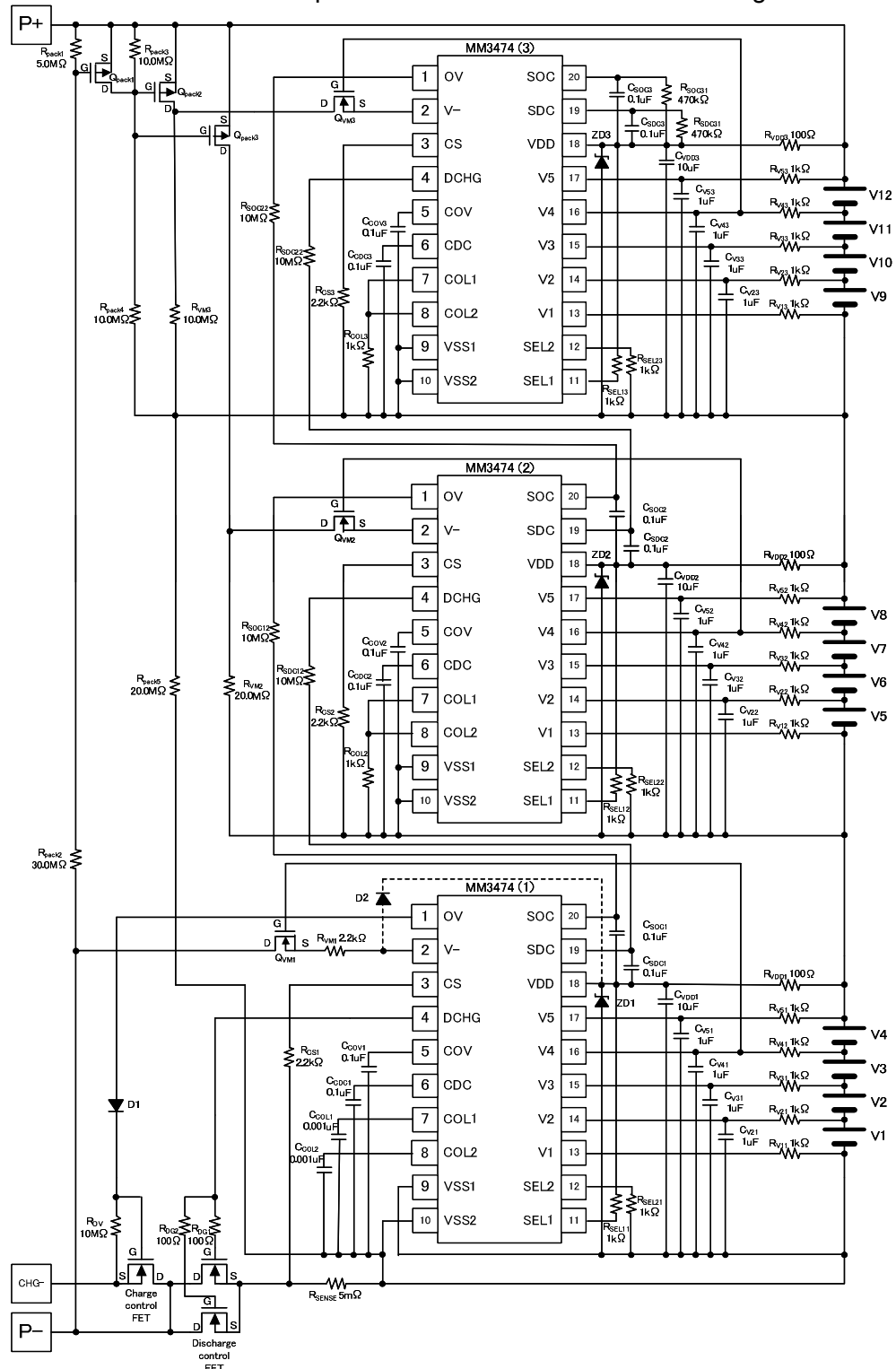
10. Examples of application circuit

10-9. Examples of 12 cells application circuit

10-9-2. Circuit condition 2

Circuit condition 2

- Number of cells : 12 cells (4cells + 4cells + 4 cells)
- Charge and discharge route : Separated
- Overdischarge release metho : Load release + Voltage release
- Optional functions : Nothing



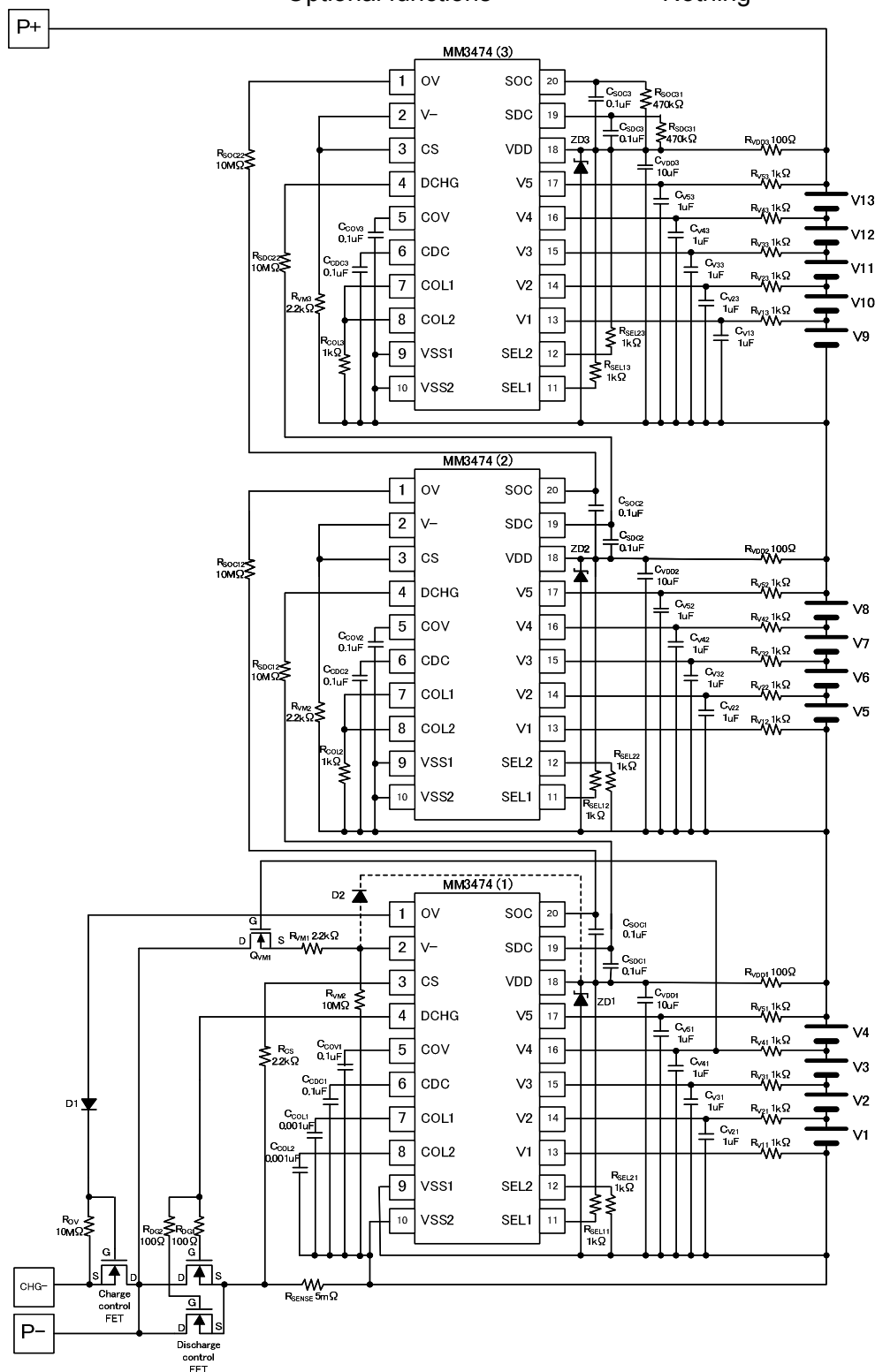
10. Examples of application circuit

10-10. Examples of 13 cells application circuit

10-10-1. Circuit condition 1

Circuit condition 1

- Number of cells : 13 cells (4cells + 4cells + 5 cells)
- Charge and discharge route : Separated
- Overdischarge release metho : Voltage release
- Optional functions : Nothing



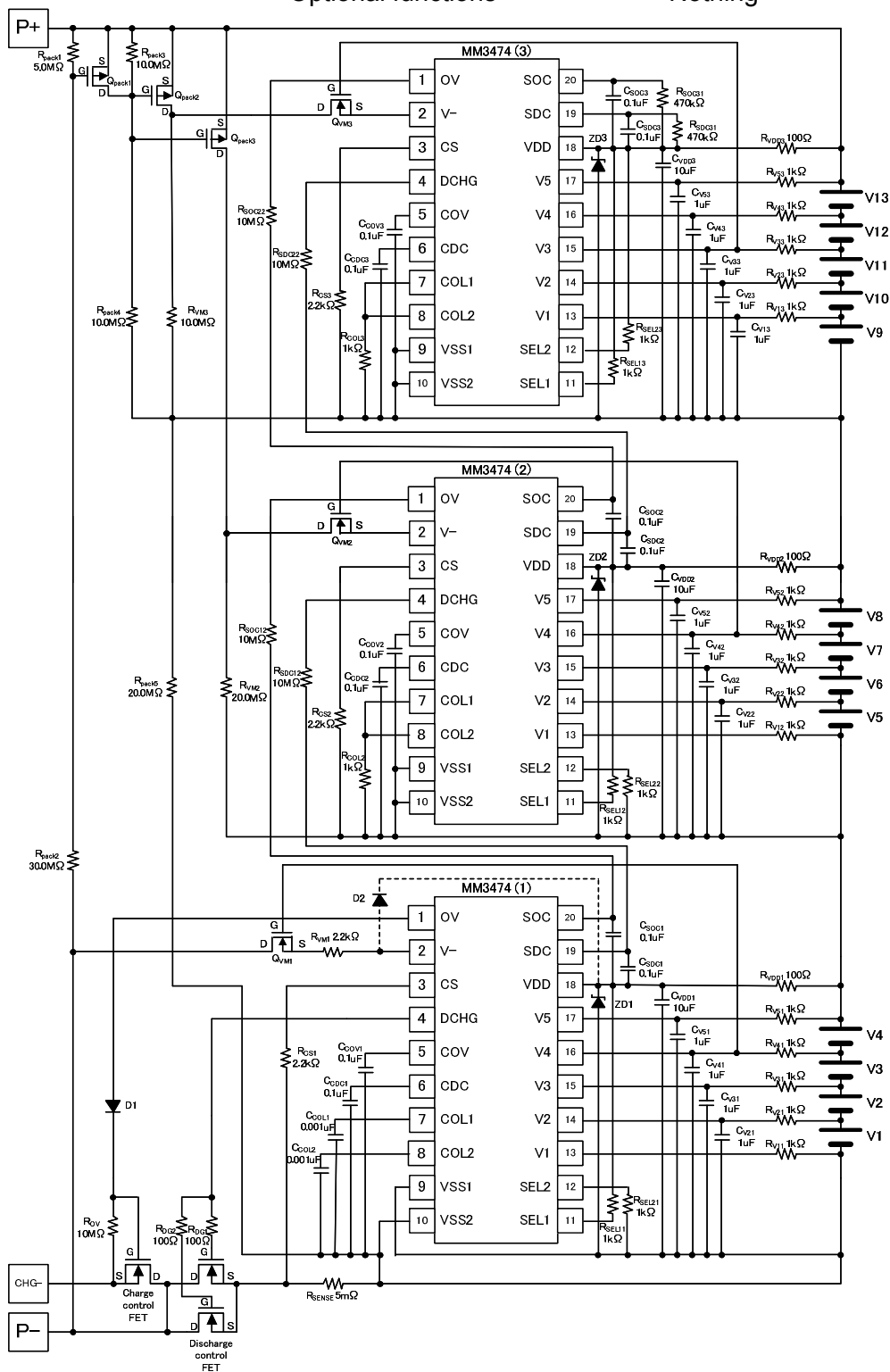
10. Examples of application circuit

10-10. Examples of 13 cells application circuit

10-10-2. Circuit condition 2

Circuit condition 2

- Number of cells : 13 cells (4cells + 4cells + 5 cells)
- Charge and discharge route : Separated
- Overdischarge release metho : Load release + Voltage release
- Optional functions : Nothing



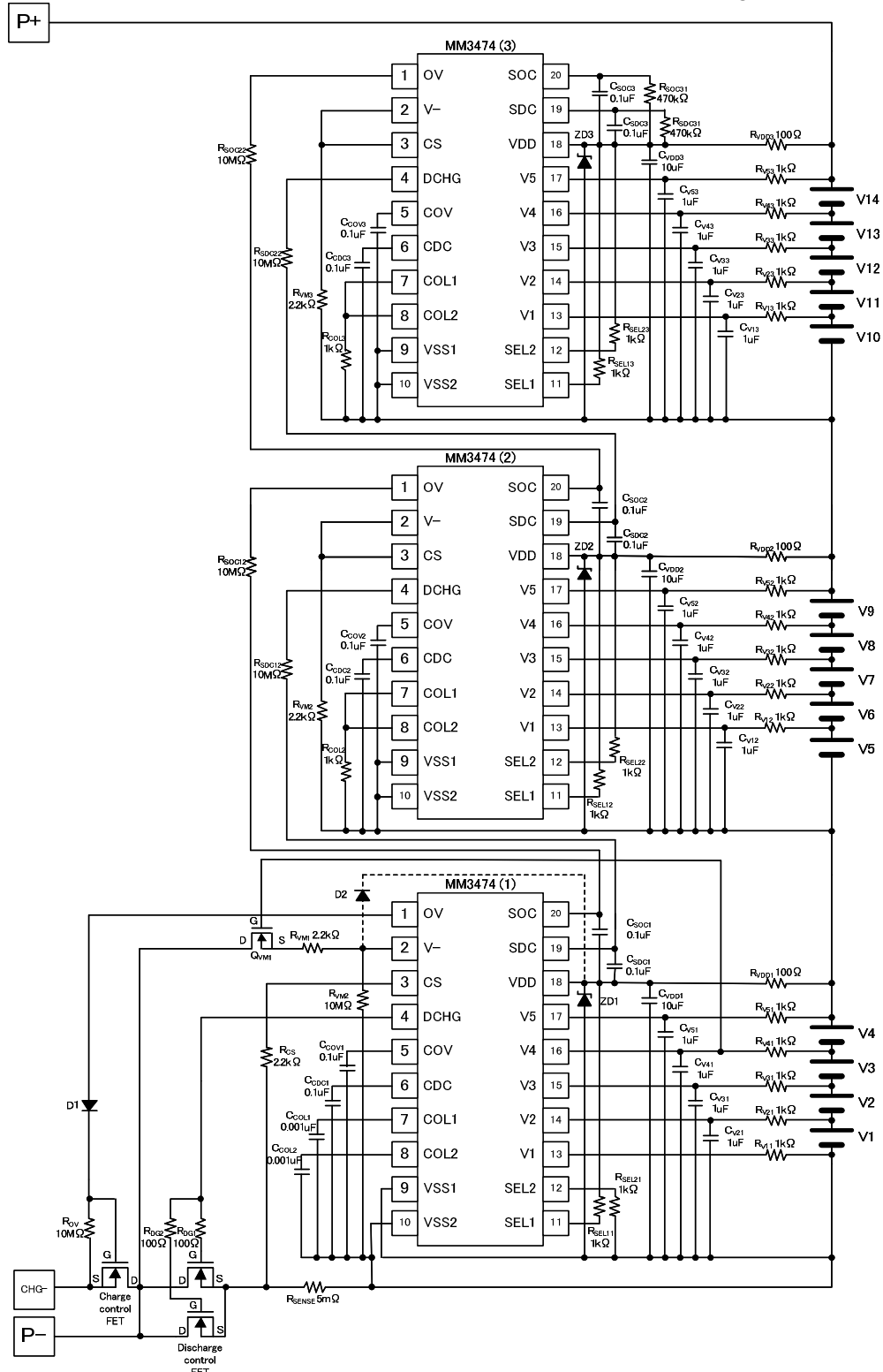
10. Examples of application circuit

10-11. Examples of 14 cells application circuit

10-11-1. Circuit condition 1

Circuit condition 1

- Number of cells : 14 cells (4cells + 5cells + 5 cells)
- Charge and discharge route : Separated
- Overdischarge release metho : Voltage release
- Optional functions : Nothing



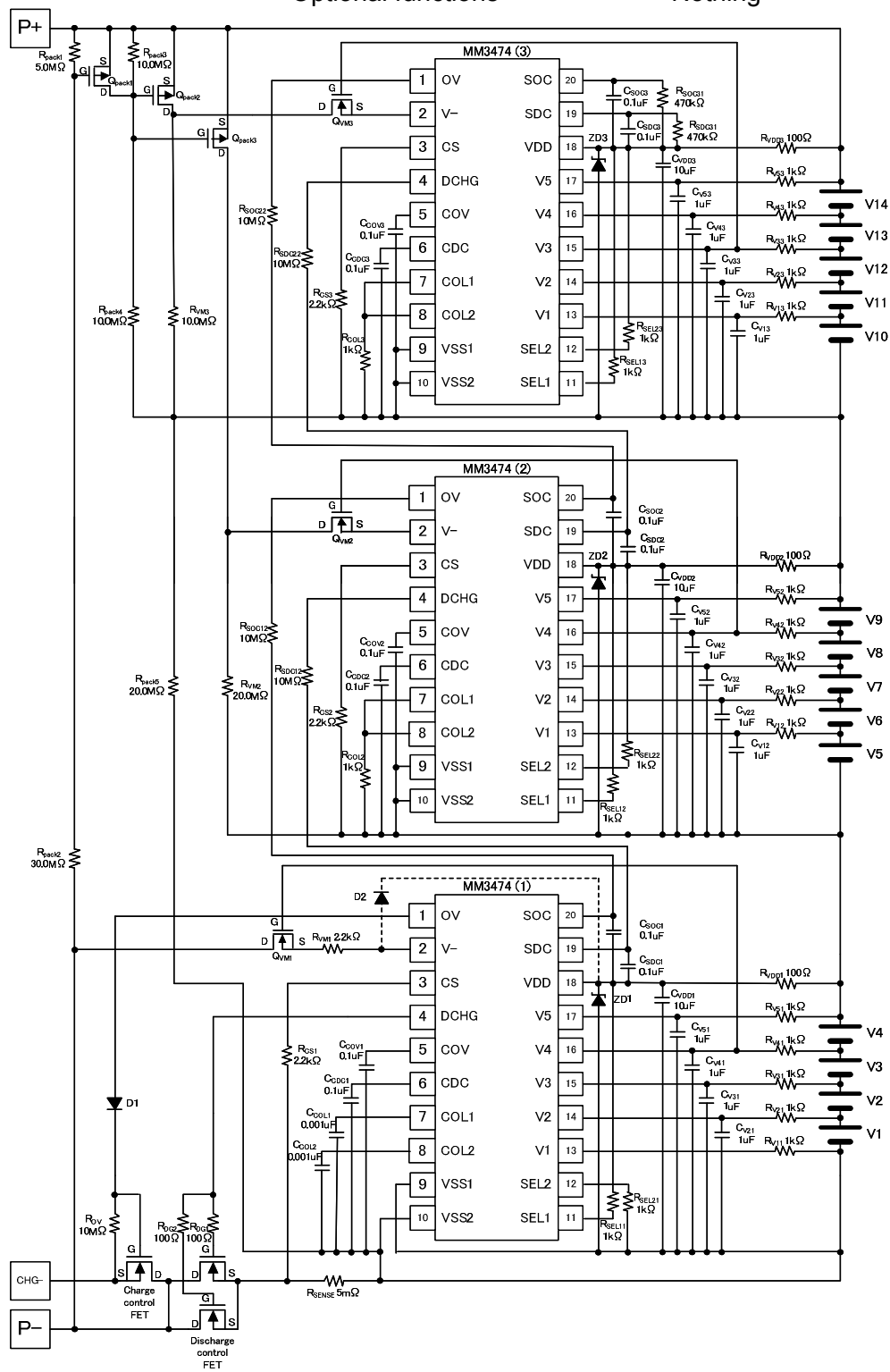
10. Examples of application circuit

10-11. Examples of 14 cells application circuit

10-11-2. Circuit condition 2

Circuit condition 2

- Number of cells : 14 cells (4cells + 5cells + 5 cells)
- Charge and discharge route : Separated
- Overdischarge release metho : Load release + Voltage release
- Optional functions : Nothing

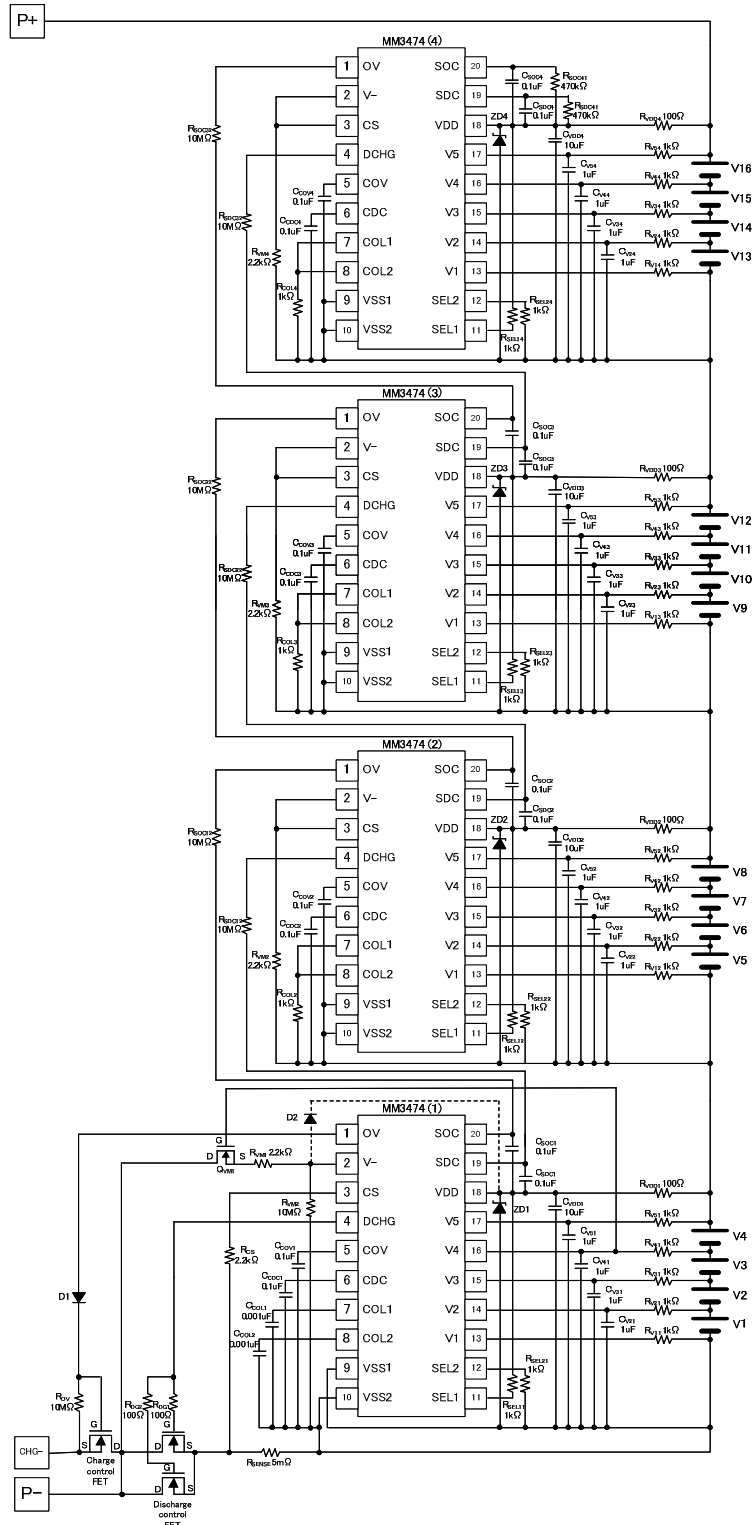


10. Examples of application circuit

10-12. Examples of 16 cells application circuit

10-12-1. Circuit condition 1 Circuit condition 1

- Number of cells : 16 cells (4cells+4cells+4cells+4cells)
- Charge and discharge route : Separated
- Overdischarge release metho : Voltage release
- Optional functions : Nothing

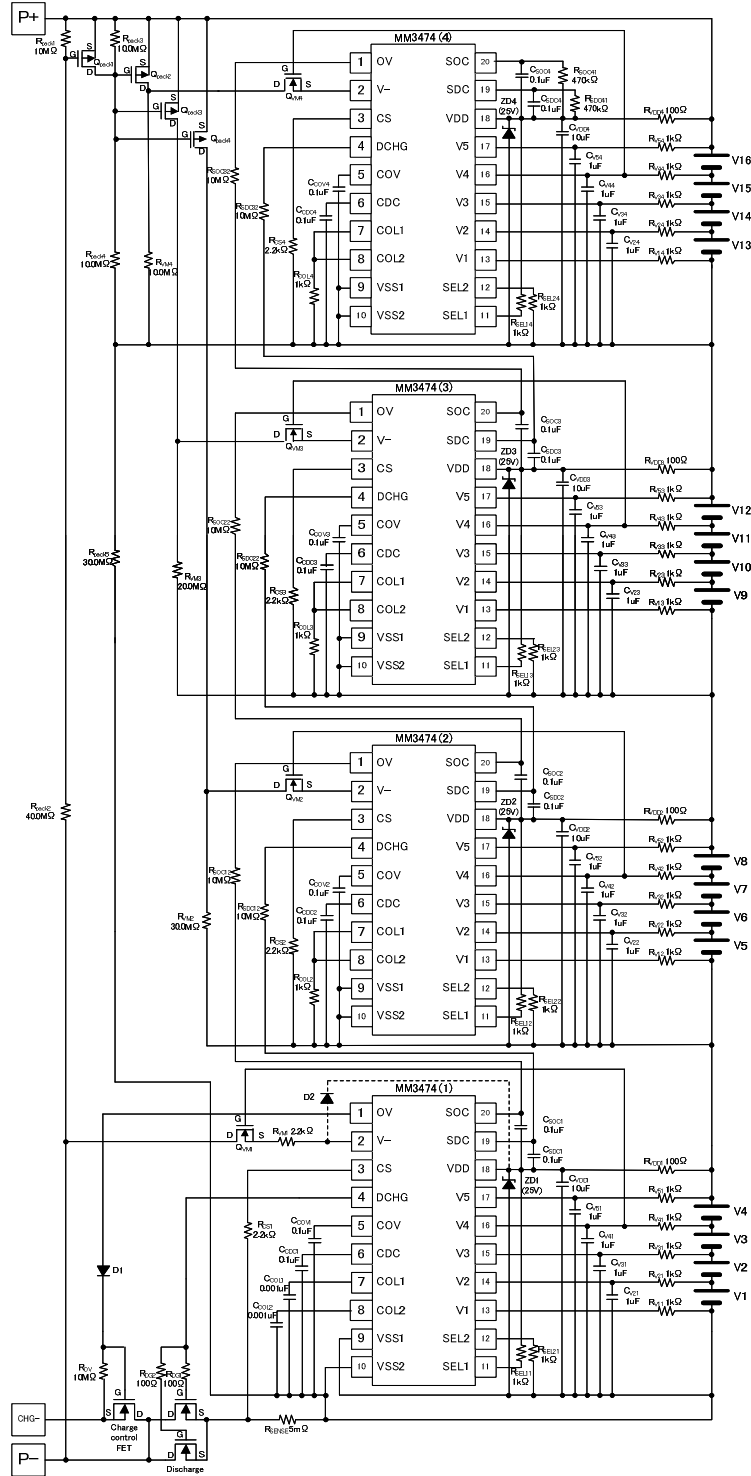


10. Examples of application circuit

10-12. Examples of 16 cells application circuit

10-12-2. Circuit condition 2 Circuit condition 2

- Number of cells : 16 cells (4cells+4cells+4cells+4cells)
- Charge and discharge route : Separated
- Overdischarge release metho : Load release + Voltage release
- Optional functions : Nothing

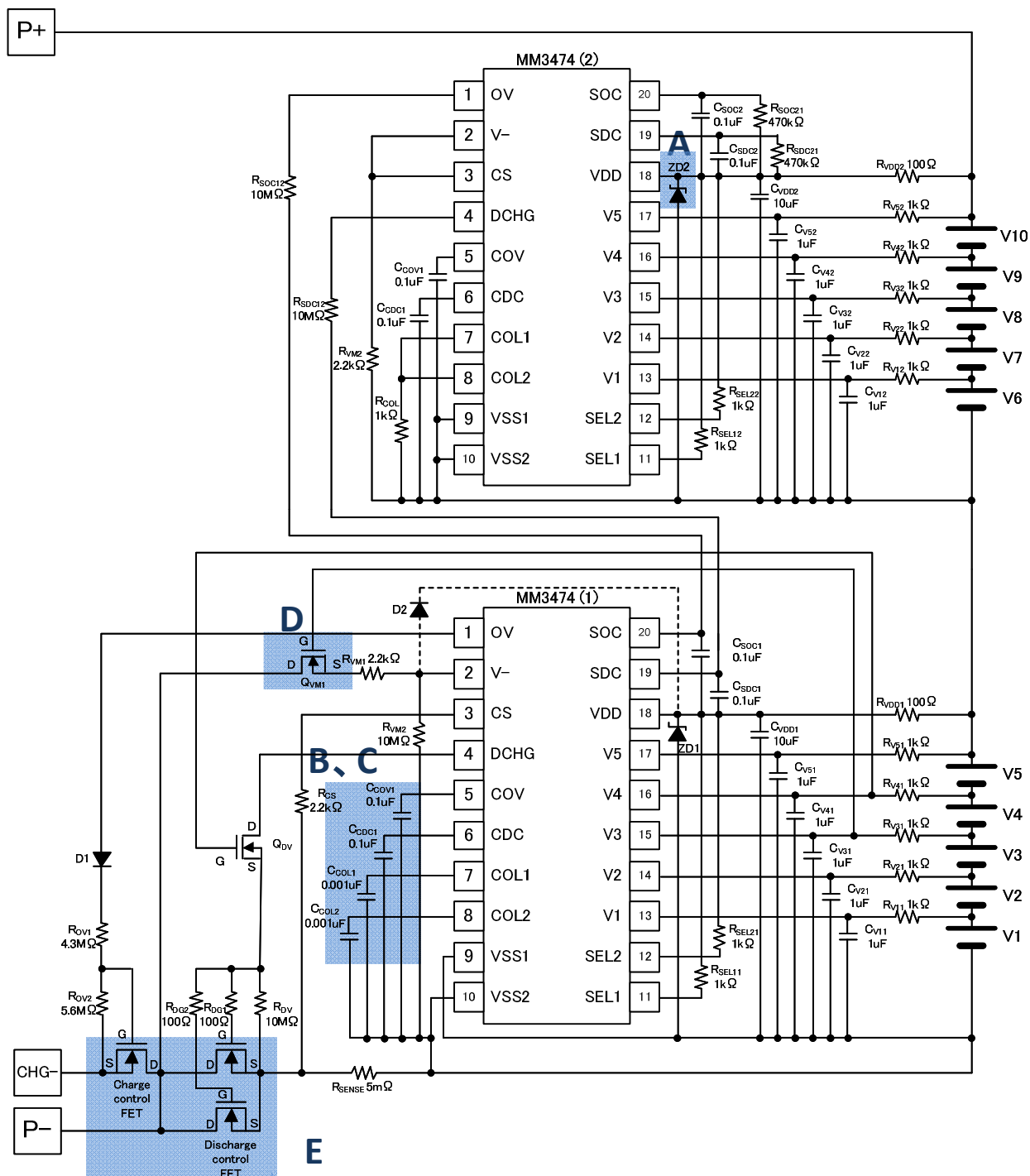


11. Selecting methods

Based on the following application circuits for 10-cells, recommended ranges and selecting methods for peripheral parts are shown on the Page 2 and 3. Please refer the recommended constants of parts to the following circuit example.

(1) Example of application circuit for MM3474 for 10-cells

※ A - E has matters that require attention in the use.



*This circuit is a representative application example as a reference.

Please use this IC after sufficient consideration of resistance, permissible loss and electrostatic resistance of each parts depending on the actual use environment and conditions.

11. Selecting methods

(2) Recommended range and selection method for parts

Circuit symbol	Recommended range	Selection method
R_{VDD1}	$R_{VDDx} * C_{VDDx} \rightarrow 200\mu s$ or more $R_{VDDx} \rightarrow 500\Omega$ or less	These are RC low pass filters to restrain power supply of VDD pin from changing . To prevent malfunction, please set the time constant to 200 μs or more, and resistance value to 500 Ω or less. Please adjust the filter time constant of VDD pin with those of V5 to V1 pins.
C_{VDD1}		
R_{VDD2}		
C_{VDD2}		
R_{V51}	$R_{V5x} * C_{V5x} = R_{VDDx} * C_{VDDx}$ $R_{V5x} \rightarrow 1k\Omega$ or less	These are RC low pass filters to restrain power supply of V5 pin from changing. Please adjust the filter time constant of VDD pin with those of V5 to V1 pins. When supply voltage changes precipitously, V5 pin voltage beyond VDD to make parasitic element inside the IC operates, which causes malfunction. In order to prevent the voltage detecting of overcharge and overdischarge from being misaligned, please set the resistance value to 1k Ω or less.
C_{V51}		
R_{V52}		
C_{V52}		
R_{V41}	$R_{VDDx} * C_{VDDx} = R_{V5x} * C_{V5x}$ $= R_{V4x} * C_{V4x}$ $R_{V4x} \rightarrow 1k\Omega$ or less	These are RC low pass filters to restrain power supply of V4 pin from changing. Please adjust the filter time constant of VDD pin with those of V5 to V1 pins. In order to prevent voltage detecting of overcharge and overdischarge from being misaligned, please set the resistance value to 1k Ω or less.
C_{V41}		
R_{V42}		
C_{V42}		
R_{V31}	$R_{VDDx} * C_{VDDx} = R_{V5x} * C_{V5x}$ $= R_{V3x} * C_{V3x}$ $R_{V3x} \rightarrow 1k\Omega$ or less	These are RC low pass filters to restrain power supply of V3 pin from changing. Please adjust the filter time constant of VDD pin with those of V5 to V1 pins. In order to prevent the voltage detecting of overcharge and overdischarge from being misaligned, please set the resistance value to 1k Ω or less.
C_{V31}		
R_{V32}		
C_{V32}		
R_{V21}	$R_{VDDx} * C_{VDDx} = R_{V5x} * C_{V5x}$ $= R_{V2x} * C_{V2x}$ $R_{V2x} \rightarrow 1k\Omega$ or less	These are RC low pass filters to restrain power supply of V2 pin from changing. Please adjust the filter time constant of VDD pin with those of V5 to V1 pins. In order to prevent the voltage detecting of overcharge and overdischarge from being misaligned, please set the resistance value to 1k Ω or less.
C_{V21}		
R_{V22}		
C_{V22}		
R_{V11}	$R_{VDDx} * C_{VDDx} = R_{V5x} * C_{V5x}$ $= R_{V1x} * C_{V1x}$ $R_{V1x} \rightarrow 1k\Omega$ or less	These are RC low pass filters to restrain power supply of V1 pin from changing. Please adjust the filter time constant of VDD pin with those of V5 to V1 pins. In order to prevent voltage detecting of overcharge and overdischarge from being misaligned, please set the resistance value to 1k Ω or less.
C_{V11}		
R_{V12}		
C_{V12}		
R_{SEL11}	1k Ω ~ 100k Ω	These are resistances to protect SEL1 pin and SEL2 pin. Please note that noise may cause malfunction when the resistance value is large.
R_{SEL21}		
R_{SEL12}		
R_{SEL22}		
R_{SENSE}	-	This is a sense resistance for overcurrent detection. Overcurrent detection current $I_{OC} = \text{Overcurrent detection voltage } V_{OC} / \text{Sense resistance: } R_{SENSE}$ Please set the wattage of R_{SENSE} to $I_{OC} * V_{OC}$ or more.
R_{VM1}	1k Ω ~ 10k Ω	These are pin protection resistance for V-pin. In order to prevent discharge overcurrent release voltage from being misaligned, please set it to 10k Ω or less.
R_{VM2}		
Q_{VM1}	-	This is a Nch MOS FET to prevent V-pin from increasing to VDD pin voltage or more. Even though when P- increases to VDD pin voltage or more, the maximum voltage of V-pin is limited. Please select the resistance voltage between the gate and source of FET to 20V or more; and please select the FET between drain and source with sufficient margin against the estimated voltage between P+ and P-.
R_{CS}	1k Ω ~ 10k Ω	This is a resistance to protect CS pin. In order to prevent the detection voltage of discharge overcurrent and short from being misaligned, please set the resistance value to 10k Ω or less.

11. Selecting methods

(2) Recommended range and selection method for parts

Circuit symbol	Recommended range	Selection method
R_{DV}	$R_{DV} = 1M\Omega \sim 10M\Omega$	These are resistance and Nch MOS FET to limit the voltage between the gate and source of discharge control FET. The voltage between the gate and source of discharge control FET is limited with the voltage that decreased by the range of V_{gs} from the gate voltage of Q_{DV} . Current consumption is increased by current value of supply voltage and resistance value. Please select the resistance voltage between the gate and source of FET to 20V or more; and please select the FET between drain and source with sufficient margin against the estimated voltage between VDD and VSS of MM3474(1).
Q_{DV}	-	
R_{DG1}	$10\Omega \sim 100\Omega$	These are resistance to prevent FET from being destroyed by parasitic oscillation during switching DCHG pin. If FET is not used in parallel, it is not needed.
R_{DG2}		
R_{OV1}	$R_{OV1} + R_{OV2} \cong 10M\Omega$	These are resistances to divide the pull down resistance and output voltage of OV pin. Please set the partial pressure not to over the resistance voltage between gate and source of charging control as appropriately. If it does not need to divide voltage, ROV1 is not necessary. Please be careful if the total resistance value is small, it may not return from discharge overcurrent and short.
R_{OV2}		
D1	-	This is a diode to prevent current from flowing into OV pin, when P- is VDD pin voltage or more. Please set a diode with sufficient margin against the voltage between P+ and P- for the resistance voltage of opposite side.
R_{SDC21}	500k Ω or less	These are resistances to limit pin current of SDC pin. To prevent miss detection, it must be 500k Ω or less. When resistance value decreases, noise resistance increases and pin current also increases.
R_{SOC21}		
R_{SDC12}	8M \sim 14M	These are resistances to transmit the voltage signal of OV pin and DCHG pin to the lower SOC pin and SDC pin. Please set it to 14M Ω or less to prevent miss detection. Please pay attention, when it is 8M Ω or less, SDC and SOC pin may over VDD pin to cause malfunction.
R_{SOC12}		
C_{SDC1}	0.1 μ F	These are capacitors to prevent miss detection when VDD pin voltage changes suddenly.
C_{SDC2}		
C_{SOC1}		
C_{SOC2}		
C_{COV1}	100pF or more $C_{COL1}:C_{COL2} = 1:100 \sim 100:1$ $C_{CDC} > C_{COL1}$	These are capacitors to set insensitive time. Please set the constant number of capacitor depending on the insensitive time which you want to set. When the capacity value is 100pF or less, circuit delay affects insensitive time. Please confirm the actual application before using.
C_{CDC1}		
C_{COL1}		
C_{COL2}		
C_{COV2}		
C_{CDC2}		
C_{COV3}		
C_{CDC3}		
ZD1	24 \sim 30V	This is a zener diode to prevent IC from being destroyed by surge voltage.
D2	-	This is a diode to prevent the current from flowing into the parasite element inside of IC even when V pin increases up to VDD pin or more. When it is beyond cramping lower than the VDD pin voltage because of the parasitic inductance elements of board etc., please insert it depending on the necessity. Schottky diode is recommended.

*The above constants provide no guarantees for actual operation. Sufficient evaluation with actual application is needed before selecting the constant.

12. Instructions and directions for use

- A. In order to prevent IC destruction by surge voltage, it is recommended to insert zener diode where is close to the pin between VDD and VSS of IC.
- B. If overdischarge release method is voltage release type, please set $CCDC > CCOL1$, in order that overcurrent detection delay time becomes shorter than overdischarge detection delay time. When cell voltage becomes less than overdischarge detection voltage during over current discharge and overdischarge is detected before overcurrent, overdischarge detection and release may be repeated.
- C. If the method of overcharge release is voltage release type and the range of voltage changed by charge current and cell impedance is larger than overcharge hysteresis voltage, overcharge detection and release are repeated. With consideration of heat value of charge control FET, please set the C_{COV} value.
- D. Q_{VM1} is a part to clamp in order to prevent the voltage which is input to V-pin from exceeding the maximum rating. In any case which P- increases more than VDD, the maximum voltage of V-pin is kept as below value.
V-pin voltage < Gate voltage of Q_{VM1} - Gate cut off voltage of Q_{VM1}
With consideration of minimum voltage of cells under each detection condition, please choose Q_{VM1} which meets the following conditions without fail.
- (1) $VDD - (\text{Gate voltage of } Q_{VM1} - \text{Gate cut off voltage of } Q_{VM1}) > 1.5V$ *when overdischarge is detected
output circuit is 1.5V. When the voltage between VDD pin and V-pin becomes 1.5V or less, output of OV pin may be high impedance.
For the circuit of which charge and discharge route is separated, the voltage of V-pin may not be lowered even battery charger is connected and battery may not be able to be charged.
- (2) $\text{Gate voltage of } Q_{VM1} - \text{Gate cut off voltage of } Q_{VM1} > V_{VM}$ *When overcurrent or short detected
If V-pin voltage doesn't increase beyond V_{VM} during overcurrent or short detection, detection condition may not be maintained and detection and release may be repeated .
Voltage of the total voltage of all cells or more may be impressed between the source of Q_{VM1} and drain.
Please select parts with sufficient margin of Q_{VM1} resistance voltage.
- E. It is recommended to branch the wiring from the drain of charge and discharge control FET when charge and discharge route is divided.

13. Products line up list

Status of current IC	Product name (MM3474)	Detection / Release voltage						Detection / Release voltage						Optional function
		Overcharge detection voltage	Overcharge release voltage	Overdischarge detection voltage	Overdischarge release voltage	Overcurrent detection voltage	Short detection voltage	Overcharge detection dead time	Overcharge release dead time	Overdischarge detection dead time	Overdischarge release dead time	Overcurrent detection dead time	Overcurrent release dead time	Overdischarge release
		V _{CELLU}	V _{CELLO}	V _{CELLS}	V _{CELLD}	V _{OC}	V _{SHORT}	t _{OV1}	t _{OV2}	t _{DC1}	t _{DC2}	t _{OC1}	t _{OC2}	
		V	V	V	V	mV	V	sec	msec	sec	msec	msec	msec	
MP	C01VBE	4.250	4.150	2.800	3.000	250	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
MP	C02VBE	4.250	4.150	2.400	2.600	250	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
ES	C03VBE	4.250	4.150	2.800	3.000	250	0.80	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
ES	C04VBE	4.250	4.150	2.800	3.000	150	0.25	1.0	0.1	1.0	Max.15	10.0	10.0	Latch
ES	C05VBE	4.250	4.150	2.800	3.000	150	0.25	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
MP	D01VBE	3.850	3.650	2.300	2.500	150	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
MP	D03VBE	3.800	3.600	2.000	2.500	150	0.60	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
ES	E01VBE	4.250	4.150	2.800	3.000	150	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
ES	E02VBE	4.200	4.100	2.800	3.000	150	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
ES	E03VBE	4.175	4.100	2.800	3.000	150	0.50	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
MP	E04VBE	4.250	4.150	2.800	3.000	100	0.50	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
MP	E05VBE	4.250	4.150	2.800	3.000	50	0.40	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
MP	F01VBE	4.250	4.150	2.500	3.000	150	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
ES	F02VBE	4.200	4.100	2.500	3.000	100	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
MP	F03VBE	4.250	4.150	2.500	3.000	100	0.30	1.0	0.1	1.0	Max.15	10.0	10.0	Latch
MP	F04VBE	4.250	4.210	2.500	3.000	100	0.80	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
MP	F05VBE	4.250	4.150	2.500	3.000	100	0.25	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
ES	F06VBE	4.225	4.150	2.000	3.000	50	0.20	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
ES	F08VBE	4.400	4.300	2.500	3.000	120	0.25	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
ES	F11VBE	4.400	4.300	2.500	3.000	150	0.50	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
ES	F12VBE	4.250	4.150	2.500	3.000	200	0.50	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
MP	G01VBE	4.200	4.100	2.750	3.000	100	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
MP	G02VBE	4.250	4.150	2.750	3.000	100	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
MP	G03VBE	4.200	4.100	2.750	3.000	100	0.40	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
MP	G05VBE	4.250	4.150	2.750	3.000	100	0.40	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
MP	G06VBE	4.225	4.100	2.750	3.000	100	0.80	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
MP	G07VBE	4.250	4.150	2.750	3.000	100	0.20	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
ES	J01VBE	4.250	4.100	2.800	3.000	50	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
ES	K02VBE	4.250	4.100	3.000	3.225	100	0.40	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch

※1 Non Latch : voltage release Latch : voltage release + load remove

Please inquire to us, if you request a rank other than the above.

13. Products line up list

Status of current IC	Product name (MM3474)	Detection / Release voltage						Detection / Release voltage						Optional function
		Overcharge detection voltage	Overcharge release voltage	Overdischarge detection voltage	Overdischarge release voltage	Overcurrent detection voltage	Short detection voltage	Overcharge detection dead time	Overcharge release dead time	Overdischarge detection dead time	Overdischarge release dead time	Overcurrent detection dead time	Overcurrent release dead time	Overdischarge release
		V _{CELLU}	V _{CELLO}	V _{CELLS}	V _{CELLD}	V _{OC}	V _{SHORT}	t _{OV1}	t _{OV2}	t _{DC1}	t _{DC2}	t _{OC1}	t _{OC2}	
		V	V	V	V	mV	V	sec	msec	sec	msec	msec	msec	
ES	K03VBE	4.250	4.190	3.000	3.200	80	0.70	1.0	0.1	1.0	Max.15	10.0	10.0	Latch
MP	K04VBE	4.175	4.100	3.000	3.200	100	0.50	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
MP	L02VBE	3.750	3.550	2.200	2.700	100	0.40	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
MP	L03VBE	3.650	3.500	2.000	2.700	200	0.25	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
ES	L04VBE	3.750	3.550	2.200	2.700	100	0.40	1.0	0.1	1.0	Max.15	10.0	10.0	Latch
MP	M01VBE	4.350	4.150	2.300	3.000	150	0.50	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
ES	N01VBE	3.900	3.600	2.000	3.000	100	0.20	1.0	0.1	1.0	Max.15	10.0	10.0	Latch
MP	P03VBE	4.230	4.220	2.800	3.400	100	0.80	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
ES	P04VBE	4.200	4.170	2.750	2.800	100	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
MP	P05VBE	4.200	4.140	2.750	2.810	100	0.50	1.0	0.1	1.0	Max.15	10.0	10.0	Latch
ES	P06VBE	4.230	4.220	2.800	3.000	100	0.80	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
MP	S01VBE	3.600	3.500	2.800	3.000	100	0.40	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch

※1 Non Latch : voltage release

Latch : voltage release + load remove

Please inquire to us, if you request a rank other than the above.

14. Introduction of releted products

14-1. MM3220V series : 2-Cells Li-ion Battery protection IC

•Outline

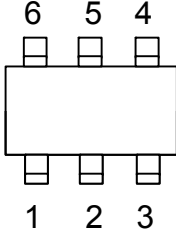
MM3220V series are used by an application of 6- cells and 7- cells etc in cascade connection with MM3474 series. It's possible to make it the composition in low cost and space-saving by using MM3220 V series.It's connected with MM3474 easily by making the output form a Pch open drain.

•Main characteristics

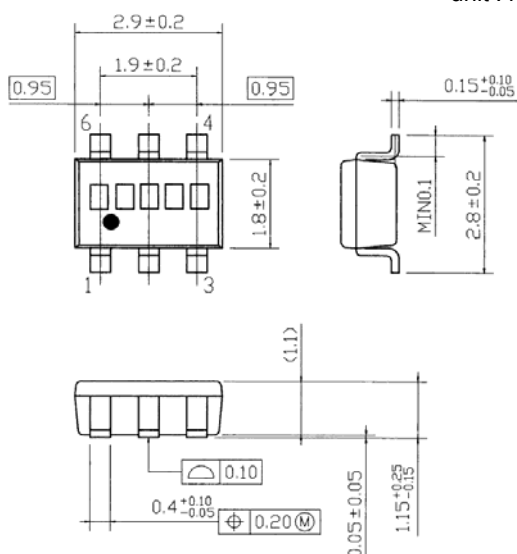
Overcharge detection voltage	3.6V~4.5V, 5mV steps	Accuracy±25mV (Topr=-5~+60°C)
Overcharge release voltage	3.4V~4.5V, 50mV steps	Accuracy±50mV
Overdischarge detection voltage	2.0V~3.0V, 50mV steps	Accuracy±80mV
Overdischarge release voltage	2.0V~3.4V, 50mV steps	Accuracy±100mV

•Package outline and PIN configuration

MM3220V series PIN configuration ... SOT-26A

Top view	Pin No.	Symbol	Function
	1	DOUT	Output of overdischarge detection. Output type is Pch open drain.
	2	COUT	Output of overcharge detection. Output type is Pch open drain.
	3	V-	Input terminal connected to charger negative voltage.
	4	VBL	Input terminal of the low side cell.
	5	VDD	Input terminal of the high side cell. Supply terminal.
	6	VSS	VSS terminal. Connected to ground

unit : mm



SOT-26A

14. Introduction of releted products

14-2. MM3513 series : Voltage monitor IC for Li-ion cell balance

•Outline

It's possible to add a cell balance control function by connecting MM3513 to each cell.
When MM3513 senses that the cell voltage exceeds detecting voltage, Cell balance control is performed by bypassing charging current of the cell by NchMOSFET and external resistance.

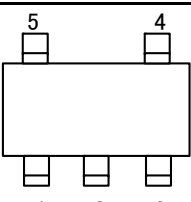
•Main characteristics

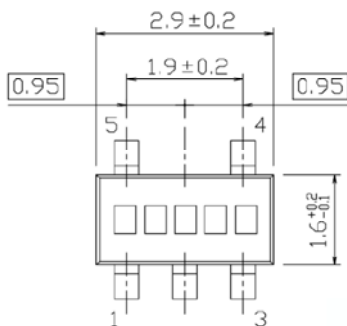
detection voltage 3.5V~4.5V, 5mV steps

Accuracy±20mV,

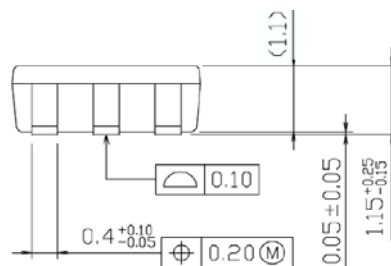
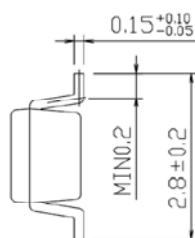
Accuracy±25mV (Topr=-5~+60°C)

•Package outline and PIN configuration

Top view SOT-25A	Pin No.	Symbol	Function
	1	NC	No connection.
	2	VDD	Connected to IC substrait.
	3	VSS	Connected to ground.
	4	DS	Delay shorten terminal.
	5	OUT	Output of detecting voltage. Output type is CMOS.



SOT-25A



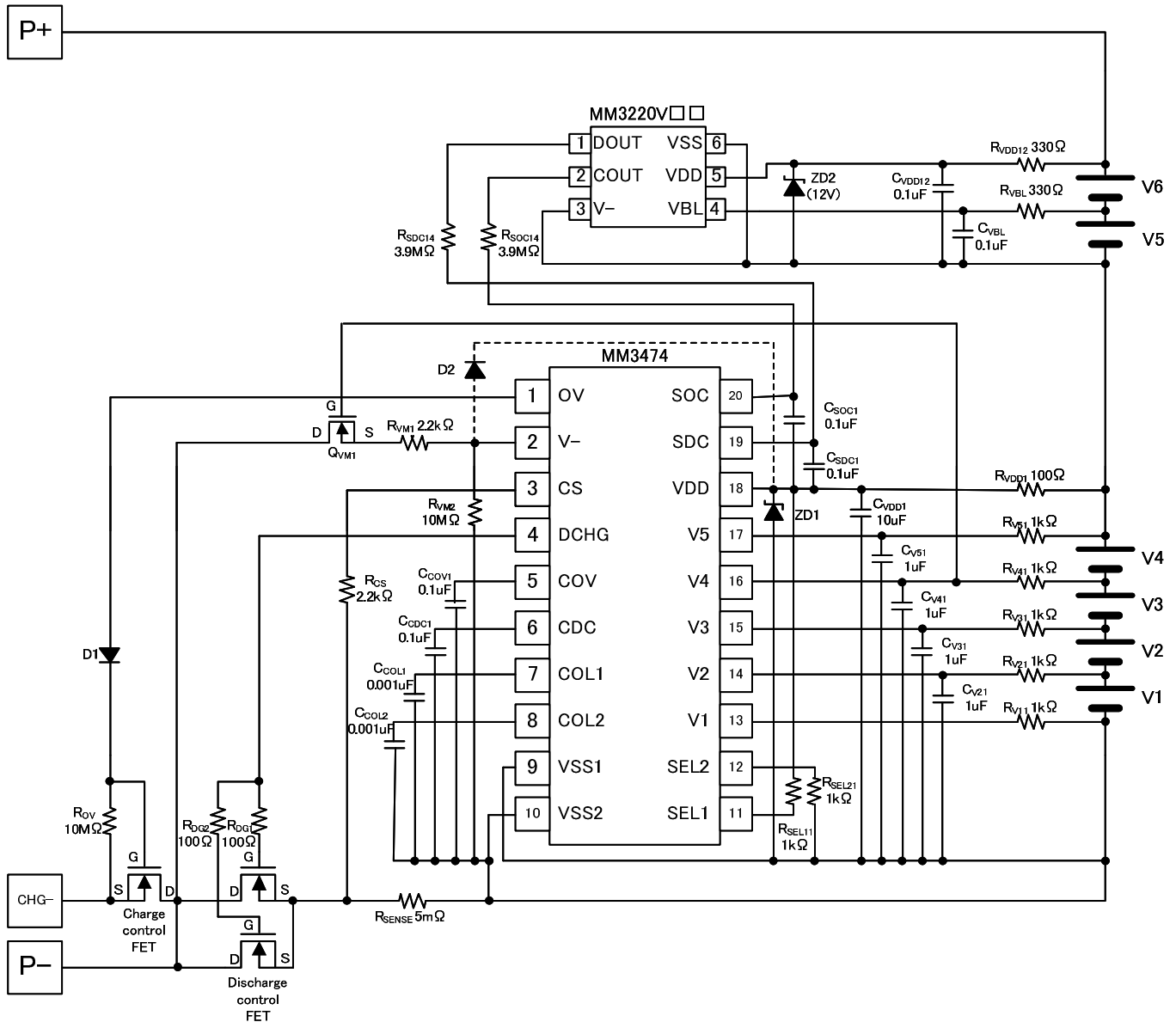
unit : mm

15. Examples of circuit using related products

15-1. Examples of circuit using 2cell protection MM3220V

15-1-1. Circuit condition 1 Circuit condition 1

- Number of cells : 6cells (4cells+2cells)
- Charge and discharge route : Separated
- Overdischarge release methc : Voltage release
- Optional functions : Nothing

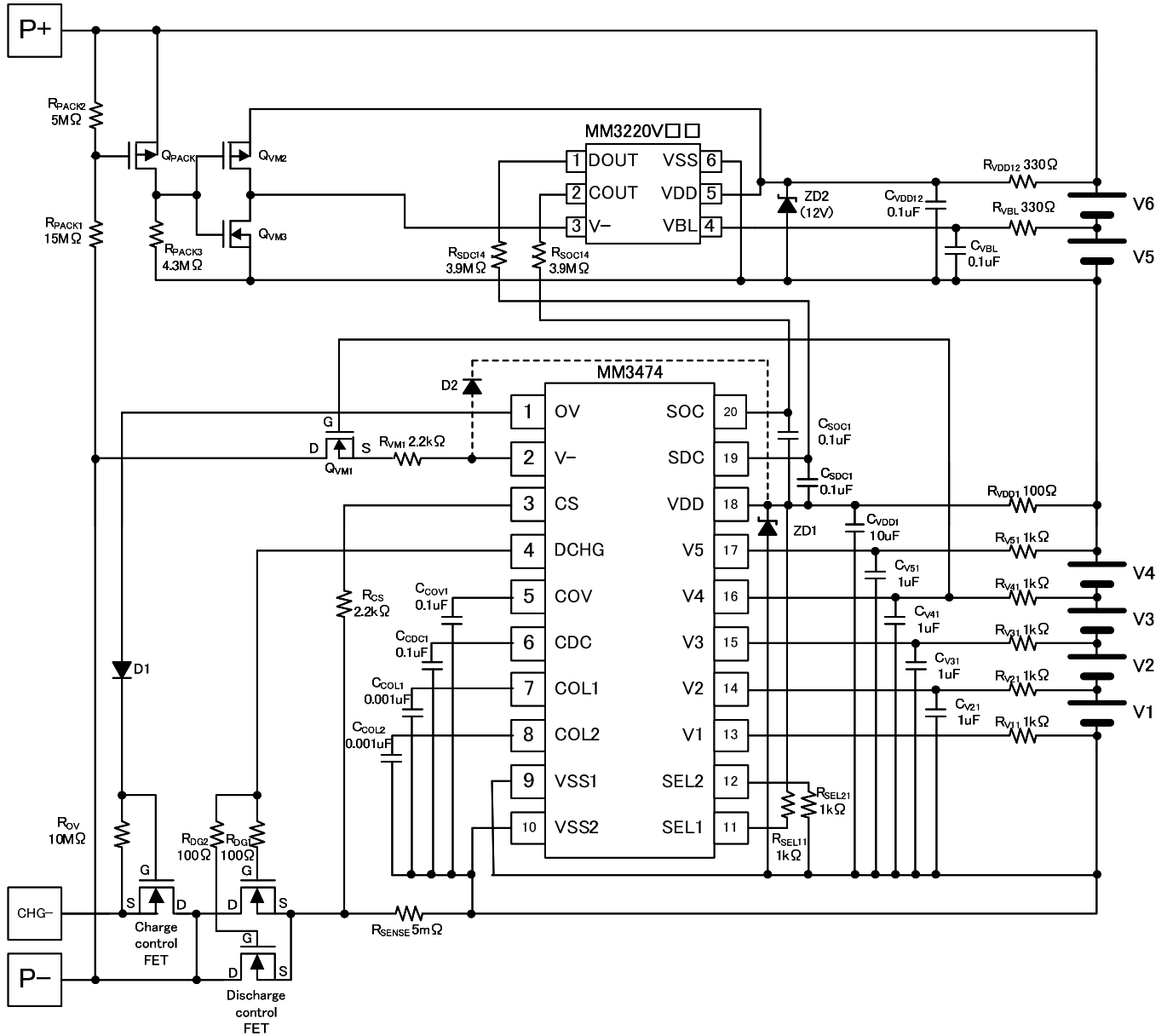


15. Examples of circuit using related products

15-1. Examples of circuit using 2cell protection MM3220V

15-1-2. Circuit condition 2 Circuit condition 2

- Number of cells : 6cells (4cells+2cells)
- Charge and discharge route : Separated
- Overdischarge release methc : Load release + Voltage release
- Optional functions : Nothing

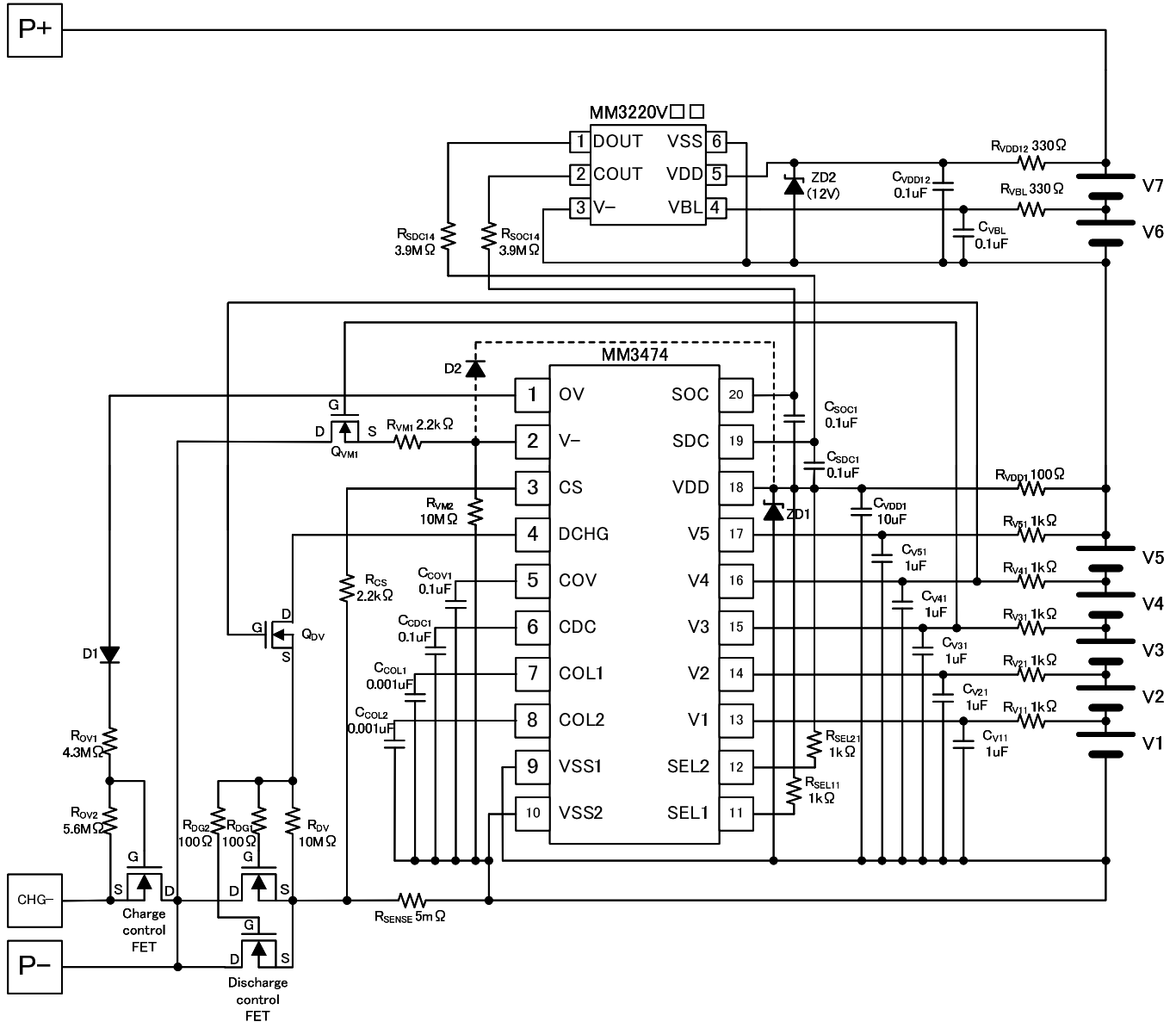


15. Examples of circuit using related products

15-1. Examples of circuit using 2cell protection MM3220V

15-1-3. Circuit condition 3 Circuit condition 3

- Number of cells : 7cells (5cells+2cells)
- Charge and discharge route : Separated
- Overdischarge release methc : Voltage release
- Optional functions : Nothing

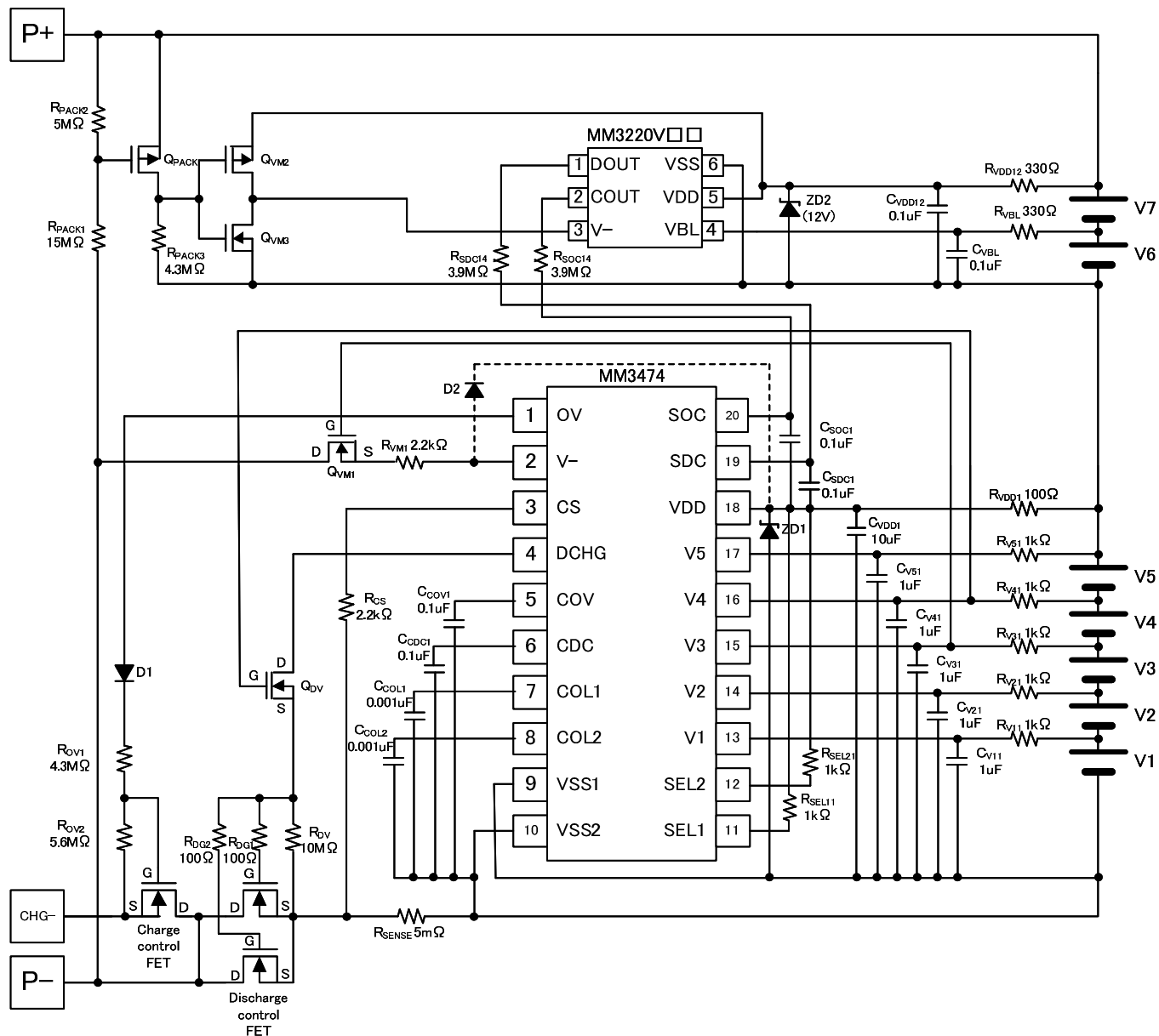


15. Examples of circuit using related products

15-1. Examples of circuit using 2cell protection MM3220V

15-1-4. Circuit condition 4 Circuit condition 4

- Number of cells : 7cells (5cells+2cells)
- Charge and discharge route : Separated
- Overdischarge release methc : Load release + Voltage release
- Optional functions : Nothing

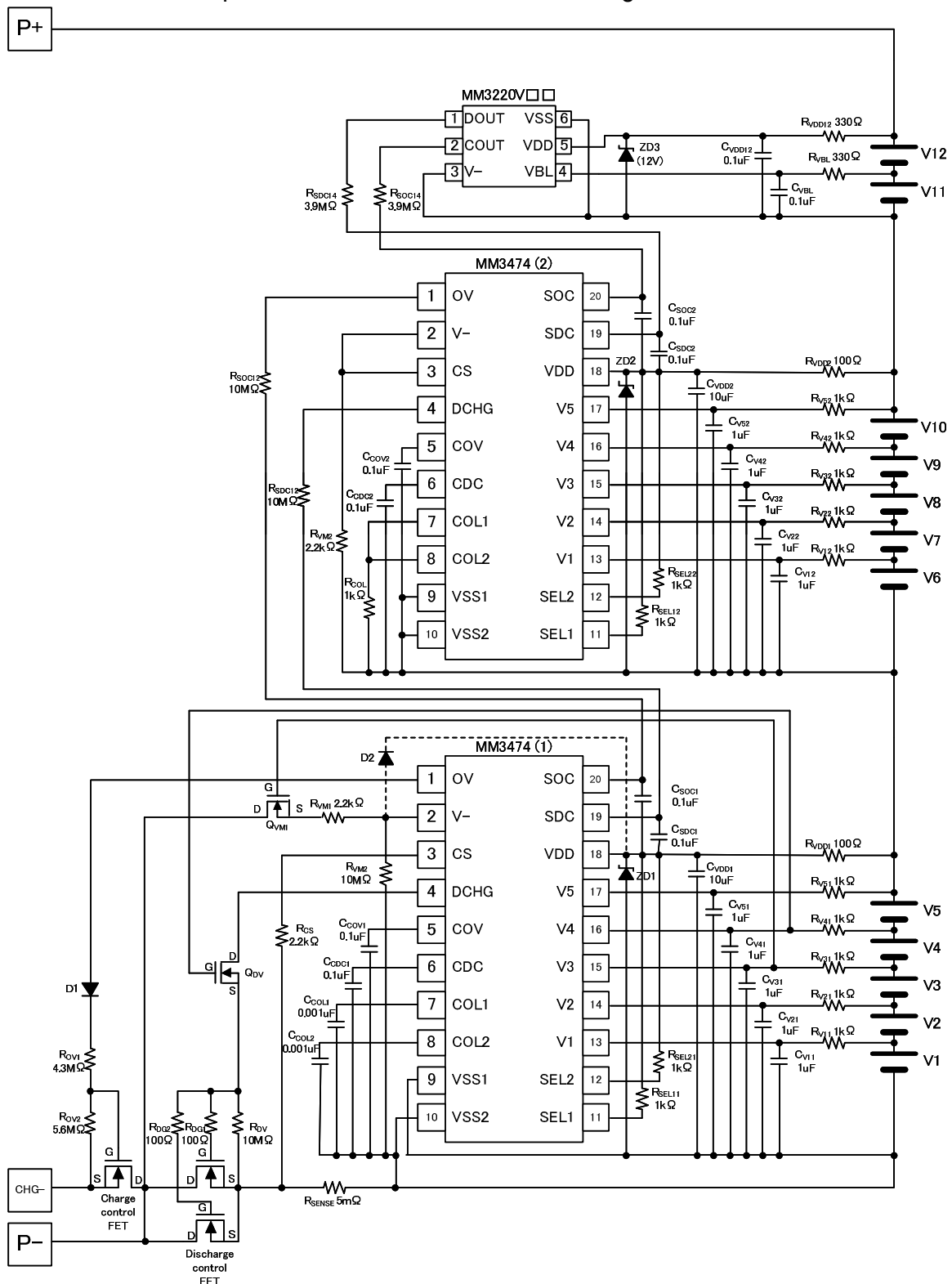


15. Examples of circuit using related products

15-1. Examples of circuit using 2cell protection MM3220V

15-1-5. Circuit condition 5 Circuit condition 5

- Number of cells : 12cells (5cells+5cells+2cells)
- Charge and discharge route : Separated
- Overdischarge release methcd : Voltage release
- Optional functions : Nothing

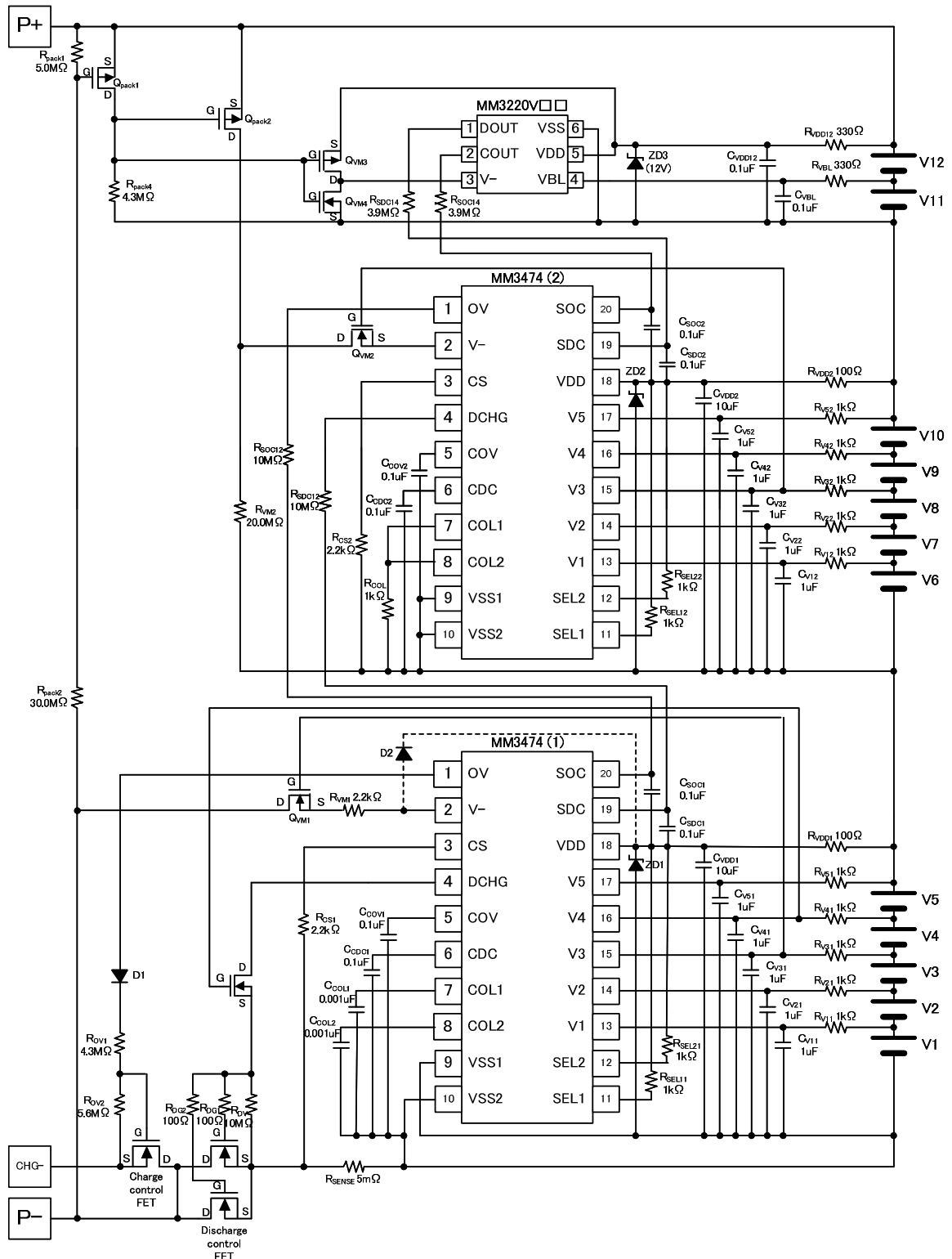


15. Examples of circuit using related products

15-1. Examples of circuit using 2cell protection MM3220V

15-1-6. Circuit condition 6 Circuit condition 6

- Number of cells : 12cells (5cells+5cells+2cells)
- Charge and discharge route : Separated
- Overdischarge release methc : Load release + Voltage release
- Optional functions : Nothing

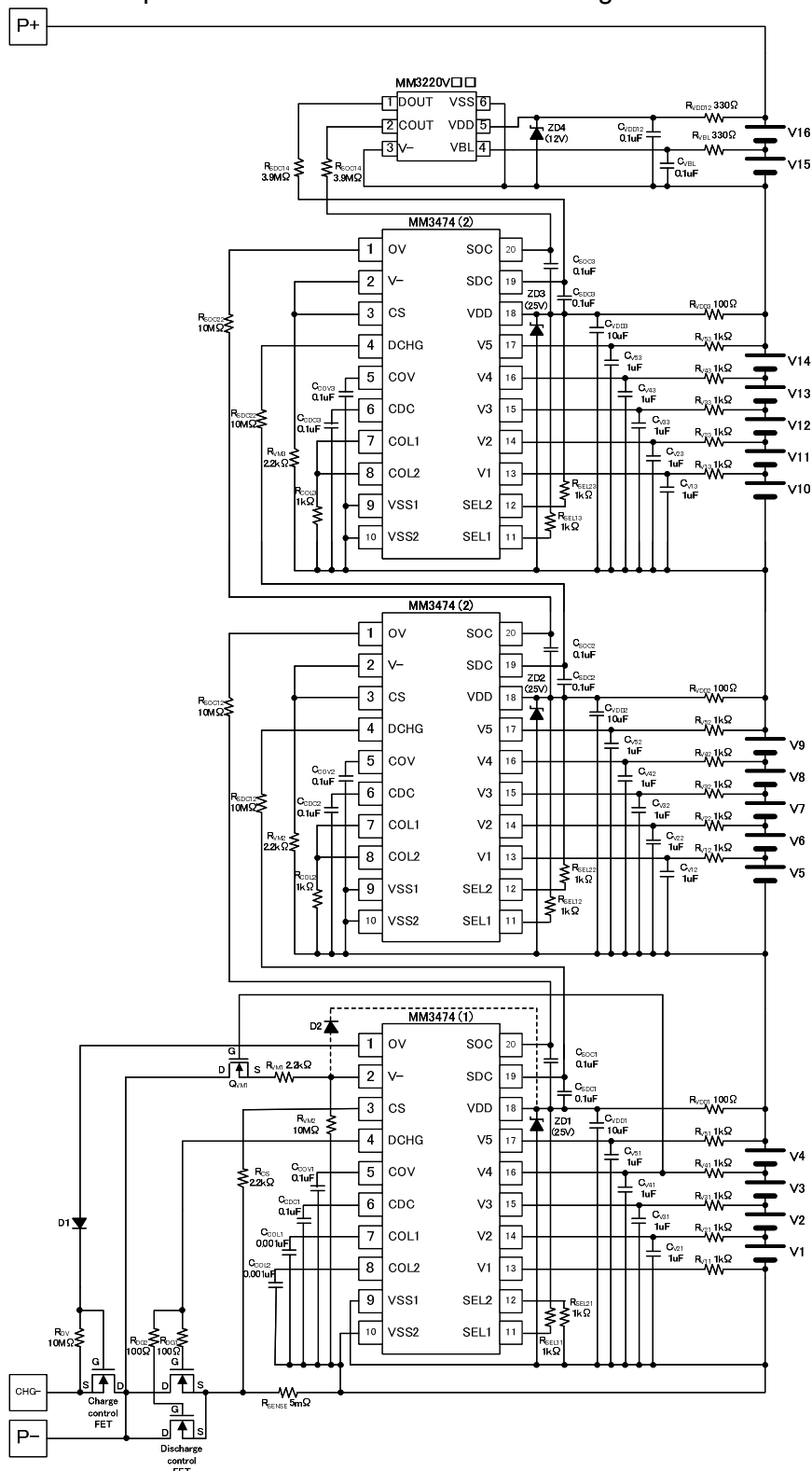


15. Examples of circuit using related products

15-1. Examples of circuit using 2cell protection MM3220V

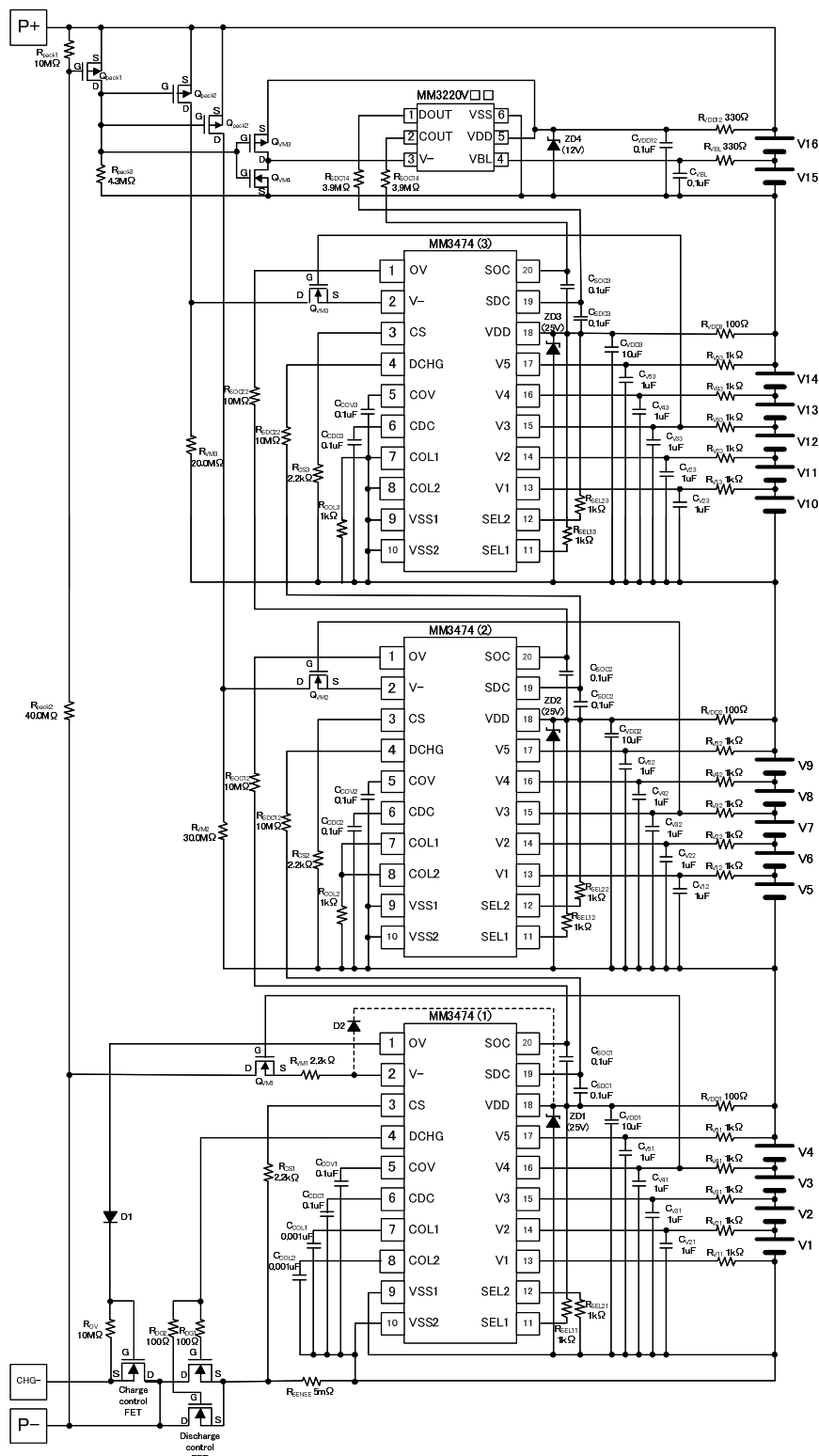
15-1-7. Circuit condition 7 Circuit condition 7

- Number of cells : 16cells (4cells+5cells+5cells+2cells)
- Charge and discharge route : Separated
- Overdischarge release methc : Voltage release
- Optional functions : Nothing



15-1-8. Circuit condition 8 Circuit condition 8

- Number of cells : 16cells (4cells+5cells+5cells+2cells)
- Charge and discharge route : Separated
- Overdischarge release methc : Load voltage + Voltage release
- Optional functions : Nothing

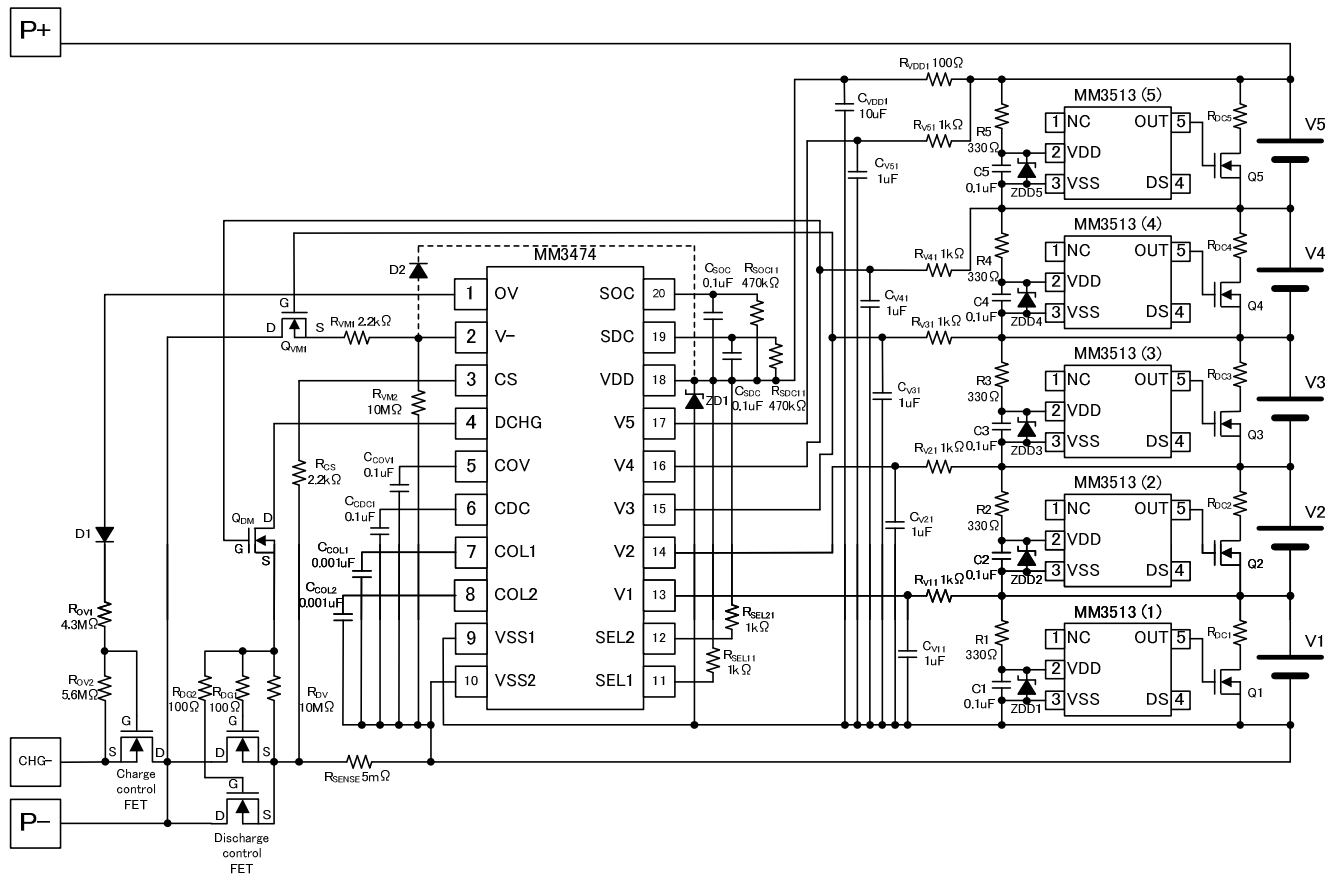


15. Examples of circuit using related products

15-2. Examples of circuit using cell balance MM3513

15-2-1. Circuit condition 1 Circuit condition 1

- Number of cells : 5cells
- Charge and discharge route : Separated
- Overdischarge release methc : Voltage release
- Optional functions : Cell balance

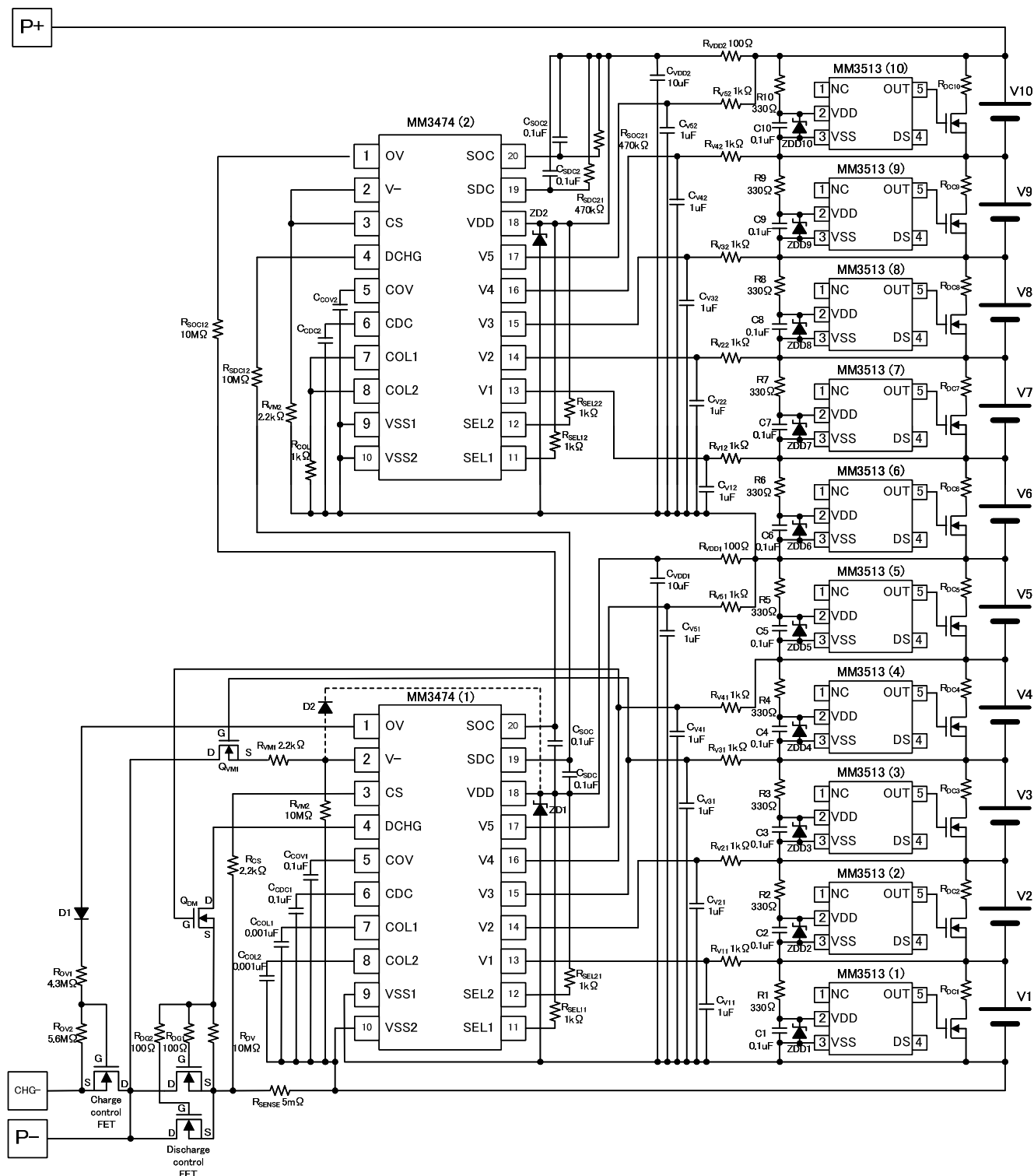


15. Examples of circuit using related products

15-2. Examples of circuit using cell balance MM3513

15-2-2. Circuit condition 2 Circuit condition 2

- Number of cells : 10cells (5cells + 5cells)
- Charge and discharge route : Separated
- Overdischarge release methc : Voltage release
- Optional functions : Cell balance



16. Line up list of related products

16-1. MM3220V serie product lineup

Product name (MM3220)	Detection / Release voltage				delay time		MM3474□□□VBE Correspondence rank
	Overcharge detection voltage	Overcharge release voltage	Overdischarge detection voltage	Overdescharge release voltage	Overcharge detection delay time	Overdischarge detection delay time	
	V	V	V	V	sec	sec	
V01NRH	4.250	4.150	2.800	3.000	1.0	1.0	C01/C03/C04/C05/E01/E04/E05
V02NRH	3.850	3.650	2.300	2.500	1.0	1.0	D01
V05NRH	4.250	4.150	2.500	3.000	1.0	1.0	F01/F03/F05
V06NRH	4.200	4.100	2.750	3.000	1.0	1.0	G01/G03
V07NRH	4.250	4.150	2.750	3.000	1.0	1.0	G02/G05/G07
V12NRH	3.750	3.550	2.200	2.700	1.0	1.0	L02/L04
V14NRH	3.900	3.600	2.000	3.000	1.0	1.0	N01
V15NRH	4.200	4.100	2.500	3.000	1.0	1.0	F02
V23NRH	4.200	4.170	2.750	2.800	1.0	1.0	P04

Please inquire to us, if you request a rank other than the above.

16. Line up list of related products

16-2. MM3513 serise product lineup

Product name (MM3513)	Detection voltage	Hysteresis voltage	Detection delay time	Release delay time
	V	V	sec	ms
A01NRH	4.150	0.010	0.25	8.0
B01NRH	3.750	0.010	0.25	8.0
C01NRH	4.200	0.010	0.25	8.0
D01NRH	3.600	0.010	0.25	8.0
D02NRH	3.600	0.100	0.25	8.0
F01NRH	3.650	0.010	0.25	8.0
H01NRH	4.175	0.010	0.25	8.0
J01NRH	3.475	0.010	0.25	8.0
K01NRH	4.180	0.010	0.25	4000.0
L01NRH	4.175	0.000	0.25	4000.0
R01NRH	4.210	0.010	0.25	8.0

Please inquire to us, if you request a rank other than the above.

17. Note

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This product is intended for applying to computers, OA units, communication units, instrumentation units, machine tools, industrial robots, AV units, household electrical appliances, and other general electronic units.

If any intend to apply this product to the units related to the control and safety of transportation units (vehicles, trains,etc.), traffic signaling units, disaster-preventive & burglar-proof units, or the like,section in charge of such a use in advance. you are requested to inform our sales

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The performance outline described herein is to explain standard performance and usage of integrated circuit.

No part of the contents contained herein may be reprinted or reproduced without our prior permission.

Please handle with care since the pins of this product may be subject to damage of electrostatic.

18. Related materials

Lithium-ion battery 3 to 5 cells protection IC	MM3474 data sheet
Lithium-ion battery 2 cells protection IC	MM3220 data sheet
Cell balance control IC	MM3513 data sheet

*The contents mentioned in this application note and data sheets are changed without notice.
Please contact to our sales department for the latest edition.