Datasheet
Rev 0, 4/2006
PRELIMINARY

ACT34

ACT34 — Primary Switching Regulator ActiveSwitcher™ IC Family

FEATURES

- Lowest Total Cost Solution
- <0.3W Standby Power
- 73% Peak Efficiency
- CEC Average Efficiency Higher than 65%
- Primary Side Feedback Only - No Optocoupler
- Exceeds California Energy Commission (CEC), European Union Blue Angel, and US Energy Star Standards
- Univeral AC Input
- Programmable Constant Voltage/Constant Current Operation
- Fewest Secondary Side Components
- Emitter Drive of NPN for Safe High Voltage Operation
- Over Power Protection
- Very Low Line and Load Regulation
- Short Circuit Fold Back Current Limit
- No Audible Noise
- Current Mode PWM Control
- Low EMI
- 65kHz Switching Frequency
- Tiny SOT23-6 Package

APPLICATIONS

- Battery Chargers
- Linear Adaptor Replacements
- RCC Adaptor Replacements
- CEC-Compliant Applications
- Standby Power Supplies
- Appliances

GENERAL DESCRIPTION

The ACT34 belongs to the high performance ActiveSwitcher™ family of primary switching regulators (PSR). Specially designed for cost-sensitive applications, the IC uses Active-Semi's patent-pending primary feedback control architecture to regulate the output voltage and current without the need of an opto-coupler or a reference device such as the '431.

Consuming less than 0.3W in standby, the ACT34 exceeds the California Energy Commission (CEC) average efficiency requirement, as well as surpasses the European Union Blue Angel and US Energy Star standards. The IC also features programmable constant voltage/constant current (CVCC) operation, over power protection, and fold back short circuit current limit.

The ACT34 is ideal and most cost effective for use in high performance universal input adaptors and chargers. Its tiny SOT23-6 package and unique architecture enable adaptor designs in smallest form factor.

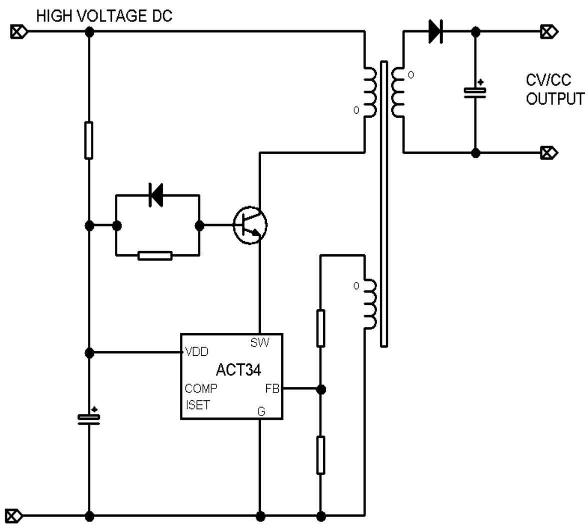
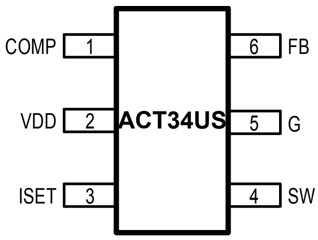


Figure 1. Simplified Application Circuit

ORDERING INFORMATION

PART NUMBER	TEMP RANGE	PACKAGE	PINS	PACKING METHOD	TOP MARK
ACT34US-T	-40°C to 85°C	SOT23-6	6	Tape & Reel	BMHK

PIN CONFIGURATION



SOT23-6

PIN DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	COMP	Compensation Pin
2	VDD	Power Supply
3	ISET	Current Setting Pin. Connect a resistor from this pin to G to set the constant current limit level.
4	SW	Switch Output. Connect to the emitter of the power NPN or source of the power FET.
5	G	Ground
6	FB	Feedback Pin

ABSOLUTE MAXIMUM RATINGS

(Note: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

PARAMETER	VALUE	UNIT
VDD Supply Voltage	-0.3 to 16.5	V
VDD Current	20	mA
ISET, FB Voltage	-0.3 to 6	V
SW Voltage	-0.3 to 18	V
Continuous SW Current	Internally limited	A
Junction to Ambient Thermal Resistance (θ_{JA})	200	°C/W
Maximum Power Dissipation (derate 5mW/°C above T_A = 50°C)	0.5	W
Operating Junction Temperature	-40 to 150	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 14V, T_A = 25°C unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD Turn-On Voltage	V_{DDON}	Rising edge	11	11.7	12.4	V
VDD Turn-Off Voltage	V_{DDOFF}	Falling edge	9	9.6	10.2	V
VDD Clamp Voltage	$V_{DDCLAMP}$	10mA	15.7	16.4	17.1	V
Supply Current	I_{DD}			1	1.5	mA
Start Up Supply Current	I_{DDST}	V_{DD} = 10V, before turn-on		15	60	µA
Switching Frequency	f_{SW}	FB in regulation, V_{COMP} = 1.5V	58	62	66	kHz
Effective FB Feedback Voltage	V_{FB}		1.23	1.26	1.29	V
Maximum Duty Cycle	D_{MAX}	I_{SW} = 10mA	67	75	83	%
Minimum Duty Cycle	D_{MIN}	I_{SW} = 100mA		3.5		%
ISET Pin Voltage	V_{ISET}	R_{ISET} = 10kΩ		1.24		V
Switch Current Limit	I_{LIM}	R_{ISET} = 10kΩ	304	320	336	mA
Ratio of I_{LIM} to ISET Pin Current	β			2.6		A/mA
Switch On-Resistance	R_{ON}	I_{SW} = 50mA		3.6		Ω
SW Rise Time		1nF load, 15Ω pull-up		30		ns
SW Fall Time		1nF load, 15Ω pull-up		20		ns
SW Switch Off Current		Switch in off-state, V_{SW} = 18V		1	10	µA

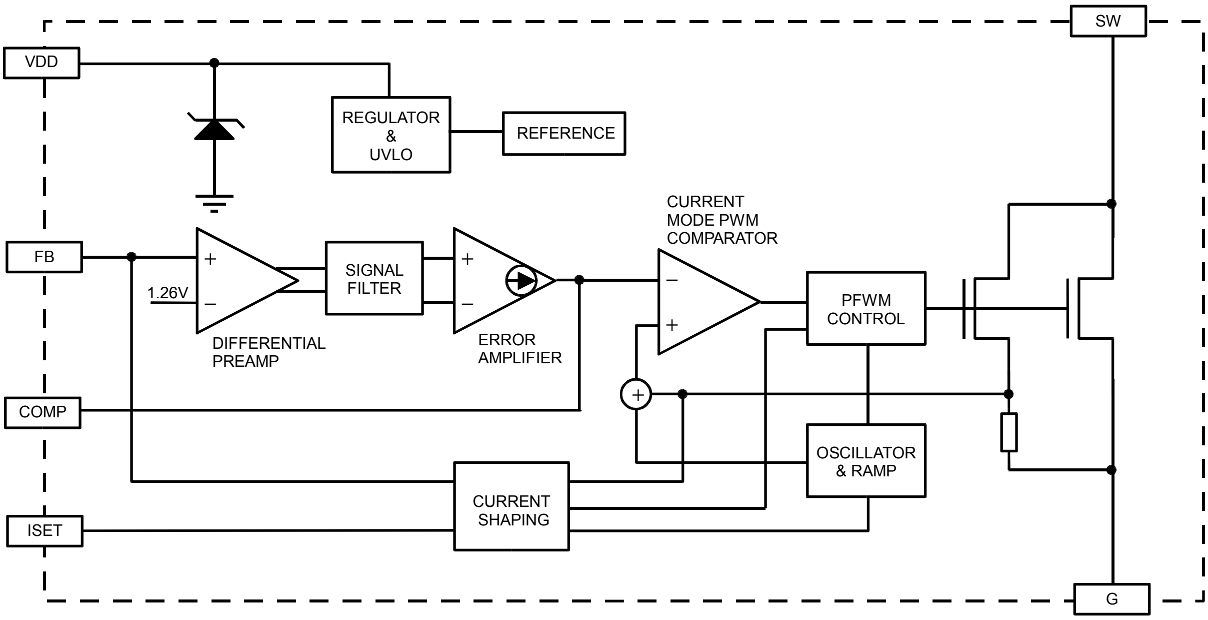


Figure 2. Functional Block Diagram

FUNCTIONAL DESCRIPTION

Figure 2 shows the *Functional Block Diagram* of the ACT34. Feedback regulation is done via several circuit blocks to pre-amplify the FB pin error voltage relative to an internal 1.26V reference, filter out the switching transients, and integrate the resulting useful differential error voltage for current mode PFWM (Pulse Frequency and Width Modulation) control. The external COMP pin allows optimal trade off between stability and transient response performance. The ISET pin externally programs the power switch peak current, and, together with the Current Shaping circuitry, produces a constant current (CC) profile when the secondary output reaches current limit.

SW is a driver output that drives the emitter of an external high voltage NPN transistor or N-channel MOSFET. This emitter-drive method takes advantage of the high V_{CBO} of the transistor, allowing a low cost transistor such as ‘13003 (V_{CBO} = 700V) or ‘13002 (V_{CBO} = 600V) to be used for a wide AC input range.

STARTUP MODE

VDD is the power supply terminal for the IC. When starting up, the IC stays in the startup mode with 15μA supply current. The bleed resistor from the rectified high voltage DC rail supplies current to VDD until it passes the 11.7V V_{DDON} threshold. At this point, the IC enters normal operation.

CONSTANT VOLTAGE (CV) MODE

In constant voltage operation, the IC captures the auxiliary fly-back signal at FB pin (through a resistor divider pair R3 and R4 as shown in Figure 3, *Connection Diagram*). The FB pin is pre-amplified against the reference voltage, and the secondary side output voltage error is extracted based on Active-Semi's patent-pending filter architecture. This error signal is then integrated by the Error Amplifier and output to the COMP pin.

The driver pulls SW low at the beginning of each switching cycle, causing the primary current to go through the high voltage transistor Q1 to the internal SW power switch. The current sense resistor current increases with time as the primary current increases. When the voltage across this current sense resistor plus the oscillator ramp signal equals COMP voltage, the driver turns off. As a result, the COMP voltage determines the switch current.

When the secondary output voltage is above regulation, the COMP voltage decreases to reduce the switch current. When the secondary side is below regulation, COMP increases to ramp up the switch current to bring the output back to regulation.

CONSTANT CURRENT (CC) MODE

When the secondary output current reaches a level set by the pin ISET, the IC enters current limit and causes the secondary output voltage to drop. As the output voltage decreases, so does the fly-back voltage in a proportional manner. The Current Shaping circuitry adjusts the switching frequency based on the fly-back voltage so that the secondary side output current stays constant.

LIGHT LOAD OPERATION

When the secondary side output load current reduces, the COMP voltage decreases. When COMP gets lower than 0.9V, the IC's switching frequency is also reduced to save power. This enables the application to meet all current green energy standards.

The switching frequency reduction is clamped at 10kHz. However, the actual minimum switching frequency is programmable with a small dummy load (while still meeting standby power).

SHORT CIRCUIT OPERATION

When the secondary side output is short circuited, the ACT34 enters hiccup mode operation. In this condition, the auxiliary supply voltage collapses and the VDD voltage drops below the V_{DDOFF} threshold. This turns off the IC and causes it to restart. This hiccup behavior continues until the short circuit is removed. In this behavior, the effective duty cycle is very low, resulting in very low short circuit current.

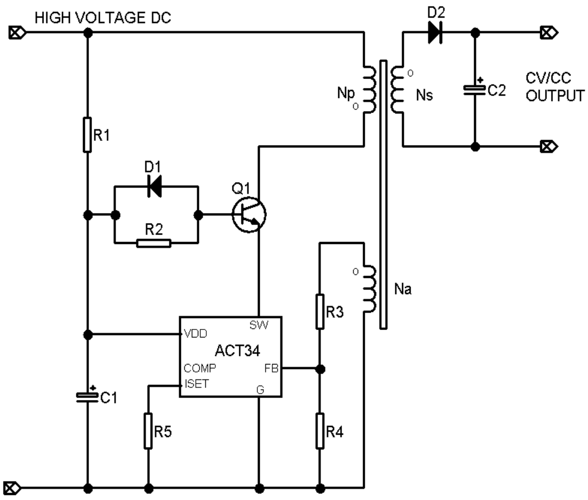


Figure 3. Connection Diagram

APPLICATION INFORMATION

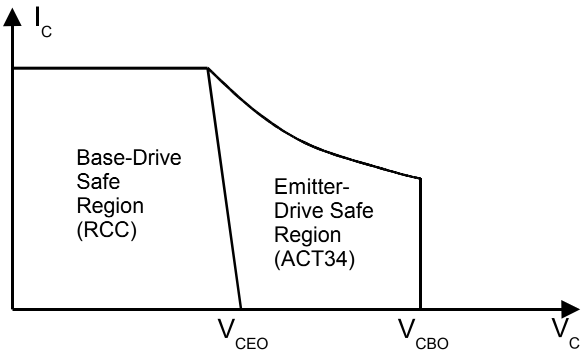


Figure 4. NPN Reverse Bias Safe Operation Area

CV MODE VOLTAGE SETTING

The output voltage can be set as the following equation 1(refer to Figure 3).

$$Vo = \frac{VFB*(R3+R4)}{R4}*(\frac{Ns}{Na}) ......(1)$$

1)If the output current foldback point should be as high as possible, you can set the output voltage by changing the ratio between secondary winding and auxiliary winding;

2)If output current foldback point is not critical, you can set the output voltage by changing the ratio R3 and R4, but keep R4 larger than 2K because R4 is not only for output voltage setting, but also for negative voltage clamping at pin FB.

CC MODE CURRENT SETTING

To set the CC mode output current, change the value of R5 (refer to Figure 3.) as equation 2.

$$Io = \frac{\frac{1}{2}*Lp*(\frac{VISET*\beta}{R5})^2*fsw}{Vo} ......(2)$$

1)R5 is the current setting resistor. If high accuracy of CC mode output current is required, use accurate resistor for R5;

2)β is the Ratio of I_{LIM} to ISET Pin Current;

3)Lp is the inductance of primary winding;

4)f_{SW} is the switching frequency of the converter when output voltage is in regulation.

EXTERNAL POWER TRANSISTOR

The ACT34 allows a low-cost high voltage power NPN transistor such as ‘13003 or ‘13002 to be used safely in flyback configuration. The required collector voltage rating for V_{AC} = 265V with full output load is at least 600V to 700V. As seen from Figure 4, *NPN Reverse Bias Safe Operation Area*, the breakdown voltage of an NPN is significantly improved when it is driven at its emitter. Thus, the ACT34+’13002 or ‘13003 combination meet the necessary breakdown safety requirement even though RCC circuits using ‘13002 or ‘13003 do not. Table 1 lists the breakdown voltage of some transistors appropriate for use with the ACT34.

Table 1. Recommended Power Transistors List

DEVICE	V_{CBO}	V_{CEO}	I_C	h_{FEMIN}	PACKAGE
MJE13002	600V	300V	1.5A	8	TO-126
MJE13003, KSE13003	700V	400V	1.5A	8	TO-126
STX13003	700V	400V	1A	8	TO-92

The power dissipated in the NPN transistor is equal to the collector current times the collector-emitter voltage. As a result, the transistor must always be in saturation when turned on to prevent excessive power dissipation. Select an NPN transistor with sufficiently high current gain (h_{FEMIN} > 8) and a base drive resistor (R2 in Figure 1) low enough to ensure that the transistor easily saturates.

TYPICAL PERFORMANCE CHARACTERISTICS

(Circuit of Figure 2, unless otherwise specified.)

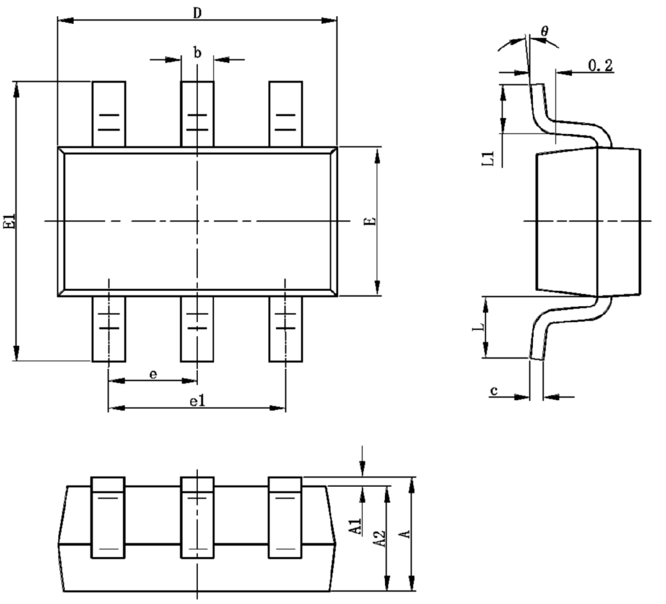
1270 Oakmead Parkway, Suite 310, Sunnyvale, California 94085-4044, USA

TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(Circuit of Figure 2, unless otherwise specified.)

PACKAGE OUTLINE

SOT23-6 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.700 REF		0.028 REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°