Tentative

Panasonic

AN49503A

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This document contains design target of AN49503A, which is under development. Changes may be made without prior notice, please consult our local sales representatives for latest information.

Features

- Maximum support 16 battery cells in series
- 10mV measurement accuracy with 14 bits voltage ADC for cell voltage, and 5 channels analog input measurement
- Built-in 16 bits low speed current measurement ADC (Coulomb Counter) and high speed current measurement ADC
- Low –side shunt sense resistor for current measurement and monitoring
- 2 interrupt pins ADIRQ1, ADIRQ2 for voltage measurement and current measurement
- Operation mode - Active, Standby and Shutdown Mode
- SPI serial communication interface up to 1MHz clock with CRC code correction and watchdog timer
- Built-in ALARM pins for overvoltage, undervoltage, overcurrent and short circuit detection and protection feature
- Built-in cell balancing MOSFET, with support of external cell balance MOSFET operation
- 6 channels General GPIO and 2 channels high voltage output
- High-side Charge (CHG) & Discharge (DIS) N-ch FET driver with built-in charge pump and FETOFF control pin
- 50mA 5V LDO
- Package : LQFP080-P-1414E

Description

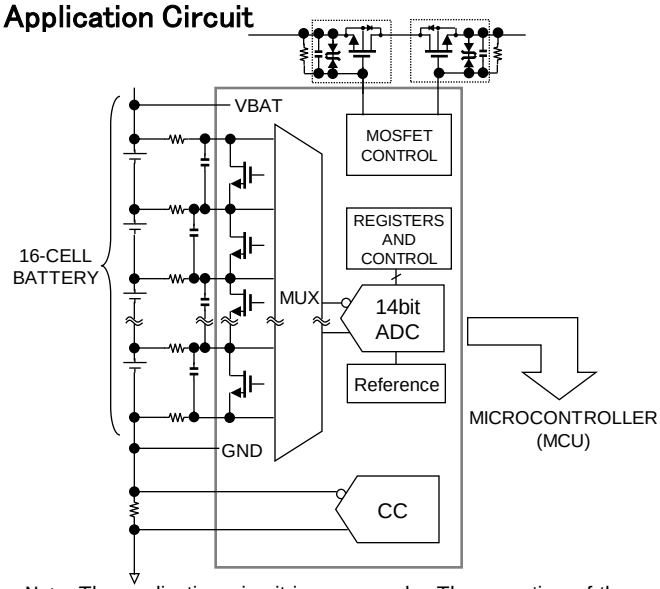
AN49503A is a battery management IC with battery measurement and protection function. With high resolution ADC built-in, AN49503A is capable to measure battery cell voltage and current level accurately. Through SPI serial interface, microcontroller unit (MCU) is able to read the status and measured result by AN49503A. The ALARM pins alert the MCU with the abnormal condition such as over voltage (OV), under voltage (UV), over current (OC) and short circuit (SC).

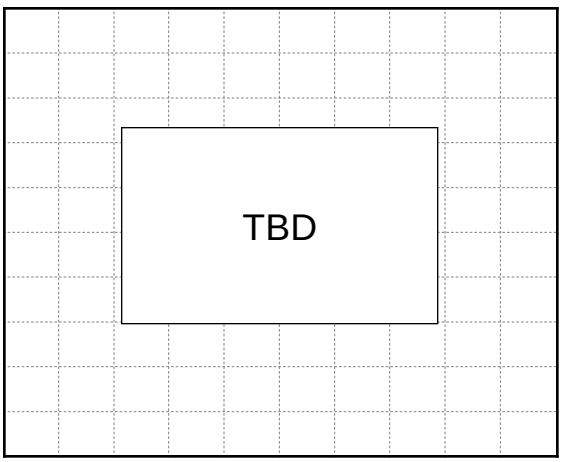
AN49503A can support an application with up to 16 batteries cells in series or a maximum voltage of 85V, it is suitable for application with high input voltage such as E-bike, UPS etc.

Application

- Pedelec, e-Bike, UPS, Server Backup System, Power Tool etc

Application Circuit





Note: The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. Customer is fully responsible for the incorporation of the above illustrated application circuit in the production.

Table of Contents

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Notes
Supply voltage	V_{VBAT}	99	V	*1
	V_{CVDD}	6.5	V	*1
Operating junction temperature	T_j	125	°C	*2
Storage temperature	T_{stg}	-55 ~ 125	°C	*2
Input Voltage Range	C16	-0.3 ~ VBAT+1.2	V	*3
	Cn (n=1~15)	-0.3 ~ VBAT+0.3	V	*3
	C0	-0.3~6.5	V	
	SEN, SCL, SDI GPIOn (n=1~6)	-0.3 ~ V_{CVDD}+0.3	V	*4
	TMONIn (n=1~5),	-0.3 ~ V_{VDD50}+0.3	V	*4
	SRP, SRN	-0.5 ~ 2.0	V	
Output Voltage Range	ALARM1, SDO	-0.3 ~ V_{CVDD}+0.3	V	
	SDO, VDD50	-0.3 ~ 6.5	V	
	GPOHn (n=1~2)	-0.3 ~ 99	V	
Allowable Voltage Between Pins	Cn to Cn-1,	-0.3 ~ 11	V	—

Notes) This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range.

When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

Do not apply external currents and voltages to any pin not specifically mentioned.

*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25 °C

*3 : (VBAT+0.3) & (VBAT+1.2) shall not over 99V..

*4: (V_{CVDD} + 0.3), (V_{VDD50} + 0.3) must not exceed 6.5 V.

POWER DISSIPATION RATING

Package	θj-a	θj-c	P_D(Ta=25℃)	P_D(Ta=105℃)
LQFP080-P-1414E	55.5 °C/W	7.2 °C/W	1.80 W	0.36 W

Notes) For the actual usage, please refer to the PD-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Min.	Typ.	Max.	Unit	Notes
Supply voltage range	V_{VBAT}	12.5	59.2	85	V	—
	V_{CVDD}	3.0	5.0	5.5	V	—
Input Voltage Range	Cn-1 – Cn	0	3.7	5.0	V	—
	SEN, SCL, SDI	0		V_{CVDD}	V	—
	TMONIn (n=1～5)	0		5.0	V	—
	GPIOn (n=1～6)	0		V_{CVDD}	V	—
	SRP, SRN	-0.18		0.18	V	—
Output Voltage Range	ALARM1	0		V_{CVDD}	V	—
	SDO	0		V_{CVDD}	V	—
	GPOHn (n=1～2)	0		V_{VBAT}	V	—
Pin External Components	C_{VBAT}	TBD (100nF)			µF	—
	C_{VDD}	10			µF	—
	C_{AVDD}, C_{DVDD}	2.2			µF	—
	C_{VC}		2.2		µF	—
	R_{VC}		4.7		kΩ	—
Operating Ambient Temperature	Ta^{opr}	–40		105	℃	—

ELECTRICAL CHARACTERISTICS

Test condition under recommended voltage supply range and operating ambient temperature unless otherwise noted.

Note: Limit values for items below is target design value, it may be different from final value after MP. Please consult our representative for latest update.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SUPPLY CURRENT							
VBAT Active Mode	I_{BAT1}			2.5	TBD	mA	
VBAT Standby Mode	I_{BAT3}	5VLDO:Low Power, Coulomb Counter:off Communication:off		0.15	TBD	mA	
VBAT Shutdown Mode	I_{BAT4}	@25℃		TBD	1	μA	
5VLDO							
VDD50 Output Voltage	V_{VDD}		4.75	5.0	5.25	V	
VDD50 Drive Current	I_{VDD1}	Active			50	mA	
VDD50 Drive Current	I_{VDD2}	Standby			5	mA	
CELL BALANCING CONTROL OUTPUT (CBn)							
Output Impedance	Z_{CB}	⊿Cn = 3.0V ～ 5.0V			20	Ω	

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Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
CELL VOLTAGE MONITOR							
Input Voltage Range	ΔCn	Cn-1 – Cn	0		5	V	
Voltage Resolution	V_{RES}	14bits		0.3		mV	
Voltage Accuracy	V_{ACC_VC}	ΔCn = 2.0V ～ 4.3 V Ta = –30℃ ～ 65℃	–10		10	mV	
Conversion Time	t_{conv}	time/cell		50		μs	
Effective Input Current	I_{IN}	Active			5	μA	
Input Leakage Current	I_{LK}	Shutdown			1	μA	
OVER / UNDER VOLTAGE DETECTOR (OV / UV)							
OV detection threshold step	V_{ACC_OV}	T_a=25℃, 2.0～4.5V@6bit		50		mV	
UV detection threshold step	V_{ACC_UV}	T_a=25℃, 0.5～3.0V@6bit		50		mV	*1
VPACK CELL VOLTAGE MONITOR							
Input Voltage Range	V_{IN}		0		85	V	
Voltage Resolution	V_{RES}	14bits		6.1		mV	
Voltage Accuracy	V_{ACC_VPACK}	V_{VPACK} = 12.5V ～ 72V Ta = –30℃ ～ 65℃	–1	0	1	V	
TMONI1-5 VOLTAGE MONITOR							
Input Voltage Range	V_{IN}		0		5	V	
Voltage Resolution	V_{RES}	14bits		0.3		mV	
Voltage Accuracy	V_{ACC_VC}	VIN = TBD Ta = –20℃ ～ TBD℃	–10	0	10	mV	
Effective Input Current	I_{IN}	Active			5	μA	
Input Pull-up Resistance	R_{PU}		TBD	10	TBD	kΩ	
THERMAL SHUTDOWN							
Shutdown Threshold	T_{SD2}	Tj		175		°C	*2

*1: Design reference value.

*2: Typical design value. When thermal shutdown occurs, all circuitry is shutdown. Following wake up (to active mode) sequence in order to restart.

ELECTRICAL CHARACTERISTICS

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Note: Limit values for items below is target design value, it may be different from final value after MP. Please consult our representative for latest update.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
LOW SPEED CURRENT MONITOR(SRP,SRN)							
Input Voltage Range	V_{IN}		-180		180	mV	
Voltage Resolution	V_{RES}			5.493		μV	
Voltage Accuracy1	V_{ACC_IMONI}	VIN = 100mV			1000	μV	
Voltage Accuracy2	V_{ACC_IMONI}	VIN = 10mV			150	μV	
Voltage Accuracy3	V_{ACC_IMONI}	VIN = 1mV			25	μV	
HIGH SPEED CURRENT MONITOR(SRP,SRN)							
Input Voltage Range	V_{IN}		-180		180	mV	
Voltage Resolution	V_{RES}			10.99		μV	
Voltage Accuracy1	V_{ACC_IMONI}	VIN = 100mV			1000	μV	
Voltage Accuracy2	V_{ACC_IMONI}	VIN = 10mV			150	μV	
Voltage Accuracy3	V_{ACC_IMONI}	VIN = 1mV			50	μV	
CURRENT PROTECTION(SRP,SRN)							
Over Current in Charge Detection Threshold step	V_{CP_OCC}	10～200mV@5bits		10		mV	
Over Current in Discharge Detection Threshold step	V_{CP_OCD}	25～800mV@5bits		25		mV	
Short Circuit in Discharge Detection Threshold step	V_{CP_SCD}	50～500mV@4bits		50		mV	
GENERAL PURPOSE INPUT/OUTPUT (GPIO)							
Input Voltage High	V_{IH}		V_{CVDD} ×0.8			V	
Input Voltage Low	V_{IL}				V_{CVDD} ×0.2	V	
Output Voltage High	V_{OH}	I_{OH} = –1mA	V_{CVDD} –0.6		V_{CVDD} +0.3	V	
Output Voltage Low	V_{OL}	I_{OL} = +1mA	–0.3		0.4	V	
GENERAL PURPOSE HV OUTPUT (GPO)							
Output Voltage Low	V_{OL}	I_{OL} = +1mA	–0.3		7.0	V	

ELECTRICAL CHARACTERISTICS

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Note: Limit values for items below is target design value, it may be different from final value after MP. Please consult our representative for latest update.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
DIGITAL INPUT(1) VPC							
Input Voltage High	V_{IH}		4.0	—	—	V	—
Input Voltage Low	V_{IL}		—	—	0.3	V	—
Pull-down resistance	R_{IL}		2.5	7	20	MΩ	—
DIGITAL INPUT(3) SHDN							
Input Voltage High	V_{IH}		3.0	—	—	V	—
Input Voltage Low	V_{IL}		—	—	0.1	V	—
Pull-down resistance	R_{IL}		TBD	820	TBD	kΩ	—
DIGITAL INPUT(4) SDI,SCL,SEN, FETOFF							
Input Voltage High	V_{IH}		V_{CVDD} × 0.8			V	
Input Voltage Low	V_{IL}				V_{CVDD} × 0.2	V	
Input Leakage Current	I_{LK}		-1	0	1	uA	
DIGITAL INPUT(5) STB							
Input Voltage High	V_{IH}		V_{CVDD} × 0.8			V	
Input Voltage Low	V_{IL}				V_{CVDD} × 0.2	V	
DIGITAL OUTPUT(1) ALARM1,SDO							
Output Voltage High	V_{OH}	I_{OH} = –1mA	V_{CVDD} –0.6		V_{CVDD} +0.3	V	
Output Voltage Low	V_{OL}	I_{OL} = +1mA	–0.3		0.4	V	
DIGITAL OUTPUT(2) NRST							
Output voltage low	V_{OL}	I_{OL} = 0 mA	0	—	0.5	V	
Pull-up resistance	R_{IL}	—	50	100	200	kΩ	

ELECTRICAL CHARACTERISTICS

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Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
CVDD POR (POWER ON-RESET)							
Positive-going input voltage	V_{IH_POR}	—	2.65	2.80	2.95	V	
Negative-going input voltage	V_{IL_POR}	—	2.2	2.45	—	V	
VDD50 UVLO							
UVLO wake up voltage	V_{IH_UVLO}			4.2		V	
UVLO shutdown voltage	V_{IL_UVLO}			4.0		V	
Hysteresis voltage	V_{HYS_UVLO}			0.2		V	
N-ch FET DRIVER (CHG & DIS FET)							
Drive voltage (DIS_N="H")	V_{ON_DIS}	$V_{ON\_DIS} = V_{DIS\_N} - V_{PACK}$ VGS connect 10MΩ	TBD	11	13	V	
Drive voltage (CHG_N="H")	V_{ON_CHG}	$V_{ON\_CHG} = V_{CHG\_N} - V_{BAT}$ VGS connect 10MΩ	TBD	11	13	V	
Drive voltage (DIS_N="L")	V_{OFF_DIS}	$V_{OFF\_DIS} = V_{DIS\_N} - V_{PACK}$ VGS connect 10MΩ	—	—	0.2	V	
Drive voltage (CHG_N="L")	V_{OFF_CHG}	$V_{OFF\_CHG} = V_{CHG\_N} - V_{BAT}$ VGS connect 10MΩ	—	—	0.2	V	
Rise time (DIS_N="L" to "H")	tr	V_{DIS} = 10% to 90% C_L = 39nF	—	1	2	ms	
Rise time (CHG_N="L" to "H")	tr	V_{CHG} = 10% to 90% C_L = 39nF	—	1	2	ms	
Fall time (DIS_N ="H" to "L")	tf	V_{DIS} = 90% to 10% C_L = 39nF	—	1	2	ms	
Fall time (CHG_N="H" to "L")	tf	V_{CHG} = 90% to 10% C_L = 39nF	—	1	2	ms	

ELECTRICAL CHARACTERISTICS

Test condition under recommended voltage supply range and operating ambient temperature unless otherwise noted.

Note: Limit values for items below is target design value, it may be different from final value after MP. Please consult our representative for latest update.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min.	Typ.	Max.		
SPI Interface Timing (SEN, SDI, SCL, SDO)							
SCL Frequency	f_{SCK}	—	—	—	1	MHz	
SCL Duty Cycle	t_{DUTY}	—	45	50	55	%	
SEN Rising to SCL Rising	t_{SEN_LD}	—	100	—	—	ns	
SCL Falling to SEN Falling	t_{SEN_LG}	—	100	—	—	ns	
SEN "Low" Width	t_{SEN_LO}	—	500	—	—	ns	
SDI Setup Time	t_{SDI_SU}	SDI valid to SCL falling	100	—	—	ns	
SDI Hold Time	t_{SDI_HD}	SCL falling to SDI valid	100	—	—	ns	
SDO Valid Time	t_{SDO_VD}	SCL rising to SDO valid $C_L \leqq 50$ pF	—	—	400	ns	
SDO Disable Time	t_{SDO_DIS}	SEN falling to SDO disable	—	—	400	ns	

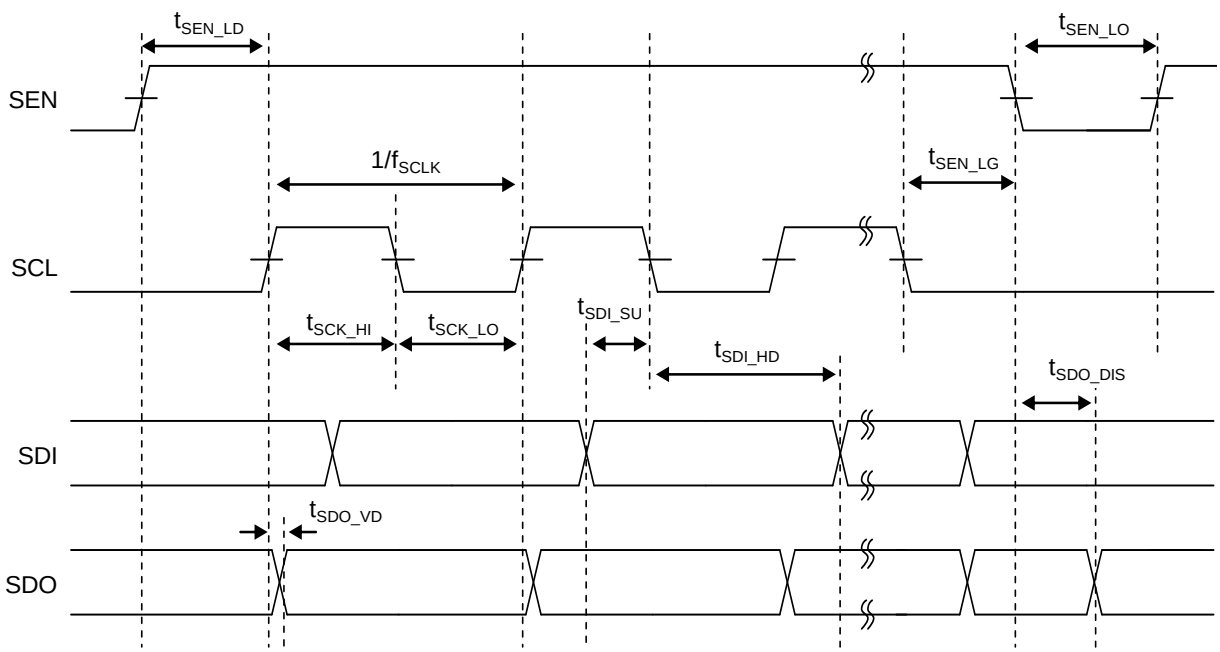
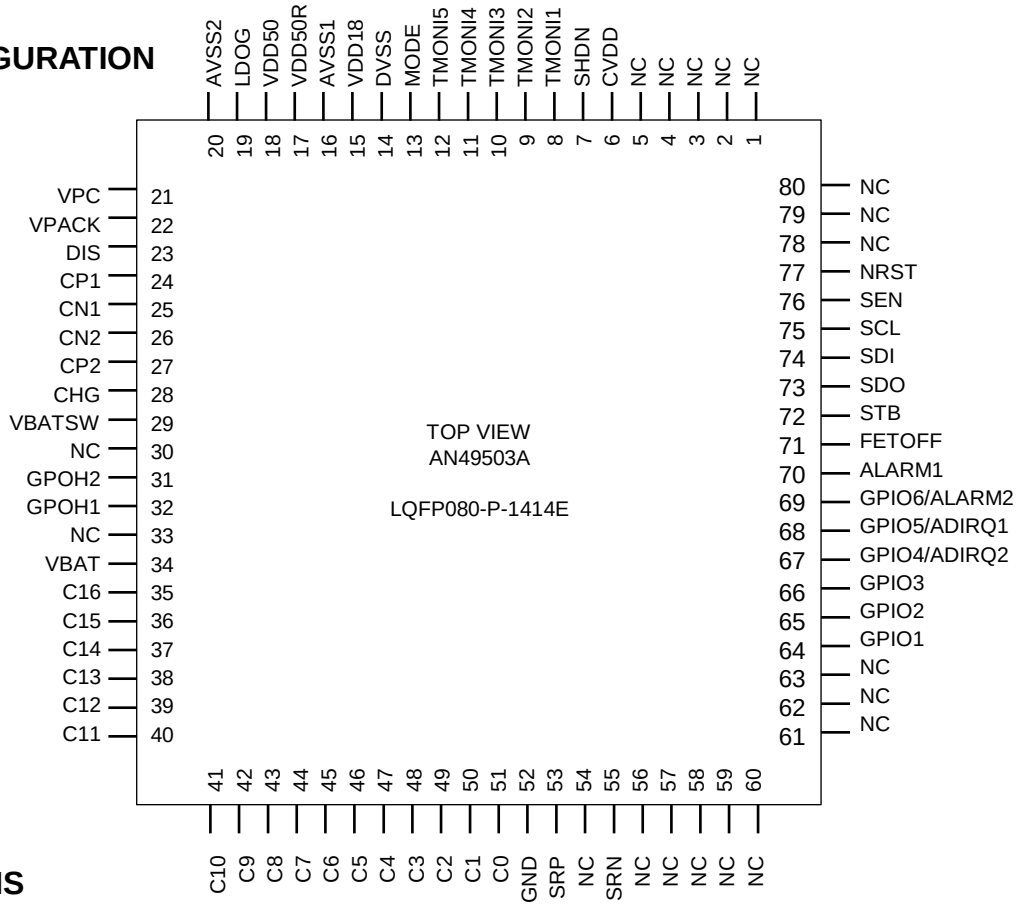


Figure :SPI Timing

PIN CONFIGURATION



PIN FUNCTIONS

Pin No.	Pin name	Type	Description
1	NC	–	N.C. Pin
2	NC	–	N.C. Pin
3	NC	–	N.C. Pin
4	NC	–	N.C. Pin
5	NC	–	N.C. Pin
6	CVDD	I(Supply)	Digital Voltage Supply
7	SHDN	I	Shutdown Control “L”: Active / “H”: Shutdown
8	TMONI1	I	Analog Input Pin 1
9	TMONI2	I	Analog Input Pin 2
10	TMONI3	I	Analog Input Pin 3
11	TMONI4	I	Analog Input Pin 4
12	TMONI5	I	Analog Input Pin 5
13	MODE	I	Test Mode pin for Manufacturer Use Only (Connect to DVSS always)
14	DVSS	GND	Digital Ground

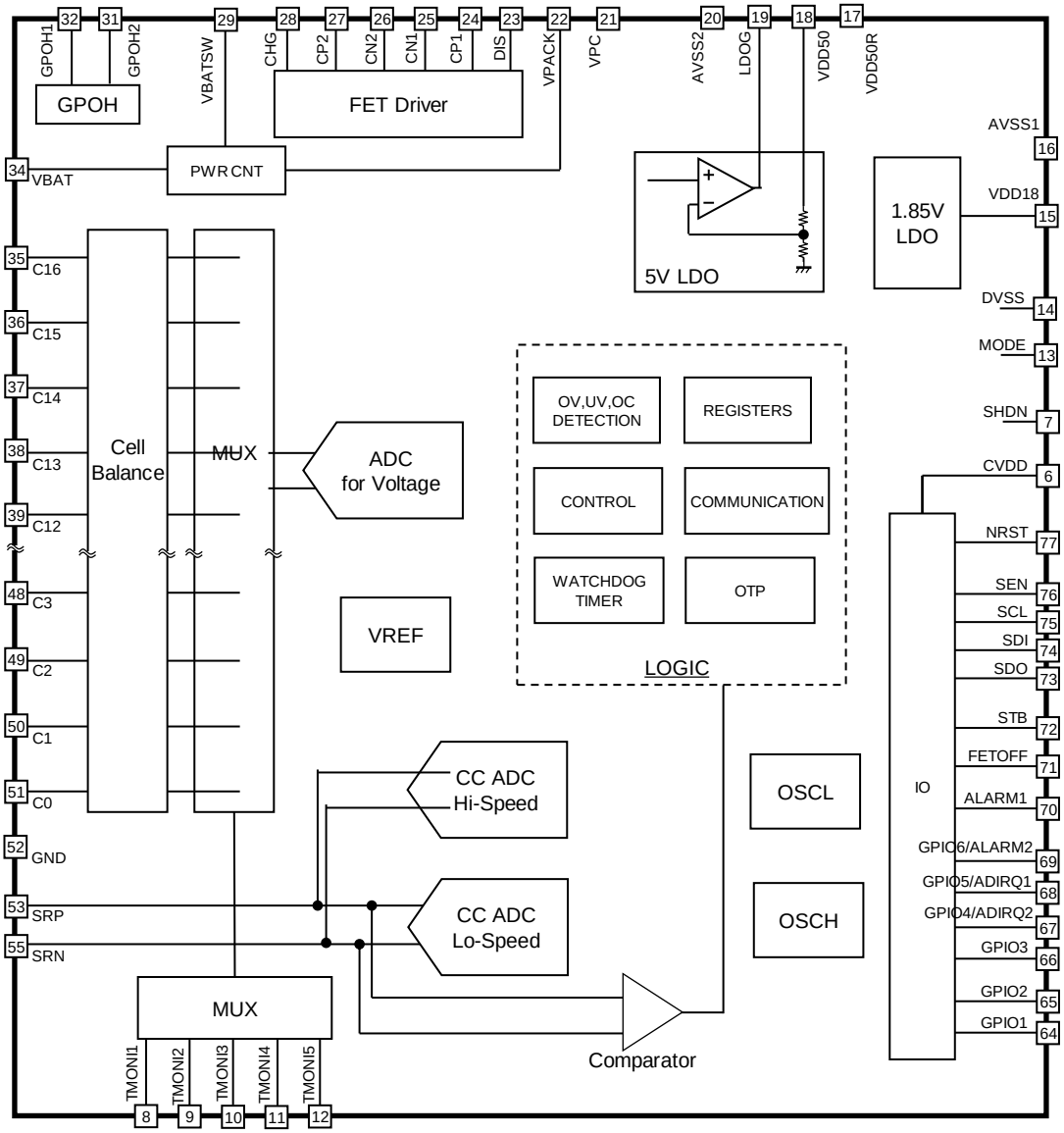
PIN FUNCTIONS

Pin No.	Pin name	Type	Description
15	VDD18	O	1.85V LDO Output Pin for Internal Use
16	AVSS1	GND	Analog Ground
17	VDD50R	I	5V LDO Feedback Pin 1 (To be connected to VDD50 pin)
18	VDD50	I	5V LDO Feedback Pin
19	LDOG	O	Gate Control Pin for 5V LDO NMOS Gate Terminal
20	AVSS2	GND	Analog Ground
21	VPC	I	Wake Up Signal Pin – "L" Active / "H" Wake Up
22	VPACK	I(Power Supply)	Positive Terminal for Battery Pack
23	DIS	O	Discharge NMOSFET Gate Drive Pin
24	CP1	O	Charge Pump Capacitor Pin (Positive Terminal for VPACK)
25	CN1	O	Charge Pump Capacitor Pin (Negative Terminal for VPACK)
26	CN2	O	Charge Pump Capacitor Pin (Negative Terminal for VBAT)
27	CP2	O	Charge Pump Capacitor Pin (Positive Terminal for VBAT)
28	CHG	O	Charge NMOSFET Gate Drive Pin
29	VBATSW	O	Power Pin for 5V LDO NMOS Drain Terminal
30	NC	–	N.C. Pin
31	GPOH2	O	High Voltage General Purpose Output Pin 2 (Open Drain)
32	GPOH1	O	High Voltage General Purpose Output Pin 1 (Open Drain)
33	NC	–	N.C. Pin
34	VBAT	I(Power Supply)	Battery Top Most Pin
35	C16	I	Cell 16 Input Pin (+ve)
36	C15	I	Cell 15 Input Pin (+ve) / Cell 16 Input Pin (–ve)
37	C14	I	Cell 14 Input Pin (+ve) / Cell 15 Input Pin (–ve)
38	C13	I	Cell 13 Input Pin (+ve) / Cell 14 Input Pin (–ve)
39	C12	I	Cell 12 Input Pin (+ve) / Cell 13 Input Pin (–ve)
40	C11	I	Cell 11 Input Pin (+ve) / Cell 12 Input Pin (–ve)
41	C10	I	Cell 10 Input Pin (+ve) / Cell 11 Input Pin (–ve)
42	C9	I	Cell 9 Input Pin (+ve) / Cell 10 Input Pin (–ve)
43	C8	I	Cell 8 Input Pin (+ve) / Cell 9 Input Pin (–ve)
44	C7	I	Cell 7 Input Pin (+ve) / Cell 8 Input Pin (–ve)
45	C6	I	Cell 6 Input Pin (+ve) / Cell 7 Input Pin (–ve)
46	C5	I	Cell 5 Input Pin (+ve) / Cell 6 Input Pin (–ve)

PIN FUNCTIONS

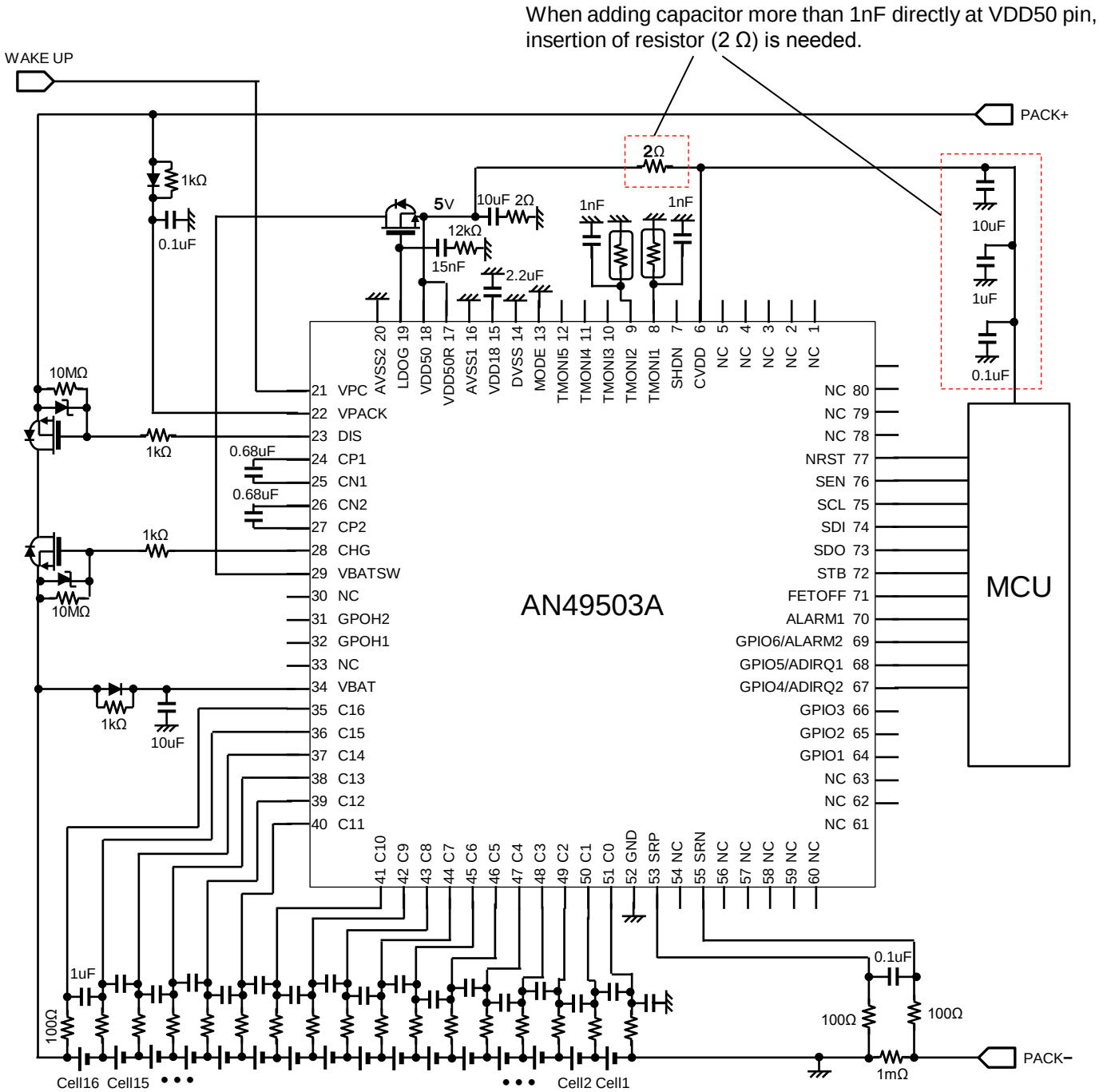
Pin No.	Pin name	Type	Description
47	C4	I	Cell 4 Input Pin (+ve) / Cell 5 Input Pin (−ve)
48	C3	I	Cell 3 Input Pin (+ve) / Cell 4 Input Pin (−ve)
49	C2	I	Cell 2 Input Pin (+ve) / Cell 3 Input Pin (−ve)
50	C1	I	Cell 1 Input Pin (+ve) / Cell 2 Input Pin (−ve)
51	C0	I	Cell 1 Input Pin (−ve)
52	GND	GND	Analog Ground
53	SRP	I	Shunt Resistor Positive Pin
54	NC	−	N.C. Pin
55	SRN	I	Shunt Resistor Negative Pin
56	NC	−	N.C. Pin
57	NC	−	N.C. Pin
58	NC	−	N.C. Pin
59	NC	−	N.C. Pin
60	NC	−	N.C. Pin
61	NC	−	N.C. Pin
62	NC	−	N.C. Pin
63	NC	−	N.C. Pin
64	GPIO1	I/O	General Purpose I/O Pin 1
65	GPIO2	I/O	General Purpose I/O Pin 2
66	GPIO3	I/O	General Purpose I/O Pin 3
67	GPIO4/ADIRQ2	I/O	General Purpose I/O Pin 4 / ADIRQ2 Pin
68	GPIO5/ADIRQ1	I/O	General Purpose I/O Pin 5 / ADIRQ1 Pin
69	GPIO6/ALARM2	I/O	General Purpose I/O Pin 6 / ALARM2 Pin
70	ALARM1	O	ALARM1 Pin
71	FETOFF	I	CHG/DIS FET Control Pin − “L” Normal / “H” FET Forced OFF
72	STB	I	Standby Mode Control Pin − “L” Active Mode / “H” Standby Mode
73	SDO	O	SPI Interface Pin − Data Out (Open Drain)
74	SDI	I	SPI Interface Pin − Data In
75	SCL	I	SPI Interface Pin − Clock
76	SEN	I	SPI Interface Pin − Enable
77	NRST	O	Power Reset Output Pin (Open Drain)
78	NC	−	N.C. Pin
79	NC	−	N.C. Pin
80	NC	−	N.C. Pin

FUNCTIONAL BLOCK DIAGRAM



Application Circuit Example

When connecting a circuit to VDD50, please be careful about below.
・Adding capacitor more than 1nF to VDD50 pin directly is prohibited.
・When needing capacitor more than 1nF, please use through 2Ω resistor.
Please design as the total capacitor is from 6uF to 16uF.



Note: The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. Customer is fully responsible for the incorporation of the above illustrated application circuit in the production.

Functional Description

1. Battery Connection

The minimum required VBAT voltage is 12.5V to guarantee normal operation.

For application using less than 16 cells, all unused cells Cn pins should be connected as shown in figure below, user shall connect cells C16, C15, C1 and C2 first and follow by connecting battery from lower cell.

Figures below show example connection for 15 battery cells and 4 battery cells, please note, it is possible co be connected for 4 battery cells only when the minimum VBAT is higher then 12.5V.

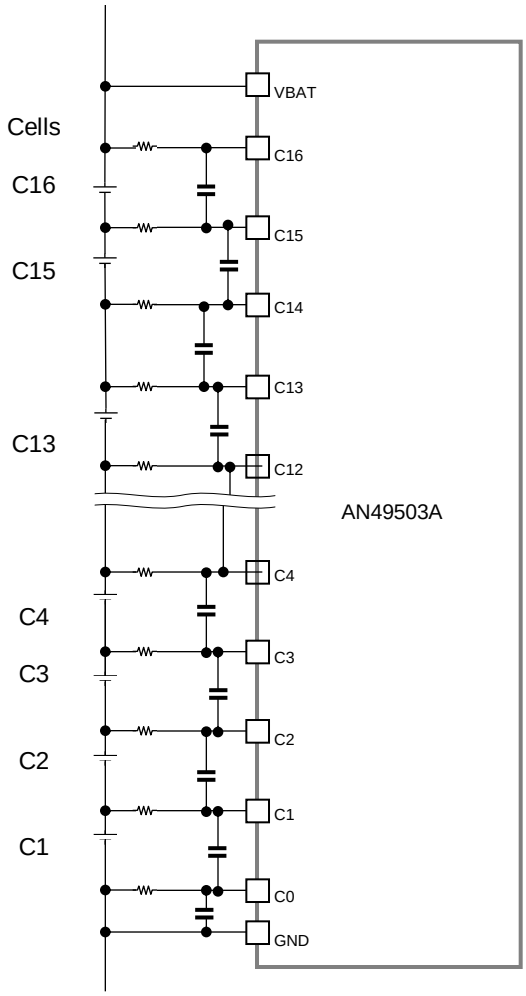


Fig. AN49503A Cell Connection example with 15 cell connected

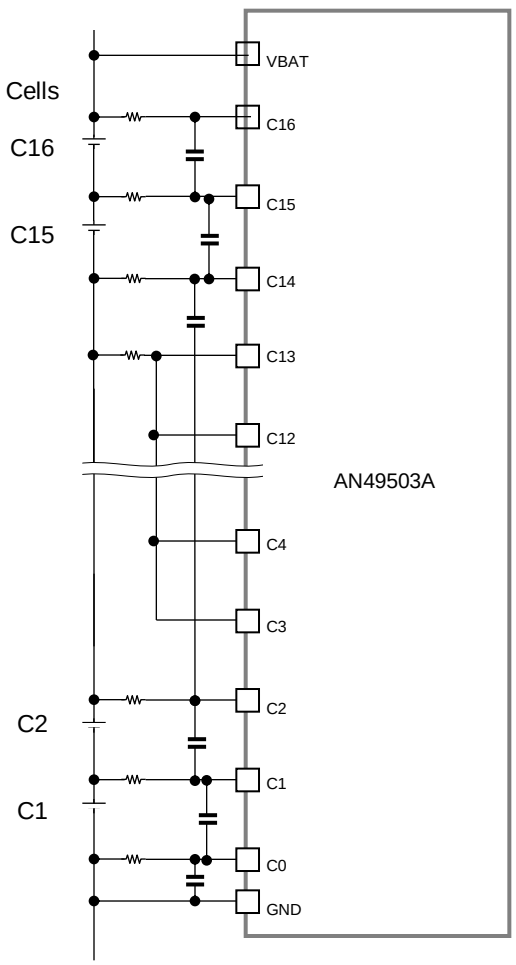


Fig. AN49503A Cell Connection Example with only 4 cell connected

Functional Description

2. Operation Mode Explanation

2.1 Active Mode

At Active Mode, all circuitry is in full operation condition. Voltage measurement, overvoltage and undervoltage detection will only be performed under Active Mode.

When wake up from shut down mode, with **VPC** pin at HI condition and **VPACK** or VBAT pins voltage higher than 12.5V, AN49503A will enter Active Mode. After wake up, **SDO** pin will change from LO to HI indicating the SPI communication is ready.

2.2 Standby Mode

From Active Mode, IC enter Standby Mode by setting STB pin to HI. At Standby Mode, to reduce power consumption, voltage measurement, overvoltage and undervoltage detection is hence disabled LDO can be set to operate at low power mode by register *LP50EN*.

Low speed Current measurement, SPI communication and cell balance can be enabled in this mode. With register *COM_STP* set to 1, SPI communication is turned OFF for further power reduction, this register will be auto reset to 0. To resume SPI communication, input HI to **SEN** pin for longer than 1ms.

When **STB** pin is set to LO, the system will resume to Active Mode.

When AN49503A enters Standby Mode with OV/UV detection enabled and register *STB_MONEN* and ADC_CONT set to 1, a timing counter will be started, if no SPI communication is done within 1s, it will automatically switch back to Active Mode for OV/UV detection and it will switch back to Standby Mode automatically when this operation is done.

2.3 Shutdown Mode

All circuit stopped functioning, the current consumption is minimized at Shutdown Mode. The IC can be shutdown by setting **SHDN** pin to HI or by setting register MSET_*SHDN* to 1 from any mode with **VPC** pin at LO condition.

Refer to table next page for the available features at different modes.

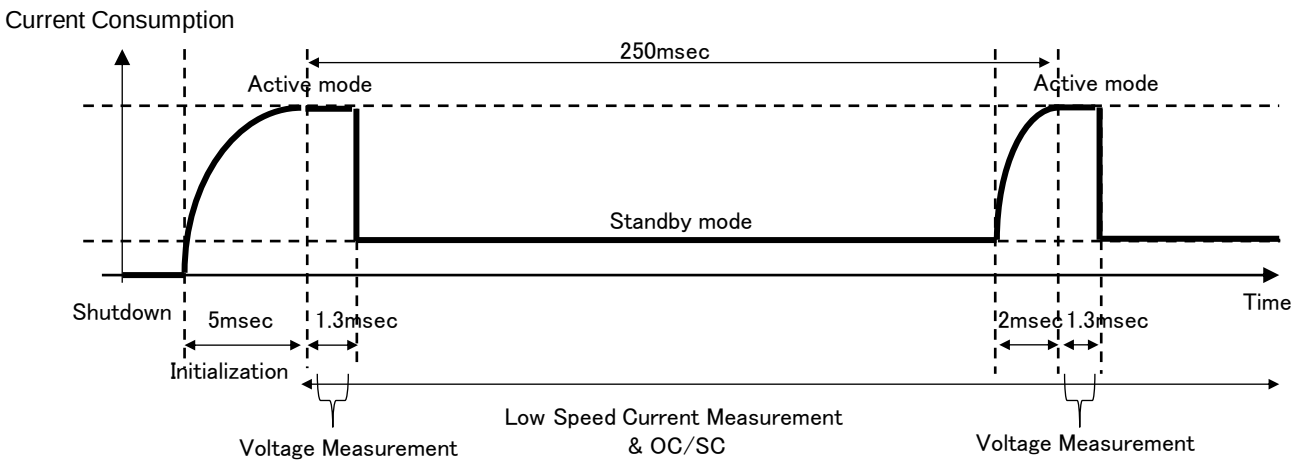


Fig. Example of operation on intermittent operation (Active Mode -> Standby Mode and repeating)

- For AN49503A, it is possible to reduce the current consumption by operating the IC in intermittent operation, MCU control the IC to operate switching form Active Mode to Standby Mode and repeating.
- It required minimum of 5ms for initialization wake up from Shutdown Mode before IC start voltage measurement.
- It required minimum of 2ms for initialization when return to Active Mode from Standby mode before start voltage measurement.

Functional Description

2.4 State Diagram

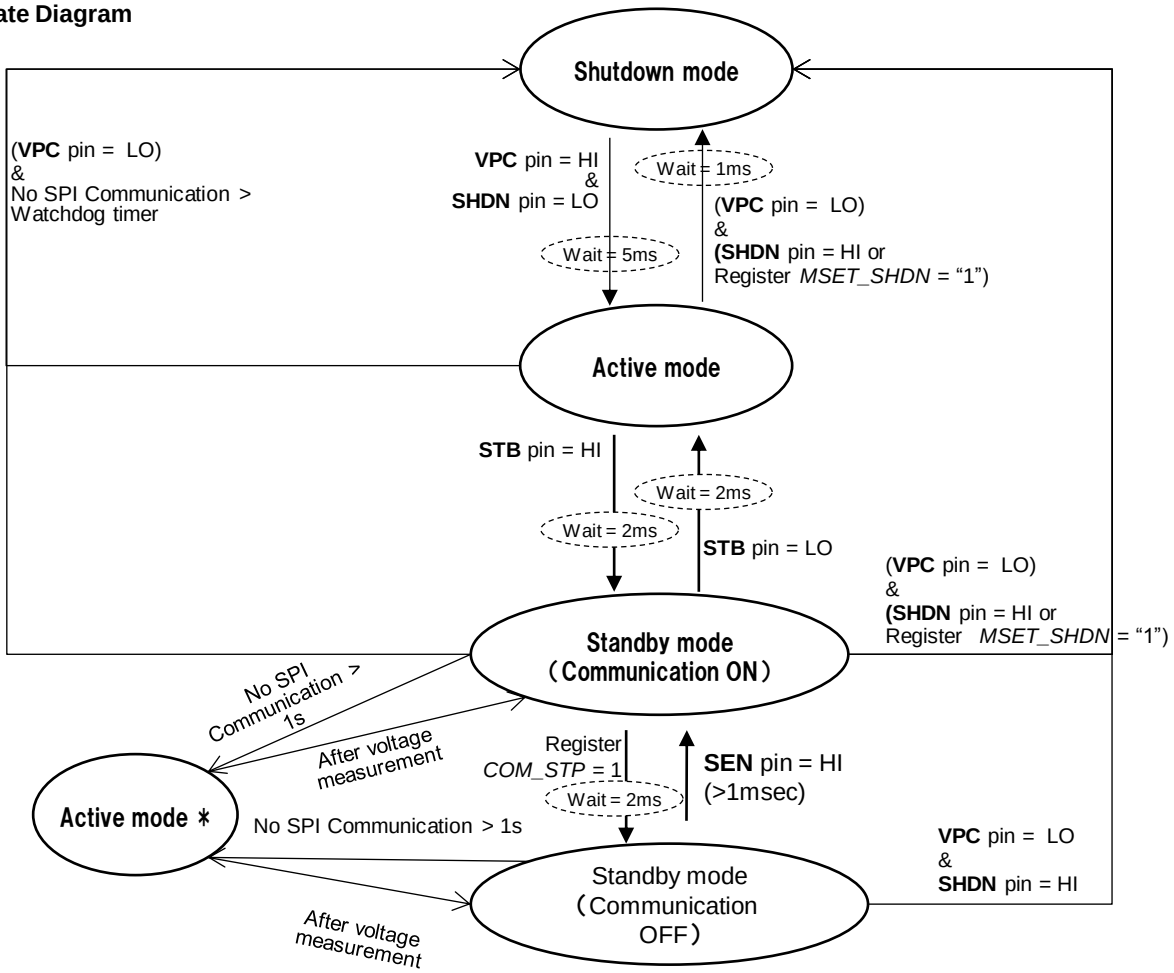


Table. Operation Mode Summary

Mode	5VLDO drivability	Cell Voltage Measurement	Coulomb Counter (CC)	DIS, CHG FET ON/OFF	Cell Balance	SPI I/F	ALARM
Active	50mA	ON	ON/OFF	ON/OFF	ON/OFF*2	ON	ON/OFF (OV/UV/ OC/SC)
Standby	5mA/ 50mA	OFF	ON/OFF	ON/OFF *1	ON/OFF	ON/OFF	ON/OFF (OC/SC)
Shutdown	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Note: The LDO drivability, coulomb counter (CC), FET control, cell balance control can be set by respective register.

*1 DIS and CHG FET setting is kept when operation mode change from Active Mode to Standby Mode, FET control is available in Standby Mode (Communication ON) except when register FDRV_STBY = 1. During Standby Mode (Communication OFF), it can only be turned OFF by FETOFF pin.
*2 Cell balance can be turned ON during Active Mode, however it could cause wrong abnormal detection, user shall not enable UV/OV detection at the same time.

Functional Description

3. 5V LDO

AN49503A has built-in with a 5V LDO controller, with a external NMOS, it generate a 5V regulated output which can drive up to 50mA load current.

At Active Mode, the LDO operate at Normal Mode which can drive load up to 50mA while at Standby Mode, it could be set to operate at Low Power Mode which drive up to 5mA with register *LP50EN* set to 1. The register can be set to 1 at Active Mode, however, it only take effect when it enters Standby Mode.

Address：0x18

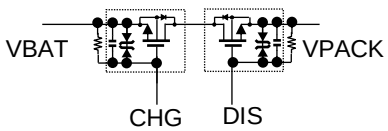
bit	Register	Description
4	LP50EN	VDD50 LDO Power Mode 1： Low power mode 0： Normal mode（Default）

4. CHG / DIS FET Control

AN49503A has built-in charge pump circuit to drive high side NMOS FET switches. The two NMOS FETs are controlled by connecting CHG and DIS pins to gate terminal of the NMOS FETs as shown, this control can be done in both Active and Standby Mode.

The turning ON of NMOS FETs are controlled by setting registers *FDRV_CHG_FET* and *FDRV_DIS_FET* to 1 respectively. When it is turned ON, the VGS voltage is 11V typically. The VGS voltage can be set by register FDRV_LEVEL.

While the NMOS FETs can be turned OFF by setting the registers to 0, it can also be turned OFF through setting FETOFF pin to HI. Under ALARM condition, the NMOS FETs could be set to be response to the ALARM condition, refer Section 10 for details.



During Standby Mode, with register FDRV_STBY set to 1, internal circuit of the FET driver will operate intermittently for further power reduction while no change in FET ON/OFF state. When user wants to change FET state, user shall first change register FDRV_STB to 0 before changing FDRV_CHG_FET and FDRV_DIS_FET setting.

Address：0x01

bit	Register	Description
1	FDRV_CHG_FET	CHG FET ON/OFF 1:FET ON 0:FET OFF (Default)
0	FDRV_DIS_FET	DIS FET ON/OFF 1:FET ON 0:FET OFF (Default)

Address：0x03

bit	Register	Description
8	FDRV_ STBY	FET Driver Operation 1： Intermittent 0： Continuous（Default）
[4:2]	FDRV_LEV EL	FET Gate-Source Voltage 11V(Typ)－(setting)×1V Setting range：0 (Default)～7

5. General Purpose High Voltage Output (GPOH1/2)

There are two high voltage open drain GPOH pins (GPOH1/GPOH2) for AN49503A. The two pins can sustain voltage up to VBAT level. These pins could be use to drive high side PMOS FET. When used, pull up resistors of more than 100kΩ are needed.

These pins could be set to response to ALARM condition. Refer to Section 10 for details.

Table below shows the register setting for GPOH1 and GPOH2 pins.

Address：0x1B

bit	Register	Description
5	GPOH2_A LM_ST	GPOH2 pin output data at ALARM condition (when FDRV_ALM_SD = 1 and GPOH_FET = 1) 1 : Low 0 : Hi-z (Default)
4	GPOH1_A LM_ST	GPOH1 pin output data at ALARM condition (when FDRV_ALM_SD = 1 and GPOH_FET = 1) 1 : Low 0 : Hi-z (Default)
1	GPOH2_E N	GPOH2 pin output 1 : Low 0 : Hi-z (Default)
0	GPOH1_E N	GPOH1 pin output 1 : Low 0 : Hi-z (Default)

Functional Description

Refer table below for possible configuration for each pin.

6. General Purpose Input Output (GPIO1~6)

6.1 GPIO Pins Configuration

There are six low voltage (CVDD) GPIO pins (GPIO1~6) for AN49503A.

Table. GPIO Pins Configuration

pin	Description	Pin Configuration	Internal Pull Down Resistor	Other Function
GPIO1	General Purpose Input Output Pin	Input / Output (Push pull or N-ch open drain) set by register	Pull Down Resistor set by register	Analog Input/ GPOH1Data Output
GPIO2	General Purpose Input Output Pin	Input / Output (Push pull or N-ch open drain) set by register	Pull Down Resistor set by register	Analog Input/ GPOH2Data Output
GPIO3	General Purpose Input Output Pin	Input / Output (Push pull or N-ch open drain) set by register	Pull Down Resistor set by register	High Speed Oscillator Clock Divided Output
GPIO4	General Purpose Input Output Pin	Input / Output (Push pull or N-ch open drain) set by register	Pull Down Resistor set by register	ADIRQ2 / Low Speed Oscillator Clock Divided Output
GPIO5	General Purpose Input Output Pin	Input / Output (Push pull or N-ch open drain) set by register	Pull Down Resistor set by register	ADIRQ1
GPIO6	General Purpose Input Output Pin	Input / Output (Push pull or N-ch open drain) set by register	Pull Down Resistor set by register	ALARM2

6.2 GPIO Pins Input / Output Configuration

Each GPIO Pins can be configured as input or output by register below:

Address：0x0C

bit	Register	Description
13	GPIO6_NOE	GPIO6 Pin Output Enable 1 : Disabled （Default） 0 : Enabled
12	GPIO5_NOE	GPIO5 Pin Output Enable 1 : Disabled （Default） 0 : Enabled
11	GPIO4_NOE	GPIO4 Pin Output Enable 1 : Disabled （Default） 0 : Enabled
10	GPIO3_NOE	GPIO3 Pin Output Enable 1 : Disabled （Default） 0 : Enabled
9	GPIO2_NOE	GPIO2 Pin Output Enable 1 : Disabled （Default） 0 : Enabled
8	GPIO1_NOE	GPIO1 Pin Output Enable 1 : Disabled （Default） 0 : Enabled

Address：0x0C

bit	Register	Description
5	GPIO6_IE	GPIO6 Pin Input Enable 1： Enabled 0： Disable （Default）
4	GPIO5_IE	GPIO5 Pin Input Enable 1： Enabled 0： Disable （Default）
3	GPIO4_IE	GPIO4 Pin Input Enable 1： Enabled 0： Disable （Default）
2	GPIO3_IE	GPIO3 Pin Input Enable 1： Enabled 0： Disable （Default）
1	GPIO2_IE	GPIO2 Pin Input Enable 1： Enabled 0： Disable （Default）
0	GPIO1_IE	GPIO1 Pin Input Enable 1： Enabled 0： Disable （Default）

Functional Description

6.3 GPIO Pins Output Configuration and Pull Down Resistor Configuration

Register address *0x0D* is used to configure output configuration and pull down resistor for each GPIO pin.

Address : 0x0D

bit	Register	Description
13	GPIO6_OD	GPIO6 Pin Output Configuration 1 : Nch Open Drain 0 : Push Pull (Default)
12	GPIO5_OD	GPIO5 Pin Output Configuration 1 : Nch Open Drain 0 : Push Pull (Default)
11	GPIO4_OD	GPIO4 Pin Output Configuration 1 : Nch Open Drain 0 : Push Pull (Default)
10	GPIO3_OD	GPIO3 Pin Output Configuration 1 : Nch Open Drain 0 : Push Pull (Default)
9	GPIO2_OD	GPIO2 Pin Output Configuration 1 : Nch Open Drain 0 : Push Pull (Default)
8	GPIO1_OD	GPIO1 Pin Output Configuration 1 : Nch Open Drain 0 : Push Pull (Default)

Address : 0x0D

bit	Register	Description
5	GPIO6_PD	GPIO6 Pin Pull-Down Resistor 1 : Yes 0 : No（Default）
4	GPIO5_PD	GPIO5 Pin Pull-Down Resistor 1 : Yes 0 : No（Default）
3	GPIO4_PD	GPIO4 Pin Pull-Down Resistor 1 : Yes 0 : No（Default）
2	GPIO3_PD	GPIO3 Pin Pull-Down Resistor 1 : Yes 0 : No（Default）
1	GPIO2_PD	GPIO2 Pin Pull-Down Resistor 1 : Yes 0 : No（Default）
0	GPIO1_PD	GPIO1 Pin Pull-Down Resistor 1 : Yes 0 : No（Default）

Note: When GPIO pin is configured as an output (GPIO[n]_NOE = 0), GPIO[n]_PD shall not be set to 1 at the same time.

6.4 GPIO Pins Input and Output Data Configuration

Register address *0x0E* is used to configure input and output data for each GPIO pin.

Address : 0x0E

bit	Register	Description
13	ST_GPIO6	GPIO6 Pin Input Data 1: HI (CVDD) 0: LO (VSS) （Default）
12	ST_GPIO5	GPIO5 Pin Input Data 1: HI (CVDD) 0: LO (VSS) （Default）
11	ST_GPIO4	GPIO4 Pin Input Data 1: HI (CVDD) 0: LO (VSS) （Default）
10	ST_GPIO3	GPIO3 Pin Input Data 1: HI (CVDD) 0: LO (VSS) （Default）
9	ST_GPIO2	GPIO2 Pin Input Data 1: HI (CVDD) 0: LO (VSS) （Default）
8	ST_GPIO1	GPIO1 Pin Input Data 1: HI (CVDD) 0: LO (VSS) （Default）

Address : 0x0E

bit	Register	Description
5	GPIO6_OUT	GPIO6 Pin Output Data 1 : HI 0 : LO (Default)
4	GPIO5_OUT	GPIO5 Pin Output Data 1 : HI 0 : LO (Default)
3	GPIO4_OUT	GPIO4 Pin Output Data 1 : HI 0 : LO (Default)
2	GPIO3_OUT	GPIO3 Pin Output Data 1 : HI 0 : LO (Default)
1	GPIO2_OUT	GPIO2 Pin Output Data 1 : HI 0 : LO (Default)
0	GPIO1_OUT	GPIO1 Pin Output Data 1 : HI 0 : LO (Default)

Functional Description

6.5 GPIO Pins Output Drivability

Register address *0x0F* is used to configure output drivability for each GPIO pin at output configuration.

Address : 0x0F

bit	Register	Description
5	GPIO6_CHDRV	GPIO6 Pin Output Drivability 1 : 4mA 0 : 2mA (Default)
4	GPIO5_CHDRV	GPIO5 Pin Output Drivability 1 : 4mA 0 : 2mA (Default)
3	GPIO4_CHDRV	GPIO4 Pin Output Drivability 1 : 4mA 0 : 2mA (Default)
2	GPIO3_CHDRV	GPIO3 Pin Output Drivability 1 : 4mA 0 : 2mA (Default)
1	GPIO2_CHDRV	GPIO2 Pin Output Drivability 1 : 4mA 0 : 2mA (Default)
0	GPIO1_CHDRV	GPIO1 Pin Output Drivability 1 : 4mA 0 : 2mA (Default)

6.6 GPIO Pins Function Configuration

Register address *0x17* is used to configure function for each GPIO pin.

Address : 0x17

bit	Register	Description
11-10	GPIO6SEL[1:0]	GPIO6 Pin Function 00: GPIO6 Pin (Default) 01: ALARM2 Output 10: Prohibited 11: Prohibited
9-8	GPIO5SEL[1:0]	GPIO5 Pin Function 00: GPIO5 Pin (Default) 01: ADIRQ1 Output 10: Prohibited 11: Prohibited
7-6	GPIO4SEL[1:0]	GPIO4 Pin Function 00: GPIO4 Pin (Default) 01: ADIRQ2 Output 10: Prohibited 11: Low Speed Oscillator Clock Divided Output (262kHz)
5-4	GPIO3SEL[1:0]	GPIO3 Pin Function 00: GPIO3 Pin (Default) 01: Prohibited 10: Prohibited 11: High Speed Oscillator Clock Divided Output (20.48MHz)
3-2	GPIO2SEL[1:0]	GPIO2 Pin Function 00: GPIO2 Pin (Default) 01: Prohibited 10: Analog Input 11: GPOH2 Output Data
1-0	GPIO1SEL[1:0]	GPIO1 Pin Function 00: GPIO1 Pin (Default) 01: Prohibited 10: Analog Input 11: GPOH1 Output Data

Note: It is required to change other registers accordingly when setting GPIO[n]SEL.

eg. GPIO6 is set to ALARM2,
User shall set:
GPIO6SEL : 01 (ALARM 2)
GPIO6_NOE: 0 (Output enable)
GPIO6_IE: 0 (Input disable)
And set GPIO6_CHDRV, GPIO6_PD and GPIO6_OD accordingly depend on need.

Note: When GPIO1/2 pin is configured as an analog input, GPIO1_IE and GPIO2_IE should be set to 0.

Functional Description

7. Cell Balance Control

Procedure to set up cell balance operation:

1. Set CB_PD to 0 to turn ON cell balance circuit
2. Set DI_CBSEL[16:1] to 1 for cell to be cell balanced
3. Set CB_SET to1 to start cell balancing operation
4. Set CB_SET to 0 to stop cell balancing operation when finish
5. Set DI_CBSEL[16:1] to 0 to deselect cell
6. Repeat step 2 to 5 when doing another cell balancing operation

   or

7. Set CB_PD to 1 to turn OFF cell balance circuit

Cell balance function can be turned ON during Active Mode, and Standby Mode. However, when cell balance is turned ON, the OV/UV detection (only in Active Mode) will not operate correctly, user shall turn OFF OV/UV detection when using cell balance during Active Mode. Adjacent cell should not be operate in cell balance at the same time.

When using cell balance, user shall set 5V LDO to normal operation(register LP50EN to 0). When using the Cell balance, the current per path should not exceed 50mA When multi-cells are to be in cell balance on the same time, the cell balance current for each cell shall not exceed 25mA. If more current is required, it is recommended to use external FET for cell balance. The cell balance current can be decided by external resistor.

Example circuit for using internal MOSFET cell balance and external FET cell balance is given at the figures at the right.

Case 1: using internal FET

$I_{CB(n+1)} = V_{cell(n+1)} / (2R + R_{ON})$

R_{ON} = ON resistance of internal MOSFET (usually negligible when external R is much higher in value)

Case 2: using external FET

$I_{bn(n+1)} = V_{cell(n+1)} / (2R + R_{ON})$

-> $VGS = I_{B(n+1)} * R = V_{cell(n+1)} / 2$

R_{ON} = ON resistance of internal MOSFET

(usually negligible when external R is much higher in value)

$I_{CB(n+1)} = V_{cell(n+1)} / (R_{CB} + R_{ONext})$

R_{ONext} = ON resistance of external MOSFET

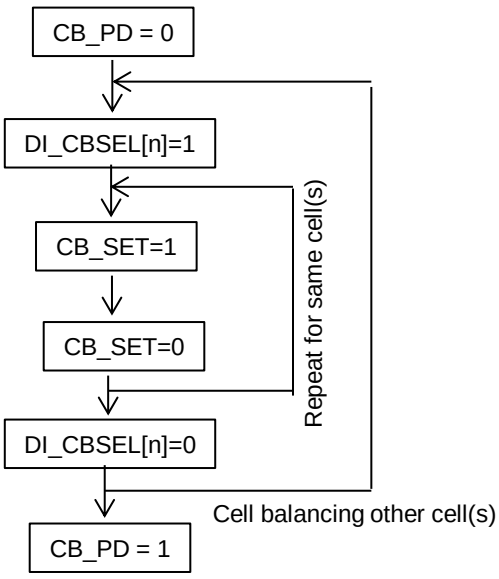
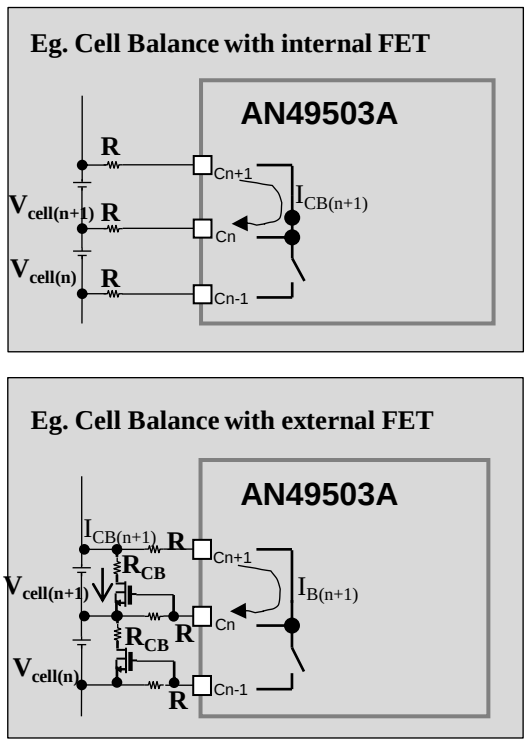


Fig. Cell Balancing Operation Flow



Functional Description

8. Voltage Measurement

The voltage data is measured by the built-in 14 bits ADC in Active Mode with a period of 1.3ms. Figure below shows the sequence of data measured by ADC.

The voltage measurement can be set to continuous measurement (register *ADC_CONT* = 1) or one shot measurement. (register *ADC_CONT* = 0) For one-shot measurement, voltage is measured once when register *ADC_TRG* is set to 1, this register is auto cleared to 0 after measurement completed.

After voltage measurement completed, ADIRQ1 pin (share pin with GPIO5 pin, to be configured as ADIRQ1 output) will flagged HI and register VAD_DONE will be set to 1.

When register *ADV_LATCH* is set to 1, the data will be latched to data register address 0x33~0x4B. this register will be auto reset after data written completely, ADIRQ1 pin will be cleared to 0 when register ADV_LATCH = 1. To cleared register VAD_DONE, it is required to write 1 to this register.

8.1 Cell Voltage Measurement

The battery cell voltage is measured following the sequence in figure below. The converted data will be written to the data registers *CV01_AD ~CV16_AD(0x33~0x42)* when register *ADV_LATCH* is set to 1. Cell data to be latched is set by register *CV[n]SEL*.

The full range and resolution of cell voltage measurement is shown below and listed in table below.

・Maximum input voltage：4.999695V = 5.0V × (2^{14}-1)/2^{14}

・Minimum Input Voltage：0V

・Resolution：0.000305V = 5.0V/2^{14}

Fig. Voltage Measurement Cycle

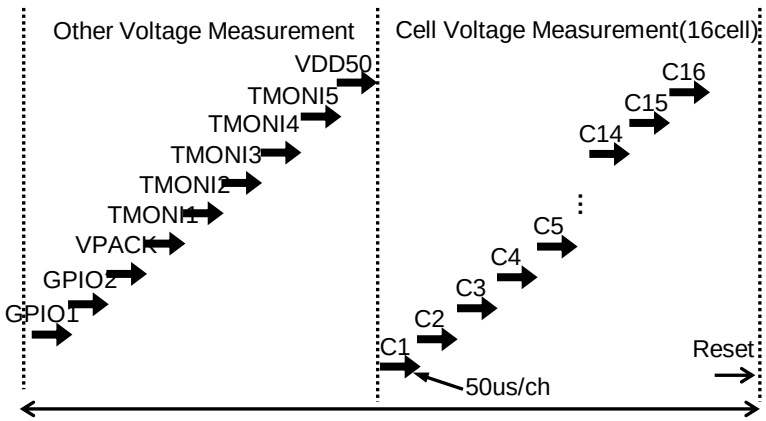


Table. Battery Cell Voltage Conversion Table

Analog level [V] (typ)	Code	Digital output (*CV01_AD*[15:0] to *CV16_AD*[15:0])													
		MSB													LSB
		b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
4.999695	0x3FFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
2.500305	0x2001	1	0	0	0	0	0	0	0	0	0	0	0	0	1
2.500000	0x2000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
2.499695	0x1FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
0.000305	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0.000000	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: b15 and b14 is always 0 and does not affect the calculation of voltage.

Functional Description

8.2 VPACK Voltage Measurement

Voltage at VPACK pin is measured when voltage measurement is done in Active Mode. The converted data will be written to the data register *VPAC_AD* when register *ADV_LATCH* is set to 1 when register VPACSEL = 1.

The full range and resolution of VPACK measurement is shown below and listed in table below.

- Maximum input voltage : 99.993896V = $100.0V \times (2^{14}-1)/2^{14}$
- Minimum Input Voltage : 0V
- Resolution : 0.0060104V: = $100.0V/2^{14}$

The GPIO1/2 voltage is measured at the starting of each voltage measurement. cycle The converted data will be written to the data registers *GPIO1_AD* and *GPIO2_AD* when register *ADV_LATCH* is set to 1, the data to be latched is set by registers GPAD[n]SEL.

It is required for GPIO1/2 to be configured as analog input by register GPIO1/2SEL and input enabled by register GPIO1/2_IE as explained in Section 6.

The full range and resolution of cell voltage measurement is shown below and listed in table below.

- Maximum input voltage : 4.999695V = $5.0V \times (2^{14}-1)/2^{14}$
- Minimum Input Voltage : 0V
- Resolution : 0.000305V = $5.0V/2^{14}$

8.3 GPIO1/2 Voltage Measurement

Table. VPACK Voltage Conversion Table

Analog level [V] (typ)	Code	Digital output (VPAC_AD[15:0])													
		MSB													LSB
		b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
99.993896	0x3FFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
50.006104	0x2001	1	0	0	0	0	0	0	0	0	0	0	0	0	1
50.000000	0x2000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
49.993896	0x1FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
0.006104	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0.000000	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table. GPIO1/2 Voltage Conversion Table

Analog level [V] (typ)	Code	Digital output (GPIO1_AD[15:0] / GPIO2_AD[15:0])													
		MSB													LSB
		b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
4.999695	0x3FFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
2.500305	0x2001	1	0	0	0	0	0	0	0	0	0	0	0	0	1
2.500000	0x2000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
2.499695	0x1FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
0.000305	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0.000000	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: b15 and b14 is always 0 and does not affect the calculation of voltage.

Functional Description

8.4 TMONI1~5 Voltage Measurement

AN49503A has 5 analog input pins TMON1~TMON5, which are measured during Active Mode when voltage measurement is operating..

The converted data will be written to the data registers *TMONI1_AD~TMONI5_AD* when register *ADV_LATCH* is set to 1, the data to be latched is set by registers TMONI[n]SEL.

The full range and resolution of TMONI voltage measurement is shown below and listed in table below.

・Maximum input voltage : 4.999695V = 5.0V × $(2^{14}-1)/2^{14}$

・Minimum Input Voltage : 0V

・Resolution : 0.000305V = $5.0V/2^{14}$

Table. TMONI 1~5 Voltage Conversion Table

Analog level [V] (typ)	Code	Digital output (TMONI1_AD～TMONI5_AD[15:0])													
		MSB													LSB
		b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
4.999695	0x3FFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
2.500305	0x2001	1	0	0	0	0	0	0	0	0	0	0	0	0	1
2.500000	0x2000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
2.499695	0x1FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
0.000305	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0.000000	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: b15 and b14 is always 0 and does not affect the calculation of voltage.

8.5 VDD50 Voltage Measurement

Voltage at VDD50 pin is measured when voltage measurement is done in Active Mode. The converted data will be written to the data register VDD50_AD when register *ADV_LATCH* is set to 1 when register VDD50SEL = 1.

The full range and resolution of VDD50 voltage measurement is shown below and listed in table below.

・Maximum input voltage : 7.499542V = 7.5V × $(2^{14}-1)/2^{14}$

・Minimum Input Voltage : 0V

・Resolution : 0.000458V = $7.5V/2^{14}$

Table. VDD50 Voltage Conversion Table

Analog level [V] (typ)	Code	Digital output (VDD50_AD[15:0])													
		MSB													LSB
		b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7.499542	0x3FFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
3.750458	0x2001	1	0	0	0	0	0	0	0	0	0	0	0	0	1
3.750000	0x2000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
3.749542	0x1FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
0.000458	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0.000000	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: b15 and b14 is always 0 and does not affect the calculation of voltage.

Functional Description

8.6 Temperature Measurement Procedure with TMONI1~5 pins

There are 5 TMONI pins in AN49503A, which can be configured to measure temperature. It is required to connect each TMONI pin with Ground connected thermistor externally.

Internal pull up resistor can be used for temperature measurement, AN49503A has pre-determined internal pull up resistor value for precise temperature measurement.

Procedure to calculate thermistor's resistance from VDD50 pin's voltage and internal pull up resistor is given below:

1. Reading Internal Pull Up Resistor Value
   - Follow following step to read pull up resistor value with FUSE setting

TMONI1 pin's pull up resistor:
a. Set register 0x2E FUSE_RADR 0x2B
b. Read register 0x2F FUSE_DATA bit15-11
c. Set register 0x2E to 0x2C
d. Read register 0x2F bit15-11 and obtain resistor value from next page

TMONI2 pin's pull up resistor:
a. Set register 0x2E to 0x2E
b. Read register 0x2F bit7-0 and obtain resistor value from next page

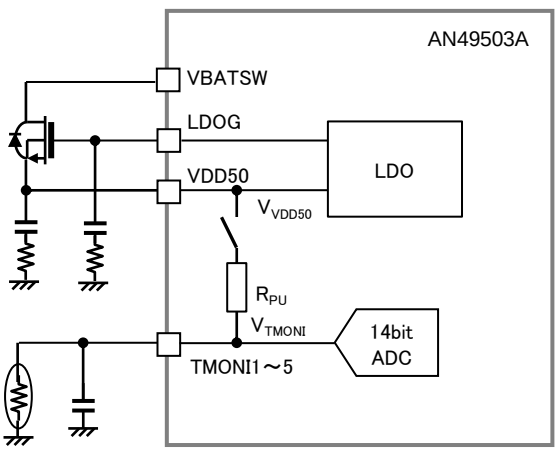


Fig. Thermistor Connection

TMONI3 pin's pull up resistor:
a. Set register 0x2E to 0x2E
b. Read register 0x2F bit15-8 and obtain resistor value from next page

TMONI4 pin's pull up resistor
a. Set register 0x2E to 0x2F
b. Read register 0x2F bit7-0 and obtain resistor value from next page

TMONI5 pin's pull up resistor
a. Set register 0x2E to 0x2F
b. Read register 0x2F bit15-8 and obtain resistor value from next page

2. TMONI pins pull up resistor setting
Set register 0x0F GPIO_CTRL4 bit 12-8 accordingly.
(Pull up resistor only connected during voltage measurement for respective pin)

3. TMONI pin voltage, VDD50 pin voltage measurement
Obtain TMONI pins and VDD50 pin voltage with voltage measurement.

4. Calculate the thermistor resistance
$R_S = V_{TMONI} / (V_{VDD50} – V_{TMONI}) \times R_{PU}$
V_{TMONI} : TMONI pin voltage
V_{VDD50} : VDD50 pin voltage
R_{PU} : TMONI pin pull up resistance

5. Calculate the temperature
Find out the temperature from thermistor datasheet from R_S obtained from step 4.

Address : 0x0F

bit	Name	Description
12-8	PULLUP_SEL [5:1]	TMONI pins pull up control [5] 1 : TMONI5 with internal pull up 0 : TMONI5 without internal pull up [4] 1 : TMONI4 with internal pull up 0 : TMONI4 without internal pull up [3] 1 : TMONI3 with internal pull up 0 : TMONI3 without internal pull up [2] 1 : TMONI2 with internal pull up 0 : TMONI2 without internal pull up [1] 1 : TMONI1 with internal pull up 0 : TMONI1 without internal pull up Default : 0 Note : When the bit data =1, TMONI pins will be pulled up internally only during voltage measurement of respective pin.

Functional Description

Internal Pull Up Resistor Value for TMONI pins

1. For TMONI1 pin

Refer to the table below to obtain pull up resistance from data read (from previous page)

- Max: 12.99414 kΩ
  = 6 kΩ × $(2^9 - 1) / 2^{10}$ + 10kΩ
- Min: 7 kΩ
- Resolution: 5.86 Ω = 6 kΩ / 2^{10}

(2's complement data)

2.For TMONI2 pin

For TMONI2 pin, the differences from TMONI1 pin is determined from the table below using data read (from previous page)

- Max: 0.74414 kΩ
  = 1.5 kΩ × $(2^7 - 1) / 2^8$
- Min: -0.75 kΩ
- Resolution: 5.86 Ω = 1.5 kΩ / 2^8

(2's complement data)

TMONI2's resistance is calculated by =differences read in this step+TMONI1 resistance

3.TMONI3/4/5 pins

TMONI3~TMONI5 resistance can be determined similarly as for TMONI2, with the data read changes accordingly:

TMONI3: 0x2E bit15-8
TMONI4: 0x2F bit7-0
TMONI5: 0x2F bit15-8

Table. TMONI1 pin pull up resistance conversion

resistance [kΩ] (typ)	Code	Fuse Digital output (0x2B[15:11] / 0x2C[15:11])									
		MSB									LSB
		0x2B					0x2C				
		b15	b14	b13	b12	b11	b15	b14	b13	b12	b11
12.99414	0x1FF	0	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・
10.00586	0x001	0	0	0	0	0	0	0	0	0	1
10	0x000	0	0	0	0	0	0	0	0	0	0
9.99414	0x3FF	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・
7.00586	0x201	1	0	0	0	0	0	0	0	0	1
7	0x200	1	0	0	0	0	0	0	0	0	0

Table. TMONI2 pin pull up resistance conversion

resistance (diferrence from TMONI1) [kΩ] (typ)	Code	Fuse Digital output (0x2E[7:0])							
		MSB							LSB
		b7	b6	b5	b4	b3	b2	b1	b0
0.74414	0x7F	0	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・
0.00586	0x01	0	0	0	0	0	0	0	1
0	0x00	0	0	0	0	0	0	0	0
-0.00586	0xFF	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・
-0.74414	0x81	1	0	0	0	0	0	0	1
-0.75	0x80	1	0	0	0	0	0	0	0

Functional Description

9. SRP/SRN Current Measurement (High Speed / Low Speed)

AN49503A built-in with two current measurement mode , high speed (HS) current measurement and low speed (LS) current measurement (Coulomb Counter) using the high accuracy 16 bit ADC. Both are done by measuring the voltage across SRP and SRN pins.

HS current measurement are available at Active Mode while LS current measurement are available at Active Mode and Standby Mode.

By setting registers ADSWHY_EN and IADH_ON to 1, HS current measurement is enabled. It will start coincide with cell voltage measurement. When measurement completed, ADIRQ1 pin (same as voltage measurement) will flagged HI, and IADH_DONE will become 1.

By setting registers ADSWSD_EN and IADL_ON to 1, LS current measurement is enabled and started. When completed, ADIRQ2 pin (share pin with GPIO4 pin, to be configured as ADIRQ2 output) will flagged HI, and IADL_DONE will become 1.

The converted data is written to the data registers *CVIH_AD* for HS current measurement when register ADIH_LATCH is set to 1. The converted data is written to register CVIL_AD for LS current measurement when register ADIL_LATCH is set to 1. Both registers ADIH_LATCH and ADIL_LATCH are auto cleared to 0 after data latched completed. ADIRQ1/2 is reset to LO when registers ADIH_LATCH and ADIL_LATCH is set to 1. To clear registers IADH_DONE and IADL_DONE, write 1 to each register.

The full range and resolution of cell voltage measurement is shown below and listed in table below.

- Maximum input voltage : +179.994507 mV
  = 360 mV × $(2^{15} - 1) / 2^{16}$
- Minimum input voltage : -180 mV
- Resolution : 0.005493 mV = 360 mV / 2^{16}

The explanation of current measurement operation is explained in Section 12 and 13.

Table. SRP/SRN Voltage Conversion Table

Analog level [mV] (typ)	Code	Digital output (CVIL_AD[15:0] / CVIH_AD[15:0])															
		MSB															LSB
		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
179.994507	0x7FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
0.005493	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-0.005493	0xFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
-179.994507	0x8001	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
-180	0x8000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Functional Description

10. Monitoring and Protection

10.1 ALARM Pins Operation

AN49503A indicates abnormal condition through ALARM pins. When there is an abnormal condition occurs, designated ALARM pins will be triggered LO depend on register *ALARMSEL* setting. As ALARM2 is shared pin with GPIO6, it is required to configure GPIO6 when use as ALARM2, refer Section 6 for the details.

AN49503A built-in with 2 ALARM pins, which the setting of these pins are shown in table below.

Table. ALARM pins output at different condition

Condition	Abnormal Condition	ALARMSEL = 0	ALARMSEL = 1	
		ALARM1	ALARM1	ALARM2
Over Voltage Under Voltage Over Current	OV/UV/OC	LO	HI	LO
Short Circuit	SC	LO	LO	HI
Normal Condition	SV	HI	HI	HI

10.2 Overcurrent at Charge and Discharge and Short Circuit at Discharge Protection (OCC, OCD, SCD)

At Active Mode and Standby Mode, OCC, OCD and SCD protection can be enabled. The detection is done by measuring voltage across SRP/SRN. Each detection is enabled by registers EN_OCC, EN_OCD and EN_SCD respectively and EN_CP is set to 1.

In AN49503A. The detection threshold are set by registers OCC_C[4:0] , OCD_D[4:0] and SCD_D[3:]] respectively. While the delay time are set by register OCC_DLY[3:0], OCD_DLY[3:0] and OCC_DLY[3:0] respectively.

There are 2 types of register to look for when OCC/OCD/SCD condition occurs. MODE_STAT register [0x22] COND_SCD, COND_OCD and COND_OCC will be flagged immediately according to alarm state. STAT register [0x30] *ST_SCD, ST_OCD* and *ST_OCC* will be flagged after delay time and ALARM pin will output a LO indicating an incident of abnormality.
ALARM pin and flagged STAT register [0x30] are not automatically cleared if the OC/SC condition removed. User has to write 1 to each status register to clear the register and ALARM will be cleared immediately.

The response of DIS and CHG FET control and GPOH1/2 to ALARM will be discussed in section 10.5.

Tables below shows the settable threshold level for OC for charge and discharge and SC for discharge.

Table. Overcurrent in Charge Threshold Setting

Analog level [mV]	Digital output (OCC_D[4:0])					
	Code	MSB				LSB
		b4	b3	b2	b1	b0
200	0x13	1	0	0	1	1
190	0x12	1	0	0	1	0
.	.	.	.	.	.	.
20	0x01	0	0	0	0	1
10	0x00	0	0	0	0	0

Table. Overcurrent in Discharge Threshold Setting

Analog level [mV]	Digital output (OCD_D[4:0])					
	Code	MSB				LSB
		b4	b3	b2	b1	b0
800	0x1F	1	1	1	1	1
775	0x1E	1	1	1	1	0
.	.	.	.	.	.	.
50	0x01	0	0	0	0	1
25	0x00	0	0	0	0	0

Table. Short Circuit in Discharge Threshold Setting

Analog level [mV]	Digital output (SCD_D[3:0])				
	Code	MSB			LSB
		b3	b2	b1	b0
800	0x0F	1	1	1	1
750	0x0E	1	1	1	0
.	.	.	.	.	.
100	0x01	0	0	0	1
50	0x00	0	0	0	0

Functional Description

10.3 Over and Under Voltage Protection (OV, UV)

The detection of OV/UV is done by the voltage measurement ADC and is only function during Active Mode. Registers OVMSK[n] and UVMSK[n] are used to determine the cell for OV and UV detection.

The threshold for OV/UV detection is set by register *OVTH[5:0]* and *UVTH[5:0]* respectively. The OV threshold can be limited by register *OVHLMT*, by default, OVHLMT = 0, and the lowest limit of OV threshold is set to 3.5V. When OVHLMT is set to 1, the lowest limit of OV threshold is set to 2.0V.

The delay time of OV/UV is set by registers *OV_DLY[1:0]* and *UV_DLY[1:0]*. The OV/UV is designed with hysteresis to prevent the mis-trigger due to varying in cell voltage. This hysteresis level is set by registers *OV_HYS[2:0]* and *UV_HYS[2:0]*.

When a OV/UV condition occurs, status register *ST_OV* and *ST_UV, registers OV[n]_F, UV[n]_F will be flagged immediately accordingly,* and if the condition hold longer than the delay time set, ALARM pin will output LO indicating an incident of OV/UV. The condition will be determined by registers OV[n]_LF and UV[n]_LF.

For OV/UV condition, , status register *ST_OV* and *ST_UV, registers OV[n]_F, UV[n]_F will be cleared automatically if the condition removed while* ALARM pin will be cleared if the OV/UV condition removed with the hysteresis level set for longer than delay time set. OV[n]_LF, UV[n]_LF register will be hold until it is cleared by user by writing 1 to each register.

During Standby Mode, when register *STB_MONEN and ADC_CONT are set to 1*, and AN49503A does not receive effective SPI communication with MCU for 1s, it will automatically change to Active Mode for OV/UV detection and resume to Standby Mode after the operation.

The response of DIS and CHG FET control and GPOH1/2 to ALARM condition will be explained in Section 10.5.

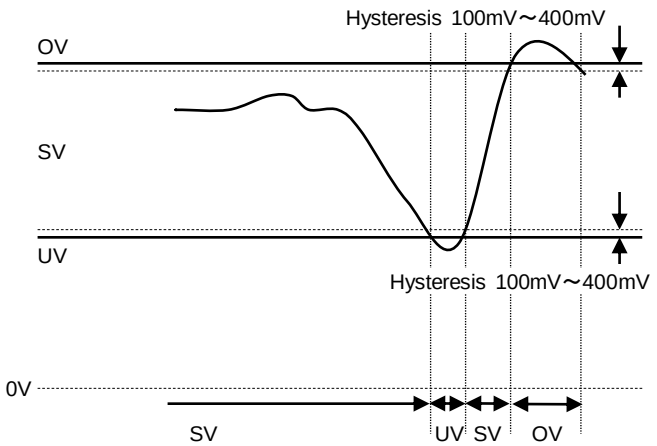


Fig. OV/UV detection threshold

Tables below shows the threshold level for OV and UV.

Address：0x07

bit	register	Description
15	OVHLMT	OV Threshold Lowest Limit 0 : Lowest Limit = 2.0V 1 : Lowest Limit = 3.5V (Default)

Table. OV Threshold Level Setting

Analog level [V] (typ)	Code	Digital output (OVTH[5:0]) MSB b5	b4	b3	b2	b1	LSB b0
4.500	0x34	1	1	0	1	0	0
4.450	0x33	1	1	0	0	1	1
・	・		・	・	・	・	・
3.550	0x21	1	0	0	0	0	1
3.500	0x20	1	0	0	0	0	0
3.450	0x1F	0	1	1	1	1	1
・	・		・	・	・	・	・
2.050	0x03	0	0	0	0	1	1
2.000	0x02	0	0	0	0	1	0

Note: When OVHLMT = 1、OVTH[5] will be fixed to 1.

Table. UV Threshold Level Setting

Analog level [V] (typ)	Code	Digital output (UVTH[5:0]) MSB b5	b4	b3	b2	b1	LSB b0
3.000	0x32	1	1	0	0	1	0
2.950	0x31	1	1	0	0	0	1
・	・		・	・	・	・	・
0.550	0x01	0	0	0	0	0	1
0.500	0x00	0	0	0	0	0	0

Functional Description

10.4 Monitoring and Protection Setting and OV Detection Timing Chart Example

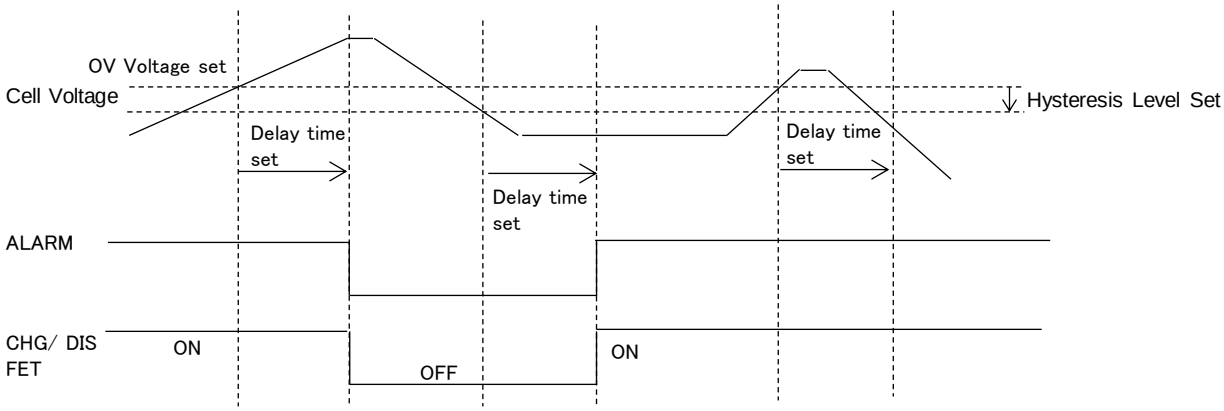
Table below summarize the threshold for current and voltage detection. The operation of DIS_FET, CHG_FET and GPOH pins under abnormal condition is explained in section 10.5.

Table. Abnormality Detection Setting Overview

Abnormal Condition		MIN	MAX	STEP	BITS	Recovery
Over voltage	Voltage	2.0V/3.5V	4.5V	50mV	6/5	Hysteresis and MCU control
	Delay	1000ms	4000ms	1000ms	2	
	Hysteresis	100mV	450 mV	50mV	3	
Under voltage	Voltage	0.5V	3.0V	50mV	6	Hysteresis and MCU control
	Delay	1000ms	4000ms	1000ms	2	
	Hysteresis	100mV	450 mV	50mV	3	
Over current in charge	Voltage	10mV	200mV	10 mV	5	Removal of condition and MCU control
	Delay	1ms	16ms	1ms	4	
Over current in discharge	Voltage	25mV	800mV	25mV	5	Removal of condition and MCU control
	Delay	1ms	16ms	1ms	4	
Short circuit in discharge	Voltage	50 mV	800 mV	50mV	4	Removal of condition and MCU control
	Delay	50 us	1600 us	50 us	5	

When OV condition hold less than delay time set, ALARM signal is not triggered.

Fig. OV Detection Timing Chart (Active Mode)



The details of CHG/DIS operation under ALARM condition are provided in next few pages

Functional Description

10.5 GPOH1/2, DIS and CHG Control Response at ALARM Condition

GPOH1/2, DIS and CHG control can be set to response to ALARM condition depend on register *FDRV_ALM_SD*, *FDRV_ALM_RCV* and *FDRV_ALM_CLR* setting as shown.

Address : 0x03

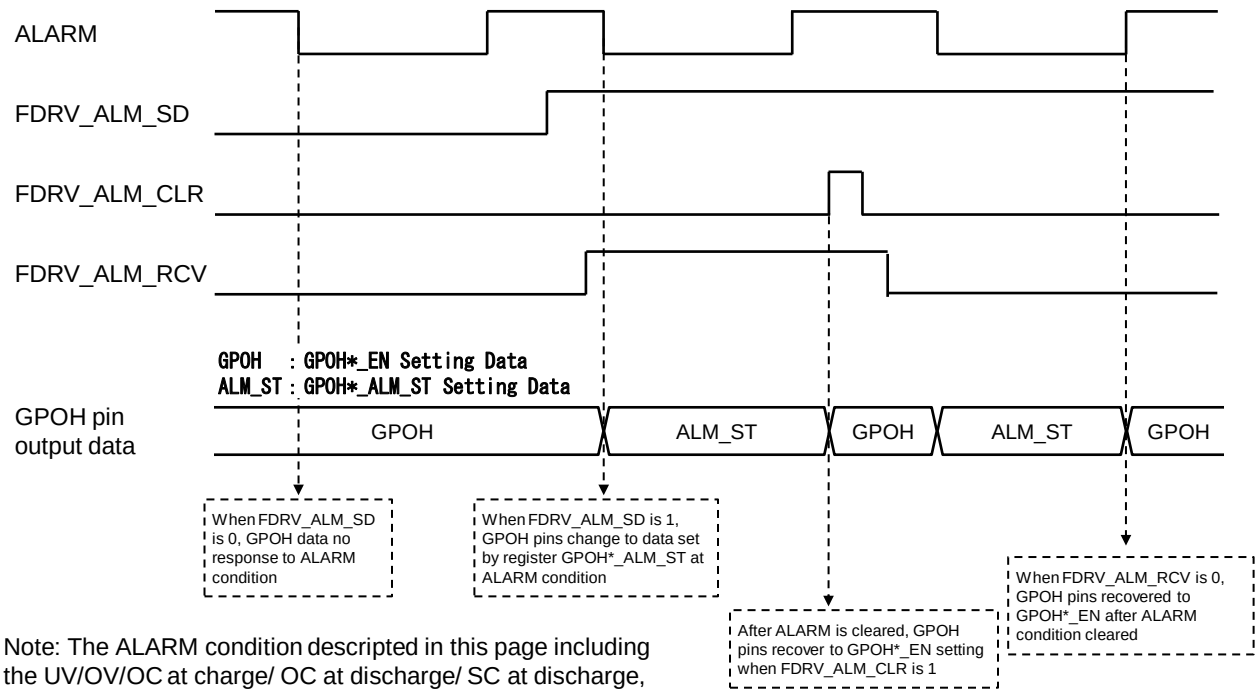
bit	Register	Description
15	FDRV_ALM_SD	Set GPOH1/2, DIS and CHG control response to ALARM condition
14	FDRV_ALM_RCV	Auto recover GPOH1/2, DIS and CHG Control at ALARM cleared
13	FDRV_ALM_CLR	Manual clear GPOH1/2, DIS and CHG Control at ALARM cleared

10.5.1 GPOH1/2 Response to ALARM Condition

Table GPOH Pin Control (when GPOH_FET = 1)

Status	FDRV_ALM_SD	FDRV_ALM_RCV	FDRV_ALM_CLR	GPOH1/2 Pins Output
Initial	–	–	–	As set by register GPOH*_EN
ALARM=1 (Normal)	–	–	–	As set by register GPOH*_EN
ALARM=0 (Abnormal)	1	–	–	As set by register GPOH*_ALM_ST
	0	–	–	As set by register GPOH*_EN
ALARM=1 (Normal)	1	1	0	As set by register GPOH*_ALM_ST
	1	0	–	As set by register GPOH*_EN
	1	1	1	As set by register GPOH*_EN

Figure. GPOH at ALARM Detection Timing Chart (ALARM detection ON)



Note: The ALARM condition descripted in this page including the UV/OV/OC at charge/ OC at discharge/ SC at discharge, and it is LO at ALARM condition.

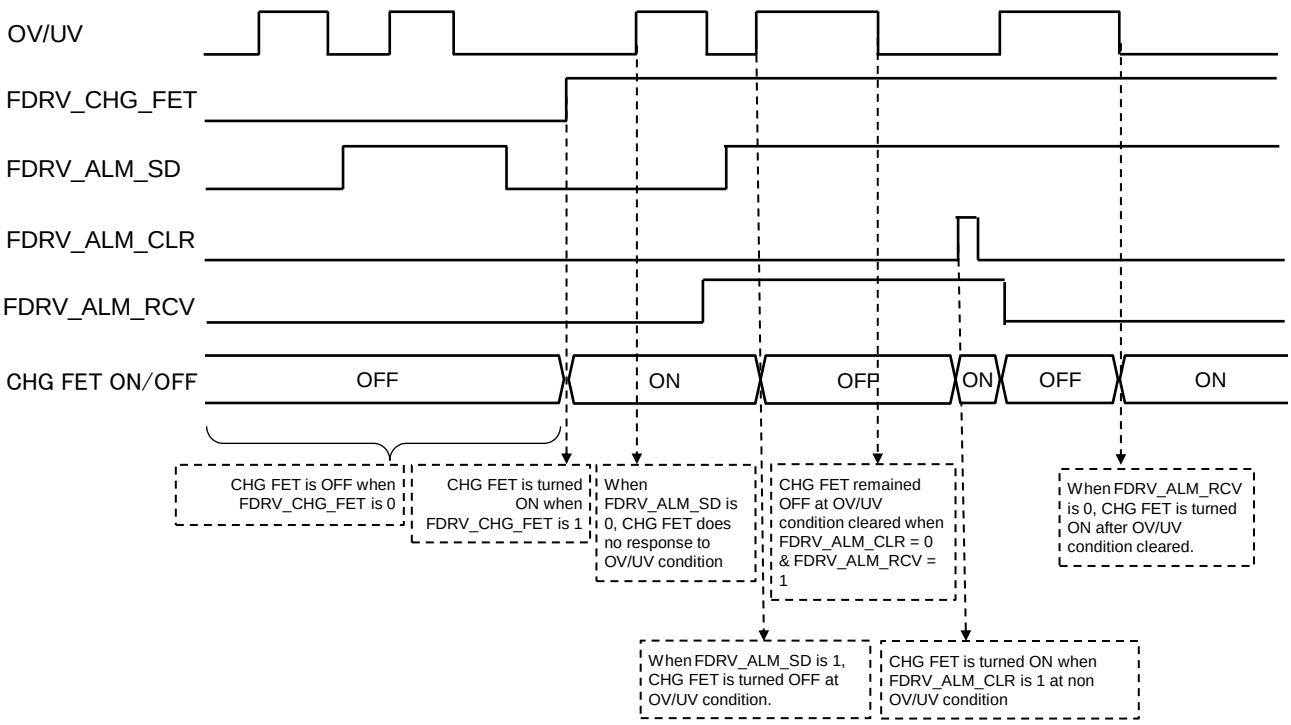
Functional Description

10.5.2 CHG FET Response to ALARM Condition

Table CHG pin control

Status	FDRV_CHG_FET	FDRV_ALM_SD	FDRV_ALM_RCV	FDRV_ALM_CLR	CHG FET ON/OFF	CHG Voltage
Initial					OFF	VBAT
OV/UV/OCC Normal（0）	0	-	-	-	OFF	VBAT
	1	-	-	-	ON	VBAT + 11V(typ)
OV/UV/OCC Abnormal（1）	1	1	-	-	OFF	VBAT
	1	0	-	-	ON	VBAT + 11V(typ)
OV/UV Normal（0）	1	1	1	0	OFF	VBAT
	1	1	0	-	ON	VBAT + 11V(typ)
OCC Normal（0）	1	1	1	0	OFF	VBAT
	1	1	0	-	OFF	VBAT
OV/UV/OCC Normal（0）	1	1	1	1	ON	VBAT + 11V(typ)

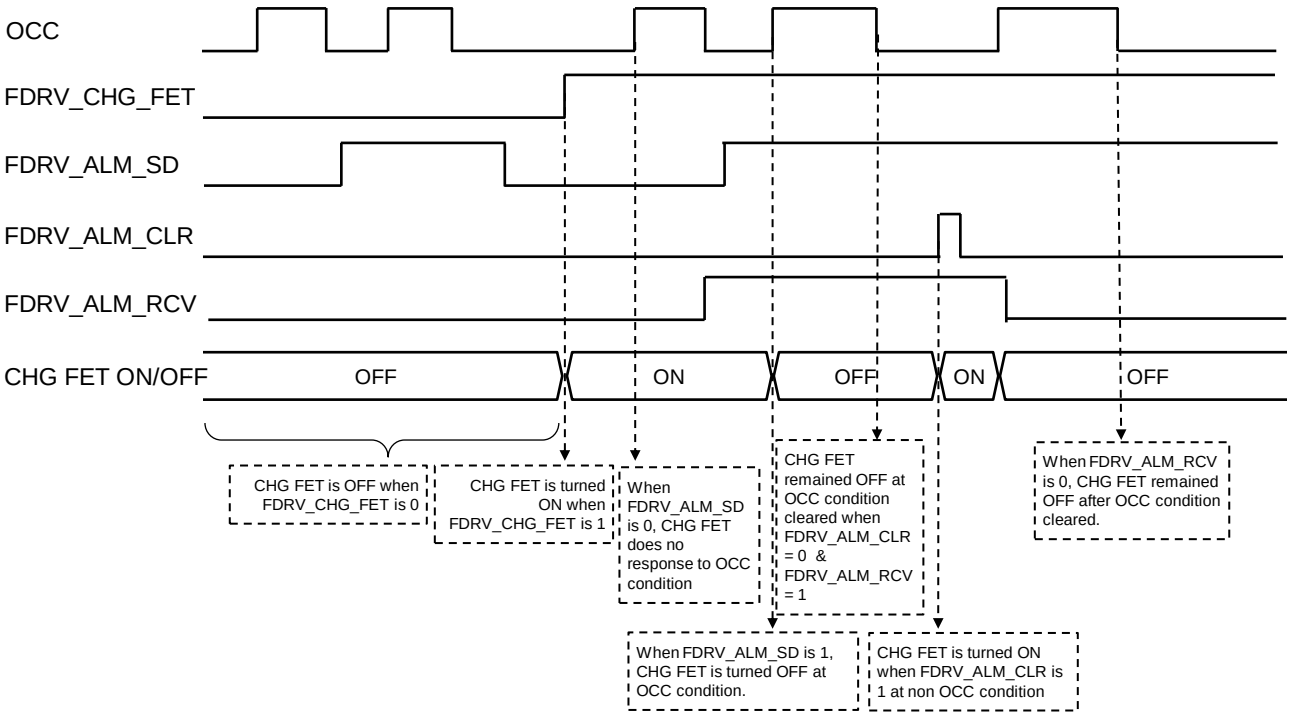
Figure. CHG FET at OV/UV Detection Timing Chart (OV/UV Detection ON)



Functional Description

10.5.2 CHG FET Response to ALARM Condition (cont'd)

Figure. CHG FET at OCC Detection Timing Chart (OCC Detection ON)



Note: CHG pins does not resume from OCC condition when condition cleared and FDRV_ALM_RCV=0, but it resume when FDRV_ALM_CLR=1 when condition cleared.

10.5.3 DIS FET Response to ALARM Condition

Table. DIS pin control

Status	FDRV_DIS_FET	FDRV_ALM_SD	FDRV_ALM_RCV	FDRV_ALM_CLR	DIS FET ON/OFF	DIS Voltage
Initial					OFF	VPACK
OV/UV/OCD/SCD Normal (0)	0	-	-	-	OFF	VPACK
	1	-	-	-	ON	VPACK + 11V(typ)
OV/UV/OCD/SCD Abnormal (1)	1	1	-	-	OFF	VPACK
	1	0	-	-	ON	VPACK + 11V(typ)
OV/UV Normal(0)	1	1	1	0	OFF	VPACK
	1	1	0	-	ON	VPACK + 11V(typ)
OCD/SCD Normal(0)	1	1	1	0	OFF	VPACK
	1	1	0	-	OFF	VPACK
OV/UV/OCD/SCD Normal (0)	1	1	1	1	ON	VPACK + 11V(typ)

Functional Description

10.5.3 DIS FET Response to ALARM Condition (cont'd)

Figure. DIS FET at OV/UV Detection (OV/UV detection ON)

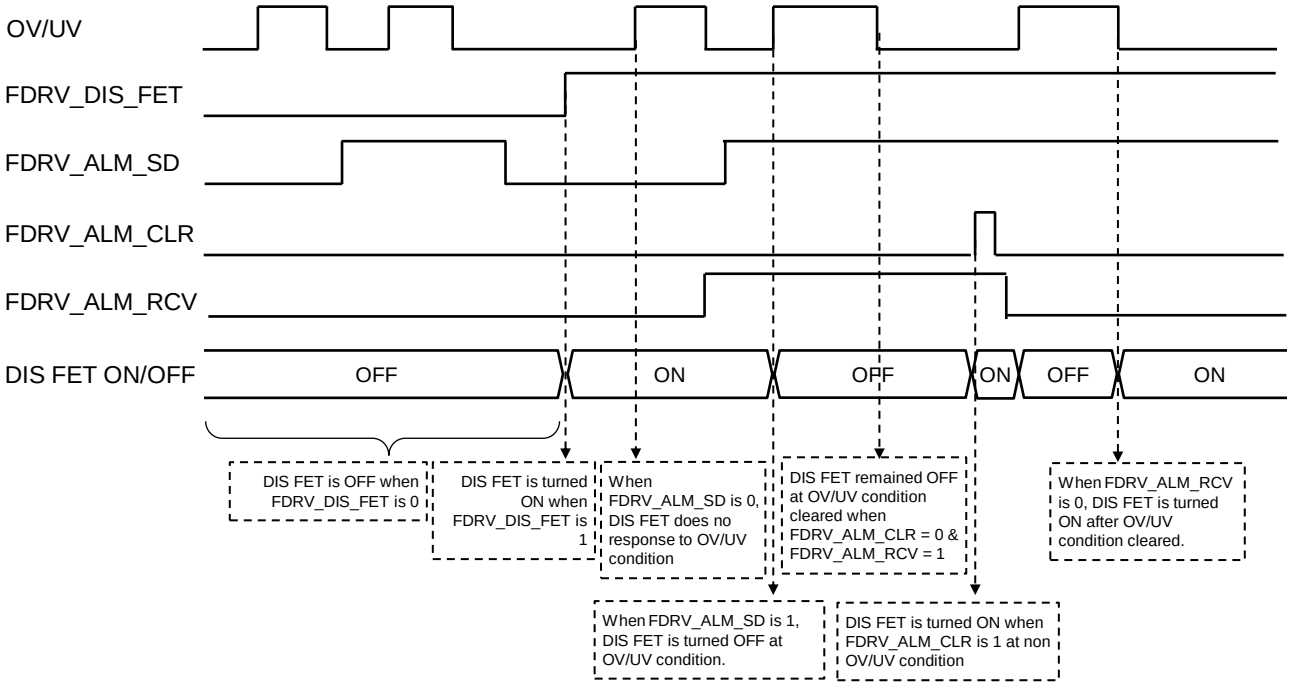
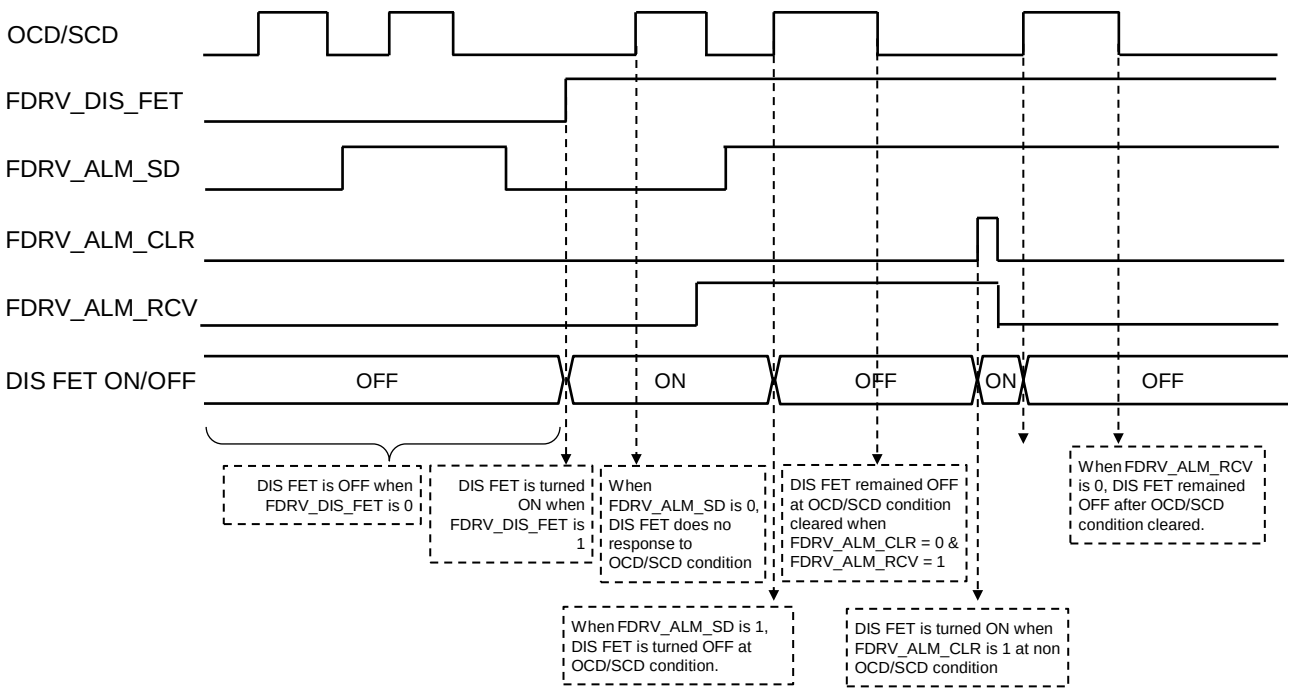


Figure. DIS FET at OCD/SCD Detection Timing Chart (OC/SC Detection ON)



Note: DIS pins does not resume from OCD/SCD condition when condition cleared and FDRV_ALM_RCV=0, but it resume when FDRV_ALM_CLR=1 when condition cleared.

Functional Description

11. Voltage and High Speed (HS) Current Measurement Timing

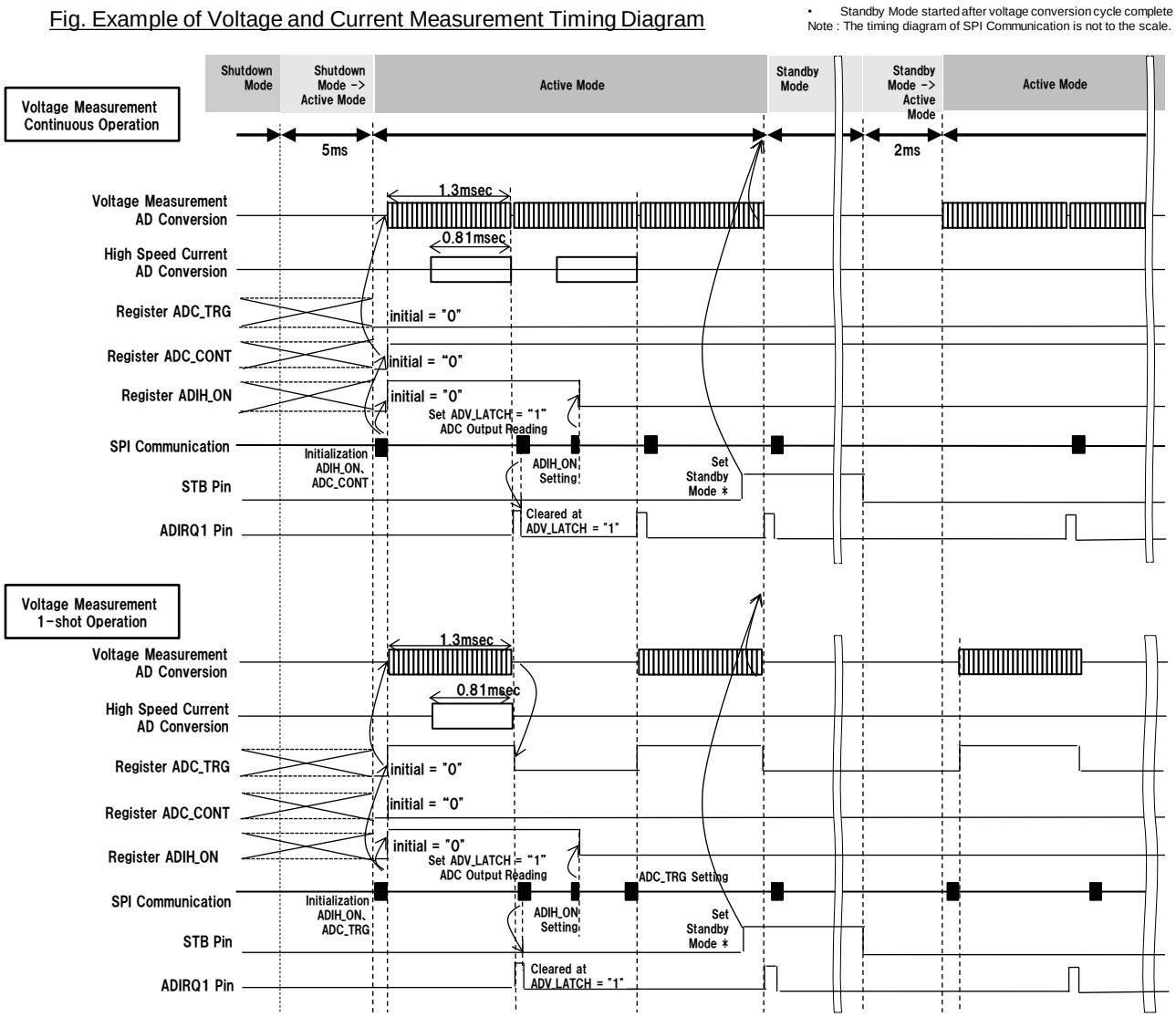
Voltage measurement is operated during active mode only. There are two measurement operation, continuous measurement (when *ADC_CONT* = 1) and one shot operation (when *ADC_CONT* = 0). During continuous measurement, the voltage measurement cycle is repeating. While one shot measurement is done once when register *ADC_TRG* is set to 1. This register is automatically cleared to 0 after measurement.

When each measurement cycle completed, ADIRQ1 pin will be triggered to HI and register *VAD_DONE* will be set to 1. ADIRQ1 is cleared when register *ADV_LATCH* is set to 1. Measured data is latched to data register 0x33~0x4B, ADIRQ1 pin will be reset to LO and register ADV_LATCH become 0 after completion. Register *VAD_DONE* is cleared by write 1 to it.

HS current measurement only operates during active mode which can be set by register *ADIH_ON and ADSWHY_EN to 1*. HS current measurement will start at next cell voltage measurement. The current is measured at the same time cell voltage is being measured, which is about 0.81ms for each measurement.

When current measurement completed, register *IADH_DONE* will be set to "1", and the measured data is latched to data register *CVIH_AD* when register *ADIH_LATCH* is set to 1, this register is cleared to 0 after completion. Register I*ADH_DONE* is cleared by write 1 to it.

Fig. Example of Voltage and Current Measurement Timing Diagram



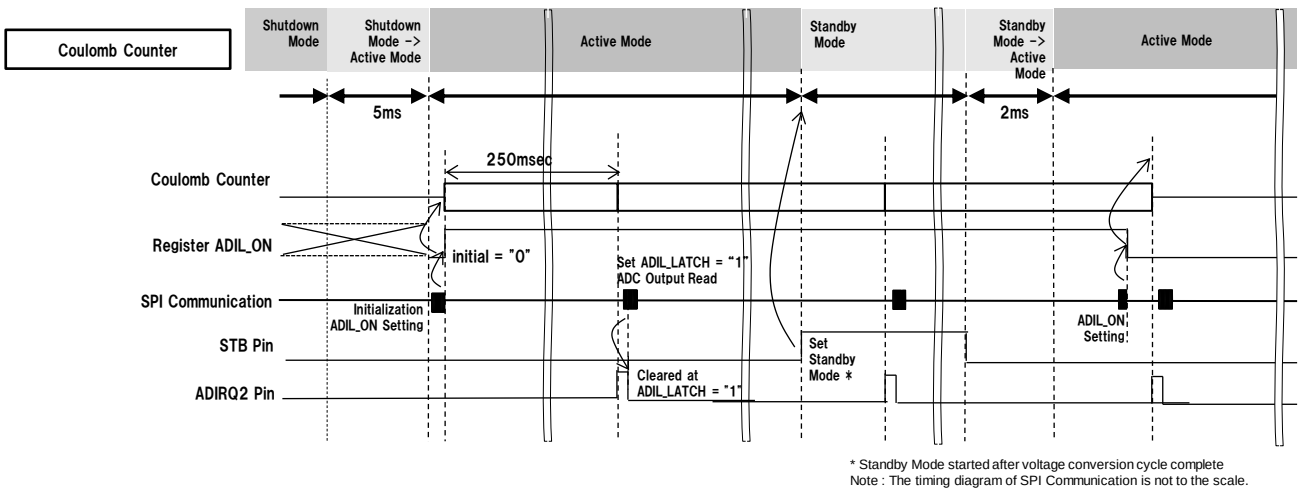
Functional Description

12. Low Speed Current Measurement (Coulomb Counter) Timing

Coulomb Counter can be operating during Active Mode and Standby Mode. The measurement starts when register *ADIL_ON* and ADSWSD_EN set to 1 and accumulating the current for a period of 250ms.

When each measurement cycle completed, **ADIRQ2** pin will be triggered to HI and register *IADS_DONE* will be set to 1. The measured data will be updated to register *CVIL_AD* when register ADIL_LATCH is set to 1. **ADIRQ2** pin is cleared when register *ADIL_LATCH* is set to 1. Register *ADIL_LATCH* is cleared to 0 after completion. Register I*ADS_DONE* is cleared by write 1 to it.

Fig. Example Coulomb Counter Timing Diagram



* Standby Mode started after voltage conversion cycle complete
Note : The timing diagram of SPI Communication is not to the scale.

Functional Description

13. ADC Measurement Setting Procedure

13.1 AD Setting

For Voltage Measurement

1. Set Measurement Target:
   Register address:
   0x04(CVSEL) : cell 1~16
   0x05(GVSEL) : VPACK, GPIO1/2, TMONI1~5, VDD50
2. Set UV/OV Setting:
   Register Address :
   0x06(OUVCTL1): OV/UV threshold level
   0x07(OUVCTL2): OV/UV hysteresis, delay time, OVHLMT
   0x08(UVMSK): UV Detection Mask Cell 1~16
   0x09(OVMSK): OV Detection Mask Cell 1~16
3. TMONI Pull Up Setting:
   Register Address :
   0x0F(GPIO_CTL4) b12-8: Set to 1 when use as TMONI
4. ADIRQ1 Pin Setting:
   Register Address:
   0x0C(GPIO_CTL1), 0x17(GPIOSEL):
   for ADIRQ1pin setting (which is shared pin with GPIO5) (Section 6)

For Current Measurement (High Speed)

1. Set AD Input Enable:
   Register Address 0x1A b13: ADSWHY_EN set to 1
2. Measurement Enable:
   Register Address 0x1A b0: IADH_ON set to 1

For Current Measurement (Low Speed)

1. ADIRQ2 Pin Setting:
   Register Address:
   0x0C(GPIO_CTL1), 0x17(GPIOSEL):
   for ADIRQ2 pin setting (shared pin with GPIO4)

Some of the register require register address 0x0B (LOCK_CONT) to be set to correct value before.

13.2 Start AD Measurement

For Voltage Measurement

1. Continuous Measurement :

Register Address:
0x01 b8 : ADC_CONT set to 1.
or
2. 1shot Measurement :

Register Address:
0x0A b4: ADC_TRG set to 1(ADC_CONT =0).

For Current Measurement (High Speed)

1. When IADH_ON =1, high speed measurement is started at the same time as cell voltage measurement.

For Current Measurement (Low Speed)

1. AD Input Enable:
   Register Address :
   0x1A b12 : ADSWSD_EN set to1
2. Register address:
   0x1A b1: IADL_ON set to 1

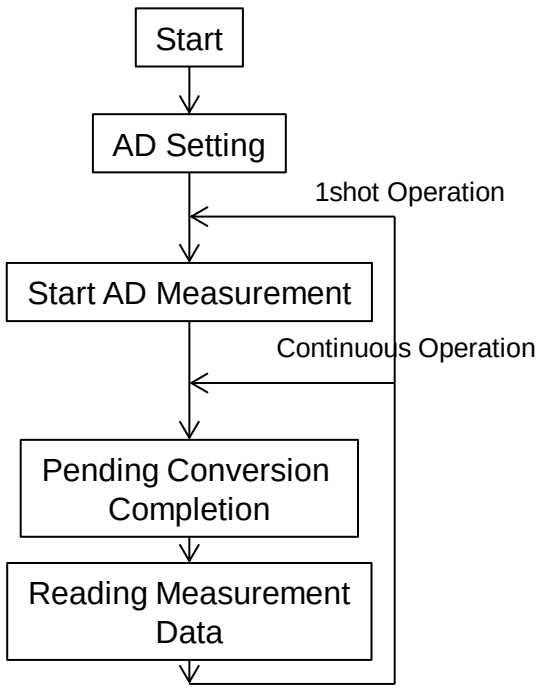


Fig. ADC Conversion Flow

Functional Description

13. ADC Measurement Setting Procedure

13.3 Pending Conversion Completion

For Voltage Measurement

1. Detection of measurement completion with:
   a. When using interrupt ADIRQ1 pin:
      ADIRQ1 -> HI when measurement complete,

or

   b. Using flag polling:
      Read register address 0x30 b0 VAD_DONE:
      it become 1 when measurement complete,
      (write 1 to clear this register)

For Current Measurement (High Speed)

1. Detection of measurement completion with:
   a. When using interrupt ADIRQ1 pin:
      ADIRQ1 -> HI when measurement complete,

or

   b. Using flag polling:
      Read register address 0x30 b1 IADH_DONE:
      it become 1 when measurement complete,
      (write 1 to clear this register)

For Current Measurement (Low Speed)

1. Detection of measurement completion with:
   a. When using interrupt ADIRQ2 pin:
      ADIRQ2 -> HI when measurement complete,

or

   b. Using flag polling:
      Read register address 0x30 b2 IADL_DONE:
      it become 1 when measurement complete,
      (write 1 to clear this register)

13.4 Reading Measurement Data

For Voltage Measurement

1. Latch measured data to data register
Register address:
0x0A b0 ADV_LATCH to 1

2. Detect Latch Completion with
   a.. Polling until ADV_LATCH become 0 or ADIRQ1 become LO

or

   b. Wait for 315ns

3. Reading data registers
Read register address 0x33~0x4B CV01_AD~GPIO2_AD

For Current Measurement (High Speed)

1. Latch measured data to data register
Register address:
0x0A b1 ADIH_LATCH to 1

2. Detect Latch Completion with
   a.. Polling until ADV_LATCH become 0

or

   b. Wait for 315ns

3. Reading data registers
Read register address 0x4C CVIH_AD

For Current Measurement (Low Speed)

1. Latch measured data to data register
Register address:
0x0A b2 ADIL_LATCH to 1

2. Detect Latch Completion with
   a.. Polling until ADIL_LATCH become 0 or ADIRQ2 become LO

or

   b. Wait for 48us

3. Reading data registers
Read register address 0x4D CVIL_AD

Functional Description

14.Open Detection

AN49503A has built-in with open detection function. The operation is as following.

1. Firstly, obtain the cell voltage before performs open detection
2. Secondly, turn ON the open detection
   a. set register 0x1E bit0 INR_EN to 1
   b. set register 0x1C INR_CV[15:0] and register 0x1D INR_CV16 accordingly (pin to be performed open detection is set to 1)
   ⇒ By doing so, it will draw about 32uA from C2～C16 pins to Ground, and it will source about 32uA to C0,C1.
3. Obtain cell voltage when open detection is performed.
   - After required time is decided by external RC,（when R=1k, C=1uF, about 10ms）, measure again the cell voltage
4. Stop open detection
   a. set register 0x1C INR_CV[15:0] and register 0x1D INR_CV16 to 0
   b. set register 0x1E bit0 INR_EN to 0
5. Compare Data
   - Compare data obtained from 1 and 3, when the differences is large (eg 100mV or above), it could be considered as open circuit

Please note that, when C2 and C1 is set to perform open detection, the changes of measured voltage of V2 could be large despite no open connection occur. In this case, the changes of measured voltage may be ⊿V2=2 x 32uA x Rc.

Fig. Open Detection Circuit

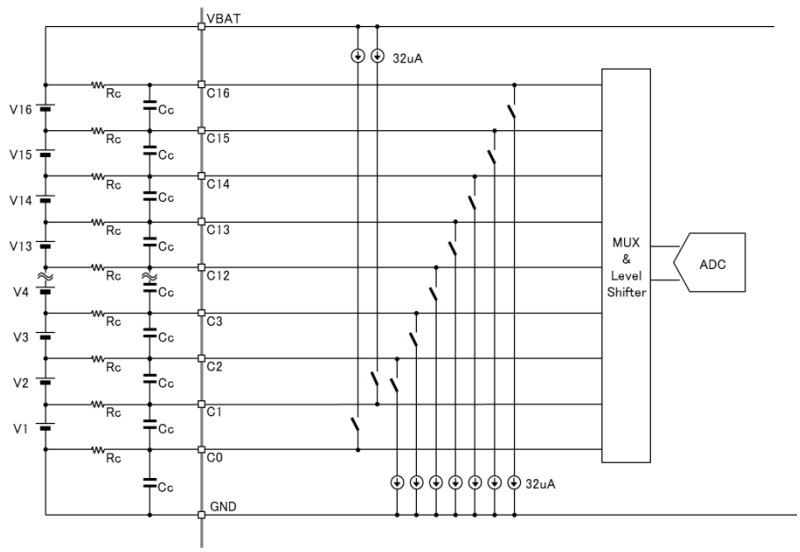
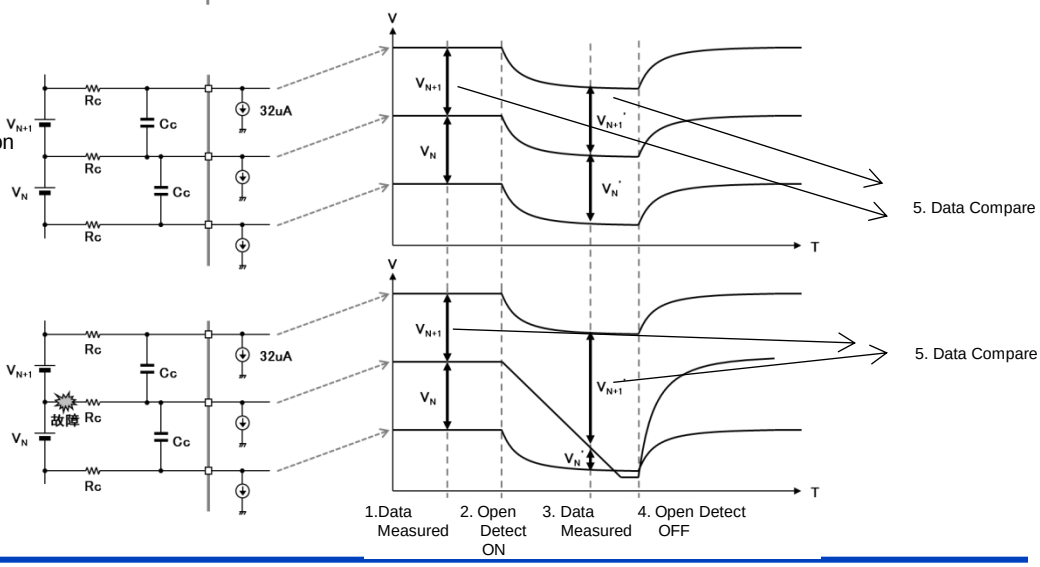


Fig. Open Detection Operation



Functional Description

15. Communication

15.1 SPI Communication Interface

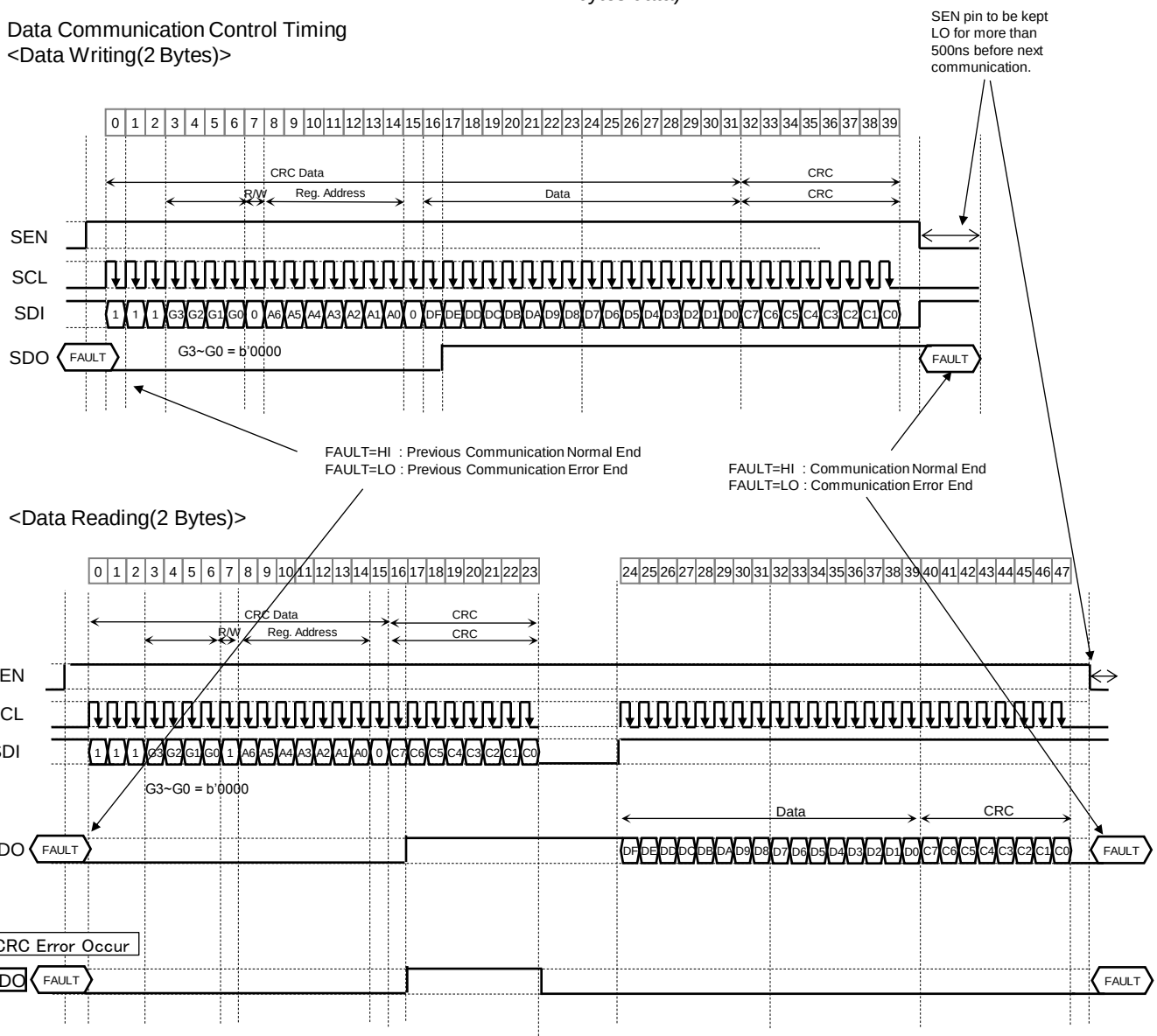
AN49503A communicates with MCU using four lines SPI communication interface, with SDI, SDO, SCL and SEN pins. When wake up to Active Mode from Shutdown Mode, SDO will change from LO to HI, indicating AN49503A is ready for communication, communication can be started after 500ns. Use b'0000 for G3~G0 for SPI communication.

AN49503A uses CRC for communication error detection, the polynomial for CRC generator is $X^8+X^7+X^6+X^4+X^2+1$.

SDO pin is used to indicate the correctness of communication, when there is error with the communication, **SDO** pin will become LO. The causes of error could be read from status register SPI_F as explained in section 15.3. All register data are double byte size, refer register map for details.

The communication support the following communication mode:
1.MCU to AN49503A single data write (2 bytes)
2.MCU to AN49503A single data read (2 bytes)
3.MCU to AN49503A continuous data read (up to 128 2 bytes data)

Data Communication Control Timing
<Data Writing(2 Bytes)>

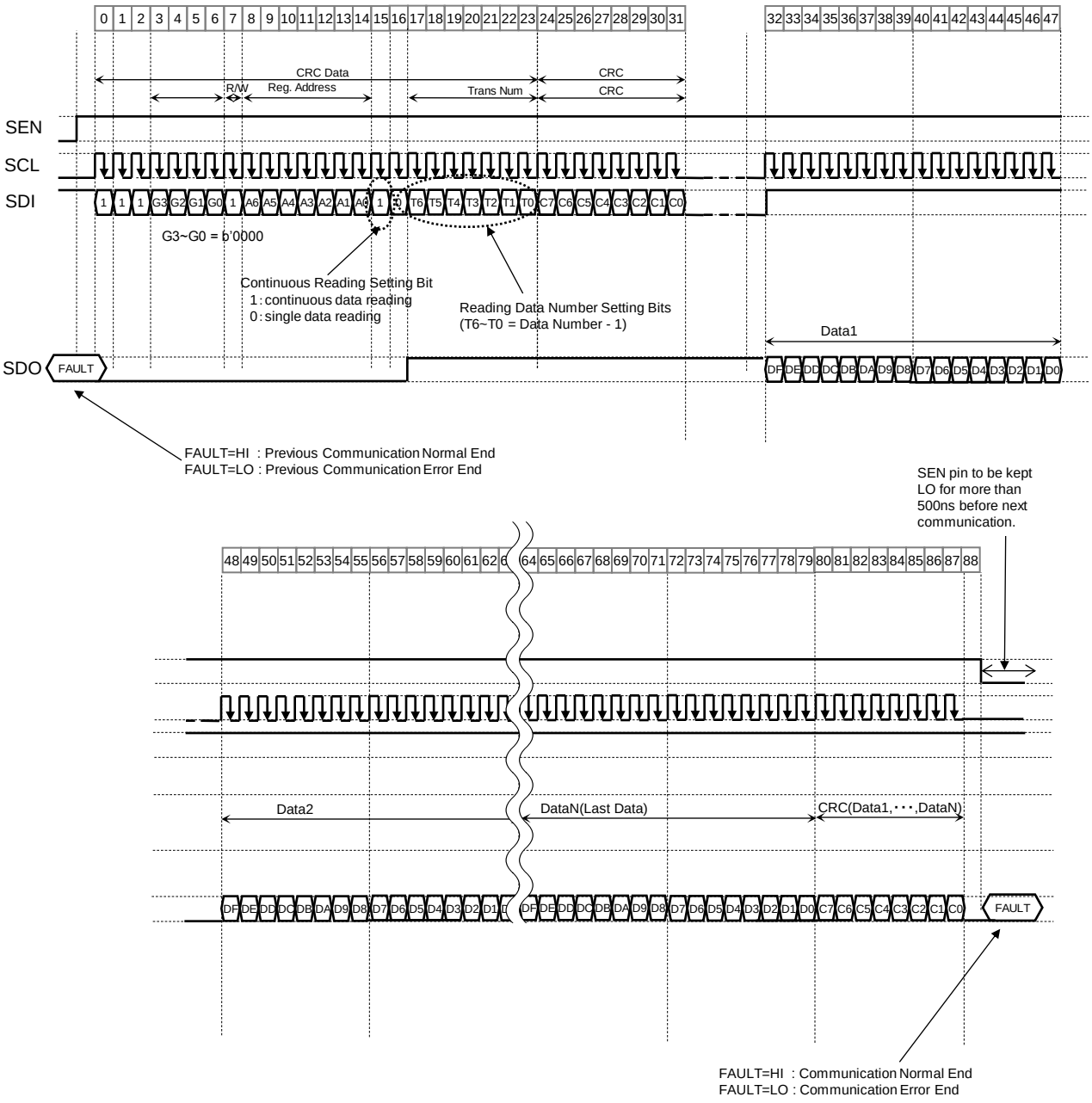


Functional Description

15.1 SPI Communication Interface

Data Communication Control Timing

＜Continuous Reading (2 Byte)＞



Functional Description

15.2 Communication Timing

Table below listed required time for communication at different operation

Communication	MCU - AN49503A Communication Time
Data Writing	$(1/f_{SCK} \times 40) + t_{SEN\_LD} + t_{SEN\_LG} + t_{SEN\_LO}$
Data Reading (Single Data)	$(1/f_{SCK} \times 48) + t_{SEN\_LD} + t_{SEN\_LG} + t_{SEN\_LO}$
Data Reading (Continuous Data)	$(1/f_{SCK} \times (40+(16 \times M))) + t_{SEN\_LD} + t_{SEN\_LG} + t_{SEN\_LO}$

M : continuous read data number
t_{senxx} : delay time for communication (refer to electrical characteristic)

15.3 Communication Error

During communication, SDO pin become LO when communication error occur. To find out the reason of the error, read the status register address 0x54 bit 14 SPI_F.

The table below list the cause of communication error.

Register Name	Description
SPI_F (0x54 bit 14)	CRC error during MCU– AN49503A communication

15.4 Watchdog Timer

AN49503A will shutdown when no communication between MCU and the IC is made in set duration by register *SPI_WDTCOUNT* and VPC is LO when watchdog timer is enabled by register COMTIMON = 1.

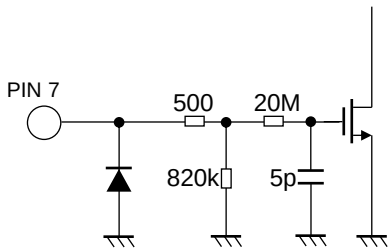
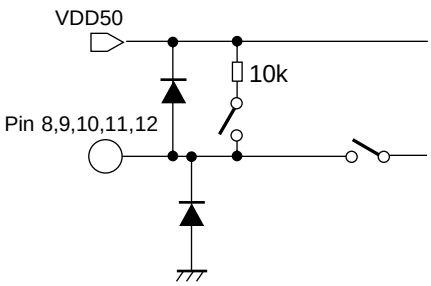
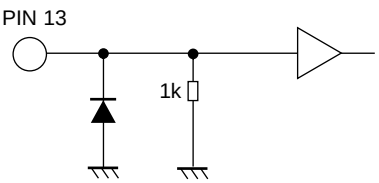
Address : 0x02

Bit	Register Name	Description
[12]	COMTIMON	Watchdog Timer ON/OFF Control 1 : ON (Default) 0 : OFF
[11:0]	SPI_WDTCOUNT[11:0]	Watchdog Timer Timing Setting Time = (value +1)x 1 s (range 1~4096s) [11:0] = 0x03B : 1 minute (Default)

Technical Information

Pin configuration diagram

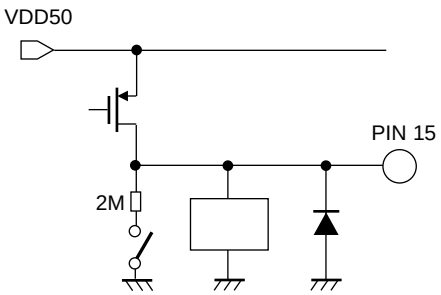
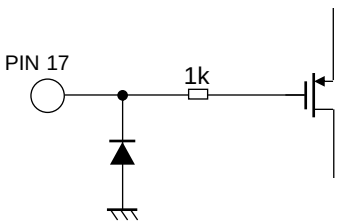
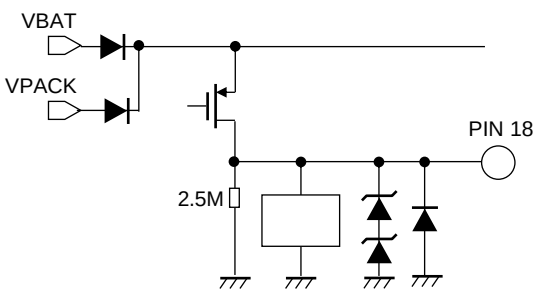
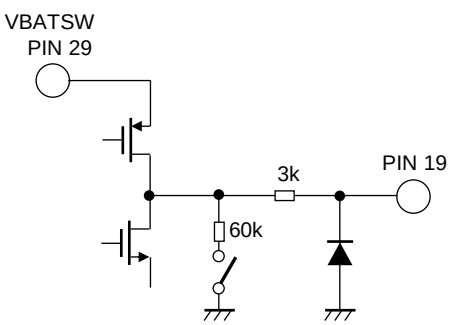
Note: The following information is design value for reference purpose, the value is not guaranteed by test.

Pin No.	Waveform / voltage	Internal Circuit	Description
6	DC		Digital IO Power Supply Pin (CVDD)
7	DC		Shutdown Control Signal Input Pin (SHDN)
8 9 10 11 12	DC		Analog Voltage Input Pin (TMONI1-5)
13	DC		Test Mode Setting Pin (MODE)

Technical Information

Pin configuration diagram

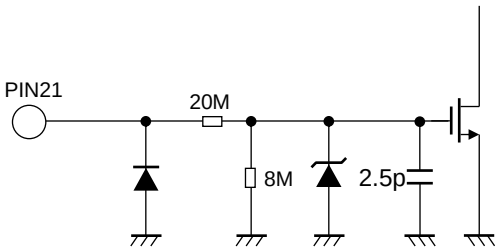
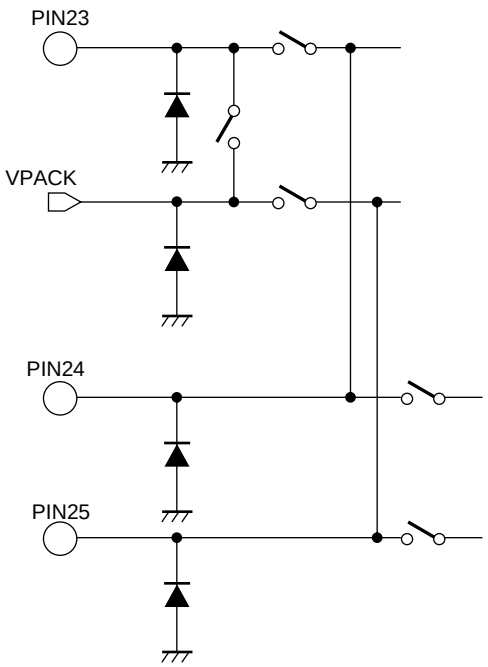
Note: The following information is design value for reference purpose, the value is not guaranteed by test.

Pin No.	Waveform / voltage	Internal Circuit	Description
15	DC		Internal Regulator Pin (VDD18)
17	DC		VDD50R
18	DC		5V Regulator Pin (VDD50)
19	DC		5V Regulator External NMOS Gate Pin (LDOG)

Technical Information

Pin configuration diagram

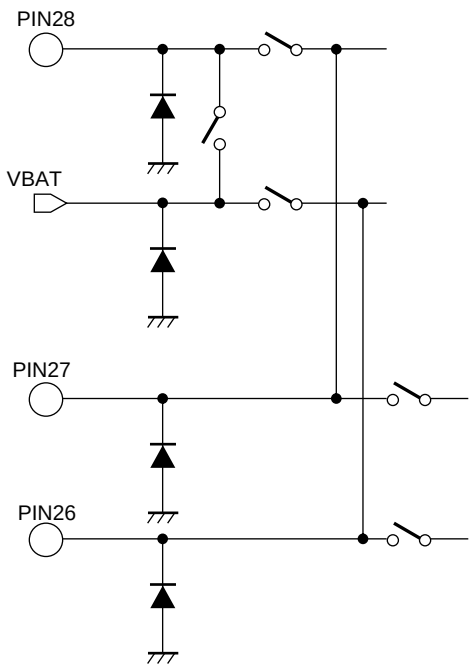
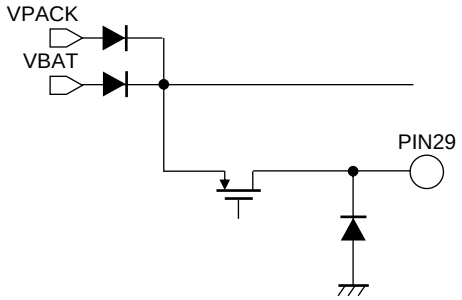
Note: The following information is design value for reference purpose, the value is not guaranteed by test.

Pin No.	Waveform / voltage	Internal Circuit	Description
21	DC		Wake Up Signal Pin (VPC)
23	AC		External DIS_FET (NMOS) Gate Driver Pin (DIS)
24	AC		Charge Pump Capacitor Pin (CP1)
25	AC		Charge Pump Capacitor Pin CN1

Technical Information

Pin configuration diagram

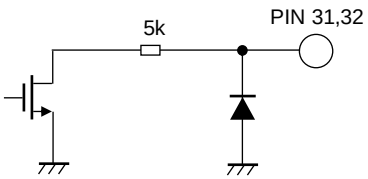
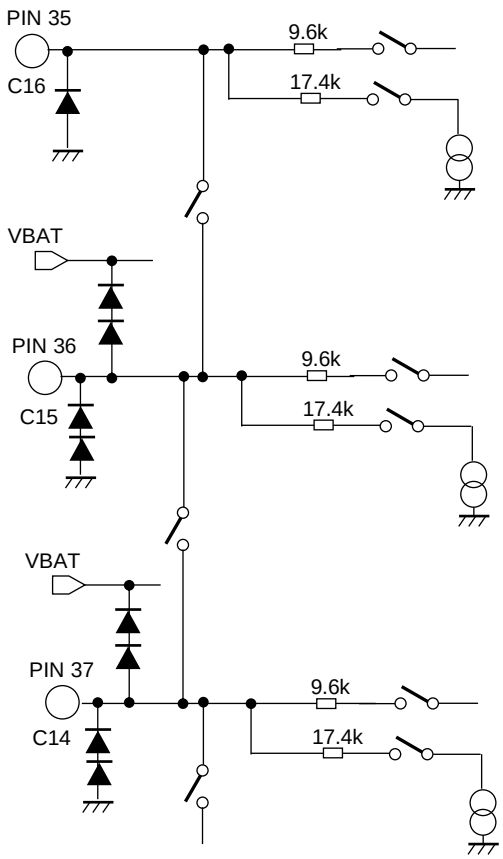
Note: The following information is design value for reference purpose, the value is not guaranteed by test.

Pin No.	Waveform / voltage	Internal Circuit	Description
26	AC		Charge Pump Capacitor Pin (CN2)
27	AC		Charge Pump Capacitor Pin (CP2)
28	AC		External CHG_FET (NMOS) Gate Driver Pin (CHG)
29	DC		5V Regulator External NMOS Drain Pin (VBATSW)

Technical Information

Pin configuration diagram

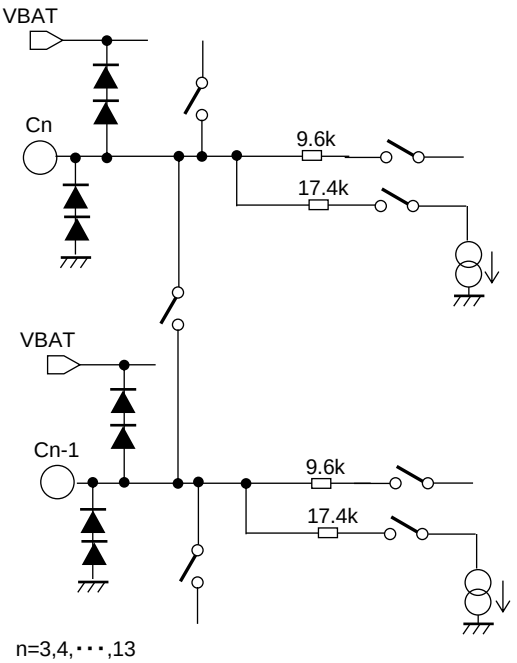
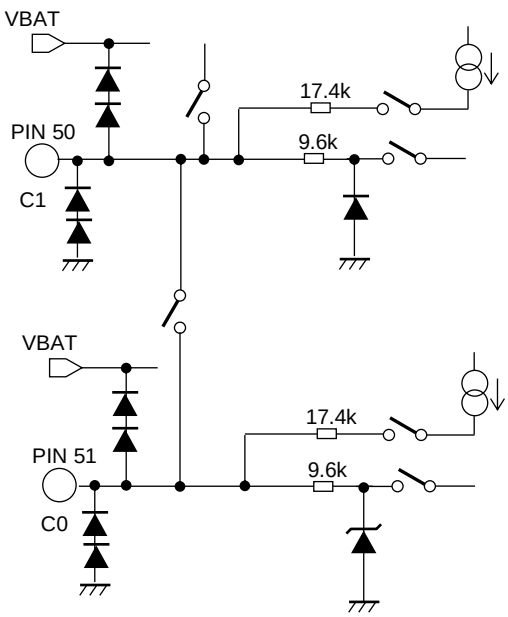
Note: The following information is design value for reference purpose, the value is not guaranteed by test.

Pin No.	Waveform / voltage	Internal Circuit	Description
31 32	DC		High Breakdown Voltage GPO Pin (GPOH2/GPOH1)
35	DC		Cell Voltage Input Pin (C16)
36	DC		Cell Voltage Input Pin (C15)
37	DC		Cell Voltage Input Pin (C14)

Technical Information

Pin configuration diagram

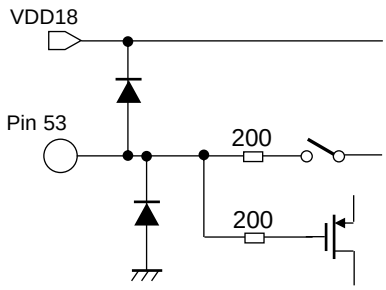
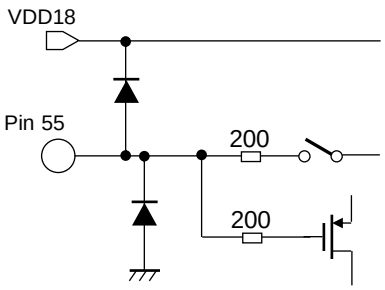
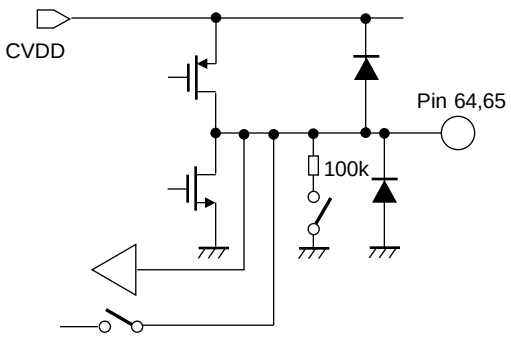
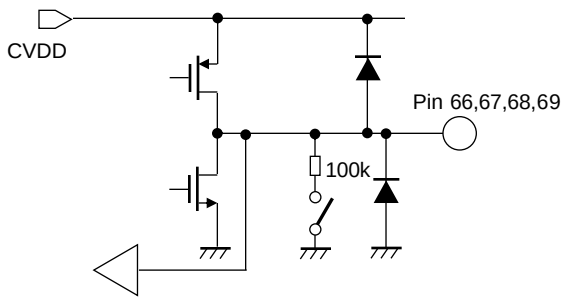
Note: The following information is design value for reference purpose, the value is not guaranteed by test.

Pin No.	Waveform / voltage	Internal Circuit	Description
38 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49	DC		Cell Voltage Input Pin (C13,C12,C11・・・C2)
50	DC		Cell Voltage Input Pin (C1)
51	DC		Cell Voltage Input Pin (C0)

Technical Information

Pin configuration diagram

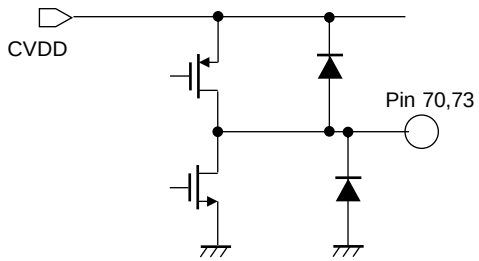
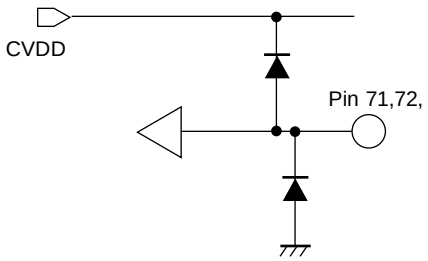
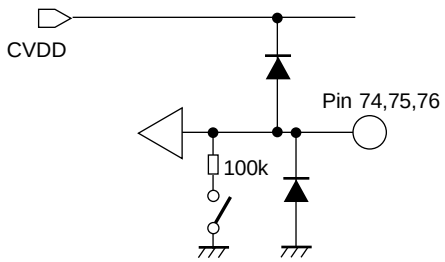
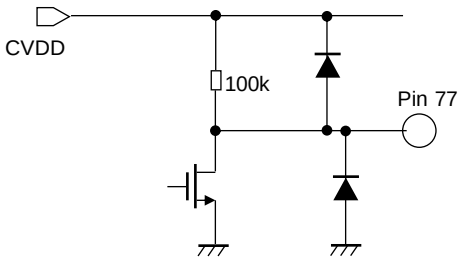
Note: The following information is design value for reference purpose, the value is not guaranteed by test.

Pin No.	Waveform / voltage	Internal Circuit	Description
53	DC		Shunt Current Monitor Pin (+ve) (SRP)
55	DC		Shunt Current Monitor Pin (−ve) (SRN)
64 65	DC		GPIO1/2 Pin (GPIO1/GPIO2)
66 67 68 69	DC		GPIO3/4/5/6 Pin (GPIO3−GPIO6)

Technical Information

Pin configuration diagram

Note: The following information is design value for reference purpose, the value is not guaranteed by test.

Pin No.	Waveform / voltage	Internal Circuit	Description
70 73	DC		Digital Output Pin (ALARM1,SDO)
71 72	DC		Digital Input Pin (FETOFF,STB)
74 75 76	DC		Digital Input Pin (SDI,SCL,SEN)
77	DC		Power ON Reset Output Pin (NRST)

Register Map

Register		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
PWRCTRL	bit name	-	-	-	-	-	-	STB_MONEN	ADC_CONT	MSET_SHDN	NPD_RST	-	-	NPD_FDRV	FDRV_LPWR	FDRV_CHG_FET	FDRV_DIS_FET
0X01	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W
Initial	0x0048	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0
SPIWD_CTRL	bit name	-	-	-	COMTIMON	SPI_WDTCOUNT											
0x02	R/W	R	R	R	R/WL	R/WL											
Initial	0x103B	0	0	0	1	0	0	0	0	0	0	1	1	1	0	1	1
FDRV_CTRL	bit name	FDRV_ALM_SD	FDRV_ALM_RCV	FDRV_ALM_CLR	-	<Reserved>	<Reserved>	<Reserved>	FDRV_STBY	-	-	-	FDRV_LEVEL[2:0]			<Reserved>	<Reserved>
0x03	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CVSEL	bit name	CV16SEL	CV15SEL	CV14SEL	CV13SEL	CV12SEL	CV11SEL	CV10SEL	CV9SEL	CV8SEL	CV7SEL	CV6SEL	CV5SEL	CV4SEL	CV3SEL	CV2SEL	CV1SEL
0x04	R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
Initial	0xFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
GVSEL	bit name	<Reserved>	<Reserved>	<Reserved>	<Reserved>	-	<Reserved>	<Reserved>	GPAD2SEL	GPAD1SEL	VDD50SEL	TMONI5SEL	TMONI4SEL	TMONI3SEL	TMONI2SEL	TMONI1SEL	VPACSEL
0x05	R/W	R/WL	R/WL	R/WL	R/WL	R	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
Initial	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
OUVCTL1	bit name	-	-	OVTH[5:0]						-	-	UVTH[5:0]					
0x06	R/W	R	R	R/WL						R	R	R/WL					
Initial	0x3E00	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
OUVCTL2	bit name	OVHLMT	OV_HYS[2:0]			-	UV_HYS[2:0]			-	-	OV_DLY[1:0]		-	-	UV_DLY[1:0]	
0x07	R/W	R/WL	R/WL			R	R/WL			R	R	R/WL		R	R	R/WL	
Initial	0x8000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
UVMSK	bit name	UVMSK16	UVMSK15	UVMSK14	UVMSK13	UVMSK12	UVMSK11	UVMSK10	UVMSK9	UVMSK8	UVMSK7	UVMSK6	UVMSK5	UVMSK4	UVMSK3	UVMSK2	UVMSK1
0x08	R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OVMSK15	bit name	OVMSK16	OVMSK15	OVMSK14	OVMSK13	OVMSK12	OVMSK11	OVMSK10	OVMSK9	OVMSK8	OVMSK7	OVMSK6	OVMSK5	OVMSK4	OVMSK3	OVMSK2	OVMSK1
0x09	R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OP_MODE	bit name	-	<Reserved>	-	-	-	-	<Reserved>	CB_SET	-	-	-	ADC_TRG	-	ADIL_LATCH	ADIH_LATCH	ADV_LATCH
0x0A	R/W	R	R/W	R	R	R	R	R/W	R/W	R	R	R	R/W	R	R/W	R/W	R/W
Initial	0x4000	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LOCK	bit name	LOCK_CONT[15:0]															
0x0B	R/W	R/W															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPIO_CTRL1	bit name	-	-	GPIO6_NOE	GPIO5_NOE	GPIO4_NOE	GPIO3_NOE	GPIO2_NOE	GPIO1_NOE	-	-	GPIO6_IE	GPIO5_IE	GPIO4_IE	GPIO3_IE	GPIO2_IE	GPIO1_IE
0x0C	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial	0x3F00	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
GPIO_CTRL2	bit name	-	-	GPIO6_OD	GPIO5_OD	GPIO4_OD	GPIO3_OD	GPIO2_OD	GPIO1_OD	-	-	GPIO6_PD	GPIO5_PD	GPIO4_PD	GPIO3_PD	GPIO2_PD	GPIO1_PD
0x0D	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPIO_CTRL3	bit name	-	-	ST_GPIO6	ST_GPIO5	ST_GPIO4	ST_GPIO3	ST_GPIO2	ST_GPIO1	-	-	GPIO6_OUT	GPIO5_OUT	GPIO4_OUT	GPIO3_OUT	GPIO2_OUT	GPIO1_OUT
0x0E	R/W	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPIO_CTRL4	bit name	-	-	-	PULLUP_SEL[5:1]					-	-	GPIO6_CHDRV	GPIO5_CHDRV	GPIO4_CHDRV	GPIO3_CHDRV	GPIO2_CHDRV	GPIO1_CHDRV
0x0F	R/W	R	R	R	R/W					R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ALARM_CTRL1	bit name	ALARMSEL	-	<Reserved>	<Reserved>	-	-	<Reserved>	<Reserved>	-	-	-	-	EN_SCD	EN_OCD	EN_OCC	EN_CP
0x11	R/W	R/WL	R	R/WL	R/WL	R	R	R/WL	R/WL	R	R	R	R	R/WL	R/WL	R/WL	R/WL
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note : 1. Register address not listed is reserved register, user shall not access these registers
2. There are three access category for register:
R : Readable
R/W : Readable and writable always
R/WL : Readable always and writable only when register LOCK [0x0B] = 0xE3B5

Register Map

Register		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ALARM_CTRL2	bit name	-	-	SCD_D[3:0]				OCD_D[4:0]						OCC_D[4:0]			
0x12	R/W	R	R	R/WL				R/WL						R/WL			
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ALARM_CTRL3	bit name	-	SCD_DLY[4:0]					-	OCD_DLY[3:0]				-	OCC_DLY[3:0]			
0x13	R/W	R	R/WL					R	R/WL				R	R/WL			
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CB_CTL	bit name	-	-	-	-	-	-	-	-	-	-	-	CB_PROTECT	-	-	<Reserved>	CB_PD
0x14	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W
Initial	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
CBSEL	bit name	DI_CBSEL[16:1]															
0x15	R/W	R/WL															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPIOSEL	bit name	-	-	OSC2_DIV[1:0]		GPIO6SEL[1:0]		GPIO5SEL[1:0]		GPIO4SEL[1:0]		GPIO3SEL[1:0]		GPIO2SEL[1:0]		GPIO1SEL[1:0]	
0x17	R/W	R	R	R/WL		R/WL		R/WL		R/WL		R/WL		R/WL		R/WL	
Initial	0x0000	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
SPICTL	bit name	-	-	<Reserved>	<Reserved>	-	SDI_PLDW	SCL_PLDW	SEN_PLDW	-	-	<Reserved>	LP50EN	-	-	-	COM_STP
0x18	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R/W
Initial	0x0700	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
ADCTRL1	bit name	<Reserved>	<Reserved>	<Reserved>		<Reserved>		-	-	<Reserved>	<Reserved>	ADI_LATCH_SET	ADV_LATCH_SET	-	<Reserved>	<Reserved>	<Reserved>
0x19	R/W	R/WL	R/WL	R/WL		R/WL		R	R	R/WL	R/WL	R/WL	R/WL	R	R/WL	R/WL	R/WL
Initial	0x0C87	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0
ADCTRL2	bit name	-	-	ADSWHY_EN	ADSWSD_EN	-	-	-	-	<Reserved>	<Reserved>	<Reserved>	ISD_STOPEN	-	-	ADIL_ON	ADIH_ON
0x1A	R/W	R	R	R/WL	R/WL	R	R	R	R	R/WL	R/WL	R/WL	R/WL	R	R	R/WL	R/WL
Initial	0x0030	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
GPOH_CTRL	bit name	-	-	-	-	-	-	-	-	-	-	GPOH2_ALM_ST	GPOH1_ALM_ST	-	GPOH_FET	GPOH2_EN	GPOH1_EN
0x1B	R/W	R	R	R	R	R	R	R	R	R	R	R/WL	R/WL	R	R/WL	R/WL	R/WL
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INRCV1	bit name	INR_CV[15:0]															
0x1C	R/W	R/WL															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INRCV2	bit name	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	INR_CV_16
0x1D	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/WL
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INR_CTL	bit name	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	INR_EN
0x1E	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/WL
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPI_STAT	bit name	-	SPI_F	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0x21	R/W	R	R/WL	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MODE_STAT	bit name	-	-	-	-	-	-	-	-	-	-	COND_SCD	COND_OCD	COND_OCC	ST_SDWN	ST_STBY	ST_ACT
0x22	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial	0x000x	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x
FUSE_RADR	bit name	-	-	-	-	-	-	-	-	FUSE_RADR[7:0]							
0x2E	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FUSE_DATA	bit name	FUSE_DATA[15:0]															
0x2F	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial	0xxxxx	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Note : 1. Register address not listed is reserved register, user shall not access these registers
2. There are three access category for register:
R : Readable
R/W : Readable and writable always
R/WL : Readable always and writable only when register LOCK [0x0B] = 0xE3B5

Register Map

Register		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
STAT	bit name	-	-	-	-	-	-	ST_OV	ST_UV	-	ST_SCD	ST_OCD	ST_OCC	-	IADS_DONE	IADH_DONE	VAD_DONE
0x30	R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OVSTAT	bit name	OV16_F	OV15_F	OV14_F	OV13_F	OV12_F	OV11_F	OV10_F	OV9_F	OV8_F	OV7_F	OV6_F	OV5_F	OV4_F	OV3_F	OV2_F	OV1_F
0x31	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
UVSTAT	bit name	UV16_F	UV15_F	UV14_F	UV13_F	UV12_F	UV11_F	UV10_F	UV9_F	UV8_F	UV7_F	UV6_F	UV5_F	UV4_F	UV3_F	UV2_F	UV1_F
0x32	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CV[n]_AD	bit name	CV01_AD[15:0] ~ CV16_AD[15:0]															
0x33~0x42	R/W	R															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VPAC_AD	bit name	VPAC_AD[15:0]															
0x43	R/W	R															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TMONI[n]_AD	bit name	TMONI1_AD[15:0] ~ TMONI5_AD[15:0]															
0x44~0x48	R/W	R															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VDD50_AD	bit name	VDD50_AD[15:0]															
0x49	R/W	R															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPIO1_AD	bit name	GPIO1_AD[15:0]															
0x4A	R/W	R															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPIO2_AD	bit name	GPIO2_AD[15:0]															
0x4B	R/W	R															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CVIH_AD	bit name	CVIH_AD[15:0]															
0x4C	R/W	R															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CHIL_AD	bit name	CVIL_AD[15:0]															
0x4D	R/W	R															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OVL_STAT	bit name	OV16_LF	OV15_LF	OV14_LF	OV13_LF	OV12_LF	OV11_LF	OV10_LF	OV9_LF	OV8_LF	OV7_LF	OV6_LF	OV5_LF	OV4_LF	OV3_LF	OV2_LF	OV1_LF
0x52	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
UVL_STAT	bit name	UV16_LF	UV15_LF	UV14_LF	UV13_LF	UV12_LF	UV11_LF	UV10_LF	UV9_LF	UV8_LF	UV7_LF	UV6_LF	UV5_LF	UV4_LF	UV3_LF	UV2_LF	UV1_LF
0x53	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FAILSTAT	bit name	-	-	-	-	-	-	-	-	-	-	-	-	-	VO_POUVC_OUT	-	VDD50_OVP
0x54	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial	0x0xx0	0	0	0	0	0	0	X	X	0	0	0	X	0	0	0	0
FDRVST	bit name	-	-	-	-	-	-	-	-	-	-	-	-	FDRV_DIS_ST	FDRV_DHG_ST	GPOH2_ST	GPOH1_ST
0x55	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CBSTAT	bit name	CB_ST[16:1]															
0x56	R/W	R															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note : 1. Register address not listed is reserved register, user shall not access these registers

2. There are three access category for register:

R : Readable

R/W : Readable and writable always

R/WL : Readable always and writable only when register LOCK [0x0B] = 0xE3B5

1. Summary of Registers

The addresses of this IC which consist of 16 bits are shown in the summary table below.
The detail description of each register is shown in the following pages.

Note) Please take note that IC operation might be affected when writing other than the initial values into the Reserved Register.

Address	Register Name	Register Summary
0x00	<Reserved>	
0x01	PWR_CTRL	Mode of Operation・FET Driver Operation Control
0x02	SPIWD_CTRL	SPI watchdog timer control
0x03	FDRV_CTRL	FET Driver Setting
0x04	CVSEL	Respective cell voltage measurement ON/OFF setting
0x05	GVSEL	Other voltage measurement ON/OFF setting
0x06	OUVCTL1	OV/UV setting 1
0x07	OUVCTL2	OV/UV setting 2
0x08	UVMSK	UV detection setting
0x09	OVMSK	OV detection setting
0x0A	OP_MODE	ADC Operation
0x0B	LOCK	Unlock code setting for accessing specific register
0x0C	GPIO_CTRL1	GPIO control 1
0x0D	GPIO_CTRL2	GPIO control 2
0x0E	GPIO_CTRL3	GPIO control 3
0x0F	GPIO_CTRL4	GPIO control 4
0x10	<Reserved>	
0x11	ALARM_CTRL1	Alarm Control 1
0x12	ALARM_CTRL2	Alarm Control 2
0x13	ALARM_CTRL3	Alarm Control 3
0x14	CB_CTL	Cell Balance Control
0x15	CBSEL	Cell selection for cell balance
0x16	<Reserved>	
0x17	GPIOSEL	GPIO output control
0x18	SPICTL	SPI control
0x19	ADCTRL1	ADC control・Shutdown setting
0x1A	ADCTRL2	ADC control
0x1B	GPOH_CTRL	GPOH control
0x1C	INRCV1	Line selection 1 for Disconnection detection
0x1D	INRCV2	Line selection 2 for Disconnection detection
0x1E	INR_CTL	Disconnection detection ON/OFF
0x1F～0x20	<Reserved>	
0x21	SPI_STAT	SPI Status
0x22	MODE_STAT	Operation Mode Status
0x23～0x2D	<Reserved>	
0x2E	FUSE_RADR	Address setting for FUSE Read address setting
0x2F	FUSE_DATA	FUSE read data

Address	Register Name	Register Summary
0x30	STAT	ADC/ALARM Status
0x31	OVSTAT	OV Status
0x32	UVSTAT	UV Status
0x33	CV01_AD	Voltage measurement result for cell 1
0x34	CV02_AD	Voltage measurement result for cell 2
0x35	CV03_AD	Voltage measurement result for cell 3
0x36	CV04_AD	Voltage measurement result for cell 4
0x37	CV05_AD	Voltage measurement result for cell 5
0x38	CV06_AD	Voltage measurement result for cell 6
0x39	CV07_AD	Voltage measurement result for cell 7
0x3A	CV08_AD	Voltage measurement result for cell 8
0x3B	CV09_AD	Voltage measurement result for cell 9
0x3C	CV10_AD	Voltage measurement result for cell 10
0x3D	CV11_AD	Voltage measurement result for cell 11
0x3E	CV12_AD	Voltage measurement result for cell 12
0x3F	CV13_AD	Voltage measurement result for cell 13
0x40	CV14_AD	Voltage measurement result for cell 14
0x41	CV15_AD	Voltage measurement result for cell 15
0x42	CV16_AD	Voltage measurement result for cell 16
0x43	VPAC_AD	Voltage measurement result for VPACK
0x44	TMONI1_AD	Voltage measurement result for TMONI1
0x45	TMONI2_AD	Voltage measurement result for TMONI2
0x46	TMONI3_AD	Voltage measurement result for TMONI3
0x47	TMONI4_AD	Voltage measurement result for TMONI4
0x48	TMONI5_AD	Voltage measurement result for TMONI5
0x49	VDD50_AD	Voltage measurement result for VDD50
0x4A	GPIO1_AD	Voltage measurement result for GPIO1
0x4B	GPIO2_AD	Voltage measurement result for GPIO2
0x4C	CVIH_AD	High speed current ADC measurement result
0x4D	CVIL_AD	Low speed current ADC measurement result
0x4E～0x51	<Reserved>	
0x52	OVL_STAT	OV detection flag
0x53	UVL_STAT	UV detection flag
0x54	FAILSTAT	FAIL status
0x55	FDRVSTAT	FET Driver status
0x56	CBSTAT	Cell balance operation status
0x57～0x7F	<Reserved>	

2. Register Detail Explanation

*The registers in this map are categorized into 3 types as shown below.

R : Read only
R/W : Read or write
R/WL : Read or write only when LOCK register [0x0B] = 0xE3B5

Address:0x01 PWR_CTRL

bit	15	14	13	12	11	10	9	8
bit name	-	-	-	-	-	-	STB_MONEN	ADC_CONT
R/W	R	R	R	R	R	R	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	MSET_SHDN	NPD_RST	-	-	NPD_FDRV	FDRV_LPWR	FDRV_CHG_FET	FDRV_DIS_FET
R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W
initial	0	1	0	0	1	0	0	0

bit	bit name	explanation
15-10	-	
9	STB_MONEN	Enable for Standby Mode Monitoring/Measurement 0:No Voltage Monitoring/Measurement in Standby Mode 1:During Standby Mode, when no SPI communication occurs for more than 1s, it is automatically switched to Active Mode and performs voltage measurement. Subsequently, it resumes to standby mode after measurement, please refer to specification in section 2. ※ Please set to 0 whenever the ADC_CONT = 0
8	ADC_CONT	ADC Operation Setting 0:Voltage and HS Current Measurement are performed only when register (0x0a) ADC_TRG = 1 1:Voltage and HS current measurement is performed during Active Mode. Once this bit is set, cell measurement is repeated after completing measurement.
7	MSET_SHDN	Shutdown Control 0:Normal operation 1:Shutdown Mode, only function when VPC is LO.
6	NPD_RST	Soft Reset 0: Reset 1: Normal operation Auto recovery to “1” after "0“ is written.
5-4	-	
3	NPD_FDRV	High Side (CHG/DIS) NMOSFET Power Down 1 : Normal 0 : Power Down
2	FDRV_LPWR	High Side (CHG/DIS) NMOSFET Power Mode 1 : Low Power Mode 0 : Normal
1	FDRV_CHG_FET	High Side (CHG) NMOSFET ON/OFF 1 : FET ON 0 : FET OFF
0	FDRV_DIS_FET	High Side (DIS) NMOSFET ON/OFF 1 : FET ON 0 : FET OFF

Address: 0x02 SPIWD_CTRL

bit	15	14	13	12	11	10	9	8
bit name	-	-	-	COMTIMON	SPI_WDTCOUNT[11:8]			
R/W	R	R	R	R/WL	R/WL			
initial	0	0	0	1	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	SPI_WDTCOUNT[7:0]							
R/W	R/WL							
initial	0	0	1	1	1	0	1	1

bit	bit name	explanation
15-13	-	
12	COMTIMON	Watchdog Timer ON/OFF Control 1 : ON (Default) 0 : OFF
11-0	SPI_ WDTCOUNT [11:0]	Watchdog Timer Timing Setting Time = (value +1) x 1 s (range 1~4096s) [11:0] = 0x03B : 60s (Default)

Address: 0x03 FDRV_CTRL

bit	15	14	13	12	11	10	9	8
bit name	FDRV_ALM_ SD	FDRV_ALM_ RCV	FDRV_ALM_ CLR	-	<Reserved>	<Reserved>	<Reserved>	FDRV_STBY
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	-	-	-	FDRV_LEVEL[2:0]			<Reserved>	<Reserved>
R/W	R	R	R	R/W			R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15	FDRV_ALM_ SD	CHG/DIS FET and GPOH pins response to ALARM condition 1 : CHG/DIS FET auto OFF and GPOH become value set, refer to specification section 10 CHG FET OFF : OV/UV/OCC DIS FET OFF : OV/UV/OCD/SCD) 0 : CHG/DIS FET and GPOH no response to ALARM condition
14	FDRV_ALM_ RCV	CHG/DIS FET and GPOH pins recover when ALARM(OV/UV) condition removed (when FDRV_ALM_SD = 1) with the following setting. 1 : Depend on FDRV_ALM_CLR 0: Recover when ALARM(OV/UV) condition is removed.
13	FDRV_ALM_ CLR	CHG/DIS FET and GPOH pins recover when ALARM(OV/UV/OCD/OCC/SCD) condition removed (when FDRV_ALM_SD = 1 & FDRV_ALM_RCV=1) 1 : CHG/DIS FET and GPOH pins recover 0 : No change * This bit is not cleared automatically. * If ALARM condition continue and this bit is set, CHS/DIS FET remains OFF.
12	-	
11-9	<Reserved>	Please always set to “0”.
8	FDRV_STBY	FET Driver Standby Control 1 : Standby 0 : Normal This bit will be cleared automatically and FET driver will be operated in Normal Mode when ALARM occur or when FETOFF = 1.
7-5	-	
4-2	FDRV_ LEVEL [2:0]	Setting of External FET drive voltage 111 : -7V 011 : -3V 110 : -6V 010 : -2V 101 : -5V 001 : -1V 100 : -4V 000 : 0V
1-0	<Reserved>	Please always set to “0”.

Address: 0x04 CVSEL

bit	15	14	13	12	11	10	9	8
bit name	CV16SEL	CV15SEL	CV14SEL	CV13SEL	CV12SEL	CV11SEL	CV10SEL	CV9SEL
R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
initial	1	1	1	1	1	1	1	1

bit	7	6	5	4	3	2	1	0
bit name	CV8SEL	CV7SEL	CV6SEL	CV5SEL	CV4SEL	CV3SEL	CV2SEL	CV1SEL
R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
initial	1	1	1	1	1	1	1	1

bit	bit name	explanation
15	CV16SEL	Select respective cell (from Cell 1 to Cell 16) voltage measurement ON/OFF 1 : Measurement ON (Default) 0 : Measurement OFF * Cell Voltage ADC measured data with these bits set to 1 will be latched to respective data registers when ADV_LATCH = 1.
14	CV15SEL	
13	CV14SEL	
12	CV13SEL	
11	CV12SEL	
10	CV11SEL	
9	CV10SEL	
8	CV9SEL	
7	CV8SEL	
6	CV7SEL	
5	CV6SEL	
4	CV5SEL	
3	CV4SEL	
2	CV3SEL	
1	CV2SEL	
0	CV1SEL	

Address: 0x05 GVSEL

bit	15	14	13	12	11	10	9	8
bit name	<Reserved>	<Reserved>	<Reserved>	<Reserved>	-	<Reserved>	<Reserved>	GPAD2SEL
R/W	R/WL	R/WL	R/WL	R/WL	R	R/WL	R/WL	R/WL
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	GPAD1SEL	VDD50SEL	TMONI5SEL	TMONI4SEL	TMONI3SEL	TMONI2SEL	TMONI1SEL	VPACSEL
R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
initial	0	0	0	0	0	0	0	1

bit	bit name	explanation
15-12	<Reserved>	Please always set to “0”.
11	-	
10	<Reserved>	Please always set to “0”.
9	<Reserved>	Please always set to “0”.
8	GPAD2SEL	GPIO2 Pin Voltage Measurement ON/OFF (when set to analog input) 1 : Measurement ON 0 : Measurement OFF (Default) * Set in advance GPIO2_NOE = 1, GPIO2_IEN = 0 when GPAD2SEL = 1 for analog input.
7	GPAD1SEL	GPIO1 Pin Voltage Measurement ON/OFF (when set to analog input) 1 : Measurement ON 0 : Measurement OFF (Default) * Set GPIO1_NOE = 1, GPIO1_IEN = 0 when GPAD1SEL = 1 for analog input
6	VDD50SEL	VDD50 Voltage Measurement ON/OFF 1 : Measurement ON 0 : Measurement OFF (Default)
5	TMONI5SEL	TMONI1 to TMONI5 Voltage Measurement ON/OFF 1 : Measurement ON 0 : Measurement OFF (Default)
4	TMONI4SEL	
3	TMONI3SEL	
2	TMONI2SEL	
1	TMONI1SEL	
0	VPACSEL	VPACK Voltage Measurement ON/OFF 1 : Measurement ON (Default) 0 : Measurement OFF

Note: Voltage ADC measured data with bit 0~8 set to 1 will be latched to respective data registers when ADV_LATCH = 1.

Address: 0x06 OUVCTRL1

bit	15	14	13	12	11	10	9	8
bit name	-	-	OVTH[5:0]					
R/W	R	R	R/WL					
initial	0	0	1	1	0	1	0	0

bit	7	6	5	4	3	2	1	0
bit name	-	-	UVTH[5:0]					
R/W	R	R	R/WL					
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-14	-	
13-8	OVTH[5:0]	Over-Voltage Detection Threshold 110100 : 4.50V ～ 100000 : 3.50V ～ 000010 : 2.00V 111111～110101 (remains at 4.5V) 000001,000000 : prohibited * OVTH[5] = 1 when OVHLMT= 1

bit	bit name	explanation
7-6	-	
5-0	UVTH[5:0]	Under-Voltage Detection Threshold 110010 : 3.00V ～ 000000 : 0.50V 111111～110011 : prohibited

Address: 0x07 OUVCTRL2

bit	15	14	13	12	11	10	9	8
bit name	OVHLMT	OV_HYS[2:0]			-	UV_HYS[2:0]		
R/W	R/WL	R/WL			R	R/WL		
initial	1	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	-	-	OV_DLY[1:0]		-	-	UV_DLY[1:0]	
R/W	R	R	R/WL		R	R	R/WL	
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15	OVHLMT	OV Detection Threshold Lower Limit Control 0 : Lower Threshold (Threshold < = 3.5V) 1 : Limit at 3.5V (Lower threshold = 3.5V)(Default)
14-12	OV_HYS [2:0]	OV Detection Hysteresis Level 000 : 100mV(Default) 001 : 150mV 010 : 200mV 011 : 250mV 100 : 300mV 101 : 350mV 110 : 400mV 111 : 450mV
11	-	
10-8	UV_HYS [2:0]	UV Detection Hysteresis Level 000 : 100mV(Default) 001 : 150mV 010 : 200mV 011 : 250mV 100 : 300mV 101 : 350mV 110 : 400mV 111 : 450mV

bit	bit name	explanation
7-6	-	
5-4	OV_DLY [1:0]	OV ALARM Delay Time Delay Time = (OV_DLY+1)s
3-2	-	
1-0	UV_DLY [1:0]	UV ALARM Delay Time Delay Time=(UV_DLY+1)s

Address: 0x08 UVMSK

bit	15	14	13	12	11	10	9	8
bit name	UVMSK16	UVMSK15	UVMSK14	UVMSK13	UVMSK12	UVMSK11	UVMSK10	UVMSK9
R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	UVMSK8	UVMSK7	UVMSK6	UVMSK5	UVMSK4	UVMSK3	UVMSK2	UVMSK1
R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15 to 0	UVMSK 16 to 1	Cell Voltage Under-Voltage Detection ON/OFF (Cell16 to Cell 1) 1 : UV OFF 0 : UV ON (Default)

Address: 0x09 OVMSK

bit	15	14	13	12	11	10	9	8
bit name	OVMSK16	OVMSK15	OVMSK14	OVMSK13	OVMSK12	OVMSK11	OVMSK10	OVMSK9
R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	OVMSK8	OVMSK7	OVMSK6	OVMSK5	OVMSK4	OVMSK3	OVMSK2	OVMSK1
R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15 to 0	OVMSK 16 to 1	Cell Voltage Overvoltage Detection ON/OFF (Cell 16 to Cell 1) 1 : OV OFF 0 : OV ON (Default)

Address: 0x0A OP_MODE

bit	15	14	13	12	11	10	9	8
bit name	-	<Reserved>	-	-	-	-	<Reserved>	CB_SET
R/W	R	R/W	R	R	R	R	R/W	R/W
initial	0	1	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	-	-	-	ADC_TRG	-	ADIL_LATCH	ADIH_LATCH	ADV_LATCH
R/W	R	R	R	R/W	R	R/W	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15	-	
14	<Reserved>	Please always set to “0”.
13-10	-	
9	<Reserved>	Please always set to “0”.
8	CB_SET	Cell Balance Operation Enable 1 : Cell Balance ON 0 : Cell Balance OFF (Default)
7-5	-	
4	ADC_TRG	Manual ADC Measurement Trigger 1 : Voltage ADC Measurement Start, when ADC_CONT = 0 (Auto returns to 0 after completion) 0 : When ADC_CONT = 1, always set this bit = 0.
3	-	
2	ADIL_LATCH	Low Speed Current ADC Measurement Result Latch 1 : Measured result latched to register 0x4D (Auto returns to 0 after data latch completed) 0 : No effect
1	ADIH_LATCH	High Speed Current ADC Measurement Result Latch 1 : Measured result latched to register 0x4C (auto return to 0 after data latch completed) 0 : No effect
0	ADV_LATCH	Voltage ADC Measurement Result Latch 1 : Measured result latched to register 0x33~0x4B (auto return to 0 after data latch completed) 0 : No effect

Address: 0x0B LOCK

bit	15	14	13	12	11	10	9	8
bit name	LOCK_CONT[15:8]							
R/W	R/W							
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	LOCK_CONT[7:0]							
R/W	R/W							
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-0	LOCK_CONT [15:0]	Setting to unlock the access to specified registers (refer each register for details) Writing to write protect register (R/WL) is possible when 0xe3b5 is written to this register.

Address:0x0C GPIO_CTRL1

bit	15	14	13	12	11	10	9	8
bit name	-	-	GPIO6_NOE	GPIO5_NOE	GPIO4_NOE	GPIO3_NOE	GPIO2_NOE	GPIO1_NOE
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
initial	0	0	1	1	1	1	1	1

bit	7	6	5	4	3	2	1	0
bit name	-	-	GPIO6_IE	GPIO5_IE	GPIO4_IE	GPIO3_IE	GPIO2_IE	GPIO1_IE
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-14	-	
13 to 8	GPIO6_NOE to GPIO1_NOE	GPIO6 to GPIO1 Pin Output Enable 1 : Disabled （Default） 0 : Enabled
7-6	-	
5 to 0	GPIO6_IE to GPIO1_IE	GPIO6 to GPIO1 Pin Input Enable 1 : Enabled 0 : Disable （Default）

Address:0x0D GPIO_CTRL2

bit	15	14	13	12	11	10	9	8
bit name	-	-	GPIO6_OD	GPIO5_OD	GPIO4_OD	GPIO3_OD	GPIO2_OD	GPIO1_OD
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	-	-	GPIO6_PD	GPIO5_PD	GPIO4_PD	GPIO3_PD	GPIO2_PD	GPIO1_PD
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-14	-	
13 to 8	GPIO6_OD to GPIO1_OD	GPIO6 to GPIO1 Pin Output Configuration 1 : Nch Open Drain 0 : Push Pull (Default)
7-6	-	
5 to 4	GPIO6_PD to GPIO1_PD	GPIO6 to GPIO1 Pin Pull-Down Resistor 1 : Yes (with pull-down resistor) 0 : No (without pull-down resistor)（Default）

Address:0x0E GPIO_CTRL3

bit	15	14	13	12	11	10	9	8
bit name	-	-	ST_GPIO6	ST_GPIO5	ST_GPIO4	ST_GPIO3	ST_GPIO2	ST_GPIO1
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	-	-	GPIO6_OUT	GPIO5_OUT	GPIO4_OUT	GPIO3_OUT	GPIO2_OUT	GPIO1_OUT
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-14	-	
13 to 8	ST_GPIO6 to ST_GPIO1	GPIO6 to GPIO1 pins input (Only effective when GPIO6_IE to GPIO1_IE = 1) 1: Input = 1 0: Input = 0
7-6	-	
5 to 0	GPIO6_OUT to GPIO1_OUT	GPIO6 to GPIO1 pins digital output data GPIO6_OD to GPIO1_OD = 0 (push pull) 1 : Output =1 0 : Output = 0 (Default) GPIO6_OD to GPIO1_OD = 1 (open drain) 1 : Output = HiZ 0 : Output =0 (Default)

Address:0x0F GPIO_CTRL4

bit	15	14	13	12	11	10	9	8
bit name	-	-	-	PULLUP_SEL[5:1]				
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	-	-	GPIO6_ CHDRV	GPIO5_ CHDRV	GPIO4_ CHDRV	GPIO3_ CHDRV	GPIO2_ CHDRV	GPIO1_ CHDRV
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-13	-	
12-8	PULLUP_ SEL [5:1]	Pull up setting for TMONI1 to TMONI5 pin [5] : For TMONI5 1 : with pull up 0 : without pull up (default) [4] : For TMONI4 1 : with pull up 0 : without pull up (default) [3] : For TMONI3 1 : with pull up 0 : without pull up (default) [2] : For TMONI2 1 : with pull up 0 : without pull up (default) [1] : For TMONI1 1 : with pull up 0 : without pull up (default)
7-6	-	
5 to 0	GPIO6_ CHDRV to GPIO1_ CHDRV	GPIO6 to GPIO1 Pins Output Drivability 1 : 4mA 0 : 2mA (Default)

Address:0x11 ALARM_CTRL

bit	15	14	13	12	11	10	9	8
bit name	ALARMSEL	–	<Reserved>	<Reserved>	–	–	<Reserved>	<Reserved>
R/W	R/WL	R	R/WL	R/WL	R	R	R/WL	R/WL
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	–	–	–	–	EN_SCD	EN_OCD	EN_OCC	EN_CP
R/W	R	R	R	R	R/WL	R/WL	R/WL	R/WL
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15	ALARMSEL	ALARM1 pin setting 0: ALARM for OV/UV/OCD/OCC/SCD 1: ALARM for SCD (ALARM2/GPIO6 will be used for OV/UV/OCD/OCC ALARM when GPIO6 set as ALARM2 Output)
14	-	
13-12	<Reserved>	Please always set to “0”
11-10	-	
9-8	<Reserved>	Please always set to “0”
7-4	-	
3	EN_SCD	Short circuit detection at discharge 1 : Enable 0 : Disable (Default)
2	EN_OCD	Overcurrent detection at discharge 1 : Enable 0 : Disable (Default)
1	EN_OCC	Overcurrent detection at charge 1 : Enable 0 : Disable (Default)
0	EN_CP	Current Protection 1 : Enable 0 : Disable (Default)

Note: Bits 3 to 0 are required to be set to 1 depending on OCD/OCC/SCD is required.

Address: 0x12 ALARM_CTRL2

bit	15	14	13	12	11	10	9	8
bit name	-	-	SCD_D[3:0]				OCD_D[4:3]	
R/W	R	R	R/WL				R/WL	
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	OCD_D[2:0]			OCC_D[4:0]				
R/W	R/WL			R/WL				
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-14	-	
13-10	SCD_D[3:0]	Short circuit detection at discharge threshold (SCD_D[3:0] + 1) x 50mV 0000 : 50mV (Default)
9-5	OCD_D[4:0]	Overcurrent detection at discharge threshold (OCD_D[4:0] + 1) x 25mV 00000 : 25mV (Default)
4-0	OCC_D[4:0]	Overcurrent detection at charge threshold (OCC_D[4:0] + 1) x 10mV (maximum 200mV) 00000 : 10mV (Default) 10011~11111 : 200mV

Address: 0x13 ALARM_CTRL3

bit	15	14	13	12	11	10	9	8
bit name	-	SCD_DLY[4:0]					-	OCD_DLY[3]
R/W	R	R/WL					R	R/WL
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	OCD_DLY[2:0]			-	OCC_DLY[3:0]			
R/W	R/WL			R	R/WL			
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15	-	
14-10	SCD_DLY [4:0]	Delay time for Short circuit detection at discharge (SCD_DLY[4:0] + 1) x 50us. If alarm condition continues after delay time, ALARM will be turned ON. 00000 : 50us (Default)
9	-	
8-5	OCD_DLY [3:0]	Overcurrent detection at discharge delay time (OCD_DLY[3:0] + 1) x 1ms. If alarm condition continues after delay time, ALARM will be turned ON. 0000 : 1ms (Default)
4	-	
3-0	OCC_DLY [3:0]	Overcurrent detection at charge delay time (OCC_DLY[3:0] + 1) x 1ms. If alarm condition continues after delay time, ALARM will be turned ON. 0000 : 1ms (Default)

Address: 0x14 CB_CTRL

bit	15	14	13	12	11	10	9	8
bit name	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	-	-	-	CB_ PROTECT	-	-	<Reserved>	CB_PD
R/W	R	R	R	R/W	R	R	R/W	R/W
initial	0	0	0	0	0	0	0	1

bit	bit name	explanation
15-5	-	
4	CB_ PROTECT	Adjacent cell protection during balancing 0 : cell operation as per register setting 1: Lower cell (n-1) has higher priority than upper cell (n) when the adjacent cells are performing cell balancing, (Note: Recommended to use when all cells are connected.)
3-2	-	
1	<Reserved>	Please always set to “0”
0	CB_PD	Cell balance circuit control 0： Cell balance circuit active 1： Cell balance circuit power down（default）

Address: 0x15 CBSEL

bit	15	14	13	12	11	10	9	8
bit name	DI_CBSEL[16:9]							
R/W	R/WL							
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	DI_CBSEL[8:1]							
R/W	R/WL							
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-0	DI_CBSEL [16:1]	Selection of cell for balancing 1 : Cell balance selected 0 : Cell balance not selected (Default)

Address: 0x17 GPIOSEL

bit	15	14	13	12	11	10	9	8
bit name	-	-	OSC2_DIV		GPIO6SEL[1:0]		GPIO5SEL[1:0]	
R/W	R	R	R/WL		R/WL		R/WL	
initial	0	0	1	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	GPIO4SEL[1:0]		GPIO3SEL[1:0]		GPIO2SEL[1:0]		GPIO1SEL[1:0]	
R/W	R/WL		R/WL		R/WL		R/WL	
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-14	-	
13-12	OSC2_DIV	Low Speed Clock Divider (when output from GPIO4) 00: 1/1 (262.144kHz) 01: 1/32 (8.192kHz) 10: 1/64 (4.096kHz) (Default) 11: 1/128 (2.048kHz)
11-10	GPIO6SEL [1:0]	GPIO6 output selection 00: GPIO6(Default) 01: ALARM2 10: Prohibited 11: Prohibited
9-8	GPIO5SEL [1:0]	GPIO5 output selection 00: GPIO5(Default) 01: High speed AD conversion interrupt 10: Prohibited 11: Prohibited
7-6	GPIO4SEL [1:0]	GPIO4 output selection 00: GPIO4(Default) 01: Low speed AD conversion interrupt 10: Prohibited 11: Low speed clock output
5-4	GPIO3SEL [1:0]	GPIO3 output selection 00: GPIO3(Default) 01: Prohibited 10: Prohibited 11: High speed clock output
3-2	GPIO2SEL [1:0]	GPIO2 output selection 00: GPIO2(Default) 01: Prohibited 10: Analog input 11: GPOH2 output state
1-0	GPIO1SEL [1:0]	GPIO1 output selection 00: GPIO1(Default) 01: Prohibited 10: Analog input 11: GPOH1 output state

Address: 0x18 SPICTRL

bit	15	14	13	12	11	10	9	8
bit name	-	-	<Reserved>	<Reserved>	-	SDI_PLDW	SCL_PLDW	SEN_PLDW
R/W	R	R	R/W	R/W	R	R/W	R/W	R/W
initial	0	0	0	0	0	1	1	1

bit	7	6	5	4	3	2	1	0
bit name	-	-	<Reserved>	LP50EN	-	-	-	COM_STP
R/W	R	R	R/W	R/W	R	R	R	R/W
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-14	-	
13-12	<Reserved>	Please always set to “0”
11	-	
10	SDI_PLDW	SDI pin pull-down control signal 0: No pull-down 1: Pull-down (default)
9	SCL_PLDW	SCL pin pull-down control signal 0: No pull-down 1: Pull-down (default)
8	SEN_PLDW	SEN pin pull-down control signal 0: No pull-down 1: Pull-down (default)
7-6	-	
5	<Reserved>	Please always set to “0”
4	LP50EN	VDD50 power drive mode selection 1 : Low power mode 0 : Normal mode (default)
3-1	-	
0	COM_STP	SPI communication control operation SPI communication can be turned OFF with this bit setting. It is required to input High to SEN pin for more than 1ms in order to resume communication. This bit is cleared automatically.

Address: 0x19 ADCTRL1

bit	15	14	13	12	11	10	9	8
bit name	<Reserved>	<Reserved>	<Reserved>		<Reserved>		-	-
R/W	R/WL	R/WL	R/WL		R/WL		R	R
initial	0	0	0	0	1	1	0	0

bit	7	6	5	4	3	2	1	0
bit name	<Reserved>	<Reserved>	ADI_LATCH_SET	ADV_LATCH_SET	-	<Reserved>	<Reserved>	<Reserved>
R/W	R/WL	R/WL	R/WL	R/WL	R	R/WL	R/WL	R/WL
initial	1	0	0	0	0	0	0	0

bit	bit name	explanation
15-14	<Reserved>	Please always set to “0”.
13-12	<Reserved>	Please always set to “00”.
11-10	<Reserved>	Please always set to “11”.
9	-	
8	-	
7-6	<Reserved>	Please always set to "10“.
5	ADI_LATCH_SET	High speed current ADC measurement data latch timing 1 : After ADIH_LATCH = 1, on-going data latch when 1 cycle is completed. 0 : After ADIH_LATCH = 1, previous data latch immediately (default).
4	ADV_LATCH_SET	ADC Voltage measurement data latch Timing 1 : After ADV_LATCH = 1, on-going all data latch when 1 cycle is completed. 0 : After ADV_LATCH = 1, previous all data latch immediately (default).
3	-	
2-0	<Reserved>	Please always set to “000”.

Address: 0x1A ADCTRL2

bit	15	14	13	12	11	10	9	8
bit name	-	-	ADSWHY_EN	ADSWSD_EN	-	-	-	-
R/W	R	R	R/WL	R/WL	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	<Reserved>	<Reserved>	<Reserved>	ISD_ STOPEN	-	-	ADIL_ON	ADIH_ON
R/W	R/WL	R/WL	R/WL	R/WL	R	R	R/WL	R/WL
initial	0	0	1	1	0	0	0	0

bit	bit name	explanation
15-14	-	
13	ADSWHY_EN	High Speed Current ADC Enable 0 : OFF(Default) 1 : ON
12	ADSWSD_EN	Low Speed Current ADC Enable 0 : OFF(Default) 1 : ON
11-8	-	
7-5	<Reserved>	Please always set to “001”.
4	ISD_ STOPEN	Low Speed Current ADC Stop Control 0 : Enable simultaneous operation high speed and low speed current ADC 1 : Disable Low Speed Current ADC for high speed current ADC operation. (default)
3-2	-	
1	ADIL_ON	Enable Low speed current ADC Operation 0 : Disable (default) 1 : Enable
0	ADIH_ON	Enable High Speed current ADC operation 0 : Disable (default) 1 : Enable

Address:0x1B GPOH_CTRL

bit	15	14	13	12	11	10	9	8
bit name	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	-	-	GPOH2_ ALM_ST	GPOH1_ ALM_ST	-	GPOH_FET	GPOH2_EN	GPOH1_EN
R/W	R	R	R/WL	R/WL	R	R/WL	R/WL	R/WL
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-6	-	
5	GPOH2_ ALM_ST	If using FET at GPOH2 pin, to set GPOH2 pin data to output during ALARM Effective only when FDRV_ALM_SD=1 & GPOH_FET=1 1 : Low output 0 : HiZ (default)
4	GPOH1_ ALM_ST	If using FET at GPOH1 pin, set GPOH1 pin data to output during ALARM Effective only when FDRV_ALM_SD=1 & GPOH_FET=1 1 : Low output 0 : HiZ (default)
3	-	
2	GPOH_FET	Set GPOH_FET=1 when using FET at GPOH By setting this bit to “1”, the FET driver ON/OFF Control is made possible during ALARM condition (as per FDRV_CTRL setting) GPOH_FET=0 (Default)
1	GPOH2_EN	GPOH2 output data 1 : Low output 0 : HiZ (default)
0	GPOH1_EN	GPOH1 output data 1 : Low output 0 : HiZ (default)

Address:0x1C INRCV1

bit	15	14	13	12	11	10	9	8
bit name	INR_CV[15:8]							
R/W	R/WL							
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	INR_CV[7:0]							
R/W	R/WL							
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-0	INR_CV[15:0]	Input PORT number setting for disconnection detection circuit INR_CV[n] Cn pin (INR_CV_16bit as shown in INRCV2 register corresponds to Cell 16)

Address:0x1D INRCV2

bit	15	14	13	12	11	10	9	8
bit name	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	-	-	-	-	-	-	-	INR_CV_16
R/W	R	R	R	R	R	R	R	R/WL
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-1	-	
0	INR_CV_16	Input PORT C16 setting for disconnection detection circuit.

Address:0x1E INR_CTL

bit	15	14	13	12	11	10	9	8
bit name	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	-	-	-	-	-	-	-	INR_EN
R/W	R	R	R	R	R	R	R	R/WL
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-1	-	
0	INR_EN	Disconnection detection circuit operation 0：Disconnection detection OFF（default） 1：Disconnection detection ON

Address: 0x21 SPI_STAT

bit	15	14	13	12	11	10	9	8
bit name	-	SPI_F	-	-	-	-	-	-
R/W	R	R/WL	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15	-	
14	SPI_F	SPI Communication Error Flag 0 : No Communication Error 1 : Communication Error If communication error is detected, SPI_F=1 and it is cleared by writing “1”.
13-0	-	

Address: 0x22 MODE_STAT

bit	15	14	13	12	11	10	9	8
bit name	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	-	-	COND_SCD	COND_OCD	COND_OCC	ST_SDWN	ST_STBY	ST_ACT
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	x	x	x

bit	bit name	explanation
15-6	-	
5	COND_SCD	SCD detection flag 0 : SCD not detected 1 : SCD detected (auto cleared when short circuit condition removed)
4	COND_OCD	OCD detection flag 0 : OCD not detected 1 : OCD detected (auto cleared when over current at discharge condition removed)
3	COND_OCC	OCC detection flag 0 : OCC not detected 1 : OCC detected (auto cleared when over current at charge condition removed)
2	ST_SDWN	Shutdown Mode(Operation Mode) Flag 0 : Not under Shutdown Mode 1 : Under Shutdown Mode * The initial state depend on external pins setting
1	ST_STBY	Standby Mode (Operation Mode) Flag 0 : Not Under Standby Mode 1 : Under Standby Mode * The initial state depend on external pins setting
1	ST_ACT	Active Mode (Operation Mode) 0 : Not under Active Mode 1 : Under Active Mode * The initial state depend on external pins setting

Address: 0x2E FUSE_RADR

bit	15	14	13	12	11	10	9	8
bit name	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	FUSE_RADR[7:0]							
R/W	R/W							
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-8	-	
7-0	FUSE_RADR [7:0]	Setting for FUSE read address The value of this register is shown in 0x2F register.

Address: 0x2F FUSE_DATA

bit	15	14	13	12	11	10	9	8
bit name	FUSE_RDATA[15:8]							
R/W	R							
initial	X	X	X	X	X	X	X	X

bit	7	6	5	4	3	2	1	0
bit name	FUSE_RDATA[7:0]							
R/W	R							
initial	X	X	X	X	X	X	X	X

bit	bit name	explanation
15	FUSE_RDATA [15:0]	0x2E register (FUSE_RADR) The value of 0x2E register (FUSE_RADR) is shown in this address.

Address: 0x30 STAT

bit	15	14	13	12	11	10	9	8
bit name	-	-	-	-	-	-	ST_OV	ST_UV
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	-	ST_SCD	ST_OCD	ST_OCC	-	IADS_DONE	IADH_DONE	VAD_DONE
R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-10	-	
9	ST_OV	OV detection status display 0 : OV not detected 1 : OV detected If OV is detected in any cell, OVSTAT=1 is shown.
8	ST_UV	UV detection status display 0 : UV not detected 1 : UV detected If UV is detected in any cell, UVSTAT=1 is shown.
7	-	
6	ST_SCD	SCD detection flag 0 : SCD not detected 1 : SCD detected If SCD is detected, ST_SCD=1 and it is cleared by writing “1”. ALARM1 pin outputs LOW when ST_SCD=1.
5	ST_OCD	OCD detection flag 0 : OCD not detected 1 : OCD detected If OCD is detected, ST_OCD=1 and it is cleared by writing “1”. Either ALARM1 pin or ALARM2 pin outputs LOW when ST_OCD=1.
4	ST_OCC	OCC detection flag 0 : OCC not detected 1 : OCC detected If OCC is detected, ST_OCC=1 and it is cleared by writing “1”. Either ALARM1 pin or ALARM2 pin outputs LOW when ST_OCC=1.
3	-	
2	IADS_DONE	Low speed current ADC completion flag 0 : Measurement incomplete 1 : Measurement completed It is cleared to “0” by writing "1“
1	IADH_DONE	High speed current ADC completion flag 0 : Measurement incomplete 1 : Measurement completed It is cleared to “0” by writing "1“
0	VAD_DONE	Voltage measurement ADC Completion flag 0 : Measurement incomplete 1 : Measurement completed It is cleared to “0” by writing "1“

Address: 0x31 OVSTAT

bit	15	14	13	12	11	10	9	8
bit name	OV16_F	OV15_F	OV14_F	OV13_F	OV12_F	OV11_F	OV10_F	OV9_F
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	OV8_F	OV7_F	OV6_F	OV5_F	OV4_F	OV3_F	OV2_F	OV1_F
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15 - 0	OV16_F to OV1_F	Cell 16 to Cell1 OV detection output *automatic update 1 : Abnormal 0 : Normal

Address: 0x32 UVSTAT

bit	15	14	13	12	11	10	9	8
bit name	UV16_F	UV15_F	UV14_F	UV13_F	UV12_F	UV11_F	UV10_F	UV9_F
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	UV8_F	UV7_F	UV6_F	UV5_F	UV4_F	UV3_F	UV2_F	UV1_F
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15 - 0	UV16_F to UV1_F	Cell16 to Cell1 UV detection output *automatic update 1 : Abnormal 0 : Normal

Address: 0x33 CV01_AD

bit	15	14	13	12	11	10	9	8
bit name	CV01_AD[15:8]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	CV01_AD[8:0]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-0	CV01_AD [15:0]	Cell 1Voltage Measurement output. Value: 0x3FFF : 4.999695V … 0x2000 : 2.5V … 0x0001 : 0.000305V 0x0000 : 0V Measured Voltage = Value x 0.000305V * Note: bit15,14 are always "0“.

Note: The definition for register addresses 0x34 (CV02_AD) ~ 0x42 (CV16_AD) are the same as register 0x33 (CV01_AD).

Address: 0x43 VPAC_AD

bit	15	14	13	12	11	10	9	8
bit name	VPAC_AD[15:8]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	VPAC_AD[8:0]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-0	VPAC_AD [15:0]	VPACK Voltage Measurement output Value: 0x3FFF : 99.993896V … 0x2000 : 50V … 0x0001 : 0.006104V 0x0000 : 0V Measured Voltage = value x 0.006104V * Note: bit15,14 are always "0“.

Address: 0x44 TMONI1_AD

bit	15	14	13	12	11	10	9	8
bit name	TMONI1_AD[15:8]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	TMONI1_AD[8:0]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-0	TMONI1_AD [15:0]	TMONI1Voltage Measurement output Value: 0x3FFF : 4.999695V … 0x2000 : 2.5V … 0x0001 : 0.000305V 0x0000 : 0V Measured Voltage = Value x 0.000305V * Note: bit15,14 are always "0“.

Note: The definition for register addresses 0x45 (TMONI2_AD) ~ 0x48 (TMONI5_AD) are the same as register 0x44 (TMONI1_AD).

Address: 0x49 VDD50_AD

bit	15	14	13	12	11	10	9	8
bit name	VDD50_AD[15:8]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	VDD50_AD[8:0]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-0	VDD50_AD [15:0]	VDD50 Voltage Measurement output Value: 0x3FFF : 7.499542V … 0x2000 : 3.75V … 0x0001 : 0.000458V 0x0000 : 0V Measured Voltage = Value x 0.000458V * Note: bit15,14 are always "0“.

Address: 0x4A GPIO1_AD

bit	15	14	13	12	11	10	9	8
bit name	GPIO1_AD[15:8]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	GPIO1_AD[8:0]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-0	GPIO1_AD [15:0]	GPIO1Voltage Measurement output Value: 0x3FFF : 4.999695V … 0x2000 : 2.5V … 0x0001 : 0.000305V 0x0000 : 0V Measured Voltage = Value x 0.000305V * Note: bit15,14 are always "0“.

Note: The definition for register address 0x4B (GPIO2_AD)is the same as register 0x4A (GPIO1_AD).

Address: 0x4C CVIH_AD

bit	15	14	13	12	11	10	9	8
bit name	CVIH_AD[15:8]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	CVIH_AD[8:0]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-0	CVIH_AD [15:0]	High speed current ADC Measurement output Value: 0x7FFF : 179.994507mV … 0x0001 : 0.005493mV 0x0000 : 0V 0xFFFF : -0.005493mV … 0x8001 : -179.994507mV 0x8000 : -180mV Voltage/step = 0.005493mV Measured voltage = 2's complement data * 360mV/2^16

Note: It is 2's complement data range -180mV to 179.994507mV

Address: 0x4D CVIL_AD

bit	15	14	13	12	11	10	9	8
bit name	CVIL_AD[15:8]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	CVIL_AD[8:0]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-0	CVIL_AD [15:0]	Low speed current ADC measurement output Value: 0x7FFF : 179.994507mV … 0x0001 : 0.005493mV 0x0000 : 0V 0xFFFF : -0.005493mV … 0x8001 : -179.994507mV 0x8000 : -180mV Voltage/step = 0.005493mV Measured voltage = 2's complement data * 360mV/2^16

Note: It is 2's complement data range -180mV to 179.994507mV

Address: 0x52 OVL_STAT

bit	15	14	13	12	11	10	9	8
bit name	OV16_LF	OV15_LF	OV14_LF	OV13_LF	OV12_LF	OV11_LF	OV10_LF	OV9_LF
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	OV8_LF	OV7_LF	OV6_LF	OV5_LF	OV4_LF	OV3_LF	OV2_LF	OV1_LF
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15 – 0	OV16_LF to OV1_LF	Cell 16 to Cell1 OV detection flag 0 : OV not detected 1 : OV detected

* If OV is detected, the detected bit=1and it is cleared to “0” by writing “1”.

Address: 0x53 UVL_STAT

bit	15	14	13	12	11	10	9	8
bit name	UV16_LF	UV15_LF	UV14_LF	UV13_LF	UV12_LF	UV11_LF	UV10_LF	UV9_LF
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	UV8_LF	UV7_LF	UV6_LF	UV5_LF	UV4_LF	UV3_LF	UV2_LF	UV1_LF
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15 - 0	UV16_LF to UV1_LF	Cell 16 to Cell 1 UV detection flag 0 : UV not detected 1 : UV detected

* If UV is detected, the detected bit=1 and it is cleared to “0” by writing “1”.

Address:0x54 FAILSTAT

bit	15	14	13	12	11	10	9	8
bit name	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	X	X

bit	7	6	5	4	3	2	1	0
bit name	-	-	-	-	-	VO_POUVC_OUT	-	VDD50_OVP
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	X	0	0	0	0

bit	bit name	explanation
15 – 3	-	
2	VO_POUVC_OUT	CVDD pin UVLO detection signal (H:UVLO release)
1	-	
0	VDD50_OVP	VDD50 OVP detection output

Address:0x55 FDRVSTAT

bit	15	14	13	12	11	10	9	8
bit name	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	-	-	-	-	FDRV_DIS_ST	FDRV_CHG_ST	GPOH2_ST	GPOH1_ST
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-4	-	
3	FDRV_DIS_ST	DIS Pin state
2	FDRV_CHG_ST	CHG Pin state
1	GPOH2_ST	GPOH2 state 0 : HiZ, 1 : Output Low
0	GPOH1_ST	GPOH1 state 0 : HiZ, 1 : Output Low

Address: 0x56 CBSTAT

bit	15	14	13	12	11	10	9	8
bit name	CB_ST[16:9]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
bit name	CB_ST[8:1]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	bit name	explanation
15-0	CB_ST[16:0]	Display of Individual cell balance control status. 0 : Cell balance OFF 1 : Cell balance ON