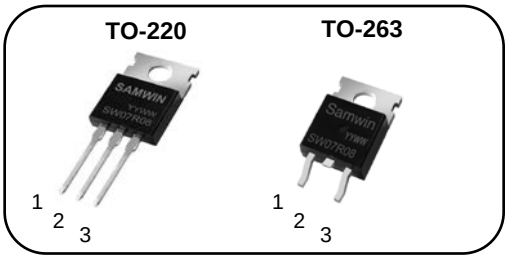
Samwin®

SW07R08

N-channel Enhanced mode TO-263/TO220 MOSFET

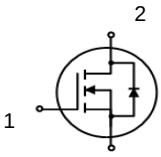
Features

- High ruggedness
- Low $R_{DS(ON)}$ (Typ 7mΩ)@V_{GS}=10V
- Low Gate Charge (Typ 76nC)
- Improved dv/dt Capability
- 100% Avalanche Tested
- Application: LED, Charge, Adaptor



1. Gate 2. Drain 3. Source

BV_{DSS} : 80V
I_D : 80A
$R_{DS(ON)}$: 7mΩ



General Description

This power MOSFET is produced with advanced super junction technology of SAMWIN. This technology enable the power MOSFET to have better characteristics, including fast switching time, low on resistance, low gate charge and especially excellent avalanche characteristics.

Order Codes

Item	Sales Type	Marking	Package	Packaging
1	SW B 07R08	SW07R08	TO-263	REEL
2	SW P 07R08	SW07R08	TO-220	REEL

Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to source voltage		80	V
I_D	Continuous drain current (@T_C=25°C)		80*	A
	Continuous drain current (@T_C=100°C)		70*	A
I_{DM}	Drain current pulsed	(note 1)	340	A
V_{GS}	Gate to source voltage		±25	V
E_{AS}	Single pulsed avalanche energy	(note 2)	350	mJ
E_{AR}	Repetitive avalanche energy	(note 1)	210	mJ
P_D	Total power dissipation (@T_C=25°C)		240	W
	Derating factor above 25°C			W/°C
T_{STG}, T_J	Operating junction temperature & storage temperature		-55 ~ 175	°C

*. Drain current is limited by junction temperature.

Thermal characteristics

Symbol	Parameter	Value		Unit
		TO263	TO220	
R_{thjc}	Thermal resistance, Junction to case	0.52		°C/W
R_{thja}	Thermal resistance, Junction to ambient	55		°C/W

Electrical characteristic (T_C = 25ºC unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	V_{GS}=0V, I_D=250uA	80			V
I_{DSS}	Drain to source leakage current	V_{DS}=64V, V_{GS}=0V			1	uA
		T_C=125ºC			100	uA
I_{GSS}	Gate to source leakage current, forward	V_{GS}=30V, V_{DS}=0V			100	nA
	Gate to source leakage current, reverse	V_{GS}=-30V, V_{DS}=0V			-100	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250uA	2	3	4	V
$R_{DS(ON)}$	Drain to source on state resistance	V_{GS}=10V, I_D=40A		7	9	mΩ
Dynamic characteristics						
C_{iss}	Input capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz		3110		pF
C_{oss}	Output capacitance			445		
C_{rss}	Reverse transfer capacitance			270		
$t_{d(on)}$	Turn on delay time	V_{DS}=37.5V, I_D=40A, R_G=6.8Ω, V_{GS}=10V (note 4,5)		20.4		ns
t_r	Rising time			63		
$t_{d(off)}$	Turn off delay time			67		
t_f	Fall time			43		
Q_g	Total gate charge	V_{DS}=37.5V, V_{GS}=10V, I_D=40A (note 4,5)		76		nC
Q_{gs}	Gate-source charge			9.5		
Q_{gd}	Gate-drain charge			40		
R_g	Gate resistance	V_{DS}=0V, Scan F mode		1.3		Ω

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET			80	A
I_{SM}	Pulsed source current				320	A
V_{SD}	Diode forward voltage drop.	I_S=40A, V_{GS}=0V			1.3	V
t_{rr}	Reverse recovery time	I_S=40A, dI_F/dt=100A/us		25		ns
Q_{rr}	Reverse recovery charge			18.5		nC

※. Notes

1. Repeatitive rating : pulse width limited by junction temperature.
2. L =1mH, I_{AS} =40A Starting T_J = 25ºC
3. I_{SD} ≤80A, di/dt = 100A/us, V_{DD} ≤ BV_{DSS}, Staring T_J =25ºC
4. Pulse Test : Pulse Width ≤ 300us, duty cycle ≤ 2%
5. Essentially independent of operating temperature.

Fig. 1. On-state characteristics

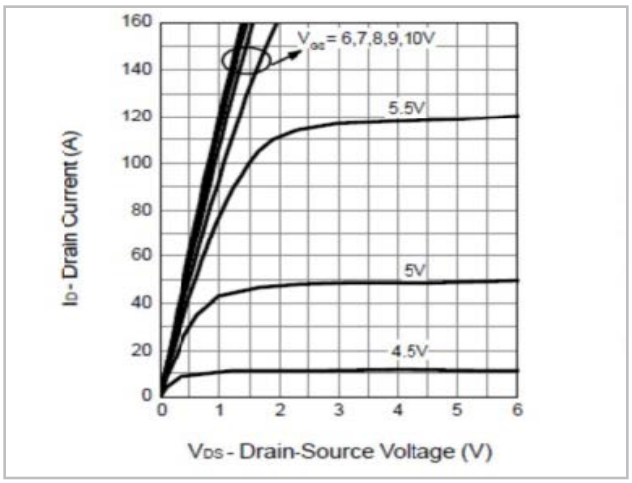


Fig. 2. On-resistance variation vs. drain current and gate voltage

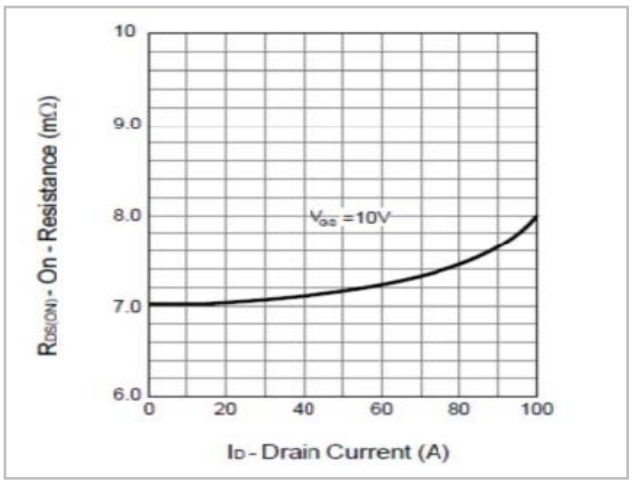


Fig. 3. Gate charge characteristics

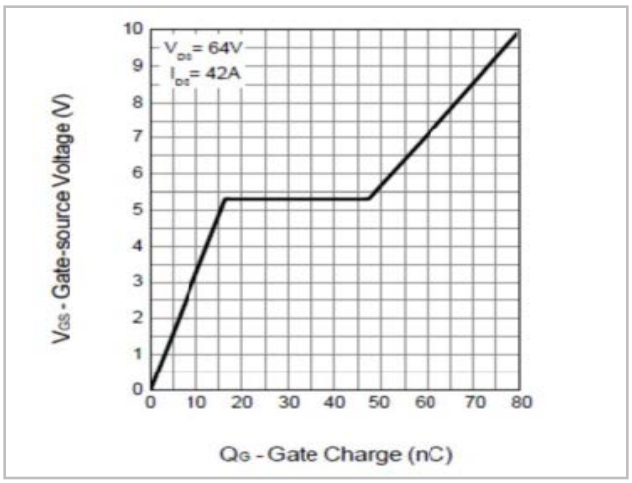


Fig. 4. On state current vs. diode forward voltage

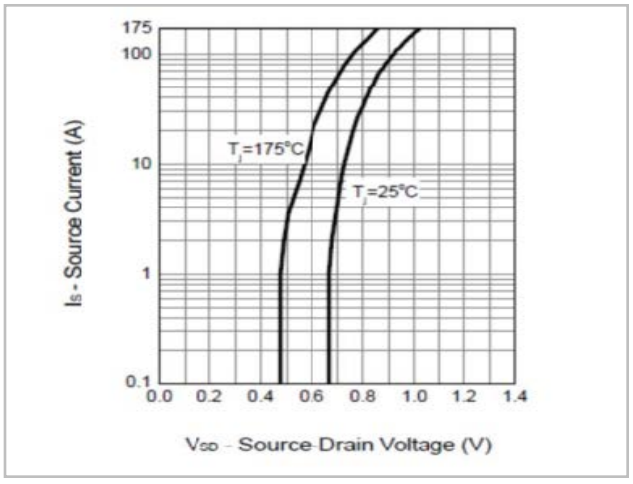


Fig 5. Breakdown Voltage Variation vs. Junction Temperature

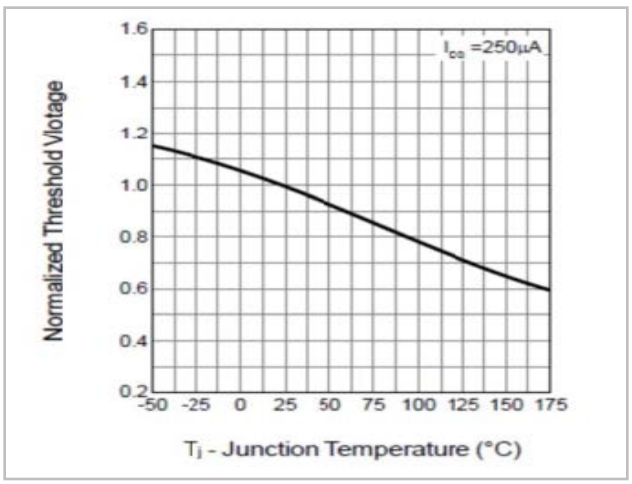


Fig. 6. On resistance variation vs. junction temperature

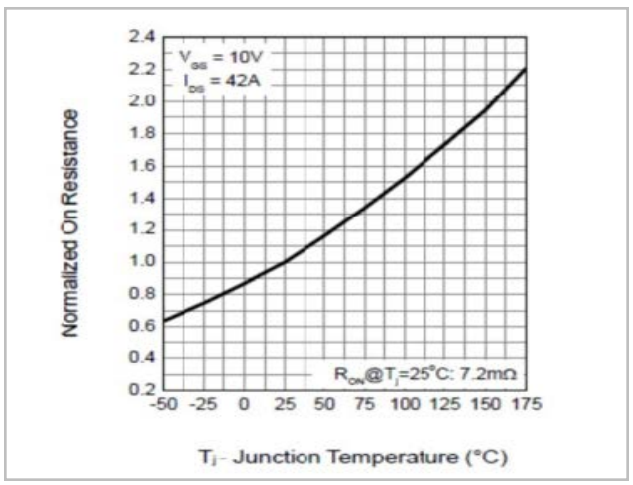


Fig. 7. Maximum safe operating area

Fig. 8. Capacitance Characteristics

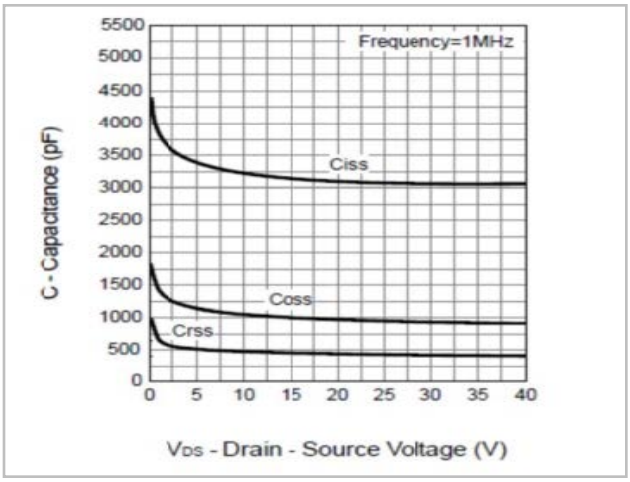


Fig. 9. Transient thermal response curve

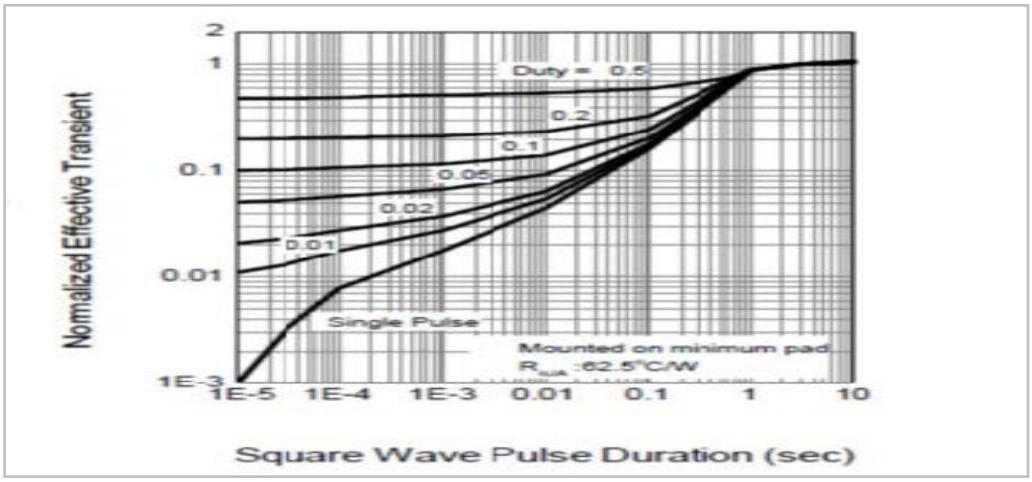


Fig. 10. Gate charge test circuit & waveform

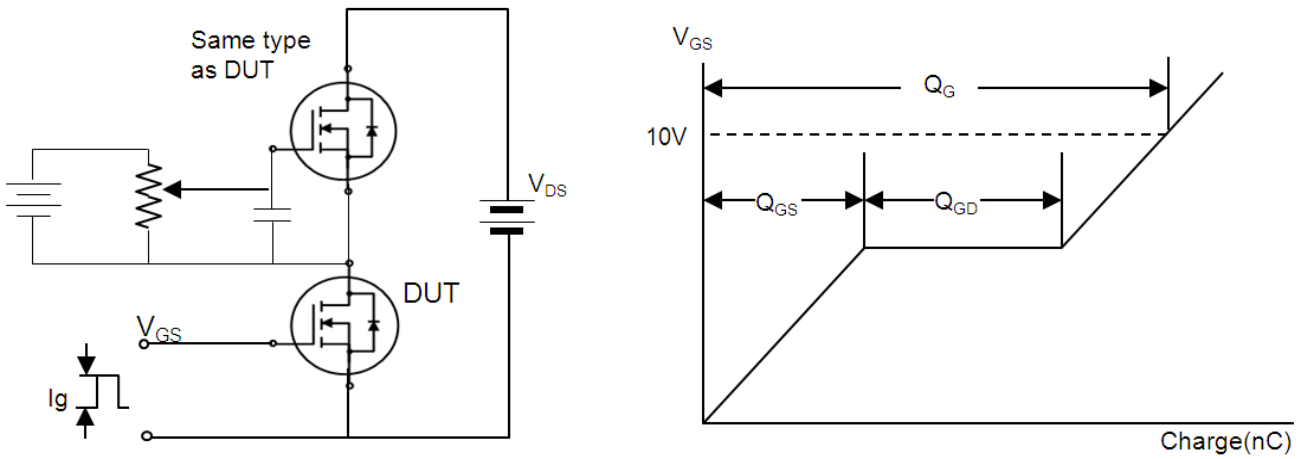


Fig. 11. Switching time test circuit & waveform

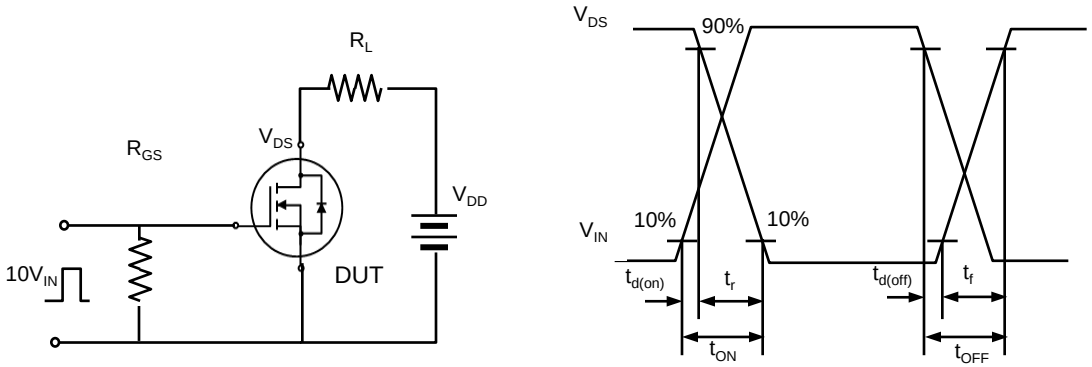


Fig. 12. Unclamped Inductive switching test circuit & waveform

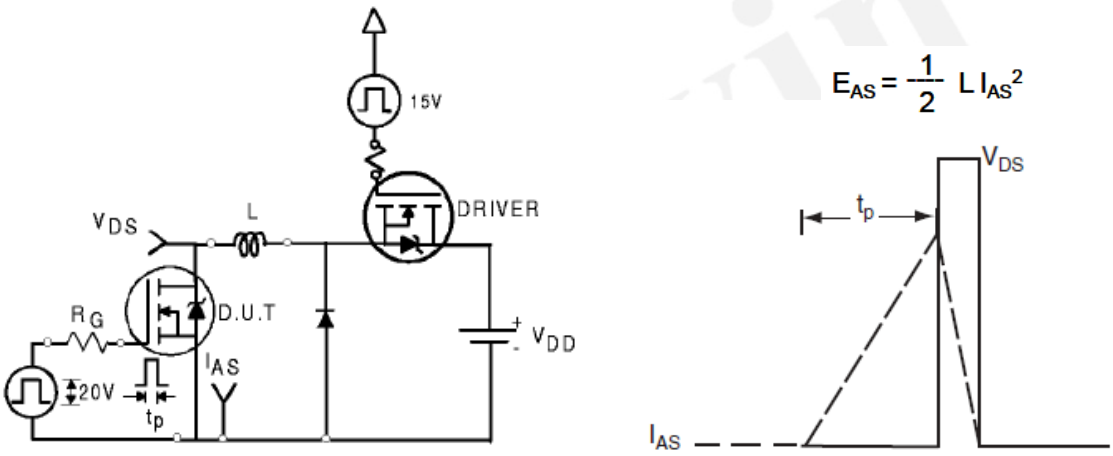
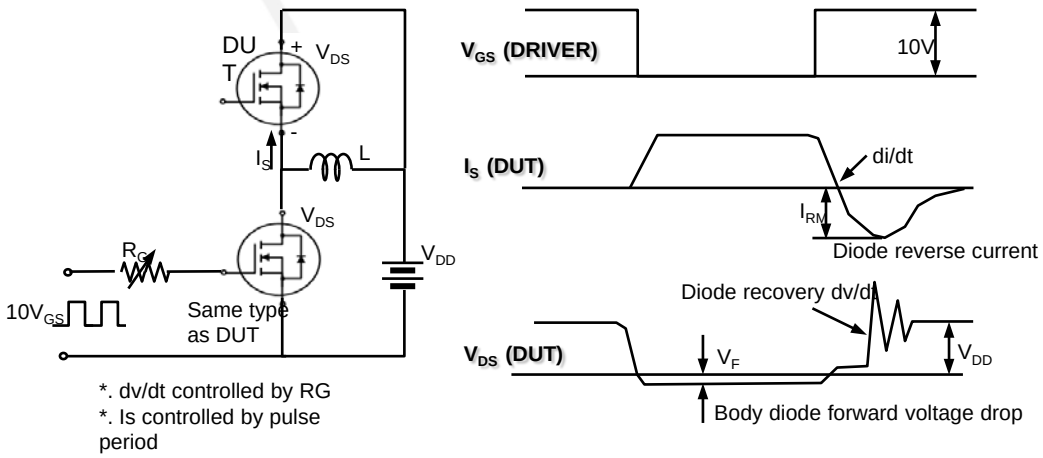


Fig. 13. Peak diode recovery dv/dt test circuit & waveform



*. dv/dt controlled by RG
*. Is controlled by pulse period

DISCLAIMER

* All the data & curve in this document was tested in XI'AN SEMIPOWER TESTING & APPLICATION CENTER.
* This product has passed the PCT,TC,HTRB,HTGB,HAST,PC and Solderdunk reliability testing.
* Qualification standards can also be found on the Web site (**http://www.semipower.com.cn**)
* Suggestions for improvement are appreciated, Please send your suggestions to **samwin@samwinsemi.com**