High Side Driver for Buck Converter with an LDO

Introduction

Most boost converters have been applied to step-up voltage applications, such as the PDA, N/B PC, cellular phone, palmtop computer, GPS, camcorder, portable DVD, toy, and DSC, to elevate a low voltage to a high voltage to provide low quiescent current and high efficiency regulator in the recent years. Yet, technically, the boost converter does not supply applications of high loading current today. Also, the LDO usually can not transform to a relatively high energy.

AIC1630A is not only a boost converter but also an application of step-down and a low-dropout function. The circuit, shown as Fig. 1, can step down from 5V or 12V to as low as 2.5V, 1.8V and 1.25V with 80% efficiencies. A linear controller can be implemented by using the pin 6 and 7 of AIC1630A, as shown Fig. 1.

And it works well at low input voltages. For example, a 2.5V input, which comes from the output of AIC1630A, can be converted into an output of 1.8V. Due to the ultra-low dropout voltage, the power dissipation is much lower than the general LDO's.

Principle of operation

The principle of energy storage in the inductor L can be applied to the buck converter. And the inductor energy then is to be transferred to the output via the schootky diode D. When the switch is on, the diode is used as a reverse biased and the inductor current will ramp up. When the switch is off, the inductor reverses its polarity with a switch current to maintain output voltage.

1. AIC1630A driving P-MOSFET

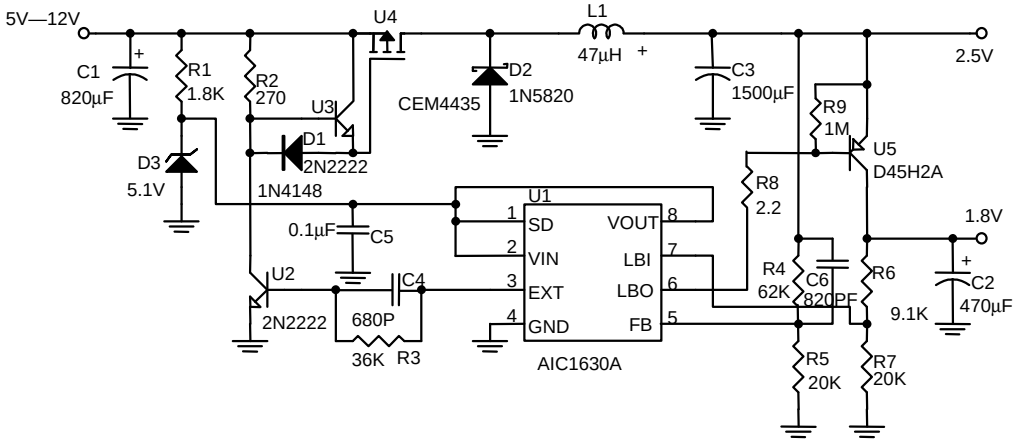

Fig. 1 AIC1630A+LDO for P-MOSFET Circuit

A boost-switching regulator with the addition of two external switching transistors is considered as a buck converter, shown in Fig. 1. Via EXT (pin3), the internal switch of AIC1630A, drives the transistor (U2). When U2 is set on, the gate polarity of U4 (P-MOS) will be low and U4 will be turned on. When U2 is off, the U4 gate polarity will be high and U4 will be turned off, due to the input voltage delivered to gate polarity via U3 transistor. The rising time of gate signal is much longer when U3 and D1 are not considered. See Fig. 2 and 3 for the difference.

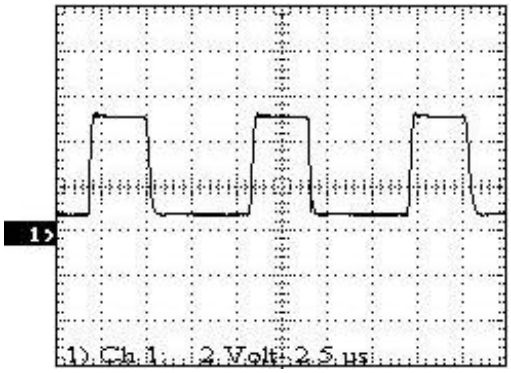

Fig. 2 Gate Signal of P-MOS

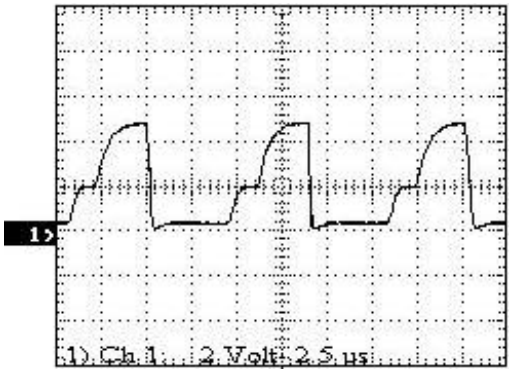

Fig. 3 Gate Signal of P-MOS

C_{ISS} capacitor of MOSFET results in the gate signal in Fig. 3. The use of U3 and D1 can reduce the influence of C_{ISS} on the boost-switching regulator.

2. AIC1630A Driving N-MOSFET

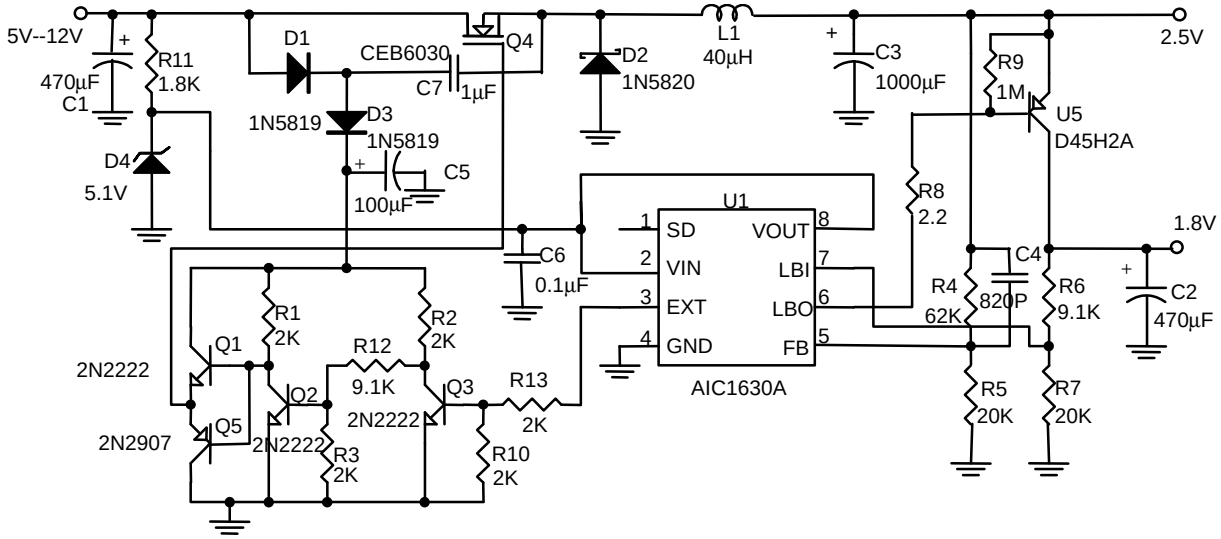

Fig. 4 AIC1630A+LDO for N-MOSFET Circuit

AIC1630A with the addition of four external switching transistors is considered as a buck converter, shown in Fig. 4. Via EXT (pin3), the internal switching of IC drives fast driving N-channel circuit, which is composed of Q1, Q2, Q3, and Q5. Bootstrapping circuit (composed of D1, D3, C5 and C7) can provide N-channel circuit with twice as much as the input voltage. When Q4 is on, the diode is used as a reverse biased. Current flows via Q4 as well as the inductor L1 to output polarity. When Q4 is off, the inductor L1 reverses its polarity with its energy transferred to the output loading, and the diode turns forward biased.

Functions of the bootstrapped driver circuit and driven N-channel circuit play important roles in the application of AIC1630A and LDO with N-MOSFET circuit.

3. Bootstrapped Function

As shown in Fig. 5 and 6, the peak rectifier circuit comprises two diodes (D1 and D3) and two filter capacitors (C7 and C5). And the voltage filtered by peak rectifier may provide control voltage with two times of V_{IN} dc voltage as shown in Fig. 6 (the lower waveform). Because the output voltage is boosted up by a square waveform of amplitude V_{IN} to two times of the input voltage, the circuit is considered as a "bootstrapped circuit".

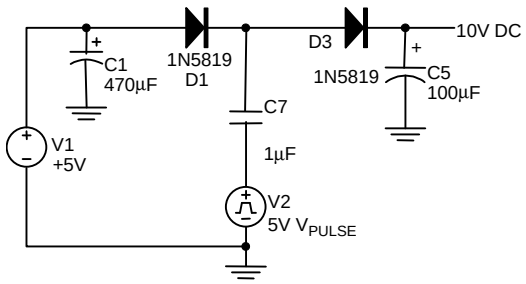

Fig. 5 Bootstrapped Voltage

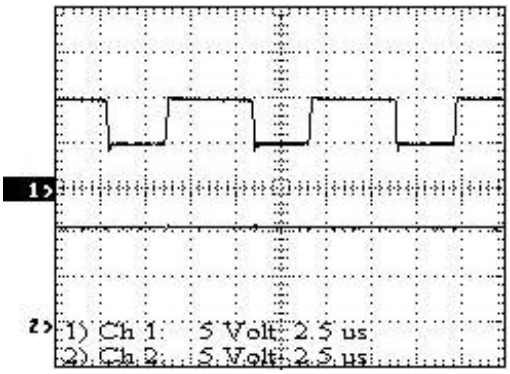

Fig. 6 Bootstrapped Circuit
Upper: D1 Cathode Polarity Signal
Lower: 10VDC

- Driven N-channel function

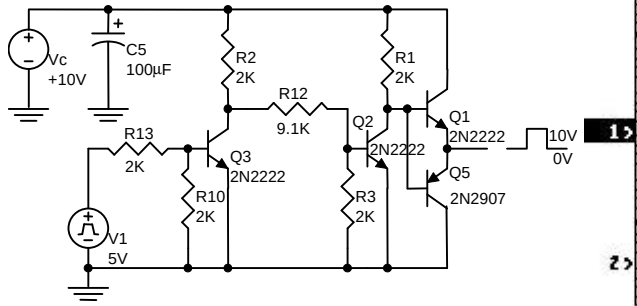

Fig. 7 Fast Driven N-MOSFET Circuit

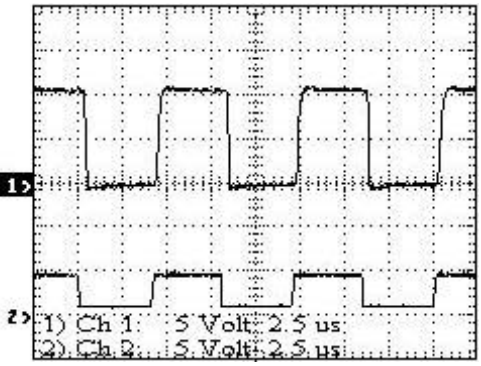

Fig. 8 Driven N-channel Signal
Upper: 5V-Driving Signal
Lower: 10V-Driving Signal

Such as Fig. 7, this driven N-channel function is composed of three NPN transistors, one PNP transistor and six resistors. The configuration of the function block consists of two inverters and one push-pull. The output from the driven circuit, which has an input of 1MHZ, can produce a perfect square signal of 1MHZ. As Fig. 8, the 5V-driving signal will push to 10V-driving signal, which drives N-MOSFET Q4 working properly.

3. AIC1630A for LDO application

1. Input voltage of LDO is provided by the output voltage of buck converter. It can resolve some LDO problems, such as: high dropout voltage and high power consumption. Therefore, the advantage of LDO is to provide a fast transient response, which is what switch converter can not offer. Fig. 4 illustrates that the base current of U5 is controlled by R8 and R9 turns U5 off when LBO floats. Note that, at a light load, R8 and R9 have an effect on efficiency as well as the maximum available output current. And lower R8 and R9 may drive higher output current, but cause AIC1630A N-MOSFET circuit to draw higher level of quiescent current.

Component selection

The section is divided into two parts. The first part talks about the calculation and selection of the circuit components on buck converter. And the second part introduces an LDO application.

All of the following calculations are effective when switch converter is operated in a continuous-conduction mode.

(1) Switch converter application

The duty cycle is calculated as:

$$DUTY_{(MAX)} = \frac{T_{ON(MAX)}}{T} = \frac{V_{OUT} + V_F}{V_{IN(MIN)} - V_Q + V_F}$$

Where

V_F: sckottky diode forward voltage

V_Q: series pass element (MOSFET) switch on voltage ($V_Q = I_Q \times R_{DS(ON)}$)

For example 1:

	Min	typ	max	unit
V_{IN}	5		12	V
V_{OUT}		2.5		V
I_{OUT}	0.1		3	A
V_{RIPPLE}		50		mV

Assumed that the frequency of operation is 100KHZ, the forward voltage of sckottky diode is 0.2V and the switch on voltage of MOSFET is 0.5V. The sequence, when the switch is on, is calculated as below:

- **Selection of inductor**

There are many different ways to calculate the inductance of the required inductor. We can get easily it from the inductor ripple current ΔI_P. When the minimum loading current is 100mA, the regulator will operate in continuous–conduction mode. Thus, the inductor ripple current is calculated as:

$$T_{ON(MAX)} = DUTY_{(MAX)} \times T = \frac{2.5+0.2}{5-0.5+0.2} \times \frac{1}{120K} = 4.7\mu s$$

$$\Delta I_P = 2I_{OUT(MIN)} = 200mA$$

Required inductance:

$$L(MIN) = \frac{\Delta V_L}{\Delta I_P} \times \Delta T = \frac{V_{IN} - V_{OUT} - V_Q}{\Delta I_P} \times T_{ON}$$
$$= \frac{5-2.5-0.5}{200\times10^{-3}} \times 4.7\times10^{-6}$$
$$= 47\mu H$$

In order to avoid inductor saturation and achieve the best power efficiency, the material of the inductor core is recommended to be either in MPP or in iron powder and also inductance over 47μH should be applied.

- **Selection of capacitor**

I. Input capacitor:

The input capacitor is selected mainly on its ESR value and the RMS current rating, in order to support high current on an instant at input polarity. Low ESR capacitors may decrease input ripple and avoid the disturbance to other circuits in the system. In addition, a LC filter circuit can improve EMI in the power system.

II. Output capacitor:

Capacitance and ESR value are two major considerations for output capacitor. Capacitance must be able to deliver high loading current when the switch turns on. And ESR value is a main parameter in determining the output ripple, transient voltage and load impedance.

Thus the ESR of output capacitor is calculated as:

$$ESR = \frac{\Delta V_{RIPPLE}}{\Delta I_P} = \frac{50\times10^{-3}}{200\times10^{-3}} = 250m\Omega$$

ΔV_{RIPPLE}: desired output ripple voltage

The maximum output peak switch current:

$$I_{P(MAX)} = I_{O(MAX)} + \frac{\Delta I_P}{2} = 3 + \frac{200mA}{2} = 3.1A$$

The minimum capacitor value for a desired output ripple and load current:

$$C_{OUT(MIN)} = \frac{I_{P(MAX)}}{8\Delta V_{RIPPLE} F}$$
$$= \frac{3.1}{8\times50\times10^{-3}\times120\times10^{3}}$$
$$= 65\mu F$$

- **Selection of efficiency**

As shown in Fig. 9 and 10 for AIC1630A-2.5V application, the efficiency of N-MOS circuit is better than that of P-MOS circuit. Yet, some problems like MOSFET I^2R loss, inductor loss, feedback resistor loss, output capacitor ESR loss, sckottky diode loss, and switch loss, which have influence on MOSFET

efficiency, need to be concerned.

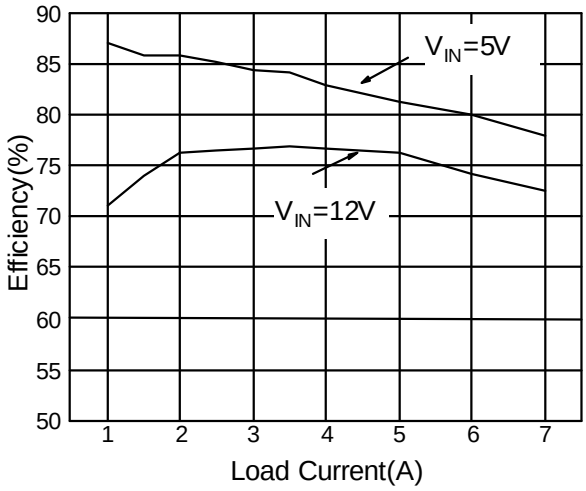

Fig. 9 Efficiency of N-MOS Circuit

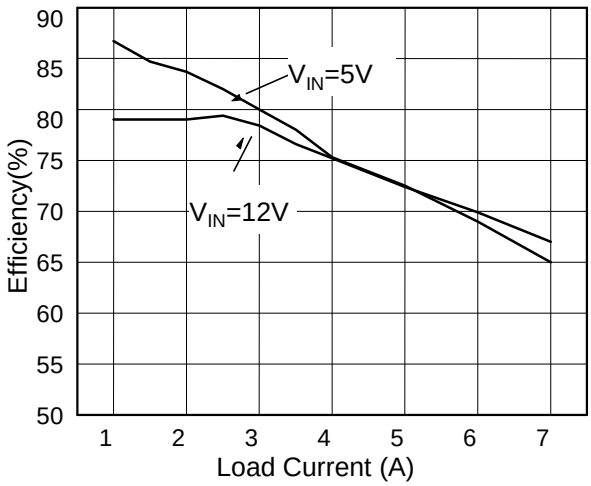

Fig. 10 Efficiency of P-MOS Circuit

(2) **LDO application**

The selecting of bipolar transistor or MOSFET depends on output current, power efficiency, and dropout voltage. However, a 100uF(or great) capacitor is required between the LDO output and ground for stability. Otherwise, the output polarity will oscillate. Most types of capacitors may work. Yet, when aluminum electrolytic type of capacitor is used its equivalent series resistor (ESR) should be 5Ω or less.

5. PCB Layout Guidelines

A recommended printed circuit board (PCB) layout for AIC1630A N-MOS application circuit is shown in Fig. 10, 11, and12. It is very important to place the bootstrapped circuit as close as possible to input line and source polarity of N-MOS. In order to achieve the best performance, the driven N-MOS circuit has to be placed as close as to the EXT pin of AIC1630A, too. A good layout practice is always the use of a separation layer of AIC1630A between power ground and signal ground. However, a small trace is connecting between power ground and signal ground to avoid power ground noise to affect signals of AIC1630A.

At higher load current (>1A), the size of metal traces and the placement of components have to be cautiously concerned. Note that high switch currents may cause voltage drops in long metal traces. In addition, short component leads may avoid unwanted parasitic inductance, which is a serious problem to EMI.

When low ESR capacitors fail to avoid the spikes at input/output polarities, application of input/output LC filters are recommended.

N-MOS

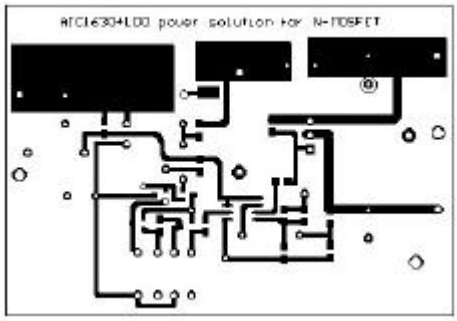

Fig. 11 Top Layer of AIC1630A

N-MOS

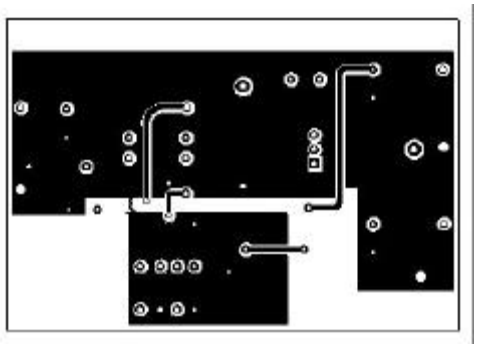

Fig. 12 Bottom Layer of AIC1630A

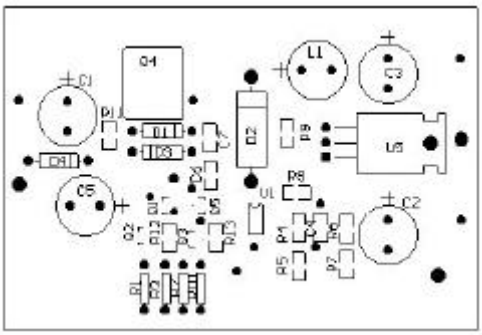

Fig. 13 Silk screen of AIC1630A N-MOS

Conclusion

Most low voltage microprocessors, DSPs, and PLDs use two power supplies of different voltages, such as V_{CORE} voltage and I/O voltage of graphic card. The use of dual voltage architecture often requires management of both voltages to avoid potential problems with device and system reliability. Users must consider the timing sequence between core and I/O during power switching operations.

Timing sequence for dual low voltage applications has grown rapidly. Also power IC's of two output voltages have been in great demand recently. AIC1630A+LDO provide V_{CORE} voltage and I/O voltage with power and solve the problems with different potentials.

AIC1630A+LDO of high efficiency and heavy load current can support a larger range of application fields. In addition, not only AIC1630A can be applied to step-up converter for high efficiency, but also it can be used as a step-down solution for different applications and requirements.