Active Chipset Reference Design Guide

Reference Guide

Literature Number: SLUUAS6
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Introduction

This document provides system design information for the Texas Instruments Active-Cell Balancing chipset. Use this reference design guide along with the data sheets for the devices listed in this document.

1.1 Conventions and Acronyms

This section describes the conventions and acronyms used in this document.

1.1.1 Conventions

'0' — Binary digit zero; a logic-low level (a low voltage for active-high logic, and a high voltage for active-low logic)

'1' — Binary digit one; a logic-high level (a high voltage for active-high logic, and a low voltage for active -ow logic)

"d…" — A binary number with more than one digit (d is 0-1)

d… — A decimal number (d is 0-9)

0xd… — A hexadecimal number (d is 0-F)

d..h — A hexadecimal number (d is 0-F)

k — kilo; 1000

K — kilo; 1024 (**Note**: this is not official SI usage)

b — bit

B — byte

1.1.2 Acronyms

ADC — Analog-to-Digital Converter

AFE — Analog Front-End

BMS — Battery Management System

BSP — Battery Stack Protection

CAN — Controller Area Network

DAC — Digital-to-Analog Converter

EEPROM — Electrically-Erasable Programmable Read-Only Memory

GPIO — General-Purpose Input Output

MCU — Microcontroller Unit

OC — Over Current

OV — Over Voltage

OVP — Overvoltage Protection

PWM — Pulse-Width Modulation

Stack — Series connection of cells managed by the BMS

SPI — Serial Peripheral Interface

UV — Under Voltage

UVP — Undervoltage Protection

1.2 Chipset Components

The core active balancing components are shown in Table 1-1.

Table 1-1. Active Chipset IC List

IC	Description	Quantity Required		Order Number
		Up to 7 cells	8 to 14 cells	
EMB1432	Analog front-end (AFE)	1	1	EMB1432QSQ
EMB1426	ADC	1	1	EMB1426QMM
EMB1428Q	Gate controller	1	2	EMB1428QSQ
EMB1499Q	PWM controller	1	2	EMB1499QMH
EMB1412	Gate driver	1	2	EMB1412MY
EMB1433	Battery stack protection	1	1	EMB1433QSQ

Additional components that are part optional are listed in Table 1-2.

Table 1-2. Active Chipset Optional Items

IC	Description	Quantity Required		Order Number
		up to 7 cells	8 to 14 cells	
EMB1420	Flyback controller (12 V)	1	1	EMB1420MM
EMB1437	12-V LDO	1	2	EMB1437MP
EMB1487	–5-V charge pump	1	1	EMB1487MM
EMB1466	Dual 5-V LDO	1	1	EMB1466MM
EMB1402	12-bit ADC (temperature sense)	1	1	EMB1402QMT

1.3 External Hardware Dependencies

An external microcontroller is typically used to initialize the EMB1432 and EMB1428Q, initiate new actions by these devices, and collect data from these integrated circuits. An external MCU can also be required to report data and provide a command, control protocol, or both on an isolated communications interface.

1.4 Microcontroller

A microcontroller is suggested to provide the peripheral interfaces and IO required to control the system. The required peripherals are:

- SPI
- Two DAC or timers with PWM output capability
- External communications interface for control command and measurement data
- Sufficient data memory for desired communications protocol layer and data buffering
- Sufficient non-volatile program memory for the system initialization routines, peripheral drivers, and control algorithms
- Non-volatile memory (Flash or external EEPROM) for system configuration and calibration parameters
- 14 or more GPIO (depending on cell count and system options, see Appendix C for a complete list of chipset interface signals)

Optional features included:

- Non-volatile memory (Flash or EEPROM) for long-term data log retention
- ADC for additional system fail-safe monitoring and/or temperature sensors with the pack
- Additional GPIO may also be required to control the power supplies if advanced features are required (see Appendix D)

The EM1401 Battery-Management System-Evaluation Board used the TI Stellaris® LM3S5R31-IQC.

TI recommends to also use an external reset controller to provide a reliable power-on and brown-out reset signal. The EMB1424MF is recommended.

1.4.1 Isolation

Any connection from battery modules to a central pack controller must be isolated to withstand the maximum working voltage of the entire pack in compliance with any system standards.

1.4.2 Transceivers

Transceivers can be required depending on the desired communications protocol, and in order to achieve robust, error-free communication.

System Critical Circuits

This section describes circuits that are global in nature and require more than one device in the chipset.

2.1 Zener Diodes

Zener diodes are must be placed close to the external battery connection on the system PCB, with one Zener diode across each cell. The Zener diodes are required for the system and serve two functions:

1. Provide overvoltage protection to the AFE inputs
2. Provide a path for in-rush currents during hot plug-in

Figure 2-1 shows the Zener-diode schematic and shows the direct connection to the battery connection header.

The Zener diodes must be selected to ensure the following conditions are met:

1. The EMB1432 and EMB1433 inputs are protected from input voltage transients and kept below 6 V.
2. The Zener current (I_z) at typical battery-cell voltage levels is as low as possible to keep the quiescent current low.

For example, the Zener diodes used in the active chipset reference schematic are 5.6 V, which has an Iz ≈ 7 µA at 4.2 V.

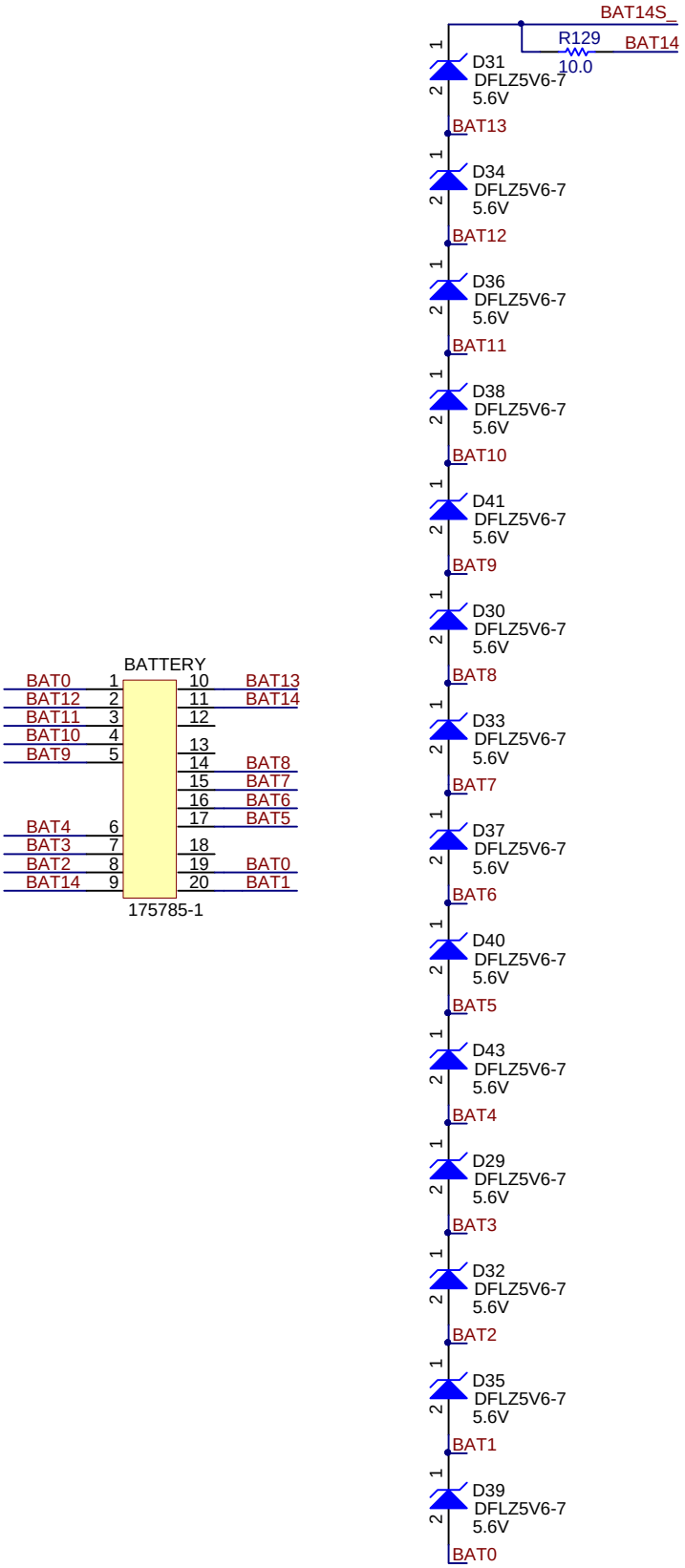


Figure 2-1. Zener Diode Schematic

2.2 In-Rush Protection

Protection circuits are required to limit the in-rush circuit which occurs when the battery connections are first made to the system. There are two circuits required in the system:

1. In-rush current-limit to protect the internal ESD-protection diodes in the EMB1432 and EMB1433 devices.
2. In-rush current limiting for the FET switch-matrix.

Figure 2-1 shows the in-rush current protection for the EMB1432 device. The in-rush current is identified as R129 on the EMB1432 BAT14 pin.

Limiting the in-rush current into the FET switch matrix which occurs when the system in first plugged in to battery pack is required. Figure 2-2 shows the schematic for this circuit. The basic operation occurs at first power-up when all in-rush current passes through R166 (22 Ω), until R166 is bypassed by the FET Q46. Before any active-cell balancing is enabled ,the system microcontroller is expected to enable Q46.

2.3 Battery Connection Fuses

For safety purposes, TI recommends using 8-A fuses on all cell connections. If a converter is employed for each half-stack of 7 cells, cell 7 requires a higher fuse value as cell 7 can be subjected to a total current of 10 A, with 5 A of current from the top-half stack and 5 A of current from the bottom-half stack. These fuses are shown as F1 through F15 in Figure 2-2.

2.4 Stack-Transient Suppression Diode

The transient suppression diode (TVS) is shown as D42 in Figure 2.

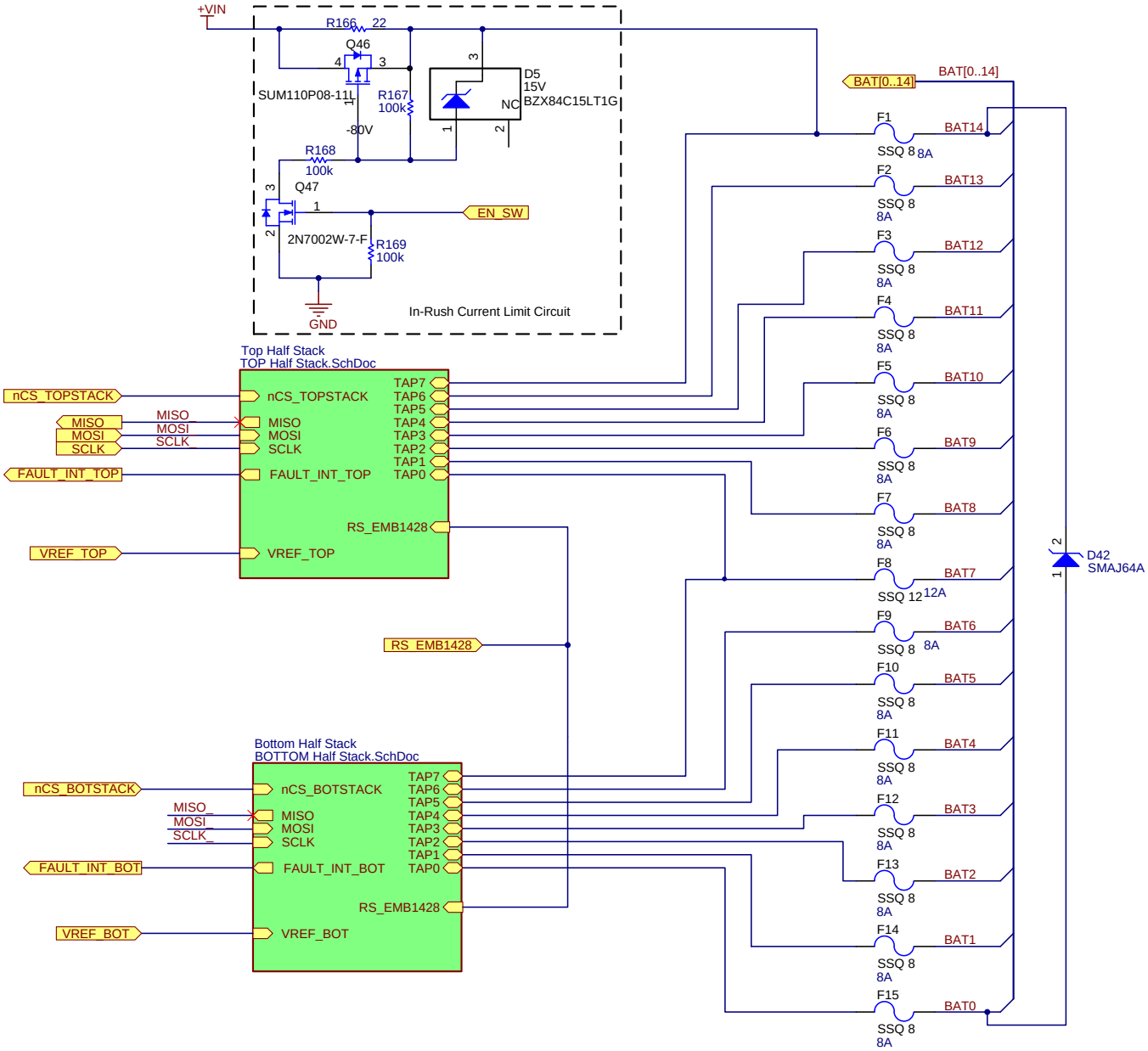


Figure 2-2. In-Rush Current-Limit and Battery Fuses Schematic

The EMB1432 analog front-end (AFE) is a high-voltage analog interface that monitors a lithium battery stack. The EMB1432 device selects and level shifts the voltage across any of the 14 stacked batteries plus the other two low-voltage auxiliary inputs which multiplexes the signals to an output pin.

3.1 Hardware Overview

Figure 3-1 shows the major stages of the AFE signal path. The battery-terminal voltage is first fed into a low-pass RC filter (user-defined Hz). The filtered differential signal is sent to a 14-channel AFE where the signal is buffered and level translated to the AFE ground. Finally an external ADC controlled by the microcontroller converts the signal to a 14-bit digital word.

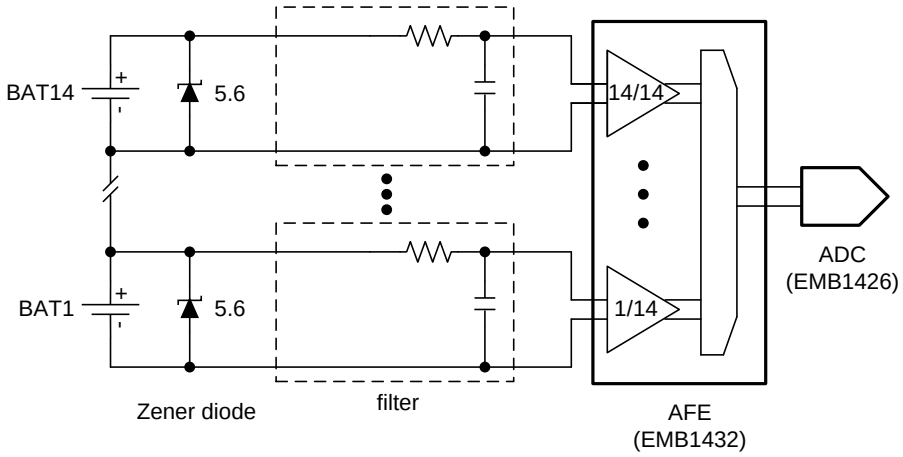


Figure 3-1. Battery-Cell Monitoring Simple Diagram

3.2 Interface Signals

The EMB1432 device is designed with two control interfaces. One of these interfaces is the Serial Peripheral Interface (SPI). The other is a proprietary IO-based interface (MUX[0:3]). The MUX line interface provides control of cell selection at a faster rate than the SPI allows. The proper MUX-pin configuration or SPI command to select any specific channel on the EMB1432 AFE is listed in the AFE-channel selection table in Appendix A.

Table 3-1 lists the interface signals required by the EMB1432 and the general requirements of the signals.

Table 3-1. EMB1432 Interface Signals

Signal	IC	Pin No.	Description	Type
CLK	EMB1432	43	SPI Clock	Microcontroller SPI peripheral or GPIO
MUX0	EMB1432	1	MUX selection bit 0	Microcontroller GPIO (output)
MUX1	EMB1432	48	MUX selection bit 1	Microcontroller GPIO (output)
MUX2	EMB1432	47	MUX selection bit 2	Microcontroller GPIO (output)
MUX3	EMB1432	46	MUX selection bit 3	Microcontroller GPIO (output)
nCS	EMB1432	42	SPI chip select	Microcontroller GPIO (output)
nRS	EMB1432	39	Reset (active low)	Microcontroller GPIO (output)

Table 3-1. EMB1432 Interface Signals (continued)

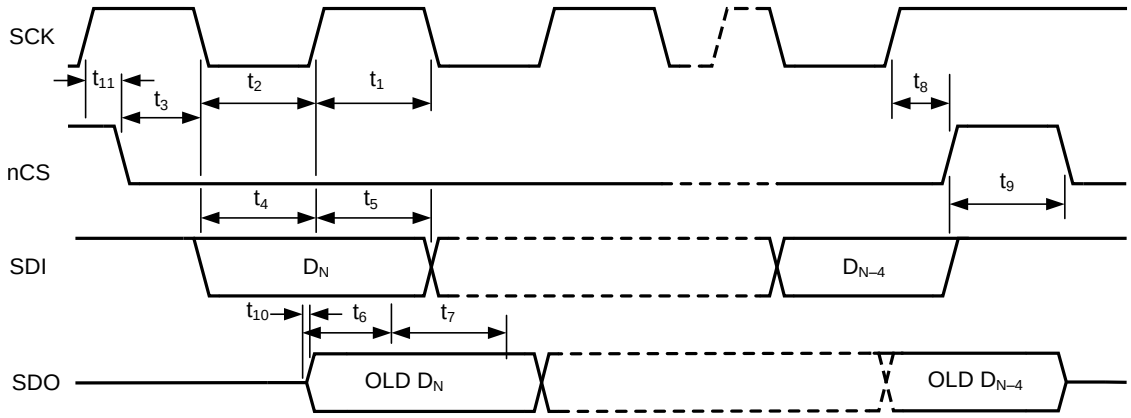
Signal	IC	Pin No.	Description	Type
nSD	EMB1432	40	Shutdown (active low)	Microcontroller GPIO (output)
SDI	EMB1432	41	SPI slave input	Microcontroller SPI peripheral MOSI or GPIO
SDO	EMB1432	44	SPI slave output	Microcontroller SPI peripheral MISO or GPIO

To maximize the speed of multiplexing the 14 battery inputs, the EMB1432 device must be in direct-multiplexer addressing mode. In direct-multiplexer addressing mode, multiplexing is controlled by four dedicated MUX lines (MUX0 through MUX3) rather than through the SPI interface. See the source selection table in Appendix A or the EMB1432 data sheet (SNOSB86) for each source address. When using the MUX line interface as the primary interface to the EMB1432 device, there is no access to AUX1 or AUX2 data. When using the SPI as the primary interface to the EMB1432 device, the MUX lines must be tied high.

If the primary communication method between the EMB1432 device and the system microcontroller is through Serial Peripheral Interface (SPI), this serial interface can be configured in a variety of standard ways.

The recommended host-SPI peripheral settings for the EMB1432 device are:

1. CPOL = high (CLK high when idle)
2. CPHA = 2nd clock edge (The second clock transition is the first data capture edge)
3. Data-bit order = most-significant bit first



Where:
D_N = B3, D_{N-1} = B2, D_{N-2} = B1, D_{N-3} = B0, D_{N-4} = FB

Figure 3-2. Basic-AFE SPI Timing Diagram

Battery input channels can be selected in any order. However, most applications scan through all channels in order to get a *snapshot* of the battery-pack cell voltages. When implementing a scan of all channels, because of the internal design of the EMB1432 device, TI recommends to scan from the highest channel to the lowest channel.

The fastest rate at which battery-cell data is read accurately from the EMB1432 device is dependent in part on the ADC timing characteristics and the external RC-filter components implemented along with the chosen ADC (EMB1426). Because the EMB1426 device is a sample-and-hold ADC, to minimize the delay associated with selecting a new AFE channel, TI recommends to make the channel selection as soon as possible after the start of conversion. This quick selection allows the ADC filter for the data of the next channel to stabilize while the data of the previous channel is converted. A stable ADC input at the beginning of conversion is essential.

3.3 Open-Wire Sense

Setting the force current bit to 1 (FB=1) sinks 100 µA from the negative terminal of the selected node which allows for a fast settling of any node left floating (broken wire to the battery stack). Next, a typical mode reading of the 14 cells is able to detect a broken wire through the finding of one below-minimum-voltage cell adjacent to one exceeding the maximum voltage.

The FB bit is only configurable when controlling EMB1432 through the SPI interface.

3.4 Power Supply Requirements

The –5 V can be supplied with the internal charge pump or with an external supply. To achieve the most accurate results an external precision –5-V supply must be implemented. Special care must be taken to keep this supply as noise free and isolated from other switching circuits as possible.

The voltage reference and EMB1432 (VP) device must be on a clean 5-V power supply, shared only with the EMB1426 (VA) device. VIO must be the same supply used by the microcontroller and can be 2.7 V to 5.5 V.

3.5 EMB1432 Circuit Schematic

Figure E-2 shows the schematic for the AFE circuit. The EMB1432 in the provided schematic is setup to use an external –5-V supply and the internal charge pump is disabled. The following devices are shown in the schematic:

- EMB1432
- EMB1426 (see Section 3.8)
- REF5025 (see Section 3.8.2)

3.5.1 Front-End In-Rush Protection and RC Filter

The series resistors on the EMB1432 sense inputs (R1 to R15 in the schematic provided in Figure E-2) are required by the system and serve two functions:

1. The series resistors protect the AFE inputs from in-rush currents during hot plug-in. This requirement limits the input series R to a minimum of 100 Ω. This resistance must be kept as low as possible to minimize input voltage offset which can also be subject to drift over temperature. For this reason, they must be kept below 1 kΩ.
2. Together with the capacitors on each input the series resistors provide an RC filter for high-frequency noise on the AFE inputs. The tuning of this filter cutoff is up to the customer and the noise which canbe present in the end application.

3.5.2 AFE Output RC Filter

To maximize measurement accuracy the AFE output needs to settle within less than one-half of the ADC LSB. As a worst case, the AFE output moves the full-range that is possible in the system. The full-range is 4.2 V when the AFE output is coming up on the first cell, when very high ADC sample rates are desired, when there are extreme imbalance conditions, or when there is a broken cell-sense connection.. The RC filter must be tuned to allow the AFE output to settle before the ADC sample is taken. TI recommends to allow up to 11 RC time-constants. However, in typical conditions where cell to cell variation will only be within 100 mV, the AFE output does not require as much time to settle, therefore only the first cell sampled requires the extra time allowed to let the AFE output settle.

3.6 AFE Calibration

To provide maximum accuracy, the system is not required to be factory calibrated for voltage offset and gain on each input channel. The system is required to be calibrated with accurate voltage references applied to the battery connection input. In the end application the user can also have an external wire harness attached to the battery connection header which is in between the system and the target cells. The battery harness presents a small series resistance to the connection from the target cell and the system AFE. There are small leakage currents because of the onboard circuits. These circuits present a small additional error offset because of this additional external resistance in the AFE-to-cell connection. The following procedure lists the steps to adjust the calibration offsets in order to return accuracy to the system.

The method to adjust the AFE offset calibration is as follows:

1. Read current cell measurement from the system.
2. Take measurement at the cell with external precision meter and calculate difference from system measurement.
3. Write AFE offset calibration value found in previous step to a non-volatile data memory area (Flash or EEPROM).
4. Repeat this procedure for all channels.
5. Apply the stored calibration value to all cell measurements.

3.7 EBM1432 PCB Layout Guidelines

To ensure the best possible accuracy performance, TI recommends to follow some basic layout guidelines for the EMB1432 AGND and RGND signal planes. The planes can be on the same layer as the GND plane for the rest of the board, as long as they are separated and connected as close to BAT0 as possible. For a description of the EMB1432 AGND and RGND signals and connections see the schematic in Figure E-2.

Figure 3-3 shows a basic diagram of the AGND and RGND planes and the star connection at the battery-connection header (BAT0 pin) to the GND plane. AGND and RGND must be on different layers.

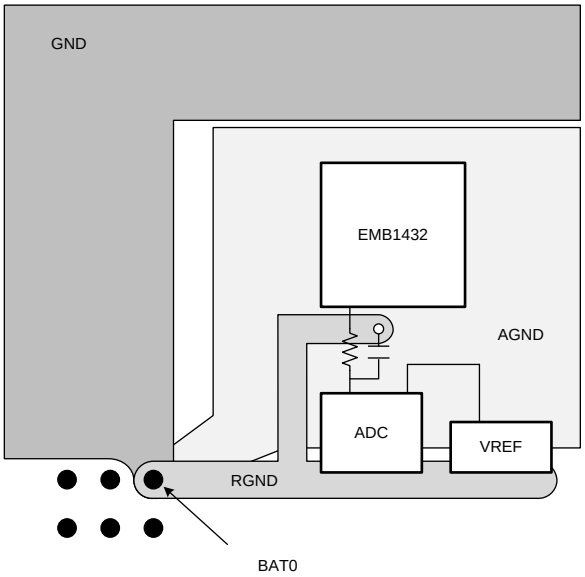


Figure 3-3. AFE AGND and RGND Layout Example

3.8 EMB1426 ADC

3.8.1 Hardware Overview

A 14-bit ADC (EMB1426) is employed to achieve the highest possible voltage measurement accuracy.

3.8.2 ADC Voltage Reference

The important voltage-reference electric-characteristic parameters have been, from experience, the regulation performance over the temperature range and the long-term drift performance. Stability is critical.

The recommended precision voltage reference is the REF5025 device from TI. The schematic in Figure E-2 includes the circuit required for the recommended voltage reference.

3.8.3 REF5025

Temperature drift: down to 3 ppm/°C (maximum)
Accuracy: 0.05% (maximum)
Noise: 3 µVPP/V

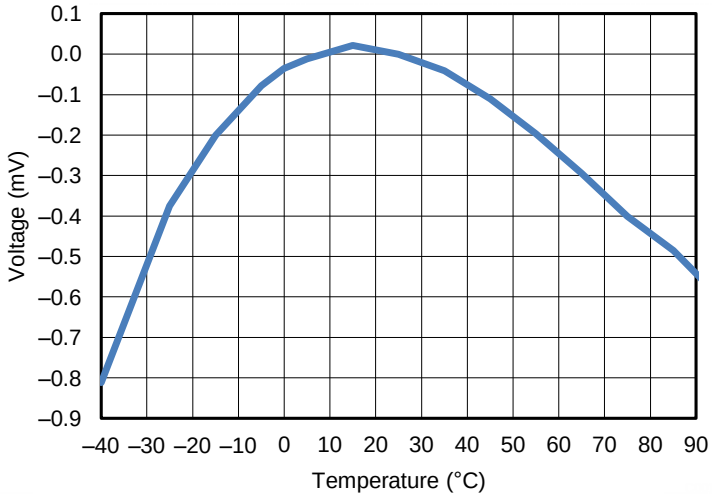


Figure 3-4. Reference Output Versus Temperature (Measured)

3.8.4 Interface Signals

Table 3-2 lists the interface signals required by the EMB1426 device and the general requirements of the signals.

Table 3-2. ADC Interface Signals

Signal	IC	Pin No.	Description	Type
CLK	EMB1426	8	SPI Clock	Microcontroller SPI peripheral or GPIO
nCS	EMB1426	6	SPI chip select	Microcontroller GPIO (output)
SDO	EMB1426	7	SPI slave output	Microcontroller SPI peripheral MISO or GPIO

The recommended host SPI peripheral settings for the EMB1426 device are:

1. CPOL = high (CLK high when idle)
2. CPHA = 2nd clock edge (The second clock transition is the first data-capture edge)
3. Data-bit order = most-significant bit first

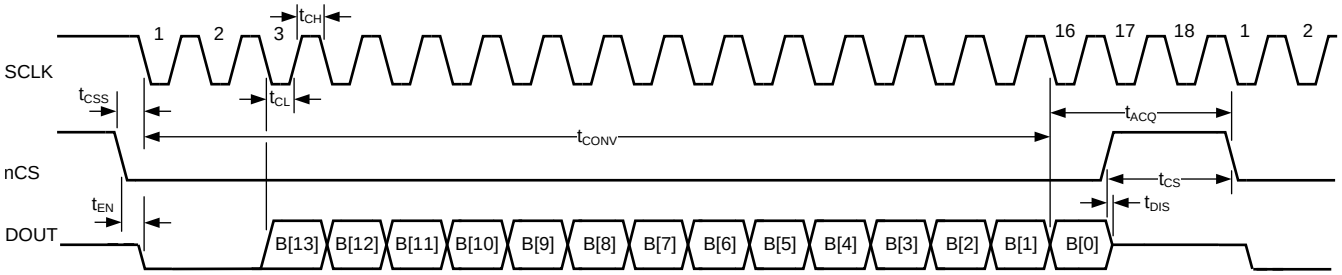


Figure 3-5. Basic-ADC SPI Timing Diagram

3.8.5 Power Supply Requirements

The voltage reference and EMB1426 (VA) device must be on a clean 5-V power supply, shared only with the EMB1432 (VP) device. VIO must be the same supply used by the microcontroller and can be 2.7 to 5.5 V.

3.8.6 Circuit Schematic

The schematic in Figure E-2 includes the ADC and voltage reference circuits.

3.8.7 PCB Layout Guidelines

The ADC is included in the PCB layout guidelines shown in Figure 3-3.

EMB1433 Battery-Stack Protection

4.1 Hardware Overview

The EMB1433 device is a protection chip that provides an additional layer of safety to the regular battery stack voltage acquisition chain. The EMB1433 device can monitor a stack of six to 14 cells, with a maximum of 60 V at the top of the stack and can support a battery pack architecture comprised of multiple modules. The EMB1433 device functions are independent from the main acquisition path, providing a layer of redundancy to the battery system. An internal flag signal is asserted any time that either one or more cells of the stack are outside a *safety*-voltage window (under voltage, over voltage) or the voltage on the positive terminal of the external thermistor connected to the pin AUX exceeds a customer selectable threshold.

4.2 Configuration

There are several external components that must be configured to properly evaluate with a user's battery pack architecture. The following lists the features that must be configured.

- Setpoint thresholds for:
  - HTH: over voltage (OV)
  - LTH: under voltage (UV)
  - AUXTH: over temperature (OT)
- Thermistor compensation pull-down
- Number of cells
- Top module ID
- Mask delay

4.2.1 Set-Point Thresholds

The EMB1433 device has built-in comparators for OV, UV, and auxiliary (AUX). AUX is typically used for OT. The threshold set points are configured by external resistor dividers, as shown in Equation 1.

$$\text{Threshold} = \frac{4.5\ \text{V} \times \text{R1}}{\text{R1} + \text{R2}} \quad (1)$$

where

- R1 is equal to the following:
  - OV = R135
  - UV = R132
  - OT/AUX = R139
- R2 is equal to the following:
  - OV = R136
  - UV = R133
  - OT/AUX = R140

Figure E-3 shows he external circuit containing these values. Table 4-1 lists the default values for each threshold.

Table 4-1. Default Threshold Values

Threshold	Description	R1	R2	Set Point
OT/AUX	Over temperature	17.7 k	10.2 k	2.85 V
OV	Over voltage	51 k	10.7 k	3 V
UV	Under voltage	8.2 k	10.2 k	2 V

4.2.2 Thermistor Compensation

The NTC thermistor is attached to the AUX input, and R128 provides a compensation pulldown to form the voltage divider for the temperature voltage input. R128 must be set as needed by the thermistor selected by the user to match the voltage set by the R139-R140 divider for the desired temperature. Equation 2 calculates the pulldown (R128) value for a given thermistor.

$$\text{Voltage at temp} = \frac{4.5\ \text{V} \times \text{R128}}{\text{R128} + \text{Rt}} \quad (2)$$

where

- Rt is the thermistor resistance at the desired temperature threshold

With the default values of R139-R140 (shown in Table 4-1), the overtemperature threshold is 2.85 V. A 103JT thermistor at this threshold is at approximately 40°C, and a 104JT is at approximately 98°C.

4.2.3 Number of Cells

The EMB1433 device monitors six to 14 cells and is configured by setting the CELLN[3:0] inputs with external resistors. The pullup resistors are R115, R117, R119, and R121. The pulldown resistors are R199, R255, R256, and R257.

CELLN[3:0] must set as shown in Table 4-2.

Table 4-2. Cell Number Configuration

Monitored Cells	CELLN_3	CELLN_2	CELLN_1	CELLN_0
14	1	0	0	0
13	0	1	1	1
12	0	1	1	0
11	0	1	0	1
10	0	1	0	0
9	0	0	1	1
8	0	0	1	0
7	0	0	0	1
6	0	0	0	0

4.2.4 Mask Delay

Before a fault is reported the UV, OV, and OT conditions are filtered to avoid a false, or unwanted, fault assertion determined by glitches and spikes on input voltage which are common in a noisy environment as the battery pack is. The amount of filtering can be programmed with an external pin C_{EXT} where an external capacitor proportional to the amount of the desired *mask time* must be connected.

C_{EXT} = 100 pF provides approximately 3-ms mask delay. This value can be multiplied to get an appropriate C_{EXT} value for the user's application.

4.3 Interface Signals

Table 7 lists the interface signals required by the EMB1433 device and the general requirements of the signals.

Table 4-3. EMB1433 Interface Signals

Signal	IC	Pin No.	Description	Type
HEART	EMB1433	2	1-Wire Fault Communication Channel	Microcontroller watchdog timer peripheral or GPIO
PING_LS_IN	EMB1433	47		Microcontroller SPI peripheral MISO or GPIO
PING_LS_OUT	EMB1433	48		Microcontroller GPIO (output)

4.3.1 HEART — 1-Wire Fault Communication Channel

The fault communication channel allows for the communication of a fault occurrence with no extra galvanic isolation component. The fault communication channel consists of a 0.2-mA current mode heart-beat signal which is sourced from the pin DOUT_LS downwards to the next level module DIN_LS. The heart beat is a 730-Hz low duty-cycle (6.7%) signal used to reduce power consumption.

The current signal is unidirectional and propagates from the top module downwards. When there are no faults detected by the adjacent higher level module, the EMB1433 device on each module receives the 0.2-mA heart-beat signal on the DIN_LS pin. If the EMB1433 device detects a fault on its own module or detects no signal coming from the next high-side module (either for a fault on any higher level module or for a broken wire), the EMB1433 device stops generating or re-transmitting the heart-beat sourcing current from its own DOUT_LS to lower modules.

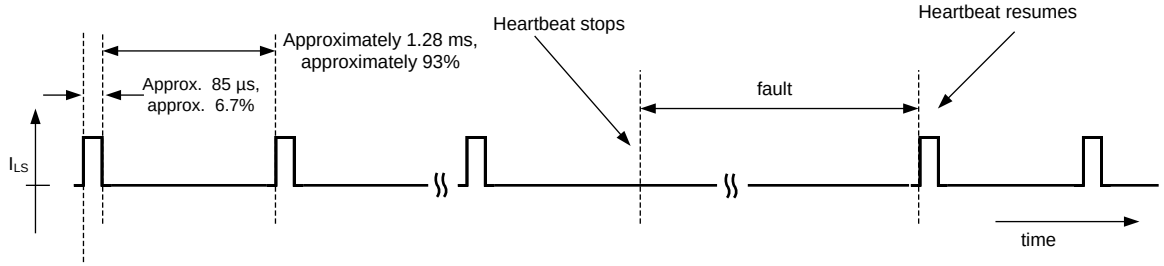


Figure 4-1. HEART Signal Diagram

The dedicated HEART pin allows for direct interface of the external pack controller to the bottom module sitting at ground level. The external pack controller must embed an internal watchdog to capture a fault event which is encoded on the HEART pin as an interruption of the normal beat activity.

The external pack-controller watchdog timer must be chosen taking into account the tolerance of the internal oscillator frequency of the EMB1433 device because this is used for the heart-beat signal generation as well as the jitter that can be induced along the chain. Refer to the f_{HTB} parameter in the EMB1433 data sheet (SNVS786). A watchdog time of 3 ms (or more) is recommended.

4.3.2 PING Bus

Once a fault is indicated by the lack of a pulse on the HEART output, the specific fault is found by using the PING bus. Fault Information is presented at PING_LS_OUT pin after a falling edge in detected by the EMB1433 device on the PING_LS_IN input pin. Figure 4-2 shows the PING fault output frame output on PING_LS_OUT.

The ping communication consists of 10 bits sent in sequence as follows:

- Start bit (same as zero bit)
- 3 bits for transmitting the fault status: OV, UV, and OT
- 4 bits for transmitting the faulty cell number
- 1 bit for parity
- Stop bit (same as one bit)

Nominal bit width is equal to 21 µs. The start bit or a zero bit value for OV, UV, or OT is indicated by a 25% duty cycle signal. Nominal logic 0 width is equal to 5.3 µs. The stop bit or a one-bit value for OV, UV, or OT is indicated by a 75% duty cycle signal. Nominal logic 1 width is equal to 16 µs. Each bit takes four time-units to transmit and is generated using an internal 375-kHz oscillator. The number of internal oscillator-clock periods per time-unit is eight.

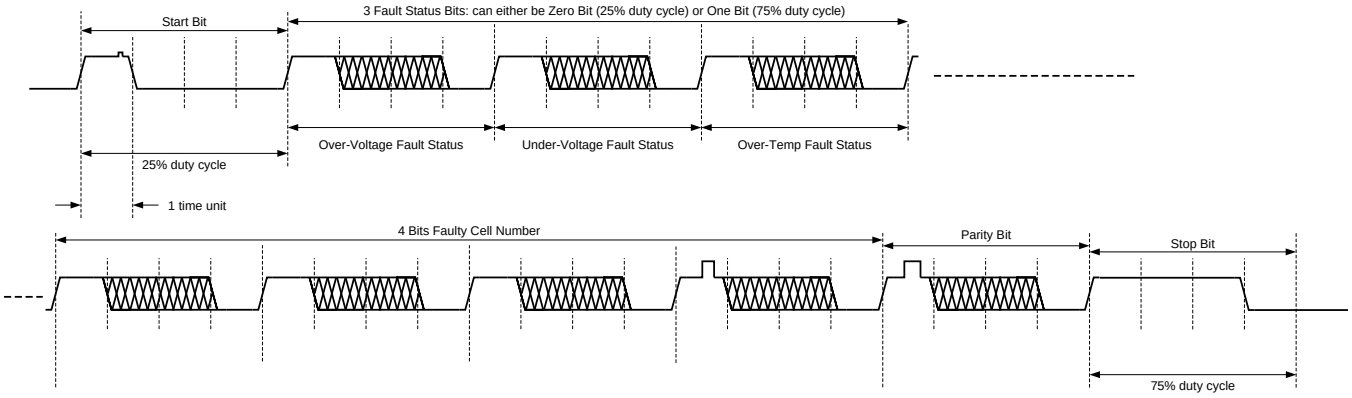


Figure 4-2. PING Fault-Bus Frame

Parity is calculated based on the 8 bits in the frame excluding start and stop bits. The bits are the three fault-status bits, the four cell-number bits, and parity itself. Odd parity is used.

An OV or UV fault also includes the cell channel number at fault. In the case of an OV and UV fault being simultaneously present, the cell-channel number output is valid for the OV fault. Table 4-4 lists the cell number mapping.

In the case of an OT (AUX) fault, the cell-channel number is invalid.

Table 4-4. Error-Cell Number Mapping

Faulty Cell Number	4-bit Cell Number
1	0000
2	0001
3	0010
4	0011
5	0100
6	0101
7	0110
8	0111
9	1000
10	1001
11	1010
12	1011
13	1100
14	1101
Reserved	1110
Reserved	1111

4.3.3 Example 1

For example 1, assume that a module is faulty with both over voltage (cell number 5) and over temperature. In this case the following is transmitted:

0 101 0100 0 1

- 0 = start bit,
- 101 = over voltage, no under voltage, over temperature
- 0100 = cell number 5
- 0 = parity Bit
- 1 = stop bit

4.3.4 Example 2

In case of no fault, the following is transmitted:

0 000 xxxx y 1

- xxxx: ranges from 0000 to 1101
- y: parity bit
- If fault = 000 and channel = 0000, parity is 1 → 0 000 0000 1 1
- If fault = 000 and channel = 0001, parity is 0 → 0 000 0001 0 1

4.4 Power Supply Requirements

The –5 V is supplied with the internal charge pump or with an external supply. Use of the internal –5-V supply yields adequate results, however for extremely accurate results an external precision –5-V supply can be implemented. Special care must be taken to keep this supply as noise free and isolated from other switching circuits as possible.

VIO must be the same supply level used by the external pack controller and can be 2.7 to 5.5 V.

4.5 Single-Supply Operation

The EMB1433 has an internal charge pump which supplies the required negative voltage to the device. The internal charge pump requires a fly capacitor between CHP and CHM and a storage capacitor between CHPVM and GND and tie the negative supply pin VM to CHPVM. To enable the internal charge pump, tie CHPnSD to VP. If CHPnSD is connected to GND the internal charge pump is disabled. TI recommends to connect the bypass capacitors on CHPVP and the storage capacitor on CHPVM to the DGND pin. The 100-Ω resistor across CHPVM and VM is optional (can be replaced by a short) but TI recommends to filter the charge pump switching noise.

4.6 Circuit Schematic

Figure E-3 shows the schematic for the EMB1433 circuit. The circuit gated by Q56 simply detects the presence of BAT14, 5VD, and –5 V. When 5VD and –5 V are present the connection of PING_IO_LS and DOUT_LS (Q52 and Q53 respectively) are enabled. When the module is configured as the top module (TOP_DRV is connected to 3V3) Q60 connects PING_IO_HS to BAT14.

4.7 PING Header Connections

The PING_IN and PING_OUT headers shown in the EMB1433 circuit schematic (see Figure E-3) must be connected in the following manner for different positions in the battery pack.

- PING_OUT (bottom module)
  - pin 7 (HEART) connects to the external pack controller
  - pin 6 (LS_IN) connects to the external pack controller
  - pin 5 (LS_OUT) connects to the external pack controller
  - pins 1-4 and pin 8 are not connected
- PING_OUT (all higher modules)
  - pin 7 (HEART) is not connected
  - pin 6 (LS_IN) is not connected
  - pin 5 (LS_OUT) is not connected
  - pin 4 connects to the adjacent lower modules PING_IN pin 1
  - pin 3 connects to the adjacent lower modules PING_IN pin 2
  - pin 1 and pin 2 are not connected
- PING_IN (top module)
  - pin 4 (TOP-DRV) connects to pin 3 (3V3)
  - pin 1 and pin 2 are not connected
- PING_IN (all lower modules)
  - pin 4 and pin 3 are not connected
  - pin 2 connects to the adjacent higher modules PING_OUT pin 3
  - pin 1 connects to the adjacent higher modules PING_OUT pin 4

4.8 PCB Layout Guidelines

The PCB layout guidelines for the EMB1433 device are similar to the EMB1432 device. The AGND and RGND signal planes can be on the same layer as the GND plane for the rest of the board, as long as they are separated and connected as close to BAT0 as possible. The EMB1433 and EMB1432 AGND planes can be shared. See the schematic in Figure 4-3 for a description of the EMB1433 AGND and RGND signals and connections.

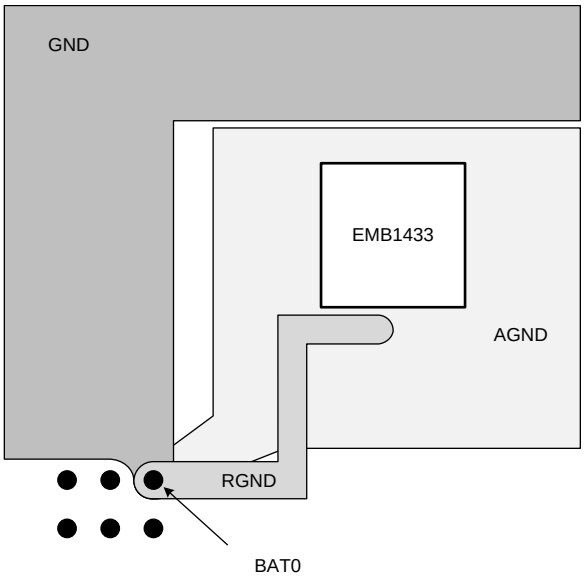


Figure 4-3. EMB1433 AGND and RGND Layout Example

Active-Cell Balancing (ACB) Architecture

5.1 Hardware Overview

A switch-matrix gate controller (EMB1428Q) and isolated DC-DC PWM controller (EMB1499Q) are provided for each group of cells up to 7, and each can be individually controlled. The typical BMS module manages up to 14 cells, so two cells can be simultaneously charged or discharged.

The chipset combination of the EMB1428Q and EMB1499Q devices is controlled by a single command through SPI.

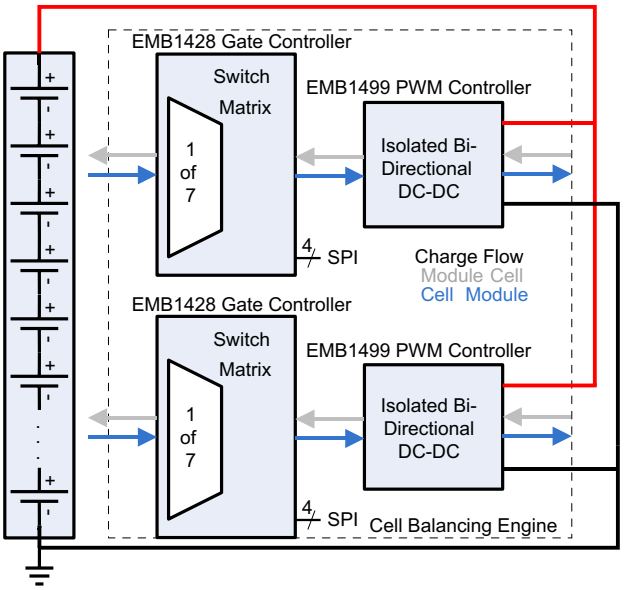


Figure 5-1. Simplified Cell-Balance Block Diagram

The switch matrix uses dual 40-V FETs in series with each positive and negative terminal of the battery. The source of each dual FET is connected such that there is no conduction path through the body diodes. In addition to the dual FETs in series with each battery, four FETs are used to route the converter to the top and bottom of the selected battery.

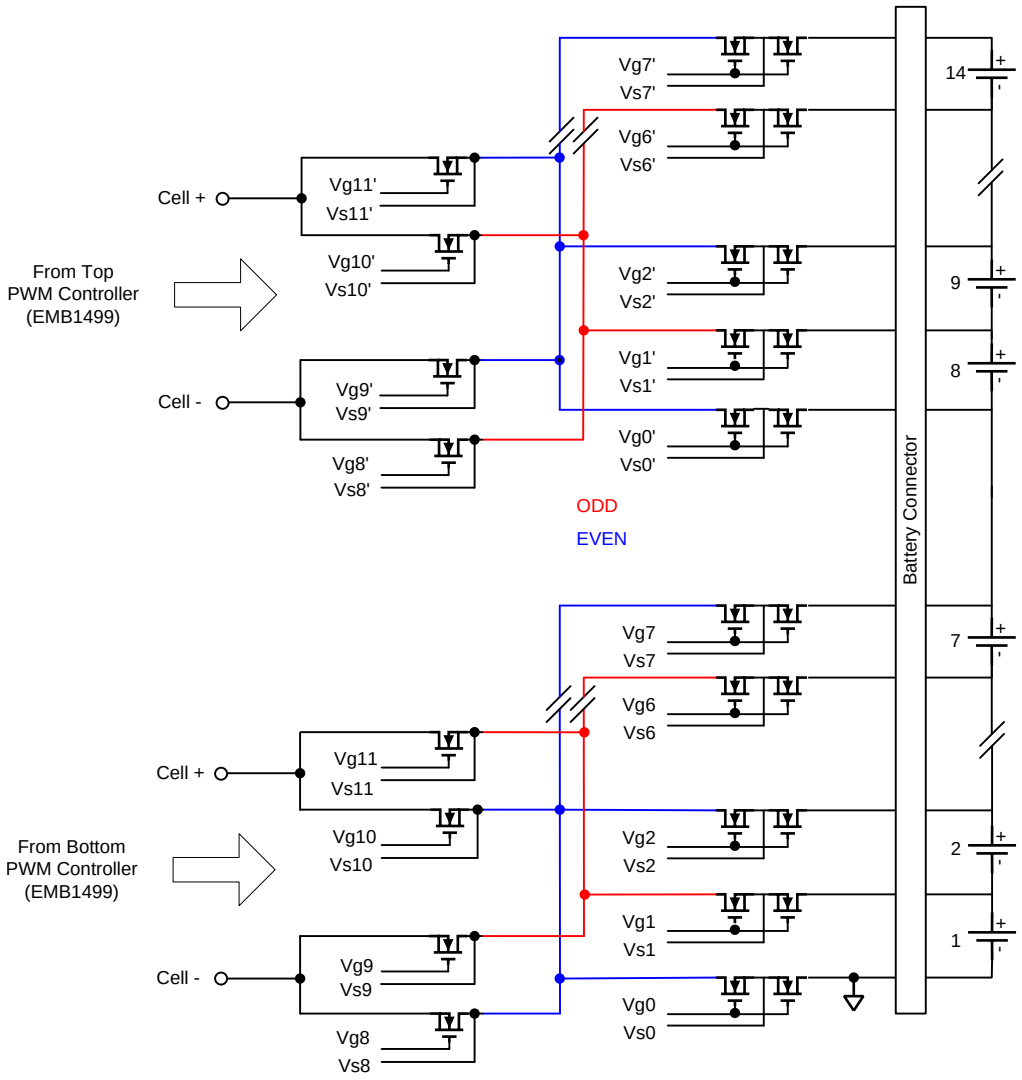


Figure 5-2. Cell-Balancing Simplified Diagram

The EMB1428Q device is a 12-channel floating NFET driver that is designed specifically for BMS systems. The primary role of the EMB1428Q device is to automatically select multiple switches based on an input of a simple cell selection command from the microcontroller. For example, selecting cell 1 (bottom half-stack cell 1) activates bottom EMB1428Q Vg1 and Vg0, and Vg11 and Vg8. Selecting cell 14 (top half-stack cell 7) activates top EMB1428Q Vg7' and Vg6', and Vg10' and Vg9'. This device also serves as a communication bridge between the microcontroller and the EMB1499Q PWM controller. The EMB1428Q device also passes fault information from the EMB1499Q device to the system microcontroller.

The EMB1499Q device is specially designed to control the active-clamp forward topology with the ability to control the charge current in both directions (sink or source).

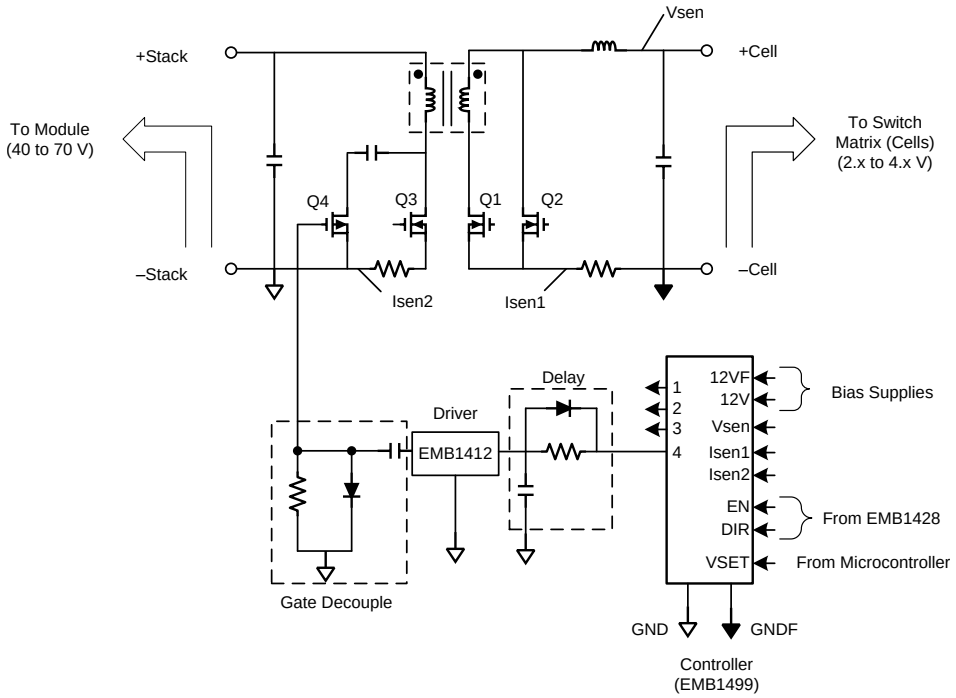


Figure 5-3. PWM-Controller Simplified Diagram

5.2 Interface Signals

Table 5-1 lists the interface signals required by the EMB1428Q and EMB1499Q devices and the general requirements of the signals.

Table 5-1. EMB1428Q and EMB1499Q Interface Signals

Signal	IC	Pin Number	Description	Type
CS[(1)]	EMB1428Q	30	SPI chip select	Microcontroller GPIO (output)
FAULT_INT[(1)]	EMB1428Q	31	Fault interrupt source	Microcontroller GPIO (interrupt input)
RESET[(1)]	EMB1428Q	35	Reset (active high)	Microcontroller GPIO (output)
SCL_C	EMB1428Q	27	SPI clock	Microcontroller SPI peripheral or GPIO
SDI	EMB1428Q	28	SPI slave input	Microcontroller SPI peripheral MOSI or GPIO
SDO	EMB1428Q	29	SPI slave output	Microcontroller SPI peripheral MISO or GPIO
VSET	EMB1499Q	6	Current set point	Microcontroller DAC or PWM (with low-pass filter) output
Inrush limit bypass	Q46[(2)]		Enables FET bypass of in-rush limit circuit	Microcontroller GPIO (output)

(1) Two of these interface signals are required for both bottom and top half-stacks if design includes more than 7 cells.
(2) Q46 is described in Section 2.2.

The primary communication method between the EMB1428Q device and the system microcontroller is through Serial Peripheral Interface (SPI). This serial interface can be configured in a variety of standard ways.

The recommended host SPI peripheral settings for the EMB1428Q device are:

1. CPOL = low (CLK low when idle)
2. CPHA = 1st clock edge (The first clock transition is the first data capture edge)
3. Data-bit order = most-significant bit first

The serial interface operates on 8-bit transactions. The microcontroller must send a 4-bit command on SDI followed by four zeros. The EMB1428Q device provides FAULT[3:0] on SDO, followed by the 4-bit command that was previously received. The EMB1428Q device drives SDO on the falling edge of SCL_C and samples SDI on the rising edge of SCL_C. If nCS goes high at any point before the eighth rising edge of SCL_C, the transaction is considered aborted and the data that was received on SDI is discarded. No command change occurs from such a transaction. However, if FAULT_INT was cleared by the transaction, it remains cleared and the fault data is no longer accessible. See the device data sheet (SNVS812) for AC timing specifications.

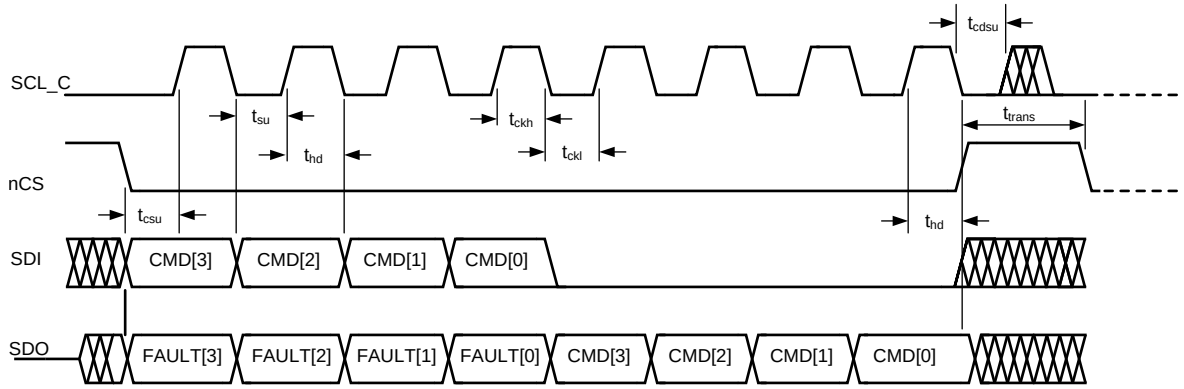


Figure 5-4. EMB1428Q SPI Timing Diagram

The EMB1428Q SPI drivers are optimized for a maximum interface speed of 1 MHz. Because SPI can be configured to operate at speeds higher than this rate, care must be exercised to configure SPI properly to limit the interface rate. Failure to properly limit the interface speed can result in bit errors during communication.

The EMB1428Q device controls the EMB1499Q device with a digital I/O interface. All communication between the EMB1428Q and the EMB1499Q devices originates from the EMB1428Q device, and the EMB1428Q device initiates this communication only in response to SPI commands received from the system microcontroller.

5.2.1 EMB1428Q Commands Codes

The channel selection and charge transfer direction are combined into a single SPI command byte sent from the microcontroller to the EMB1428Q device (which then controls the DIR and EN pins of the EMB1499Q device after having selected the desired channel). The command to the EMB1428Q device is a single byte of data. Bits 7 to 4 of this data byte control the channel selection and current charge transfer direction, whereas bits 3 to 0 of this data byte must be zero. Bit 7 controls the charge transfer direction (0 for charge, 1 for discharge), and bits 4 to 6 sets the channel selection (001 = channel 1, 010 = channel 2, to 111 = channel 7) or disconnects all channels (0000 = STOP or open all channels). Appendix B lists the commands.

NOTE: The EMB1499Q device has a built-in safety timer which expires in 8 seconds.

Once a command to start a charge or discharge current transfer has been sent to the EMB1428Q device, and the EN and DIR signals to the EMB1499Q device have been set, the transfer can be cancelled in one of two ways:

1. STOP command
2. EMB1499Q time-out

Sending the STOP command stops the EMB1499Q device and disconnects the EMB1428Q device from all cell channels. A STOP command must be sent to the EMB1428Q device before 8 seconds have elapsed.

For current transfers longer than 8 seconds, the user must send a STOP command followed by a START command (after t_{trans} — see EMB1428Q data sheet, SNVS812), in a period of less than 8 seconds.

Alternately, the EMB1499Q device can be allowed to time-out using its built-in 8-second timer. However, if the EMB1499Q device is allowed to time-out, the EMB1499Q device generates a fault which causes the EMB1428Q FAULT_INT line to be asserted and the device must be reset (by toggling the EMB1428Q RESET signal) before a new command can be sent for a subsequent cell selection and charge or discharge.

When the EMB1499Q device has ramped the output current down to zero, the DONE output is set which communicates to the EMB1428Q device that a new command can be accepted.

5.2.2 EMB1499Q Fault Codes

Fault Codes (or lack of any faults) are reported by the EMB1499Q device to the EMB1428Q companion IC through the FAULT[2:0] pins of the EMB1499Q device, which connect to the FAULT[2:0] pins on the EMB1428Q device. The codes which appear on the FAULT[2:0] pins of the EMB1428Q are translated into codes reported through SPI back to the microcontroller.

5.2.3 FAULT Generation and Reporting

The response from the EMB1428Q device after having communicated with the EMB1499Q through the I/O pins is also a single byte of information. This single byte contains the FAULT code (or lack of fault, as the case may be) associated with the previous command concatenated with the channel or direction command that was just sent to the EMB1428Q device to initiate the communication. The response byte contains the FAULT code in bits 4 to 7, and the channel selection/direction command in bits 0 to 3. The possible FAULT codes can be seen in Appendix B.

For example, if the application selects channel 5 for charge, the microcontroller sends 05h to the EMB1428Q device. If there was no fault in carrying out the command, the EMB1428Q device responds with, A5h. A request to discharge channel 3 is sent as 0Bh, and if there was no fault in carrying out the command the response to this command is ABh.

5.2.4 Sleep Mode

The EMB1428Q enters sleep mode when any of the following methods are applied:

- A STOP command is received
- The RESET pin is held high
- The RESET pin is toggled high then low

There are several conditions which, if present, the EMB1428Q device does allow any switches to be closed. These include:

- Insufficient VDDCP to VSTACK voltage
- Insufficient supply voltage on an individual floating driver rail
- Loss of the VDD_5V or VDD_12V supply
- The following illegal combinations of gate driver output are detected:
  - More than 2 bits of Vg[7:0] are set
  - Two non-consecutive bits of Vg[7:0] are set
  - (Vg11 | Vg8) and (Vg10 | Vg9)

5.2.5 Example Flow

The following flow charts (see Figure 5-5 and Figure 5-6) describe the basic relationship of commands and faults in the EMB1428Q and EMB1499Q devices.

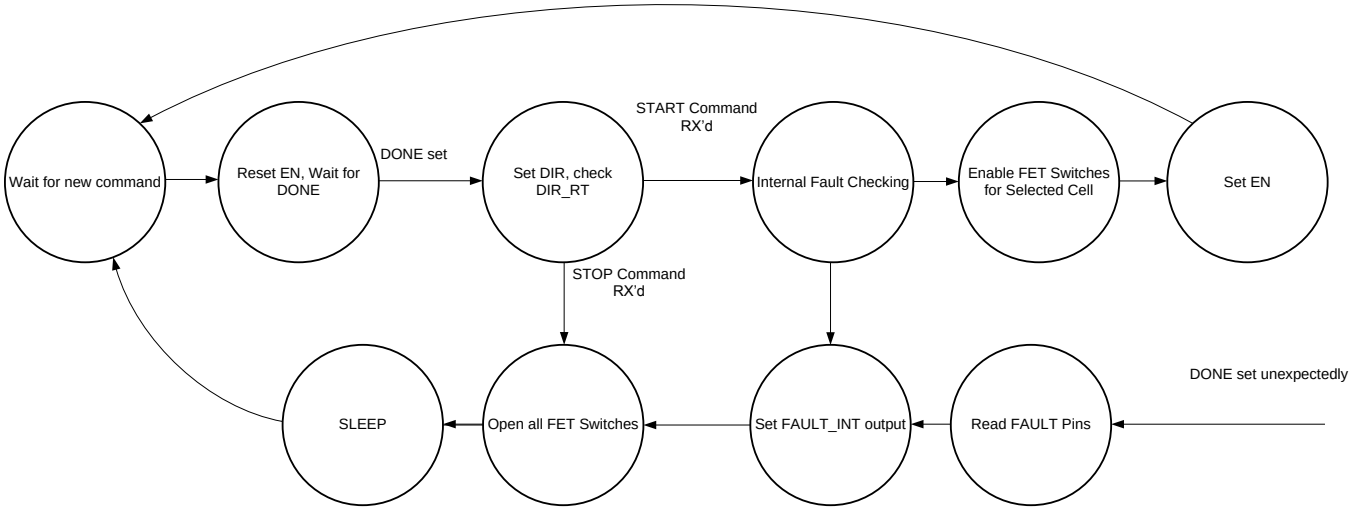


Figure 5-5. EMB1428Q Flowchart

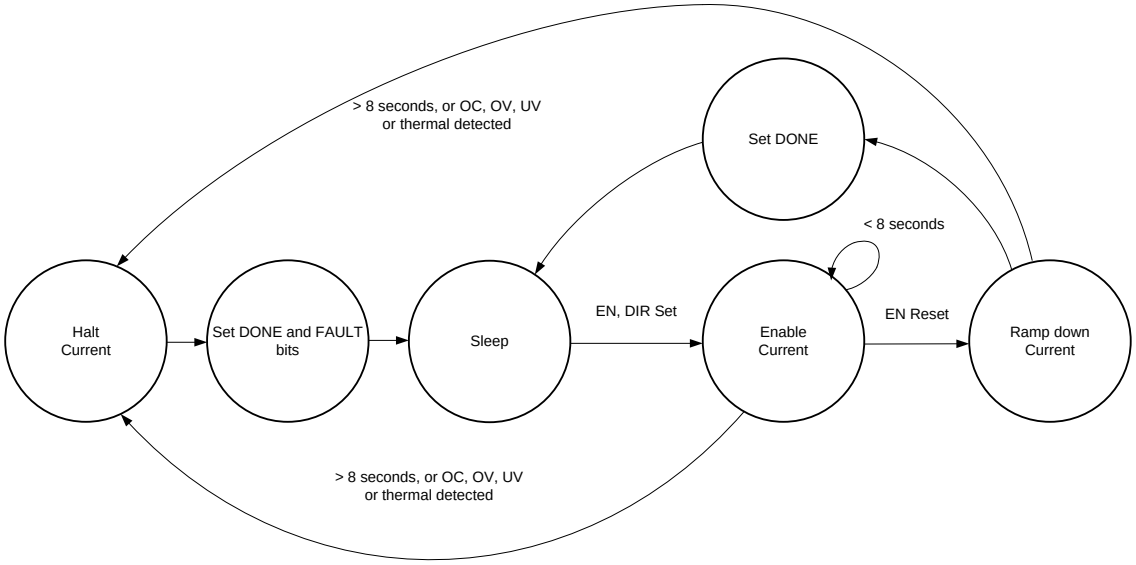


Figure 5-6. EMB1499Q Flowchart

5.3 Current Set Point

One input signal not provided to the EMB1499Q device by the EMB1428Q device is the current set point (VSET). This set point, in conjunction with the current sense resistor, controls the amount of current used in the transfer. The current is set by a combination of the setting of the feedback voltage (through VSET), and selection of the secondary current sense resistor as governed by Equation 3.

$$\text{balance current} = \text{feedback voltage} \div \text{secondary sense resistor} \quad (3)$$

The primary current sense resistors are R179 and R197 in the schematics for the EMB1499Q circuit provided in Figure E-6 and Figure E-8. The secondary current sense resistors are R174 and R192 in the schematics for the EMB1499Q circuit shown in Figure E-6 and Figure E-8.

5.3.1 Setting the Balancing Current (VSET and Secondary Sense Resistor)

The cell-balancing current is equal to the steady-state value of the main inductor current. Two external parameters determine the balancing current ($I_{balancing}$): the voltage at VSET pin and the secondary-side sense resistance (RSENSE2). The voltage at the VSET pin controls the reference voltage at the internal error amplifier, and therefore the voltage at the V_{SENSE_HS} pin.

Equation 4 is the equation for selecting the secondary side sense resistance.

$$R_{SENSE2} = \frac{V_{SENSE\_HS}}{I_{balancing}} \tag{4}$$

In the equation, V_{SENSE_HS} is a value dictated by the VSET voltage, in accordance with Equation 5.

$$V_{SENSE\_HS} = \frac{VSET}{40} \tag{5}$$

Supported values for VSET range from 1 to 2.2 V. However, the EMB1499Q device is factory trimmed at VSET = 2 V. Therefore, TI recommends to use VSET = 2 V for the highest balancing-current accuracy. See the Electrical Characteristic table in the EMB1499Q data sheet (SNOSCV7)for specified tolerances on V_{SENSE_HS} when for VSET = 2 V and 1.2 V.

Note that in order to ensure loop stability, the sense resistor value must also be chosen in conjunction with the output inductor. See Section 5.11 for a detailed description of the output inductor selection.

For example, if a 5-A balancing current is desired, and VSET voltage is set to 2 V, a 10-mΩ sense resistor must be chosen as shown in Equation 6.

$$V_{SENSE\_HS} = \frac{2\ V}{40} = 50\ mV$$

$$\therefore R_{SENSE2} = \frac{50\ mV}{5\ A} = 10\ m\Omega \tag{6}$$

Because of the switching noise present at the secondary side current sense resistor, current values can be slightly different for different directions of balancing, even if VSET is the same. In such a case, TI recommends that a calibration be conducted at the system level so that a slightly different VSET is programmed when changing the direction of balancing. A procedure for this is described in Section 5.14.

5.3.2 Primary Sense-Resistor Selection

The primary sense resistor must be chosen in conjunction with the secondary sense resistor so that the ratio between the two resistors is approximately equal to the transformer turns ratio. For example if the secondary sense resistor is 10 mΩ, and the transformer turns ratio is 3.5:1 (14 cell application), the primary sense resistor must be chosen to be approximately 35 mΩ.

5.4 EMB1428Q Switch-Matrix FET Selection

For optimal balance transfer efficiency, the switch matrix FETs must be selected to provide the lowest possible conduction loss. For the purpose of FET selection, a good parameter to use is on resistance (R_{dson}). Equation 7 calculates the total power loss due to this parameter.

Conduction power loss are calculated by multiplying the square of the charge current by the static drain to source on resistance ($r_{DS(on)}$) parameter.

$$P_{LOSS} = I_{RMS}^{2} \times R_{dson} \tag{7}$$

In addition to the total conduction loss, the EMB1428Q switch-matrix FETs have the following additional requirements:

- N-channel
- All FETS must have an absolute maximum rating for V_{GS} at least 20 V
- A breakdown voltage > than half of the stack voltage (from cell 0– to top of half-stack cell+) + 10 V
- Gate resistance (R_g) ≤ approximately 10 Ω, to ensure adequate turn-off strength during transient events

5.5 EMB1499Q Switch FET Selection

The parameters described in this section can be used to estimate the total conduction and gate charge losses for each FET, which must be minimized:

$$P_{LOSS} = I_{RMS}^{2} \times R_{dson} + Q_G \times F_{SW}$$

where

- F_{SW} is the switching frequency of the EMB1499Q device (typically 250 kHz)
- I_{RMS} is the RMS drain current in each FET during steady state (8)

The following equations can be used to provide a first order estimation of the RMS drain current in each FET.

Primary switching N-channel FET (Q28 and Q33 in the schematics for the EMB1499Q circuit provided in Figure E-6 and Figure E-8):

$$I_{RMS} \approx \frac{I_{balancing}}{2 \times NumCells} \quad (9)$$

Secondary switching N-channel FET (Q27 and Q29 in the schematics for the bottom EMB1499Q circuit shown in Figure E-6 and Q31 and Q34 in the schematics for the top EMB1499Q circuit shown in Figure E-8):

$$I_{RMS} \approx \frac{I_{balancing}}{\sqrt{2}} \quad (10)$$

Active Clamp P-channel FET (Q26 and Q32 in the schematics for the EMB1499Q circuit shown in Figure E-6 and Figure E-8):

$$I_{RMS} \approx 25\ mS \times V_{CELL\_MAX}$$

where

- V_{CELL_MAX} is the maximum operating voltage of any cell in the stack (11)

The FETs package thermal characteristics must also be sufficient to handle the sum of the conduction and switching power losses.

In addition to power dissipation concerns, and assuming that the transformer turns ratio has been chosen correctly (see Section 5.10), the EMB1499Q FETs have the following additional requirements:

- All FETS must have an absolute maximum rating for V_{GS} at least 20 V.
- Primary FETS (switching and active clamp) must have drain-source voltage rating at least 2.5 times the maximum operating stack voltage.
- Secondary FETs must have drain-source voltage rating at least 30 V, gate resistance no more than 3 Ω, and be avalanche robust (for example: have an Avalanche Energy rating (EAR) specified in the EMB1499Q data sheet, SNOSCV7).

5.6 Active-Clamp Driver Circuit

The active-clamp driver circuit is found in the schematics for the EMB1499Q circuit shown in Figure E-6 and Figure E-8. The driver path consists of a delay circuit (around U24 and U28), the driver (U30 and U12), and a passive-level shifting circuit (C129, C139, D17, D20, R172 and R190).

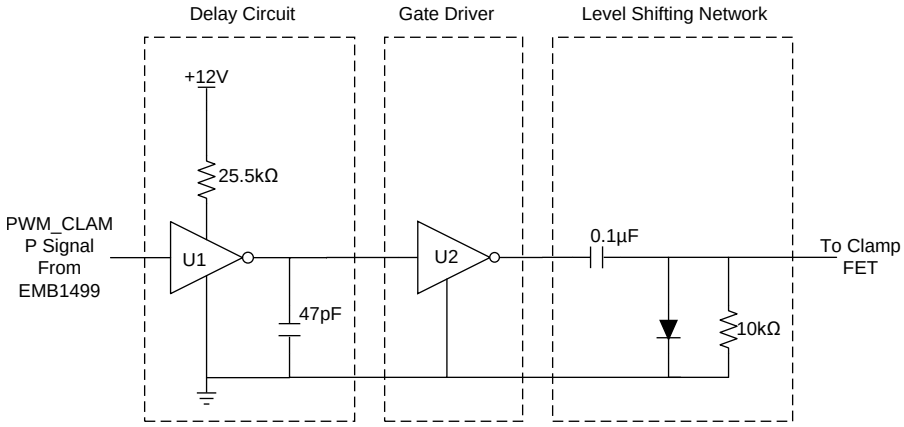


Figure 5-7. Active Clamp Circuit

5.6.1 Delay Circuit

The delay network must provide approximately 300 to 400 ns delay to the turn-on transition of the clamp FET, and minimal delay to the turn-off transition. The recommended inverter for this application is the BU4S584G2 Schmitt Trigger Inverter from Rohm Semiconductor. An N-channel MOSFET can also be used.

An N-channel FET must be selected with a drain-source capacitance significantly less than the external 47-pF capacitor (C225 and C226) to properly set the desired delay. TI also recommends that the FET must be able to withstand gate-source and drain-source voltages higher than 20 V. Using an inverter has the advantage of consuming no standing current regardless of the state of the input, whereas using the FET creates standing current through the 25-kΩ resistor when the PWM_CLAMP signal is high (this is the default state of the PWM_CLAMP signal during shutdown). For this reason U24 was selected because it can withstand 12-V.

5.6.2 Driver

The recommended driver for this application is the EMB1412 device (U30 for the bottom converter and U12 for the top converter). Configuring the driver in an inverting configuration is important.

5.6.3 Passive-Level Shifting Circuit

The passive-level shifting network (C129, D17 and R172 for the bottom converter C139, D20, and R190 for the top converter) is required in order to provide a negative gate voltage for the clamp P-channel FET. The passive-level shifting network consists of a 0.1-µF AC-coupling capacitor, a clamping diode, and a 10-kΩ resistor to provide a DC path to ground for the gate of the clamp PFET.

5.6.4 Clamp FET

The clamp FET must have the following specifications:

- P-channel
- Absolute maximum V_{gs} ≥ 20 V
- Drain-source breakdown voltage ≥ 150 V

5.7 Input Capacitor Selection

The input capacitors are C122, C123 and C124 in the schematics for the bottom EMB1499Q circuit whosn in Figure E-6 and C132, C133 and C134 in the schematics for the top EMB1499Q circuit shown in Figure E-8.

Ceramic capacitors are required for proper operation, because of the low equivalent-series resistance (ESR). The voltage rating of the capacitor must exceed the maximum stack voltage in an application with proper de-rating. For example, in a 14 cell Li-ion application, the maximum stack voltage is approximately 60 V. Therefore, a 100-V rated capacitor is recommended.

TI recommends to use at least 6.6-µF of capacitance. Optimum performance is achieved by using multiple smaller value capacitors in parallel to minimize series resistance and inductance.

For proper performance, X5R or X7R ceramics are recommended.

5.8 Output Capacitor Selection

The output capacitors are C126 and C127 in the schematics for the bottom EMB1499Q circuit shown in Figure E-6 and C136 and C137 in the schematics for the top EMB1499Q circuit shown in Figure E-8.

As with the input capacitors, ceramic capacitors are required (X5R or X7R recommended). Because the maximum operating cell voltage of a Li-ion cell is 4.2 V, a voltage rating of 6.3 V or higher is recommended.

Using at least 10-µF of capacitance is required. Optimum performance is achieved by using multiple smaller-value capacitors in parallel to minimize series resistance and inductance.

5.9 Clamp Capacitor Selection

The clamp capacitors are C125 and C135 in the schematics for the EMB1499Q circuit shown in Figure E-6 and Figure E-8.

As with the input and output capacitors, a ceramic capacitor is required for the clamp capacitor. Assuming that the transformer turns ratio is chosen correctly (see Section 5.10), the voltage rating of the capacitor must be at least 2.5 times the maximum operating voltage of the battery stack.

For example, in a 14 cell solution with a maximum operating cell voltage of 4.2 V, the maximum operating voltage of the stack is 58.8 V. Therefore, the voltage rating of the capacitor must be at least 2.5 × 58.8 V = 147 V.

So for a 14 cell solution, a voltage rating of 200 V (the next closest commonly found voltage rating) is recommended.

The recommended capacitance value for the clamp capacitor is 0.1-µF.

5.10 EMB1499Q Transformer Selection

In selecting the proper transformer (T2 and T3 in the schematics for the EMB1499Q circuit shown in Figure E-6 and Figure E-8) for use with the EMB1499Q device, several major factors must be considered, including turns ration, primary magnetizing inductance, leakage inductance and DC-winding resistance.

5.10.1 Turns Ratio

The EMB1499Q device was designed to work with a transformer turns ratio of 3.5:1 when operating within a stack of 14 cells. In order to maintain proper peak currents and voltage stresses on the drains of the power FETs, TI recommends to maintain this relationship between turns ratio and number of cells. In other words, use Equation 12 when choosing a turns ratio for the transformer.

$$n = 0.25 \times NumCells \quad (12)$$

5.10.2 Primary Magnetizing Inductance

As shown in the schematic for the EMB1499Q circuit is provided in Figure E-6 and Figure E-8, the forward transformer for the EMB1499Q device has a minimum primary-side inductance of 190 µH. To ensure proper operation, TI recommends to use this inductance as the minimum inductance specification for a 14-cell solution. Scaling this inductance with the number of cells in the stack is reasonable. For example, for a 7-cell stack, use a minimum primary inductance of 95 µH.

5.10.3 Leakage Inductance

The leakage inductance is directly related to the coupling coefficient of the transformer. For proper operation, TI recommends that the leakage inductance of the transformer be less than or equal to 1% of the magnetizing inductance.

5.10.4 DC Winding Resistance

On the transformer used in a typical 5-A design, the primary-side DC resistance is typically 57 mΩ, and the secondary side resistance is typically 12 mΩ. In order to ensure reasonable efficiency, and to ensure properly gauged wires are used in the transformer, TI recommends to follow this specification for 5-A balancing current. Scaling these resistance specifications for constant DC-power dissipation with different balancing currents is reasonable.

5.11 EMB1499Q Inductor Selection

In selecting the proper inductor (L5 and L7 in the schematics for the EMB1499Q circuit shown in Figure E-6 and Figure E-8) for use with the EMB1499Q, several major factors must be considered, including output current ripple, loop stability, core saturation current, and DC resistance.

5.11.1 Output Current Ripple

The value of the inductor, along with the converter I/O voltages, determines the AC ripple of the inductor current. A good practice is to choose the inductance value so that the peak-to-peak ripple falls somewhere between 20% and 40% of the steady state balancing current during typical operation. If the transformer turns ratio is selected properly (see Section 4.8), and assuming a 250-kHz switching frequency, then the equation relating inductance to current ripple for the EMB1499Q device is reduced as shown in Equation 13.

$$L = 3 \times 10^{-6} \times V_{CELL} \times \Delta i_L \quad (13)$$

where

- V_{CELL} is the typical cell voltage in the given application
- Δi_L is the peak-to-peak current-ripple value, calculated as Equation 14

$$0.2\ I_L \le \Delta i_L \le 0.4\ I_L \quad (14)$$

For example, a 6.8-µH inductor is used in the active-chipset reference design (5-A balancing current). With this inductance value and a typical cell voltage of 3.5 V, the peak-to-peak ripple is calculated as shown in Equation 15 which is about 31% of the 5-A balancing current.

$$\Delta i_L = \frac{3 \times 10^{-6} \times 3.5\ V}{6.8\ \mu H} = 1.54\ A \quad (15)$$

5.11.2 Loop Stability

The EMB1499Q device uses peak current-mode control, which means that the inductor current is sampled in real time and used for loop control. In this type of control method, the slope of the sensed inductor-current ripple is an important parameter. This sensed slope is inversely proportional to the inductor value, and directly proportional to the gain of the current sense path which is calculated with Equation 16.

$$\frac{dI_{SENSE}}{dt} \propto \frac{R_{SENSE2} A_I}{L} \quad (16)$$

where

- I_{sense} is the sensed inductor current
- R_{sense2} is the secondary side sense resistor value
- A_I is the gain of the internal current sense amplifier.

In order to ensure stability of the internal current-sense loop, TI recommends that the slope of the sensed inductor current remain somewhat constant if external component values are changed. This linear relationship means that if the value of the secondary sense resistor is increased (possibly to achieve lower balancing current), then the value of the output inductor must increase with approximately the same scale (see Equation 16).

5.11.3 Core Saturation Current

When selecting an inductor, choose an inductor that can support the peak output current without saturating. Inductor saturation causes a sudden reduction in the inductance value, and causes the converter to operate incorrectly.

5.11.4 DC Resistance

This parameter becomes especially important at higher balancing currents (such as 5 A). TI recommends to choose an inductor with minimal DC resistance in order to minimize conduction losses and maximize efficiency.

As with the input and output capacitors, a ceramic capacitor is required for the clamp capacitor. The recommended capacitance is 0.1 µF with a voltage rating of at least 200 V.

5.12 EMB1428Q and EMB1499Q Power Supply Requirements

The following power supplies are common to both the EMB1428Q and EMB1499Q devices:

- 12 V
  - Supplies EMB1428Q VDD_12V and EMB1499Q VINA and VINP
  - Consumes approximately 22 mA during use and 4.6 µA during shutdown

5.12.1 EMB1428Q

- VIO
  - 2.5 to 5.5 V
- 5 V
  - VDD_5V
  - Digital logic supply, can be shared with +5-V supply used for other ICs (EMB1432, EMB1433)
- Top of Stack
  - VDD_CP
  - Internal charge pump supply that provides the gate drive.
  - This supply must always be present before VDD_12V, VDD_5V and VDD_IO.

5.12.2 EMB1499Q

- Floating 12 V
  - Separate supply required for each EMB1499Q device
  - Supplies EMB1499Q VINF and PVINF
  - Consumes approximately 36 mA during use and 5 µA during shutdown

5.13 Circuit Schematic

The schematic for the EMB1428Q circuit is shown in Figure E-5 and Figure E-7. The schematic for the EMB1499Q circuit is shown in Figure E-6 and Figure E-8.

5.14 Current Calibration

To provide maximum accuracy, the system must be factory calibrated for current offset and gain on each converter. The system must be calibrated with an accurate ammeter measuring each converter output.

Although the current set point can be implemented with a fixed external-voltage reference, typically a microcontroller provides this reference to the EMB1499Q device using a DAC or a PWM signal and an external RC filter. Configuration of the DAC output, or calculation of the PWM duty cycle required to reach a specific voltage level depends on the microcontroller internal features and IO voltage. Please consult the selected-microcontroller data sheet for specific configuration information.

The procedure described here allows the user to adjust the calibration offsets to return accuracy to the system.

The method to adjust the current offset calibration is as follows:

1. Start a cell charge transfer.
2. Take measurement at the cell with external ammeter and calculate difference from system current setpoint (EMB1499Q Vset).
3. Write current offset calibration value by found in step 2 to a non-volatile data memory area (Flash or EEPROM).
4. Repeat this procedure for all converters.
5. Repeat this procedure for a cell discharge transfer.
6. Apply the stored calibration value to the DAC or PWM (EMB1499Q driving Vset).

5.15 PCB Layout Guidelines

5.15.1 EMB1428Q

This section describes the design criteria that must be considered for the EMB1428Q PCB layout. Figure E-5 and Figure E-7 show the EMB1428Q schematics.

The charge pump components are C_Vstack1, CEXT1, CEXT2 and D7 for bottom EMB1428Q and C_Vstack2, CEXT3, CEXT4 and D2 for the top EM1428.

The decoupling caps (C17–19 and C209 for bottom EMB1428Q and C118–120 and C210 for top EMB1428Q) are as close as possible to the EMB1428Q devices.

The layout must keep every gate trace as close as possible to the companion source trace.

5.15.2 EMB1499Q

The EMB1499Q device is a bi-directional active-clamp forward-switching converter and therefore the designer must simply follow the basic guidelines for layout of a forward converter. To follow the basic guidelines, keep the traces short and the loops small for discontinuous currents. There are also a couple of unique considerations for this specific application and topology. Figure E-6 and Figure E-8 show the schematics for the EMB1499Q.

The designer must ensure the decoupling capacitor from the EMB1499Q PGNDF to GND is situated close to the EMB1499Q device and that the PCB trace loop is as small as possible. This capacitor is critical to providing an AC return path and must be kept as clean as possible. This capacitor is C215 for bottom EMB1499Q and C216 for the top EMB1499Q.

The sense lines for the current sense resistor (R174 for bottom EMB1499Q and R192 for top EMB1499Q) must also be setup as a Kelvin connection. Traces to both sides of the resistor must be close to the EMB1499Q device to minimize offset errors and reduce the risk of noise being coupled in.

The following basic criteria must also be met:

- All decoupling capacitors must be placed as close as possible to the EMB1499Q device.
- Run the gate traces in parallel with the associated ground planes for as much of the total runs as possible.
- Keep current sensing traces away from high dv/dt nodes such as the drain of power FETs.
- Place enough copper underneath the power FETs to help it cool.
- The EMB1499Q device must be ideally located within a couple inches of the power FETs so that the gates are tightly controlled.
- Place ten or so 8-mil vias on the PCB pad beneath the EMB1499Q device and connect them to the corresponding ground planes on all layers to cool down the chip.

System Integration Considerations

This section describes features or issues which must be considered when the previously mentioned subsystems and circuits are integrated in a design.

6.1 Cell Connection

The EMB1499Q internal protection circuits and the EMB1432 cell measurement can be affected by the cell connection method.

The EMB1499Q has built-in protection for over voltage and under voltage while transferring current to and from a battery cell. The current transfer protects the BMS from damage caused by an open cell connection. The cell voltage is sensed on the CELLPLUS pin of the EMB1499Q device. The specification for OVP and UVP is provided in the electric specifications section of the EMB1499Q data sheet (SNOSCV7).

There are some battery cell connection design considerations which influence PCB layout, connector selection, and wire harness construction.

Equation 17 describes the voltage level on CELLPLUS while balance current is flowing. What is referred to as *Common Path* includes every circuit connection from the CELLPLUS pin to the external connector.

This includes:

- Harness connector contact resistance
- Switch matrix FET $r_{DS(on)}$ (x4)
- PCB trace resistance

$$\text{CELLPLUS V} = \text{Vcell} + [\text{Balance Current} \times (\text{BMS common path R} + \text{Harness R})] \quad (17)$$

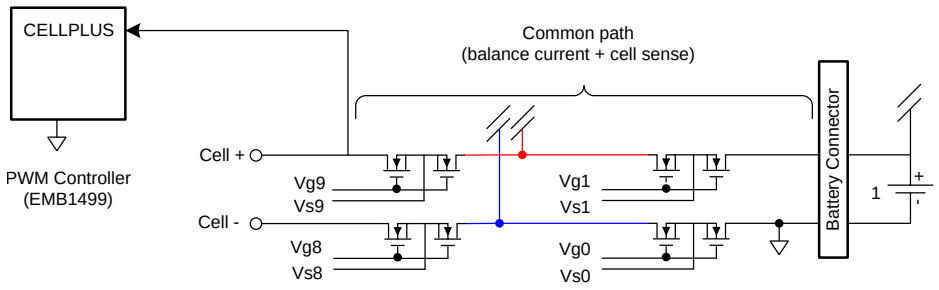


Figure 6-1. CELLPLUS Common Path

As an example, on the EM1401 BMS Evaluation Board, the resistance of the common path shown in Figure 6-1 is approximately 75 mΩ. At 5-A charge, with a common path resistance from the board connector to the cell of 75 mΩ, a wire harness resistance of 100 mΩ and a cell voltage of 4 V, the voltage level at CELLPLUS is 4.875 V.

In a similar manner, the EMB1432 cell measurement can be affected depending on design choices regarding the cell connection method. There are two choices:

- Separate cell sense connector (Kelvin sense) with a connection to a point as close to the cell terminal as possible dedicated to the purpose of cell measurement.
- Cell sense connection that is shared with cell balance connection, with a significant portion of the cell measurement path also subject to cell balance charge and discharge currents.

System Power Supplies

7.1 Overview

An external power supply circuit must be designed to meet the system requirements with the following goals:

- Provide the supplies required by the system with as high efficiency as possible.
- Provide the ability to go into a shutdown or standby mode with extremely low quiescent power draw.
- Provide the ability to come out of shutdown or standby mode (wake-up) and reach a stable level in a reasonable amount of time.
- Able to control the supply generation to adapt to the needs of the system in a dynamic fashion, (for example, under the control of the microcontroller).
- Achieve minimal quiescent current draw in shutdown mode with required decoupling.

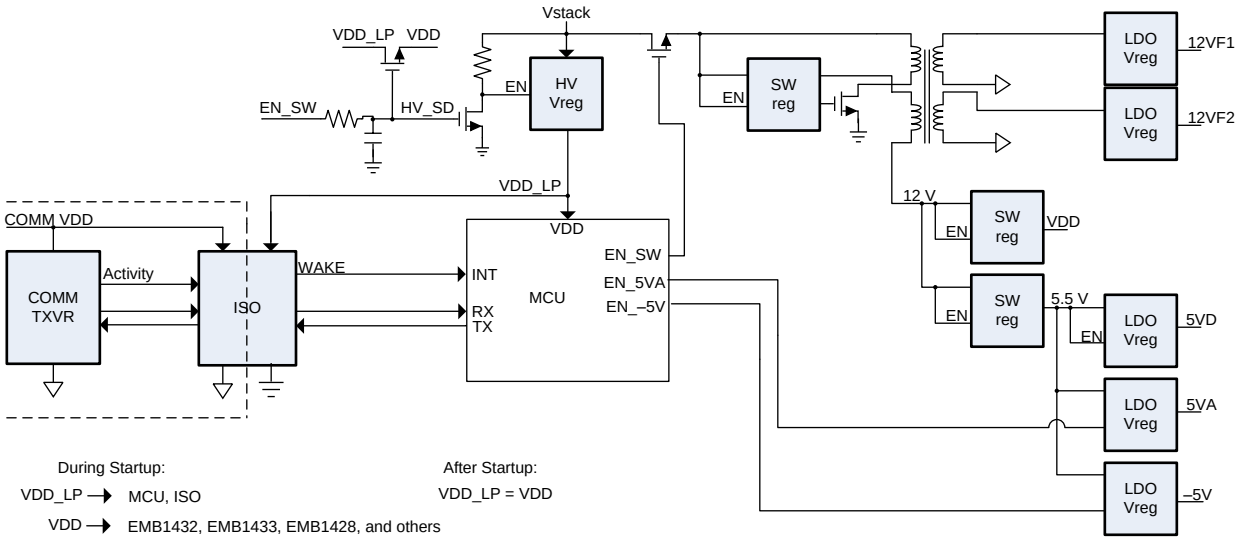


Figure 7-1. Power-Supply Proposal Block diagram

The design proposed here supplies 12 V (3x 1 GND referenced, 2x floating), 5VD, 5VA, –5 V and 3.3 V from the BMS module cells as a source. Appendix D lists a summary of the power supply requirements of the system. A simple block diagram of the power supply is shown in Figure 7-1. There are many possible strategies to provide these supplies, and customer requirements also influences the design, including different internal or external sources. Appendix D briefly lists other possible solutions.

7.2 Design

The HV linear regulator is required to provide a fast-starting supply to the minimal circuits required during system startup and initialization. The fast-starting supply is not an efficient supply for continued operation, and therefore is intended to only be used during the MCU initialization or low-power standby modes (depending on the MCU). As the HV linear regulator is only required for initialization, it must only be powering the MCU (and any other peripheral circuits required during initialization). The HV linear regulator output must be decoupled (through an FET) from the supply used by other ICs which are not required to be powered during initialization.

The switching regulator input is also decoupled by an FET to reduce the quiescent current during shutdown mode to a minimum. Once the MCU has initialized, the EN_SW signal turns on the switching regulator, which in turn provides an efficient supply for all ICs VDD and VDDIO. Once the switching regulator output is stable, the circuits supplied by the HV linear regulator are sourced from the switching regulator output (decoupling FET enabled) and the HV linear regulator is turned off. The required delay from the switching-regulator output stable to the HV-linear regulator turn-off is typically achieved by a fixed RC delay from the EN_SW signal (called HV_SD in Figure E-10).

Figure E-10 shows a tested power supply design schematic.

AFE Source Selection Tables

Table A-1. AFE Source Selection Table

Source	Discrete MUX Lines				SPI				
	MUX3	MUX2	MUX1	MUX0	Bit 3 (MSB)	Bit 2	Bit 1	Bit 0	FB[1] (LSB)
Battery 1	0	0	0	0	0	0	0	0	0
Battery 2	0	0	0	1	0	0	0	1	0
Battery 3	0	0	1	0	0	0	1	0	0
Battery 4	0	0	1	1	0	0	1	1	0
Battery 5	0	1	0	0	0	1	0	0	0
Battery 6	0	1	0	1	0	1	0	1	0
Battery 7	0	1	1	0	0	1	1	0	0
Battery 8	0	1	1	1	0	1	1	1	0
Battery 9	1	0	0	0	1	0	0	0	0
Battery 10	1	0	0	1	1	0	0	1	0
Battery 11	1	0	1	0	1	0	1	0	0
Battery 12	1	0	1	1	1	0	1	1	0
Battery 13	1	1	0	0	1	1	0	0	0
Battery 14	1	1	0	1	1	1	0	1	0
AUX1	Not Selectable				1	1	1	0	0
AUX2	Not Selectable				1	1	1	1	0

(1) This function not fully described in this document. Please see the EMB1432 data sheet (SNOSB86).

EMB1428Q and EMB1499Q Tables

Table B-1. EMB1428Q Command and Output Table

Command [3:0]	Description	Direction	Cell	Converter			
			Vg[7:0]	Vg11	Vg10	Vg9	Vg8
0000b	STOP (Open all switches)	—	00000000b	0b	0b	0b	0b
0001b	START (Connect) cell 1	Charge	00000011b	1b	0b	0b	1b
0010b	START (Connect) cell 2	Charge	00000110b	0b	1b	1b	0b
0011b	START (Connect) cell 3	Charge	00001100b	1b	0b	0b	1b
0100b	START (Connect) cell 4	Charge	00011000b	0b	1b	1b	0b
0101b	START (Connect) cell 5	Charge	00110000b	1b	0b	0b	1b
0110b	START (Connect) cell 6	Charge	01100000b	0b	1b	1b	0b
0111b	START (Connect) cell 7	Charge	11000000b	1b	0b	0b	1b
1000b	Test mode (reserved)	—	00000000b	0b	0b	0b	0b
1001b	START (Connect) cell 1	Discharge	00000011b	1b	0b	0b	1b
1010b	START (Connect) cell 2	Discharge	00000110b	0b	1b	1b	0b
1011b	START (Connect) cell 3	Discharge	00001100b	1b	0b	0b	1b
1100b	START (Connect) cell 4	Discharge	00011000b	0b	1b	1b	0b
1101b	START (Connect) cell 5	Discharge	00110000b	1b	0b	0b	1b
1110b	START (Connect) cell 6	Discharge	01100000b	0b	1b	1b	0b
1111b	START (Connect) cell 7	Discharge	11000000b	1b	0b	0b	1b

Table B-2. EMB1428Q and EMB1499Q Fault Code Table

Failure Description	Fault Code	Fault Interrupt Triggered?
DONE went high while EN was high and FAULT[2:0] != 3'b000	{1'b0, FAULT[2:0]}	yes
DONE went high while EN was high and FAULT[2:0] == 3'b000	4'b1100	yes
SDI sampled high when it should be low	4'b1101	yes
9th SCL_C rising edge seen while nCS is low	4'b1101	yes
nDIR_RT isn't the opposite of DIR	4'b1110	yes
nCS falling edge while the Switch & Tigon Control block is still waiting for a transition on DONE (rising or falling edge)	4'b1000	no
nCS falling edge while out_slew is high or we are waiting for it to go high	4'b1001	no
nCS falling edge while bg_good is low and the current command is not 4'h0 (open all switches)	4'b1011	no
Internal signal bg_good went low after it was sampled high	4'b1011	yes
No fault condition	4'b1010	no

Chipset and Optional Interface Signals

C.1 Chipset Interface Signals

For up to seven cells, 10 to 16 control signals are required. For eight or more cells 12 to 19 control signals minimum are required.

Signal	IC	Pin	Description	Type
CLK	EMB1432	43	SPI Clock	Microcontroller SPI peripheral or GPIO
	EMB1426	8		
	EMB1428Q	27		
SDI	EMB1432	41	SPI slave input	Microcontroller SPI peripheral MOSI or GPIO
	EMB1428Q	28		
SDO	EMB1432	44	SPI slave output	Microcontroller SPI peripheral MISO or GPIO
	EMB1426	7		
	EMB1428Q	29		
MUX0(1)	EMB1432	1	MUX selection bit 0	Microcontroller GPIO (output)
MUX1(1)	EMB1432	48	MUX selection bit 1	Microcontroller GPIO (output)
MUX2(1)	EMB1432	47	MUX selection bit 2	Microcontroller GPIO (output)
MUX3 (1)	EMB1432	46	MUX selection bit 3	Microcontroller GPIO (output)
nSD(2)	EMB1432	40	Shutdown (active low)	Microcontroller GPIO (output)
nRS(2)	EMB1432	39	Reset (active low)	Microcontroller GPIO (output)
FAULT_INT(3)	EMB1428Q	31	Fault interrupt source	Microcontroller GPIO (interrupt input)
RESET	EMB1428Q	35	Reset (active high)	Microcontroller GPIO (output)
VSET(3)	EMB1499Q	6	Current set point	Microcontroller DAC or PWM (with low-pass filter) output
nCS(4)	EMB1432	42	SPI chip select (active low)	Microcontroller GPIO (output)
nCS	EMB1426	6	SPI chip select (active low)	Microcontroller GPIO (output)
nCS(3)	EMB1428Q	30	SPI chip select (active low)	Microcontroller GPIO (output)
Inrush limit bypass	Q46(5)		Enables FET bypass of in-rush limit circuit	Microcontroller GPIO (output)

(1) The MUX[3:0] signals are only required if the fastest switch rate of the EMB1432 is desired.
(2) Can be tied high, or controlled by the microcontroller.
(3) Two of these interface signals are required for if design includes more than seven cells.
(4) This signal is only required if the EMB1432 Open-Wire-Sense feature is used, or SPI control of the EMB1432 device is desired.
(5) Q46 is described in Section 2.2.

C.2 Optional Interface Signals

These are extra signals which can be required for additional optional features such as temperature sensing or power supply control.

Signal	IC	Pin	Description	Type	Description
nCS	EMB1402	1	SPI chip select (active low)	Microcontroller GPIO (output)	ADC (Temp Sense) CS
EN	EMB1420	7	Enable (active high)	Microcontroller GPIO (output)	HV Switching Regulator enable
EN	EMB1487	4	Enable (active high)	Microcontroller GPIO (output)	–5 V enable

Power Supply Rails

The supplies listed below are separate power supply rails or planes and the respective pin connections in the chipset. Refer to the system schematics in Appendix E for a detailed description.

Supply	IC	Signal	Pin	Description
2.7 to 5.5 V	EMB1432	VIO	3	IO supply
	EMB1433	VIO	3	IO supply
	EMB1428Q	VDD_IO	32	IO supply
	EMB1426	VIO	9	IO supply
	EMB1402	VA	2	Analog supply
		VD	13	Digital or IO supply
	Microcontroller	VDD		VDD, VDDA and, or, VDDIO
	EMB1424	VCC	5	Supply
5 V	EMB1432	CHPVP	35	Charge pump supply
	EMB1433	CHPVP	35	Charge pump supply
12 V	EMB1428Q	VDD_12V	34	
	EMB1499Q	VINA	16	
	EMB1499Q	VINP	21	
	EMB1412	VCC	4, 6	Low-side driver supply
GND	EMB1432	DGND	4	Digital GND
	EMB1433	DGND	4	Digital GND
	EMB1428Q	GND	13, 36, DAP	Digital GND
	EMB1428Q	GNDP	1	Charge pump GND
	EMB1426	GND	5	ADC digital GND
	EMB1499Q	GND	GNDA, GNDP, DAP	
	EMB1412	VEE	1, 3, DAP	Low-side driver GND
	EMB1402	AGND	3	Analog GND
		DGND	12	Digital GND
	Microcontroller	GND		GND, GNDA
	EMB1424	GND	1, 2	Supply GND
5 V (analog)	EMB1432	VP	28	Charge pump supply
	EMB1433	VP	28	Analog supply
	EMB1433	VPREF	29	Voltage reference supply
	EMB1426	VA	10	Analog supply
–5 V	EMB1432	VM	32	Negative voltage supply
AGND	EMB1432	GND	5, 23, DAP	Analog GND
	EMB1433	GND	5, 23, DAP	Analog GND
RGND	EMB1432	GNDREF	31	Reference GND
	EMB1426	GND	4	Analog GND
	REF5025	GND	4	Supply GND
RGND_BSP	EMB1433	GNDREF	31	Reference GND
12VF1	EMB1499Q	PVINF	22	Floating 12-V supply
	EMB1499Q	VINF	28	Floating 12-V supply
GNDF1	EMB1499Q	PGNDF	24	Floating GND
	EMB1499Q	GNDF	27	Floating GND
12VF2	EMB1499Q	PVINF	22	Floating 12-V supply
	EMB1499Q	VINF	28	Floating 12-V supply
GNDF2	EMB1499Q	PGNDF	24	Floating GND
	EMB1499Q	GNDF	27	Floating GND

Chipset Schematics

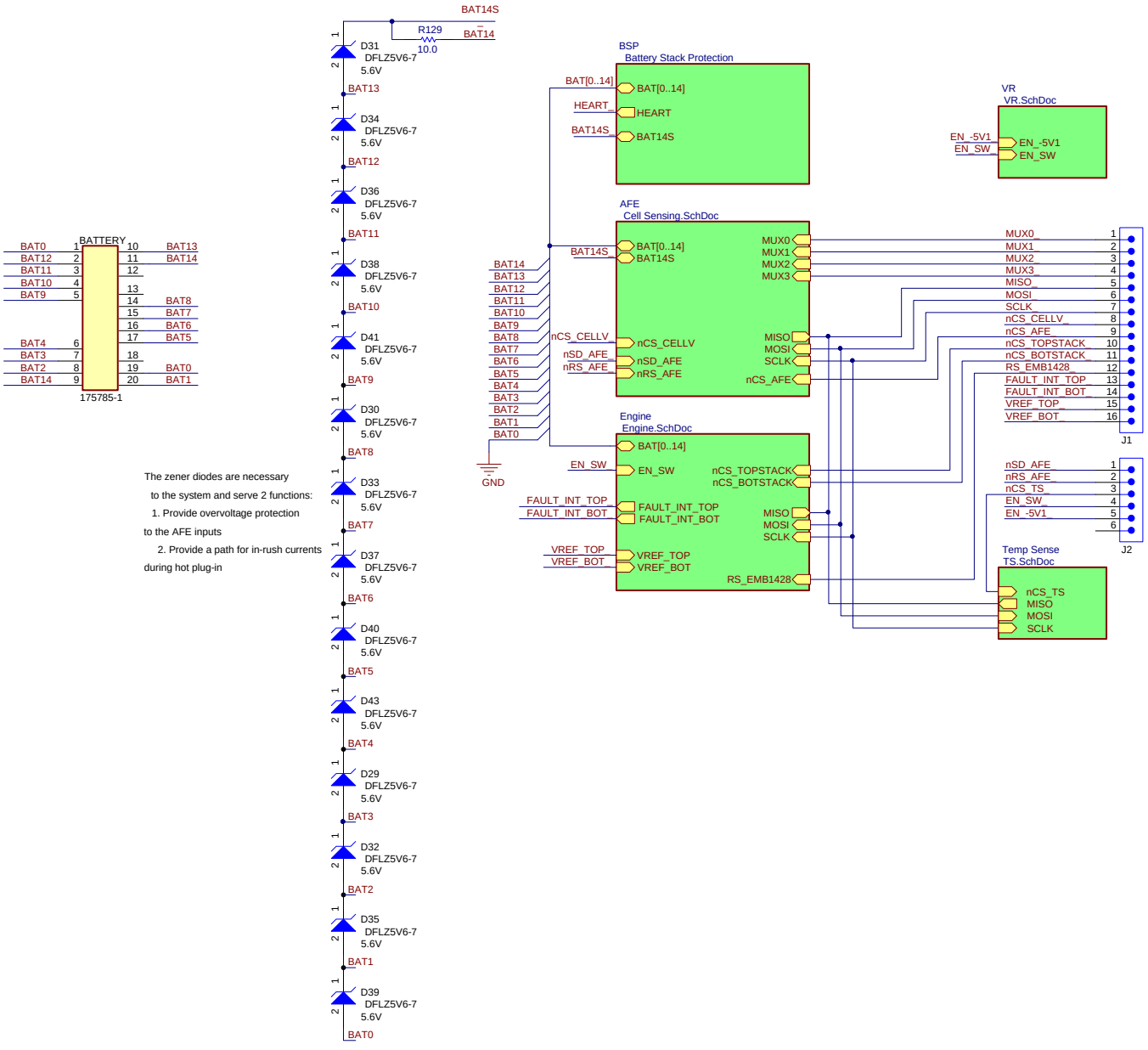


Figure E-1. Top Level Schematic

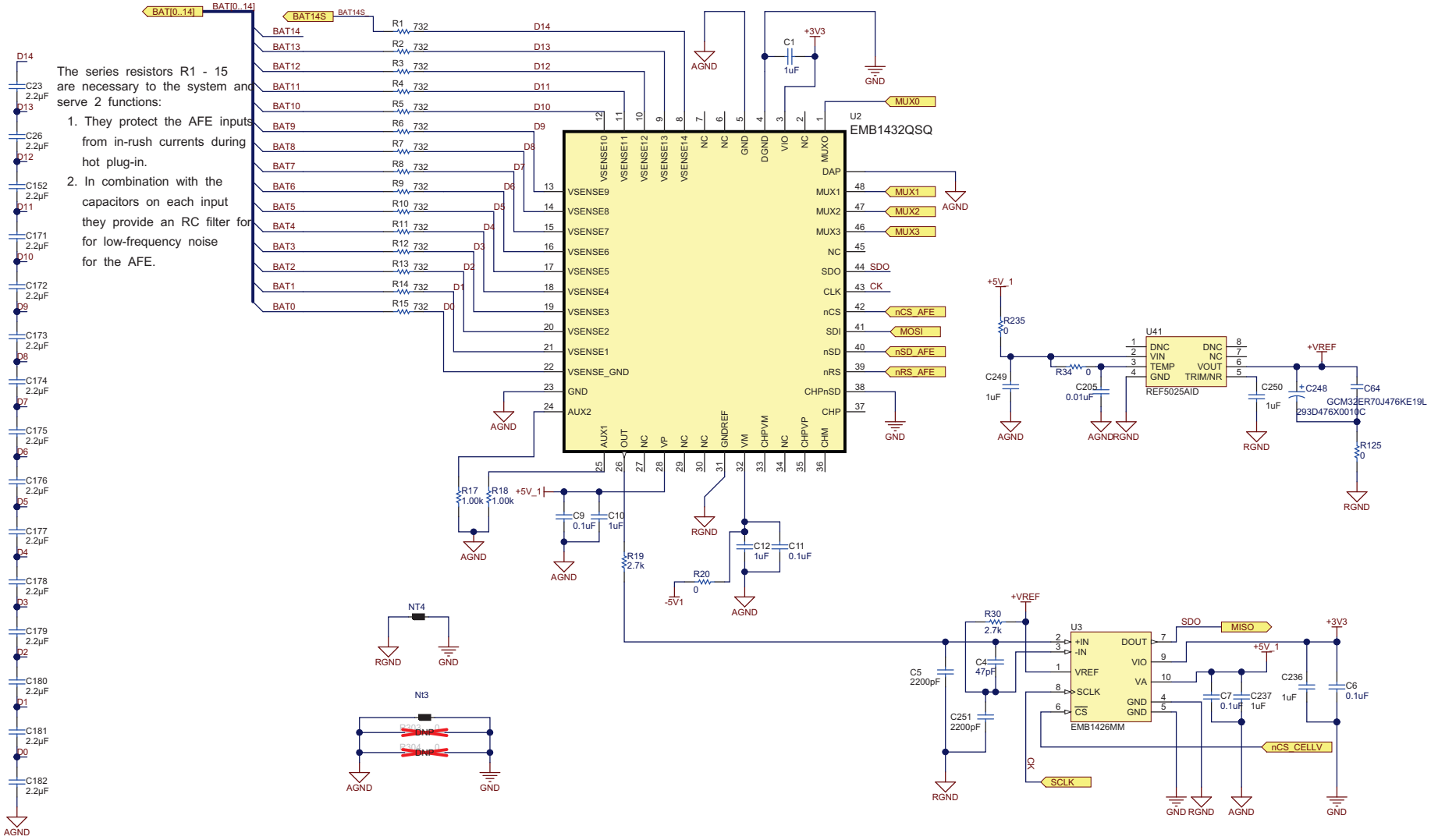


Figure E-2. Cell Sensing Schematic

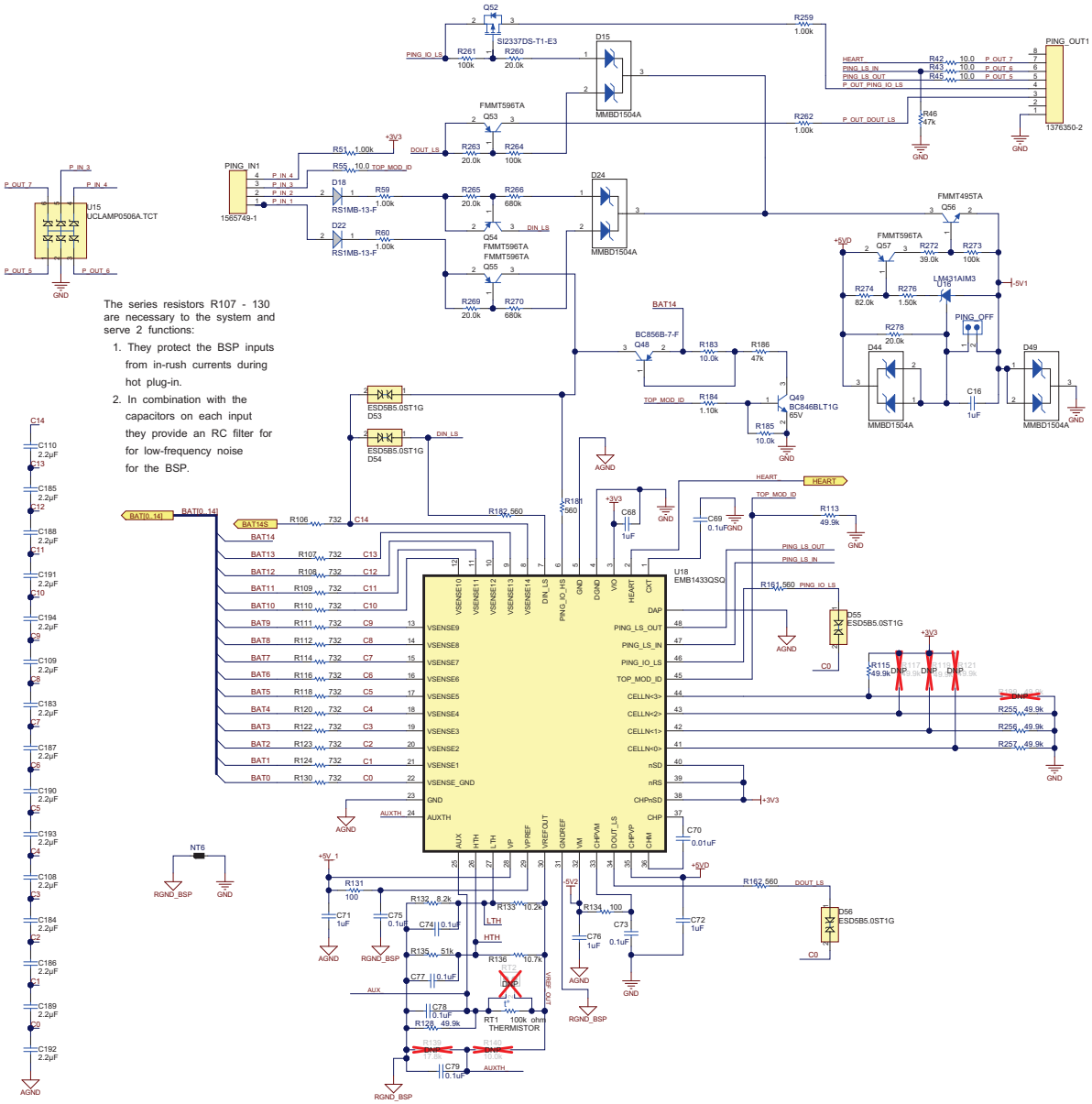


Figure E-3. Battery Stack Protection Schematic

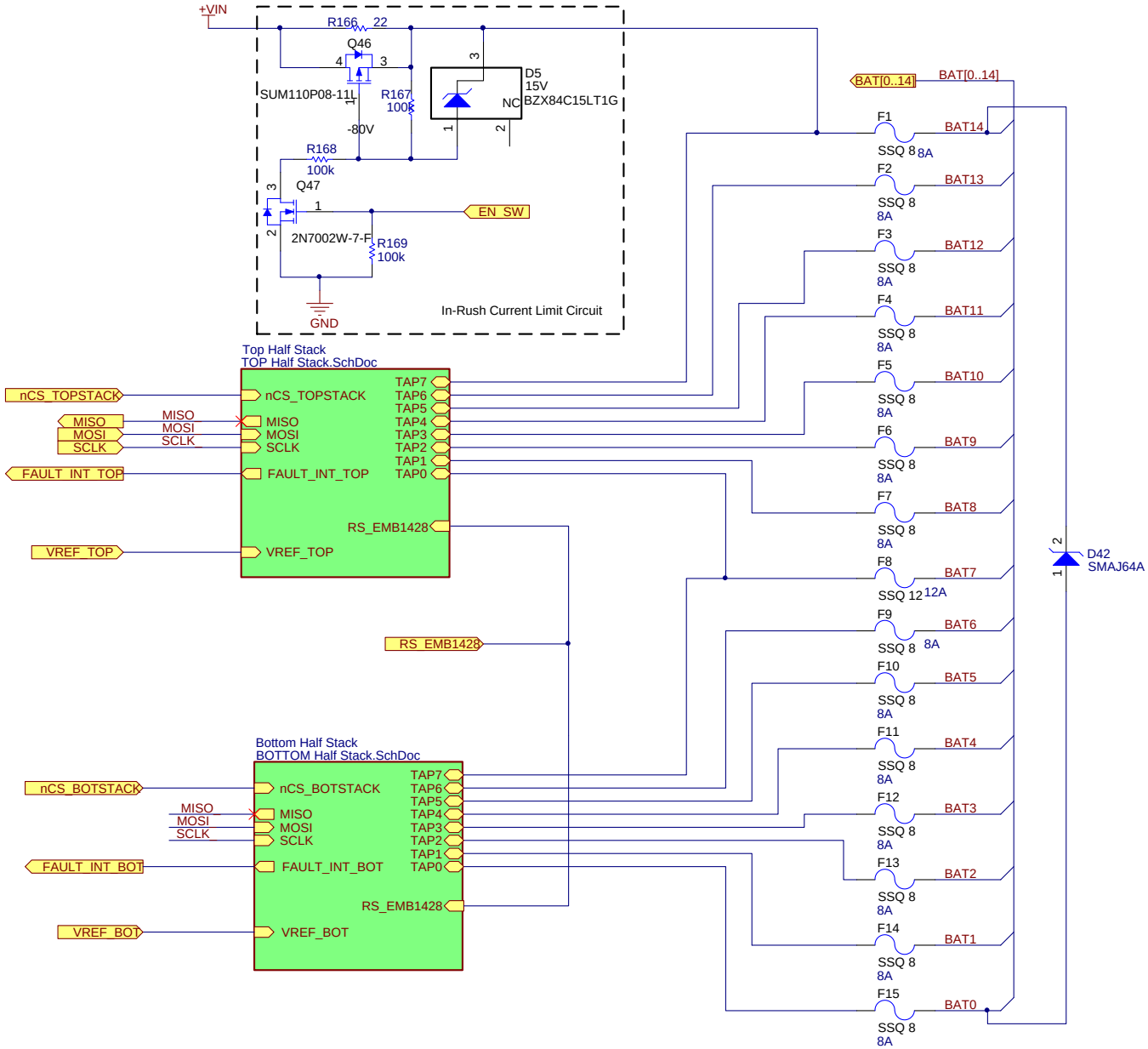


Figure E-4. Active Cell Balance Top Level Schematic

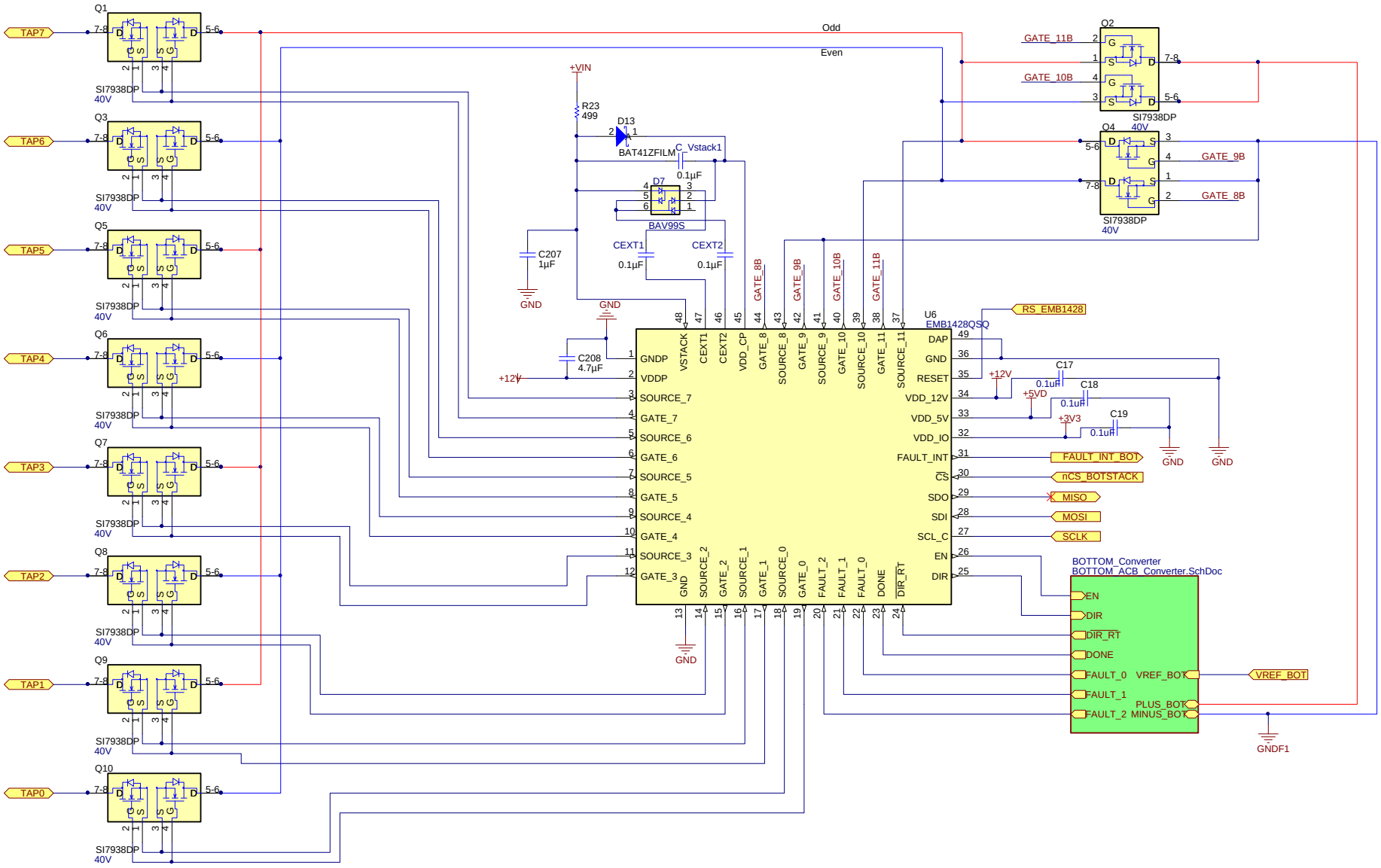


Figure E-5. Bottom Half-Stack Switch Matrix Schematic

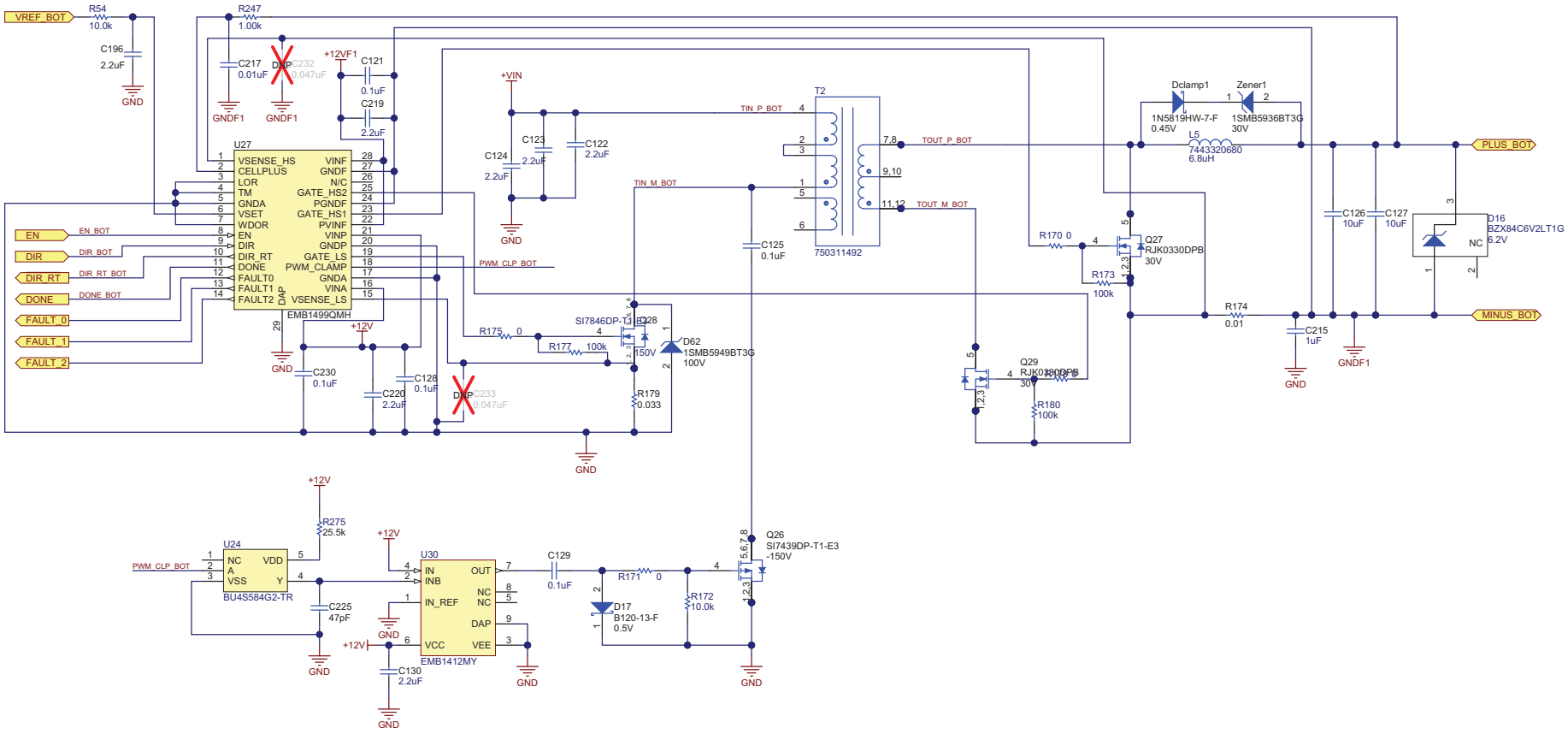


Figure E-6. Bottom Converter Schematic

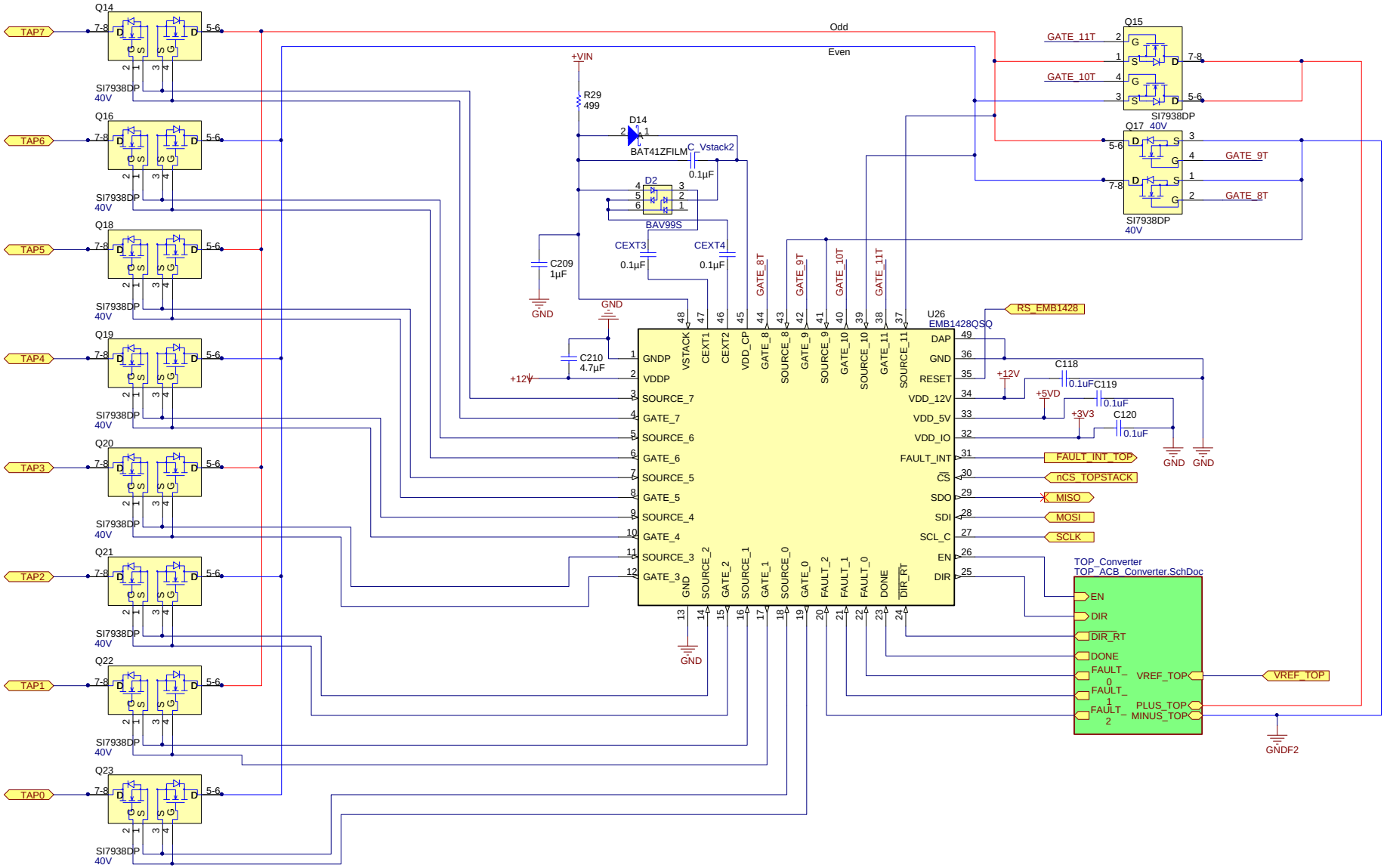


Figure E-7. Top Half-Stack Switch Matrix Schematic

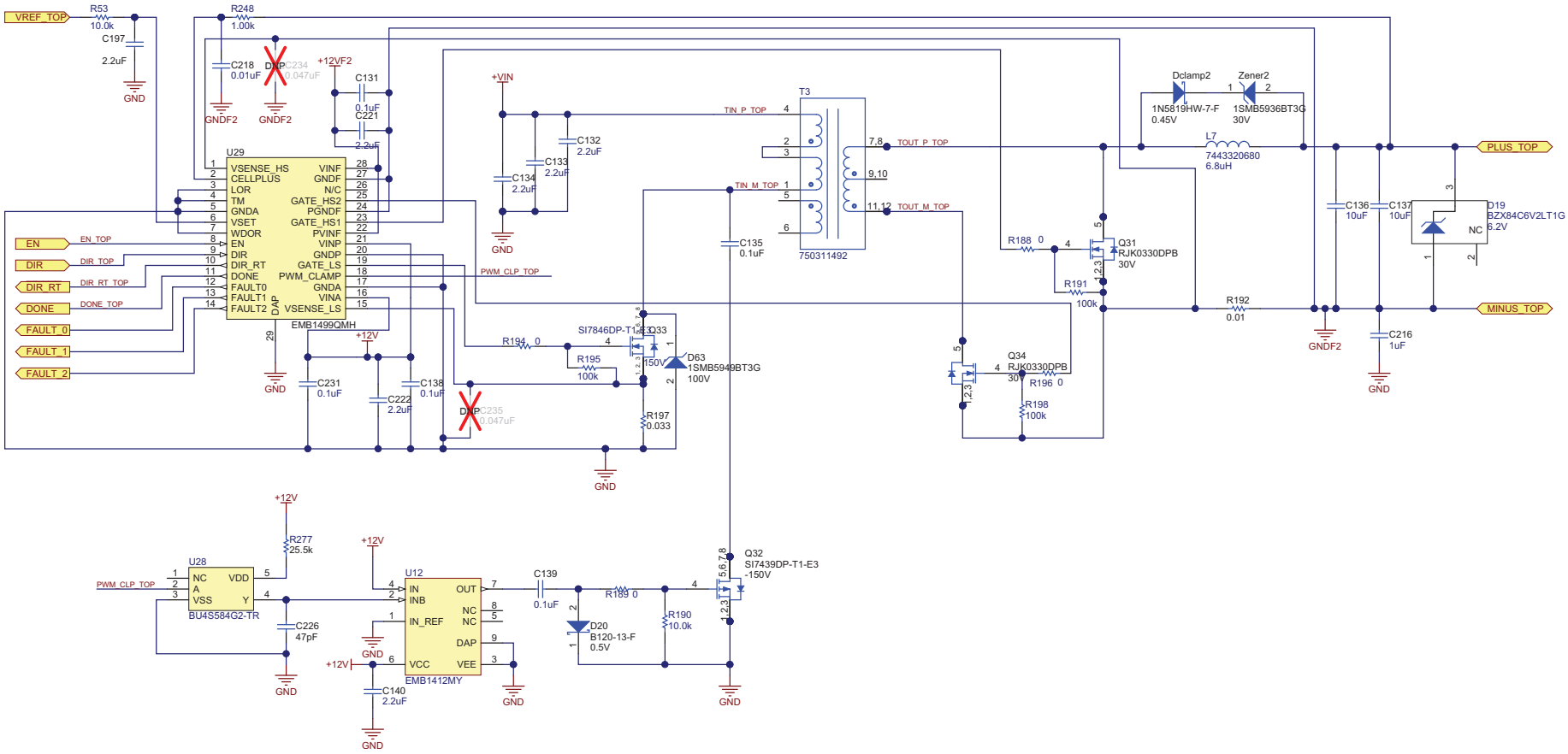


Figure E-8. Top Converter Schematic

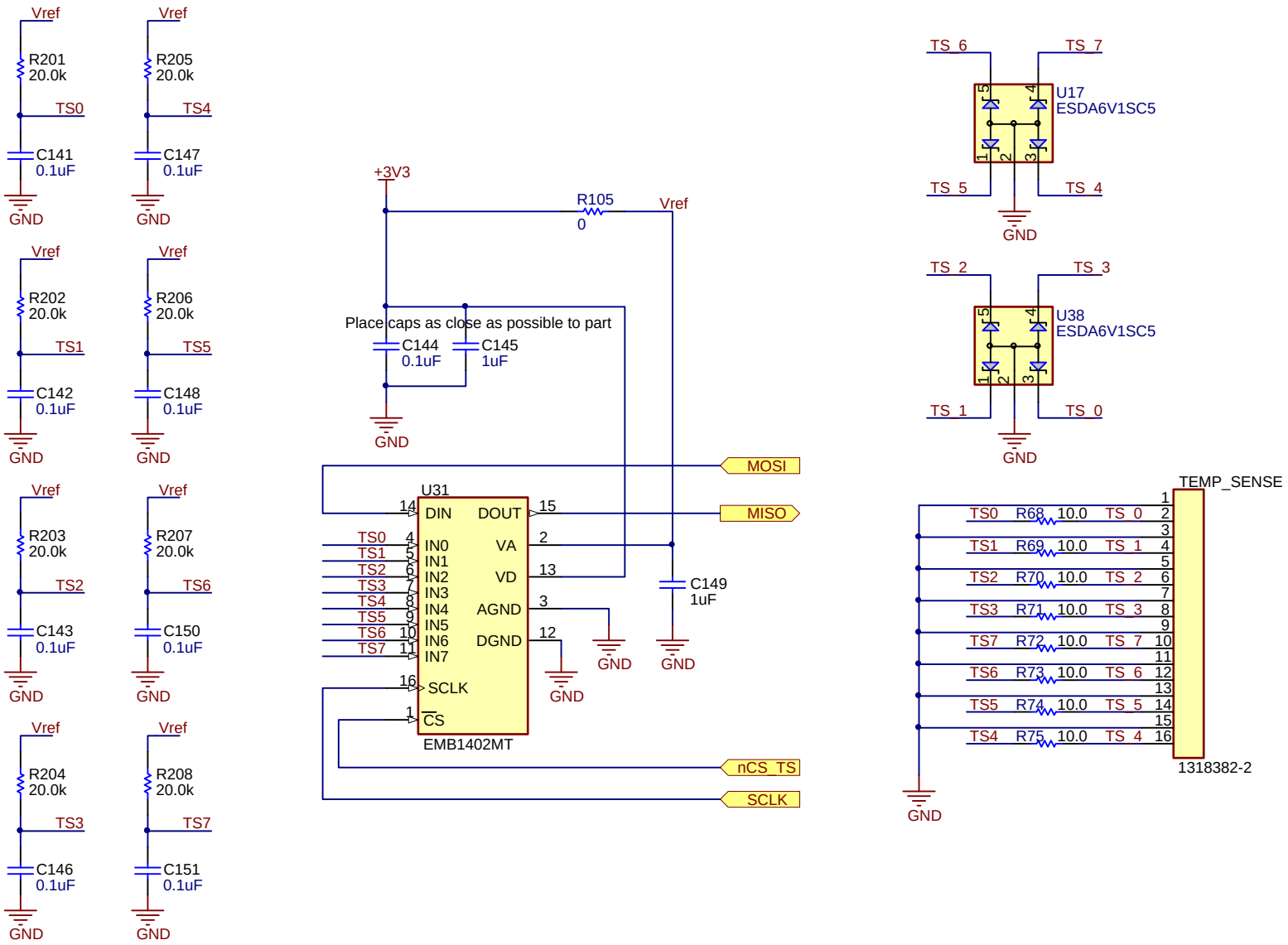


Figure E-9. Temperature Sensing Schematic

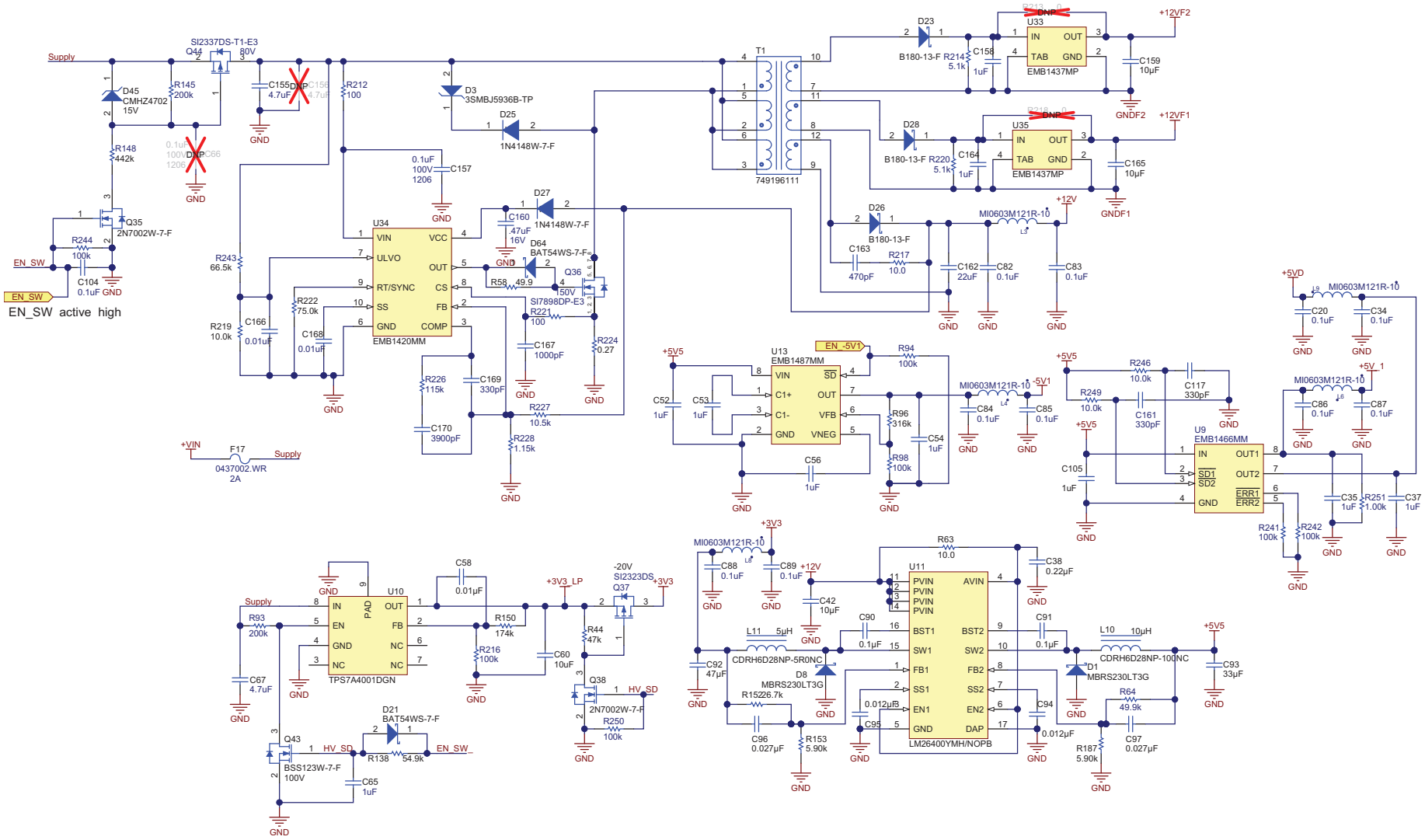


Figure E-10. Power Supply Schematic

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