REVISION HISTORY

Revision No.	Description of change	Release Date
V0.50	Initial release	

OZ8920

Battery Pack Protection and Monitor IC

FEATURES

- **Supports 5-8 Series Li-ion Battery Cells including Cobalt, Manganese and Phosphate Cells**
- **Multi-channel ADC for current, voltage and temperature measurement**
  - 8 channels for cell voltage measurement (12 bits).
  - 1 channel for current measurement (16 bits)
  - 1 channel for internal temperature measurement (12 bits)
  - 3 channels reserved for customer specific applications (12 bits, one for external extra channel; two for external temperature channels)
- **Built-in Protections include:**
  - Over voltage (OV)
  - Under voltage (UV)
  - Reversal voltage (RV)
  - Over current (OC)
  - Short circuit (SC)
  - Over temperature (OT)
  - Under temperature (UT)
  - Permanent Fail (PF)
- **Embedded 64X16 Bits EEPROM supports programmable settings of various protection thresholds/timers and protection release thresholds/timers**
- **Supports Internal/External Bleeding for Cell balance**
- **Supports hardware mode (without uP) or software mode (with uP)**
- **Supports separate charge and discharge loop**
- **Integrated 3.3V, 10V voltage regulator**
- **Integrated N-MOSFET driver**
- **Supports SMBus serial Interface**
- **Low power consumption**

APPLICATIONS

- **Electric Bicycle**
- **Electric Motorcycle**
- **Power Tools**
- **UPS backup battery**

GENERAL DESCRIPTION

OZ8920 is a highly integrated battery pack protection and monitor IC for managing Li-Ion or Li-polymer pack in electric bicycle, electric motorcycle, power tools, and UPS applications. It supports 5-8 series Li-Ion battery pack or Li-polymer battery pack applications.

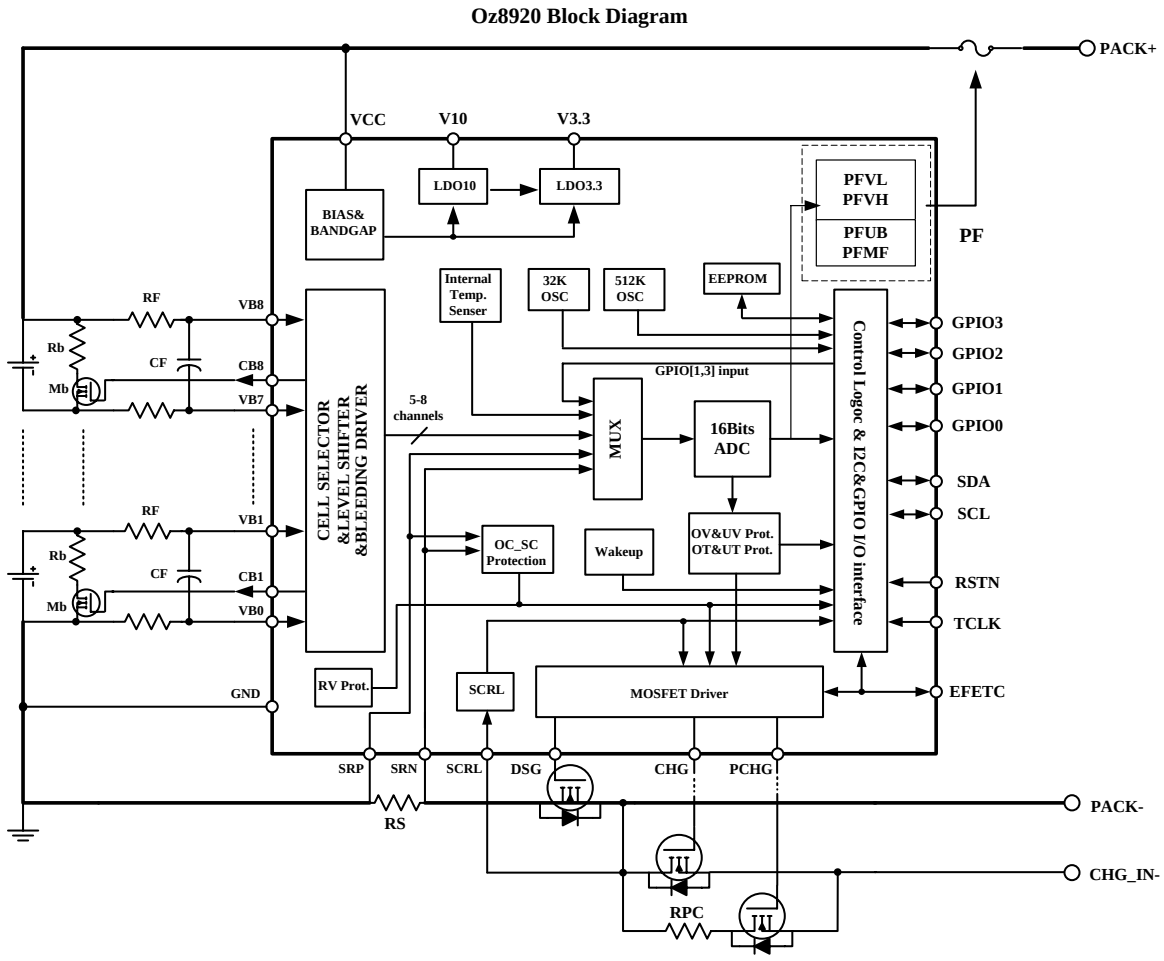
With integrated multi-channel 16-bit ADC, OZ8920 works constantly to monitor each cell's voltage, the charge/discharge current and the pack temperature to provide over-voltage, under-voltage, reversal voltage, over-current, short circuit, over-temperature and under-temperature safety protection. Working with embedded FET driver circuits, the protection circuits will independently shut off the FETs when the battery cells are experiencing extreme stress. When cell voltage is higher than the pre-set maximum rating voltage PFVH or lower than pre-set lowest working voltage PFVL, OZ8920 can automatically assert the Permanent Fail (PF) signal to blow an external fuse to cut off the power line or to signal an alarm to user. All of the protection thresholds and their related delay time are programmable in EEPROM for different battery types and different applications.

"Balance on Demand (BOD)" technology has been embedded in the OZ8920 to support internal/ external bleeding for cell voltage balance during charge state and optional idle state (no charge and discharge) (1 bit EEPROM configuration); BOD technology can achieve the longer life cycle of the battery pack..

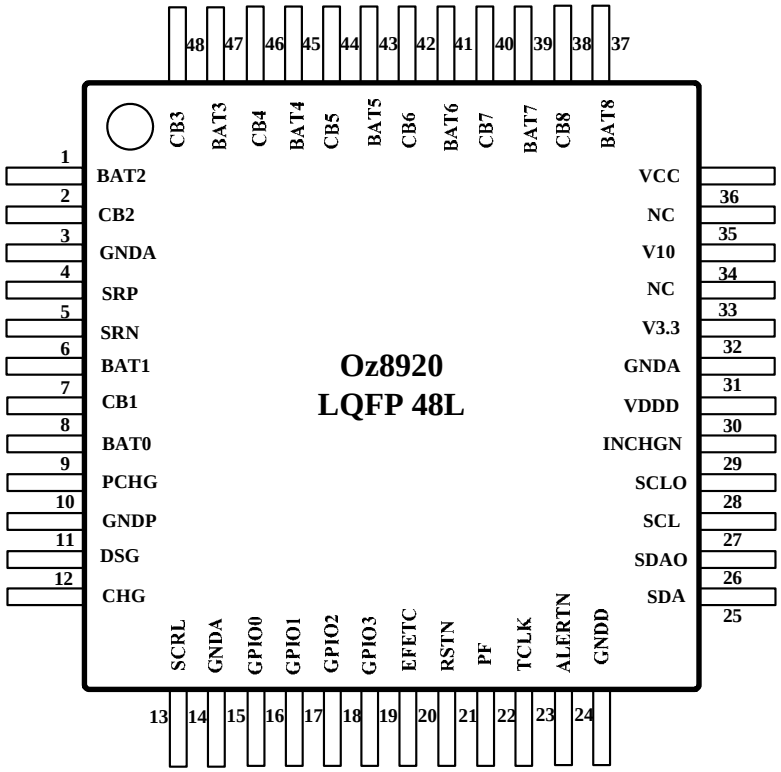
OZ8920 can be configured to work in hardware mode (without uP) or software mode (with uP) by embedded EEPROM. In hardware mode OZ8920 can work independently for battery pack protection and Monitoring. In software mode, OZ8920 can work with external uP or MCU to implement a more accurate coulomb counting gas gauge function.

Package: LQFP 48L
Operating Temperature Range:
-40°C to +85°C

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

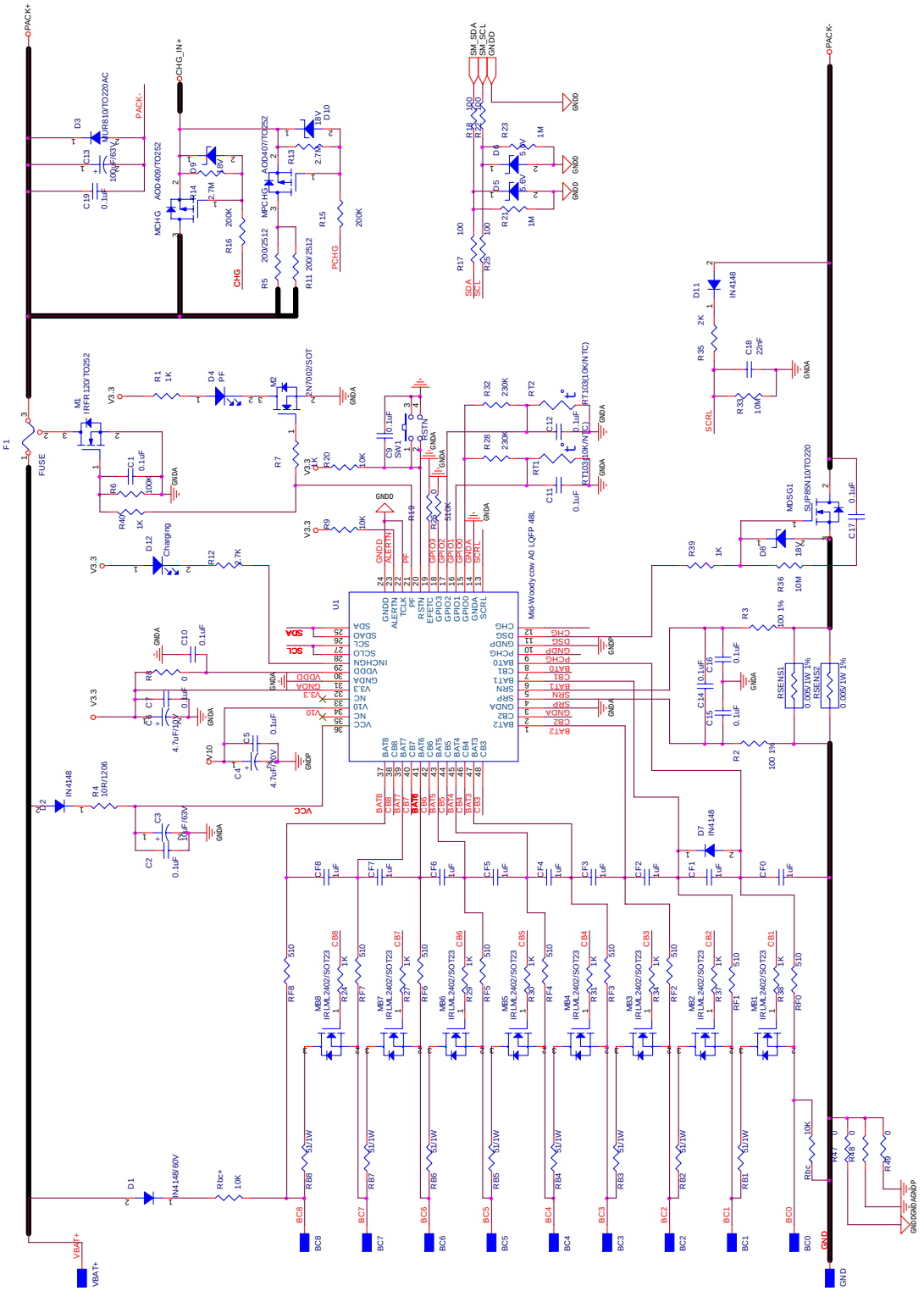
Name	Pin No	I/O	Description	
			Hardware Mode	Software Mode
BAT2	1	I	Cell2 positive input	
CB2	2	O	Cell2 external bleeding control	
GNDA	3	Ground	Analog ground	
SRP	4	I	Current sense resistor positive terminal	
SRN	5	I	Current sense resistor negative terminal	
BAT1	6	1	Cell1 positive input	
CB1	7	O	Cell1 external bleeding control	
BAT0	8	I	Cell1 negative input	
PCHG	9	O	Pre-charge MOSFET control	
GNDP	10	Ground	MOSFET driver power ground	
DSG	11	O	Discharge MOSFET control	
CHG	12	O	Charge MOSFET control	

Name	Pin No	I/O	Description	
			Hardware Mode	Software Mode
SCRL	13	I	Short circuit external automatic release input	
GNDA	14	Ground	Analog ground	
GPIO0	15	I/O	External thermal sensor driver voltage	GPIO0
GPIO1	16	I/O	External thermal sensor input	GPOI1
GPIO2	17	I/O	External thermal sensor input	GPIO2
GPIO3	18	I/O	External thermal sensor input	GPIO3
EFETC	19	I/O	External FET control signal, can be configured to input or output	External shutdown
RSTN	20	I/O	External reset input	
PF	21	O	Permanent failure output. Active high	
TCLK	22	I	External clock input	
ALERTN	23	O	Interrupt output in software mode. Active low	
GNDD	24	Ground	Digital ground	
SDA	25	I/O	4-wire SMBUS data input	
SDAO	26	I/O	4-wire SMBUS data output	
SCL	27	I/O	4-wire SMBUS clock input	
SCLO	28	I/O	4-wire SMBUS clock output	
INCHGN	29	O	Indicates “In charge” state. Active low	
VDDD	30	Power	Digital 3.3V power	
GNDA	31	Ground	Analog ground	
V3.3	32	Power	3.3V power supply	
NC	33	--		
V10	34	Power	10V power supply	
NC	35	--		
VCC	36	Power	Chip Power supply	
BAT8	37	I	Cell8 positive input	
CB8	38	O	Cell8 external bleeding control	
BAT7	39	I	Cell7 positive input	
CB7	40	O	Cell7 external bleeding control	
BAT6	41	I	Cell6 positive input	
CB6	42	O	Cell6 external bleeding control	
BAT5	43	I	Cell5 positive input	
CB5	44	O	Cell5 external bleeding control	

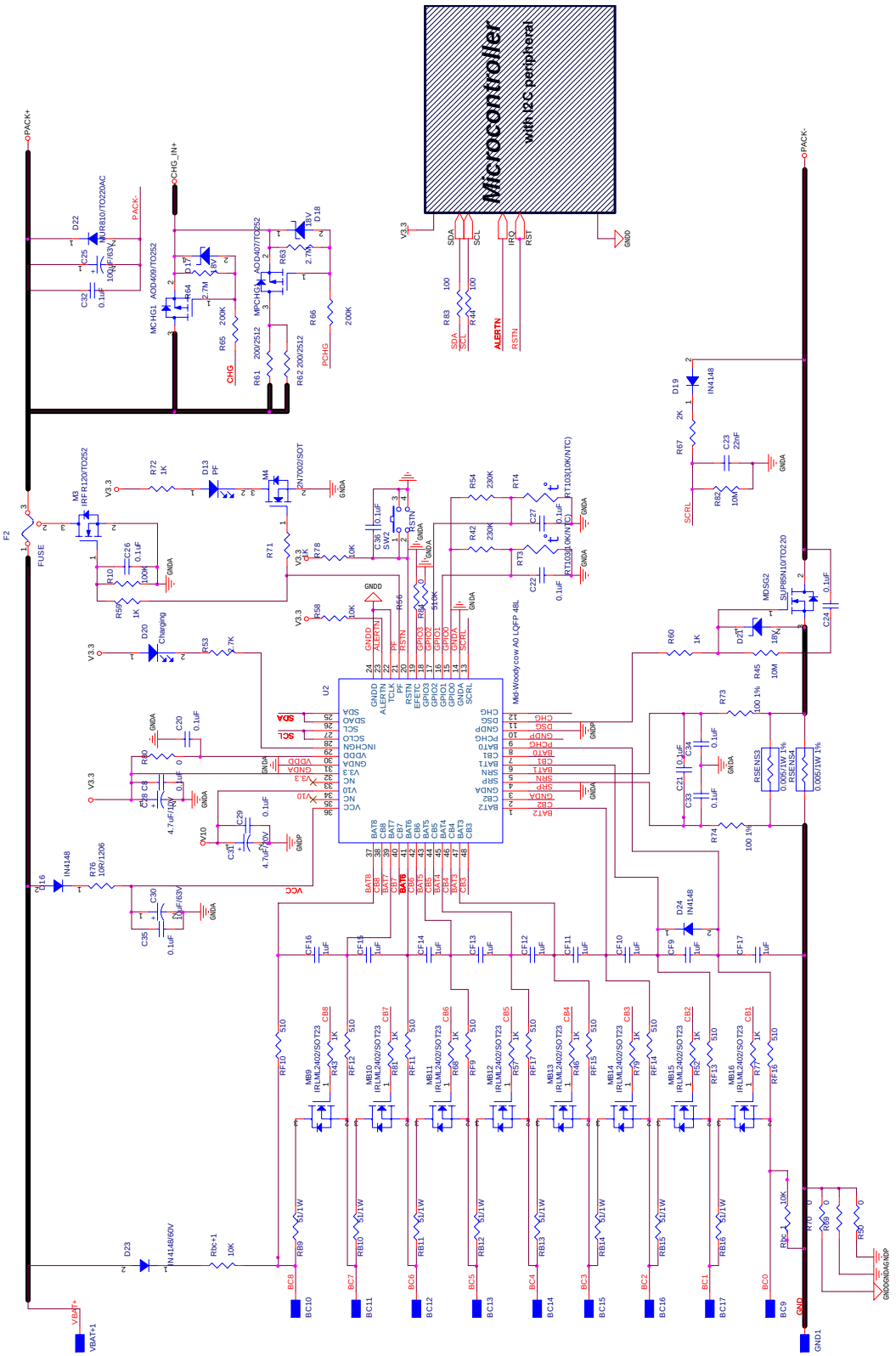
Name	Pin No	I/O	Description	
			Hardware Mode	Software Mode
BAT4	45	I	Cell4 positive input	
CB4	46	O	Cell4 external bleeding control	
BAT3	47	I	Cell3 positive input	
CB3	48	O	Cell3 external bleeding control	

TYPICAL APPLICATION SCHEMATICS

Hardware Mode



Software Mode



DC CHARACTERISTICS

Absolute Maximum Ratings

Supply voltage range		VCC	-0.3V to 48V
Input	Analog	SRP,SRN	-0.3V to 5.5V
	Analog	THERMV(power supply for temperature sense resistor)	-0.3V to 5.5V
	Analog	THERM1(12bits ADC input),THERM2(12bits),THERM3(12bits)	-0.3V to 5.5V
	Analog	BAT0 to BAT1,BAT1 to BAT2,BAT2 to BAT3,BAT3 to BAT4,BAT4 to BAT5,BAT5 to BAT6,BAT6 to BAT7,BAT7 to BAT8	-0.3V to 5.5V
	Analog	SCRL	-0.3V to 48V
	Digital	RSTN, TCLK	-0.3V to 5.5V
		All other input pins	
Output	Analog	PCHG,CHG	-0.3V to 48V
	Analog	DSG	-0.3V to 10V
	Digital	PF	-0.3V to 5.5V
	Digital	CB1,CB2,…CBn…CB8	(n-1)*Vcell to n*Vcell
I/O	Digital	GPIO[0:3], SCLO, SCL, SDAO, SDA, EFETC, INCHGN	-0.3V to 5.5V
Operating free-air temperature range, TA			-40℃ to 85℃
Storage temperature range, Tstg			-55℃ to 150℃
Lead temperature(soldering, 10 sec)			300℃

Note 1: All voltages are with respect to ground of this device except BATn - BAT(n-1),where n=1,2,3,4,5,6,7,8 cell voltage
Note 2: Ground refers to common node of GNDA, GNDD, and GNDP

Electrical Characteristics

Power Supply					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Supply Voltage(VCC)		8		48	V
Supply Current	Normal Mode		590		uA
	Sleep Mode		38		uA
	Shut Down		24		uA

General Purpose Inputs And Outputs(GPIO)					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
V_{IH} High-level Input Voltage		2			V
V_{IL} Low-level Input Voltage				0.8	V
V_{OH} Output Voltage High	ILoad=-0.5mA	V3.3-0.7			V
V_{OL} Output Voltage Low	ILoad=0.5mA			0.4	V
Current Drive Capability	GPIO0		1		mA
Current Drive Capability	GPIO1, 2, 3		8		mA

3.3V LDO Regulator					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Regulator Output Voltage	I_o<60mA	2.97	3.3	3.63	V
Line Regulation @ iload=32.8mA		-52			dB
Load Regulation @ Vcc=32V				127	mV
3.3V Current Limit				60	mA

10V LDO Regulator					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Regulator Output Voltage		9.45	10.5	11.55	V
Line Regulation @ iload=32.8mA		-45			dB
Load Regulation @ Vcc=32V				184	mV
10V Current Limit				60	mA

Multi-Channel ADC						
Parameter		**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Current Channel (1 channel)	Input Voltage Range		-250		250	mV
	Resolution			16 bits		
	Conversion Time				256	mS
	Offset		Auto offset cancellation			
	Slope		In software mode, support slope calibration			
Lion-ion Cell Voltage Channel	Input Voltage Range		-0.3		5	V
	Resolution			12 bits		
	Conversion Time				16	mS
	Offset		Auto offset cancellation			
	Slope		In software mode, support slope calibration			

Internal Temperature (1 channel)	Input Voltage Range		0.1		2.5	V
	Resolution			12 bits		
	Conversion Time				16	mS
	Offset		Auto offset cancellation			
	Slope		In software mode, support slope calibration			
GPIO[1:2] channel	Input Voltage Range		0.1		2.5	V
	Resolution			12 bits		
	Conversion Time				16	mS
	Offset		Auto offset cancellation			
	Slope		In software mode, support slope calibration			
GPIO[3]	Input Voltage Range		0.1		2.5	V
	Resolution			12 bits		
	Conversion Time				16	mS
	Offset		Auto offset cancellation			
	Slope		In software mode, support slope calibration			

Internal Oscillator					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
512kHz Oscillator Frequency		470	512	552	KHz
32kHz Oscillator Frequency		21	29	37	KHz

Over-Current(OC) And Short-Circuit(SC) Protection				
Parameter	**Test Conditions**	**MIN**	**MAX**	**Step/Unit**
OC0 Detection Threshold Range (16-bit setup)		16 bits programmable		Negative ADC Value
OC0 Delay Time(3-bit setup)		2	32	Scan Cycle
OC0 Release Time(3-bit setup)		2	32	Scan Cycle
OC Detection Threshold Range	Charge	10mV	105mV	5mV
	Discharge	30	285mV	5mV
OC Hysteresis Value	Charge	N/A		
	Discharge	11mV		mV
OC Delay Time (8-bit setup)		2ms	16.3s	***Note1***
OC Release Time (3-bit setup)	Charge	1s	32s	Variable
	Discharge	1s	32s	Variable
SC Detection Threshold Range	Discharge	50mV	620mV	10mV

Parameter	Test Conditions	MIN	MAX	Step/Unit
SC Hysteresis Value	Charge	N/A		
	Discharge	15mV		mV
SC Delay Time (8-bit setup)		8us	32.8ms	***Note 2***
SC Release Time (3-bit setup)		0.25min	1.75min	0.25min

Note1: 8-bit OC delay control byte divided into two sections, The high 5 bits are used to indicate the over current delay time as N+1 (N is the 5 bits value) delay units ; the low 3 bits are used to indicate the OC delay unit as following:

OC delay scale	OC delay unit	OC delay scale	OC delay unit
3'b000	2ms*1=2ms	3'b100	2ms*31=62ms
3'b001	2ms*3=6ms	3'b101	2ms*63=126ms
3'b010	2ms*7=14ms	3'b110	2ms*127=254ms
3'b011	2ms*15=30ms	3'b111	2ms*255=510ms

The OC delay time = (N+1)*(OC delay unit), so its range is 2ms~16.3s

Note2: 8-bit SC delay control byte divided into two sections. The high 5 bit are used to indicate the short circuit delay time as N+1 (N is the 5 bits value) delay units; the low 3 bits are used to indicate the SC delay unit as following:

SC delay scale	SC delay unit	SC delay scale	SC delay unit
3'b000	4us*2=8us	3'b100	4us*32=128us
3'b001	4us*4=16us	3'b101	4us*64=256us
3'b010	4us*8=32us	3'b110	4us*128=512us
3'b011	4us*16=64us	3'b111	4us*256=1024us

The SC delay time = (N+1)*(SC delay unit), so its range is 8us~32.8ms

Over-Voltage(OV) And Under-Voltage(UV) Protection					
Parameter	**Test Condition**	**MIN**	**TYP**	**MAX**	**Unit/step**
OV Detection Threshold Value		12bits programmable (0-5V)			V
OV Release Value		12bits programmable (0-5V)			V
OV Delay Time (4-bit setup)		1		16	Scan Cycle
OV Release Time (same as OV delay time)		1		16	Scan Cycle
UV Detection Threshold Value		12bits programmable (0-5V)			V
UV Release Value		12bits programmable (0-5V)			V
UV Delay Time (4-bit setup)		1		16	Scan Cycle
UV Release Time (same as UV delay time)		1		16	Scan Cycle
RV Detection Threshold Value			1.0V		
RV Release Value		Same as UV release value			
RV Delay Time (2-bit setup)		2ms		8ms	Variable

Permanent Fail Voltage (PFVL, PFVH and Cell Un-balance PF) Protection					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**units/step**
PFVL Threshold Range		12bits programmable (0-5V)			V
PFVL Delay Time (4bits setup)		1		16	Scan Cycle
PFVH Threshold Range		12bits programmable (0-5V)			V
PFVH Delay Time (4bits setup)		1		16	Scan Cycle
Cell Un-balance PF threshold Range		12bits programmable(0-5V)			V
Cell un-balance PF Delay Time (4bits setup)		1		16	Scan Cycle

Internal Thermal Protection (OT & UT)					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit/Step**
OT Detection Threshold value		User Programmable			1°C /2.1mV
OT Detection release Range		User Programmable			1°C /2.1mV
OT Delay Time (4-bit setup)		1		16	Scan Cycle
OT Release Time (same as OT delay time)		1		16	Scan Cycle
UT Detection Threshold Value		User Programmable			V
UT Detection Release Value		User Programmable			V
UT Delay Time (4-bit setup)		1		16	Scan Cycle
UT Release Time (same as UT delay time)		1		16	Scan Cycle

External Thermal Protection (OT & UT)					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit/Step**
OT Detection Threshold value		User Programmable			***(Note1)***
OT Detection release Range		User Programmable			***(Note1)***
OT Delay Time (4-bit setup)		1		16	Scan Cycle
OT Release Time (same as OT delay time)		1		16	Scan Cycle
UT Detection Threshold Value		User Programmable			V

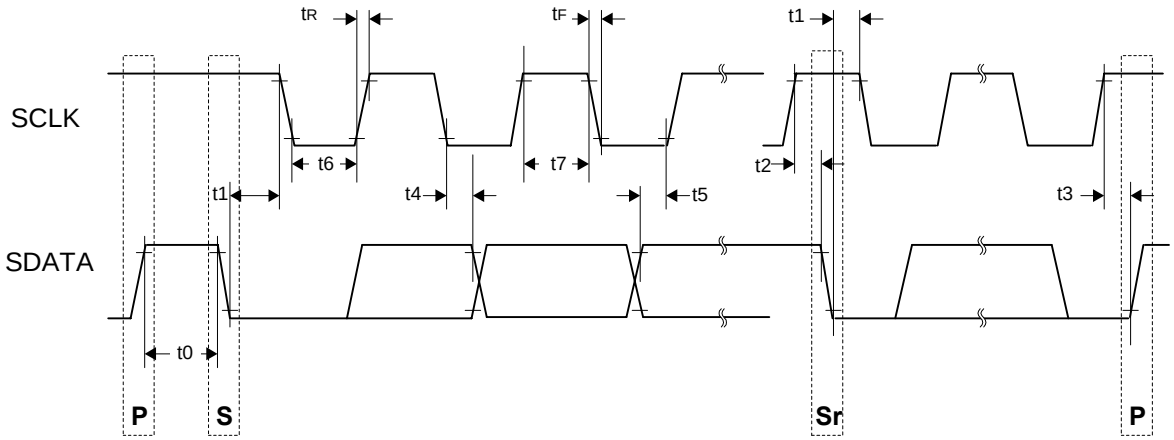
External Thermal Protection (OT & UT)					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit/Step**
UT Detection Release Value		User Programmable			V
UT Delay Time (4-bit setup)		1		16	Scan Cycle
UT Release Time (same as UT delay time)		1		16	Scan Cycle

Note1: Depends on external temperature sensor characteristics, refer to 'External Temperature Sensor'.

Power MOSFET Driver Circuit					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
CHG High Level			Vcc		V
CHG Low Level			Vcc-10		V
PCHG High Level			Vcc		V
PCHG Low Level			Vcc-10		V
Rise Time			TBD		
Fall Time			TBD		
DSG High Level		9.45	10.5	11.55	V
DSG Low Level		0		0.5	V
Rise Time			TBD		
Fall Time			TBD		

AC TIMING

SMBUS Bus Timing



Symbol	Parameter	Limits		*Units*	Note
		Min	Max		
FSMB	SMBUS Bus Operating Frequency	10	250	KHz	
t0	Bus free time between Stop and Start condition	4.7	-	µs	
t1	Hold time after (Repeated) Start condition. After this period, the first clock is generated	4.0	-	µs	
t2	Repeated Start condition set up time	4.7	--	µs	
t3	Stop Condition setup time	4.0	-	µs	
t4	Data hold time	150	-	ns	
t5	Data setup time	250	-	ns	
TIMOUT		25	35	ms	See **Note 1**
t6	Clock low period	4.7	-	µs	
t7	Clock high period	4.0	50	µs	See **Note 2**
TLOW:SEXT	Cumulative clock low extend time (slave device)	-	25	ms	See **Note 3**
TLOW:MEXT	Cumulative clock low extend time (master device)	-	10	ms	See **Note 4**
tF	Clock/Data Fall time	-	300	ns	See **Note 5**
tR	Clock/Data Rise Time	-	1000	ns	See **Note 5**

Note 1: A device will timeout when any clock low duration exceeds this value
Note 2: t5 Max provides a simple guaranteed method for devices to detect bus idle conditions.
Note 3: TLOW:SEXT is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to stop. If a slave device exceeds this time, it is expected to release both its clock and data lines and reset itself.
Note 4: TLOW:MEXT is the cumulative time a master device is allowed to extend its clock cycles within one byte of a message as defined from start-to-ack, ack-to-ack, or ack-to-stop.
Note 5: Rise and Fall times are measured between 10% to 90% of the signal amplitude.

FUNCTIONAL DESCRIPTION

OZ8920 Power Up Sequence

Fig.1 shows the OZ8920 power up sequence. When power supply is applied to VCC, the common bias starts firstly, then 10V LDO and 3.3V LDO. When Vldo3.3>2.4V, the power on reset block generates Power On Reset (POR) signal to enable the 512K oscillator and initializes the digital section. When Power and clock are ready, the digital circuits will read EEPROM data, and then go to different working state based on the ***auto_scan_enable*** setting. If the ***auto_scan_enable*** (2-bit in EEPROM register ***Scan Rate [19h]***) is 00 (default), the OZ8920 will go to the assembly state, in this state, OZ8920 doesn't do ADC scan, only after pushing RSTN (reset pin), OZ8920 can go to the normal working state; if the ***auto_scan_enable*** bit is 11, OZ8920 will go to the normal working state directly.

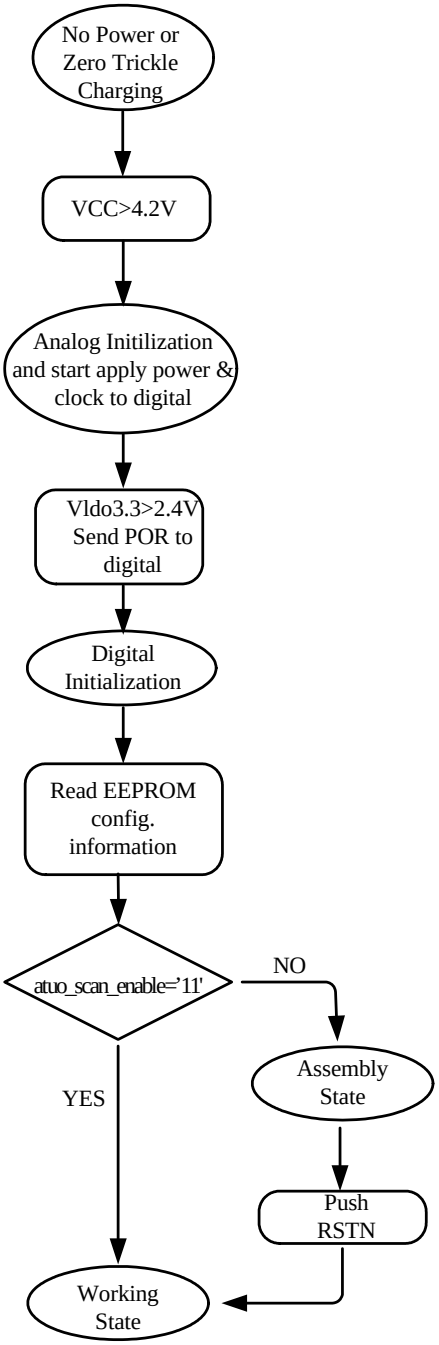


Fig. 1 OZ8920 Power Up

Measurements

OZ8920's multi-channel ADC (as shown in Fig. 2) measures up to 8 cell voltages, current, internal temperature and external temperature based on cyclic scan and time slot method. It will periodically measure all these values by predefined scan rate. During one measurement period, voltage, current, etc will be measured one by one in different time slot.

The ADC scan cycle period can be programmed in EEPROM register ***scan rate [19h]*** from 0.5S~16S.

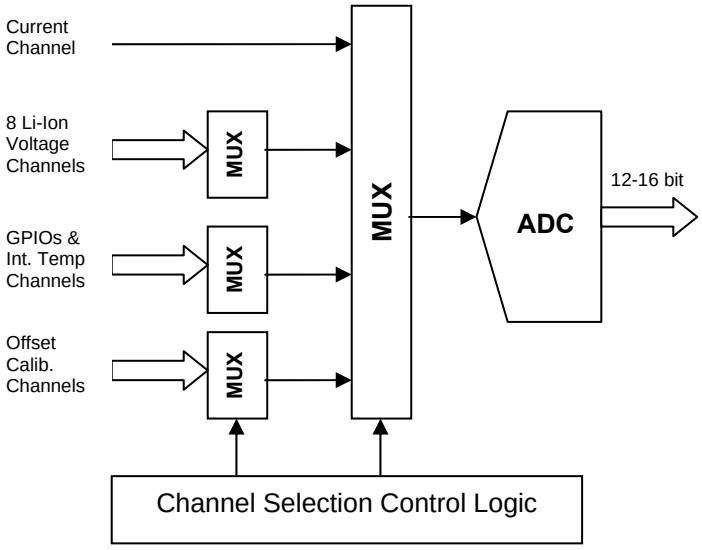


Fig. 2, Muti-Channel ADC

1. ADC Channel Description

a. Current Channel (1 channel)

This is a dedicated channel to measure the current across the sense resistor (2mΩ to 10mΩ), during charging and discharging for coulomb counting or other purpose.

Resolution: 16-bit (signed)
Input Voltage Range: ± 250mV
Auto offset cancellation
Slope calibration can be implemented in software mode for better accuracy.

b. Lion-ion Cell Voltage Channel (5~8 channels)

These channels are designed for cell voltage measurement.

Resolution: 12bits (signed)
Input Voltage Range: -0.3V~5.0V
Auto offset cancellation
Slope calibration can be implemented in software mode for better accuracy.

c. Internal Temperature (1 channel)

This channel is designed for internal temperature sensor.

Resolution: 12bits (signed)
Input Voltage Range: 0.1V~2.5V
Auto offset cancellation
Slope calibration can be implemented in software mode for better accuracy.

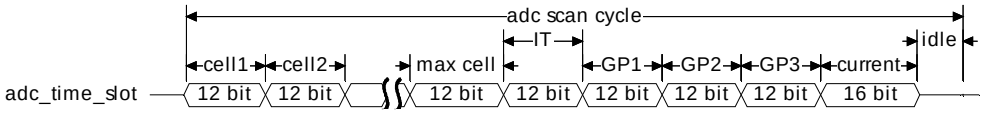
d. GPIO Channel (3 channel)

GPIO1, GPIO2 and GPIO3 can be configured as external temperature sensor (please refer to the external thermal sensor section) or other analog input in software mode, for detailed configuration information please refer to EEPROM register ***GP Mode [1ah]***.

GPIO1, GPIO2, GPIO3 can be configure to the external thermal sensor
- Accuracy: 12bits (signed)
- Input Voltage Range: 0.1V~2.5V
- Auto offset cancellation
- Slope calibration can be implemented in software mode for better accuracy.

GPIO1, GPIO2, GPIO3 can be configure to other analog input or digital I/O in software mode.

2. ADC Time Slot



Note:
(1) The time slot's length is not in scale.
(2) Max cell can be cell5~cell8.
(3) IT indicates 12-bit internal temperature channel.
(4) GP1 indicates 12-bit gpio1 channel; GP2 indicates 12-bit gpio2 channel; GP3 indicates 12-bit gpio3 channel. gpio1, gpio2, gpio3 channel can be scanned or not controlled by the control registers mapped from EEPROM; If gpio1, gpio2, gpio3 channel is not scanned, the corresponding ADC time slot will be skipped.

Internal/External Bleeding

OZ8920 can do cell bleeding for Li-ion batteries when the cells are being charged or in idle state. OZ8920 supports internal bleeding and external bleeding (can be configured by setting 1 Bit in EEPROM register ***[1dh]***: ***Select External Bleeding***). The bleeding function can also be disabled by setting 1 Bit in EEPROM register ***[18h]***: ***Hardware Bleeding Support***. Bleeding is performed during charging process or optionally during idle state (enable in EEPROM register ***[1d]***: ***Allow Idle Bleeding***) and start bleeding voltage point is programmable (***Bleeding Start:*** 12 Bits in EEPROM registers ***[56h, 57h]***).

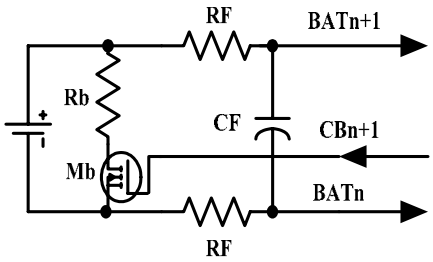


Fig.3 External Bleeding Diagram

For internal bleeding, the current will be 10mA~15mA for the thermal consideration, and the cell with highest voltage will be bled one time; for the external bleeding, bleeding current is decided by external bleeding resistor Rb (Fig. 3), and can support 1~4 or 7 maximum cell bleeding simultaneously (configured in EEPROM 1dh). Balance accuracy is programmable from 9.76mV~78.1mV (***Bleeding Accuracy:*** 3 Bits in EEPROM register ***[1dh]***).

OZ8920 has embedded O2micro "Balance on Demand (BOD)" technology:
- Battery pack is in charge state (current larger than charge current threshold) or in idle state (current smaller than charge current threshold and larger than discharge current threshold) if idle bleeding is enabled by setting 1 Bit in EEPROM register ***[1dh]***: ***Allow Idle Bleeding.***
- The bleeding function is enabled
- The highest cell voltage exceeds the ***Bleeding Start*** voltage
- The cell voltages' difference exceeds the ***Bleeding Accuracy***
- No error event, like OT, UT, UV, RV, OC0, OC, SC. If any error event happens, bleeding stops right away.

In software mode, hardware bleeding is supported by setting 1 Bit in EEPROM register ***[18h]***: ***Hardware Bleeding Support***. If software bleeding is selected, software can start cell bleeding by writing the bleeding control/statue register at any time. If any bleeding error(s) happen, the bleeding control/status will be automatically cleared to stop the bleeding (software can know the bleeding error exactly because any safety bleeding error will make ALERTN active to inform the software). If software wants to continue to do bleeding, it needs to write the bleeding control/status register again.

Battery Protection

OZ8920 includes a digital Battery Protection Engine (BPE), which can operate independently. The BPE constantly monitors data from the ADC and other protection circuits. If a protection error condition is detected and persists for certain time, the BPE will force the charge and/or discharge FET off. If some vital safety condition, such as extremely high cell voltage (PFVH) or extremely low cell voltage (PFVL), or extremely un-balanced cell voltage happens, or the Power MOSFET fails, the BPE will assert the Permanent Fail (PF) signal to instruct an optional external fuse circuit to permanently disable the battery pack. In software mode the chip provides an exclusive pin ALERTN to inform the uP while switching off the protection power mosfet when error condition happens.

1. Over-current (OC)

OZ8920 includes two level over current protection, first level OC0 is based on the ADC measured current value; second level OC is based on an independent hardware over-current detector (separate from the ADC) that monitors the sense resistor to detect over-current condition in either charge or discharge. If the over-current condition continues for a programmable delay time, the protection circuit will turn off the charge and discharge FETs. The charge and discharge over-current thresholds are set in protection register in EEPROM.

OC0 Protection Set

OC0 protection detection is for discharge current protection which is based on the current measurement of ADC, by comparing the 16-bit signed current value with the 16-bit signed threshold which is a negative value (indicating the discharge state). When current value < the threshold for a specified delay time, the OC0 state is detected; when current value >= the threshold, no OC0 state is detected. Please refer to EEPROM register information: ***OC0 Control [27h], OC0 Threshold [2ch, 2dh].***

When the OC0 state is detected and continues for some delay time selected by the 3-bit in EEPROM register ***OC0 Control [27h]***, all of the FETs (charge FET, discharge FET, precharge FET) will be turned off. When no OC0 continues for some delay time selected by 3-bit in EEPROM register ***OC0 Control [27h]***, charge FET and discharge FET will be turned on, if no other error(s) happen.

In general, compared to the OC protection, OC0's threshold is lower than that of OC protection and OC0's delay time is longer than the OC's one. For example, for discharge state, the absolute value of current is larger and larger, at first OC0's threshold is met, OC0 is detected; then, OC's (discharge OC) threshold is met, OC is detected. If user wants to disable the OC0 protection, he can set the OC0's threshold as most minimum value (16'8000) in EEPROM register ***OC0 Threshold [2ch, 2dh]***.

OC Protection Set

OZ8920 includes an independent hardware over-current detector that monitors the current that flows through the sense resistor to detect over-current condition in either charge or discharge. If the over-current condition continues for a programmable delay time, the protection circuit will turn off the charge and discharge FETs. The charge and discharge over-current thresholds are set in EEPROM registers ***Charge OC Threshold [1eh]*** and ***Discharge OC Threshold [1fh]***.
The real OC value is the Voc/Rs, where Rs is current sense resistor value. The over-current delay allows the system to momentarily accept a high current condition. The delay time can be programmed from 2ms to 16.3s by the parameter in EEPROM register ***OC Delay [2ah]***. Charge and discharge OC share the same delay time. Charge OC release time and Discharge OC release time can be programmed from 1second to 32 seconds in EEPROM register ***OC Release Control [2dh]*** independently.

Item		Description
OC Value	Charge	5bits EEPROM (***Charge OC Threshold [1eh]***) Control: Start: 10mV; Stop:105mV; Step:5mV
	Discharge	6bits EEPROM (***Discharge OC Threshold [1fh]***) Control: Start: 30mV; Stop:285mV; Step: 5mV
Hyst. Value	Charge	N/A
	Discharge	10mV
Delay Time		8bits EEPROM (***OC Delay [2ah]***) Configure, Range from 2mS to 16.3S
Release	Charge	3 bits EEPROM (***OC Release Control [2dh]***) Control: Range from 1S to 32S
	Discharge	3bits control external release or timer release (***OC Delay [2ah]***) Control: (000: external release; 001~111: 1S~31S)

2. Short-circuit (SC)

Short circuit protection is very similar to over-current protection. When short circuit condition is detected, OZ8920 will turn off charge and discharge FETs. Short circuit threshold and delay time can be programmed. Vsc can be programmed from 50mV to 620mV in 10mV steps by the parameter in EEPROM register ***SC Threshold [2bh]***. The real current is Vsc/Rs. Short circuit delay time can be programmed from 8us to 32.8ms. The short circuit delay time is configured by EEPROM register ***SC Delay [2ch]***. SC release time can be programmed in EEPROM register ***SC Release Control [2dh]*** from 0.25min~1.75min in 0.25min step. OZ8920 also supports an external release function, when SC happens, the chip will release when the input analog signal of Pin SCRL come back to the normal levels, this function is enabled by setting in EEPROM register ***SC Release Control [2dh].***

Item		Description
SC Value	Charge	N/A
	Discharge	6bits EEPROM (***SC Threshold [2bh]***) Control:Start:50mV; Stop:620mV; Step:10mV
Hysteresis Value		20mV
Delay Time		8bits EEPROM (***SC Delay [2ch]***) Configure, Range from 8uS to 32.8mS
Release		3bits EEPROM (***SC Release Control [2dh]***) Control: (000: external release; 001~111:0.25min~1.75min)

3. Over-voltage (OV)

The protection engine performs over-voltage detection by comparing 12 bit values from the ADC with an OV threshold, which is programmed in EEPROM register ***OV Threshold [38h, 39h]***. When over-voltage condition is detected, OZ8920 will turn off the charge FET after a specified delay time. This delay time can be programmed in EEPROM register ***OV Delay Control [25h]***. When cell voltage is less than the OV release value and persists for the specified time which is the same as OV delay time, OZ8920 Protection Engine will quit the OV condition and turn on the charge FET. The OV release value also can be programmed in EEPROM register ***OV Release [3ah, 3bh]***. The OV release value should set lower than OV threshold value.

4. Under-voltage (UV)

Under-voltage protection operates in the same way as over-voltage protection. When under-voltage condition is detected, OZ8920 will turn off discharge FET after a specified delay time. Its threshold can also be programmed in EEPROM register ***UV Threshold [3ch, 3dh]***. UV release value can be programmed in EEPROM register ***UV Release [3eh, 3fh]***. The UV release voltage value should be set higher than UV threshold value. Under-voltage protection and release has the same delay time as the over-voltage protection and release.

5. Reversal Voltage (RV)

OZ8920 incorporates cell reversal-voltage (RV) protection function. When cell voltage falls under about 1.0V, OZ8920 will turn off the discharge MOSFET immediately to prevent the battery cells from immediate reversal. The RV protection will be released only when cell voltage recovers to the configured release threshold voltage and delay a certain time which pre-configured. RV function and RV delay time can be set in EEPROM register Gp Mode [1ah]. RV release value and release delay time are the same as UV setting.

Item	Description
RV Value	About 1.0V
RV Release Value	Same as UV release value. ***UV Threshold [3ch, 3dh]***
RV Delay Time	2bits EEPROM (***Gp Mode [1ah]***) Control: (00:RV disable; 01~11:2ms~8ms)
RV Release Time	Same as UV release value. ***UV Release [3eh, 3fh]***

6. Thermal Protection (OT and UT)

Thermal protection is performed based on inputs from both the internal temperature sensor and the optional external temperature sensors. Thermal information may be used to temporarily interrupt the charge cycle and/or disable discharge. OZ8920 provides both under temperature (UT) and over temperature (OT) protection. When over-temperature is detected, OZ8920 will turn off charge and discharge FETs after a specified delay time; when under-temperature is detected, OZ8920 will turn off charge FET after a specified delay time and permit discharge if no other protection events happen. Both OT and UT thresholds are programmable. For discharge state, 12-bit DOTE threshold can be programmed in EEPROM registers ***DOTE Threshold [28h and 29h]***, 12-bit DOTE release value can be programmed in EEPROM registers ***DOTE Release [2ah, 2bh]***. For charge state, 12-bit COTE threshold can be programmed in EEPROM registers ***COTE Threshold [4eh and 4fh]***, 12-bit COTE release value can be programmed in EEPROM registers ***COTE Release [50h, 51h]***. External under temperature (UTE) threshold is set up in EEPROM registers ***UTE Threshold [52h, 53h],*** UTE release value can be programmed in EEPROM registers ***UTE Release [54h, 55h].*** Internal over temperature (OTI) threshold setting is in EEPROM registers ***OTI Threshold [4ah, 4bh].*** OTI release value can be programmed in EEPROM registers ***OTI Release [48h, 49h]***. Internal under temperature (UTI) threshold setting is in EEPROM registers ***UTI Threshold [4ah, 4bh]***. UTI release value is programmed in EEPROM registers ***UTI Release [4ch, 4dh]***. External and Internal OT/UT delay time can be programmed in EEPROM register ***OT/UT Delay Control [25h].***

7. Permanent Fail (PF) protection

a. Cell voltage extremely low or high permanent fail (PFVL and PFVH)

If any cell voltage lower than **PFVL** or higher than **PFVH** continues for pre-defined time (4-bit configuration in ***EEPROM register PF Control [26h]***), OZ8920 will assert a PF signal to blow the external fuse then shut down the system and the pack will be in permanent fail; this function acts as the secondary voltage protection and can be disabled by setting the ***PFVH enable*** and ***PFVL enable*** bits in the EEPROM register ***PF Control [26h]***. The PFVL and PFVH thresholds are programmable by setting the EEPROM register ***PFVH Threshold [40h, 41h]*** and ***PFVL Threshold [42h, 43h]***.

b. Cell voltage extremely unbalances permanent fail (PFUB)

If the (max cell voltage – min cell voltage) > the extremely unbalanced threshold voltage, the cell unbalance is detected, if the cell unbalance is detected for a specified delay time (4-bit configuration in ***EEPROM register PF Control [26h]***), it will send out PF to blow the external fuse and shut down the system. This function can be disabled by setting the ***PF unbalance enable*** bit in EEPROM register ***PF Control [26h].*** The PFUB threshold is programmable by setting the EEPROM register ***PF Unbalance Threshold [44h, 45h].***

c. MOSFET failure permanent fail (PFMF)

If the charge MOSFET, precharge MOSFET are both turned off, but the chip is in charge state (the current > the “in_charge” current threshold), the charge or pre-charge MOSFET will be regarded as failure; on the other hand, if the discharge MOSFET is turned off, but the chip is in discharge state (the

current < the "in_discharge" current threshold; the current, discharge current threshold both are negative value), the discharge MOSFET will be regarded as failure.
If the MOSFET fail is detected for a specified delay time (4-bit configuration in ***EEPROM register PF Control [26h]***), it will send out PF and shut down the system. This function can be disabled by setting the ***PF mosfet fail enable*** bit in EEPROM register ***PF Control [26h].***

PFVL threshold value [40h, 41h]	12Bits EEPROM programmable
PFVH threshold value [42h, 43h]	12Bits EEPROM programmable
PFUB threshold value [44, 45h]	12Bits EEPROM programmable
PF Mosfet Failure ***[26h]***	There is discharge current when discharge MOSFET is off or there is charge current when charge MOSFET is off
Release Value	N/A
Delay Time ***[26h]***	Range: 1~16 scan cycles Step: 1scan cycle

Power Mode

To save power, OZ8920 works in different power modes according to the system status. There are 3 power modes as follows:

Full Power Mode: < 750µA
Sleep Mode: < 50uA
Shut Down: <25uA

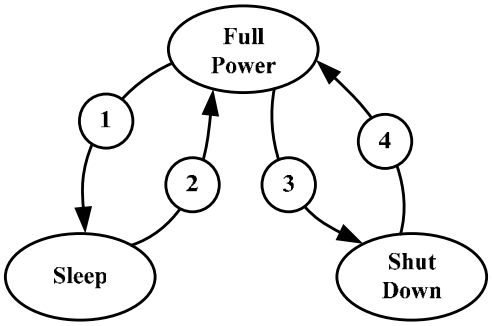


Fig. 4 OZ8920 Power Mode Diagram

State Description (Fig. 4)

State	Description
Full Power	Voltage, temp. and current scan Safety protection check
Sleep	Stop voltage, temp. and current scan Stop safety protection check Wake up ,RV protection block ,and SCRL pin is working
Shut Down	Only common bias is working Power consumption<25uA

Transition Description

Transition	Initial State	Condition		Final State
		Hardware Mode	Software Mode	
1	Full Power	➢ No charge/discharge and No protection event occurs for 10 minutes ➢ Sleep timer expired ➢ No bleeding event ➢ SMBUS is not active	uP makes decision	Sleep

Transition	Initial State	Condition		Final State
		Hardware Mode	Software Mode	
2	Sleep	➢ sleep timer expired ➢ SC or RV event occurs ➢ SMBUS is active ➢ EFETC Signal ➢ wake-up circuit detected ➢ charge/discharge current	uP makes decision	Full Power
3	Full Power	➢ PF (PFVL, PFVH, PFUB, PFMF) shut down ➢ EFETC shutdown active	uP makes decision	Shutdown
4	Shutdown	Any one of the Wake up events happens: ➢ EFETC shut down inactive ➢ Reset or SMBUS active for PF shutdown or software shutdown		Full Power

Internal Temperature Sensor

OZ8920 takes advantage of silicon device physics and circuit design technology for the internal temperature sensor. The internal temperature sensor generates a voltage level which is proportional to the temperature. As Fig.5 showing below, with a temperature increase of 1°C, internal temperature sensor output voltage will increase 2.0976mV. The offset can be get from the 12Bit EEPROM which measured in the ATE test. So, if at T0, ADC reading out VT0, the characteristic curve function can be get: VTS (mV)=2.0976*T+(VT0 – 2.0976*T0)

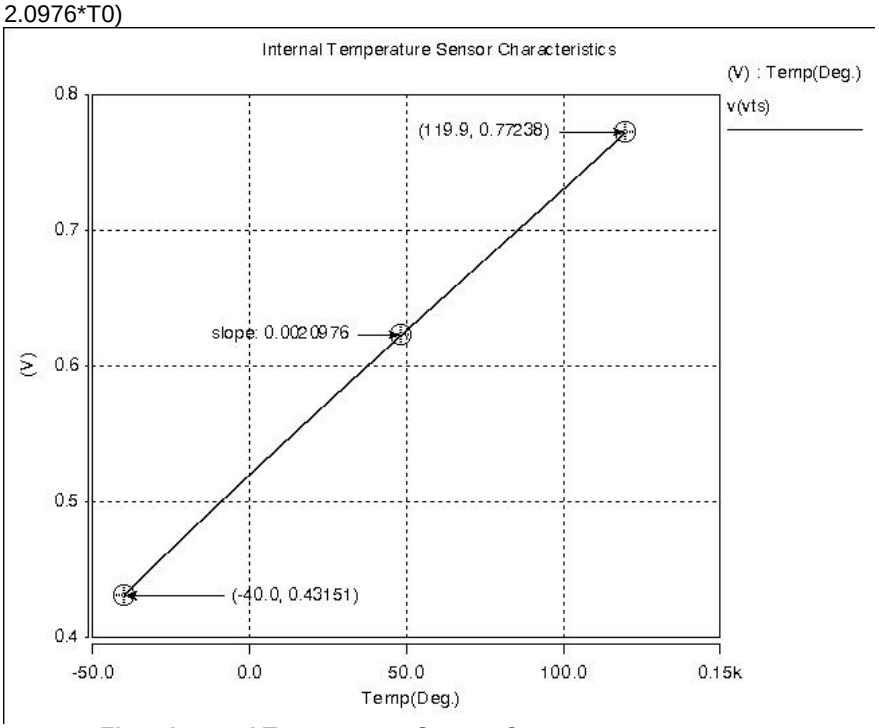


Fig. 5 Internal Temperature Sensor Curve

External Temperature Sensor

OZ8920 provides 3 GPIOs for external temperature detection, the application circuitry is shown in Fig.6. We recommend using 103 NTC type thermistor.
103 NTC Thermistor RT characteristics are shown in Fig. 7. The sensed voltage Vt characteristics are shown in Fig. 8

For Example: Vt2=3.3V * RT2 / (RB2 + RT2)

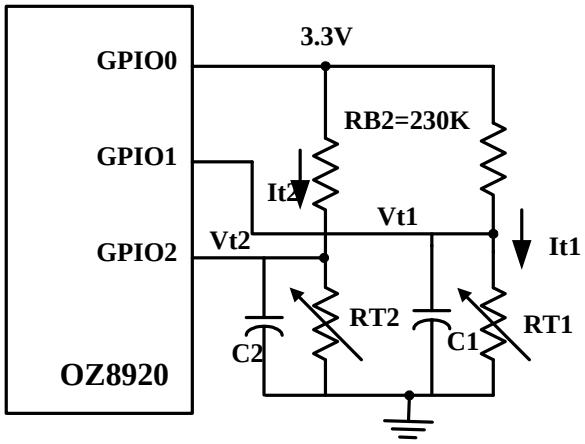


Fig.6 External Temperature Sensor Application

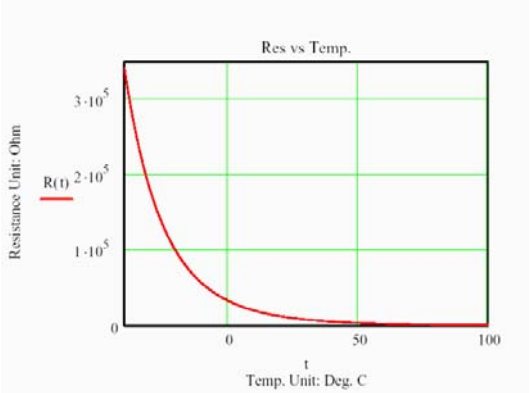


Fig.7 Thermistor RT characteristics

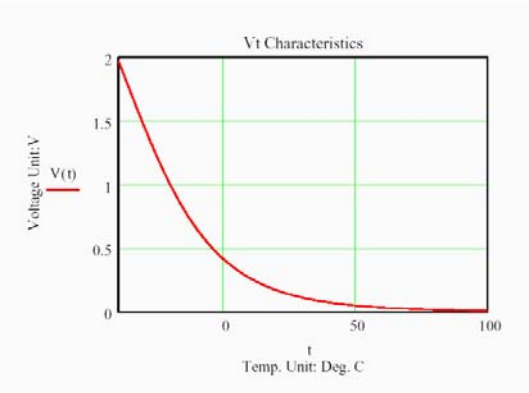


Fig.8 The sensed voltage Vt characteristics

Power MOSFET Driver Control

Smart MOSFET driver is designed for N-type MOSFET controlled charge, and discharge. The driver also supports parallel and series charge discharge loop.
The charge and discharge MOSFET are controlled through protection register, subject to override by the Battery Protection Engine (BPE). OZ8920 also provides a pin (EFETC) for external MOSFET control signal input or internal MOSFET control signal output①it makes the MOSFET control very flexible. The discharge (DSG) MOSFET gate-to-source voltage is clamped to 10V (typical) when MOSFET is in ON state; the charge and pre-charge MOSFET gate-to-source voltage is decide by external divider resistor and the pack voltage.

Note ① 2Bits in EEPROM configure the PIN's function: charge & discharge FET off (input), charge FET off (input), discharge FET off (input) and discharge FET off (output)

Serial Communication Bus

OZ8920 supports SMBus communication interface. The SMBUS master can access OZ8920's registers with SMBUS protocol. In this condition, OZ8920 is working as an SMBUS slave node.

2-wire SMBUS Bus
In this case, Pin27 should be shorted with Pin28 as input clock pin and the clock comes from external SMBUS host, Pin25 should be shorted with Pin 26 as bi-directional data pin. For detailed SMBUS protocol and timing information, please refer to the SMBUS Specifications.

4-wire SMBUS Bus
In this case, Pin28 is the output clock pin (SCLO) and Pin27 is the input clock pin (SCL), Pin26 is the output data pin (SDAO), Pin25 is the input data pin (SDA). This bus protocol and timing is the same as 2-wire SMBUS bus except separating input/output line.
4-wire SMBUS bus is used to support non-common ground communication.

Deadman

Deadman check function is enabled by a non-zero value to "***deadman control***" register (***operation register 2ch***). If deadman check is enabled, OZ8920 will increment the deadman timer every second when the safety scan is enabled. The software needs to do as following:

- Read the deadman timer by reading the operation register ***Deadman Timer 2dh***
- Write "1" into the bit 7 "clear deadman timer" of operation register ***Deadman Timer 2dh*** to clear the deadman timer.

If the handshake between OZ8920 and the software is normal, the software will clear the deadman timer before the deadman timer expires. In a result no deadman is found.
If the handshake has some problems, the software can not clear the deadman timer in time, while the deadman timer will do +1 every second. After some time, the deadman timer exprires. As a result, OZ8920 will send out a 64ms low active pulse to RSTN pin to reset the external uP.

It is noted that when starting up the deadman check, it's possible to get a false deadman. To avoid this problem, handshake procedure is needed immediately after writing a non-zero value to "deadman control".

EEPROM AND OPERATION REGISTERS MAP

OZ8920 has two types of registers. One type is OZ8920's operation registers which address is from 00h to 7fh; the other type is embedded EEPROM registers which address is from 00h to 7fh. Software can directly access OZ8920's operation registers via SMBUS bus; and software can access the EEPROM registers indirectly by access the operation register 5ch~5fh.

EEPROM registers are used to store important battery pack, battery cell information and to configure the OZ8920 chip. Operation registers are used to store ADC instant data, OZ8920 status information, and some parameters to control OZ8920 state-machine, etc. When system is powered on, the data in EEPROM register 12h-15h, 16h-27h, 5ah-5bh, 74h-75hwill be loaded into the Operation registers 02h-05h, 06h-17h, 18h-19h, 1ah-1bh respectively. Fig. 9 shows the configuration of EEPROM registers and Operation registers.

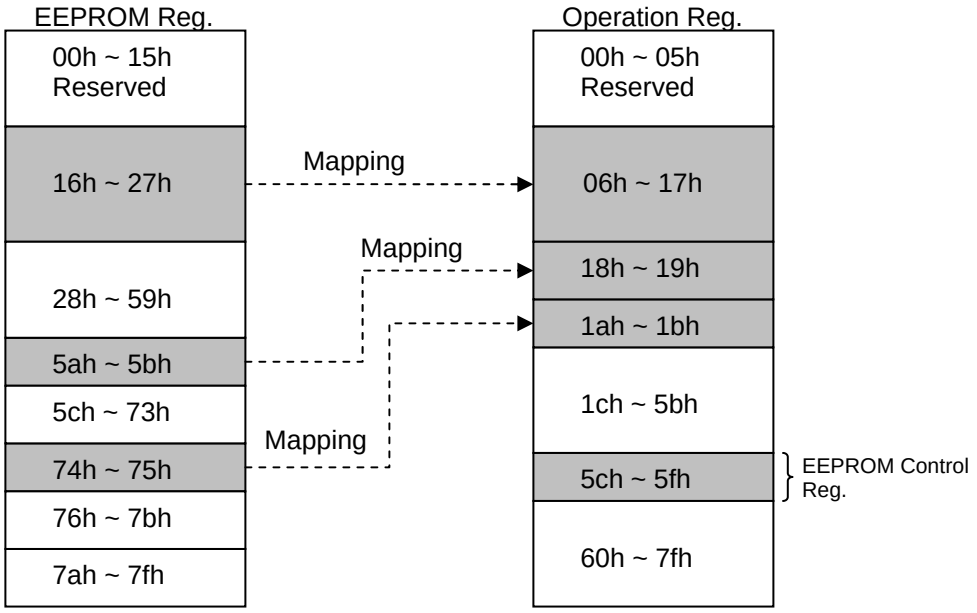


Fig.9 Configuration of EEPROM Register and Operation Register

EEPROM Section	Description
00h~15h ATE data	This section reserved for O2Micro internal use only.
16h~5bh User data	This section used for user control, programming data. 16h~27h are mapped into the Operation registers 06h~17h; 5ah~5bh are mapped into the Operation registers 18h~19h; Access is controlled by 2-bit ***paramter_access*** in bit7, bit6 of EEPROM register ***Parameter Access [5bh]***. Parameter_access = 00: the safety scan is disabled; readable; writable; Parameter_access = 01: the safety scan is enabled; readable; writable; Parameter_access = 10: the safety scan is enabled; read only; Parameter_access = 11: the safety scan is enabled; not-readable; not-writable
5ch~7bh Project info data	This section stores project information data. 74h~75h are mapped into the Operation registers 1ah~1bh. Access is controlled by 1-bit ***project_info_access*** in bit7 of EEPROM register ***Project Info Access [75h]***. Project_info_access = 0: readable; writable; Project_info_access = 1: not-readable; not-writable
7ch~7fh Log Data	These data are readable, writable always.

OZ8920 EEPROM Registers

Reg index (hex)	Reg Name	Bit Number 7	6	5	4	3	2	1	0
00~15	Reserved								
16	Cell Number	sda_delay_enable	pec enable	SMBus address config				Cell number	
17	Hardware Mode	reserved						hardware mode	
18	Function Support	reserved	efetc mode			reserved	Pre_charge support	hardware bleeding support	sleep support
19	Scan Rate	auto scan enable		reserved				scan rate	
1a	Gp Mode	rv support		gp3 mode		gp2 mode		gp1 mode	
1b	Charge/Discharge Threshold	reserved		charge threshold control		reserved		discharge threshold control	
1c	Sleep Control	charge integrator control		discharge integrator control		sleep time control			
1d	Bleeding Mode	select external bleeding	bleeding accuracy			allow idle bleeding	allow bleeding all	bleeding number	
1e	Charge OC Threshold	Reserved			charge OC threshold				
1f	Discharge OC Threshold	reserved		discharge OC threshold					
20	OC Delay	OC delay number					OC delay scale		
21	OC Release Control	reserved		discharge OC release control			charge OC release control		
22	SC Threshold	reserved		SC threshold					
23	SC Delay	SC delay number					SC delay scale		
24	SC Release Control	prmt_reserved4	prmt_reserved3	prmt_reserved2	prmt_reserved1	prmt_reserved0	SC release control		
25	OT/UT, OV/UV Delay Control	OT/UT delay				OV/UV delay			
26	Pf Control	pfvh enable	pfvl enable	pf unbalance enable	pf mosfet fail enable	pf delay			
27	OC0 Control	reserved		OC0 release control			OC0 delay		
28	DOTE Threshold	bit3~bit0 of discharge OTE threshold				Reserved			
29		bit11~bit4 of discharge OTE threshold							
2a	DOTE Release	bit3~bit0 of OTE release for discharge OTE				Reserved			
2b		Bit11~bit4 of OTE release for discharge OTE							
2c	OC0 Threshold	bit7~bit0 of OC0 (level-0 ocver current) threshold							
2d		bit15~bit8 of OC0 threshold							
2e~37	reserved	Reserved							

Reg index (hex)	Reg Name	Bit Number							
		7	6	5	4	3	2	1	0
38	OV Threshold	bit3~bit0 of OV threshold				Reserved			
39		bit11~bit4 of OV threshold							
3a	OV Release	bit3~bit0 of OV release				Reserved			
3b		bit11~bit4 of OV release							
3c	UV Threshold	bit3~bit0 of UV threshold				Reserved			
3d		bit11~bit4 of threshold							
3e	UV Release	bit3~bit0 of UV release				Reserved			
3f		bit11~bit4 of UV release							
40	Pfvh Threshold	bit3~bit0 of pfvh threshold				Reserved			
41		bit11~bit4 of pfvh threshold							
42	Pfvl Threshold	bit3~bit0 of pfvl threshold				Reserved			
43		bit11~bit4 of pfvl threshold							
44	Pf Unbalance Threshold	bit3~bit0 of pf unbalance threshold				Reserved			
45		bit11~bit4 of pf unbalance threshold							
46	OTI Threshold	bit3~bit0 of OTI threshold				Reserved			
47		bit11~bit4 of OTI threshold							
48	OTI Release	bit3~bit0 of OTI release				Reserved			
49		bit11~bit4 of OTI release							
4a	UTI Threshold	bit3~bit0 of UTI threshold				Reserved			
4b		bit11~bit4 of UTI threshold							
4c	UTI Release	bit3~bit0 of UTI release				Reserved			
4d		bit11~bit4 of UTI release							
4e	COTE Threshold	bit3~bit0 of charge OTE threshold				Reserved			
4f		bit11~bit4 of charge OTE threshold							
50	COTE Release	bit3~bit0 of OTE release for charge OTE or internal OT				Reserved			
51		bit11~bit4 of OTE release for charge OTE or internal							
52	UTE Threshold	bit3~bit0 of UTE threshold				Reserved			
53		bit11~bit4 of UTE threshold							
54	UTE Release	bit3~bit0 of UTE release				Reserved			
55		bit11~bit4 of UTE release							
56	Bleeding Start	bit3~bit0 of bleeding start				reserved			
57		bit11~bit4 of bleeding start							
58~59	Reserved	reserved							
5a	Reserved	reserved							

Reg index (hex)	Reg Name	Bit Number							
		7	6	5	4	3	2	1	0
5b	Parameter Access	parameter access		reserved					
5c	Current_ 2nd_offset	Low byte of current 2nd offset							
5d		High byte of current 2nd offset							
5e	Gpio1_2nd_offset	gpio1 2nd offset							
5f	Gpio2_2nd_offset	gpio2 2nd offset							
60	Gpio3_ 2nd_offset	gpio3 2nd offset							
61	Reserved	reserved							
62~6d	Factory Name	Factory Name(ASCII code)							
6e~72	Project Name	Project Name(ASCII code)							
73	Version Number	Version Number							
74	Reserved	reserved							
75	Project Info Access	project info access	reserved						
76	Reserved	reserved							
77	Reserved	reserved							
78~79	Reserved	reserved							
7a	Reserved	reserved							
7b	Reserved	reserved							
7c	Pf Record	reserved				pfvh	pfvl	pf unbalance	pf mosfet fail
7d~7f	Reserved	reserved							

Detailed EEPROM Register Information

EE register 00h~15h are reserved for OZ8920 chip's internal use. Some of the data in this area are mapped into operation register 02h~05h..

EE register 16h ~ 5bh are paramter data which are used by customer for OZ8920 chip configuration, battery management control setup and customer information purpose. EE register 16h ~ 27h, 5bh are mapped to operation register 06h ~ 17h, 19h respectively. Its access is controlled by the EEPROM-mapped 2-bit ***parameter access***.

Register 16h−Cell Number Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
16h	sda_delay_enable	pec_enable	SMBus address config				cell number	

This register specifies cell number, SMBus address, sda delay and pec control.

Bit #	Name	Description	R/W	Default Value
7	sda_delay_enable	Control the extra delay on SDA input line. If "1", enable the extra delay on SDA input line; if "0", disable the extra delay on SDA input line.	RW	0h
6	pec_enable	Enable PEC (packet error check) function in SMBUS protocol. If "1", enable the PEC function; if "0", disable the PEC function. It is noted that when pec enable bit is "1", OZ8920 only support s one-byte SMBUS PEC-write, one-byte SMBUS PEC-read; doesn't support multi-byte SMBUS PEC-write, doesn't support multi-byte SMBUS PEC-read.	RW	0h
5:2	SMBus address config	Specify the 8-bit SMBus device address as 8'h60 + 2*N.	RW	0h
1:0	cell number	Specify the cell count in the battery pack as following: cell number: 2'b00 → cell count in the battery pack: 5 2'b01 → 6 2'b10 → 7 2'b11 → 8	RW	0h

Register 17h −Hardware Mode Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
17h	reserved						Hardware mode	

This register selects hardware mode or software mode.

Bit #	Name	Description	R/W	Reset Value
7:2	reserved	Reserved.	R	0h
1:0	Hardware mode	Select hardware mode or software mode. If "0", "1", "3", select hardware mode; if "2", select software mode. this bit can not be written directly via SMBus interface. Instead this bit can be changed only when EEPROM mapping.	R	1h

Register 18h − Function Support Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
18h	reserved	efetc mode			reserved	Precharge support	Hardware bleeding support	Sleep support

This register specifies efetc mode, precharge, hardware bleeding and sleep control.

Bit #	Name	Description	R/W	Reset Value
7	reserved	reserved	R	0h
6:4	EFETC mode	Select EFETC pin function as following: EFETC mode / EFETC pin function 000: Input signal to disable charge fet.. If "1", disable charge fet forcely; if "0", charge fet is controlled by the internal logic. 001: Input signal to disable discharge fet. If "1", disable discharge fet forcely; if "0", discharge fet is controlled by the internal logic. 010: Input signal to disable charge/discharge fet. If "1", disable charge fet and discharge fet forcely; if "0", charge fet and discharge fet are controlled by the internal logic. 011: To output discharge fet control logic 100: Input shut down signal. If "1", shut down OZ8920; if "0", OZ8920 works normally. 101, 110, 111: Reserved.	RW	0h
3	Reserved	reserved	R	0h
2	Precharge support	Support precharge function. If "1", support precharge function; if "0", don't support precharge function.	RW	0h
1	Hardware bleeding support	Select hardware bleeding or software bleeding. If "1", select hardware bleeding; if "0", select software bleeding, software can control the bleeding by writing the bleeding control/status register.	RW	0h
0	Sleep support	Support sleep function. If "1", support sleep function; if "0", don't support sleep function.	RW	0h

Register 19h –Scan Rate Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
19h	auto_scan_ebale		reserved			scan rate		

This register specified auto scan control and configuration.

Bit #	Name	Description	R/W	Default Value
7:6	auto_scan_enable	auo scan control. If "01", "10", "11", auto scan is enabled. After power on reset, the safety scan will automatically start afterEEPROM mapping. if "00", auto scan is disabled. After power on reset, the safety scan will not start after EEPROM mapping until the detection of a low pulse on RSTN pin. For reliability reason, if want to enable auto scan, we need to set it to "11"; if want to disable auto scan, we need to set it to "00".	RW	0h
5:3	reserved	reserved	R	0h

Bit #	Name	Description	R/W	Default Value
2:0	scan rate	Select the safety scan period as following table: scan rate / scan period 000 / 1s 001 / 2s 010 / 4s 011 / 6s 100 / 8s 101 / 12s 110 / 16s 111 / 0.5s	RW	0h

Register 1ah –GPIO Mode Control Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1ah	RV protection control		gpio3 mode		gpio2 mode		gpio1 mode	

This register sets GPIO mode and reversal voltage control.

Bit #	Name	Description	R/W	Reset Value
7:6	RV protection control	RV(Reverse Voltage) Protection control as following: RVcontrol / RV function 2'b00 / RV protection function is disabled. 2'b01 / RV delay time is 2ms 2'b10 / RV delay time is 4ms 2'b11 / RV delay time is 8ms	R	0h
5:4	gp3 mode	Select gpio3 function as following: gpio3 mode / gpio3 function 2'b00 / not-scanned analog pin. 2'b01 / scanned analog pin (12-bit adc channel); no temperature check on gp3. 2'b10 / scanned analog pin (12-bit adc channel); temperature check on gp3. 2'b11 / a digital pin.	RW	0h
3:2	gp2 mode	Select gpio2 function as following: gpio2 mode / gp2 function 2'b00 / not-scanned analog pin. 2'b01 / scanned analog pin (12-bit adc channel); no temperature check on gp2. 2'b10 / scanned analog pin (12-bit adc channel); temperature check on gp2. 2'b11 / a digital pin.	RW	0h
1:0	gp1 mode	Select gpio1 function as following: gpio1 mode / gp1 function 2'b00 / not-scanned analog pin. 2'b01 / scanned analog pin (12-bit adc channel); no temperature check on gp2. 2'b10 / scanned analog pin (12-bit adc channel); temperature check on gp2. 2'b11 / a digital pin	RW	0h

Register 1bh−Charge/Discharge Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1bh	reserved		charge_threshold control		reserved		discharge_threshold control	

This register sets charge/discharge state threshold.

Bit #	Name	Description	R/W	Default Value
7:6	reserved	Reserved.	R	0h
5:4	charge_threshold control	Specify charge state current threshold as following: charge_threshold control: charge state threshold(Unit is current ADC's LSB) 2'b00: 8 2'b01: 16 2'b10: 32 2'b11: 64 If the current > charge state threshold, the chip will be regarded in charge state; otherwise the chip is not in charge state.	RW	0h
3:2	reserved	Reserved.	R	0h
1:0	discharge_threshold control	Specify the discharge state current threshold as following: discharge_th control: discharge state threshold(Unit is current ADC's LSB) 3'b000: -16 3'b001: -32 3'b010: -64 3'b011: -128 If the current < the discharge state threshold, the chip will be regarded in_discharge state; otherwise the chip is not in discharge state.	RW	0h

Register 1ch −Sleep Control Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1ch	Charge integrator control		Discharge integrator control		Sleep time control			

This register specifies sleep time control and charge/discharge integrator control.

Bit #	Name	Description	R/W	Default Value
7:6	Charge integrator control	Control the time width of charge integrator to define the charge wake up current: charge integrator control: The integrating time width 2'b00: 8ms 2'b01: 16ms 2'b10: 32ms 2'b11: 64ms	RW	0h
5:4	Discharge integrator control	Control the time width of charge integrator to define the discharge wake up current: Discharge integrator control: The integrating time width 2'b00: 8ms 2'b01: 16ms 2'b10: 32ms 2'b11: 64ms	RW	0h
3:0	Sleep time control	Control the sleep time as following: Sleep time control: Sleep time	RW	0h

Bit #	Name	Description	R/W	Default Value
		4'b0000 disable sleep time expired wakeup function. 4'b0001 1 minutes … N minutes 4'b1111 15 minutes In sleep mode every sleep time, the chip will wake up to enter into full power mode to check the events.		

Register 1dh −Bleeding Mode Control Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1dh	select external bleeding	bleeding accuracy			allow idle bleeding	allow bleeding all	bleeding number	

This register specifies bleeding mode.

Bit #	Name	Description	R/W	Reset Value
7	select external bleeding	Select external bleeding. If "1", select external bleeding; if "0", select internal bleeding.	RW	0h
6:4	bleeding accuracy	Select bleeding accuracy as follows: 3 bits: Bleeding accuracy 3'b000: 4*2.44 = 9.76mv 3'b001: 8*2.44 = 19.5mv 3'b010: 12*2.44 = 29.3mv 3'b011: 16*2.44 = 39.0mv 3'b100: 20*2.44 = 48.80mv 3'b101: 24*2.44 = 58.56mv 3'b110: 28*2.44 = 68.3mv 3'b111: 32*2.44 = 78.1mv The cell bleeding is to be stopped if the max_voltage – min_voltage < bleeding accuracy.	RW	0h
3	allow idle bleeding	If "1", allow bleeding in idle state and bleeding in OV state; if "0", don't allow bleeding in idle state or OV state.	RW	0h
2	allow bleeding all	If "1", allow bleeding all cells; if "0", only allow bleeding one cell at the same time.	RW	0h
1:0	bleeding number	Select the maximum bleeding number for external bleeding, if allow bleeding all is "0", select the maximum bleeding number as N+1. For example, if bleeding number is 2'b10, the maximum bleeding number is 3. For other cases, the maximum bleeding number is 1.	RW	0h

Register 1eh−Charge OC Threshold

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1eh	Reserved			Charge OC threshold				

This register sets the charge over current protection threshold.

Bit #	Name	Description	R/W	Default Value
7:5	reserved	Reserved.	R	0h
4:0	Charge OC threshold	Configure the charge OC threshold. The charge OC threshold as the following: 4 bits over current offset M from bit 7~bit4 in EE register03h (M is limited in -6~+6);	RW	0h

Bit #	Name	Description	R/W	Default Value
		its start value is 10mv and its step is 5mv; The threshold = (N+M-4)*5mv; for the case M=6(over current offset=30mv), the threshold = (N+2)*5mv (N:0~31) so that its range is 10mv~165mv; for the case M=0(over current offset=0mv), the threshold = (N-4)*5mv (N:6~31) so that its range is 10mv~135mv; for the case M=-6(over current offset=-30mv), the threshold = (N-10)*5mv (N:12~31) so that its range is 10mv~105mv. In a result, when M is in the range -6~+6, the threshold can be in the range 10mv~105mv. At the condition the over current offset =0, the charge over current threshold as followings:		

5 bits control	Charge OC threshold
0	-20mv
1	-15mv
2	-10mv
3	-5mv
4	0mv
5	5mv
6	10mv
…	…
N	(N-4)*5mv
30	130mv
31	135mv

Register 1fh−Discharge OC Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1fh	Reserved		Discharge OC threshold					

This register sets the discharge over current protection threshold.

Bit #	Name	Description	R/W	Reset Value
7:6	reserved	Reserved.	R	0h
5:0	Discharge OC threshold	Configure the discharge OC threshold. The over current offset M is from bit7~bit4 in EE register03h (M is limited in -6~+6). The start value is 30mv and its step is 5mv. The discharge OC threshold as the following: (N+M)*5mv for the case M=6(over current offset=30mv), the threshold = (N+6)*5mv (N:0~63) so that its range is 30mv~345mv; for the case M=0(over current offset=0mv), the threshold = N*5mv (N:6~63) so that its range is 30mv~315mv; for the case M=-6(over current offset=-30mv), the threshold = (N-6)*5mv (N:12~63) so that its range is 30mv~285mv. In a result, when M is in the range -6~+6, the threshold can be in the range 30mv~285mv. At the condition the over current offset =0, the discharge OC threshold as the following table:	RW	0h

6 bits control	Discharge OC threshold
0	0mv
1	5mv
2	10mv
3	15mv

Bit #	Name	Description		R/W	Reset Value
		…	…		
		N	N*5mv		
		…	…		
		62	310mv		
		63	315mv		

Register 20h –OC Delay Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20h	OC delay number					OC delay scale		

This register sets over current delay time.

Bit #	Name	Description	R/W	Reset Value
7:3	OC delay number	5 bits OC delay number are used to indicate the over current delay number as N+1 (N is the 5 bits value); 3 bits OC delay scale are used to indicate the oc delay unit as following:	RW	0h
2:0	OC delay scale	Oc delay scale / oc delay unit 3'b000 – 2ms*1=2ms 3'b001 – 2ms*3=6ms 3'b010 – 2ms*7=14ms 3'b011 – 2ms*15=30ms 3'b100 – 2ms*31=62ms 3'b101 – 2ms*63=126ms 3'b110 – 2ms*127=254ms 3'b111 – 2ms*255=510ms The OC delay time = (N+1)*(oc delay unit)., so its range is 2ms~16.3s	RW	0h

Register 21h –OC Release Control Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
21h	reserved		Discharge OC release control			Charge OC release control		

This register sets over current release control.

Bit #	Name	Description	R/W	Reset Value
7:6	reserved	Reserved.	R	0h
5:3	Discharge OC release control	Control the discharge OC release as following: 3-bit control / Discharge OC release 3'b000 – External release. The discharge OC will be released by the signal from analog SCRL Pin. 3'b001 – 1s time release. The discharge OC will be released after 1 second. 3'b010 – 2s time release. The discharge OC will be released after 2 seconds. 3'b011 – 4s time release. The discharge OC will be released after 4 seconds. 3'b100 – 8s time release. The discharge OC will be released after 8 seconds. 3'b101 – 16s time release. The discharge OC will be released after 16 seconds. 3'b110 – 24s time release. The discharge OC will be released after 24 seconds. 3'b111 – 32s time release. The discharge OC will	RW	0h

Bit #	Name	Description	R/W	Reset Value
		be released after 32 seconds.		
2:0	Charge OC release control	Control the charge OC release as following: 3-bit control: charge OC release 3'b000: 1s time release. The charge OC will be released after 1 second. 3'b001: 1s time release. The charge OC will be released after 1 second. 3'b010: 2s time release. The charge OC will be released after 2 seconds. 3'b011: 4s time release. The charge OC will be released after 4 seconds. 3'b100: 8s time release. The charge OC will be released after 8 seconds. 3'b101: 16s time release. The charge OC will be released after 16 seconds. 3'b110: 24s time release. The charge OC will be released after 24 seconds. 3'b111: 32s time release. The charge OC will be released after 32 seconds.	RW	0h

Register 22h –SC Threshold

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
22h	reserved		SC threshold					

This register sets the short circuit current protection threshold.

Bit #	Name	Description	R/W	Reset Value
7:6	reserved	Reserved.	R	0h
5:0	SC threshold	Configure the SC threshold as following: 4 bits short circuit offset M from bit3~bit0 in EE register03h (M is limited in -3~+3); Its start value is 50mv and its step is 10mv*1; The threshold*2 = (N+M+2)*10mv. for the case M=3(short circuit offset=30mv), the threshold = (N+5)*10mv (N:0~63) so that its range is 50mv~680mv; for the case M=0(short circuit offset=0mv), the threshold = (N+2)*10mv (N:3~63) so that its range is 50mv~650mv; for the case M=-3(short circuit offset=-30mv), the threshold = (N-1)*10mv (N:6~63) so that its range is 50mv~620mv. In a result, when M is in the range -3~+3, the threshold can be in the range 50mv~620mv. At the condition the short circuit offset =0, the short circuit threshold as following: 6 bits control: SC threshold 0: 20mv 1: 30mv 2: 40mv 3: 50mv 4: 60mv …: …	RW	0h

Bit #	Name	Description	R/W	Reset Value
		N: (N+2)*10mv …: … 62: 640mv 63: 620mv		

Register 23h –SC Delay

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
23h	SC delay number					SC delay scale		

This register sets short circuit delay time.

Bit #	Name	Description	R/W	Reset Value
7:3	SC delay number	5 bits SC delay number are used to indicate the short circuit delay number as N+1 (N is the 5 bits value); 3 bits SC delay scale are used to indicate the sc delay unit as following:	RW	0h
2:0	SC delay scale	SC delay scale / sc delay unit: 3'b000: 4us*2=8us 3'b001: 4us*4=16us 3'b010: 4us*8=32us 3'b011: 4us*16=64us 3'b100: 4us*32=128us 3'b101: 4us*64=256us 3'b110: 4us*128=512us 3'b111: 4us*256=1024us The SC delay time = (N+1)*(sc delay unit), so its range is 8us~32.8ms.	RW	0h

Register 24h –SC Release Control Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
24h	prmt_reserved4	prmt_reserved3	prmt_reserved2	prmt_reserved1	prmt_reserved0	SC release control		

This register sets short circuit release control.

Bit #	Name	Description	R/W	Reset Value
7	prmt_reserved4	real register is reserved for future use.	RW	0h
6	prmt_reserved3	real register is reserved for future use.	RW	0h
5	prmt_reserved2	real register is reserved for future use.	RW	0h
4	prmt_reserved1	real register is reserved for future use.	RW	0h
3	prmt_reserved0	real register is reserved for future use.	RW	0h
2:0	SC release control	Control the SC release as following: 3-bit SC control / SC release 3'b000: External release. The SC will be released by SCRL Pin. 3'b001: 0.25min time release. The SC will be released after 0.25 minutes. 3'b010: 0.5min time release. The SC will be released after 0.5 minutes. 3'b011: 0.75min time release. The SC will be	RW	0h

Bit #	Name	Description	R/W	Reset Value
		released after 0.75 minutes.		
		3'b100 — 1.0min time release. The SC will be released after 1.0 minutes.		
		3'b101 — 1.25min time release. The SC will be released after 1.25 minutes.		
		3'b110 — 1.5min time release. The SC will be released after 1.5 minutes.		
		3'b111 — 1.75min time release. The SC will be released after 1.75 minutes.		

OT/UT, OV/UV Delay Control Register 25h

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
25h	OT/UT Delay				OV/UV Delay			

This register sets over voltage/under voltage, over temperature/under temperature delay time.

Bit #	Name	Description	R/W	Reset Value
7:4	OT/UT Delay	Control the OT/UT delay time and release time as (N+1) scan cycles	RW	0h
3:0	OV/UV Delay	Control the OV/UV delay time and release time as (N+1) scan cycles	RW	0h

Register 26h –PF Control Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
26h	pfvh enable	pfvl enable	pf unbalance enable	pf mosfet fail enable	pf delay			

This register sets PF functions and delay time.

Bit #	Name	Description	R/W	Reset Value
7	pfvh enable	Enable pfvh function. If "1", enable pfvh function; if "0', disable pfvh function.	RW	0h
6	pfvl enable	Enable pfvl function. If "1", enable pfvl function; if "0', disable pfvl function.	RW	0h
5	pf unbalance enable	Enable pf unbalance function. If "1", enable pf unbalance function; if "0', disable pf unbalance function.	RW	0h
4	pf mosfet enable	Enable pf mosfet fail function. If "1", enable mosfet fail function; if "0", disable mosfet fail function. The detailed mosfet fail function as following: If the charge mosfet, precharge mosfet both are turned off, but the chip is in charge state(the current > the charge current threshold), the mosfet will be regarded as falied; in other hand, if the discharge mosfet is turned off, but the chip is in discharge state(the current < the discharge current threshold. (the current, discharge current threshold both are negative value), the mosfet will be regarded as failed. If this bit is "0", disable the mosfet fail detection.	RW	0h
3:0	Pf delay	Configure the pf delay time for pfvh, pfvl, pf unbalance, pf mosfet fail's delay time as (N+1) scan cycles. If the pfvh or pfvl or pf unbalance or pf mosfet fail is detected for continuous pf delay time, OZ8920 will send out PF and shut down the system.	RW	0h

Register 27h –OC0 Control Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
27h	Reserved		OC0 Release Control			OC0 Delay Control		

This register specifies OC0 control.

Bit #	Name	Description	R/W	Default Value
7:6	reserved	reserved	R	0h
5:3	OC0 Release Control	Control OC0 release as following: 3 bit control / OC0 release 000 / 2 scan cycles 001 / 4 scan cycles 010 / 6 scan cycles 011 / 8 scan cycles 100 / 12 scan cycles 101 / 16 scan cycles 110 / 24 scan cycles 111 / 32 scan cycles	RW	0h
2:0	OC0 Delay Control	Control OC0 delay as following: 3 bit control / OC0 delay 000 / 2 scan cycles 001 / 4 scan cycles 010 / 6 scan cycles 011 / 8 scan cycles 100 / 12 scan cycles 101 / 16 scan cycles 110 / 24 scan cycles 111 / 32 scan cycles	RW	0h

Register 28h~29h –DOTE Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
28h	bit3~bit0 of discharge OTE threshold				reserved			
29h	bit11~bit4 of discharge OTE threshold							

These two registers are used to specify the 12-bit discharge OTE (external over temperature) threshold voltage (100mV~2500mV). Please refer to 'External Temperature Sensor' section.

Register 2ah~2bh –DOTE Release Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2ah	bit3~bit0 of OTE release for discharge OTE				reserved			
2bh	bit11~bit4 of OTE release for discharge OTE							

These two registers are used to specify the 12-bit discharge OTE (external over temperature) release voltage (100mV~2500mV). Please refer to 'External Temperature Sensor' section.

Register 2ch~2dh –OC0 Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2ch	bit7~bit0 of OC0 (level 0 over current) threshold							
2dh	bit15~bit8 of OC0 threshold							

These two registers are used to specify the 16-bit OC0 (level 0 over current) threshold voltage (-250mV~250mV). Please refer to OC0 protection for detail.

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Registers 2eh~37h −Reserved

Register 38h~39h −OV Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
38h	bit3~bit0 of OV threshold				reserved			
39h	bit11~bit4 of OV threshold							

These two registers are used to specify the 12-bit OV (over voltage) threshold voltage (-300mV~5000mV).

Register 3ah~3bh −OV Release

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3ah	bit3~bit0 of OV release				reserved			
3bh	bit11~bit4 of OV release							

These two registers are used to specify the 12-bit OV (over voltage) release voltage (-300mV~5000mV). User should set this OV release voltage lower than OV threshold voltage.

Register 3ch~3dh−UV Threshold

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3ch	bit3~bit0 of UV threshold				reserved			
3dh	bit11~bit4 of UV threshold							

These two registers are used to specify the 12-bit UV (under voltage) release voltage (-300mV~5000mV).

Register 3eh~3fh −UV Release Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3eh	bit3~bit0 of UV release				reserved			
3fh	bit11~bit4 of UV release							

These two registers are used to specify the 12-bit UV (under voltage) release voltage (-300mV~5000mV). User should set this UV release voltage higher than UV threshold voltage.

Register 40h~41h −PFVH Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
40h	bit3~bit0 of PFVH threshold				reserved			
41h	bit11~bit4 of PFVH threshold							

These two registers are used to specify the 12-bit PFVH (high voltage permanent failure) threshold voltage (-300mV~5000mV). User should set this PFVH threshold higher than OV threshold.

Register 42h~43h− PFVL Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
42h	bit3~bit0 of PFVL threshold				reserved			
43h	bit11~bit4 of PFVL threshold							

These two registers are used to specify the 12-bit PFVL (low voltage permanent failure) threshold voltage (-300mV~5000mV). User should set this PFVH threshold lower than UV threshold.

Register 44h~45h –PF-Unbalance Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
44h	bit3~bit0 of PF unbalance threshold				reserved			
45h	bit11~bit4 of PF unbalance threshold							

These two registers are used to specify the 12-bit PF unbalance (unbalance permanent failure) threshold voltage (-300mV~5000mV).

Register 46h~47h –OTI Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
46h	bit3~bit0 of OTI threshold				reserved			
47h	bit11~bit4 of OTI threshold							

These two registers are used to specify the 12-bit OTI (internal over temperature) threshold voltage (100mV~2500mV). Please refer to 'internal Temperature Sensor' section.

Register 48h~49h ––OTI Release Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
48h	bit3~bit0 of OTI release				reserved			
49h	bit11~bit4 of OTI release							

These two registers are used to specify the 12-bit OTI (internal over temperature) release voltage (100mV~2500mV). Please refer to 'internal Temperature Sensor' section.

Register 4ah~4bh– UTI Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4ah	bit3~bit0 of UTI threshold				reserved			
4bh	bit11~bit4 of UTI threshold							

These two registers are used to specify the 12-bit UTI (internal under temperature) threshold voltage (100mV~2500mV). Please refer to 'internal Temperature Sensor' section.

Register 48h~49h– UTI Release Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4ch	bit3~bit0 of UTI release				reserved			
4dh	bit11~bit4 of UTI release							

These two registers are used to specify the 12-bit UTI (internal under temperature) release voltage (100mV~2500mV). Please refer to 'internal Temperature Sensor' section.

Register 4eh~4fh –COTE Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4eh	bit3~bit0 of charge OTE threshold				reserved			
4fh	bit11~bit4 of charge OTE threshold							

These two registers are used to specify the 12-bit charge OTE (external over temperature) threshold voltage (100mV~2500mV). Please refer to 'External Temperature Sensor' section.

Register 50h~51h –COTE Release Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
50h	bit3~bit0 of OTE release for charge OTE				reserved			
51h	bit11~bit4 of OTE release for charge OTE							

These two registers are used to specify the 12-bit charge OTE (external over temperature) release voltage (100mV~2500mV). Please refer to 'External Temperature Sensor' section.

Register 52h~53h –UTE Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
52h	bit3~bit0 of UTE threshold				reserved			
53h	bit11~bit4 of UTE threshold							

These two registers are used to specify the 12-bit UTE (external under temperature) threshold voltage (100mV~2500mV). Please refer to 'External Temperature Sensor' section.

Register 54h~55h – UTE Release Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
54h	bit3~bit0 of UTE release				reserved			
55h	bit11~bit4 of UTE release							

These two registers are used to specify the 12-bit UTE (external under temperature) release voltage (100mV~2500mV). Please refer to 'External Temperature Sensor' section.

Register 56h~57h – Bleeding Start Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
56h	bit3~bit0 of bleeding start				reserved			
57h	bit11~bit4 of bleeding start							

These registers are used to specify the bleeding start voltage and its LSB is 2.44mv. Only when the cell voltage > the bleeding start voltage, the cell can be in bleeding.

Registers 58h~5ah – Reserved

Register 5bh –Parameter Access Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5bh	parameter access		reserved					

This register is used to control access of parameter.

Bit #	Name	Description		R/W	Reset Value
7:6	parameter access	Control the access to the parameter data②.		RW	0h
		parameter access	parameter data access		
		2'b00	The safety scan is disabled; can read/write parameter data.		
		2'b01	The safety scan is enabled; can read/write parameter data.		
		2'b10	The safety scan is enabled; can read parameter		

Bit #	Name	Description	R/W	Reset Value
		data , can not write parameter data. 2'b11 The safety scan is enabled; can not read parameter; can not write parameter data. It is noted these 2 bits themselves can be read out always.		
5:0	Reserved	reserved	R	0h

EE register 5ch ~ 75h are project info data which are used by customer. EE register 75h is mapped to internal register 1bh. Its access is controlled by the EEPROM-mapped 1-bit ***project_info_access***.

Current _2nd_offset and GPIO_2nd_offset Registers 5ch~60h

Current_2nd_offset Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5ch	Low byte of current 2nd offset							
5dh	High byte of current 2nd offset							

GPIO_2nd_offset Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5eh	gpio1 2nd offset							
5fh	gpio2 2nd offset							
60h	gpio3 2nd offset							

These registers are used to specify the 2nd offset for current, gpio channels.

Reserved Registers 61h

Register 62h~6dh – Factory Name

10-byte registers for factory name (ASCII code) used by the user.

Register 6eh~72h –Project Name

5-byte registers for project name (ASCII code) used by the user.

Register 73h –Version Number

1-byte register for version number used by the user.

Registers 74h – Reserved

Register 75h – Project Info Access Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
75h	project info access	reserved						

This register is used to control access of project info.

Registers 76h~7bh − Reserved

EE register 7ch ~ 7fh are Log data which are used by customer. They can be read out or written always.

Register 7ch − PF Record Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
75c	reserved				pfvh	pfvl	pf unbalance	pf mosfet fail

This register saves the PF event record. When any individual PF event happens, the related PF record bit will be set to “1”.

Registers 7dh~7fh − Reserved

OZ8920 Operation Registers

OZ8920 operation registers from 00h to 7fh store the instant ADC readings, OZ8920 chip status information, etc. They also provide the control registers to control OZ8920's operation.

Register index (hex)	Register Name	Bit Number							
		7	6	5	4	3	2	1	0
00	Chip ID & Revision	Chip ID				Chip revision			
01~04	Reserved	Reserved							
05~1b	Mapping from EEPROM								
1c~1d	Reserved	Reserved							
1e	Safety Event	scan event	RV event	UT event	OT event	SC event	OC event	UV event	OV event
1f	PF Event	pfvh event	pfvl event	pf unbalance event	pf mosfet fail event	reserved	OC0 event	shut down	
20	Sleep Event	sleep_expired_event	integrator_wakeup_event	sc_wakeup_event	rv_wakeup_event	efetc_wakeup_event	reserved	sleep request	
21	Alert Enable	scan event enable	sleep_expired event enable	reserved					
22	FET Enable	reserved					Precharge enable	Charge enable	Discharge enable
23	FET Disable Status	OC0 disable	RV disable	UT disable	OT disable	SC disable	OC disable	UV disable	OV disable
24	Bleeding Control/ Status	cell8_bleeding	cell7_bleeding	cell6_bleeding	cell5_bleeding	cell4_bleeding	cell3_bleeding	cell2_bleeding	cell1_bleeding
25	OV/UV timer	ov timer				uv timer			
26	OT/UT timer	ot timer				ut timer			
27	OC Timer	OC timer							
28	PF timer	reserved				PF timer			
29	Charge/ Discharge State	OC0 timer					OC0 state	charge state	discharge state
2a	Safety Status	pfvh_state	pfvl_state	pf_unbalance_state	pf_mosfet_fail_state	ut_state	ot_state	uv_state	ov_state
2b	softeare reset	software reset		reserved					
2c	Deadman Control	reserved						deadman control	
2d	Deadman Timer	clear deadman timer	reserved			deadman timer			
2e	GPIO Data	gp3 in	gp2 in	gp1 in	gp0 in	GP3 out enable	GP3 out	GP2 out enable	GP2 out
2f	Reserved	reserved							
30	Cell1 ADC	Low byte of cell1's left-justified ADC data				reserved			

Register index (hex)	Register Name	Bit Number							
		7	6	5	4	3	2	1	0
31	Data	High byte of cell1's left-justified ADC data							
32	Cell2 ADC Data	Low byte of cell2's left-justified ADC data				reserved			
33		High byte of cell2's left-justified ADC data							
34	Cell3 ADC Data	Low byte of cell3's left-justified ADC data				reserved			
35		High byte of cell3's left-justified ADC data							
36	Cell4 ADC Data	Low byte of cell4's left-justified ADC data				reserved			
37		High byte of cell4's left-justified ADC data							
38	Cell5 ADC Data	Low byte of cell5's left-justified ADC data				reserved			
39		High byte of cell5's left-justified ADC data							
3a	Cell6 ADC Data	Low byte of cell6's left-justified ADC data				reserved			
3b		High byte of cell6's left-justified ADC data							
3c	Cell7 ADC Data	Low byte of cell7's left-justified ADC data				reserved			
3d		High byte of cell7's left-justified ADC data							
3e	Cell8 ADC Data	Low byte of cell8's left-justified ADC data				reserved			
3f		High byte of cell8's left-justified ADC data							
40	Internal Temp ADC Data	Low byte of internal temperature's left-justified ADC data				reserved			
41		High byte of internal temperature's left-justified ADC data							
42	Gpio1 ADC Data	Low byte of gpio1's of left-justified ADC data				reserved			
43		High byte of gpio1's left-justified ADC data							
44	Gpio2 ADC Data	Low byte of gpio2's of left-justified ADC data				reserved			
45		High byte of gpio2's left-justified ADC data							
46	Gpio3 ADC Data	Low byte of gpio3's of left-justified ADC data				reserved			
47		High byte of gpio3's left-justified ADC data							
48	Current ADC Data	Low byte of current's left-justified ADC data							
49		High byte of current's left-justified ADC data							
4a	Group1 Offset	Group1 offset							
4b	Group2	Group2 offset							
4c	Current Offset	Low byte of Current offset's left-justified ADC data				reserved			
4d		High byte of Current offset's left-justified ADC data							
4e~5a	Reserved	reserved							
5b	Reserved	reserved							
5c	EEPROM Data	Low byte of ee writing data or read back data							
5d		High byte of ee writing data or read back data							
5e	EEPROM Address	reserved	ee address						

Register index (hex)	Register Name	Bit Number							
		7	6	5	4	3	2	1	0
5f	EEPROM Control	ee busy	ee mode			ee op_code			
60-7f	Reserved	Reserved							

Detailed Operation Register Information

Register 00h–Chip ID & Revision Register

Bit #	Name	Description	R/W	Reset Value
7:4	Chip ID	This indicates the chip ID of OZ8920s	R	1h
3:0	Chip Revision	This indicates the chip revision of OZ8920. “0” indicates A version.	R	0h

Register 01h~04–Reserved

Register 05h–Cell Number Register

This register is mapped from EE register 15h.

Register 06h~19h–Parameter Data

These registers are mapped from EE register 16h~5bh.

Register 1ah~1bh–Project Info

These registers are mapped from EE register 5ch~75h.

Register 1ch~1dh–Reserved

Register 1eh–Safety Event Register

Bit #	Name	Description	R/W	Reset Value
7	scan event	When an adc scan is completed, this bit will be set to “1”. Once this bit is set to “1”, it will be kept until software clears it by writing “1” into this bit.	RW	0h
6	RV event	When RV (reverse voltage) happens, this bit will be set to high. And then it is kept as “1” until software clears it by writing “1” into this bit.	RW	0h
5	UT event	Once UT (under temperature) event happens, this bit will be set to “1”. And then it is kept as “1” until software clear it by writing “1” into this bit.	RW	0h
4	OT event	Once OT (over temperature) event happens, this bit will be set to “1”. And then it is kept as “1” until software clear it by writing “1” into this bit.	RW	0h
3	SC event	Once SC (short circuit) event happens, this bit will be set to “1”. And then it is kept as “1” until software clear it by writing “1” into this bit.	RW	0h
2	OC event	Once OC (over current) event happens, this bit will be set to “1”. And then it is kept as “1” until software clear it by writing “1” into this bit.	RW	0h
1	UV event	Once UV (under voltage) event happens, this bit will be set to “1”. And then it is kept as “1” until software clear it by writing “1” into this bit.	RW	0h

0	OV event	Once OV (over voltage) event happens, this bit will be set to “1”. And then it is kept as “1” until software clear it by writing “1” into this bit.	RW	0h

Register 1fh– PF Event Register

Bit #	Name	Description	R/W	Reset Value
7	pfvh event	When the pfvh is detected, this bit will be set to “1” and be kept until the software clears it by writing “1” into this bit.	RW	0h
6	pfvl event	When the pfvl is detected, this bit will be set to “1” and be kept until the software clears it by writing “1” into this bit.	RW	0h
5	pf unbalance event	When the pf unbalance is detected, this bit will be set to “1” and be kept until the software clears it by writing “1” into this bit.	RW	0h
4	pf mosfet fail event	When the pf mosfet fail is detected, this bit will be set to “1” and be kept until the software clears it by writing “1” into this bit.	RW	0h
3:2	reserved	Reserved.	R	0h
2	OC0 event	When OC0 is detected, this bit will be set to “1” and be kept until the software clears it by writing “1” into this bit.	RW	0h
1:0	software shut down	In software mode, if these bits are “01”, the chip will be shut down; when these bits are “00”, “10”, “11”, the chip will work normally. In hardware mode, this bit is ignored.	RW	10h

Register 20h–Sleep Event Register

Bit #	Name	Description	R/W	Reset Value
7	sleep_expired_event	When the sleep timer is expired, this bit will be set to “1” and be kept until the software clears it by writing “1” into this bit.	RW	0h
6	integrator_wakeup_event	When the wakeup from wakeup integrator block is acvite, this bit will be set to “1” and be kept until the software clears it by writing “1” into this bit.	RW	0h
5	sc_wakeup_event	In sleep state, when the sc_wakeup signal is active, this bit will be set to “1” and be kept until the software clears it by writing “1” into this bit.	RW	0h
4	rv_wakeup_event	In sleep state, when the rvp signal is active, this bit will be set to “1” and be kept until the software clears it by writing “1” into this bit.	RW	0h
3	efetc_wakeup_event	In sleep state, if efetc shut down function is enabled, when efetc pin is active, this bit will be set to “1” and be kept until the software clears it by writing “1” into this bit.	R	0h
2	reserved	Reserved.	R	0h
1:0	sleep request	Request sleep. In software mode, if these bits are “01”, the chip will enter into sleep state (if no events (OV, OC, OC0, SC, OT, UT, pfvh, pfvl, pf unbalance, pf mosfet fail, no bleeding, not charge state, not discharge state; if there is any of events, the chip will stay in the full power mode even this sleep request bits are set “01”); if these bits are “00”, “10”, “11”, the chip will go to full power state from sleep state. In hardware mode, these bits will be ignored.	RW	10h

If any of sleep_expired_event, integrator_wakeup_event, sc_wakeup_event, rv_wakeup_event is found, the alert_n will be active to inform the software.

Register 21h–Alert Enable Register

Bit #	Name	Description	R/W	Reset Value
7	scan event	If this bit is set to “1”, when scan event happens, the interrupt	RW	0h

Bit #	Name	Description	R/W	Reset Value
	enable	signal alert_n will be active; If this bit is set to “0”, the scan event will not make the interrupt signal alert_n active.		
6	Sleep expired event enable	If this bit is set to “HIGH”, when sleep expired event happens, the interrupt signal alert_n will be active. If this bit set to “LOW”, the ADC event will not make the interrupt signal alert_n active.	RW	0h
5:0	Reserved	Reserved	R	0h

In software mode or hardware mode, any safety events including RV event, UT event, OT event, SC event, OC event, OC0 event, UV event, OV event, PFVH event, PFVL event, PF unbalance event, PF mosfet fail event, any sleep events including integrator wakeup event, SC wakeup event, RV wakeup event, EFETC wakeup event will make AlertN pin active to inform the software; additionally if scan event enable bit is “1”, scan event will make alertn pin active; and more, if sleep expired event enable bit is “1”, sleep expired event will make alertn pin active.

Register 22h–FET Enable Register

Bit #	Name	Description	R/W	Reset Value
7:3	Reserved	Reserved.	R	0h
2	PreCharge enable	In software mode, if “1”, turn on the precharger FET if the safety check doesn’t force the FET to turn off; if “0”, turn off the precharger FET unconditionally. In hardware mode, this bit is ignored.	RW	0h
1	Charge enable	In software mode, if “1”, turn on the charger FET if the safety check doesn’t force the FET to turn off; if “0”, turn off the charger FET unconditionally. In hardware mode, this bit is ignored.	RW	0h
0	Discharge enable	In software mode, if “1”, turn on the discharger FET if the safety check doesn’t force the FET to turn off; if “0”, turn off the discharger FET unconditionally. In hardware mode, this bit is ignored.	RW	0h

Register 23h–FET Disable Status Register

Bit #	Name	Description	R/W	Reset Value
7:0	OC0, RV, UT, OT, SC, OC, UV, OV disable	Each of bits 7~0 will be set by OZ8920 in response to the safety event continues for some delay time. And the bits can be cleared automatically after some time when the corresponding events disappear.	R	0h

Register 24h–Bleeding Control/Status Register

Bit #	Name	Description	R/W	Reset Value
7	cell8_bleeding	When hw_bld_support = 0 (select software bleeding), this bit is readable/writeable. If “1”, enable cell8 bleeding; if “0”, disable cell8 bleeding. When hw_bld_support = 1 (select hardware bleeding), this bit is read only indicating cell8 is in bleeding.	RW/R	0h
6	Cell7_bleeding	When hw_bld_support = 0 (select software bleeding), this bit is readable/writeable. If “1”, enable cell7 bleeding; if “0”, disable cell7 bleeding. When hw_bld_support = 1 (select hardware bleeding), this bit is read only indicating cell7 is in bleeding.	RW/R	0h
5	Cell6_bleeding	When hw_bld_support = 0 (select software bleeding), this bit is readable/writeable. if “1”, enable cell6 bleeding; if “0”, disable cell6 bleeding.	RW/R	0h

Bit #	Name	Description	R/W	Reset Value
		When hw_bld_support = 1 (select hardware bleeding), indicate cell6 is in bleeding, this bit is read only.		
4	Cell5_bleeding	When hw_bld_support = 0 (select software bleeding), this bit is readable/writeable. if “1”, enable cell5 bleeding; if “0”, disable cell5 bleeding. When hw_bld_support = 1 (select hardware bleeding), this bit is read only indicating cell5 is in bleeding.	RW/R	0h
3	Cell4_bleeding	When hw_bld_support = 0 (select software bleeding), this bit is readable/writeable. if “1”, enable cell4 bleeding; if “0”, disable cell4 bleeding. When hw_bld_support = 1 (select hardware bleeding), this bit is read only indicating cell4 is in bleeding, this bit is read only.	RW/R	0h
2	Cell3_bleeding	When hw_bld_support = 0 (select software bleeding), this bit is readable/writeable. if “1”, enable cell3 bleeding; if “0”, disable cell3 bleeding. In hardware mode, this bit is read only indicating cell3 is in bleeding, this bit is read only.	RW/R	0h
1	Cell2_bleeding	When hw_bld_support = 0 (select software bleeding), this bit is readable/writeable. if “1”, enable cell2 bleeding; if “0”, disable cell2 bleeding. When hw_bld_support = 1 (select hardware bleeding), this bit is read only indicating cell2 is in bleeding, this bit is read only.	RW/R	0h
0	Cell1_bleeding	When hw_bld_support = 0 (select software bleeding), this bit is readable/writeable. if “1”, enable cell1 bleeding; if “0”, disable cell1 bleeding. When hw_bld_support = 1 (select hardware bleeding), this bit is read only indicating cell1 is in bleeding, this bit is read only.	RW/R	0h

Register 25h–OV/UV Timer Register

Bit #	Name	Description	R/W	Reset Value
7:4	ov timer	ov timer(unit is a scan cycle)	R	0h
3:0	ut timer	uv timer(unit is a scan cycle)	R	0h

Register 26h–OT/UT Timer Register

Bit #	Name	Description	R/W	Reset Value
7:4	ot timer	ot timer(unit is a scan cycle)	R	0h
4:0	ut timer	ut timer(unit is a scan cycle)	R	0h

Register 27h–OC Timer Register

Bit #	Name	Description	R/W	Reset Value
7:0	OC timer	It indicates the OC timer. When OC delay, Its unit is OC delay unit controlled by OC delay register; when OC release, the unit is 0.25s.	R	0h

Register 28h–PF Timer Register

Bit #	Name	Description	R/W	Reset Value
7:6	Reserved	Reserved.	R	0h
3:0	PF timer	PF timer(unit is a scan cycle).	R	0h

Register 29h–Charge/Discharge State Register

Bit #	Name	Description	R/W	Reset Value

7:3	OC0 timer	5-bit OC0 timer.	R	0h
2	OC0 state	OC0 state indicating OC0 is detected.	R	0h
1	charge state	Indicates OZ8920 is in charge state. If “1”, in charge state; if “0”, not in charge state.	R	0h
0	discharge state	Indicates OZ8920 is in discharge state. If “1”, in discharge state; if “0”, not in djscharge state.	R	0h

Register 2ah–Safety Status Register

Bit #	Name	Description	R/W	Reset Value
7	pfvh_state	Indicate pfvh is detected.	R	0h
6	pfvl_state	Indicate pfvl is detected.	R	0h
5	pf unbalance state	Indicate pf unbalance is detected.	R	0h
4	pf mosfet state	Indicate pf mosfet fail is detected.	R	0h
3	ut_state	Indicate UT is detected.	R	0h
2	ot_state	Indicate OT is detected.	R	0h
1	uv_state	Indicate UV is detected.	R	0h
0	ov_state	Indicate OV is detected.	R	0h

Register 2bh–Software Reset Register

Bit #	Name	Description	R/W	Reset Value
7:6	software reset	When software writes “01” into these bits, a software reset pulse is generated to reset the safety scan engine; when writes “00”, “10”, “11”, there is no effect. If software reads this bit, “00” is read out always.	RW	0
5:0	reserved	reserved	R	0

Register 2ch–Deadman Control Register

<table>
<tr><th>Bit #</th><th>Name</th><th>Description</th><th>R/W</th><th>Reset Value</th></tr>
<tr><td>7:2</td><td>Reserved</td><td>Reserved.</td><td>R</td><td>0h</td></tr>
<tr><td>1:0</td><td>deadman control</td><td>Specify the deadman time as following table:
<table>
<tr><th>deadman control</th><th>deadman expired time</th></tr>
<tr><td>00</td><td>deadman check is disabled.</td></tr>
<tr><td>01</td><td>4 seconds</td></tr>
<tr><td>10</td><td>8 seconds</td></tr>
<tr><td>11</td><td>16 seconds</td></tr>
</table></td><td>RW</td><td>0h</td></tr>
</table>

Deadman check function is enabled by a non-zero value to “deadman control” register. If deadman check is enabled, OZ8920 will increment the deadman timer every second when the safety scan is enabled. The software needs to do as following:

- Read the deadman timer by reading the register 2dh
- Write “1” into the bit 7 “clear timer” of register 2dh to clear the deadman timer.

If the handshake between OZ8920 and the software is normal, the software will clear the deadman timer before the dedman timer reaches the deadm expired time. In a result no deadman is found.

If the handshake has some problems, the software can not clear the deadman timer in time, while the deadman timer will do +1 every second. After some time, the deadman timer will reach the deadman expired time. In a result, OZ8920 will send out a 64ms low active pulse to RSTN pin to reset the external uP.

It is noted that when starting up the deadman check, it's possible to get a false deadman. To avoid this problem, do the above handshake procedure immediately after writing a non-zero value to "deadman control".

Register 2dh–Deadman Timer Register

Bit #	Name	Description	R/W	Reset Value
7	clear deadman timer	Clear deadman timer. If write "1" into this bit, the deadman timer will be cleared to "0"; if write "0" into this bit, no effect on the deadman timer. When read this bit, "0" is read out always.	RW	0h
6:4	reserved	Reserved.	R	0h
3:0	deadman timer	the deadman timer and its unit is 1s.	R	0h

Register 2eh–GPIO Enable & Data Register

Bit #	Name	Description	R/W	Reset Value
7	gp3 in	gpio3 input.	R	0h
6	gp2 in	gpio2 input	R	0h
5	gp1 in	gpio1 input	R	0h
4	gp0 in	gpio0 input	R	0h
3	gp3 out enable	If gpio3 is configured as a digital pin, enable gp3 output. If "1", enable gp3 output (output bit2 gp3 out); if "0", disable gp3 output.	RW	0h
2	gp3 out	the gpio3's output data.	RW	0h
1	gp2 out enable	If gp2 is configured as a digital pin, enable gp2 output. If "1", enable gp2 output (output bit0 gp2 out); if "0", disable gp2 output.	RW	0h
0	gp2 out	the gpio2's output data.	RW	0h

Register 2fh–Reserved Register

Register 30h~3fh–Cell Voltage ADC Data Register

These registers are used to store the cell1~cell8's left-justified ADC data which LSB is 2.44mv (5000mv/2048). The cell1~cell4's adc data are the adjusted value with the corresponding group1 offset register (4ah); the cell5~cell8's adc data are the adjusted value with the corresponding group2 offset register (4bh).

In adc fft mode, the adc data is the raw data without the adjustment and stored in current adc data registers (48h, 49h).

Register 40h~41h–Internal Temperature ADC Data Register

These registers are used to store the internal temperature's left-justified adc data which LSB is 1.22mv (2500mv/2048).

Register 42h~47h–GPIO ADC Data Register

These registers are used to store the 3 gpios's left-justified adc data which LSB is 1.22mv (2500mv/2048).

Register 48h~49h–Current ADC Data Register

These registers are used to store the current's left-justified adc data which LSB is 7.63uv (250mv/32768). The adc data is the adjusted value with the current offset register (4ch, 4dh).

In adc fft mode, the adc data is the raw data without the adjustment with current offset.

Register 4ah~4dh–Group1, Group2, Current Offset Register

These registers are used to store the group1 offset, group2 offset, current offset in 2's format.

For register 4ah, 4bh, offset = N*2.44mv (N:-128~127);

For register 4ch & 4dh, offset = N*7.63uv (N:-2048~2047).

Register 4eh~5bh–Reserved Register

Register 5ch~5dh–EEPROM Data Register

When writing word into EEPROM, this register is used to store the writing data; when read word from EEPROM, this register is used to store the read back word. When writing byte into EEPROM, register 5ch is used to store the writing data; register 5dh is not used.

To save the gate count, in adc fft mode, the bit3~bit0 of register 5ch can be used to specify the adc channel.

Register 5eh–EEPROM Address Register

Bit #	Name	Description	R/W	Reset Value
7	Reserved	Reserved.	R	0h
6:0	ee address	ee_address[6:1] are used to specify the EEPROM's word address. For byte write, ee_address[0] is used to specify the high or low byte. If "0", select the low byte; if "1", select the high byte.	RW	0h

Register 5fh–EEPROM Control Register

Bit #	Name	Description	R/W	Reset Value
7	ee_busy	This bit is high indicating the EEPROM is being accessed. After the access, it is low. Only when this bit is low, the software can start another EEPROM's access.	R	0h
6:4	ee_mode	These bits are used to select EEPROM mode. If set to "101", select EEPROM mode; if set to other values, select non-EEPROM mode. In EEPROM mode, software can access the EEPROM and the safety scan is disabled. In non-EEPROM mode, software can not access the EEPROM.	RW	0h
3:0	ee op code	These bits are used to specify the EEPROM's accesses as following:	RW	0h

ee_op_code	Access
4'b0000	no access
4'b0001	Word erase
4'b0010	Word write
4'b0011	Block erase
4'b0100	Block Write
4'b0101	Normal read
4'b0110	Internal high test read
4'b0111	Internal low test read
4'b1000	External high test read
4'b1001	External low test read
4'b1010	Block read
4'b1011	Byte write
Others	Reserved

Register 60h ~ 7fh – Reserved Registers

User Configurable Parameters

In order to make OZ8920 work normally and protect the battery pack, user should configure EEPROM registers correctly. Instead of setting EEPROM registers in binary code, O2Micro developed a software utility (Taurus) to help end user configure the EEPROM registers easily understandable, intuitive engineering parameters.

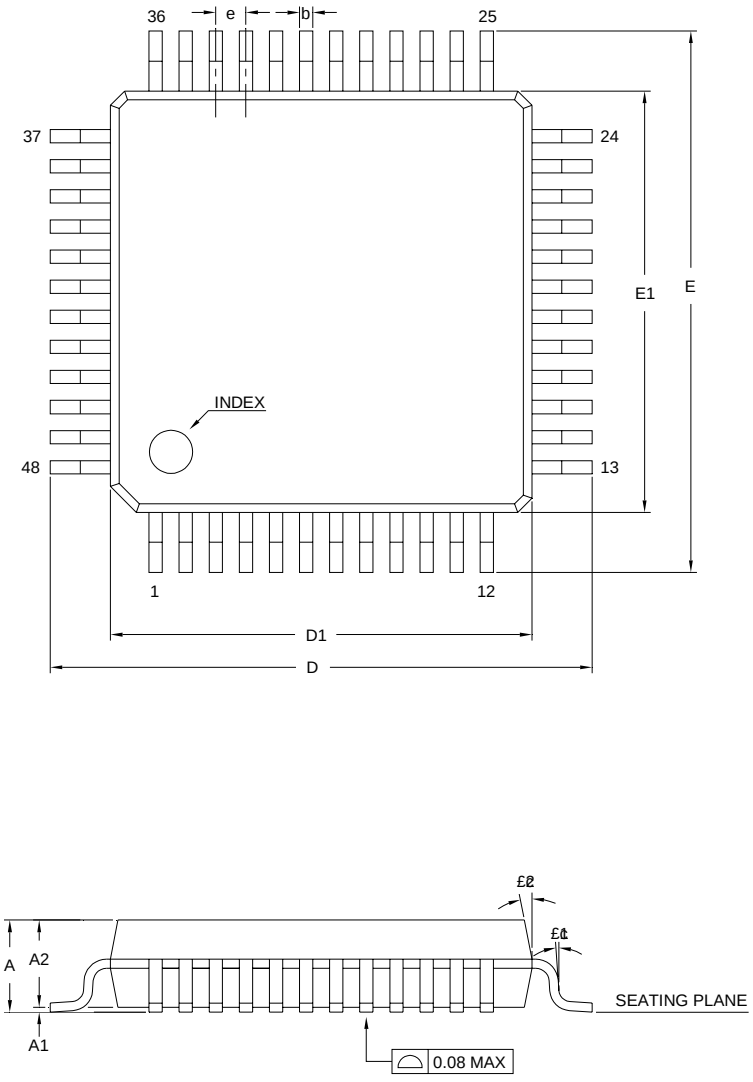
Group	Name	Units/Steps/Values	Description
Battery Setting	*CellNumber*	5-8 Li battery in series	To set the number of the battery Pack cells
Mode	*HWMode*		Hard/Software Mode selection
	EFETC Mode		To set the EFETC control mode
SMBUS Configuration	*SMBUSAddress*	N : 4 bits, Addr: 60h+2*N Support up to 16 devices	SMBUS address setting
	PECEnable		Enable packet error check based on SMBUS protocol
	SDA delay enable		Enable the extra delay on SDA input line
GPIO Config	*RV Control*	Disable,2,4,8 ms	Reverse Voltage function control
	GP1 mode		GP1 function selection
	GP2 mode		GP2 function selection
	GP3 mode		GP3 function selection
Options	*PreCHGEnable*		Pre-charge function enable
	Rsense	mOhm	The value of the sense resistor (Rs)
	Parameter Access		Control the access to parameter data
Idle Mode Configuration	*CHGCurrentTH*	8~64 ADC LSB / Rs	Charge current threshold
	DSGCurrentTH	-128~-16 ADC LSB / /Rs	Discharge current threshold
	ScanRate	0.5,1,2,4,6,8,12,16, seconds	To Specify the protection scan period in Idle Mode
	Auto Scan Enable		Auto Scan Control
Sleep Mode Configuration	*SleepEnable*		Enable the sleep mode
	SleepTime	0-15 Minutes step:1 Min	To select the period of sleep mode, after every sleep interval the chip will do protection scan
OC/SC Configuration	*CHGOverCurrentTH*	-20mV/Rs-135mV/Rs with step of 5mV/Rs	Charge over current threshold
	DSGOverCurrentTH	0mV/Rs-315mV/Rs with step of 5mV/Rs	Discharge over current threshold
	OverCurrentDelay	2ms-16.3s	Over current delay time
	ShortCurrentTH	50mV/Rs-620mV/Rs with step of 10mV/Rs	Short current threshold

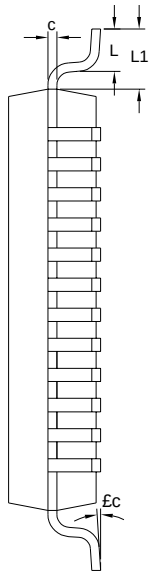
Group	Name	Units/Steps/Values	Description
	SC Delay	4us-32.6mS	Short current delay time
	DOC Release Time	External, 1~31s	DOC release time setting
	COC Release Time	1~32s	COC release time setting
	SC Release Time	0.25~1.75min with step of 0.25min	SC release time setting
	OC0 Delay Time	2~32 scan cycle	OC0 delay time setting
	OC0 Rlease Time	2~32 scan cycle	OC0 release time setting
	OC0 Threshold	Signed 16 bits data (negtive)	OC0 threshold
OV/UV Configuration	*OverVoltageTH*	0-5V	Over voltage(OV) threshold voltage setting
	OVRelease	0-5V	OV release voltage setting
	UnderVoltageTH	0-5V	Under voltage(UV) threshold voltage setting
	UVRelease	0-5V	UV release voltage setting
	OVUVDelay	1~16 scan cycle	OV and UV delay time setting
OT/UT Configuration	*COTE TH*	°C	Charge external over temperature threshold
	COTE Release	°C	Charge external OT release
	DOTE TH	°C	Discharge external over temperature threshold
	DOTE Release	°C	Discharge external OT release
	UTE TH	°C	External under temperature (UT) threshold
	UTE Release	°C	External UT release
	OTI TH	°C	Internal OT threshold
	OTI Release	°C	Internal OT release value
	UTI TH	°C	Internal UT threshold
	UTI Release	°C	Internal UT release value
	OTUTDelay	1-16 scan cycle	OT UT delay time setting
PF Configuration	*PF Record*		PF record register
	PFVHTH	0-5V	Permanent failure(PF) high voltage threshold set
	PFVLTH	0-5V	PF low voltage threshold setting
	PFDelay	1-16 scan cycle	PF delay time
	PFVHEnable		PFVH function enable
	PFVLEnable		PFVL function enable
	MOSFailEnable		PF of MOSFET failure enable
	PFUnbalanceEn		PF of the cell unbalance enable
	PFUnbalanceTH	0-2.5V	PF of the cell unbalance threshold
Bleeding	*BleedEnable*		Bleeding function enable

Group	Name	Units/Steps/Values	Description
Configuration	*ExtBleedSel*		To select the external or internal bleeding method
	BleedCellNumber	1-4	Max bleeding cell number in external bleeding method
	BleedAll		Enable all cell bleeding option
	Idle Bleed Enable		Enable bleed in idle state
	BleedStartPoint	0-5V	Bleeding start point voltage
	BleedAccuracy	9.76, 19.50, 29.30, 39.00, 48.80, 58.56, 68.30, 78.10mV	Bleeding accuracy setting

PACKAGE INFORMATION

48L LQFP 7x7mm Package Outline Drawing





SYMBOL	DIMENSION (MM)		
	MIN	NOR	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	-	0.75
L1	1.00 REF		
θ	0°	-	7°
θ1	0°	-	-
θ2	12° TYP		

NOTE:
1. REFER TO JEDEC STD MS-026 BBC

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