Synchronous Switchmode
Li-Ion and Li-Pol Charge Management IC With Integrated PowerFETs

FEATURES

- Ideal for highly-efficient charger designs for single- or two- or three-cell Li-Ion or Li-Pol battery packs
- Integrated synchronous fixed-frequency PWM controller operating at 1.1MHz
- Integrated PowerFETs for up to 2A charge rate
- High accuracy voltage and current regulation
- Offered in both standalone (built-in charge management and control) and System-controlled (under system command) versions
- Status outputs for LED or host processor interface indicates charge-in-progress, charge completion, and fault and AC-adapter present conditions
- 20V input voltage rating
- High-side current sensing
- Optional battery temperature monitoring
- Automatic sleep mode for low power consumption
- Small 3.5x4.5mm QFN package

APPLICATIONS

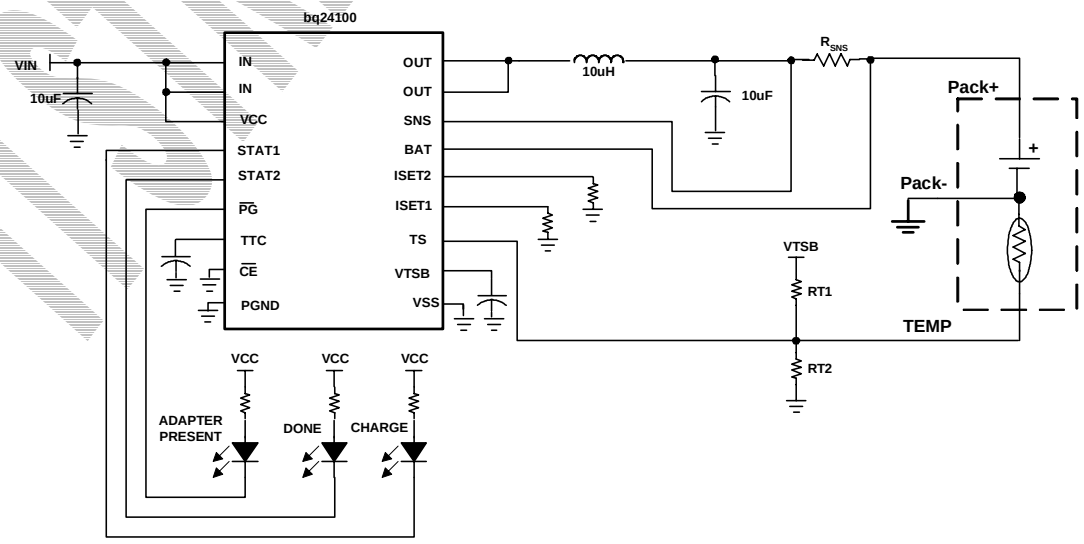
- Handheld products
- Portable media players
- Industrial and medical equipment
- Portable equipment
- Cradle and desktop chargers

DESCRIPTION

The bqSWITCHER™ series are highly integrated Li-Ion and Li-Pol switch-mode charge management devices targeted at a wide range of portable applications. The bqSWITCHER series offer integrated synchronous PWM controller and PowerFETs, high accuracy current and voltage regulation, charge conditioning, charge status, and charge termination, in a small thermally enhanced QFN package. The system –controlled version provides additional input for full charge management under system control.

The bqSWITCHER charges the battery in three phases: conditioning, constant current, and constant voltage. Charge is terminated based on user-selectable minimum current level. A programmable charge timer provides a backup safety for charge termination. The bqSWITCHER automatically re-starts the charge if the battery voltage falls below an internal threshold. The bqSWITCHER automatically enters sleep mode when Vcc supply is removed.

TYPICAL APPLICATION



AVAILABLE OPTIONS

T_J	Charge Regulation Voltage	Intended Application	Packaged Devices
-40°C to 125°C	4.2V	Standalone	bq24100RHL
	4.2V or 8.4V	Standalone	Bq24103RHL
	Externally Programmable	Standalone	bq24105RHL
	1 or 2 cell selectable (CELLS pin)	System-controlled	bq24113RHL
	Externally Programmable	System-controlled	bq24115RHL

† The RGY package is available taped and reeled. Add R suffix to device type (e.g. bq24100RGYR) to order. Quantities 3,000 devices per reel.

PACKAGE DISSIPATION RATING TABLE

Package	θ_{JA}	$T_A \leq 40°C$ POWER RATING	Derating Factor Above $T_A=40°C$
RHL (1)	46.87°C/W	1.81W	0.021 W/°C

(1) Not Final. This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. This is connected to the ground plane by a 2x3 via matrix.

ABSOLUTE MAXIMUM RATING†

	ALL DEVICES
Supply voltage (IN, and VCC with respect to VSS, and PGND)	20V
Input voltage on STATx, PG, CE, CELLS, OUT, SNS, and BAT (all with respect to VSS, and PGND)	VCC
Input voltage on CMODE, and TTC (with respect to VSS, and PGND)	7V
Input voltage on TS (with respect to VSS, and PGND)	VTSB
Input voltage on ISET1, ISET2 and VTSB (with respect to VSS, and PGND)	3.3V
Output current (OUT pin)	2.2A
Output sink/source current (STATx, PG)	10mA
Operating free–air temperature range, T_A	-40°C to 85°C
Storage temperature range, T_{stg}	- 65°C to 150°C
Junction temperature range, T_J	-40°C to 125°C
Lead temperature (Soldering, 10s)	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Supply voltage, V_{CC} (IN pin)	3.5	18	V
Operating Junction temperature range, T_J	0	+125	°C

ELECTRICAL CHARACTERISTICS,

ALL SPECIFICATIONS OVER $0^oC \leq T_J \leq 125^oC$ AND RECOMMENDED SUPPLY VOLTAGE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vcc Current, $I_{CC(VCC)}$	Vcc > Vcc(min)		10		mA
Sleep current, $I_{CC(SLP)}$	Input Bias Current on OUT, SNS, BAT, & VFB pins Current into OUT pin, $Vcc<V_{(SLP)}$			5	µA
Input Bias Current on BAT pin, $I_{IB\ (BAT)}$	$V_{I(BAT)} = V_{O(REG)}$ when not in charge			1	µA
Input Current on TS pin, $I_{IB\ (TS)}$				1	µA
Input Current on SNS pins, $I_{IB\ (SNS)}$	$V_{I(SNS)} = V_{O(REG)}$			1	µA

VOLTAGE REGULATION, $V_{O(REG)} + V_{(DO-MAX)} \leq Vcc$, $I_{(TERM)} < I_{O(OUT)} \leq 2A$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT

Output voltage, $V_{O(REG)}$	CELLS= Low		4.20		Volts
Output voltage, $V_{O(REG)}$	CELLS= High		8.4		Volts
Voltage Regulation Accuracy	T_A=25°C	-0.5		0.5	%
Voltage Regulation Accuracy		-1		1	%

CURRENT REGULATION

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output current range, $I_{O(OUT)}$	$V_{(LOWV)} \le V_{I(BAT)} \le V_{O(REG)}$, $Vcc - V_{I(BAT)} > V_{(DO-MAX)}$	150		2,000	mA
Current Regulation Accuracy	$Vcc \ge Vcc$ (min), $Vcc \ge V_{I(BAT)} + V_{(DO-MAX)}$, $V_{(LOWV)} \le V_{I(BAT)} \le V_{O(REG)}$, Over output current range. Does not include error induced by the tolerance of resistor, $R_{(SET)}$, on the ISET pin, or the sense resistor, $R_{(SNS)}$	-10		10	%
Current regulation differential threshold range, $V_{(IREG)}$	$V_{I(SNS - BAT)}$ $Vcc \ge V_{I(BAT)} + V_{(DO-MAX)}$, $V_{(LOWV)} \le V_{I(BAT)} \le V_{O(REG)}$	100		200	mV
Output current set voltage, $V_{(SET)}$	$Vcc \ge Vcc$ (min), $Vcc \ge V_{I(BAT)} + V_{(DO-MAX)}$, $V_{(LOWV)} \le V_{I(BAT)} \le V_{O(REG)}$		1.00		V
Output current set factor, $K_{(SET)}$	$Vcc \ge Vcc$ (min), $Vcc \ge V_{I(BAT)} + V_{(DO-MAX)}$, $V_{(LOWV)} \le V_{I(BAT)} \le V_{O(REG}$		1000		V/A

PRE-CHARGE AND SHORT-CIRCUIT CURRENT REGULATION

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Precharge to fast-charge transition threshold, $V_{(LOWV)}$	Voltage on BAT pin Shown for single cell. Double for two-cell	68	71.4	75	% $V_{O(REG)}$
Precharge range, $I_{O(PRECHG)}$	$V_{I(BAT)} < V_{(LOWV)}$, $t < t_{(PRECHG)}$ $I_{O(PRECHG)}=K_{(SET2)}*V_{(PRECHG)}/R_{SET2}$	15		200	mA
Precharge set voltage, $V_{(PRECHG)}$	Voltage on ISET2 pin, $V_{I(BAT)} > V_{(LOWV)}$, $t < t_{(PRECHG)}$		100		mV
Precharge current set factor, $K_{(SET2)}$			1000		V/A
Pre-charge current regulation accuracy)	$0 \le V_{I(BAT)} < V_{(LOWV)}$	-20		20	%
Short-circuit Voltage threshold on BAT, $V_{(SHORT)}$	$V_{I(BAT)}$ falling	1.95	2	2.05	V/Cell

CHARGE TAPER (TERMINATION) DETECTION

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Charge taper detection range, $I_{(TAPER)}$	$V_{I(BAT)} > V_{(RCH)}$, $t < t_{(TAPER)}$ $I_{(TAPER)}=K_{(SET2)}*V_{(TAPER)}/R_{SET2}$	15		200	mA
Charge taper detection set voltage, $V_{(TAPER)}$	Voltage on ISET2 pin, $V_{I(BAT)} > V_{(RCH)}$		100		mV
Taper current set factor, $K_{(SET2)}$			1000		V/A
Charge termination accuracy	$V_{I(BAT)} > V_{(RCH)}$	-20		20	%

TEMPERATURE COMPARATOR AND VTSB BIAS REGULATOR

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Cold Temperature Threshold, $V_{(LTF)}$	TS pin voltage	72.9	73.5	74.1	%VTSB
Hot Temperature Threshold, $V_{(HTF)}$	TS pin voltage	33.7	34.4	35.1	% VTSB
Cutoff Temperature Threshold, $V_{(TCO)}$	TS pin voltage	28.7	29.3	29.9	% VTSB
LTF Hysteresis	Hysteresis for LTF threshold	0.5	1	1.5	% VTSB
Deglitch time for Temperature Fault	Both rising and falling, TS pin voltage; 100ns rise & fall time, 2mv overdrive	20	30	40	ms
Output voltage, $V_{O(VTSB)}$	VCC > 4.5V, $C_{O(VTSB)}$=1uF, 10mA		3.0		Volts
$V_{O(VTSB)}$ Voltage Regulation Accuracy	T_A=25°C, $C_{O(VTSB)}$=1uF, 10mA	-10		10	%

BATTERY RECHARGE THRESHOLD

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Recharge Threshold, $V_{(RCH)}$		90	100	110	mV / cell
Deglitch time	$V_{I(BAT)}$ decreasing below threshold; 100ns fall time, 10mv overdrive	20	30	40	ms

STAT1, STAT2 and /PG Outputs

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output (low) saturation voltage, $V_{OL(STATx)}$	Io = 10mA			0.5	Volts

/CE , CMODE, CELLS INPUTS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input (low) voltage, V_{IL}	I_{IL} = 5µA	0		0.4	Volts
Input (high) voltage V_{IH}	I_{IH} = 20µA	1.3		Vcc	Volts

TTC Input

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pre -charge $t_{(PRECHG)}$		1440	1800	2160	s
Programmable Charge Timer, $t_{(CHG)}$	$t_{(CHG)} = C_{(TMR)} \times K_{(TMR)}$	25		480	min
Charge timer accuracy		-10		10	%
Timer Multiplier, $K_{(PROG}$			2.8		Minute/nF
Charge time Capacitor Range, $C_{(PROG)}$		0.001		0.22	µF
Termination & Timer Control, TTC, enable threshold voltage	TTC voltage rising		200		mV

SLEEP Comparator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sleep-mode entry threshold, $V_{(SLP-ENTRY)}$	$2.3V \le V_{I(OUT)} \le V_{O(REG)}$			Vcc ≤ $V_{I(OUT)}$ +80mV	
Sleep-mode exit threshold, $V_{(SLP-EXIT)}$	$2.3V \le V_{I(OUT)} \le V_{O(REG)}$	Vcc ≥ $V_{I(OUT)}$ +160mV			Volts
Deglitch time for sleep mode	Vcc decreasing below threshold; 100ns fall time, 10mv overdrive	20	30	40	ms

UVLO

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO turn-on threshold, $V_{(UVLO-ON)}$	Rising	3.2	3.3	3.5	V
UVLO turn-off Hysteresis	Falling	150	250		mV

PWM

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal P-Channel MOSFET on-resistance	$4.5V \le Vcc \le Vcc_{(MAX)}$			312	mΩ
Internal N-Channel MOSFET on-resistance	$4.5V \le Vcc \le Vcc_{(MAX)}$			85	mΩ
Oscillator Frequency, $F_{(OSC)}$			1.1		MHz
Accuracy PWM frequency		9		9	%
Maximum duty cycle		100			%
Minimum duty cycle				0	%

BATTERY DETECTION

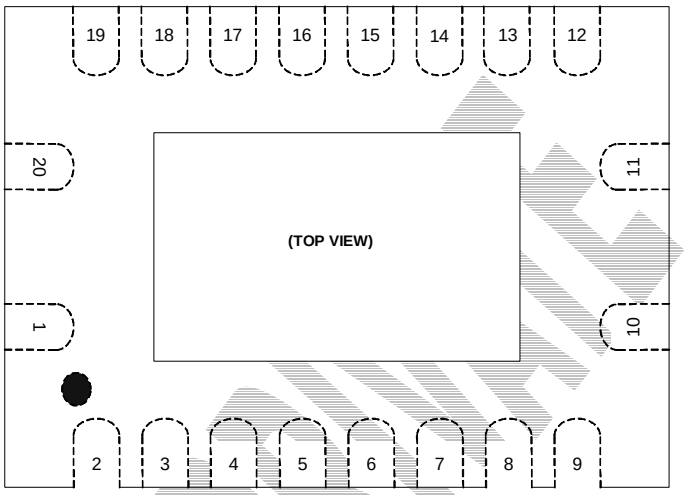
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Battery Detection Current during time out fault, $I_{(DETECT)}$	$V_{I(BAT)} < V_{O(REG)}$		2		mA
Discharge current, $I_{(DISCHRG1)}$	$V_{(SHORT)} < V_{I(BAT)} < V_{O(REG}$		100		µA
Discharge time, $t_{(DISCHRG1)}$	$V_{(SHORT)} < V_{I(BAT)} < V_{O(REG}$		4.2		s
Wake Current, $I_{(WAKE)}$	$V_{(SHORT)} < V_{I(BAT)} < V_{O(REG}$		2		mA
Wake Time, $t_{(WAKE)}$	$V_{(SHORT)} < V_{I(BAT)} < V_{O(REG}$		2.1		s
Term Discharge current, $I_{(DISCHRG2)}$	begins after termination detected, $V_{I(BAT)} \ge V_{O(REG)}$		100		µA
Term Time, $t_{(DISCHRG2)}$	begins after termination detected, $V_{I(BAT)} \ge V_{O(REG)}$		262		ms

Required Output ceramic capacitor from OUT to Vss.		4.7	10	47	µF

Output Overvoltage Protection

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVP Threshold voltage	Threshold over $V_{O(REG}$ to turn-off PMOS FET, STAT1 and STAT2 during charge or termination states.	117	119	121	%Vreg

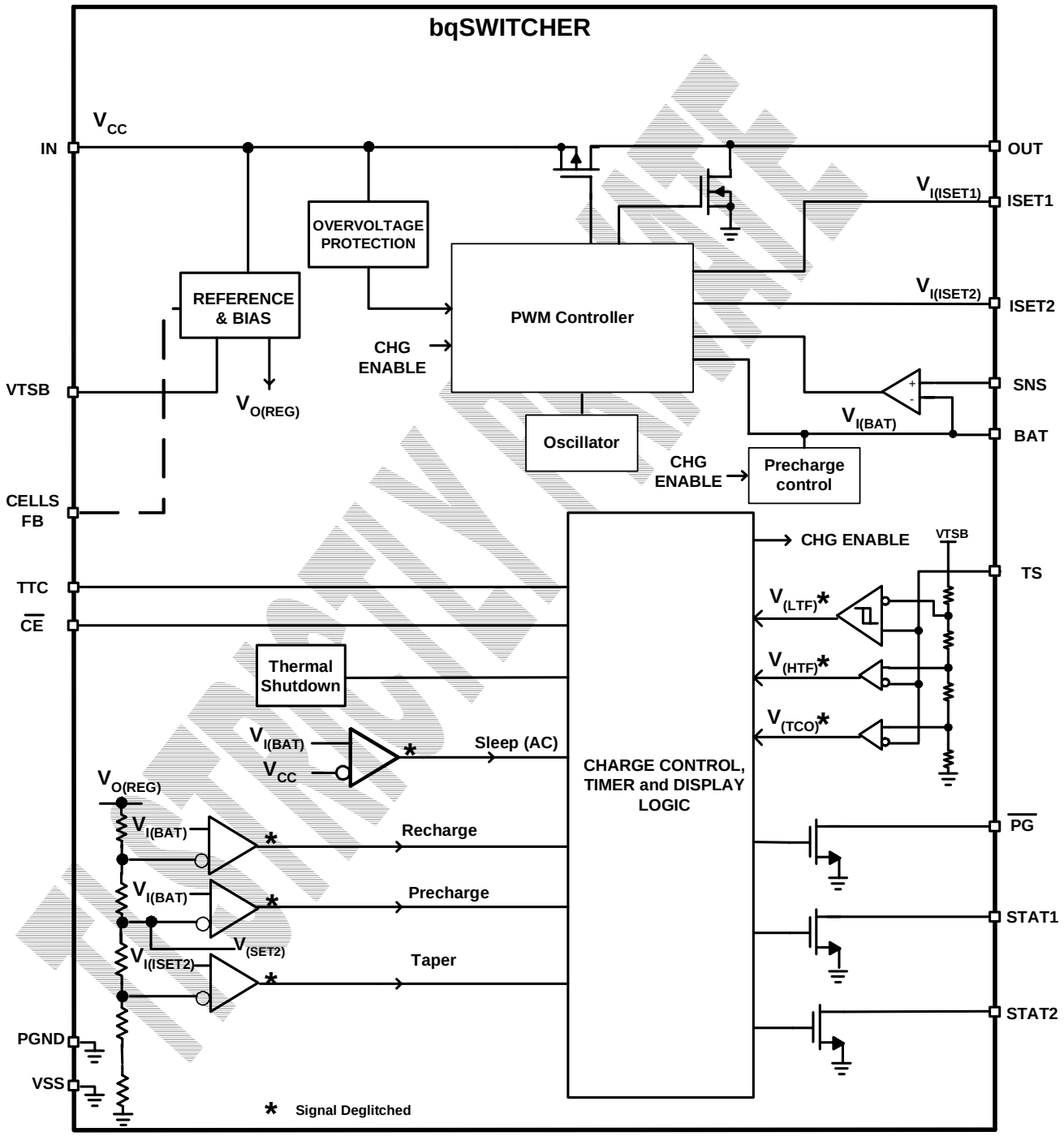
PIN ASSIGNMENT (Subject to Change)



TERMINAL FUNCTIONS

NAME	TERMINAL NO.					I/O	Description
	bq24100	bq24103	bq24105	bq24113	bq24115		
BAT	14	14	14	14	14	I	Battery voltage sense input
/CE	16	16	16	16	16	I	Charge enable Input (active Low)
CELLS		13		13		I	Number of cells (single cell or two-cell) selection input. Low or floating is single cell.
CMODE				7	7	I	Charge mode selection (low for pre-charge, high for fast charge)
FB			13		13	I	Output voltage analog feedback adjustment
IN	3,4	3,4	3,4	3,4	3,4	I	Charge Input Voltage
ISET1	8	8	8	8	8	I/O	Charge current set point 1 (Fast charge)
ISET2	9	9	9	9	9	I/O	Charge current set point 2 (pre-charge and termination)
N/C	13			19	19	-	No connection
OUT	1,20	1,20	1,20	1,20	1,20	O	Charge current output inductor connection
/PG	5	5	5	5	5	O	Power Good status output (open-drain)
PGND	17,18			17,18	17, 18		Power Ground Input
SNS	15	15	15	15	15	I	charge current sense input
STAT1	2	2	2	2	2	O	Charge Status Output 1 (open-drain)
STAT2	19	19	19			O	Charge Status Output 2 (open-drain)
TS	12	12	12	12	12	I	Temperature Sense Input.
TTC	7	7	7			I	Timer & Termination Control. Charge timer programming input. Timer and taper disabled when low.
VCC	6	6	6	6	6	I	Analog charge input voltage sense and IC supply voltage.
VSS	10	10	10	10	10		Analog ground input
VTSB	11	11	11	11	11	O	TS Internal Bias Regulator voltage
Exposed Thermal Pad	Pad	Pad	Pad	Pad	Pad		There is an internal electrical connection between the exposed thermal pad and Vss pin of the IC. The exposed thermal pad must be connected to the same potential as the Vss pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the IC. Vss pin must be connected to ground at all times

FUNCTIONAL BLOCK DIAGRAM (STANDALONE VERSION SHOWN)



APPLICATIONS INFORMATION

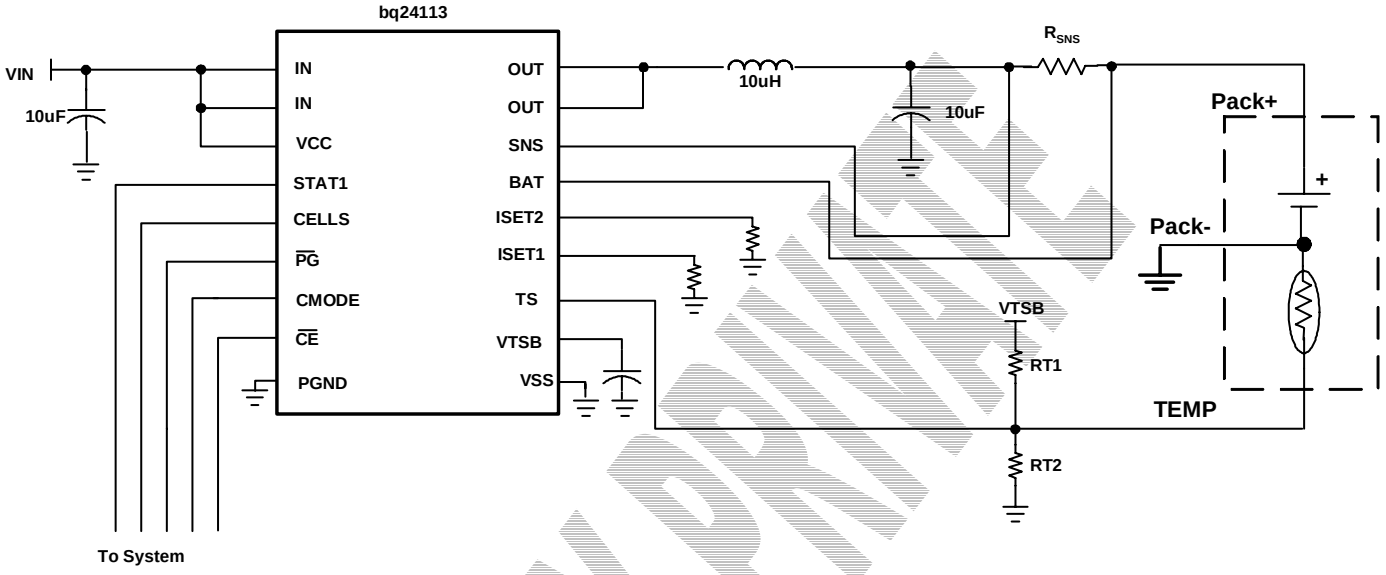


Figure 1. Typical Application Circuit (System-Controlled Version)

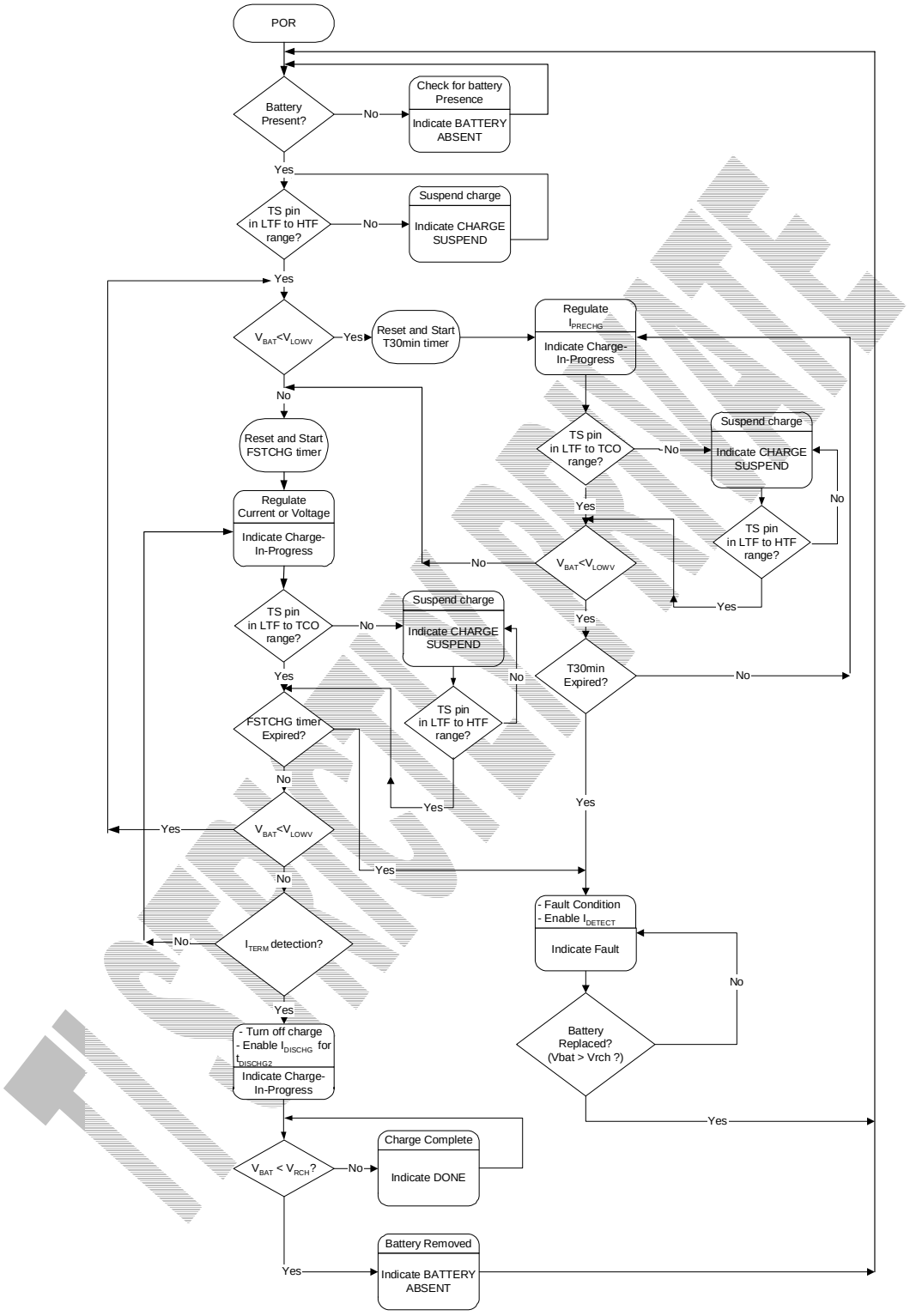


Figure 2. Standalone version Operational Flow Chart

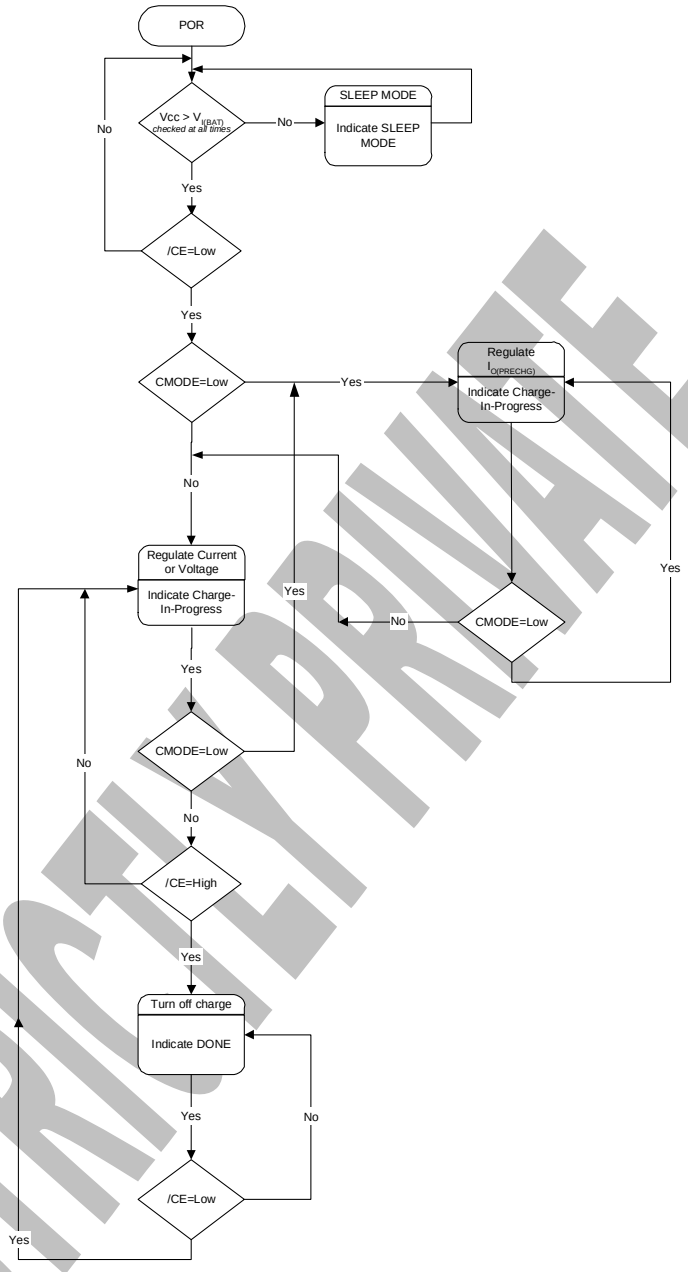


Figure 3: System Controlled Operational Flow Diagram

FUNCTIONAL DESCRIPTION FOR STANDALONE VERSION (bq2410x)

The bqSWITCHER supports a precision Li-Ion or Li-Pol charging system for single or two-cell applications. See Figure 2 and 3 for an operational flow charts and Figure 4 for a typical charge Profile.

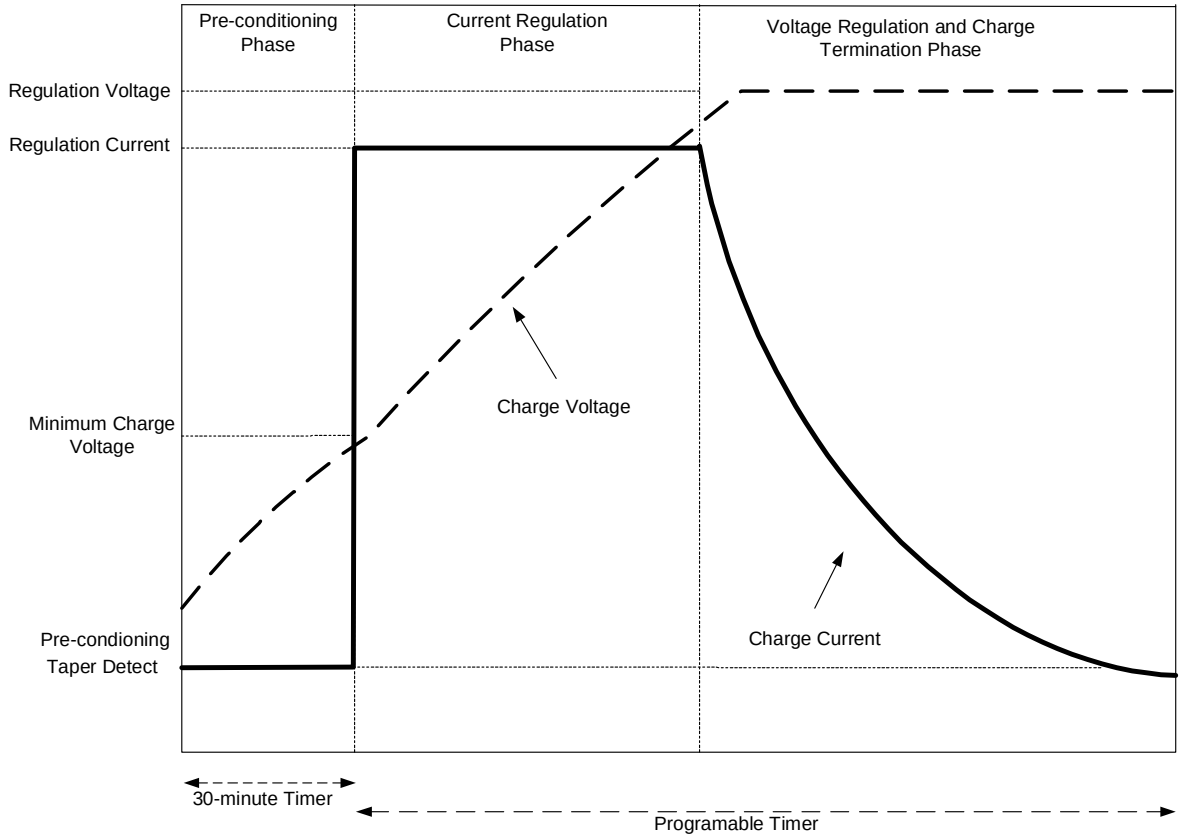


Figure 4. Typical Charging Profile

TEMPERATURE QUALIFICATION (applies to versions with TS pin)

The bqSWITCHER continuously monitors battery temperature by measuring the voltage between the TS pin and Vss. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develop this voltage. The bqSWITCHER compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the $V_{(LTF)}$ to $V_{(HTF)}$ thresholds. If battery temperature is outside of this range, the bqSWITCHER suspends charge and waits until the battery temperature is within the $V_{(LTF)}$ to $V_{(HTF)}$ range. During the charge cycle (both pre-charge and fast charge) the battery temperature must be within the $V_{(LTF)}$ to $V_{(TCO)}$ thresholds. If battery temperature is outside of this range, the bqSWITCHER suspends charge and waits until the battery temperature is within the $V_{(LTF)}$ to $V_{(HTF)}$ range. The bqSWITCHER suspends charge by turning off the MOD pin and holding the timer value (i.e. timers are not reset during a suspend condition). Note that the bias for the external resistor divider is provided from the VTSB output.

Figure 5 summarizes this operation.

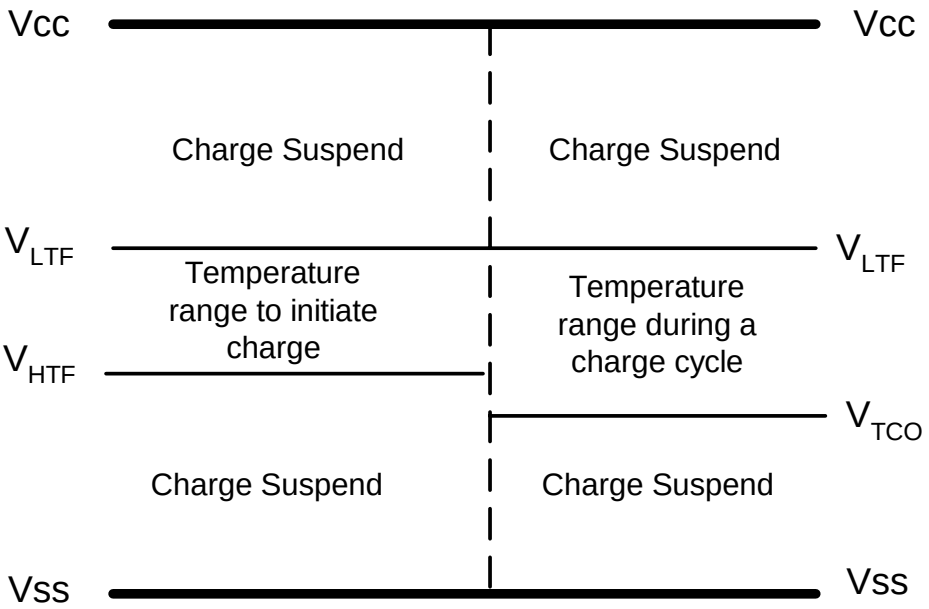


Figure 5: TS Pin Thresholds

BATTERY PRE-CONDITIONING

Upon power-up, if the battery voltage is below the $V_{(LOWV)}$ threshold, the bqSWITCHER applies a pre-charge current, $I_{(PRECHG)}$, to the battery. This feature revives deeply discharged cells. The bqSWITCHER activates a safety timer, $t_{(PRECHG)}$, during the conditioning phase. If $V_{(LOWV)}$ threshold is not reached within the timer period, the bqSWITCHER turns off the charger and enunciates FAULT on the STATx pins. In the case of a FAULT condition, the bqSWITCHER reduces the current to $I_{(DETECT)}$. $I_{(DETECT)}$ is used to detect a battery replacement condition. Fault condition is cleared by POR or battery replacement.

The magnitude of the pre-charge current, $I_{(PRECHG)}$, is determined by the value of programming resistor, $R_{(SET2)}$, connected to the ISET2 pin.

BATTERY CHARGE CURRENT

The battery charge current, $I_{O(CHARGE)}$, is established by setting the external sense resistor, $R_{(SNS)}$, and the resistor, $R_{(SET1)}$, connected to the ISET pin. In order to set the current, first $R_{(SNS)}$ should be chosen based on the regulation threshold $V_{(IREG)}$, across this resistor.

$R_{(SNS)} = V_{(IREG)} / I_{O(CHARGE)}$

The value of $R_{(SET)}$ is then calculated based on the following equation:

$$I_{(CHARGE)} = (K_{SET} * V_{SET}) / (R_{SET} * R_{SNS})$$

Where: $V_{(SET)}$ is the output of the ISET pin and $K_{(SET)}$ is the output current set factor.

BATTERY VOLTAGE REGULATION

The voltage regulation feedback is through the BAT pin. This input is tied directly to the positive side of the battery pack. The bqSWITCHER monitors the battery-pack voltage between the BAT and VSS pins. The bqSWITCHER is offered in two fixed-voltage versions: 4.2V and 8.4V as selected by the CELLS input. A low or floating input on the CELLS selects single cell (4.2V) while a high input selects two-cell. Floating the CELLS pin defaults to a low input, 1CELL, with an internal pull-down resistor. Similar (2Cell / 3Cell) spins will be available. Fixed cell spins will internally be set to 4.2, 8.4, or 12.6V.

For spins with adjustable output voltage, the voltage regulation feedback is through the FB pin. A resistor divider is used from the battery output voltage to GND. BAT is still connected directly to the battery output voltage for current sensing with respect to SNS. A small capacitor can be used from BAT to FB to provide a Zero-Pole pair if additional phase boost is needed for stability.

CHARGE TERMINATION AND RECHARGE

The bqSWITCHER monitors the charging current during the voltage regulation phase. Once the taper threshold, $I_{(TAPER)}$, is detected the bqSWITCHER terminates charge. The taper current level is selected by the value of programming resistor, $R_{(SET2)}$, connected to the ISET2 pin.

As a safety backup, the bqSWITCHER also provides a programmable charge timer. The charge time is programmed by the value of resistor and capacitor connected to the PROG pin and by the following formula:

$t_{(CHG)} = C_{(TMR)} \times K_{(TMR)}$

Where $C_{(TMR)}$ is the capacitor connected to the TMR pin, and $K_{(TMR)}$ is the multiplier. Charge timer can be disabled or reset by floating the TMR pin.

A new charge cycle is initiated when one of the following conditions are detected:

- The battery voltage falls below the $V_{(RCH)}$ threshold
- Power-on reset (POR)

SLEEP MODE

The bqSWITCHER enters the low-power sleep mode if the Vcc is removed from the circuit. This feature prevents draining the battery during the absence of Vcc.

CHARGE STATUS OUTPUTS

The open-drain STAT1 and STAT2 outputs indicate various charger operations as shown in the following table. These status pins can be used to drive LEDs or communicate to the host processor. Note that OFF indicates the open-drain transistor is turned off.

Figure 6. Status Pins Summary

Charge State	STAT1	STAT2
Battery Absent	OFF	OFF
Charge-in-Progress	ON	OFF
Charge Done	OFF	ON
Charge Suspend, timer fault, overvoltage or sleep mode	OFF	OFF

/PG OUTPUT

The open-drain /PG (Power Good) indicates when the AC adapter (i.e. Vcc) is present. The output turns ON when Sleep-mode exit threshold, $V_{(SLP-EXIT)}$, is detected. This output is turned off in the sleep mode. The /PG pin can be used to drive an LED or communicate to the host processor.

/CE INPUT (CHARGE ENABLE)

The /CE digital input is used to disable or enable the charge process. A low-level signal on this pin enables the charge and a high-level signal disables the charge. A high to low transition on this pin also resets all timers and fault conditions. Note that the /CE pin cannot be pulled up to VTSB voltage. This may create power up issues.

BATTERY ABSENT DETECTION

For applications with removable battery packs, bqSWITCHER provides a battery absent detection scheme to reliably detect insertion and/or removal of battery packs.

The voltage at the BAT pin is held above the battery recharge threshold, $V_{(RCH)}$, by the charged battery following fast charging. When the voltage at the BAT pin falls to the recharge threshold, either by a load on the battery or due to battery removal, the bqSWITCHER begins a battery absent detection test. This test involves enabling a detection current, $I_{(DETECT)}$, for a period of $t_{(DETECT)}$ and checking to see if the battery voltage is below the pre-charge threshold, $V_{(LOWV)}$. Following this, the precharge current, $I_{O(PRECHG)}$ is applied for a period of $t_{(DETECT)}$ and the battery voltage checked again to be above the recharge threshold. The purpose of this current is to attempt to "close" a battery pack with an open protector, if one is connected to the bqSWITCHER. Passing both of the discharge and charging tests indicates a battery absent fault at the STAT pins. Failure of either test will start a new charge cycle. For the absent battery condition the voltage on the BAT pin will rise and fall between the $V_{(LOWV)}$ and $V_{O(REG)}$ thresholds indefinitely. See Figure 7.

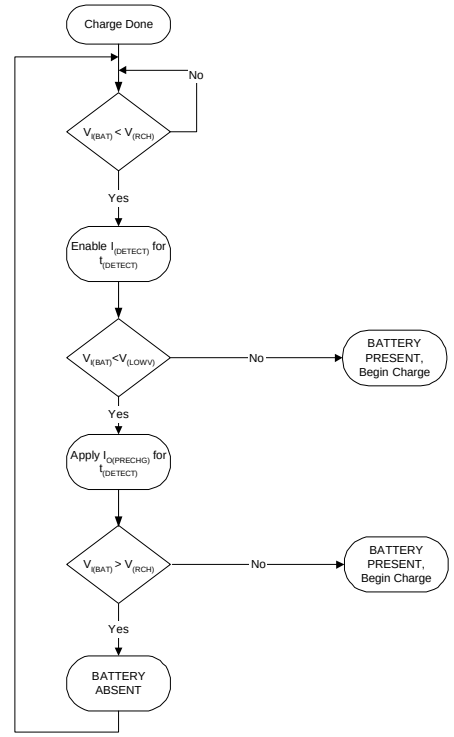


FIGURE 7. Battery Absent Detection

TIMER FAULT RECOVERY

As shown in Figure 5, bqSWITCHER provides a recovery method to deal with timer fault conditions. The following summarizes this method:

Condition #1: Charge voltage above recharge threshold ($V_{(RCH)}$) and timeout fault occurs

Recovery method: bqSWITCHER waits for the battery voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge or battery removal. Once the battery falls below the recharge threshold, the bqSWITCHER clears the fault and enters the battery absent detection routine. A POR or /CE or /TTE toggle also clears the fault.

Condition #2: Charge voltage below recharge threshold ($V_{(RCH)}$) and timeout fault occurs

Recovery method: Under this scenario, the bqSWITCHER applies the $I_{(FAULT)}$ current. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, then the bqSWITCHER disables the $I_{(FAULT)}$ current and executes the recovery method described for condition #1. Once the battery falls below the recharge threshold, the bqSWITCHER clears the fault and enters the battery absent detection routine. A POR or /CE toggle also clears the fault.

OUTPUT OVER VOLTAGE PROTECTION (APPLIES TO ALL VERSIONS)

The bqSWITCHER provides a built-in over voltage protection to protect the IC and other components against damages if the battery voltage gets too high, as when the battery is suddenly removed.

FUNCTIONAL DESCRIPTION FOR SYSTEM-CONTROLLED VERSION (bq2410x)

For applications requiring charge management under the host system control, the bqSWITCHER (bq2411x) offers a number of control functions. The following section describes these functions:

PRECHARGE AND FAST CHARGE CONTROL

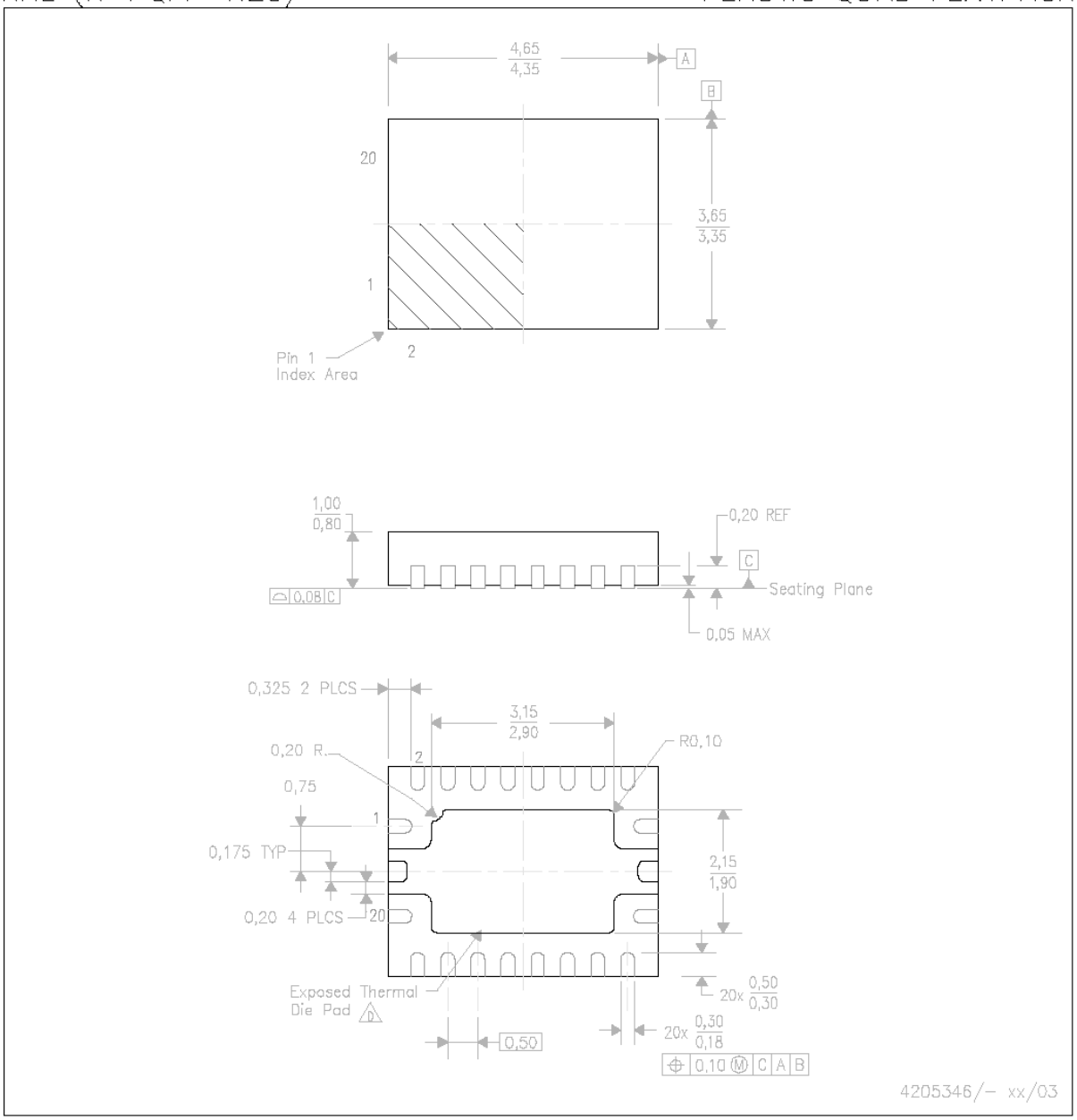
A low-level signal on the CMODE pin forces the bqSWITCHER to charge at the precharge rate set on the ISET2 pin. A high level signal forces charge at fast charge rate as set by the ISET1 pin. If the battery reaches the voltage regulation level, $V_{O(REG)}$, the bqSWITCHER transitions to voltage regulation phase regardless of the status of the CMODE input.

CHARGE TERMINATION AND SAFETY TIMERS

The charge timers and termination are disabled in the system-controlled versions of the bqSWITCHER. The host system can use the /CE input to enable or disable charge. When an overvoltage condition is detected, the charger process stops, all powerFETs are turned off.

PACKAGING

RHL (R–PQFP–N20) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The Package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.