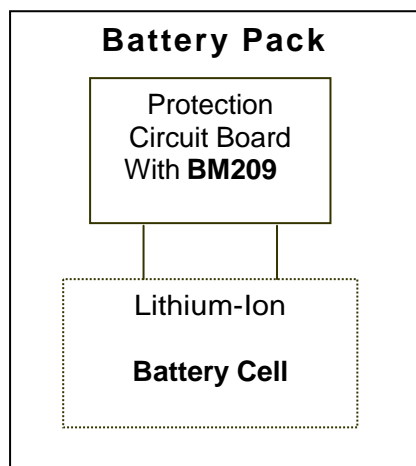


### General Description

The BM209 series are protection ICs for Lithium-ion rechargeable battery packs. It includes voltage detection unit, voltage reference unit, bias unit, delay unit, and logic circuits. The BM209 series have cell-balance function and high-accuracy voltage detection for protecting Two-cell lithium battery packs from overcharge, over-discharge, excess-current and short circuit.

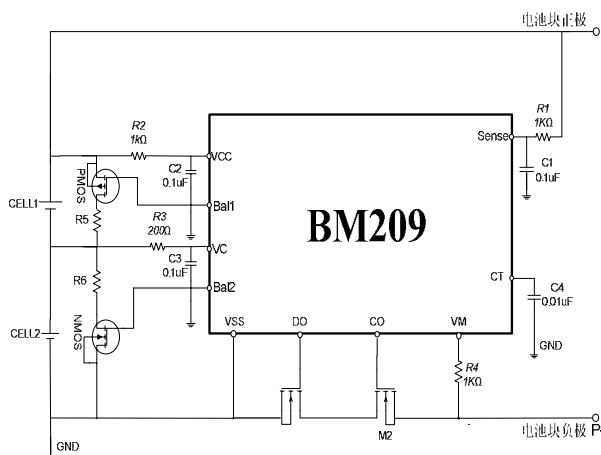
### Applications



### Features

- **Overcharge Threshold**
  - 4.100~4.400V
  - Accuracy Min.  $\pm 25\text{mV}$  (25 )  $\pm 50\text{mV}$  (-20 ~70 )
- **Over-discharge Threshold**
  - Typ. 2.33V
  - Accuracy Min.  $\pm 80\text{mV}$
- **Balance Threshold**
  - Typ. 4.07V
  - Accuracy  $\pm 0.10\text{V}$
- **Excess Current 1 Protection Threshold**
  - Typ. 0.30V @ VC = 3.30V, VCC = 6.60V
  - Accuracy  $\pm 0.03\text{V}$
- **Excess Current 2 Protection Threshold**
  - Typ. 0.60V @ VC = 3.30V, VCC = 6.60V
  - Accuracy  $\pm 0.10\text{V}$
- **Short Circuit Protection Threshold**
  - Typ. 1.50V @ VC = 3.30V, VCC = 6.60V
  - Accuracy  $\pm 0.50\text{V}$
- **Low power consumption**
  - Typ. 10.0uA @ VC = 3.90V, VCC = 7.80V (Standard working current)
  - Typ. 0.90uA @ VC = 2V, VCC = 4V (Standby current)
- **Output Delay of Overcharge**
  - Typ. 100ms (connect a 0.01uF cap to CT)
- **Output Delay of Over-discharge**
  - Typ. 24ms @ VC = 2.20V, VCC = 4.40V

### Typical Application Circuits



### Recommended value:

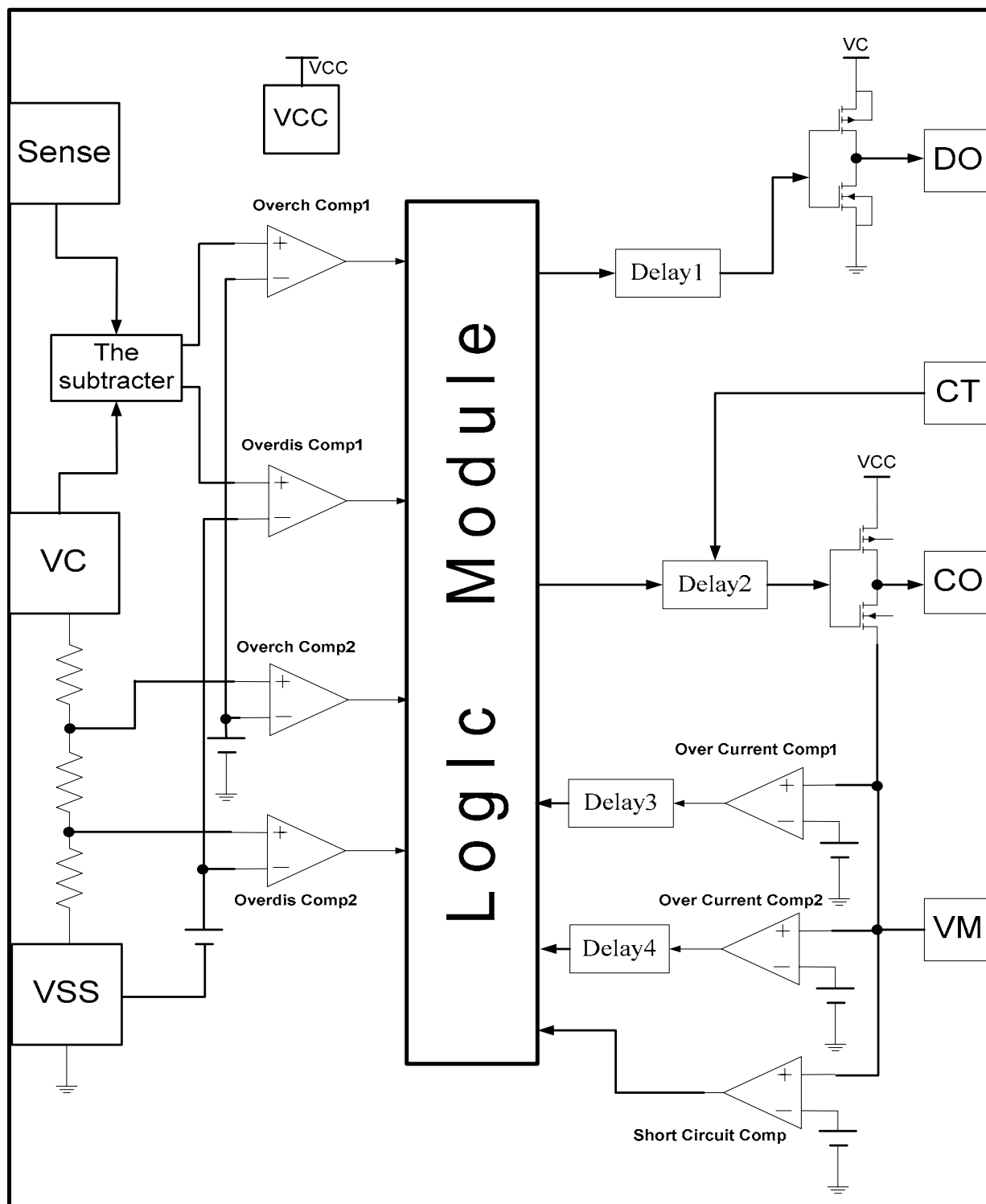
$R_1=R_2=R_4=1\text{k}\Omega$ ;  $R_3=200\Omega$ ;  $C_1=C_2=C_3=0.10\mu\text{F}$

### Notes

$R_1C_1$ ,  $R_2C_2$  and  $R_3C_3$  are to stabilize the supply voltage of the BM209 series.  $R_1C_1$  is hence regarded as the time constant for Sense pin.  $R_2C_2$  is hence regarded as the time constant for VCC pin.  $R_2$  and  $R_4$  can also be a part of current-limit circuit for the BM209 series. Recommended values of these elements are as follows:

- $R_3 < 470\Omega$ . A larger value of  $R_3$  results in high detection voltage, low detection accuracy.
- $R_4 < 2.5\text{k}\Omega$ . A larger value of  $R_4$  possibly counteracts resetting from over-discharge even with a charger.
- $R_5$ ,  $R_6$  is determined by your balance bypass current.  $R_2 + R_4 > 2\text{k}\Omega$ . Smaller values may lead to power consumption over the maximum dissipation rating of the BM209 series.

## Block Diagram



## Selection Guide

### ● Type Number

**BM209 – XXXX**

Symbol	Meaning	Description
XXXX	Overcharge/Over-discharge/Excess Current 1 detection threshold and accuracy	Assigned from AAAA to WWWW

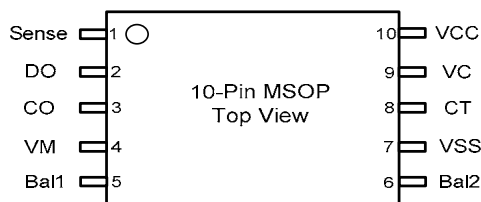
### ● Type Number Option

Through choosing the “XXXX”, the Overcharge Detection Threshold Voltage (VCT1,2), the Over-discharge Detection Threshold voltage (VDT1,2), the Excess Current 1 Detection Voltage (VIT) and their accuracy of BM209 can be decided.

**Table 1. VCT1,2 & VDT1,2 & Marking** ( @ 25 )

Type Number	Overcharge detection voltage 1,2 VCT1,2	Overcharge release voltage 1,2 VCR1,2	Over-discharge detection voltage 1,2 VDT1,2	Over-discharge release voltage 1,2 VDR1,2	Excess current 1 detection VIT1	Cell balance Detection VBAL1,2	Mark
BM209-LHHA	4.275V±25mV	4.075±100mV	2.32V±80mV	3.02V±150mV	0.30V±30mV	4.05V±100mV	9LHHA
BM209-MHHA	4.300V±25mV	4.100±100mV	2.33V±80mV	3.03V±150mV	0.30V±30mV	4.07V±100mV	9MHHA
BM209-HHHA	4.325V±25mV	4.125±100mV	2.34 V±80mV	3.04V±150mV	0.30V±30mV	4.10V±100mV	9HHHA
BM209-SHHA	4.350V±25mV	4.150±100mV	2.35 V±80mV	3.05V±150mV	0.30V±30mV	4.12V±100mV	9SHHA

## Package Type



## Pin Description

Pin number	Pin name	Description
1	Sense	The overcharge/over-discharge detection pin, for monitoring voltage relative to VC
2	DO	Over-discharge detection pin, CMOS output
3	CO	Overcharge detection pin, CMOS output
4	VM	The excess-current detection pin
5	Bal1	The balance control pin of cell1.
6	Bal2	The balance control pin of cell2.
7	VSS	Ground
8	CT	To connect capacitor for Overcharge detection delay
9	VC	The middle pin between two cells (to connect cell 1 cathode and cell 2 anode)
10	VCC	Positive power input pin (to connect cell 1 anode)

## Function Description

### 1 . Normal Condition:

When both VC and (VCC-VC) are between the Over-discharge Detection Threshold Voltage (VDT) and the Overcharge Detection Threshold Voltage (VCT), and the VM pin voltage between the Charger Detection Threshold Voltage (VCHA) and the Excess Current 1 Detection Threshold Voltage (VIT1), the outputs of DO pin and CO pin are on high level, making the charge and discharge MOSFETs on. Charging and discharging can be carried out freely.

### 2 . Overcharge Condition:

During charging, when VC or (VCC - VC) increases higher than VCT and takes the Overcharge Detection Delay Time ( $T_{CT}$ ) or longer, the output of CO pin will change from high level to low level, turning off the charging control FET to stop charging.

### 3 . Overcharge Protection Release Condition:

The output of CO pin will change to high level, making charging recovered, when either of the following conditions come into being: (1) both VC and (VCC - VC) become lower than the Overcharge Release Voltage (VCR); (2) a load connects to VCC after a charger is disconnected from the battery pack, and both VC and (VCC - VC) are lower than VCT.

### 4 . Over-discharge Condition:

During discharging, when VC or (VCC - VC) decreases lower than VDT and taking the Over-discharge Detection Delay Time ( $T_{DT}$ ) or longer, the output of DO pin will change from high level to low level, turning off the discharging control FET to stop discharging.

### 5 . Over-discharge Protection Release Condition:

The output of DO pin will change to high level, making discharging recovered, when either of the following conditions come into being: (1) a charger is connected to the battery pack, and the battery supply voltage becomes higher than VDT, and VM is higher than the Charger Detection Threshold Voltage (VCHA); (2) both the VC and (VCC - VC) become higher than the Over-discharge Release Voltage (VDR) and VM is between VCHA and VIT1.

### 6 . Excess Current 1 Protection:

During discharging, the current varies with load, and VM increases with the rise of the discharging current. Once VM rises higher than the Excess Current 1 Detection Threshold Voltage (VIT1) and stays longer than the Excess Current 1 Detection Delay Time ( $T_3$ ), DO pin changes from high to low level, turning off the discharging control FET. Once that excess current state is removed, i.e.  $VM < VIT1$ , and the circuit recovers to normal state.

#### 7 . Excess Current 2 Protection:

During discharging, the current varies with load, and VM increases with the rise of the discharging current. Once VM rises higher than the Excess Current 2 Detection Threshold Voltage (VIT2) and stays longer than the Excess Current 2 Detection Delay Time ( $T_4$ ), DO pin changes from high to low level, turning off the discharging control FET. Once that excess current state is removed, and  $VM < VIT1$ , and the circuit recovers to normal state.

#### 8 . Short Circuit Protection:

This function has the same principle as the excess current protection. But, the delay time  $T_5$  is far shorter than  $T_3$  and  $T_4$ , and the threshold VSHORT is far higher than VIT1 and VIT2. When the circuit is shorted, VM increases rapidly. Once  $VM \geq VSHORT$ , DO pin switches to low, turning off the discharging control FET. After the short circuit state is removed, and  $VM < VIT1$ , the circuit recovers to the normal state. The short circuit peak current is related to VSHORT and the ON resistance of the two FETs in series.

9 . Cell-balance Function: The cell-balance function is used to balance the two cells' voltage in the pack. When the (VCC-VC) is between the Cell-balance1 Threshold (VBAL1) and the Overcharge Detection Voltage(VCT), and VC is below the Cell-balance 2 Threshold (Vbal2) for the Cell-balance 1 Detection Delay Time( $T_{BAL1}$ ) or longer, the Bal1 pin controls the

P-MOSFET to switch on the bypass balance circuit.

When the (VCC-VC) is higher than the Overcharge Detection Threshold Voltage (VCT), or the VC is higher than the Cell-balance 2 Threshold (Vbal2), the bypass balance circuit is switched off by the P-MOSFET.

As the same, when the VC is between the Cell-balance 2 Threshold (VBAL2) and the Overcharge Detection Threshold Voltage (VCT), and (VCC-VC) is below the Cell-balance 1 Threshold (VBAL1) for the Cell-balance 2 Detection Delay Time( $T_{BAL2}$ ) or longer, the Bal2 pin controls the N-MOSFET to switch on the other bypass balance circuit. When the VC is higher than the Overcharge Detection Threshold Voltage (VCT) or the (VCC-VC) is higher than the Cell-balance Threshold 1(VBAL1), the bypass balance circuit is switched off by the N-MOSFET.

#### 10 . Abnormal Charge Current Condition:

If the VM pin voltage falls below the Abnormal Charge Current Detection Threshold Voltage (VAB) during charging under normal condition and takes the Abnormal Charge Current Detection Delay Time ( $T_{AB}$ ) or longer, the charging control FET is turned off and charging stops. This action is called the Abnormal Charge Current Detection. Abnormal charge current detection works when the DO pin voltage is "H" and the VM pin voltage falls below the Abnormal Charge Current Detection Threshold Voltage (VAB). To an over-discharged battery, only when charging makes the battery voltage higher than the Over-discharge Detection Threshold (VDT), the

Abnormal Charge Current Detection can act. Abnormal charge current state is released, once the voltage difference between VM pin and VSS pin becomes less than the Abnormal Charge Current Detection Threshold Voltage (VAB) value.

#### 11 . Charger Detect Condition:

A two-cell battery in over-discharge condition can be released, when it is connected to a charger, the VM pin voltage is lower than the Abnormal Charge Current

Detection Threshold Voltage (VAB), and each cell voltage becomes higher than the Over-discharge Detection Threshold Voltage (VDT). This action is called Charger Detection. But, if the VM pin voltage is between the Abnormal Charge Current Detection Threshold Voltage (VAB) and the Excess Current 1 Detection Threshold Voltage (VIT1), the over-discharge state is not released unless the two cell voltages both become higher than the Over-discharge Release Voltage (VDR).

**Electrical Characteristic <sup>1\*</sup>**

(T<sub>OPT</sub>=25 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Circuit
<b>Detection Voltage and Delay Time (C<sub>4</sub>=0.01u F)</b>							
Over charge Detection Voltage 1,2	VCT1,2 <sup>2*</sup>	25	VCT1,2-0.025	VCT1,2	VCT1,2+0.025	V	1
Over charge Release Voltage 1,2	VCR1,2 <sup>3*</sup>	25	VCT1,2-0.30	VCT1,2-0.2	VCT1,2-0.10	V	1
Over-discharge Detection Voltage 1,2	VDT1,2 <sup>2*</sup>	25	VDT1,2-0.08	VDT1,2	VDT1,2+0.08	V	1
Over-discharge Release Voltage 1,2	VDR1,2 <sup>3*</sup>	25	VDT1,2+0.55	VDT1,2+0.7	VDT1,2+0.85	V	1
Excess Current 1 Detection Voltage	VIT1	V1=V2=3.30V	0.27	0.30	0.33	V	1
Excess Current 2 Detection Voltage	VIT2	V1=V2=3.30V	0.50	0.60	0.70	V	1
Short Circuit Detection Voltage	VSHORT	V1=V2=3.30V	1	1.50	2	V	1
Cell-balance 1 Threshold	VBAL1	25	3.97	4.07	4.17	V	1
Cell-balance 2 Threshold	VBAL2	25	3.97	4.07	4.17	V	1
Abnormal Charge Detection Voltage	VAB	V1=V2=3.30V	-0.17	-0.15	-0.13	V	1
Charger Detection Voltage	VCHA	V1=V2=3.30V	-0.17	-0.15	-0.13	V	1
Over Charge Detection Delay Time	T <sub>CT</sub>	V1=V2=4.40V	50	100	200	ms	3
Over -discharge Detection Delay Time	T <sub>DT</sub>	V1=V2=2.20V	12	24	48	ms	3
Over Current 1 Detection Delay Time	T <sub>3</sub>	V1=V2=3.30V	6	12	24	ms	3
Over Current 2 Detection Delay Time	T <sub>4</sub>	V1=V2=3.30V	1	2	3	ms	3
Short Circuit Detection Delay Time	T <sub>5</sub>	V1=V2=3.30V			10	us	3
Abnormal Charge Detection Delay Time	T <sub>AB</sub>	V1=V2=3.30V	42	85	170	ms	3
Cell-balance 1 Detection Delay Time	T <sub>BAL1</sub>	V1=4.20V V2=3.30V	3	5	10	ms	3
Cell-balance 2 Detection Delay Time	T <sub>BAL2</sub>	V1=3.30V V2=4.20V	3	8	15	ms	3
<b>Output Voltage And VM Internal Resistance</b>							
CO "H" Voltage	VCO(H)	V1=V2=3.90V	7.55	7.60		V	4
CO "L" Voltage	VCO(L)	V1=V2=4.40V		0.10	0.13	V	4
DO "H" Voltage	VDO(H)	V1=V2=3.90V	3.77	3.82		V	4
DO "L" Voltage	VDO(L)	V1=V2=2.20V		0.05	0.08	V	4
Resistance Between VM And VCC	R <sub>VMD</sub>	V1=V2=2.20V VM=0V	40	110	200	KΩ	4
Resistance Between VM And VSS	R <sub>VMS</sub>	V1=V2=3.30V VM=1V	50	150	300	KΩ	4
<b>Operation Voltage And Current Consumption</b>							
Operation Voltage Between VCC And VSS	VCSOP	25	2	-	16	V	
Operation Voltage Between VCC And VM	VCMOP	25	5	-	28		
Current Consumption During Normal State	I <sub>OPE</sub>	V1=V2=3.90V	5	10	15	uA	2
Current Consumption During Power Down	I <sub>PDN</sub>	V1=V2=2.20V	0.50	0.90	1.50	uA	2

1\* The Electrical parameters for this temperature range is guaranteed by design, not tested in production.

2\* See "Selection Guide" section.

3\* VCT1,2 and VDT1,2 are the Overcharge and Over-discharge threshold voltage of actual testing.

4\* V1 is the voltage of cell1 and V2 is the voltage of cell2, refer to the Typical Application Circuits and test circuits.

**Electrical Characteristic <sup>1\*</sup>**

(T<sub>OPT</sub>=-20~70 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Circuit
<b>Detection Voltage and Delay Time (C<sub>4</sub>=0.01u F)</b>							
Over charge Detection Voltage 1,2	VCT1,2 <sup>2*</sup>		VCT1,2-0.050	VCT1,2	VCT1,2+0.050	V	1
Over charge Release Voltage 1,2	VCR1,2 <sup>3*</sup>		VCT1,2-0.35	VCT1,2-0.2	VCT1,2-0.05	V	1
Over-discharge Detection Voltage 1,2	VDT1,2 <sup>2*</sup>		VDT1,2-0.10	VDT1,2	VDT1,2+0.10	V	1
Over-discharge Release Voltage 1,2	VDR1,2 <sup>3*</sup>		VDT1,2+0.50	VDT1,2+0.7	VDT1,2+0.90	V	1
Excess Current 1 Detection Voltage	VIT1	V1=V2=3.30V	0.26	0.30	0.34	V	1
Excess Current 2 Detection Voltage	VIT2	V1=V2=3.30V	0.40	0.60	0.80	V	1
Short Circuit Detection Voltage	VSHORT	V1=V2=3.30V	1	1.50	2	V	1
Cell-balance 1 Threshold	VBAL1		3.92	4.07	4.22	V	1
Cell-balance 2 Threshold	VBAL2		3.92	4.07	4.22	V	1
Abnormal Charge Detection Voltage	VAB	V1=V2=3.30V	-0.18	-0.15	-0.12	V	1
Charger Detection Voltage	VCHA	V1=V2=3.30V	-0.18	-0.15	-0.12	V	1
Over Charge Detection Delay Time	T <sub>CT</sub>	V1=V2=4.40V	40	100	250	ms	3
Over -discharge Detection Delay Time	T <sub>DT</sub>	V1=V2=2.20V	8	24	60	ms	3
Over Current 1 Detection Delay Time	T <sub>3</sub>	V1=V2=3.30V	4	12	30	ms	3
Over Current 2 Detection Delay Time	T <sub>4</sub>	V1=V2=3.30V	1	2	5	ms	3
Short Circuit Detection Delay Time	T <sub>5</sub>	V1=V2=3.30V			10	us	3
Abnormal Charge Detection Delay Time	T <sub>AB</sub>	V1=V2=3.30V	40	100	250	ms	3
Cell-balance 1 Detection Delay Time	T <sub>BAL1</sub>	V1=4.20V V2=3.30V	3	5	12	ms	3
Cell-balance 2 Detection Delay Time	T <sub>BAL2</sub>	V1=3.30V V2=4.20V	3	8	20	ms	3
<b>Output Voltage And VM Internal Resistance</b>							
CO "H" Voltage	VCO(H)	V1=V2=3.90V	7.50	7.60		V	4
CO "L" Voltage	VCO(L)	V1=V2=4.40V		0.10	0.15	V	4
DO "H" Voltage	VDO(H)	V1=V2=3.90V	3.72	3.82		V	4
DO "L" Voltage	VDO(L)	V1=V2=2.20V		0.05	0.10	V	4
Resistance Between VM And VCC	R <sub>VMD</sub>	V1=V2=2.20V VM=0V	30	110	250		4
Resistance Between VM And VSS	R <sub>VMS</sub>	V1=V2=3.30V VM=1V	40	150	400		4
<b>Operation Voltage And Current Consumption</b>							
Operation Voltage Between VCC And VSS	VCSOP		2	-	16	V	
Operation Voltage Between VCC And VM	VCMOP		5	-	28		
Current Consumption During Normal State	I <sub>OPE</sub>	V1=V2=3.90V	5	10	18	uA	2
Current Consumption During Power Down	I <sub>PDN</sub>	V1=V2=2.20V	0.50	0.90	1.50	uA	2

1\* The Electrical parameters for this temperature range is guaranteed by design, not tested in production.

2\* See "Selection Guide" section.

3\* VCT1,2 and VDT1,2 are the Overcharge and Over-discharge threshold voltage of actual testing.

4\* V1 is the voltage of cell1 and V2 is the voltage of cell2, refer to the Typical Application Circuits and test circuits.



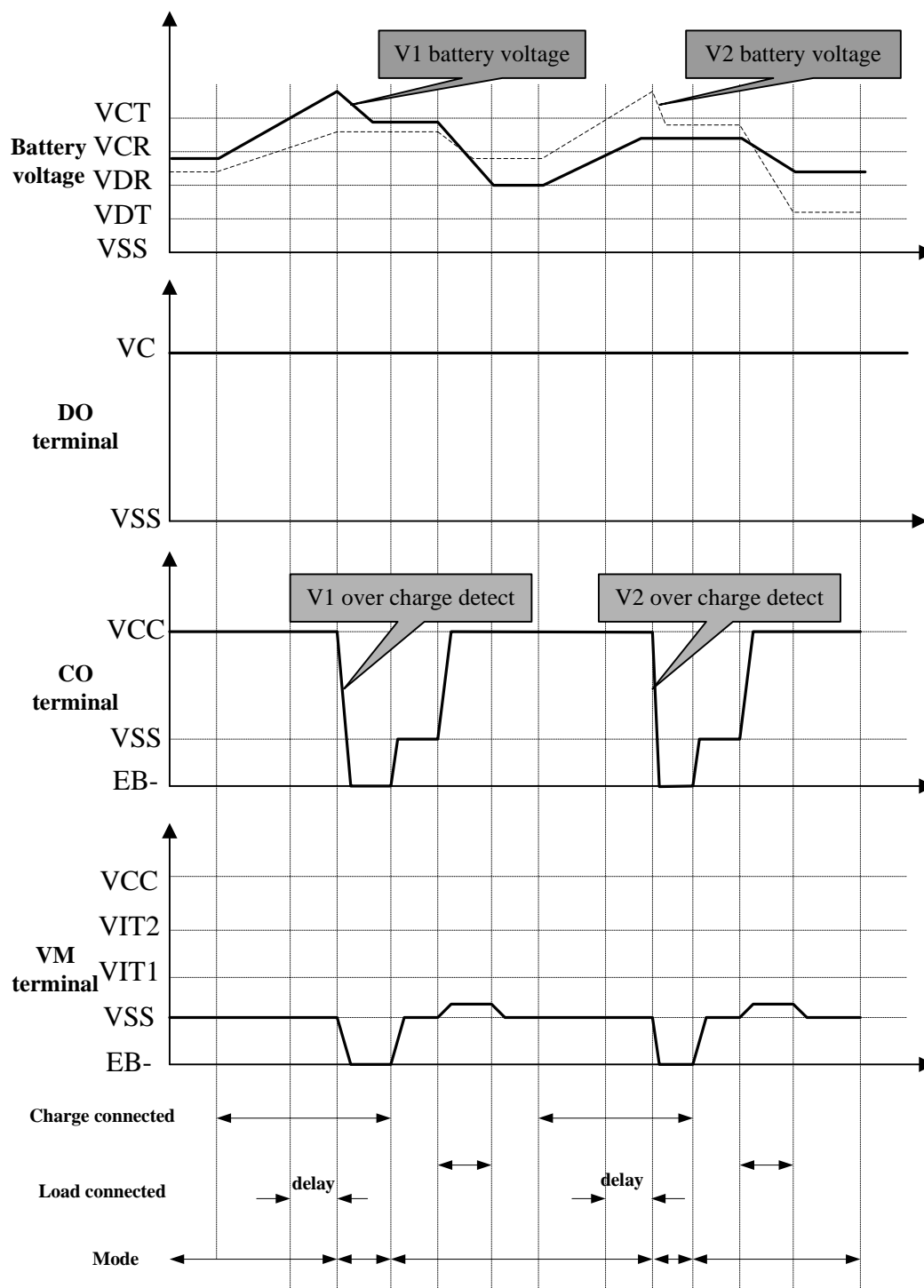
## Absolute Maximum Ratings

Item	Symbol	Pin	Rated Value	Unit
VCC-VSS Input Voltage	$V_{DS}$	VCC	VSS-0.30~VSS+18	V
Sense Pin Input Voltage	$V_{Sense}$	Sense	VSS-0.30~VCC+0.30	V
Delay Pin Input Voltage	$V_{CT}$	CT	VSS-0.30~VCC+0.30	V
VM Pin Input Voltage	$V_{VM}$	VM	VCC-28~VCC+0.30	V
DO Pin Output Voltage	$V_{DO}$	DO	VSS-0.30~VC+0.30	V
CO Pin Output Voltage	$V_{CO}$	CO	VM-0.30~VCC+0.30	V
Power Dissipation	$P_D$	-----	300	mW
Operation Temperature	$T_{opr}$	-----	-20~+85	
Storage Temperature	$T_{stg}$	-----	-40~+125	

Attention: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

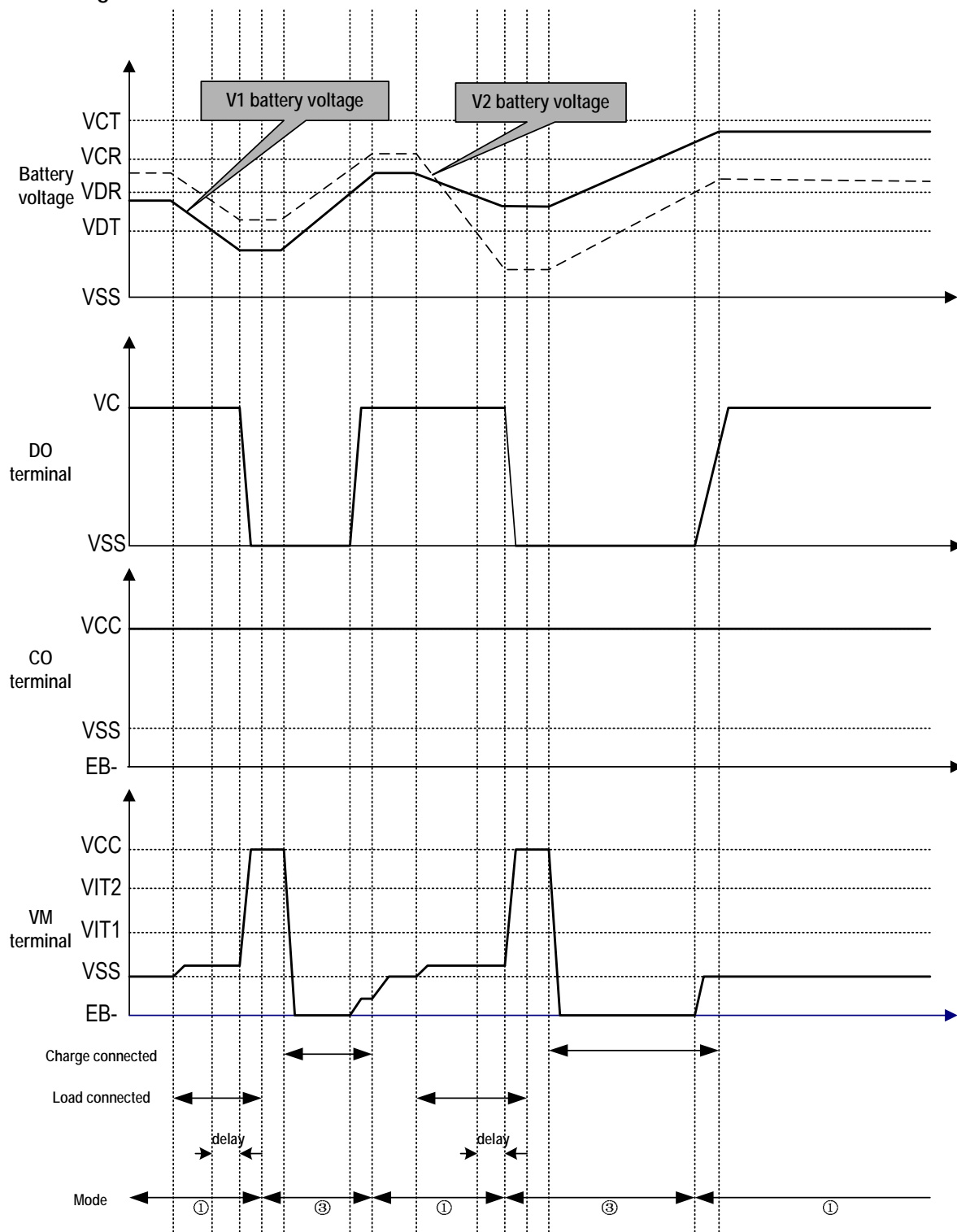
## Operation Timing Charts:

Overcharge:



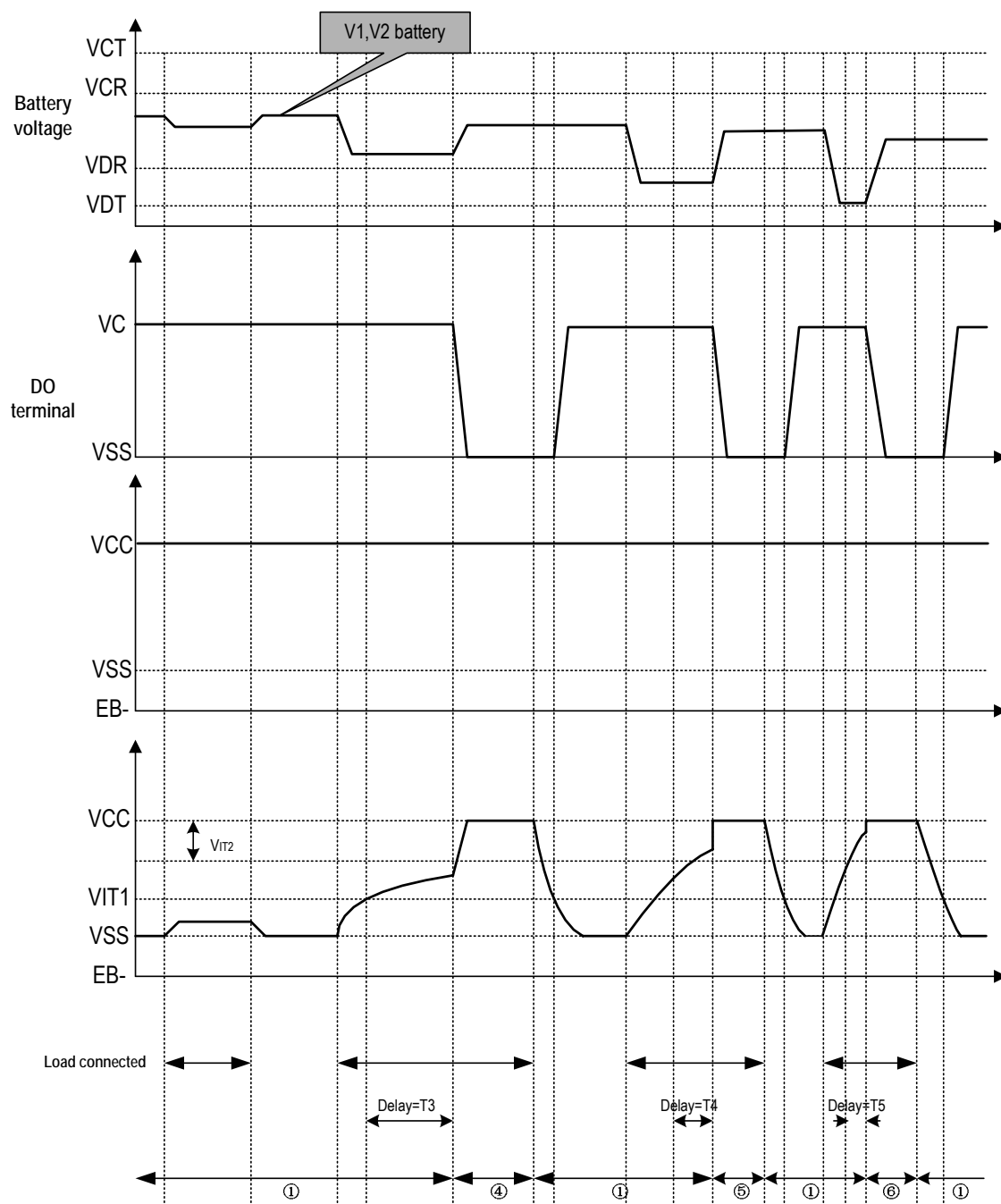
Note: Normal mode Overcharge mode Over-discharge mode  
 Excess current 1 mode Excess current 2 mode  
 Short circuit mode Bypass current work mode  
 The number N = the times of the charge-discharge cycle.

Over-discharge :



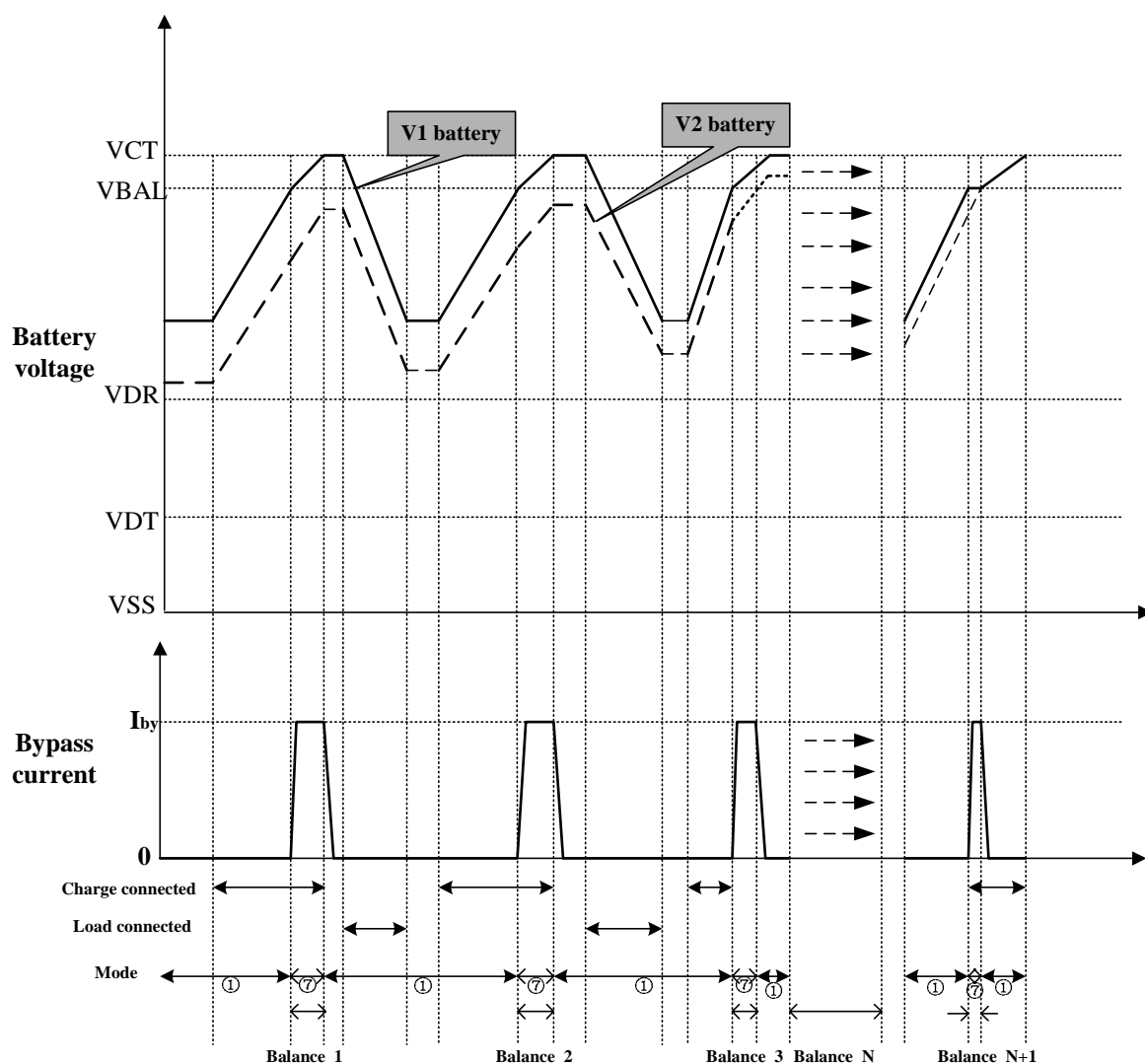
Note: Normal mode Overcharge mode Over-discharge mode  
 Excess current 1 mode Excess current 2 mode  
 Short circuit mode Bypass current work mode  
 The number N = the times of the charge-discharge cycle.

Excess current:



Note:      Normal mode      Overcharge mode      Over-discharge mode  
              Excess current 1 mode      Excess current 2 mode  
              Short circuit mode      Bypass current work mode  
 The number N = the times of the charge-discharge cycle.

Cell-balance Function:



Note:      Normal mode    Overcharge mode    Over-discharge mode  
               Excess current 1 mode    Excess current 2 mode  
               Short circuit mode    Bypass current work mode  
 The number N = the times of the charge-discharge cycle.

## Test Circuits

### (1) Overcharge detection threshold voltage and overcharge release voltage

#### Test circuit 1

Set  $V_2=3.30V$   $V_3=0V$ , the Overcharge Detection Threshold Voltage (VCT1) is the voltage between VCC and VC to which when  $V_1$  increases and keeps the condition for the Overcharge Detection Delay Time ( $T_{CT}$ ), VCO changes from “H” to “L”. The overcharge release voltage (VCR1) is the voltage between VCC and VC to which when  $V_1$  decreases, VCO changes from “L” to “H”.

Set  $V_1=3.30V$   $V_3=0V$ , the Overcharge Detection Threshold Voltage (VCT2) is the voltage between VC and VSS to which when  $V_2$  increases and keeps the condition for the Overcharge Detection Delay Time ( $T_{CT}$ ), VCO changes from “H” to “L”. The Overcharge Release Voltage (VCR2) is the voltage between VC and VSS to which when  $V_1$  decreases, VCO changes from “L” to “H”.

### (2) Over-discharge detection threshold voltage and over-discharge release voltage

#### Test circuit 1

Set  $V_2=3.30V$   $V_3=0V$ , the Over-discharge Detection Threshold Voltage (VDT1) is the voltage between VCC and VC to which when  $V_1$  decreases and keep the condition for the Over-discharge Detection Delay Time ( $T_{DT}$ ), VDO changes from “H” to “L”. The Over-discharge Release Voltage (VDR1) is the voltage between VC and VSS to which when  $V_1$  increases, VDO changes from “L” to “H”.

Set  $V_1=3.30V$   $V_3=0V$ , the Over-discharge Detection Threshold Voltage (VDT2) is the voltage between VC and VSS to which when  $V_2$  decreases and keep the condition for the Over-discharge Detection Delay Time ( $T_{DT}$ ), VDO changes from “H” to “L”. The Over-discharge Release Voltage (VDR2) is the voltage between VC and VSS to which when  $V_1$  increases, VDO changes from “L” to “H”.

### (3) Excess current detection threshold voltage and short circuit detection threshold voltage

#### Test circuit 1

Set  $V_1=V_2=3.30V$ , the Excess Current 1 Detection Threshold Voltage (VIT1) is the voltage  $V_3$  between VM and VSS to which when VM increases within 10 us and keep the

condition for the Excess Current 1 Detection Delay Time ( $T_3$ ), VDO changes from “H” to “L”.

The Excess Current 2 Detection Threshold Voltage (VIT2) is the voltage  $V_3$  between VM and VSS to which when VM increases within 10 us and keep the condition for the Excess Current 2 Detection Delay Time ( $T_4$ ), VDO changes from “H” to “L”.

The Short Circuit Detection Threshold Voltage (VSHORT) is the voltage  $V_3$  between VM and VSS to which when VM increases within 10us and keep the condition for the Short Circuit Detection Delay Time ( $T_5$ ), VDO changes from “H” to “L”.

### (4) Charger detection threshold voltage and abnormal charge current detection threshold voltage

#### Test circuit 1

In the over-discharge condition, increase  $V_2$  gradually until it is between VDT2 and VDR2. The voltage between VM and VSS to which when  $V_3$  decreases from 0V, VDO changes from “L” to “H”, is the Charger Detection Threshold Voltage (VCHA).

In the normal charging condition, the voltage between VM and VSS to which when  $V_3$  decreases from 0V, VCO changes from “H” to “L” is the Abnormal Charge Current Detection Threshold Voltage (VAB). It has the same value as the Charger Detection Threshold Voltage (VCHA).

### (5) Normal operation current consumption and power down current consumption

#### Test circuit 2

Set  $V_1=V_2=3.90V$ , the current A1 flowing through VCC and Sense pin and the current A2 flowing through VC pin are the normal operation consumption current ( $I_{OPE}$ ).

Set  $V_1=2.20V$   $V_2=2.20V$ , the current A1 flowing through VCC and Sense pin and the current A2 flowing through VC pin are the power down current consumption ( $I_{PDN}$ ).

### (6) Overcharge detection delay time and over-discharge detection delay time

#### Test circuit 3

Set  $V_3=0V$ , If  $V_1$  or  $V_2$  increases to be VCT1 or over VCT1 and keeps the condition for some time, VCO will change from “H” to “L”. The time is called Overcharge Detection Delay Time ( $T_{CT}$ ). It is used to judge whether overcharge

happens indeed.

#### Test circuit 3

Set  $V_3=0V$ , If  $V_1$  or  $V_2$  decreases to be  $V_{DT1}$  or below  $V_{DT1}$  and keeps the condition for some time, VDO will change from "H" to "L". The time is called Over-discharge Detection Delay Time ( $T_{DT}$ ). It is used to judge whether over-discharge happens indeed.

### (7) Excess current detection delay time and short circuit detection delay time

#### Test circuit 3

Set  $V_1=V_2=3.30V$ , If  $V_3$  increases to be  $V_{IT1}$  or over  $V_{IT1}$  and keeps the condition for some time, VDO will change from "H" to "L". The time is called Excess Current 1 Detection Delay Time ( $T_3$ ). It is used to judge whether excess current 1 happens indeed.

Set  $V_1=V_2=3.30V$ , If  $V_3$  increases to be  $V_{IT2}$  or over  $V_{IT2}$  and keeps the condition for some time, VDO will change from "H" to "L". The time is called Excess Current 2 Detection Delay Time ( $T_4$ ). It is used to judge whether excess current 2 happens indeed.

Set  $V_1=V_2=3.30V$ , If  $V_3$  increases to be  $V_{SHORT}$  or over  $V_{SHORT}$  and keeps the condition for some time, VDO will change from "H" to "L". The time is called Short Circuit Delay Time ( $T_5$ ). It is used to judge whether short circuit happens indeed.

### (8) Cell-balance threshold

#### Test Circuit 1

Set  $V_2=3.30V$   $V_3=0V$ , the Cell-balance1 threshold ( $V_{BAL1}$ ) is the voltage between VCC and VC to which when  $V_1$  increases and keeps the condition for Cell-balance 1 Detection Delay Time ( $T_{BAL1}$ ),  $V_{Bal1}$  changes from "H" to "L".

Set  $V_1=3.30V$   $V_3=0V$ , the overcharge detection voltage ( $V_{CT2}$ ) is the voltage VC which when  $V_2$  increases and keeps the condition for Cell-balance Detection 2 Delay Time ( $T_{BAL2}$ ),  $V_{Bal2}$  changes from "L" to "H".

### (9) Cell-balance Detection Delay Time

#### Test Circuit 3

Set  $V_2=3.30V$   $V_3=0V$ , If  $V_1$  increases to be  $V_{BAL1}$  or over  $V_{BAL1}$  but lower than  $V_{CT1}$  and keeps the condition for some time,  $V_{Bal1}$  will change from "H" to "L". The time is called cell-balance 1 detection delay time. It is used to judge

whether a bypass balance current is need indeed.

Set  $V_1=3.30V$   $V_3=0V$ , If  $V_2$  increases to be  $V_{BAL2}$  or over  $V_{BAL2}$  but lower than  $V_{CT2}$  and keeps the condition for some time,  $V_{Bal2}$  will change from "L" to "H". The time is called cell-balance 2 detection delay time. It is used to judge whether a bypass balance current is need indeed.

### (10) CO and DO output voltage

#### Test Circuit 4

Set  $V_1=V_2=3.90V$ ,  $V_5=0V$ , K1 on and K2 off, increase  $V_4$  from 0V gradually, the  $V_4$  voltage when  $A_2 = 50\mu A$  is the CO 'H' voltage ( $V_{COH}$ ).

Set  $V_1=V_2=4.40V$ ,  $V_5=0V$ , K1 on and K2 off, increase  $V_4$  from 0V gradually, the  $V_4$  voltage when  $A_2 = 50\mu A$  is the CO 'L' voltage ( $V_{COL}$ ).

Set  $V_1=V_2=3.90V$ ,  $V_5=0V$ , K1 off and K2 on, increase  $V_3$  from 0V gradually, the  $V_4$  voltage when  $A_1 = 50\mu A$  is the DO 'H' voltage ( $V_{DOH}$ ).

Set  $V_1=V_2=2.20V$ ,  $V_5=0V$ , K1 off and K2 on, decrease  $V_3$  from 0V gradually, the  $V_4$  voltage when  $A_1 = 50\mu A$  is the DO 'L' voltage ( $V_{DOL}$ ).

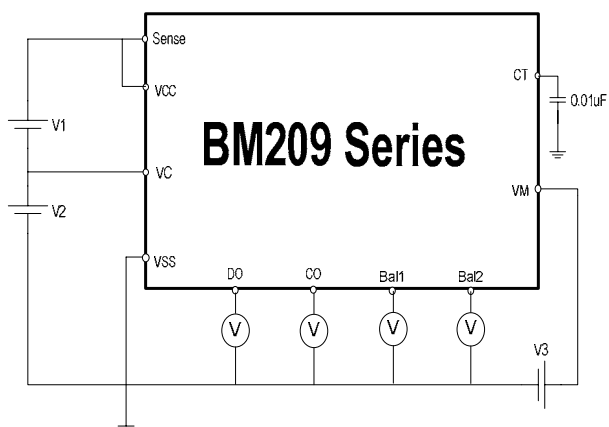
### (11) Internal resistance $V_M$ -VCC and $V_M$ -VSS

#### Test circuit 4

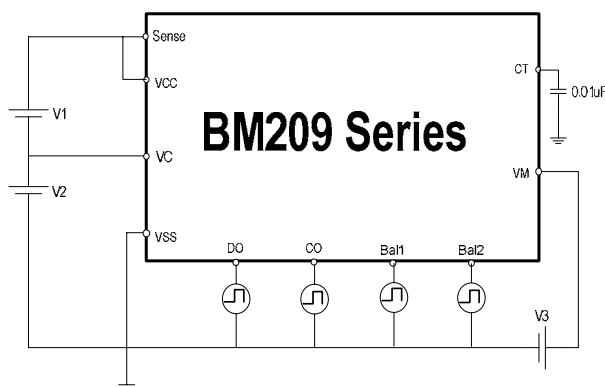
Set  $V_1=V_2=2.20V$ ,  $V_5=0V$ , K1 off and K2 off,  $(V_1+V_2)/I_3$  is the internal resistance  $R_{VMD}$ .

Set  $V_1=V_2=3.30V$ ,  $V_5=1V$ , K1 off and K2 off,  $V_5/I_3$  is the internal resistance  $R_{VMS}$ .

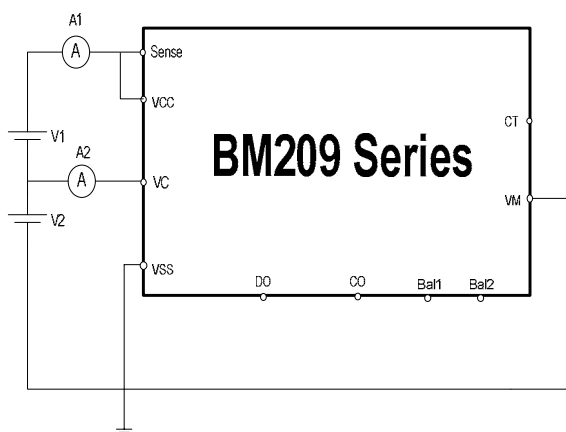
## Test Circuits



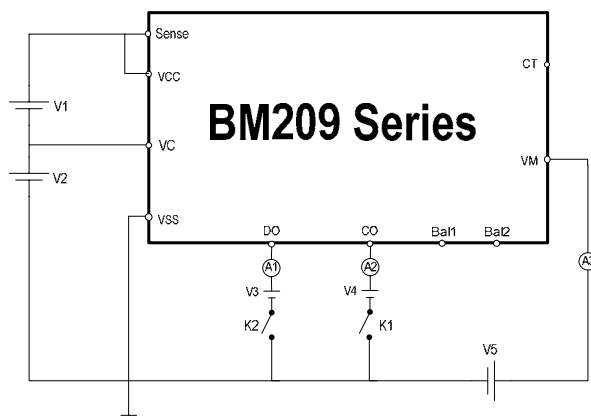
Circuit1



Circuit3



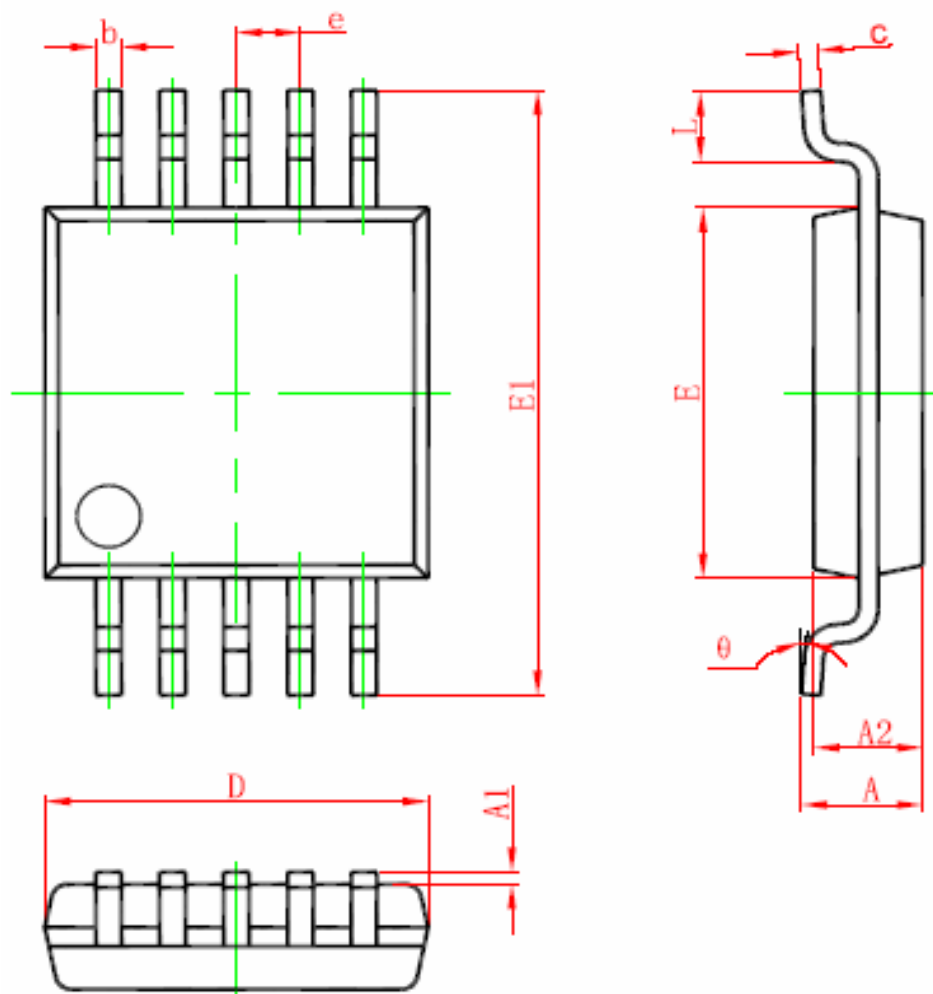
Circuit2



Circuit4



## Package Outline



### Dimensions

UNIT (mm)

	A	A1	A2	b	c	D	e	E	E1	L	
Min.	0.820	0.020	0.750	0.180	0.090	2.900	0.50	2.900	4.750	0.400	0 °
Max.	1.100	0.150	0.950	0.280	0.230	3.100	BSC	3.100	5.050	0.800	6 °

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