OZ8930 DATASHEET
Version 1.1

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Battery Pack Protection and Monitor IC

FEATURES

- **Supports 3-6 Series Li-ion, Li-polymer and Phosphate Battery Cells.**
- **Operation voltage range from 4.5V to 28V**
- **Multi-channel ADC for current, voltage and temperature measurement**
  - 6 channels for cell voltage measurement (12 bits) with effective accuracy of +/-20mV in working temperature range
  - 1 channel current measurement (14 bits), this programmable channel can be disabled to speed up the scan cycle
  - 1 channel for internal temperature measurement (12 bits)
  - 2 channels reserved for external temperature channels (12 bits)
  - ADC self-diagnostic
  - Supports ADC trigger scan by I²C control
- **Supports JEITA Requirements for different Charging/Discharging Voltage and Current protection threshold settings under low, standard and high temperature ranges**
- **Built-in Protections include:**
  - Over voltage (OV)
  - Under voltage (UV)
  - Over current (COC, DOC0, DOC1)
  - Short circuit (SC)
  - Over temperature (OT)
  - Under temperature (UT)
  - Cell Unbalance (UB)
  - Permanent Failure (PF)
- **Embedded OTP (One-Time-Programmable Memory) for programming various settings of protection thresholds/timers and protection release thresholds/timers.**
- **Supports separate charge and discharge over temperature threshold settings Embedded Internal Bleeding for Cell balance**
- **Supports EFETC MOSFET control signal**
- **Supports hardware mode (without MCU) or software mode (with external MCU)**
- **Supports separate charge and discharge loop and serial discharge/charge loop**
- **Integrated 1.8V, 3.3V, 10V voltage regulator**
- **Integrated N-MOSFET driver**
- **Supports I²C serial interface, the max communication speed is 400 KHz.**
- **Low power consumption**
  I_{VCC} in Full Power Mode < 380uA
  I_{VCC} in Sleep Mode < 45uA
  I_{VCC} in Standby Mode < 10uA
  I_{VCC} in Power Down < 1uA

GENERAL DESCRIPTION

OZ8930 is a highly integrated battery pack protection and monitor IC for managing Li-Ion or Li-polymer pack in backup power supply, power tools applications etc, and supporting the JEITA spec. It supports 3-6 series Li-Ion battery pack or Li-polymer or Phosphate battery pack applications.

Patent pending smart MOSFET driver is designed for controlling discharge N-MOSFET. Charge FET can be P-MOSFET or N-MOSFET through the design of external circuit. The driver also supports parallel and series charge and discharge loop.

With integrated multi-channel 14-bit ADC, OZ8930 works constantly to monitor each cell's voltage, the charge/discharge current and the pack temperature to provide over-voltage, under-voltage, charge over-current, over-temperature and under-temperature safety protection. Working with embedded FET driver, the protection circuits will independently shut off the FETs when the battery cells are experiencing extreme stress. OZ8930 can assert the Permanent Failure (PF) signal to blow an external fuse to cut off the power line or to issue an alarm to host/user when some extreme conditions happen. For example, when cell voltage is higher than the pre-set maximum rating voltage OVPF or cell temperature is higher than CELL_OTPF. All of the protection thresholds and their related delay time are programmable in OTP for different battery types and different applications.

With independent OC/SC protection function, OZ8930 provides multiple level discharge over current protection with programmable pre-set threshold and programmable delay control. A short circuit protection uses a fixed threshold and programmable delay control.

"Bleeding on Demand (BOD)" technology has been embedded in the OZ8930 to support internal bleeding for cell voltage balance during charge state and idle state (no charge and discharge); BOD technology can achieve longer life cycle of the battery pack.

OZ8930 can be configured to work in hardware mode or software mode. In hardware mode OZ8930 can work independently for battery pack protection and monitoring. In software mode, OZ8930 can work with MCU to implement more complete battery protection functions and gas gauge algorithm.

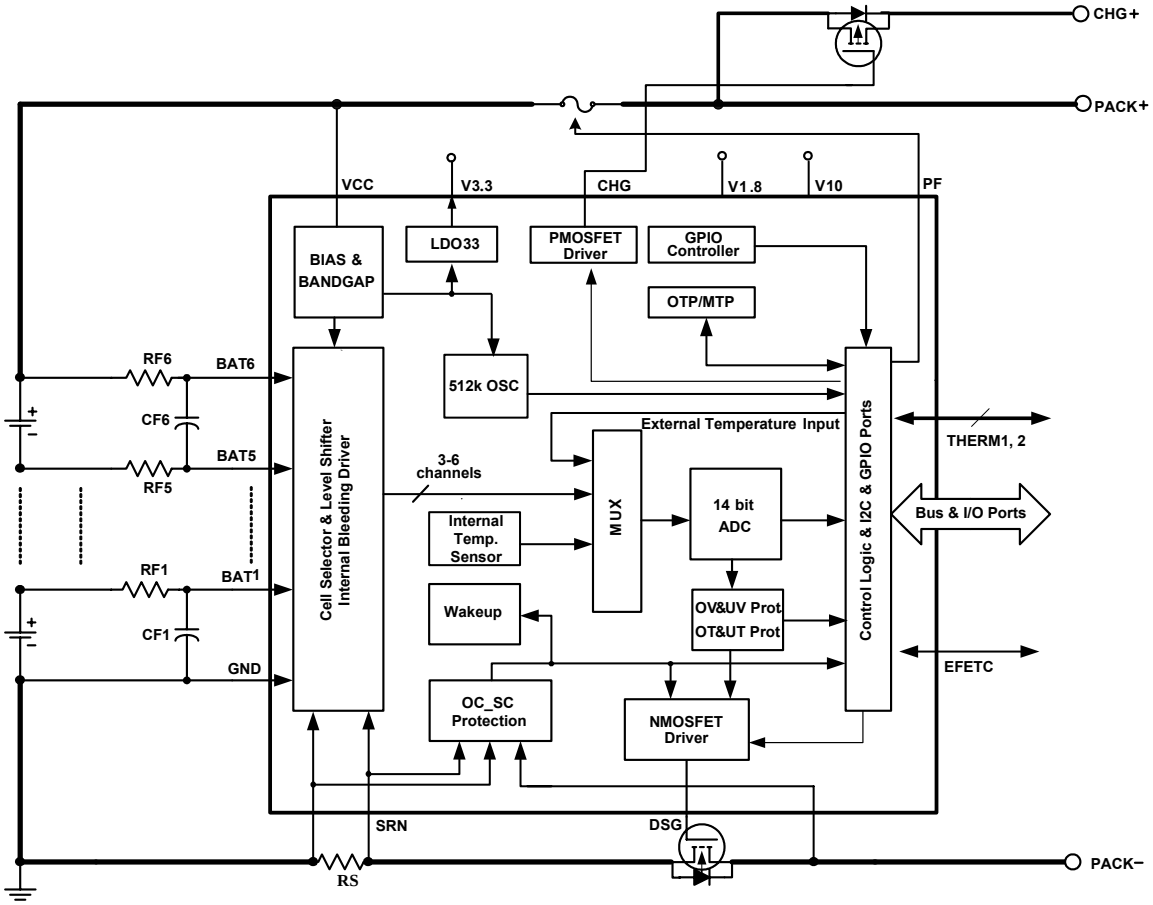
APPLICATIONS

- Power Tools
- Backup Power Supply

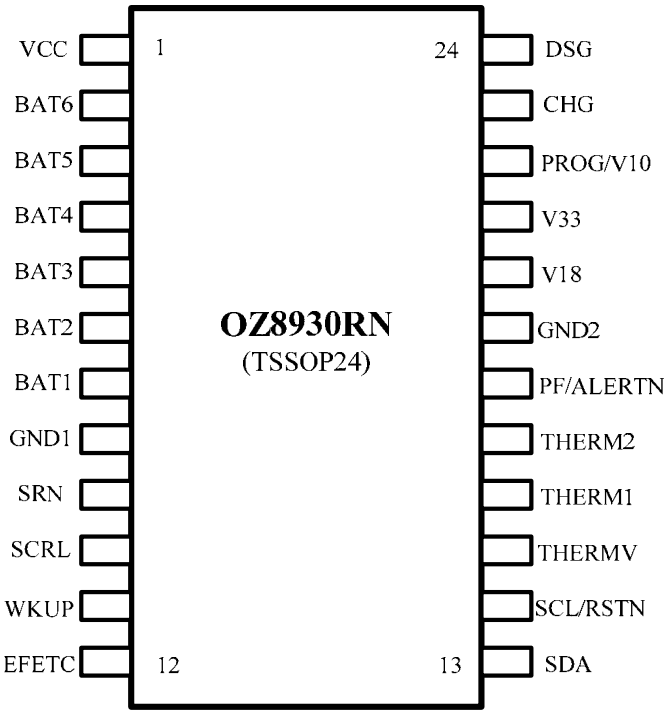
ORDERING INFORMATION

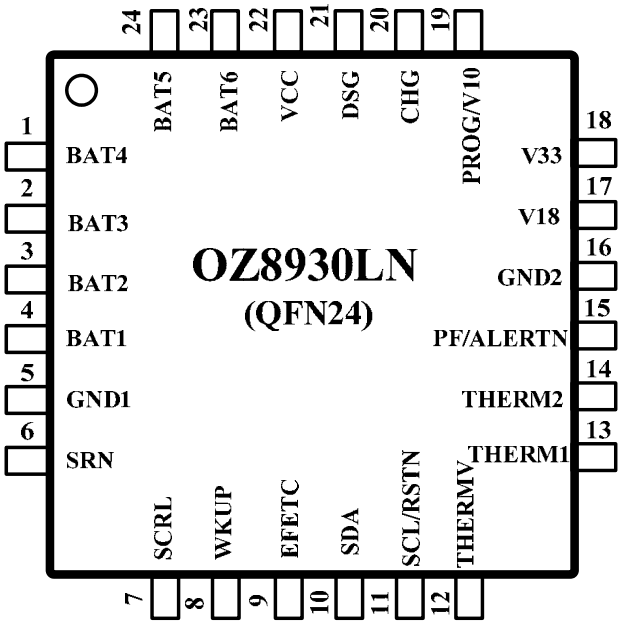
Part Number	Temp Range	Package
OZ8930RN	-40°C to 85°C	TSSOP24
OZ8930LN	-40°C to 75°C	QFN24

BLOCK DIAGRAM



PIN CONFIGURATION





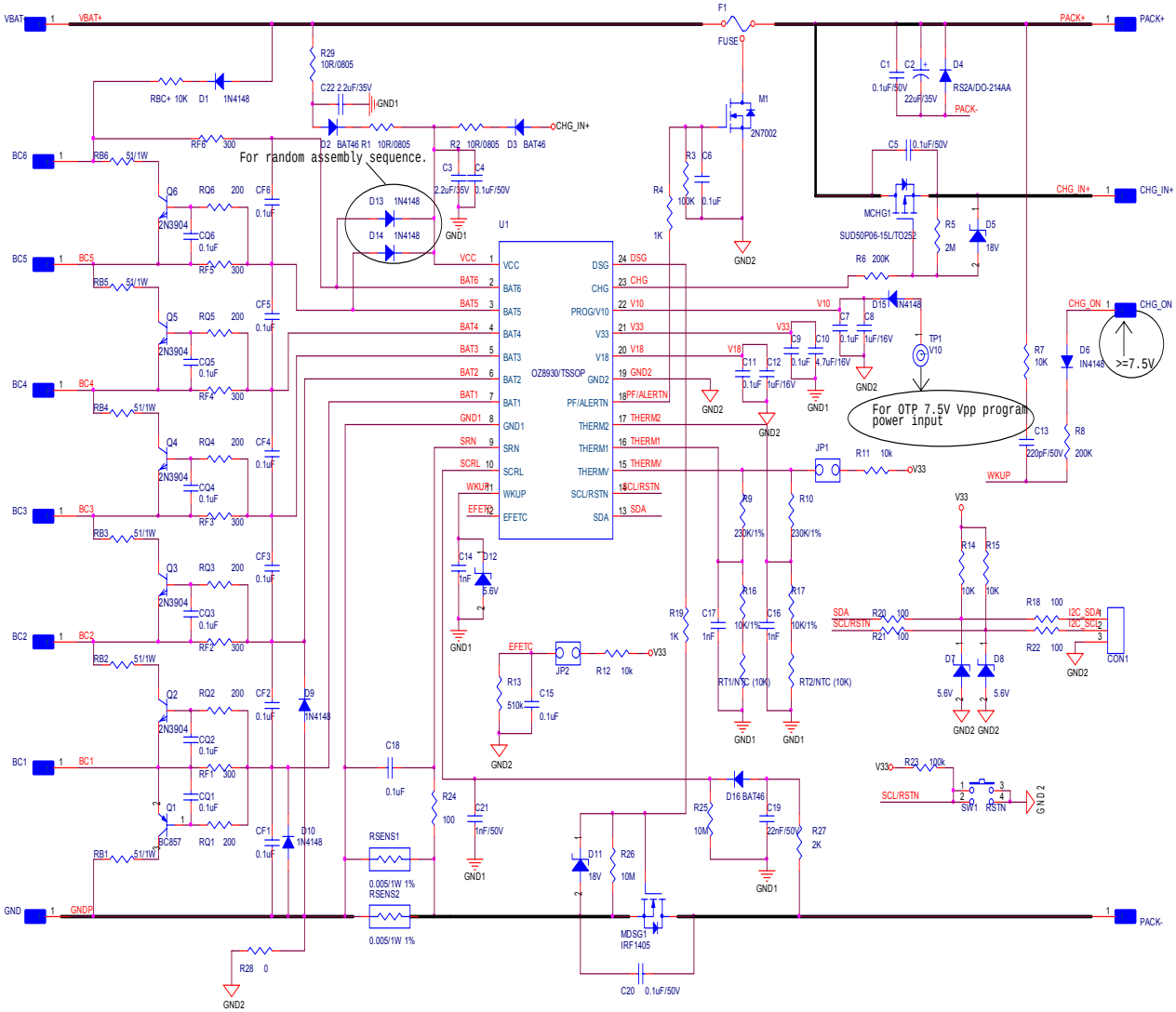
PIN DESCRIPTION

Name	Pin No. (TSSOP)	Pin No. (QFN)	I/O	Type	Description
VCC	1	22	Power	Power	Chip power supply
BAT6	2	23	I	Analog	Cell 6 positive input
BAT5	3	24	I	Analog	Cell 5 positive input
BAT4	4	1	I	Analog	Cell 4 positive input
BAT3	5	2	I	Analog	Cell 3 positive input
BAT2	6	3	I	Analog	Cell 2 positive input
BAT1	7	4	I	Analog	Cell 1 positive input
GND1	8	5	GND	Ground	Analog ground and current sense positive terminal
SRN	9	6	I	Analog	OC/SC protection, current sense and current detection negative terminal
SCRL	10	7	I	Analog	Short circuit external automatic release input
WKUP	11	8	I	Analog	External charger detection pin or analog wake up detection pin. If OZ8930 is in sleep, power down or standby mode, a positive pulse (Amplitude>3V, Width>10ms) on this pin will wake up it (charge-on wakeup). If OZ8930 is in sleep mode, a negative pulse (Amplitude>0.6V, Width>0.45us) will also wake up it. (Refer to the application note "**OZ8930 AN-8: How to use the WKUP pin?**")
EFETC	12	9	I/O	Digital	EFETC pin usage is as following: **EFETC mode** / **EFETC pin function (bit [6:4] in Operation Register 1fh)** 000 – High active input to disable charge FET. 001 – High active input to disable discharge FET. 010 – High active input to disable charge FET and discharge FET. 011 – Output discharge FET status (Open-Drain) 100 – High active input as external standby input. 101 – Output internal xx_fet_disable signal. 110, 111 – Reserved (Refer to the section "EFETC Control" in FUNCTIONAL DESCRIPTION for details)
SDA	13	10	I/O	Digital	I²C data line
SCL/RSTN	14	11	I	Digital	I²C clock line. When a low pulse with the width of 64ms or longer occurs at this pin, the chip will be reset
THERMV	15	12	O	Digital	Battery cell assembly condition: Pulling THERMV high to V33 before power on OZ8930 can disable ADC scan during battery assembly. Need to remove the pull-high after assembly. Normal condition: External thermal sensor driver voltage
THERM1	16	13	I	Digital	External Temperature Sensor1 Input
THERM2	17	14	I	Digital	External Temperature Sensor2 Input
PF/ALERTN	18	15	O	Digital	Permanent failure protection signal; Protection event alert signal
GND2	19	16	Power	Ground	Chip ground
V18	20	17	Power	Power	1.8V power supply for internal/external device
V33	21	18	Power	Power	3.3V power supply for internal/external device

PROG/V10	22	19	Power	Power	OTP external program VPP power (7.5V) in OTP programming mode; 10V regulator for internal use
CHG	23	20	O	Analog	Charge MOSFET control. CHG FET ON: Sink 5uA current CHG FET OFF: High impedance
DSG	24	21	O	Analog	Discharge MOSFET control, Push-pull structure. DSG FET ON: Drive to high level 10V DSG FET OFF: Drive to low level 0V

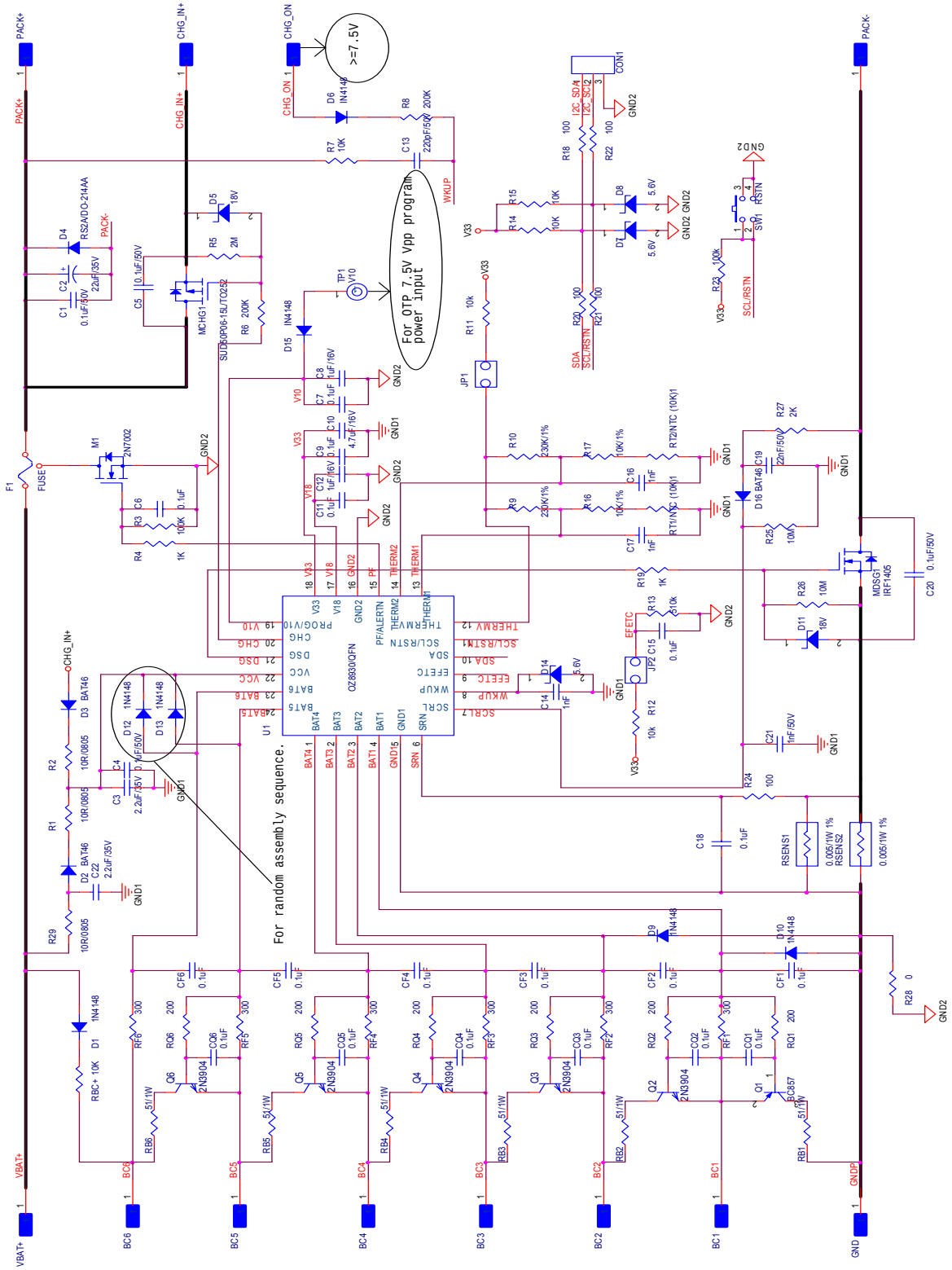
TYPICAL APPLICATION SCHEMATICS

Standalone Operation TSSOP24 package

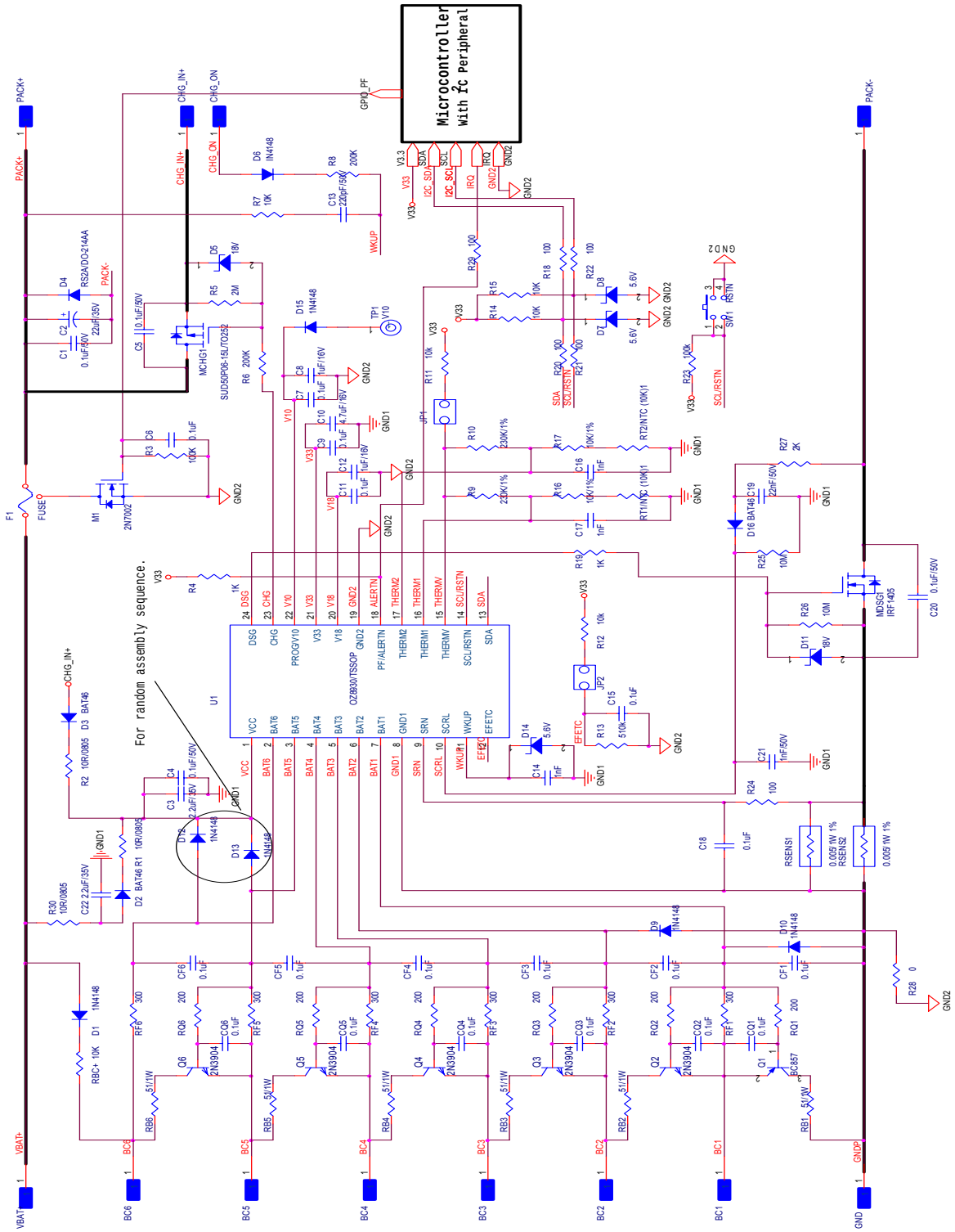


Note: The Application Note "**OZ8930 AN-3: Application circuits for 3~6 cells Li-ion battery pack and External MOSFET Driver** " describes the typical application circuits for 3S, 4S, 5S, and 6S cells Li-Ion battery pack.

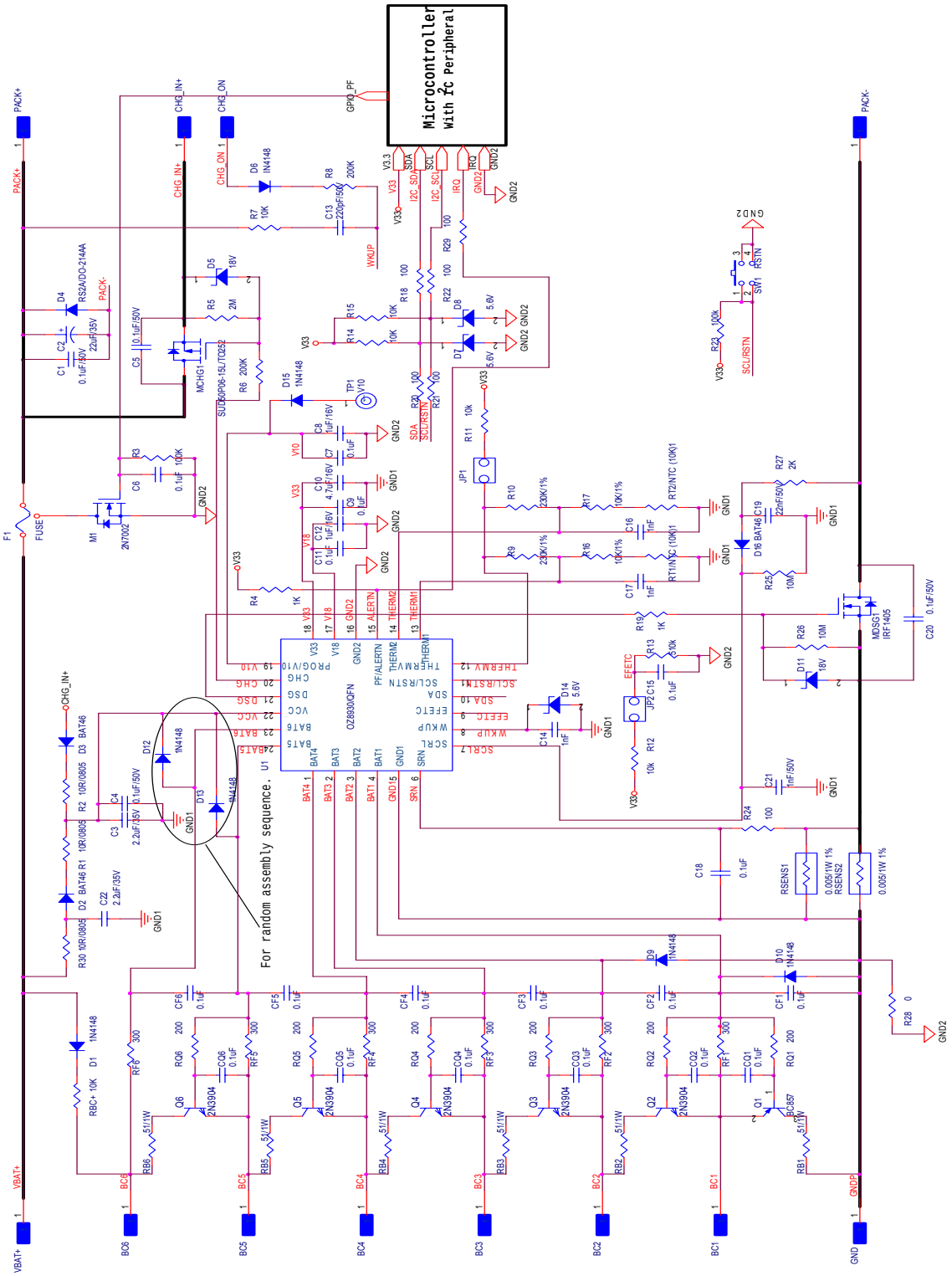
Standalone Operation QFN24 package



With MCU Operation TSSOP24 package



With MCU Operation QFN24 package



ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)

Supply voltage range		VCC	-0.3V to 32V
Input	Analog	SRN	-0.3V to 5.5V
	Analog	THERM1,THERM2	-0.3V to 5.5V
	Analog	BATn(n=1~6)	-0.3V to 32V
	Analog	BAT(n)-BAT(n-1) n=2~6, BAT1-GNDA	-0.3V to 32V
	Analog	SCRL	-0.3V to 32V
	Analog	WKUP	-0.3V to 5.5V
Output	Analog	CHG (5uA sink current)	-0.3V to 32V
	Analog	THERMV (power supply for temperature sense resistor)	-0.3V to 5.5V
	Analog	DSG	-0.3V to 32V
	Digital	PF/ALERTN	-0.3V to 5.5V
ESD Tolerance		Human Body Model (HBM)	2KV
I/O	Digital	EFETC, SDA, SCL/RSTN	-0.3V to 5.5V
Operating free-air temperature range, TA			-40℃ to 85℃
Storage temperature range, Tstg			-55℃ to 150℃
Lead temperature(soldering, 10 sec)			300℃

Note 1: All voltages are with respect to ground of this device except BATn - BAT(n-1),where n=2, 3, 4, 5, 6 cell

Note 2: Ground refers to common node of GND1, GND2

DISSIPATION RATINGS

PACKAGE	T_A≤25°C POWER RATING	DERATING FACTOR ABOVE T_A≥70°C	T_A=85°C POWER RATING	T_A=100°C POWER RATING
QFN24	1080mW	21mW/°C	842mW	526mW
TSSOP24	1333mW	25mW/°C	1000mW	625mW

RECOMMENDED OPERATING CONDITIONS

Parameter		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5		28	V
C_{REG1}	External 3.3-V regulator capacitor	2.2			μF
$I_{REGOUT1}$	External 3.3-V regulator output			30	mA
C_{REG2}	External 10-V regulator capacitor	0.47			μF
$I_{REGOUT2}$	External 10-V regulator output			5	mA
C_{REG3}	External 1.8.-V regulator capacitor	0.47			μF
$I_{REGOUT3}$	External 1.8.-V regulator output			2	mA
R_F For Internal Bleeding	Series input resistor at the BATn pin, n=2 to 6 (see **Note 1**)		100		Ω
R_F For External Bleeding	Series input resistor at the BATn pin, n=1 to 6		300		Ω
C_F	Input filter capacitor at the BATn pin, n=1 to 6		0.1		μF
f_{I^2C}	I^2C Bus Operating Frequency		100		kHz
T_{OPR}	Operating free-air temperature	-40		85	°C

Note 1: 200Ω is recommended for the series input resistor at the BAT1 pin.

ELECTRICAL CHARACTERISTICS

The test conditions are Vcc=24V, T_A=25°C, 85°C respectively; and all time units are based on the internal 512kHz oscillator and have a ±10% tolerance (unless otherwise noted)

Power Supply					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Supply Voltage (VCC)		4.5		28	V
Supply Current (I_{VCC})	Full Power Mode			380	uA
	Sleep Mode			45	uA
	Standby Mode			10	uA
	Power Down			1	uA

Digital Inputs And Outputs					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
VIH High-level Input Voltage		2			V
VIL Low-level Input Voltage				0.8	V
VOH Output Voltage High	I_{Load}=-0.5mA	V3.3-0.5			V
VOL Output Voltage Low	I_{Load}=0.5mA			0.3	V
Current Drive Capability			2		mA

3.3V LDO Regulator					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Regulator Output Voltage (Full power mode)	I_{Load}<30mA, 6V<Vcc<28V	2.97	3.3	3.63	V

Parameter	Test Conditions	MIN	TYP	MAX	Unit
Line Regulation (Full power mode)	I_{Load}=13mA, 6V<Vcc<28V		10	30	mV
Load Regulation (Full power mode)	0.2mA<I_{load}<30mA Vcc=16V		15	60	mV
3.3V Current Limit (Full power mode)	6V<Vcc<28V			30	mA
Regulator Output Voltage (In Sleep Mode and Standby Mode)	I_{Load}<150µA, 6V<Vcc<28V	2.8	3.3		V
Current Limit (In Sleep Mode and Standby Mode)	6V<Vcc<28V			150	µA

1.8V LDO Regulator					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Regulator Output Voltage (Full power mode)	I_{Load}<2mA, 6V<Vcc<28V	1.62	1.8	1.98	V
Line Regulation (Full power mode)	I_{Load}=2mA, 6V<Vcc<28V		5	20	mV
Load Regulation (Full power mode)	0<I_{load}<2mA Vcc=16V		5	30	mV
1.8V Current Limit (Full power mode)	6V<Vcc<28V			2	mA
Regulator Output Voltage (In Sleep Mode and Standby Mode)	I_{Load}<20µA, 6V<Vcc<28V	1.62	1.8		V
Current Limit (In Sleep Mode and Standby Mode)	6V<Vcc<28V			20	µA

10V LDO Regulator					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Regulator Output Voltage (Full power mode)	I_{Load}<5mA, 10V<Vcc<28V	8.5	10	11.5	V
Line Regulation (Full power mode)	I_{Load}=3mA, 12V<Vcc<28V		5	30	mV
Load Regulation (Full power mode)	0<I_{load}<5mA, Vcc=16V		15	80	mV
10V Current Limit (Full power mode)	10V<Vcc<28V			5	mA
Regulator Output Voltage (In Sleep Mode)	I_{Load}<50µA, 10V<Vcc<28V	8.5	10		V
Current Limit (In Sleep Mode)	10V<Vcc<28V			50	µA

Multi-Channel ADC						
Parameter		**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Current Channel (1 channel)	Input Voltage Range		-125		125	mV
	Resolution			14 bits		
	Conversion Time				16	ms
	Offset		Auto offset cancellation			
	Slope		In operation with MCU, support slope calibration			

Multi-Channel ADC						
Parameter		**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Voltage Channel (6 channels)	Input Voltage Range		-0.3		5	V
	Resolution			12 bits		
	Conversion Time				4.27	ms
	Offset		Auto offset cancellation			
	Slope		In operation with MCU, support slope calibration			
Internal Temperature (1 channel)	Input Voltage Range		0.1		2.5	V
	Resolution			12 bits		
	Conversion Time				4.27	ms
	Offset		Auto offset cancellation			
	Slope		In operation with MCU, support slope calibration			
THERM1, THERM2	Input Voltage Range		0.1		2.5	V
	Resolution			12 bits		
	Conversion Time				4.27	ms
	Offset		Auto offset cancellation			
	Slope		In operation with MCU, support slope calibration			

Internal Oscillator					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
512kHz Oscillator Frequency		460.8	512	563.2	KHz

Over-Current(OC) And Short-Circuit(SC) Protection (Note 1)				
Parameter	**Test Conditions**	**MIN**	**MAX**	**Unit**
COC Detection Threshold Range (4-bit setup); Support Low/Standard/High temperature range		2	80	mV
COC Hysteresis Value		N/A		
COC Delay Time (2-bit setup)		2	8	Scan Cycle (**Note 2**)
COC Detection Threshold Step		Programmable		**(Note 3)**
COC Release Time (2-bit setup)		1	8	s
DOC0 Detection Threshold Range (6-bit setup); Cover all temperature range		-285	-30	mV
DOC0 Detection Threshold Step		5		mV
DOC0 Hysteresis Value		20		mV
DOC0 accuracy	DOC0 <80mV		3.5	mV
DOC0 Delay Time (4-bit setup)		2	16000	ms
DOC0 Release Time (2-bit setup)		1	4	s

Parameter	Test Conditions	MIN	MAX	Unit
DOC1 Detection Threshold Range (6-bit setup); Cover all temperature range		-620	-50	mV
DOC1 Detection Threshold Step		10		mV
DOC1 Hysteresis Value		30		mV
DOC1 accuracy	DOC1 < 80mV		7.5	mV
DOC1 Delay Time (4-bit setup)		32	256000	ms
DOC1 Release Time (2-bit setup)		4	16	s
SC Detection Threshold Range		Pack- voltage higher than system ground 0.95V±0.3V; Not programmable		
SC Hysteresis Value		N/A		
SC Delay Time (2-bit setup)		0	1	ms
SC Release Time (2-bit setup)		8	32	s

Note 1: When DOC0/DOC1 thresholds are larger than 80mV, the error is +/- 4%.
Note 2: In current measurement mode, the scan cycle will be 55ms; In non-current measurement mode, the scan cycle will be 39ms.
Note 3: Refer to the Over-current (OC) section.

Over-Voltage(OV) And Under-Voltage(UV) Protection					
Parameter	**Test Condition**	**MIN**	**TYP**	**MAX**	**Unit/step**
OV Detection Threshold Value; Support Low/Standard/High temperature range		12bits programmable (0-5V)			V
OV Release Value (6-bit setup)		OV Threshold - 312.3mV		OV Threshold	
OV Delay Time (2-bit setup)		2		16	Scan Cycle
OV Release Time		same as OV delay time			
UV Detection Threshold Value		12bits programmable (0-5V)			V
UV Release Value (6-bit setup)		UV Threshold		UV Threshold + 1210mV	
UV Delay Time (2-bit setup)		2		16	Scan Cycle
UV Release Time		same as UV delay time			Scan Cycle

Cell Voltage Unbalance (UB) Protection					
Parameter	**Test Condition**	**MIN**	**TYP**	**MAX**	**Unit/step**
UB Detection Threshold Value		12bits programmable (0-5V)			V
UB Release Value (4-bit setup)		UB Threshold - 312.3mV		UB Threshold	
UB Delay Time (2-bit setup)		2		8	Scan Cycle
UB Release Time		same as UB delay time			Scan Cycle

Permanent failure (OVPF, CELL_OTPF, FET_OTPF, INT_OTPF, ADC_PF) Protection					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**units/step**
OVPF Threshold Range		100mV larger than OV Threshold according to Low/Standard/High temperature range respectively			
OVPF Delay Time (Not programmable)			8		Scan Cycle
CELL_OTPF Threshold Range			12bits programmable		**(Note 1)**
CELL_OTPF Delay Time (Not programmable)			8		Scan Cycle
FET_OTPF Threshold Range			12bits programmable		**(Note 1)**
FET_OTPF Delay Time (Not programmable)			8		Scan Cycle
INT_OTPF Threshold Range			12bits programmable		1°C /2.1mV
INT_OTPF Delay Time (Not programmable)			8		Scan Cycle
ADC_PF Threshold Range			**(Note 2)**		
ADC_PF Delay Time			**(Note 2)**		

Note 1: Depends on external temperature sensor characteristics, refer to the section External Temperature Sensor.
Note 2: Refer to the section Permanent failure (PF).

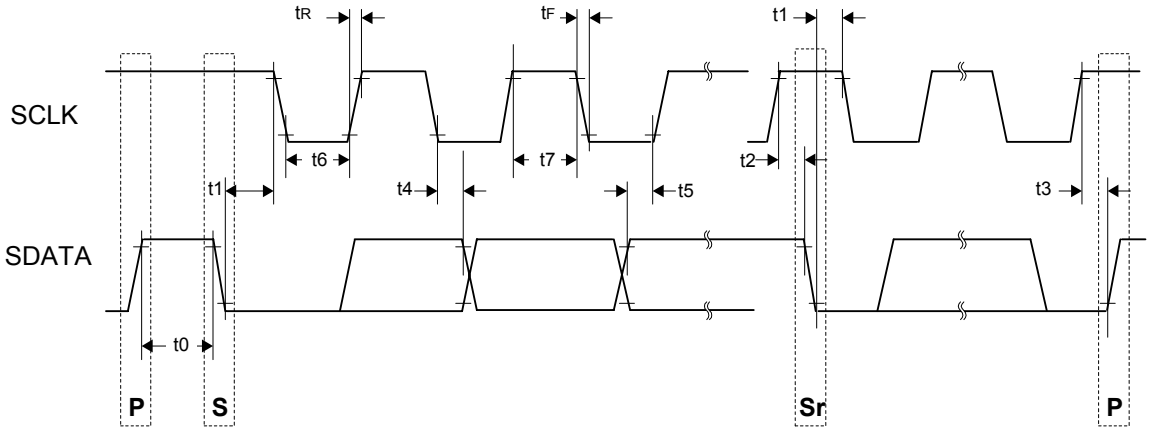
External Thermal Protection (OT & UT)					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit/Step**
OT Detection Threshold value	Charge	12bits Programmable			**(Note1)**
	Discharge	12bits Programmable			
OT Detection release Range	Charge	4bits Programmable; **(Note 1)**			**(Note1)**
	Discharge	4bits Programmable; **(Note 1)**			
OT Delay Time (2-bit setup)		2		8	Scan Cycle
OT Release Time		same as OT delay time			
UT Detection Threshold Value		12bits Programmable			**(Note 2)**
UT Detection Release Value		12bits Programmable			**(Note 2)**
UT Delay Time		same as OT delay time			
UT Release Time		same as OT delay time			

Note 1: Refer to the section Thermal Protection (OT and UT).
Note 2: Depends on external temperature sensor characteristics, refer to the section External Temperature Sensor.

Power MOSFET Driver Circuit					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
CHG on, sink current (constant current source)			5		uA
CHG off, no sink current (high impedance)			0		uA
DSG high level		8.5	10	11.5	V
DSG low level		0		0.5	V

AC TIMING

I²C Bus Timing



Symbol	Parameter	Limits		Units	Note
		Min	Max		
FSMB	I²C Bus Operating Frequency	10	400	KHz	
t0	Bus free time between Stop and Start condition	1.3	-	µs	
t1	Hold time after (Repeated) Start condition. After this period, the first clock is generated	0.6	-	µs	
t2	Repeated Start condition set up time	0.6	--	µs	
t3	Stop Condition setup time	0.6	-	µs	
t4	Data hold time	150	-	ns	
t5	Data setup time	100	-	ns	
TIMOUT		25	35	ms	See **Note 1**
t6	Clock low period	1.3	-	µs	
t7	Clock high period	0.6		µs	
tF	Clock/Data Fall time	-	300	ns	See **Note 2**
tR	Clock/Data Rise Time	-	300	ns	See **Note 2**

Note 1: A device will be timeout when any clock low duration exceeds this value.
Note 2: Rise and Fall times are measured between 10% and 90% of the signal amplitude.

FUNCTIONAL DESCRIPTION

OZ8930 Power-Up Sequence

Fig.1 shows the OZ8930 power up sequence. When power supply is applied to VCC>4.5V, the common bias starts first, followed by 1.8V, 3.3V and 10V regulators. When V3.3>2.4V, the power on reset block generates POR signal to enable the 512K oscillator and initializes the digital section. When power and clock are ready, the digital circuits will read the pin configuration and OTP data, which in turn determines the working state.

If ADC scan conditions are satisfied, OZ8930 will start the ADC scan and work in full power mode, otherwise OZ8930 will stay in the assembly state.

When VCC is lower than 4.5V, OZ8930 is in power off status. All Regulators (V1.8, V3.3 and V10) are disabled and all MOSFETs are off.

Reset Generation

In OZ8930, there are 3 system reset methods: one is power on reset when V3.3>2.4V; the second reset is generated when the bits in Operation Register 13h don't meet the parity check requirement. The third reset is generated when the voltage level on pin SCL/RSTN is low and persists for 64ms. MCU or software utility can reset OZ8930 by simply writing Operation Register 13h of OZ8930 with a binary value which doesn't meet the parity check requirement.

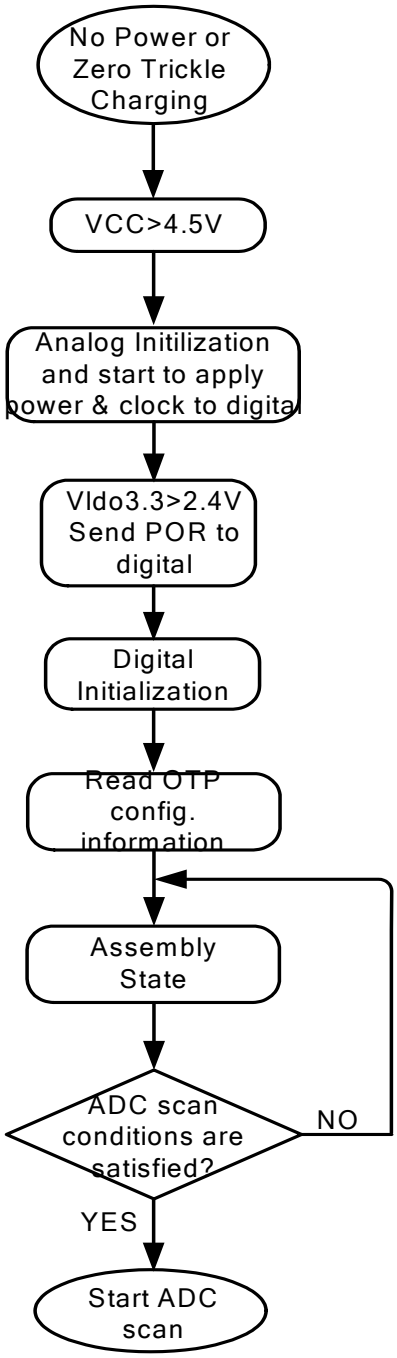


Figure 1: OZ8930 Power-Up Sequence

OTP and Operation Registers

OZ8930 has two types of registers. One type is Operation Registers, the other type is embedded OTP (One-Time-Programmable) Registers. Software can directly access OZ8930's Operation Registers via I²C bus, and access the OTP Registers indirectly through Operation Registers.

OTP Registers are used to store important battery pack, battery cell protection parameters which are used to configure the OZ8930 chip. When system is powered on, some of the data in OTP Registers are loaded into the Operation Registers respectively. Operation Registers are also used to store the ADC instant data, OZ8930 status information, and some parameters to control OZ8930 state-machine, etc. In the software mode, the Host MCU can also configure the chip by writing the Operation Registers through I²C.

Measurements

OZ8930's multi-channel ADC (as shown in Figure 2) measures up to 6 cells' voltages, current, internal temperature and external temperature based on cyclic scan and time slot method. It can periodically measure all these values by predefined scan rate or use trigger scan function by setting the register bit through the I²C. In one measurement period, cell voltages, current, temperatures etc will be measured one by one in different time slot.

ADC Scan Operation

There are two ADC scan modes: current measurement mode and non-current measurement mode, which can be programmed by **currt_scan** (bit 4 of OTP Register 13h, mapped to Operation Registers).

- Current measurement mode
  - 6 channels cell voltage measurement
  - 1 channel internal temperature measurement
  - 2 channels external temperature measurement
  - 1 channel current measurement (14 bits)
  - Maximum scan cycle time: 55ms
- Non-current measurement mode
  - 6 channels cell voltage measurement
  - 1 channel internal temperature measurement
  - 2 channels external temperature measurement
  - Maximum scan cycle time: 39ms

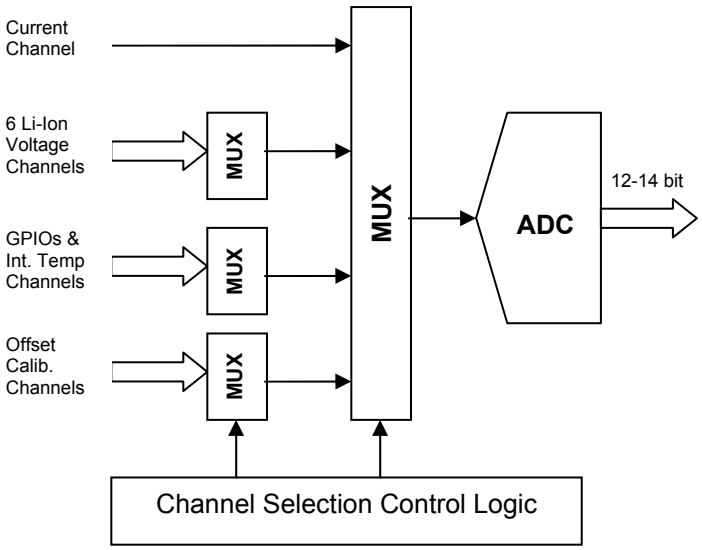


Figure 2: Multi-Channel ADC

ADC Channel Description

a. Cell Voltage Channel (3~6 channels)

These channels are designed for cell voltage measurement.
Resolution: 12bits (signed)
Input Voltage Range: -0.3V~5.0V
Auto offset cancellation
Slope calibration can be implemented in software mode for better accuracy.

b. Internal Temperature (1 channel)

This channel is designed for internal temperature sensor.
Resolution: 12bits (signed)
Input Voltage Range: 0.1V~2.5V
Auto offset cancellation
Slope calibration can be implemented in software mode for better accuracy.

c. GPIO Channel (2 channels)

GPIO Pin THERM1 and THERM2 can be configured for external temperature sensors or other analog input in software mode.
Resolution: 12bits (signed)
Input Voltage Range: 0.1V~2.5V
Auto offset cancellation
Slope calibration can be implemented in software mode for better accuracy.

d. Current measurement channel

This is a dedicated channel to measure the current across the sense resistor during charging and discharging for charge over current detection, coulomb counting or other purpose.
Resolution: 14-bit (signed)
Input Voltage Range: ± 125mV (LSB: 15.3μV)
Auto offset cancellation
Slope calibration can be implemented in software mode for better accuracy.

Note: Please refer to the application note "**OZ8930 AN-6: Resolution and Accuracy of OZ8930 Cell Voltage, Current and Temperature Measurement and accuracy of OC/SC Protection**" for offset cancellation technique and high accuracy measurement.

ADC Self-Diagnostic

OZ8930 will do ADC self-diagnostic in the 1st scan cycle after reset; it also will do ADC self-diagnostic in the 4th scan cycle after wakeup by 1min/4min sleep timer. In the ADC self-diagnostic cycle, the following ADC channels will be checked.

- cell1 offset (12-bit ADC)
- cell2 offset (12-bit ADC)
- cell3 offset (12-bit ADC)
- cell4 offset (12-bit ADC)
- cell5 offset (12-bit ADC)
- cell6 offset (12-bit ADC)
- cell6 high-side offset (12-bit ADC)
- TM1 offset (12-bit ADC)
- TM2 offset (12-bit ADC)
- current offset (14-bit ADC)
- reference 1.8v (12-bit ADC) (It is for digital power and fully independent with ADC voltage reference)

The offset detection path includes MUX switches, level shift and buffer blocks, the ADC block and reference voltage. The ideal offset value should be "0", however, if some fatal error occurs at the real signal path, big offset will happen. OZ8930 will accept the offset errors as listed below.

- between -100mV and 100mV for cell voltage offset
- between -100mV and +100mV for TM1 and TM2 offset
- between -20mV and 20mV for current offset

- between -200mV and 200mV for reference 1.8V

That is, during ADC self-diagnostic cycle, if either cell voltage offset exceed +/-100mV, AND/OR TM1, TM2 offset exceed +/- 100mV, AND/OR 1.8V reference reading's error exceed +/- 200mV (less than 1600mV or larger than 2000mV), AND/OR current offset exceed +/-20mV, OZ8930 will treat the ADC as abnormal and the internal ADC_PF counter will increase by one. If in next ADC self-diagnostic cycle, any abnormal condition of ADC also occurs, the internal ADC_PF counter will increase by one again. Else, the internal ADC_PF counter will be cleared. Not until the internal ADC_PF counter reaches the predefined value in the ADC_PF delay timer (bit [2:0] of OTP Register 1dh, customer can disable the ADC self-diagnostic (000), or programmed as 2 ~ 8 times delay count), will OZ8930 issue an ALERTN to external MCU, and then enter into standby mode. (Refer to the application note "**OZ8930 AN-9: OZ8930 ADC self-diagnostic mechanism**")

ADC Automatic Scan and Trigger Scan function

OZ8930 has two ADC scan methods selected by **auto_scan** (bit 5 of OTP Register 13h, mapped to Operation Registers). When **auto_scan** = "1", OZ8930 selects auto scan in which ADC scan is automatically processed each scan cycle; when **auto_scan** = "0", selects trigger scan in which ADC scan is processed one time triggered by writing "1" into **soft_scan_req** (bit 5 of Operation Register 01h) when **soft_enable** (bit 7 of Operation Register 08h) is "1". To enable the ADC scan, OZ8930 needs to meet the following conditions:

(a) Not in OTP mode
In OTP mode, the ADC scan is disabled for software OTP access .

(b) Auto_Scan bit = "1"
When ***auto_scan = "1"***, OZ8930 selects auto scan mode; when ***auto_scan = "0"***, select trigger scan mode

(c) User_freeze ((bit 7 of OTP Register 1fh, mapped to Operation Register) = "1")
When user_freeze is "1" indicating the user parameters are ready, the ADC scan is enabled.

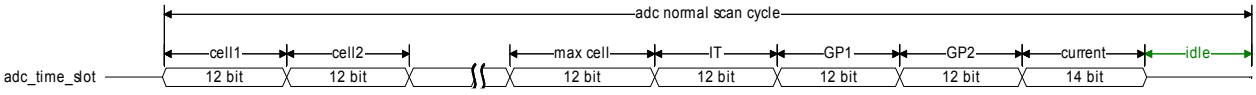
(d) **Input voltage level of pin THERMV != "1" for 16-clocks (256 kHz)**
To avoid unexpected protection error, it is needed to disable the ADC scan in battery assembly by keeping THERMV as "1". After battery assembly, the ADC scan can be started by driving "0" on pin THERMV.

OZ8930 provides 2 solutions to avoid unexpected protection error during battery assembly:

- Disable ADC scan in battery assembly. This can be implemented by pulling the pin THERMV to V33 before power on OZ8930. After getting power, OZ8930 will detect the voltage level at the pin THERMV before starting ADC scan. If it is "1", OZ8930 will not start ADC scan.
- Provide a PF delay mechanism in the assembly. To avoid unexpected OVPF detection in battery assembly, the OVPF detection will be ignored for 32 or 64 seconds (selected by bit 3 of OTP Register 1dh) after power on reset.

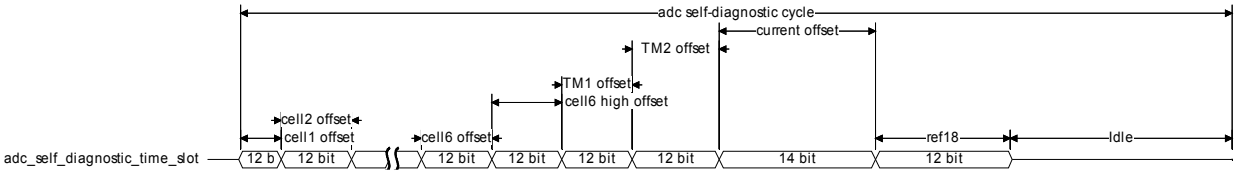
Time Slots Configuration

ADC Normal Scan Time Slot



Note 1: the time slot's length is not in scale.
Note 2: max cell can be cell3, cell4, cell5 or cell6.
Note 3: IT indicates 12-bit internal temperature channel.
Note 4: GP1 indicates 12-bit THERM1 channel; GP2 indicates 12-bit THERM2 channel.
Note 5: THERM1, THERM2 and current channel are optional (Configured in OTP Registers). When any one of them is not used, the time slot for it will be removed. However, the idle time slot will be increased accordingly to keep the ADC scan cycle to be about 39ms (Non-current measurement mode) or 55ms (current measurement mode).

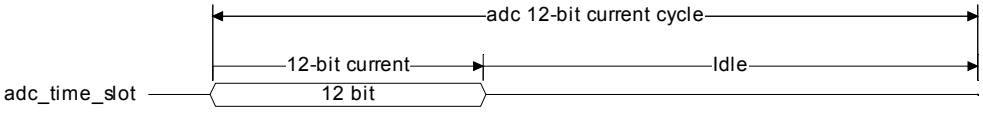
ADC Self-Diagnostic Time Slot



Note 1: in ADC self-diagnostic cycle, the time slots for THERM1, THERM2 and current channel always exist, no matter whether the channels are used. The sampled current signal is the internal 0v voltage level, and the sampled temperature signals is still THERM1 and THERM2 (THERMV is 0v at this moment).

ADC 12-bit Current Time Slot

After entering sleep mode, OZ8930 will wakeup by 2-s current measurement timer to check the current charge/discharge state by checking 12-bit current ADC value (It is noted that the 12-bit data will be left shifted 2 bit to store into the 14-bit current ADC register, so the LSB still is the same as the one of 14-bit ADC current data). If the charge current or discharge current (the thresholds are same as the ones in the full power mode) is detected, the chip will be woken up and kept in full power mode. The time slot for 12-bit current ADC is as following:



Cell Balance

OZ8930 has integrated internal bleeding function for cell balance. Bleeding occurs during charging process or in idle state and the start bleeding voltage point is programmable (12 bits in OTP Registers 3ch and 3dh), the bleeding current is around 15mA. This function can also be used to support external bleeding by adding some extra components (Figure 3). Balance accuracy can be configured within the range 9.76mV~39mV (2 bits in bit [1:0] of OTP Register 1eh). Please refer to the application note "**OZ8930 AN-4: External Bleeding Application**" for detail of external bleeding.

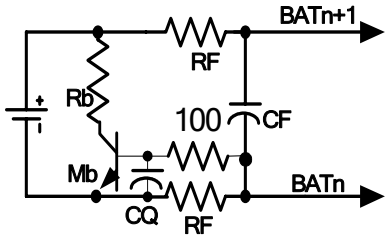
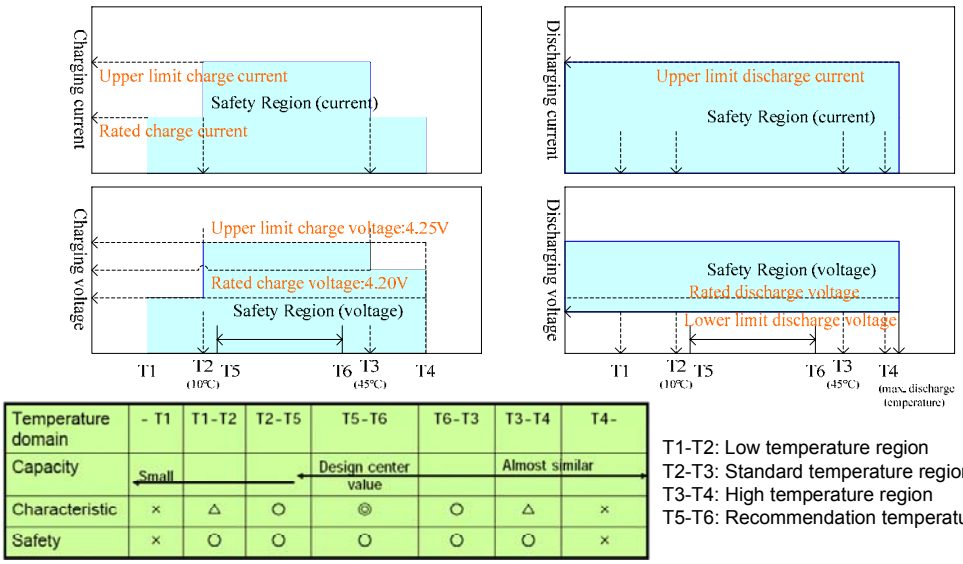


Fig.3 External Bleeding Diagram

Battery Protection

OZ8930 includes a digital Battery Protection Engine (BPE), which can operate independently. The BPE constantly monitors data from the ADC and other protection circuits. If a protection error condition is detected and persists for certain time, the BPE will force the charge and/or discharge MOSFET off. The protection mechanism is to support the requirement of JEITA (Figure 4). If some vital safety condition occurs, such as extremely high cell voltage (OVPF), the BPE will assert the Permanent failure (PF) signal to instruct an optional external fuse circuit to permanently disable the battery pack. If working with MCU, OZ8930 provides an exclusive pin ALERTN to inform MCU while switching off the protection power MOSFET when error condition happens.



Temperature domain	- T1	T1-T2	T2-T5	T5-T6	T6-T3	T3-T4	T4-
Capacity	Small			Design center value		Almost similar	
Characteristic	×	△	○	◎	○	△	×
Safety	×	○	○	○	○	○	×

T1-T2: Low temperature region
T2-T3: Standard temperature region
T3-T4: High temperature region
T5-T6: Recommendation temperature region

Source: A Guide to the Safe Use of Secondary Lithium Ion Batteries in Notebook-type Personal Computers
April 20, 2007 (Japan Electronics and Information Technology Industries Association And Battery Association of Japan.)

Fig.4 JEITA Safety Battery User Guideline

Parameter	Description	Value
JEITA Protection	**JEITA Protection Parameter**	
T1MinChgTemp	JEITA T1 Minimum Temperature Allowed threshold of Low Temperature Range	12 bits setting (OTP Registers 20h, 21h)
T2StdChgTemp	JEITA T2 Starting Temperature point of Standard Temperature Range	12 bits setting (OTP Registers 24h, 25h)
T3MaxChgStartTemp	JEITA T3 Maximum Temperature point of Standard Temperature Range	12 bits setting (OTP Registers 26h, 27h)
T4MaxChgTemp	JEITA T4 Maximum Temperature Charging point of High Temperature Range	12 bits setting (OTP Registers 28h, 29h)
HighTempChgOV	Charge OV Voltage protection threshold in high Temperature Range (T3-T4)	12 bits setting (OTP Registers 30h, 31h)
StdTempChgOV	Charge OV Voltage protection threshold in standard Temperature Range (T2-T3)	12 bits setting (OTP Registers 2eh, 2fh)
LowTempChgOV	Charge OV Voltage protection threshold in low Temperature Range (T1-T2)	12 bits setting (OTP Registers 2ch, 2dh)
HighTempChgOC	Charge OC Current protection threshold in high Temperature Range (T3-T4)	0-80mV/Rs, 4 bits setting (bit [7:4] of OTP Registers 16h)
StdTempChgOC	Charge OC Current protection threshold in standard Temperature Range (T2-T3)	0-80mV/Rs, 4 bits setting (bit [7:4] of OTP Registers 15h)
LowTempChgOC	Charge OC Current protection threshold in low Temperature Range (T1-T2)	0-80mV/Rs, 4 bits setting (bit [3:0] of OTP Registers 15h)
CellUV	Discharge UV Voltage protection threshold in all temperature range	12 bits setting (OTP Registers 34h, 35h)
DsgOC	Discharge OC Current protection threshold in all temperature range	3 levels Discharge Over-Current protection (DOC0, DOC1 and SC)
DsgOT	Discharge Over Temperature protection threshold	12 bits setting (OTP Registers 2ah, 2bh)

Over-current (OC)

OZ8930 includes two levels of discharge over-current protection and one level of charge over-current protection. OZ8930 also embeds SC protection function as the third level discharge over-current protection.

OC Protection Setting

OZ8930 includes an independent hardware over-current detector that monitors the voltage drop on the current sense resistor to detect over-current in discharge state. In charge state, OZ8930 uses the measured current value from ADC to compare with the pre-defined threshold, and then decide if over-current occurs. If the over-current condition continues for a pre-programmed delay, the protection circuit will turn off the charge and discharge MOSFETs.

The charge and discharge over-current thresholds are programmable in OTP registers. The over-current delay allows the system to momentarily accept a high current condition. The delay time is also programmable.

OC Value	COC	• Support COC protection in Low/Standard/High temperature range respectively to meet JEITA requirement • 4 bits setting (**Note 1**)
	DOC0	OTP Control. Min: 30mV; Max: 285mV; Step: 5mV; Cover all temperature range
	DOC1	OTP Control. Min: 50mV; Max: 620mV; Step: 10mV ; Cover all temperature range
Hyst. Value	COC	N/A
	DOC0	10mV
	DOC1	20mV
Delay Time	COC	2 bits delay time setting (bit [1:0] of OTP Register 16h): 2, 4, 6, 8 scan cycles
	DOC0	4 bits delay time setting (bit [3:0] of OTP Register 18h) with the range of 2ms-16s
	DOC1	4 bits delay time setting (bit [3:0] of OTP Register 1ah) with the range of 32us-256ms
Release	COC	2 bits timer release control (bit [3:2] of OTP Register 16h). 00: 1s; 01: 2s; 10: 4s; 11: 8s
	DOC0	2 bits control (bit [5:4] of OTP Register 18h). 00: external release; 01: 1s; 10: 2s; 11: 4s
	DOC1	2 bits control (bit [5:4] of OTP Register 1ah). 00: external release; 01: 4s; 10: 8s; 11: 16s

Note 1: the COC threshold can be set as the following table:

4-bit COC threshold setting	charge over current threshold
4'b0000	2mV (0.8A@2.5mohm)
4'b0001	4mV (1.6A@2.5mohm)
4'b0010	6mV (2.4A@2.5mohm)
4'b0011	8mV (3.2A@2.5mohm)
4'b0100	10mV (4.0A@2.5mohm)
4'b0101	12mV (4.8A@2.5mohm)
4'b0110	16mV (6.4A@2.5mohm)
4'b0111	20mV (8.0A@2.5mohm)
4'b1000	24mV (9.6A@2.5mohm)
4'b1001	28mV (11.2A@2.5mohm)
4'b1010	32mV (12.8A@2.5mohm)
4'b1011	40mV (16A@2.5mohm)
4'b1100	48mV (19.2A@2.5mohm)
4'b1101	56mV (22.4A@2.5mohm)
4'b1110	64mV (25.6A@2.5mohm)
4'b1111	80mV (32A@2.5mohm)

Short-circuit (SC)

Short circuit detection is to independently sense the PACK- voltage when discharge MOSFET is on. When short circuit condition is detected, OZ8930 will turn off charge and discharge MOSFETs. Short circuit delay time and release time are programmable.

SC threshold	Pack- voltage higher than system ground 0.95V±300mV
Hysteresis Value	N/A
Delay Time	2 bits control (bit [1:0] of OTP Register 1bh). ”00”: 0, immediately (nature delay); “01”: 128us; “10”: 512us; “11”: 1ms
Release	2 bits control (bit [3:2] of OTP Register 1bh). “00”: external release; “01”: 8s; “10”:16s; “11”: 32s

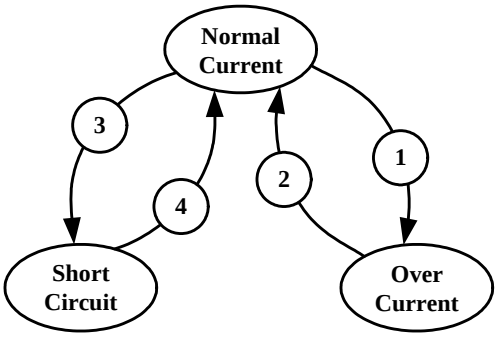


Fig.5 Current Protection Chart

Transition	Initial State	Condition & Action	Final State
1	Normal Current	• OC event occurs (charge or discharge current ≥ respective OC threshold & delay timer expires); • Switch off charge and discharge FETs; • Start release timer if timer release is chosen; • Timer release circuit or external release circuit starts to work	Over Current
2	Over Current	• DOC0/DOC1: release timer expires or external release condition is satisfied; • COC: release timer expires; • Switch on charge and discharge FETs if no other protection events occur	Normal Current
3	Normal Current	• SC event occurs (PACK- voltage is higher than the threshold & delay timer expires); • Switch off charge and discharge FETs; • Start release timer if timer release is chosen; • Timer release circuit or external release circuit starts to work	Short Circuit
4	Short Circuit	• Release timer expires or external release condition is satisfied; • Switch on charge & discharge FETs if no other protection events occur;	Normal Current

Over-voltage (OV)

The protection engine performs over-voltage detection by comparing 12 bits values of cell voltage data from the ADC with an OV threshold, which is programmable in OTP. When over-voltage condition is detected, OZ8930 will turn off the charge FET after a delay time. This delay time is programmable in OTP.

OV Threshold	Support OV protection in Low/Standard/High temperature range respectively (12 bits)
OV Delay Time	2 bits control: 2, 4, 8, 16 scan cycles (bit [1:0] of OTP Register 1ch)
Release Value	OV release = ov_threshold+ov_hys*4; ov_hys is controlled by 6 bits (bit [5:0] of OTP Register 3eh), 1 LSB=2.44*4mV; theoretical range: -312.3mV ~ +302.56mV, application range: -312.3mV ~ 0mV
Release Delay Time	Same as OV delay time

Under-voltage (UV)

Under-voltage detection operates in the same way as over-voltage detection. Its threshold also can be programmed in OTP.

UV Threshold	12 bits
UV Delay Time	2 bits control: 2, 4, 8, 16 scan cycles (bit [7:6] of OTP Register 1dh)
Release Value	UV release = uv_threshold+uv_hys*16; uv_hys is controlled by 6 bits (bit [5:0] of OTP Register 3fh), 1 LSB=2.44*16mV; theoretical range: -1249mV ~ +1210mV, application range: 0 ~ +1210mV
Release Delay Time	Same as UV delay time

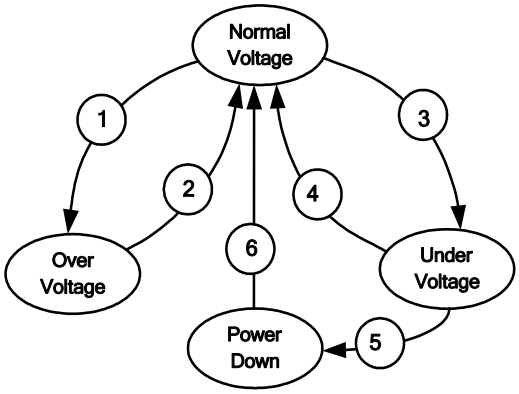


Fig.6 Voltage Protection Chart

Transition	Initial State	Condition & Action	Final State
1	Normal Voltage	• OV event occurs ($V_{CELL} \geq$ OV threshold & delay timer expires); • Switch off charge FET	Over Voltage
2	Over Voltage	• OV event clears ($V_{CELL} \leq$ OV release voltage and delay timer expires); • Switch on charge FET if no other protection events occur	Normal Voltage
3	Normal Voltage	• UV event occurs ($V_{CELL} \leq$ UV threshold & delay timer expires); • Switch off discharge FET • Start up the charger detection function	Under Voltage
4	Under Voltage	• UV event clears ($V_{CELL} \geq$ UV release voltage and delay timer expires); • Charge on signal detected • Switch on discharge FET if no other protection events occur	Normal Voltage
5	Under Voltage	• Stay in Under Voltage state for 1 minute AND no Charge on signal AND no charge current • Switch off charge and discharge FET	Power Down
6	Power Down	• Charge on signal detected • Switch on charge and discharge FET if no other protection events occur	Normal Voltage

When UV happens, it is required that the power consumption of OZ8930 is reduced to be the least to protect battery cells from extremely over-discharge. So OZ8930 will enter Power Down Mode if the following condition is satisfied.

- In UV state and persists for 1 minute

- ***AND*** No charge on signal
- ***AND*** No charge current

Cell voltage Unbalance (UB)

When voltage difference between cells is larger than the preset value (12 bits programmable in OTP Registers 32h, 33h) for a predefined delay time (bit [5:4] in OTP Register 1ch), OZ8930 will turn off the charge and discharge MOSFET. This function can be used to detect the fault of the cell voltage sense wire disconnection. When one or more cells' wires are disconnected, the sensed cells' voltage difference will be larger than 1.2V. (Please refer to the application note "**OZ8930 AN-5: Unbalance and Wire disconnection Detection and Protection**" for detail.)

UB value	12 bits programmable (OTP Registers 32h and 33h)
UB delay	2 bits Control (bit [5:4] of OTP Register 1ch): 2, 4, 6, 8 scan cycles
Release Value	ub_release = ub+ub_rl_delta*16; ub_rl_delta is controlled by 4 bits (bit [3:0] of OTP Register 32h), 1 LSB=2.44*16mV
Release Delay Time	Same as UB delay

Thermal Protection (OT and UT)

There are 2 types of temperature protections, cell temperature protection and MOSFET temperature protection. Cell temperature protection includes OT, OTPF and UT protection while MOSFET temperature protection just includes OT or OTPF protection (configured by bit 7 of OTP Register 1ch). Therm1 channel is always used to monitor cell temperature. However, therm2 can be used to monitor cell or MOSFET temperature (configured by bit 6 of OTP Register 1ch). In charge, discharge or idle state, UT event will only make charge MOSFET off.

OZ8930 supports separate OT protection threshold settings and OT release threshold settings for charge state and discharge state.

Cell over-temperature protection:

OT Value	Charge	12 bits programmable (OTP Registers 28h and 29h)
	Discharge	12 bits programmable (OTP Registers 2ah and 2bh)
OT Delay Time		2 bits control (bit [3:2] of OTP Registers 1ch): 2, 4, 6, 8 scan cycles
Release Value	Charge	12 bits chg_ot_release = chg_ot+chg_ot_rl_delta, chg_ot_rl_delta is controlled by 4 bits (bit [3:0] of OTP Registers 28h), 1 LSB=1.22mV
	Discharge	12 bits dsg_ot_release = dsg_ot+dsg_ot_rl_delta, dsg_ot_rl_delta is controlled by 4 bits (bit [3:0] of OTP Registers 2ah), 1 LSB=1.22mV
Release Delay Time		Same as OT delay time

Cell under-temperature protection:

UT Value	12 bits programmable (OTP Registers 20h and 21h)
UT Delay Time	Same as OT delay time
Release Value	12 bits programmable (OTP Registers 22h and 23h)
Release Delay Time	Same as OT delay time

Note: OT and UT use the same delay timer

Cell OTPF protection:

OTPF Value	12 bits programmable (OTP Registers 38h and 39h)
OTPF delay	8 scan cycles

If THERM2 is set to be MOSFET OT/OTPF protection, the respective OT/OTPF threshold and release delta value can be set independently (OTP Registers 3ah and 3bh); otherwise it shares the same parameter with cell temperature protection.

Note: When THERM1 is disabled for temperature protection, THERM2 can not be used to execute cell OT/UT and OTPF protection, but the FET OT/OTPF function is still effective.

Besides the THERM1 and THERM2 channels, OZ8930 provides the third channel to monitor the chip internal temperature. However, only OTPF protection is supported in the internal temperature channel. The internal OTPF threshold is also programmable (OTP Register 36h and 37h).

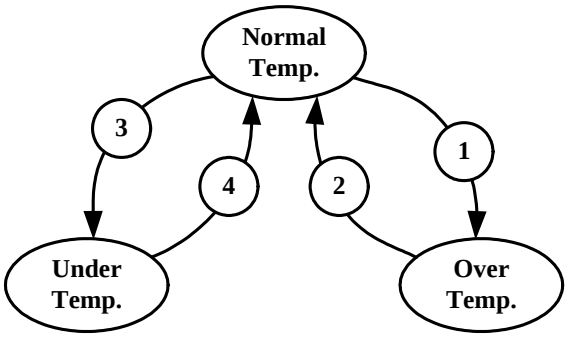


Fig.7 Temperature Protection Chart

Transition	Initial State	Condition & Action	Final State
1	Normal Temp.	• OT event occurs (external temperature ≥ preset external OT threshold & delay timer expires); • Switch off charge & discharge FET	Over Temp.
2	Over Temp.	• OT event clears (external temperature ≤ preset external OT release value & delay timer expires) • Switch on charge & discharge FET if no other protection events occur	Normal Temp.
3	Normal Temp.	• UT event occurs (external temperature ≤ preset external UT threshold & delay timer expires) • Switch off charge FET	Under Temp
4	Under Temp	• UT event clears (external temperature ≥ preset external UT release value & delay timer expires): • Switch on charge FET if no other protection events occur	Normal Temp.

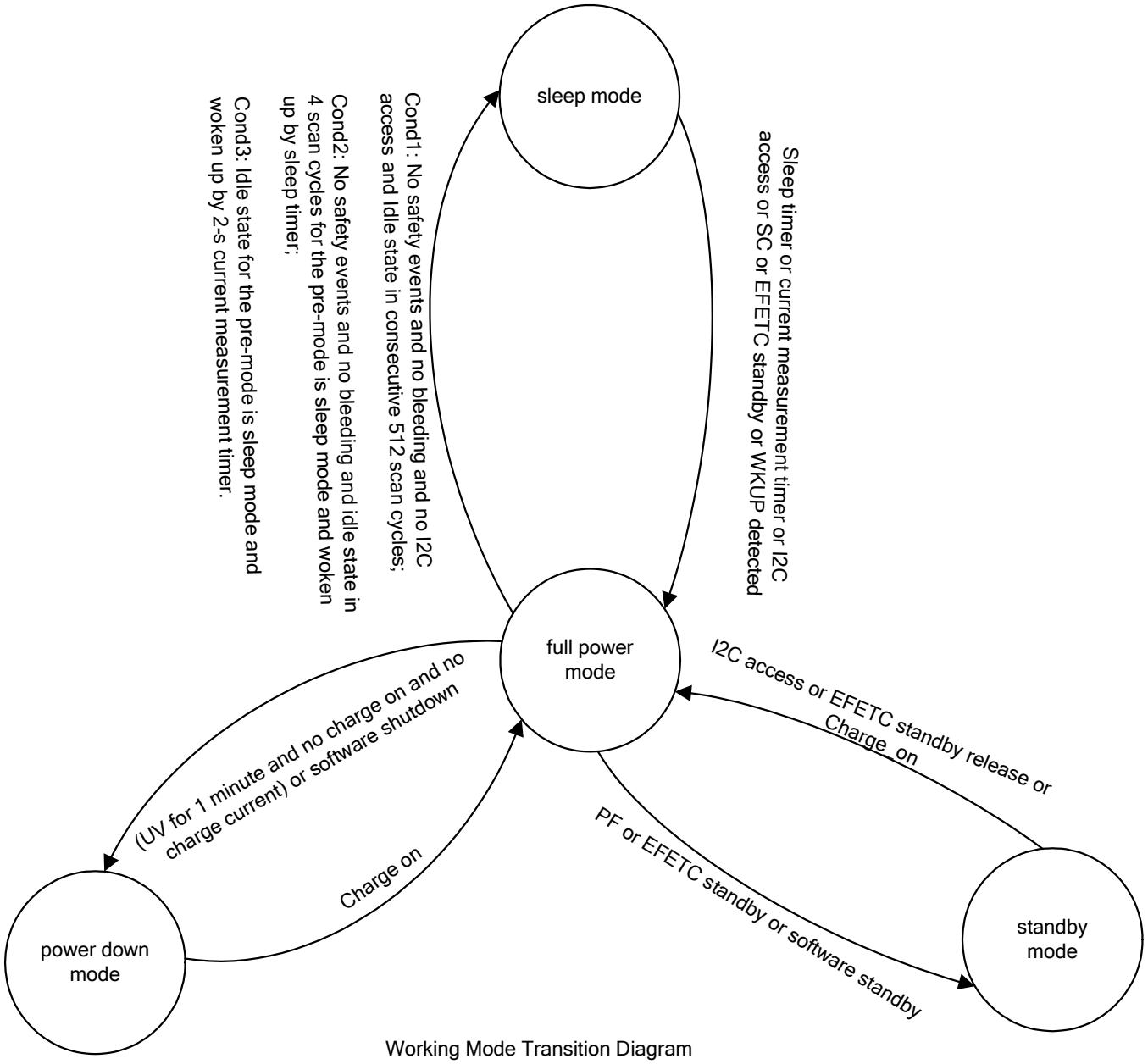
Permanent Failure (PF)

There are 5 types of PF events: OVPF, CELL_OTPF, FET_OTPF, INT_OTPF, ADC_PF. If OVPF, CELL_OTPF, FET_OTPF, INT_OTPF events persists for 8 scan cycles or ADC_PF persists for pre-defined scan cycles, OZ8930 will make PF signal active to blow the external fuse for cutting off the power line or to signal an alarm to user. Once the PF is set to "1", it is kept until chip is reset.

In full power mode, the system will check the PF condition after safety check. If PF is active, the system will enter into standby mode to save power.

Items	Description
OVPF Threshold Value	OVPF threshold is 100mV larger than OV and it is fixed for Low/Standard/High temperature range respectively Delay time: 8 scan cycles.
CELL_OTPF Threshold Value	12-bit threshold in OTP. When external temperature channels (THERM1/2) are set to be battery skin temperature measurement channels, the parameter is used to provide the CELL_OTPF protection function. Delay time: 8 scan cycles.
FET_OTPF Threshold Value	12-bit threshold in OTP. When pin THERM2 is set to measure the temperature of the MOSFET and set to be PF protection, the parameter is used to provide the FET_OTPF protection function. Delay time: 8 scan cycles.
INT_OTPF Threshold	12-bit threshold in OTP. The parameter is used to provide the INT_OTPF protection

Value	function. Delay time: 8 scan cycles.
ADC_PF Threshold Value	OZ8930 will do ADC self-diagnostic in the 1st scan cycle after reset; it also will do ADC self-diagnostic in the 4th scan cycle after wakeup by 1min/4min sleep timer. When one of the following conditions is detected, OZ8930 will treat the ADC as abnormal and the internal ADC_PF counter will increase by one. • Cell voltage offset abnormal: cell1~cell6 offset or cell 6 high-side offset < -100mV (12'hFD7, signed value, LSB = 2.44mV) or > 100mV (12'h029, signed value, LSB = 2.44mV); • TM1, TM2 offset abnormal: TM1 offset or TM2 offset < -100mV (12'hFAE, signed value, LSB=1.22mV) or > 100mV (12'h052, signed value, LSB = 1.22mV). • Current offset abnormal: current offset < -20mV (14'h3AE2, signed value, LSB = 15.3uV) or > 20mV (14'h051E, signed value, LSB = 15.3uV); • Reference 1.8v abnormal: reference 1.8 voltage < 1600mV (12'h51F, signed value, LSB = 1.22mV) or > 2000mV (12'h666, signed value, LSB = 1.22mV). Delay time controlled by 3-bit OTP-mapping register bits: "000": Disable ADC_PF check; "001": 2 ADC failed scan cycle; "010": 3 ADC failed scan cycles; "011": 4 ADC failed scan cycles; "100": 5 ADC failed scan cycles; "101": 6 ADC failed scan cycles; "110": 7 ADC failed scan cycles; "111": 8 ADC failed scan cycles. **Note:** The 1.8V reference's design value is 1800mV.



Working Mode Transition Diagram

Note: (1) Safety events include OV, UV, OT, UT, UB, PF(OVPF, CELL_OTPF, FET_OTPF, INT_OTPF), OC, SC

(2) Idle state: no charge current and no discharge current.

Fig.8 Power Mode Transition

Power Mode

In OZ8930, there are 4 different modes: full power mode, sleep mode, standby mode and power down mode. The power consumption and typical features of them are as below.

Full Power Mode < 380uA
Sleep Mode < 45uA
Standby Mode < 10uA
Power Down Mode < 1uA

In full power mode,

- ADC scan, voltage and temperature protection, current protection (over current and short circuit) work normally to provide the monitor function and the safety engine
- Charge and discharge MOSFET status are decided by the safety engine
- LDO works normally, drive ability: LDO33<30mA; LDO18<2mA; LDO10<5mA

In sleep mode,

- The short circuit protection works for avoiding the critical safety issue
- Transition check (sleep timer, current measurement timer, SC event, I²C activity, EFETC standby, WKUP signal) from sleep mode to full power mode
- Charge and discharge MOSFET status are ON
- LDO drive ability: LDO33<150uA; LDO18<20uA; LDO10<50uA

In standby mode,

- Transition check (I²C activity, EFETC standby release, WKUP signal) from standby mode to full power mode
- Charge and discharge MOSFET status are OFF
- LDO drive ability: LDO33<150uA; LDO18<20uA; LDO10=0

In power down mode,

- Transition check (WKUP signal)
- Charge and discharge MOSFET status are OFF
- LDOs (LDO18, LDO33, LDO10) disabled

Detailed description of power mode transition

No.1: Transition from full power mode into sleep mode

The condition

Condition 1:

- No safety events (OV, UV, OT, UT, UB, PF (OVPF, CELL_OTPF, FET_OTPF, INT_OTPF), OC, SC)
- ***AND*** No bleeding events
- ***AND*** No I²C access
- ***AND*** Idle state (no charge current and no discharge current, i.e. measured current doesn't exceed charge/discharge current threshold) in consecutive 512 scan cycles

Condition 2 (for the pre-mode is sleep mode and woken up by sleep timer):

- No safety events
- ***AND*** No bleeding events
- ***AND*** Idle state in consecutive 4 scan cycles

Condition 3 (for the pre-mode is sleep mode and woken up by 2-s current measurement timer):

- In idle state

Synchronization with MCU

Only when OZ8930 transitions from full power mode into sleep mode under condition 1 above, an interactive operation with MCU is needed. There are 2 I²C-writable registers (**mode_evt_enable**, **mode_event**) to achieve the interrupt function.

a. In case **mode_evt_enable** = 1
   i. Before changing into sleep mode from full power mode, OZ8930 sets **mode_event** register bit and the **next_mode** to sleep mode then asserts PF/ALERTN signal to MCU;
   ii. After receiving the active ALERTN, MCU can check the bits of **mode_event** and **next_mode (2bits)** to know that OZ8930 will enter sleep mode (see **Note 1**). After some preparation steps, if MCU agrees to OZ8930 entering sleep mode, it will clear **mode_event** by writing "1" to OZ8930;
   iii. OZ8930 will wait until the **mode_event** is cleared to "0". Once the **mode_event** is "0", OZ8930 will enter into the sleep mode;
   iv. If MCU doesn't respond to the PF/ALERTN interrupt signal and does not clear the **mode_event** for about 256ms, OZ8930 itself will enter into sleep mode.

b. In case **mode_evt_enable** = 0
   i. OZ8930 doesn't set **mode_event** register bit and does not assert PF/ALERTN signal.
   ii. OZ8930 will enter sleep mode directly.

Note 1: When MCU accesses the mode_event and next_mode, the chip is woken by I²C access wakeup event, so the next_mode is "full power mode" and the chip will enter sleep mode if it meets the sleep conditions again.

No. 2: Transition from full power mode to standby mode
The condition
- PF (OVPF, CELL_OTPF, FET_OTPF, INT_OTPF) event
- ***OR*** ADC_PF for the OTP-mapping ADC_PF delay times
- ***OR*** EFETC standby (if EFETC is configured as external control pin)
- ***OR*** Software standby (MCU sends standby command thru I²C bus)

Synchronization with MCU
a. In case **mode_evt_enable** = 1
   i. Before entering into standby mode from full power mode, OZ8930 sets **mode_event** register bit and **next_mode** to standby mode, then asserts PF/ALERTN signal to MCU;
   ii. After receiving the active ALERTN, MCU can check **mode_event** and **next_mode** to know that OZ8930 will enter standby mode (see **Note 2**). After some preparation steps, if MCU agrees OZ8930 entering standby mode, it will clear **mode_event** by writing "1" to OZ8930;
   iii. OZ8930 will wait until the **mode_event** is cleared to "0". Once the **mode_event** is "0", OZ8930 will enter standby mode;
   iv. If MCU doesn't respond to the PF/ALERTN interrupt signal and not clear the **mode_event** for about 256ms, OZ8930 itself will enter into standby mode.

b. The case **mode_evt_enable** = 0
   i. OZ8930 doesn't set **mode_event** register bit and not assert PF/ALERTN signal;
   ii. OZ8930 will enter standby mode directly.

Note 2: When MCU accesses the mode_event and next_mode, the chip is woken by I2C access wakeup event, so the next_mode is "full power mode" and the chip will enter standby mode if it meets the standby conditions again.

No. 3: Transition from full power mode into power down mode
The condition
- UV shutdown (UV for 1 minute ***AND*** No charge-on signal ***AND*** No charge current)
- ***OR*** Software shutdown (MCU sends shutdown command thru I²C bus)

Synchronization with MCU
a. In case **mode_evt_enable** = 1
   i. Before changing into power down mode from full power mode, OZ8930 sets **mode_event** register bit and **next_mode** to power down mode, then asserts PF/ALERTN signal to MCU;
   ii. After receiving the active ALERTN, MCU can check **mode_event** and **next_mode**, to know that OZ8930 will enter power down mode (see **Note 3**). After some preparation steps, if MCU agrees OZ8930 entering power down mode, it will clear **mode_event** by writing "1" to OZ8930;

iii. For UV shutdown, if mode_event is set to "1", OZ8930 is kept in full-power mode; if mode_event is set to "0", OZ8930 will enter power down mode after 1 minute (see Note 3). For software shutdown, OZ8930 will enter power down mode when mode_event is "0" or after a 256mS timeout
iv. After OZ8930 enters power down mode, all LDOs are shut down to save power. And MCU will lose the power supply;

Note 3: If MCU wants to enter power mode immediately, it can send out "software shutdown"

b. the case **mode_evt_enable** = 0
   i. OZ8930 doesn't set **mode_event** register bit and does not assert PF/ALERTN signal;
   ii. OZ8930 will enter power down mode directly.

No. 4: Transitions from sleep mode to full power mode
The condition
- Customer-setting 1-minute/4-minute sleep timer wakeup (after wakeup, do normal ADC and safety check)
- ***OR*** 2-second current measurement timer wakeup (after wakeup, do 14-bit current ADC and check current status)
- ***OR*** I²C access
- ***OR*** SC (short-circuit) event happened
- ***OR*** EFETC standby event happened (EFETC pin force OZ8930 to enter standby mode)
- ***OR*** WKUP signal detected (charge-on signal or analog wake up signal)

Synchronization with MCU
- Wakeup event such as sleep timer event, current wakeup event (if charge or discharge current is found, the current wakeup event is set), SC wakeup event, EFETC wakeup event will make PF/ALERTN active to inform MCU.
- In full power mode, scan_event will be set in each scan cycle to assert PF/ALERTN signal to MCU.

No. 5: Transitions from standby mode to full power mode
The condition
- I²C access activity
- ***OR*** EFETC standby released
- ***OR*** charge-on signal detected

Synchronization with MCU
- In full power mode, scan_event will be set in each scan cycle to assert PF/ALERTN signal to MCU.

No. 6: Transitions from power down mode to full power mode
The condition
- Charge-on signal detected

Synchronization with MCU
- After OZ8930 startup from power down mode, the LDO33 will provide 3.3V power supply to external MCU.
- In full power mode, scan_event will be set in each scan cycle to assert PF/ALERTN signal to MCU.

Brief transition table:

Transition	Initial State	Condition	Final State
1	Full Power	Condition 1: No safety events (OV, UV, OT, UT, UB, PF (OVPF, CELL_OTPF, FET_OTPF, INT_OTPF), OC, SC) ***AND*** No bleeding events ***AND*** No I²C access ***AND*** Idle state (no charge and no discharge current) in consecutive 512 scan cycles Condition 2 (for the pre-mode is sleep mode and woken up by sleep timer): No safety events ***AND*** No bleeding events ***AND*** Idle state in 4 scan cycles Condition 3 (for the pre-mode is sleep mode and woken up by 2-s current measurement timer): In Idle state	Sleep
2	Full Power	PF (OVPF, CELL_OTPF, FET_OTPF, INT_OTPF) ***OR*** ADC_PF for the OTP-mapping ADC_PF delay times ***OR*** EFETC standby control ***OR*** Software standby control by I²C access	Standby
3	Full Power	UV for 1 minute ***AND*** No charge-on signal ***AND*** No charge current ***OR*** Software shutdown by I²C access	Power Down
4	Sleep	Sleep timer expires (1-minute/4-minute) ***OR*** Current measurement timer expires (2 seconds) ***OR*** I²C access ***OR*** SC event ***OR*** EFETC standby control ***OR*** WKUP signal detected (charge-on signal or analog wake up signal)	Full Power
5	Standby	I²C access ***OR*** Charge-on signal detected ***OR*** EFETC standby release	Full Power
6	Power Down	Charge-on signal detected	Full Power

Internal Temperature Sensor

OZ8930 takes advantage of silicon device physics and circuit design technology for the internal temperature sensor. The internal temperature sensor generates a voltage level which is proportional to the temperature. As shown in Figure 9 below, with a temperature increase of 1°C, internal temperature sensor output voltage will increase by 2.0976mV. The offset can be from the 12-bit OTP which is measured in the ATE test stage. So, if at T0, ADC reads VT0, the characteristic transfer function is: VTS (mV) = 2.0976*T+ (VT0 – 2.0976*T0)

However, The internal temperature sensor's characteristics could be affected by fab process, please refer to OZ8930 Application Note for detailed calculation and compensation if high accuracy is required.

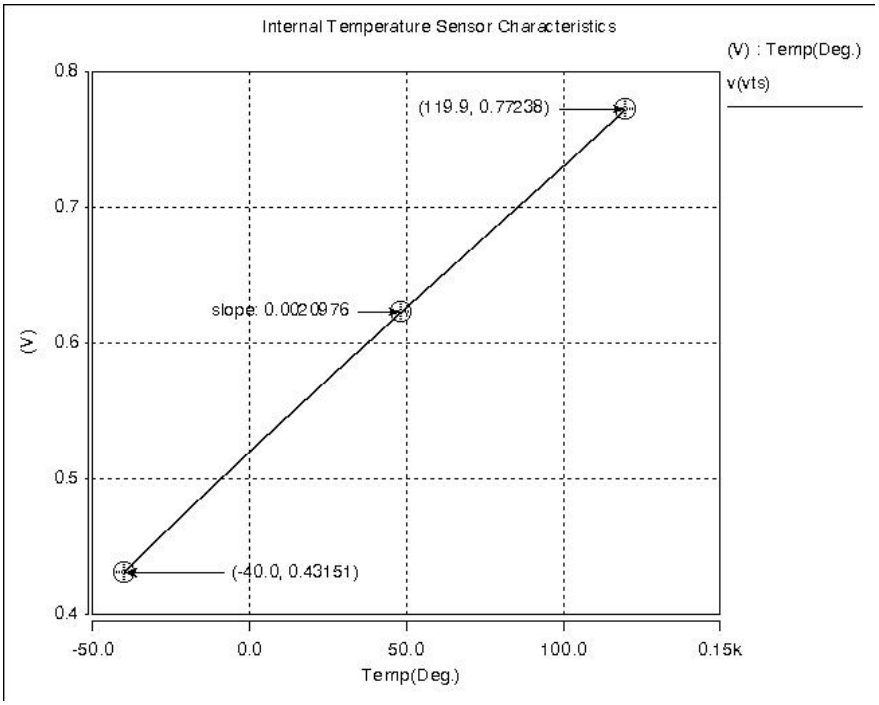


Fig.9 Internal Temperature Sensor Curve

External Temperature Sensor

OZ8930 provides 2 ADC channels for external temperature detection; the application circuitry is shown in Figure 10. Our reference application uses 103-NTC thermistor. 103-NTC thermistor's RT characteristics are shown in Figure 11. The sensed voltage Vt characteristics are shown in Figure 12. For Example: Vt2=3.3V * RT2 / (RB2 + RT2).

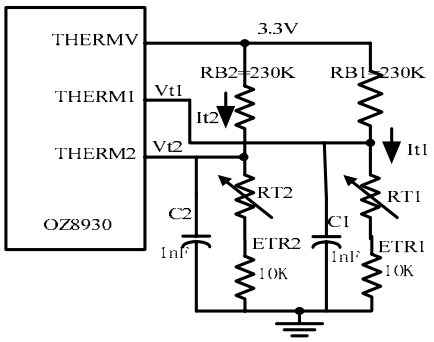


Fig.10 External Temperature Sensor Application

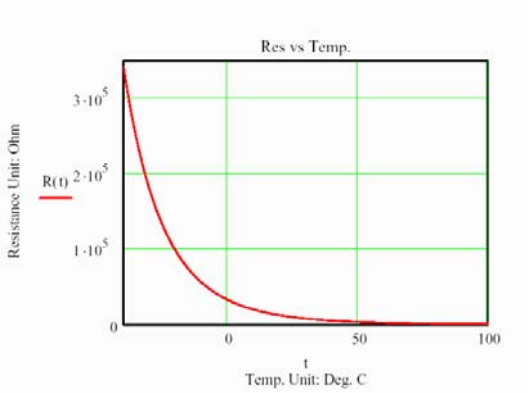


Fig.11 Thermistor RT characteristics

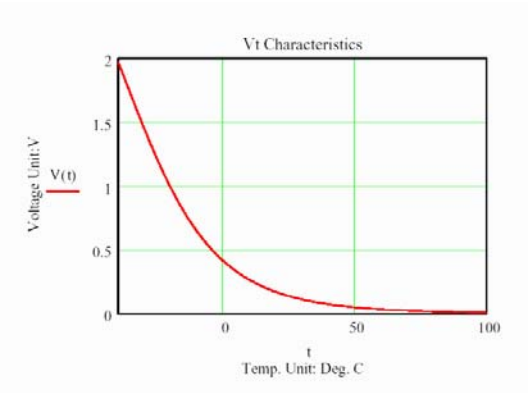


Fig.12 The sensed voltage Vt characteristics

Power MOSFET Driver

Smart MOSFET driver supports N-type MOSFET for discharge control, and supports N-type MOSFET or P-type MOSFET for charge control. The driver also supports parallel and serial charge/discharge loop.

OZ8930 provides a 10V (typical) voltage at DSG pin for keeping the discharge MOSFET in ON state. It also has an embedded a 5uA current sink for P-type charge MOSFET driver or level shifter for N-type charge MOSFET driver. If the charge MOSFET is required to be in OFF state, this 5uA sink current circuit should be disabled and the CHG pin is in high impedance state. Otherwise, the 5uA sink current is enabled and then the charge MOSFET gate-to-source voltage is decided by external divider resistor. The MOSFET driver application circuits are shown in Fig. 13 and Fig. 14.

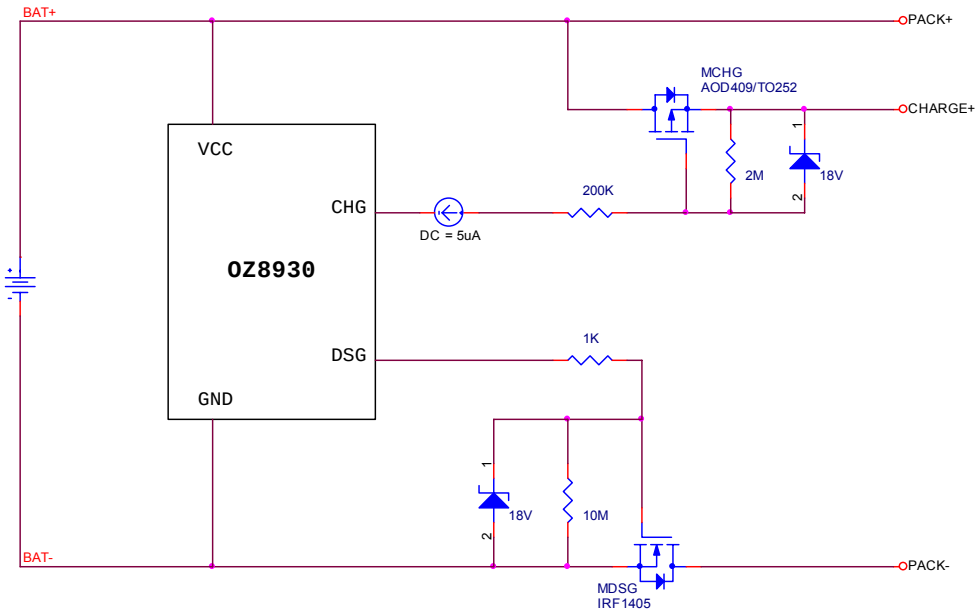


Fig.13 MOSFET drive circuit with P-type charge MOSFET

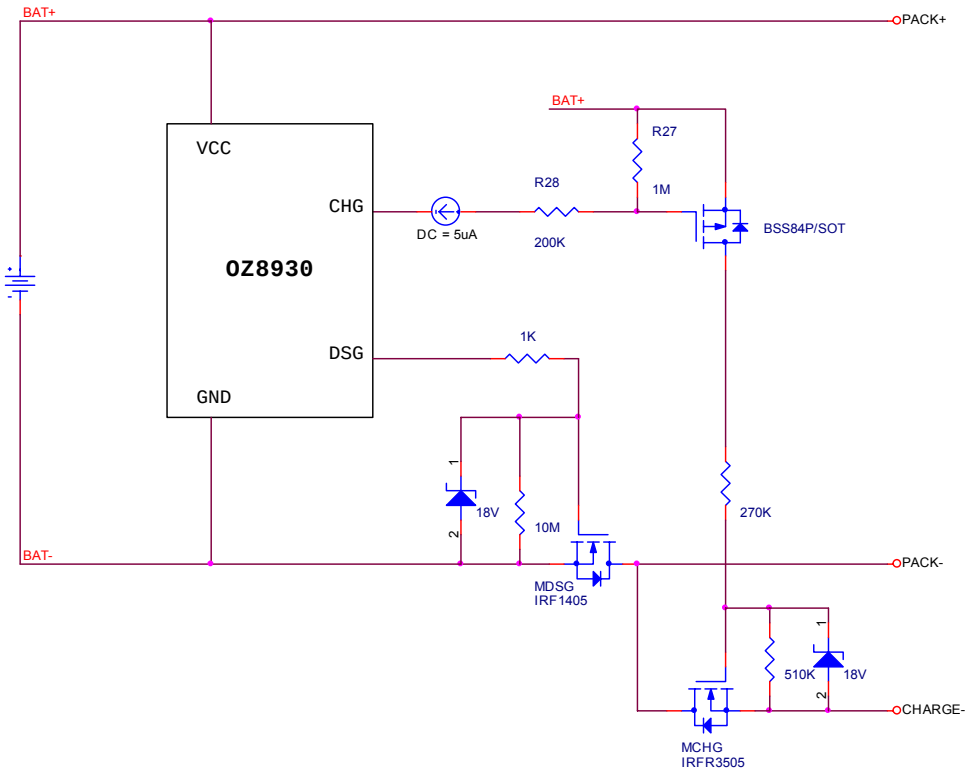


Fig.14 MOSFET drive circuit with N-type charge MOSFET

MOSFET Control

OZ8930 includes a Battery Protection Engine (BPE) used to control the charge and discharge MOSFET according to the protection events occurring at present and current charge/discharge state. The detail for charge and discharge control is summarized in the following control matrix.

safety event				Charge/discharge state		MOSFET control	
pf_fet_ disable	sc_fet_disable or coc_fet_disable or doc0_fet_disable or doc1_fet_disable or ub_fet_disable or dsg_ot_fet_disable	uv_fet_disable	ov_fet_disable or ut_fet_disable or chg_ot_fet_disable	in_ charge	in_discharge	dischg_ enable	chg_ enable
1	x	x	x	x	x	0	0
0	1	x	x	x	x	0	0
0	0	1	0	x	x	0	1
0	0	1	1	x	x	0	0
0	0	0	1	0	0	1	0
0	0	0	1	0	1	1	1
0	0	0	1	1	x	1	0
0	0	0	0	x	x	1	1

Note 1: pf_fet_disable, sc_fet_disable, coc_fet_disable, doc0_fet_disable, doc1_fet_disable, ub_fet_disable, ov_fet_disable, uv_fet_disable, ot_fet_disable, and ut_fet_disable are internal signals generated by Battery Protection Engine (BPE) embedded in OZ8930. The status of these signals is in fact decided by the safety events occurring at present.
Any time PF occurs, pf_fet_disable is “1”, else it is “0”;
Any time SC occurs, sc_fet_disable is “1”, else it is “0”;
Any time COC occurs, coc_fet_disable is “1”, else it is “0”;
Any time DOC0 occurs, doc0_fet_disable is “1”, else it is “0”;
Any time DOC1 occurs, doc1_fet_disable is “1”, else it is “0”;

Any time UB occurs, uv_fet_disable is “1”, else it is “0”;
Any time OV occurs, ov_fet_disable is “1”, else it is “0”;
Any time UV occurs, uv_fet_disable is “1”, else it is “0”;
Any time discharge OT occurs, dsg_ot_fet_disable is “1”, else it is “0”;
Any time charge OT occurs, chg_ot_fet_disable is “1”, else it is “0”;
Any time UT occurs, ut_fet_disable is “1”, else it is “0”.
Note 2: in_charge and in_discharge are internal signals in OZ8930. When in charge state, in_charge is “1”, else it is “0”; when in discharge state, in_discharge is “1”, else it is “0”. (Refer to the description of Operation Register 01h for charge and discharge state definition)
Note 3: dischg_enable and chg_enable are MOSFET control signals in OZ8930. When dischg_enable is “1”, discharge MOSFET is enabled to be in “ON” state, else it is in “OFF”. When chg_enable is “1”, charge MOSFET is enabled to be at “ON” state, else it is “OFF”.
Note 4: If the OT is detected when the chip is in charge state (in_charge is “1”, in_discharge is “0”) or in idle state (in_charge is “0” and in_discharge is “0”), the OT is regarded as charge OT and chg_ot_fet_disable is “1”. If the OT is detected when the chip is in discharge state (in_charge is “0”, in_discharge is “1”), the OT is regarded as discharge OT and dsg_ot_fet_disable is “1”.
Note 5: When DOC0, DOC1 is a time release, the OT after its release may be charge OT or discharge OT.

EFETC Control

OZ8930 also provides a pin (EFETC) for the charge and discharge MOSFET control. It’s a multi-function pin. Efect_mode2 : Efect_mode0 (bit [6:4] in OTP Register [1fh]) are used to configure the pin’s function. The following table gives the detail.

Efect_mode2 : Efetc_mode0	EFETC pin function mode
000	High active input to forcibly disable charge FET.
001	High active input to forcibly disable discharge FET.
010	High active input to forcibly disable charge FET and discharge FET.
011	Output discharge FET status.
100	High active input as external standby.
101	Output internal xx_fet_disable signal. xx_fet_disable = (ov_fet_disable & ov_out_enable)) | (uv_fet_disable & uv_out_enable) | (ot_fet_disable & ot_out_enable) | (ut_fet_disable & ut_out_enable).
110, 111	Reserved

In the above table, ov_out_enable, uv_out_enable, ot_out_enable and ut_out_enable are the configuration bits in OTP Register 1eh. ov_fet_disable, uv_fet_disable, ot_fet_disable and ut_fet_disable are internal signals generated by Battery Protection Engine (BPE) embedded in OZ8930. The status of these signals is in fact decided by the safety events occurring at present. Any time OV occurs, ov_fet_disable is “1”, else it is “0”; any time UV occurs, uv_fet_disable is “1”, else it is “0”; any time OT occurs, ot_fet_disable is “1”, else it is “0”; any time UT occurs, ut_fet_disable is “1”, else it is “0”.

The EFETC pin can be used to simplify the application circuit when multiple OZ8930 chips are used to manage the battery with more than 6 cells in series.

Serial Communication Bus

OZ8930 supports I²C Bus communication interface. The I²C Bus master can access OZ8930’s registers with I²C Bus protocol. In this condition, OZ8930 works as an I²C Bus slave device.

In OZ8930, the I²C Bus address can be configured by setting **I²C_addr1--I²C_addr0** (bit [1:0] of OTP Register [14h]). OZ8930 I²C device address is specified by the 2-bit I²C address configuration as follows:

Bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	1	1	0	0	I²C_addr[1:0]		r/wn

The following table lists the available addresses and the corresponding settings.

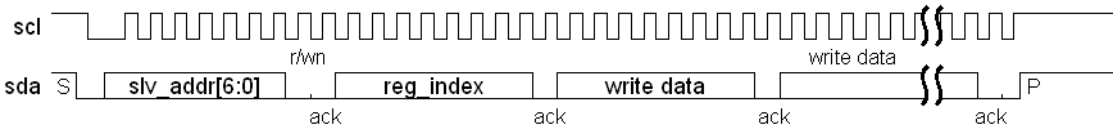
I²C_addr1-I²C_addr0	I²C Address(Hex)
00	0x60
01	0x62
10	0x64
11	0x66

Writing Data Access

In writing data access, there are some bytes transmitted from master to slave as following:

1. Slave address byte: slv_addr[6:0], r/wn;
2. Register index byte: reg_index[7:0];
3. Written data bytes: written data.

slv_addr[6:0] is the I²C address to select an I²C device. r/wn is the read/write bit. If "1", selects read access; if "0", selects write access. Here is writing data access, it is "0". Reg_index[7:0] is used to indicate the register index. Written data is the data written into the device.

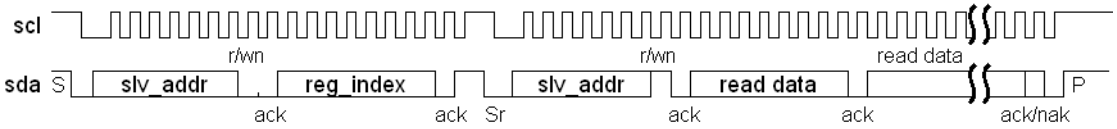


The above diagram shows the timing of writing data access. At first is the slave_addr[6:0] to select one slave node; the next byte is the reg_index to define the register index; the next bytes are the data for writing into the device. The first address to be written is indicated by the reg_index. Once one byte is written successfully, the device's internal register address will be incremented by 1 automatically so that the next byte is written into the register of the next continuous address.

Reading Data Access

In reading data access, the bytes are transmitted in the following order:

1. Slave address byte from master to slave: slv_addr[6:0], r/wn;
2. Register index byte from master to slave: reg_index[7:0];
3. Slave address byte from master to slave: slv_addr[6:0], r/wn;
4. Data read out from slave to master: read data.



The above diagram shows the reading data access. The first time slot is the slave address to select one slave device; the next is the reg_index to indicate the register index; next is the repeated start; next is slave address again, finally there is one byte of reading out data from slave device. After one byte is sent out successfully, the device internal register address will be automatically incremented by 1 so that the next byte is sent out.

Note: Continuous reading of data bytes is not recommended for OZ8930 because it may be affected by noise.

Bus Timeout

For the reliability consideration, if the SCL or SDA line keeps in low for more than 25ms, the I²C Bus engine and OZ8930 will be reset and the SCL and SDA lines will not be driven to low by OZ8930. This timeout function can be used to reset OZ8930 also.

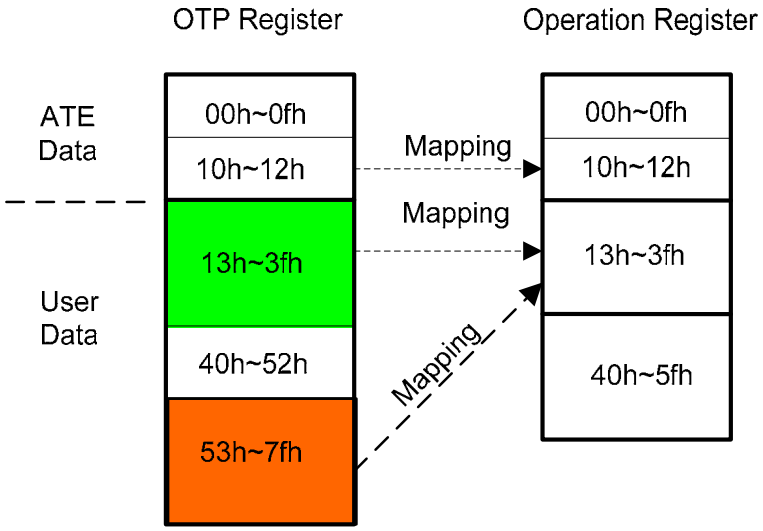
Bus Disconnection

I²C Bus is actually board level communication bus and not recommended for hot plugging. Because hot plugging may induce surge current and other noise might cause wrong data to be written into certain registers, especially during I²C Bus access.

OTP AND OPERATION REGISTERS MAP

There are two types of register data: Operation Register data (00h~5fh) and OTP Register data (00h~7fh). Software can directly access the Operation Registers and indirectly access the OTP Registers via accessing the Operation Registers 05h~07h. OTP Registers 00h~12h are used to store the ATE data. In this section, only 0ch used to store DOC offset value can be accessed. In addition, Operation Registers 0fh~12h are also reserved for the chip vendor usage. Access to the user data in OTP Registers 13h~7fh and in Operation Registers 13h~1fh is controlled by **user_freeze** and **user_unlock** register bits. When **user_freeze** is "1" and **user_unlock** is "0", the user data are read only; otherwise, the user data are readable, writable. For the user data in OTP Registers, there are 2 pages: the default page in OTP Registers 13h~3fh and the backup page in OTP Registers 53h~7fh (so customers can modify the "User data" in OTP Registers for 2-time).

Some of the Operation Register values are mapped from OTP Registers, the mapping relationship is as following:



Use Data has 2 pages:
default page (OTP register 13h~3fh) used when page_sel = "0" ;
backup page(OTP register 53h~7fh) used when page_sel = "1" .

OTP register and Operation Register Diagram

Operation Registers

Operation Registers Map

Register index (hex)	Register Name	Bit Number							
		7	6	5	4	3	2	1	0
00	Chip ID & Revision	chip_id[3:0]				chip_rev[3:0]			
01	System Status	soft_dischg_ enable	soft_chg_ enable	soft_scan_ req	in_bld	dischg_ enable	chg_ enable	in_dischg	in_chg
02	Alert Event	safety_event	scan_event	tm_wk_ event	currt_wk_ event	sc_wk_ event	efetc_wk_ event	mode_event	reserved
03	Event Enable	reserved	scan_event_ enable	tm_wk_ event_ enable	reserved	reserved	reserved	mode_event_ enable	reserved
04	Therm Data	Reserved		tm2_in	tm1_in	tm2_oe	tm2_out	tm1_oe	tm1_out
05	OTP Data	otp_data[7:0]							
06	OTP Addr	reserved	otp_addr[6:0]						
07	OTP Control	otp_busy	Reserved		otp_mode	otp_marg_rd	otp_wr	otp_map	otp_rd
08	OTP Enable	soft_enable	soft_down	soft_standby	Test_enable	select_alert	no_wk_map	user_unlock	otp_enable
09	FET Disable	pf	sc_fet_ disable	oc_fet_ disable	ub_fet_ disable	ut_fet_ disable	ot_fet_ disable	uv_fet_ disable	ov_fet_ disable
0a	Mode Change	reserved	mode_ timeout	next_mode[1:0]		reserved	pf_type[2:0]		
0b	Reserved	reserved							
0c	Max Cell	max_cell_data[3:0]				reserved	max_cell_channel[2:0]		
0d		max_cell_data[11:4]							
0e	reserved	reserved							
0f	reserved	Reserved for chip vendor use only							
10	reserved	Reserved for chip vendor use only							
11	reserved	Reserved for chip vendor use only							
12	reserved	Reserved for chip vendor use only							
13	Scan Control	prty_chk	reserved	auto_scan	currt_scan	tm_scan[1:0]		cell_num[1:0]	
14	I²C Addr	reserved						I²C_addr[1:0]	
15	COC TH	coc_mid_t_th[3:0]				coc_low_t_th[3:0]			
16	COC Time	coc_high_t_th[3:0]				coc_release[1:0]		coc_delay[1:0]	
17	DOC0 TH	reserved		doc0_th[5:0]					
18	DOC0 Time	reserved		doc0_release[1:0]		doc0_delay[3:0]			
19	DOC1 TH	reserved		doc1_th[5:0]					
1a	DOC1 Time	reserved		doc1_release[1:0]		doc1_delay[3:0]			
1b	SC Time	dischg_th[1:0]		chg_th[1:0]		sc_release[1:0]		sc_delay[1:0]	
1c	Safety Time	tm2_fet_ot_ sel	tm2_fet	ub_delay[1:0]		ot_ut_delay[1:0]		ov_delay[1:0]	
1d	ADC_PF_Time	uv_delay[1:0]		reserved		pf_ignr_shrt	adc_pf_delay[2:0]		
1e	Bleeding Control	ov_out_ enable	uv_out_ enable	ot_out_ enable	ut_out_ enable	bld_support	bld_idle	bld_accuracy[1:0]	
1f	Sleep Control	user_freeze	efetc_mode[2:0]			reserved		sleep_ support	sleep_time
20	UT	ut_th[3:0]				reserved			
21		ut_th[11:4] (under temperature threshold for battery cell tube skin, 1.22mV LSB, 2's complement format)							
22	UT_RL	ut_rl[3:0]				Reserved			
23		ut_rl[11:4] (under temperature release for battery cell tube skin, 1.22mV LSB, 2's complement format)							
24	CHG_T2	chg_t2[3:0]				Reserved			
25		chg_t2[11:4] (charge temperature point2 for battery cell tube skin, 1.22mV LSB, 2's complement format)							
26	CHG_T3	chg_t3[3:0]				Reserved			
27		chg_t3[11:4] (charge temperature point3 for battery cell tube skin, 1.22mV LSB, 2's complement format)							
28	CHG_OT	chg_ot [3:0]				chg_ot_rl_delta[3:0] (charge over temperature release delta, 1.22mV LSB, 2's complement format) (charge ot relase = charge_ot + chg_ot_rl_delta)			
29		chg_ot [11:4] (charge over temperature for battery cell tube skin, 1.22mV LSB, 2's complement format)							

Register index (hex)	Register Name	Bit Number							
		7	6	5	4	3	2	1	0
2a	DSG_OT	dsg_ot [3:0]				dsg_ot_rl_delta[3:0] (discharge over temperature release delta, 1.22mV LSB, 2's complement format) (discharge ot relase = discharge_ot + dischg_ot_rl_delta)			
2b		dsg_ot [11:4] (discharge over temperature for battery cell tube skin, 1.22mV LSB, 2's complement format)							
2c	LOW_T_OV	low_t_ov[3:0]				reserved			
2d		low_t_ov[11:4] (low-temperture over voltage threshold for under T2 temperature, 2.44mV LSB, 2's complement format; low_t_ovpf = low_ov + 41(100mV)							
2e	Mid_T_OV	mid_t_ov[3:0]				reserved			
2f		mid_t_ov[11:4] (middle-temperature over voltage threshold for T2~T3 temperature, 2.44mV LSB, 2's complement format; mid_t_ovpf = mid_ov + 41(100mV)							
30	High_T_OV	high_t_ov[3:0]				reserved			
31		high_t_ov[11:4] (high-temperature over voltage threshold for over T3 temperautre, 2.44mV LSB, 2's complement format; high_t_ovpf = high_t_ov + 41(100mV)							
32	UB	ub[3:0]				ub_rl_delta[3:0] (cell unbalance release delta, 2.44*16mV LSB, 2's complement format) (ub_release = ub + ub_rl_delta*16)			
33		ub[11:4] (cell unbalance threshold, 2.44mV LSB, 2's complement format)							
34	UV	uv[3:0]				Reserved			
35		uv[11:4] (under vlotage threshold, 2.44mV LSB, 2's complement format)							
36	INT_OTPF	int_otpf_th[3:0]				Reserved			
37		int_otpf_th[11:4] (over temperature PF threshold for internal temperature, 1.22mV LSB, 2's complement format)							
38	CELL_OTPF	cell_otpf[3:0]				Reserved			
39		cell_otpf[11:4] (over temperature PF threshold for battery cell tube skin, 1.22mV LSB, 2's complement format)							
3a	FET_OT/FET_OTPF	fet_ot/fet_otpf[3:0]				fet_ot_delta[3:0] (FET over temperature release delta, 1.22mV LSB, 2's complement format) (fet ot relase = fet_otpf + fet_ot_delta)			
3b		fet_ot/fet_otpf[11:4] (over temperature or over temperature PF threshold for MOSFET, 1.22mV LSB, 2's complement format)							
3c	Bld Start	bld_start[3:0]				Reserved			
3d		bld_start[11:4] (bleeding start poin, 2.44mV, 2's complement format)							
3e	OV Hysteresis	reserved		ov_hys[5:0] (over voltage release hysteresis, 2.44*4mV LSB, 2's complement format; theory range: -312.3mV ~ +302.56, application range: -312.3mV ~ 0m)(ov release = ov threshold + ov_hys*4)					
3f	UV Hysteresis	reserved		uv_hys[5:0] (under voltage release hysteresis, 2.44*16mV LSB, 2's complement format; theory range: -1249mV ~ +1210mV, application range: 0 ~ +1210mV)(uv release = uv threshold + uv_hys*16)					
40	Cell1 Data	cell1_data[3:0]				reserved			cell1 offset flag
41		cell1_data[11:4]							
42	Cell2 Data	cell2_data[3:0]				reserved			cell2 offset flag
43		cell2_data[11:4]							
44	Cell3 Data	cell3_data[3:0]				reserved			cell3 offset flag
45		cell3_data[11:4]							
46	Cell4 Data	cell4_data[3:0]				reserved			cell4 offset flag
47		cell4_data[11:4]							
48	Cell5 Data	cell5_data[3:0]				reserved			cell5 offset flag
49		cell5_data[11:4]							
4a	Cell6 Data	cell6_data[3:0]				reserved			cell6 offset flag
4b		cell6_data[11:4]							
4c	INT Data	int_data[3:0]				reserved			cell6 high offset flag
4d		int_data[11:4]							

Register index (hex)	Register Name	Bit Number							
		7	6	5	4	3	2	1	0
4e	TM1 Data	tm1_data[3:0]				reserved			
4f		tm1_data[11:4]							
50	TM2 Data	tm2_data[3:0]				reserved			
51		tm2_data[11:4]							
52	Current Data	current_data[5:0]						reserved	
53		current_data[13:6]							
54	Group1 Offset	group1_offset[7:0]							
55	Group2 Offset	group2_offset[7:0]							
56	Current Offset	current_offset[3:0]				reserved			
57		current_offset[11:4]							
58	Ref18 Data	ref18_data[3:0]				reserved			
59		ref18_data[11:4]							
5a	OV/UV timer	ov_timer[3:0]				uv_timer[3:0]			
5b	OT/UT timer	ot_timer[3:0]				ut_timer[3:0]			
5c	UB timer	reserved				ub_timer[3:0]			
5d-5f	Reserved	Reserved for internal use (Writing this register is prohibited)							

Detailed Operation Registers Information

Register 00h – Chip ID & Revision Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CHP_ID3 (R)	CHP_ID2 (R)	CHP_ID1 (R)	CHP_ID0 (R)	CHP_REV3 (R)	CHP_REV2 (R)	CHP_REV1 (R)	CHP_REV0 (R)

Default value is 8'h40.

Bit7 – Bit4 (CHP_ID3 – CHP_ID0) is chip ID (4'h4) which indicates OZ8930.

Bit3 – Bit0 (CHP_REV3 – CHP_REV0) is chip revision.

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Register 01h – System Status

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
soft_dischg_enable (RW)	soft_chg_enable (RW)	soft_scan_req (RW)	In_bld (R)	dischg_enable (R)	Chg_enable (R)	in_dischg (R)	In_chg (R)

Default value is 8'hC0.

Bit7 (soft_dischg_enable): Software discharge enable, software can forcibly turn off the discharge FET by setting "0" when soft_enable is "1".

Bit6 (soft_chg_enable): Software charge enable, software can forcibly turn off the charge FET by setting "0" when soft_enable is "1".

Bit5 (soft_scan_req): Soft scan request, in trigger scan mode (auto_scan = 0), trigger one ADC scan when writing "1" into this bit. When read-out, always "0" is returned

Bit4 (in_bld): a certain cell is in bleeding.

Bit3 (dischg_enable): Discharge FET status: "1" means on; "0" means off.

Bit2 (chg_enable): Charge FET status: "1" means on; "0" means off.

Bit1 (in_dischg): In discharge state, i.e., the discharge current (negative value) is below the set discharge state threshold (bit [7:6] of OTP Register 1bh).

Bit0 (in_chg): In charge state, i.e., the charge current (positive value) is above the set charge state threshold (bit [5:4] of OTP Register 1bh).

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Register 02h – Alert Event Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
safety_event (RW)	scan_event (RW)	tm_wk_event (RW)t	currt_wk_event (R)	sc_wk_event (RW)	efect_wk_event (RW)	mode_event (RW)	Reserved (R)

Default value is 8'h00.

Bit7 (safety_event): Safety event, set to "1" due to any of sc_fet_disable, oc_fet_disable, ub_fet_disable, ut_fet_disable, ot_fet_disable, ut_fet_disable, uv_fet_disable, ov_fet_disable setting, cleared to "0" by software writing "1".

Bit6 (scan_event): Scan event, set to "1" when ADC scan is finished, cleared to "0" by software writing "1".
Bit5 (tm_wk_event): Timer wakeup event, set to "1" by timer wakeup, cleared to "0" by software writing "1".

Bit4 (currt_wk_event): Current wakeup event, set to "1" by current wakeup, cleared to "0" by software writing "1".

Bit3 (sc_wk_event): SC wakeup event, set to "1" by SC (short circuit) wakeup, cleared to "0" by software writing "1".

Bit2 (efetc_wk_event): Efetc wakeup event, set to "1" by efetc wakeup, cleared to "0" by software writing "1".

Bit1 (mode_event): Mode change event, set to "1" when entering sleep mode, stand by mode or power down mode if mode_event_enable register bit is "1" and soft_enable is "1", cleared to "0" by softwaring writing "1".

Bit0 (reserved): Reserved.

==========

Register 03h – Event Enable Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved (R)	scan_event_enable (RW)	tm_event_enable (RW)t	reserved (R)	reserved (R)	reserved (R)	mode_event_enable (RW)	reserved (R)

Default value is 8'h00.

Bit7: Reserved.

Bit6 (scan_event_enable): Enable scan event interrupt, make ALERTN pin active due to scan event setting.

Bit5 (tm_event_enable): Timer wakeup event, set to "1" by timer wakeup, cleared to "0" by software writing "1".

Bit4 _ Bit2: Reserved.

Bit1 (mode_event_enable): Enable mode_event interrupt, make ALERTN pin active due to mode event setting.

Bit0 (reserved): Reserved.

==========

Register 04h – THERM Data Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved (R)	reserved (R)	tm2_in (R)	tm1_in (R)	tm2_oe (RW)	tm2_out (RW)	tm1_oe (RW)	tm1_out (RW)

Default value is 8'h00.

Bit7_Bit6: Reserved.

Bit5 (tm2_in): Therm2 input.

Bit4 (tm1_in): Therm1 input.

Bit3 (tm2_oe): High active to enable therm2 output (output tm2_out to THERM2 pin) when therm2 is a digital pin.

Bit2 (tm2_out): Therm2 output data.

Bit1 (tm1_oe): High active to enable therm1 output (output tm1_out to THERM1 pin) when therm1 is a digital pin.

Bit0 (tm1_out): Therm1 output data.

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Register 05h – OTP Data Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Otp_data7 (RW)	Otp_data6 (RW)	Otp_data5 (RW)	Otp_data4 (RW)	Otp_data3 (RW)	Otp_data2 (RW)	Otp_data1 (RW)	Otp_data0 (RW)

Default value is 8'h00.

Bit7_Bit0 (otp_data7 – otp_data0): The data written into OTP. In OTP mode, the read-back data is the OTP data; in non-OTP mode, the read-back data is the data written into these registers.

==========

Register 06h – OTP Address Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved (R)	Otp_addr6 (RW)	Otp_addr5 (RW)	Otp_addr4 (RW)	Otp_addr3 (RW)	Otp_addr2 (RW)	Otp_addr1 (RW)	Otp_addr0 (RW)

Default value is 8'h00.

Bit7: Reserved.

Bit6_Bit0 (otp_addr6 – otp_addr0): OTP address for OTP writing and OTP reading.

==========

Register 07h – OTP Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Otp_busy (R)	reserved (R)	reserved (R)	Otp_mode (RW)	Otp_marg_rd (RW)	Otp_wr (RW)	Otp_map (RW)	Otp_rd (RW)

Default value is 8'h00.

Bit7 (otp_busy): OTP busy, it is “1” when OTP reading or writing is in progress.

Bit6_Bit5: Reserved.

Bit4 (otp_mode): OTP mode, OTP access (OTP reading, OTP mapping, OTP writing, OTP margin reading) is available by setting “1” into this bit when otp_enable is “1”.

Bit3 (otp_marg_rd): OTP margin reading, writing “1” will start an OTP margin reading which has the 4th priority.

Bit2 (otp_wr): OTP writing, writing “1” will start an OTP writing which has the 3rd priority to block OTP margin read.

Bit1 (otp_map): OTP mapping, writing “1” will start an OTP mapping (map OTP data into internal registers) which has the 2nd priority to block OTP writing and OTP margin reading access.

Bit0 (otp_rd): OTP reading, writing “1” will start an OTP reading which has the 1st priority to block OTP mapping, OTP writing and OTP margin reading.
==========

Register 08h – OTP Enable Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Soft_enable (RW)	Soft_down (RW)	Soft_standby (RW)	Test_enable (RW)	Select_alert (RW)	No_wk_map (RW)	User_unlock (RW)	Otp_enable (RW)

Default value is 8’h00.

Bit7 (soft_enable): Enable software control, enable “soft_dischg_enable”, “soft_chg_enable”, “tscan_enable”, “no_wk_map”, “user_unlock” and “soft_down” register function.

Bit6 (soft_down): Software power down, software requests power down by writing “1” when software_enable is “1”. When read-out, “0” is always returned

Bit5 (soft_standby): Software standby, software requests standby by writing “1” when software_enable is “1”. When read-out, “0” is always returned

Bit4 (test_enable): Enable test mode. Test mode is enabled by setting “1”.

Bit3 (select_alert): Select alert function of PF/ALERTN pin. If select_alert is “1” and soft_enabel is “1”, select alert function; otherwise, select pf function.

Bit2 (no_wk_map): No wakeup mapping, the OTP mapping is not exectuted when wakeup if this bit is “1” when soft_enable is “1”; otherwise, the OTP mapping is executed when wakeup.

Bit1 (user_unlock): User unlock, permit to write the frozen user data (user_freeze = 1) if this bit is “1” when software_enable is “1”.

Bit0 (otp_enable): OTP check enable, check otp_mode register bit only when this bit is “1”. When this bit is “0”, the otp_mode will be ignored and the OTP access is prohibited.
==========

Register 09h – FET Disable Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Pf (R)	Sc_fet_disable (R)	Oc_fet_disable (R)	Ub_fet_disable (R)	Ut_fet_disable (R)	Ot_fet_disable (R)	Uv_fet_disable (R)	Ov_fet_disable (R)

Default value is 8'h01.

Bit7 (pf): PF set to "1" due to ovpf, cell_otpf, fet_otpf, int_otpf or adc_pf.

Bit6 (sc_fet_disable): Confirmed SC set to "1" when SC set, cleared to "0" by SC release.

Bit5 (oc_fet_disable): Confirmed OC set to "1" by OC set, cleared to "1" by OC release.

Bit4 (ub_fet_disable): Confimed UB set to "1" by UB set, cleared to "0" by UB release.

Bit3 (ut_fet_disable): Confirmed UT set to "1" by UT set, cleared to "0" by UT release.

Bit2 (ot_fet_disable): Confirmed CHG_OT or DSG_OT set to "1" by OT set, cleared to "0" by OT release.

Bit1 (uv_fet_disable): Confirmed UV set to "1" by UV set, cleared to "0" by UV release.

Bit0 (ov_fet_disable): Confirmed OV, set to "1" by OV set, cleared to "0" by OV release. For the safety consideration, default ov_fet_disable is "1".

==========

Register 0ah – Mode Change Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved (R)	Mode_timeout (R)	Next_mode1 (R)	Next_mode0 (R)	reserved (R)	Pf_type2 (R)	Pf_type1 (R)	Pf_type0 (R)

Default value is 8'h00.

Bit7: Reserved.

Bit6 (mode_timeout): When mode_event is set to "1", OZ8930 wait for MCU to clear it or a 256ms time out is detected. If the time out is detected, this bit is set to "1" and cleared by MCU writing "1".

Bit5_Bit4 (next_mode1 – next_mode0): OZ8930's next working mode.

next_mode1: next_mode0	OZ8930's next working mode
00	Full power mode
01	Sleep mode
10	Stand by mode
11	Power down mode

Bit3 (reserved): Reserved.

Bit2_Bit0 (pf_type2 – pf_type0): Confirmed CHG_OT or DSG_OT set to "1" by OT set, cleared to "0" by OT release.

pf_type2 : pf_type0	Pf type
001	Ov_pf
010	cell_ot_pf
011	fet_ot_pf
100	int_ot_pf
101	adc_pf

==========

Register 0bh – Reserved Register

Reserved for future use

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Register 0ch & 0dh – Max Cell Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0ch	Max_cell_data3 (R)	Max_cell_data2 (R)	Max_cell_data1 (R)	Max_cell_data0 (R)	Reserved (R)	Max_cell_channel2 (R)	Max_cell_channel1 (R)	Max_cell_channel0 (R)
0dh	Max_cell_data11 (R)	Max_cell_data10 (R)	Max_cell_data9 (R)	Max_cell_data8 (R)	Max_cell_data7 (R)	Max_cell_data6 (R)	Max_cell_data5 (R)	Max_cell_data4 (R)

Default value is 8'h00.

Max_cell_data11 – max_cell_data0: 12-bit max voltage cell data in 2's complement format with 2.44mV LSB.

Max_cell_channel2 – max_cell_channel0: max voltage cell's channel number.

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Register 0eh – Reserved Register

Reserved for future use

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Register 0fh –12: Reserved for chip vendor use only

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Register 13h – Scan Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Prty_chk (RW)	Reserved	Auto_scan (RW)	Currt_scan (RW)	Tm_scan1 (RW)	Tm_scan0 (RW)	Cell_num1 (RW)	Cell_num0 (RW)

Default value is 8'h00.

Bit7 (prty_chk): Even parity check bit. When writing this register, the software needs to count the number of "1" in the bit6~bit0. If the number of "1" is even, this bit should be set to "0"; if the number of "1" is odd, this bit should be set to "1". When OZ8930 finds this bit doesn't meet the above even parity check rule, it will generate an internal reset.

Bit6: Reserved. **Note:** Only "0" can be written into this bit. Writing "1" into this bit is prohibited.

Bit5 (auto_scan): Auto scan selection: "0": select trigger scan mode; "1": select auto scan mode.

Bit4 (currt_scan): Current channel scan enable, enable current channel scan by setting "1".

Bit3_Bit2 (tm_scan1 – tm_scan0): Thermal channel therm1 and therm2 scan enable selection:

tm_scan1 : tm_scan0	Thermal scan
00	disable therm2 scan, disable therm1 scan (therm2 is digital pin, therm1 is digital pin)
01	disable therm2 scan, enable therm1 scan (therm2 is digital pin, therm1 is analog pin)
10	**Note:** This setting is disabled to be used.
11	enable therm2 scan, enable therm1 scan (therm2 is analog pin, therm1 is analog pin)

Bit1_Bit0 (cell_num1 – cell_num0): Cell number in the battery pack.

cell_num1 : cell_num0	cell number in the battery pack
00	3 cells
01	4 cells

10	5 cells
11	6 cells

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Register 14h – I²C Addr Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved (R)	reserved (R)	reserved (R)	reserved (R)	reserved (R)	reserved (R)	I²C_addr1 (RW)	I²C_addr0 (RW)

Default value is 8'h00.

Bit7_Bit2: Reserved.

Bit1_Bit0 (I²C_addr1 – I²C_addr0): Specify the 8-bit I²C device address as 8'h60 + 2*N. Here, N is specified by I²C_addr1 – I²C_addr0.

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Register 15h – COC TH Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Coc_mid_t_th3 (RW)	Coc_mid_t_th2 (RW)	Coc_mid_t_th1 (RW)	Coc_mid_t_th0 (RW)	Coc_low_t_th3 (RW)	Coc_low_t_th2 (RW)	Coc_low_t_th1 (RW)	Coc_low_t_th0 (RW)

Default value is 8'h00.

Bit7_Bit4 (coc_mid_t_th3 – coc_mid_t_th0): Charge over current threshold for temperature T2~T3. Refer to the section Over-current (OC).

Bit3_Bit0 (coc_low_t_th3 – coc_low_t_th0): Charge over current threshold for under T2 temperature.

==========

Register 16h – COC Time Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Coc_high_t_th3 (RW)	Coc_high_t_th2 (RW)	Coc_high_t_th1 (RW)	Coc_high_t_th0 (RW)	Coc_release1 (RW)	Coc_release0 (RW)	Coc_delay1 (RW)	Coc_delay0 (RW)

Default value is 8'h00.

Bit7_Bit4 (coc_high_t_th3 – coc_high_t_th0): Charge over current threshold for over T3 temperature.

Bit3_Bit2 (coc_release1 – coc_release0): Charge over current release control.

Bit1_Bit0 (coc_delay1 – coc_delay0): Charge over current delay control.

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Register 17h – DOC0 TH Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved (R)	reserved (R)	Doc0_th5 (RW)	Doc0_th4 (RW)	Doc0_th3 (RW)	Doc0_th2 (RW)	Doc0_th1 (RW)	Doc0_th0 (RW)

Default value is 8'h00.

Bit7_Bit6: Reserved.

Bit5_Bit0 (doc0_th5 – doc0_th0): Used to specify Level-0 discharge over current threshold. The real threshold can be calculated by the following formula:

DOC0 = (N+M)*5mv (start value: 30mv, step: 5mv).

Here N is specified by doc0_th5 – doc0_th0; M is specified by 4-bit DOC0 offset (-6~+6) stored in OTP. Then we can get the following:
DOC0 = (N+6)*5mv (N: 0~63) @M=6 (DOC0 offset is 30mv) → the range is in 30mv~345mv;
DOC0 = (N-6)*5mv (N: 12~63) @M=-6 (DOC0 offset is -30mv) → the range is in 30mv~285mv.

It is noted that DOC0 is in the range 30mv~285mv in any case.
==========

Register 18h – DOC0 Time Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved (R)	reserved (R)	Doc0_release1 (RW)	Doc0_release0 (RW)	Doc0_delay3 (RW)	Doc0_delay2 (RW)	Doc0_delay1 (RW)	Doc0_delay0 (RW)

Default value is 8'h00.

Bit7_Bit6: Reserved.

Bit5_Bit4 (doc0_release1 – doc0_release0): Level-0 discharge over current release control.

Bit3_Bit0 (doc0_delay3 – doc0_delay0): Level-0 discharge over current delay control.
==========

Register 19h – DOC1 TH Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved (R)	reserved (R)	Doc1_th5 (RW)	Doc1_th4 (RW)	Doc1_th3 (RW)	Doc1_th2 (RW)	Doc1_th1 (RW)	Doc1_th0 (RW)

Default value is 8'h00.

Bit7_Bit6: Reserved.

Bit5_Bit0 (doc1_th5 – doc1_th0): Used to specify Level-1 discharge over current threshold. The real threshold can be calculated by the following formula:

DOC1 = (N+M+2)*10mv (start value: 50mv, step: 10mv).

Here N is specified by doc1_th5 – doc1_th0; M is specified by 4-bit DOC1 offset (-3~+3) stored in OTP. Then we can get the following:
DOC1 = (N+5)*10mv (N: 0~63) @M=3 (DOC1 offset is 30mv) → the range is in 50mv~680mv;
DOC1 = (N-1)*10mv (N: 6~63) @M=-3 (DOC1 offset is -30mv) → the range is in 50mv~620mv.

It is noted that DOC1 is in the range 50mv~620mv in any case.
==========

Register 1ah – DOC1 Time Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved (R)	reserved (R)	Doc1_release1 (RW)	Doc1_release0 (RW)	Doc1_delay3 (RW)	Doc1_delay2 (RW)	Doc1_delay1 (RW)	Doc1_delay0 (RW)

Default value is 8'h00.

Bit7_Bit6: Reserved.

Bit5_Bit4 (doc0_release1 – doc0_release0): Level-1 discharge over current release control.

Bit3_Bit0 (doc0_delay3 – doc0_delay0): Level-1 discharge over current delay control.
==========

Register 1bh – SC Time Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Dischg_th1 (RW)	Dischg_th0 (RW)	Chg_th1 (RW)	Chg_th0 (RW)	Sc_release 1 (RW)	Sc_release0 (RW)	Sc_delay1 (RW)	Sc_delay0 (RW)

Default value is 8'h00.

Bit7_Bit6: Specify the discharge threshold. (Considering current ADC's LSB: 15.3uV, 6.12mA@2.5mohm). When the current (signed value) < the discharge threshold (signed value), the chip is in discharge state (in_discharge=1); otherwise, the chip is not in discharge state (in_discharge = 0).

Dischg_th1 : dischg_th0	the discharge threshold
00→8	-48.8mA
01→16	-97.7mA
10→32	-195.3mA
11→64	-390.6mA

Bit5_Bit4 (chg_th1 – chg_th0): Specify the charge threshold as following (Considering current ADC's LSB: 15.3uV, 7.7mA@2mohm). When the current (signed value) > the charge threshold (signed value), the chip is in charge state (in_charge = 1); otherwise, the chip is not in charge state (in_charge = 0).

chg_th1 : chg_th0	the charge threshold
00→8	48.8mA
01→16	97.7mA
10→32	195.3mA
11→64	390.6mA

Bit3_Bit2 (sc_release1 – sc_release0): Short circuit release control. Refer to SC (Short Circuit) Control Table.

Bit1_Bit0 (sc_delay1 – sc_delay0): Short circuit delay control. Refer to SC (Short Circuit) Control Table.
==========

Register 1ch – Safety Time Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Tm2_fet_ot_sel (R)	Tm2_fet (RW)	Ub_delay1 (RW)	Ub_delay0 (RW)	Ot_ut_delay 1 (RW)	Ot_ut_delay 0 (RW)	Ov_delay1 (RW)	Ov_delay0 (RW)

Default value is 8'h00.

Bit7 (tm2_fet_ot_sel): When TM2 is FET temperature, if tm2_fet_ot_sel = "1", check OT and release on TM2; if tm2_fet_ot_sel = "0", check OTPF on TM2.

Bit6 (tm2_fet): TM2 is FET temperature. If tm2_fet is 0, TM1, TM2 both are battery cell tube skin temperature; if tm2_fet is "1", TM1 is battery cell tube skin temperature and TM2 is FET temperature.

Bit5_Bit4 (ub_delay1 – ub_delay0): Cell unbalance delay control.

Ub_delay1 : ub_delay0	Cell unbalance delay
00	2 scan cycles
01	4 scan cycles
10	6 scan cycles
11	8 scan cycles

Bit3_Bit2 (ot_ut_delay1 – ot_ut_delay0): Over temperature, under temperature delay control.

ot_ut_delay1 : ot_ut_delay0	Over temperature, under temperature delay
00	2 scan cycles
01	4 scan cycles
10	6 scan cycles
11	8 scan cycles

Bit1_Bit0 (ov_delay1 – ov_delay0): Over voltage delay control.

uv_delay1 : ov_delay0	Over voltage delay
00	2 scan cycles
01	4 scan cycles
10	8 scan cycles
11	16 scan cycles

==========

Register 1dh – ADC PF Delay Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
uv_delay1 (RW)	uv_delay0 (RW)	reserved (R)	reserved (R)	pf_ignr_shrt (RW)	Adc_pf_delay2 (RW)	Adc_pf_delay1 (RW)	Adc_pf_delay0 (RW)

Default value is 8'h00.

Bit7_Bit6 (uv_delay1 – uv_delay0): Under voltage delay control.

uv_delay1 : uv_delay0	Under voltage delay
00	2 scan cycles
01	4 scan cycles
10	8 scan cycles
11	16 scan cycles

Bit5_Bit4: Reserved.

Bit3 (pf_ignr_shrt): During the battery assembly, it is possible that the unexpected OVPF occurs. OZ8930 will ignore the unexpected OVPF during the assembly time. This bit defines the assembly time: if "1", set the short assembly time as 32s; if "0", set the long assembly time as 64s.

Bit2_Bit0 (adc_pf_delay2 – adc_pf_delay0): ADC_PF delay control.

Adc_pf_delay2 : adc_pf_delay0	ADC_PF delay
000	Disable adc_pf check
001	2 scan cycles
010	3 scan cycles
011	4 scan cycles
100	5 scan cycles
101	6 scan cycles
110	7 scan cycles
111	8 scan cycles

==========

Register 1eh – Bleeding Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ov_out_ enable	uv_out_ enable	ot_out_ enable	ut_out_ enable	Bld_support (RW)	Bld_idle (RW)	Bld_accurac y1 (RW)	Bld_accuracy 0 (RW)

Default value is 8'h00.

Bit7_Bit4: When efetc_mode[2:0] = 3'b101, enable to output the corresponding xx_fet_disable on EFETC pin. The output = (ov_fet_disable & ov_out_enable) | (uv_fet_disable & uv_out_enable) | (ot_fet_disa ble & ot_out_enable) | (ut_fet_disable & ut_out_enable).

Bit3 (bld_support): Bleeding support, support bleeding function by setting "1".

Bit2 (bld_idle)：Eable idle/OV bleeding, allow bleeding in idle state (no charge current, no discharge current) and OV (over voltage) state when it is "1"; stop bleeding in idle state or OV state when it is "0".

Bit1_Bit0 (bld_accuracy1 – bld_accuracy0): Bleeding Accuracy control.

Bld_accuracy1 : bld_accuracy0	Bleeding Accuracy control
00	9.76mV
01	19.5mV
10	29.3mV
11	39.0mV

==========

Register 1fh – Sleep Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
User_freeze (RW)	Efetc_mode 2 (RW)	Efetc_mode 1 (RW)	Efetc_mode 0 (RW)	reserved (R)	reserved (R)	Sleep_suppo rt (RW)	Sleep_time (RW)

Default value is 8'h00.

Bit7 (user_freeze): User data frozen, the user data (reg13h~reg1fh) is frozen to write by setting "1" unless user_unlock is "1".

Bit6_Bit4 (efetc_mode2 – effect_mode0): EFETC pin function mode as following.

Efect_mode2 : efetc_mode0	EFETC pin function mode as following
000	High active input to forcibly disable charge FET.
001	High active input to forcibly disable discharge FET.
010	High active input to forcibly disable charge FET and discharge FET.
011	Output discharge FET status.
100	High active input as external standby.
101	Output internal xx_fet_disable signal. xx_fet_disable = (ov_fet_disable & ov_out_enable)) | (uv_fet_disable & uv_out_enable) | (ot_fet_disable & ot_out_enable) | (ut_fet_disable & ut_out_enable).
110, 111	Reserved

Bit3_Bit2：Reserved.

Bit1 (sleep_support): Sleep function support by setting "1".

Bit0 (sleep_time): Sleep time control, select 1-minute sleep time by setting "0"; select 4-minute sleep time by setting "1"

==========

Register 20h ~ 21h –Under Temperature Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20h	ut_th[3]	ut_th[2]	ut_th[1]	ut_th[0]	reserved	reserved	reserved	reserved
21h	ut_th[11]	ut_th[10]	ut_th[9]	ut_th[8]	tu_th[7]	ut_th[6]	ut_th[5]	ut_th[4]

These two registers set under temperature threshold for battery cell tube sink, 1.22mV LSB, 2's complement format.

==========

Register 22h ~ 23h – Under Temperature Release Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
22h	ut_rl[3]	ut_rl[2]	ut_rl[1]	ut_rl [0]	reserved	reserved	reserved	reserved
23h	ut_rl[11]	ut_rl[10]	ut_rl[9]	ut_rl [8]	tu_rl[7]	ut_rl[6]	ut_rl[5]	ut_rl[4]

These two registers set under temperature release for battery cell tube sink, 1.22mV LSB, 2's complement format.

==========

Register 24h ~ 25h – Charge Temperature Point2 Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
24h	Chg_t2[3]	Chg_t2[2]	Chg_t2[1]	Chg_t2[0]	reserved	reserved	reserved	reserved
25h	Chg_t2[11]	Chg_t2[10]	Chg_t2[9]	Chg_t2[8]	Chg_t2[7]	Chg_t2[6]	Chg_t2[5]	Chg_t2[4]

These two registers set charge temperature point2 for battery cell tube sink, 1.22mV LSB, 2's complement format.

==========

Register 26h ~ 27h – Charge Temperature Point3 Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
26h	Chg_t3[3]	Chg_t3[2]	Chg_t3[1]	Chg_t3[0]	reserved	reserved	reserved	reserved
27h	Chg_t3[11]	Chg_t3[10]	Chg_t3[9]	Chg_t3[8]	Chg_t3[7]	Chg_t3[6]	Chg_t3[5]	Chg_t3[4]

These two registers set charge temperature point3 for battery cell tube sink, 1.22mV LSB, 2's complement format.

==========

Register 28h ~ 29h – Charge over Temperature and release Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
28h	Chg_ot[3]	Chg_ot[2]	Chg_ot[1]	Chg_ot[0]	Chg_ot_rl _delta[3]	Chg_ot_rl _delta[2]	Chg_ot_rl _delta[1]	Chg_ot_rl _delta[0]
29h	Chg_ot[11]	Chg_ot[10]	Chg_ot[9]	Chg_ot[8]	Chg_ot[7]	Chg_ot[6]	Chg_ot[5]	Chg_ot[4]

These two registers set charge over temperature for battery cell tube sink, 1.22mV LSB, 2's complement format.

Reg28h_Bit3 – Reg28h_Bit0 (chg_ot_rl_delta[3] – chg_ot_rl_delta[0]) : Charge over temperature release delta, 1.22mV LSB, 2's complement format. (Charge ot release = charge_ot + chg_ot_rl_delta)

==========

Register 2ah ~ 2bh – Discharge over Temperature and release Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2ah	dsg_ot[3]	dsg_ot[2]	dsg_ot[1]	dsg_ot[0]	dsg_ot_rl _delta[3]	dsg_ot_rl _delta[2]	dsg_ot_rl _delta[1]	dsg_ot_rl _delta[0]
2bh	dsg_ot[11]	dsg_ot[10]	dsg_ot[9]	dsg_ot[8]	dsg_ot[7]	dsg_ot[6]	dsg_ot[5]	dsg_ot[4]

These two registers set discharge over temperature for battery cell tube sink, 1.22mV LSB, 2's complement format.

Reg2ah_Bit3 – Reg28h_Bit0 (dsg_ot_rl_delta[3] – dsg_ot_rl_delta[0]) : Discharge over temperature release delta, 1.22mV LSB, 2's complement format. (Discharge ot release = discharge_ot + chg_ot_rl_delta)
==========

Register 2ch ~ 2dh – Low Temperature over Voltage Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2ch	Low_t_ov [3]	Low_t_ov [2]	Low_t_ov [1]	Low_t_ov [0]	reserved	reserved	reserved	reserved
2dh	Low_t_ov [11]	Low_t_ov [10]	Low_t_ov [9]	Low_t_ov [8]	Low_t_ov [7]	Low_t_ov [6]	Low_t_ov [5]	Low_t_ov [4]

These two registers set low temperature over voltage threshold for under T2 temperature, 2.44mV LSB, 2's complement format; low_t_ovpf = low_ov + 41 (100mV).
==========

Register 2eh ~ 2fh – Middle Temperature over Voltage Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2eh	mid_t_ov [3]	mid_t_ov [2]	mid_t_ov[1]	mid_t_ov [0]	reserved	reserved	reserved	reserved
2fh	mid_t_ov [11]	mid_t_ov [10]	mid_t_ov[9]	mid_t_ov [8]	mid_t_ov[7]	mid_t_ov[6]	mid_t_ov[5]	mid_t_ov[4]

These two registers set middle temperature over voltage threshold for T2 ~ T3 temperature, 2.44mV LSB, 2's complement format; mid_t_ovpf = mid_ov + 41 (100mV).
==========

Register 30h ~ 31h – High Temperature over Voltage Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
30h	high_t_ov [3]	high_t_ov [2]	high_t_ov [1]	high_t_ov [0]	reserved	reserved	reserved	reserved
31h	high_t_ov [11]	high_t_ov [10]	high_t_ov [9]	high_t_ov [8]	high_t_ov [7]	high_t_ov [6]	high_t_ov [5]	high_t_ov [4]

These two registers set high temperature over voltage threshold for voerT3 temperature, 2.44mV LSB, 2's complement format; high_t_ovpf = high_ov + 41 (100mV).
==========

Register 32h ~ 33h – Cell Unbalance Threshold and Release Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
32h	Ub[3]	Ub[2]	Ub[1]	Ub[0]	Ub_rl_del ta[3]	Ub_rl_del ta[2]	Ub_rl_del ta[1]	Ub_rl_del ta[0]
33h	Ub[11]	Ub[10]	Ub[9]	Ub[8]	Ub[7]	Ub[6]	Ub[5]	Ub[4]

These two registers set cell unbalance threshold, 2.44mV LSB, 2's complement format.

Reg32h_Bit3 – Reg32h_Bit0 (ub_rl_delta[3] – ub_rl_delta[0]) : cell unbalance release delta, 2.44*16mV LSB, 2's complement format. (ub release = ub + ubt_rl_delta*16)
==========

Register 34h ~ 35h – Under Voltage Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
34h	uv [3]	uv [2]	uv[1]	uv [0]	reserved	reserved	reserved	reserved
35h	uv[11]	uv[10]	uv[9]	uv [8]	uv[7]	uv[6]	uv[5]	uv[4]

These two registers set under voltage threshold, 2.44mV LSB, 2's complement format.
==========

Register 36h ~ 37h – Over Temperature PF Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
36h	Int_otpf_th [3]	Int_otpf_th [2]	Int_otpf_th [1]	Int_otpf_th [0]	reserved	reserved	reserved	reserved
37h	Int_otpf_th [11]	Int_otpf_th [10]	Int_otpf_th [9]	Int_otpf_th [8]	Int_otpf_th [7]	Int_otpf_th [6]	Int_otpf_th [5]	Int_otpf_th [4]

These two registers set over temperature PF threshold for internal temperature, 1.22mV LSB, 2's complement format.

==========

Register 38h ~ 39h – Over Temperature PF Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
38h	cell_otpf [3]	cell_otpf [2]	cell_otpf [1]	cell_otpf [0]	reserved	reserved	reserved	reserved
39h	cell_otpf [11]	cell_otpf [10]	cell_otpf [9]	cell_otpf [8]	cell_otpf [7]	cell_otpf [6]	cell_otpf [5]	cell_otpf [4]

These two registers set over temperature PF threshold for battery cell tube sink, 1.22mV LSB, 2's complement format.

==========

Register 3ah ~ 3bh – MOSFET Over Temperature PF Threshold and Release Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3ah	Fet_ot/fet_ otpf[3]	Fet_ot/fet_ otpf[2]	Fet_ot/fet _otpf[1]	Fet_ot/fet_ otpf[0]	Fet_ot_d elta[3]	Fet_ot_d elta[2]	Fet_ot_de lta[1]	Fet_ot_d elta[0]
3bh	Fet_ot/fet_ otpf[11]	Fet_ot/fet_ otpf[10]	Fet_ot/fet _otpf[9]	Fet_ot/fet_ otpf[8]	Fet_ot/fet _otpf[7]	Fet_ot/fet _otpf[6]	Fet_ot/fet _otpf[5]	Fet_ot/fet _otpf[4]

These two registers set over temperature or over temperature PF threshold for MOSFET, 1.22mV LSB, 2's complement format.

Reg3ah_Bit3 – Reg3ah_Bit0 fet_ot_delta[3] – fet_ot_delta[0]) : FET over temperature release delta, 1.22mV LSB, 2's complement format. (fet ot release = fet_otpf +fet_ot_delta)

==========

Register 3ch ~ 3dh – Bleeding Star Point Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3ch	Bld_start[3]	Bld_start [2]	Bld_start [1]	Bld_start [0]	reserved	reserved	reserved	reserved
3dh	Bld_start [11]	Bld_start [10]	Bld_start [9]	Bld_start [8]	Bld_start [7]	Bld_start [6]	Bld_start [5]	Bld_start [4]

These two registers set bleeding start point, 2.44mV LSB, 2's complement format.

==========

Register 3eh – Over Voltage Release Hysteresis Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	reserved	Ov_hys[5]	Ov_hys[4]	Ov_hys[3]	Ov_hys[2]	Ov_hys[1]	Ov_hys[0]

Bit5_Bit0 (ov_hys[5] – ov_hys[0]): Over voltage release hysteresis, 2.44*4mV LSB, 2's complement format, theory range: -312.3mV ~ +302.56mV; application range: -312.3mV ~ 0mV.
Ov release = ov threshold + ov_hys*4.

==========

Register 3fh –Under Voltage Release Hysteresis Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	reserved	uv_hys[5]	uv_hys[4]	uv_hys[3]	uv_hys[2]	uv_hys[1]	uv_hys[0]

Bit5_Bit0 (uv_hys[5] – uv_hys[0]): Under voltage release hysteresis, 2.44*16mV LSB, 2's complement format, theory range: -1249mV ~ +1210mV; application range: 0mV ~ +1210mV.
uv release = uv threshold + uv_hys*16.
==========

Register 40h ~ 4bh – Cell1~Cell6 Data Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
40h	Cell1_data [3]	Cell1_data [2]	Cell1_data [1]	Cell1_data [0]	reserved	reserved	reserved	Cell1 offset flag
41h	Cell1_data [11]	Cell1_data [10]	Cell1_data [9]	Cell1_data [8]	Cell1_data [7]	Cell1_data [6]	Cell1_data [5]	Cell1_data [4]
42h	Cell2_data [3]	Cell2_data [2]	Cell2_data [1]	Cell2_data [0]	reserved	reserved	reserved	Cell2 offset flag
43h	Cell2_data [11]	Cell2_data [10]	Cell2_data [9]	Cell2_data [8]	Cell2_data [7]	Cell2_data [6]	Cell2_data [5]	Cell2_data [4]
44h	Cell3_data [3]	Cell3_data [2]	Cell3_data [1]	Cell3_data [0]	reserved	reserved	reserved	Cell3 offset flag
45h	Cell3_data [11]	Cell3_data [10]	Cell3_data [9]	Cell3_data [8]	Cell3_data [7]	Cell3_data [6]	Cell3_data [5]	Cell3_data [4]
46h	Cell4_data [3]	Cell4_data [2]	Cell4_data [1]	Cell4_data [0]	reserved	reserved	reserved	Cell4 offset flag
47h	Cell4_data [11]	Cell4_data [10]	Cell4_data [9]	Cell4_data [8]	Cell4_data [7]	Cell4_data [6]	Cell4_data [5]	Cell4_data [4]
48h	Cell5_data [3]	Cell5_data [2]	Cell5_data [1]	Cell5_data [0]	reserved	reserved	reserved	Cell5 offset flag
49h	Cell5_data [11]	Cell5_data [10]	Cell5_data [9]	Cell5_data [8]	Cell5_data [7]	Cell5_data [6]	Cell5_data [5]	Cell5_data [4]
4ah	Cell6_data [3]	Cell6_data [2]	Cell6_data [1]	Cell6_data [0]	reserved	reserved	reserved	Cell6 offset flag
4bh	Cell6_data [11]	Cell6_data [10]	Cell6_data [9]	Cell6_data [8]	Cell6_data [7]	Cell6_data [6]	Cell6_data [5]	Cell6_data [4]

Store the calibrated cell1~cell6's 12-bit ADC data or corresponding cell offset in 2's complement format with 2.44mV LSB. When the corresponding offset flag is "0", it is the cell1~cell6's ADC data; when the corresponding offset flag is "1", it is the cell1~cell6's offset ADC data.
==========

Register 4ch ~ 4dh – INT Data Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4ch	Int_data [3]	Int_data [2]	Int_data [1]	Int_data [0]	reserved	reserved	reserved	Cell6 high offset flag
4dh	Int_data [11]	Int_data [10]	Int_data [9]	Int_data [8]	Int_data [7]	Int_data [6]	Int_data [5]	Int_data [4]

Store the internal temperature's 12-bit ADC data or cell6 high offset in 2's complement format with 1.22mV LSB. When cell6 high offset flag is "0", it is the internal temperature ADC data; when cell6 high offset flag is "1", it is the cell6 high side offset ADC data.
==========

Register 4eh ~ 51h – TM1, TM2 Data Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4eh	Tm1_data [3]	Tm1_data [2]	Tm1_data [1]	Tm1_data [0]	reserved	reserved	reserved	reserved
4fh	Tm1_data [11]	Tm1_data [10]	Tm1_data [9]	Tm1_data [8]	Tm1_data [7]	Tm1_data [6]	Tm1_data [5]	Tm1_data [4]
50h	Tm2_data [3]	Tm2_data [2]	Tm2_data [1]	Tm2_data [0]	reserved	reserved	reserved	reserved
51h	Tm2_data [11]	Tm2_data [10]	Tm2_data [9]	Tm2_data [8]	Tm2_data [7]	Tm2_data [6]	Tm2_data [5]	Tm2_data [4]

Store the calibrated external temperature1, external temperature2's 12-bit ADC data in 2's complement format with 1.22mV LSB.

==========

Register 52h, 53h – Current Data Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
52h	current_data[5]	current_data [4]	current_data [3]	current_data [2]	current_data [1]	current_data [0]	reserved	reserve
53h	current_data [13]	current_data [12]	current_data [11]	current_data [10]	current_data [9]	current_data [8]	current_data [7]	current_data [6]

Store the calibrated current's 14-bit ADC data in 2's complement format with 15.3uv (7.7mA@2mohm) LSB.

==========

Register 54h – Group1 Offset Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Group1_offset[7]	Group1_offset [6]	Group1_offset [5]	Group1_offset [4]	Group1_offset [3]	Group1_offset [2]	Group1_offset [1]	Group1_offset [0]

Store the group1's 8-bit offset in 2's complement format with 2.44mV LSB for the cell1, 2, 3's ADC auto calibration. The range is -312mV~310mV.

==========

Register 55h – Group2 Offset Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Group2_offset[7]	Group2_offset [6]	Group2_offset [5]	Group2_offset [4]	Group2_offset [3]	Group2_offset [2]	Group2_offset [1]	Group2_offset [0]

Store the group2's 8-bit offset in 2's complement format with 2.44mV LSB for the cell4, 5, 6's ADC auto calibration. The range is -312mV~310mV.

==========

Register 56h, 57h – Current Offset Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
56h	current_offset[3]	current_offset [2]	current_offset [1]	current_offset [0]	reserved	reserve	reserved	reserve
57h	current_offset[11]	current_offset[10]	current_offset[9]	current_offset[8]	current_offset[7]	current_offset[6]	current_offset[5]	current_offset[4]

Store the current's 12-bit offset in 2's complement format with 15.3uv (7.7mA@2mohm) LSB. The range is -31.3mV~+31.3mV.

==========

Register 58h, 59h – Ref18 Data Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
58h	Ref18_data[3]	Ref18_data[2]	Ref18_data[1]	Ref18_data[0]	reserved	reserve	reserved	reserve
59h	Ref18_data[11]	Ref18_data[10]	Ref18_data[9]	Ref18_data[8]	Ref18_data[7]	Ref18_data[6]	Ref18_data[5]	Ref18_data[4]

Store the reference 1.8v's 12-bit ADC data in 2's complement format with 1.22mV LSB.
==========

Register 5ah – OV/UV Timer Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Ov_timer[3] (R)	Ov_timer[2] (R)	Ov_timer[1] (R)	Ov_timer[0] (R)	Uv_timer[3] (R)	Uv_timer[2] (R)	Uv_timer[1] (R)	Uv_timer[0] (R)

Default value is 8'h00.

Bit7_Bit4 (ov_timer[3] – ov_timer[0]): OV down count delay or release timer.

Bit3_Bit0 (uv_timer[3] – uv_timer[0]):UV down count delay or release timer.
==========

Register 5bh – OT/UT Timer Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ot_timer[3] (R)	ot_timer[2] (R)	ot_timer[1] (R)	ot_timer[0] (R)	ut_timer[3] (R)	ut_timer[2] (R)	ut_timer[1] (R)	ut_timer[0] (R)

Default value is 8'h00.

Bit7_Bit4 (ot_timer[3] – ot_timer[0]): OT down count delay or release timer.

Bit3_Bit0 (ut_timer[3] – ut_timer[0]): UT down count delay or release timer.
==========

Register 5ch – UB Timer Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved (R)	reserved (R)	reserved (R)	reserved (R)	ub_timer[3] (R)	ub_timer[2] (R)	ub_timer[1] (R)	ub_timer[0] (R)

Default value is 8'h00.

Bit7_Bit4: Reserved.

Bit3_Bit0 (ub_timer[3] – ub_timer[0]): UB down count delay or release time.
==========

Register 5dh – Test Mode 1 Register

Reserved for chip test (Writing this register is prohibited).
==========

Register 5eh – Test Mode 2 Register

Reserved for chip test (Writing this register is prohibited).
==========

Register 5fh –Test Mode 3 Register

Reserved for chip test (Writing this register is prohibited).
==========

OTP Registers

The OTP register are grouped into 2 sections: ATE data (OTP register 00h ~ 12h) and user data (OTP register 13h ~ 7fh). If **page_sel** (bit 6 in OTP register 13h) is "0", the default OTP page (OTP Registers 13h~3fh) will be mapped into the Operation Registers 13h~3fh; if **page_sel** is "1", the backup OTP page (OTP Registers 53h~7fh) will be mapped into Operation Registers 13h~3fh instead. Please refer to the application note "**OZ8930 AN-7: OTP Process Sequence**" for detailed OTP programming procedure.

OTP Registers Map

OTP registers 00h~0bh, 0dh~12h are reserved for chip vendor use only. 0ch is used to store the DOC offset value which is got at the ATE test stage.

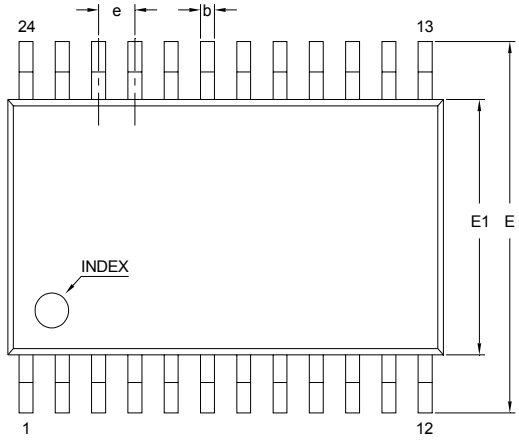
Reg index (hex)	Reg Name	Bit Number							
		7	6	5	4	3	2	1	0
00h-0bh	Reserved	Reserved for chip vendor use only							
0c	DOC offset	doc1_offset[3:0] (N*10mv limited in -30mv~+30mv, 2's complement format)				doc0_offset[3:0] (N*5mv limited in -30mv~+30mv, 2's complement format)			
0dh-12h	Reserved	Reserved for chip vendor use only							
13	Scan Control	prty_chk	page_sel	auto_scan	currt_scan	tm_scan[1:0]		cell_num[1:0]	
14	I²C Addr	Reserved						I²C_addr[1:0]	
15	COC TH	coc_mid_t_th[3:0]				coc_low_t_th[3:0]			
16	COC Time	coc_high_t_th[3:0]				coc_release[1:0]		coc_delay[1:0]	
17	DOC0 TH	Reserved		doc0_th[5:0]					
18	DOC0 Time	Reserved		doc0_release[1:0]		doc0_delay[3:0]			
19	DOC1 TH	Reserved		doc1_th[5:0]					
1a	DOC1 Time	Reserved		doc1_release[1:0]		doc1_delay[3:0]			
1b	SC Time	dischg_th[1:0]		chg_th[1:0]		sc_release[1:0]		sc_delay[1:0]	
1c	Safety Time	tm2_fet_ot_sel	tm2_fet	ub_delay[1:0]		ot_ut_delay[1:0]		ov_delay[1:0]	
1d	ADC_PF Time	uv_delay[1:0]		reserved		pf_ignr_shrt	adc_pf_delay[2:0]		
1e	Bleeding Control	ov_out_enable	uv_out_enable	ot_out_enable	ut_out_enable	bld_support	bld_idle	bld_accuracy[1:0]	
1f	Sleep Control	user_freeze	efetc_mode[2:0]			reserved		sleep_support	sleep_time
20	UT	ut_th[3:0]				reserved			
21		ut_th[11:4] (under temperature threshold for battery cell tube skin, 1.22mV LSB, 2's complement format)							
22	UT_RL	ut_rl[3:0]				reserved			
23		ut_rl[11:4] (under temperature release for battery cell tube skin, 1.22mV LSB, 2's complement format)							
24	CHG_T2	chg_t2[3:0]				reserved			

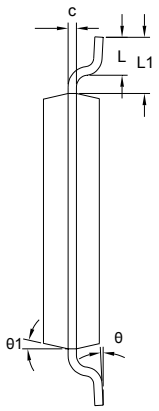
Reg index (hex)	Reg Name	Bit Number							
		7	6	5	4	3	2	1	0
25		chg_t2[11:4] (charge temperature point2 for battery cell tube skin, 1.22mV LSB, 2's complement format)							
26	CHG_T3	chg_t3[3:0]				reserved			
27		chg_t3[11:4] (charge temperature point3 for battery cell tube skin, 1.22mV LSB, 2's complement format)							
28	CHG_OT	chg_ot [3:0]				chg_ot_rl_delta[3:0] (charge over temperature release delta, 1.22mv LSB, 2's complement format) (charge ot relase = charge_ot + chg_ot_rl_delta)			
29		chg_ot [11:4] (charge over temperature for battery cell tube skin, 1.22mV LSB, 2's complement format)							
2a	DSG_OT	dsg_ot [3:0]				dsg_ot_rl_delta[3:0] (discharge over temperature release delta, 1.22mv LSB, 2's complement format) (discharge ot relase = discharge_ot + dischg_ot_rl_delta)			
2b		dsg_ot [11:4] (discharge over temperature for battery cell tube skin, 1.22mV LSB, 2's complement format)							
2c	LOW_T_OV	low_t_ov[3:0]				reserved			
2d		low_t_ov[11:4] (low-temperture over voltage threshold for under T2 temperature, 2.44mV LSB, 2's complement format; low_t_ovpf = low_ov + 41(100mV)							
2e	Mid_T_OV	mid_t_ov[3:0]				reserved			
2f		mid_t_ov[11:4] (middle-temperature over voltage threshold for T2~T3 temperature, 2.44mV LSB, 2's complement format; mid_t_ovpf = mid_ov + 41(100mV)							
30	High_T_OV	high_t_ov[3:0]				reserved			
31		high_t_ov[11:4] (high-temperature over voltage threshold for over T3 temperautre, 2.44mV LSB, 2's complement format; high_t_ovpf = high_t_ov + 41(100mV)							
32	UB	ub[3:0]				ub_rl_delta[3:0] (cell unbalance release delta, 2.44*16mv LSB, 2's complement format) (ub_release = ub + ub_rl_delta*16)			
33		ub[11:4] (cell unbalance threshold, 2.44mV LSB, 2's complement format)							
34	UV	uv[3:0]				reserved			
35		uv[11:4] (under vlotage threshold, 2.44mV LSB, 2's complement format)							
36	INT_OTPF	int_otpf_th[3:0]				reserved			
37		int_otpf_th[11:4] (over temperature PF threshold for internal temperature, 1.22mV LSB, 2's complement format)							
38	CELL_OTPF	cell_otpf[3:0]				reserved			
39		cell_otpf[11:4] (over temperature PF threshold for battery cell tube skin, 1.22mV LSB, 2's complement format)							
3a	FET_OT/ FET_OTPF	fet_ot/fet_otpf[3:0]				fet_ot_delta[3:0] (FET over temperature release delta, 1.22mv LSB, 2's complement format) (fet ot relase = fet_ot + fet_ot_delta)			
3b		fet_ot/fet_otpf[11:4] (Over temperature / over temperature PF threshold for MOSFET, 1.22mV LSB, 2's complement format)							
3c	Bld Start	bld_start[3:0]				reserved			
3d		bld_start[11:4] (bleeding start poin, 2.44mV, 2's complement format)							

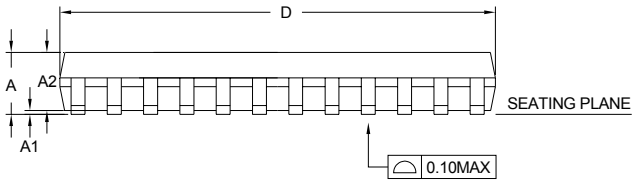
Reg index (hex)	Reg Name	Bit Number							
		7	6	5	4	3	2	1	0
3e	ov_hysteresis	reserved		ov_hys[5:0] (over voltage release hysteresis, 2.44*4mv LSB, 2's complement format; theory range: -312.3mv ~ +302.56, application range: -312.3mv ~ 0m)(ov release = ov threshold + ov_hys*4)					
3f	uv_hysteresis	reserved		uv_hys[5:0] (under voltage release hysteresis, 2.44*16mv LSB, 2's complement format; theory range: -1249mv ~ +1210mv, application range: 0 ~ +1210mv)(uv release = uv threshold + uv_hys*16)					
40~41	Rsense	2-byte Rsense value used by software.							
42~4f	Reserved	reserved							
53~7f	Backup	Backup for reg13h~3fh. When **page_sel** = 0, 13h~3fh will be used to control the chip; when **page_sel** = 1, 53h~7fh will be used to control the chip. **Note:** Bit 6 in OTP register 53h should be always written "0". (Writing "1" into the bit is prohibited).							

PACKAGE INFORMATION

24L TSSOP 173mil Package Outline Drawing



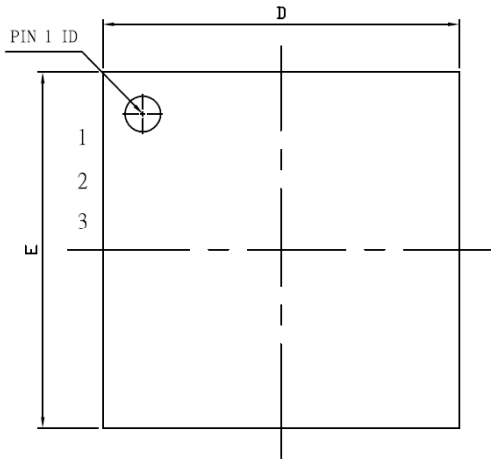




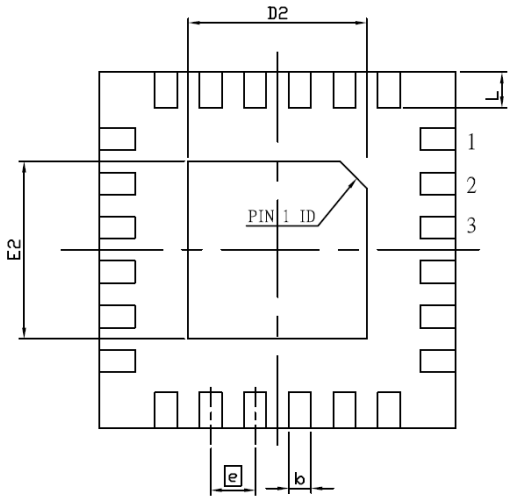
SYMBOL	DIMENSION (MM)		
	MIN	NOR	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	7.70	7.80	7.90
E	6.40 BSC		
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	-	8°
θ1	12 REF		

NOTE:
1. REFER TO JEDEC STD MO-153 AD
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE

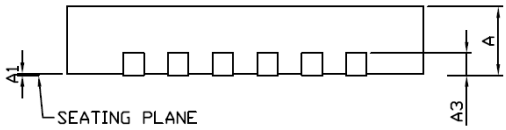
24Ld QFN 4x4mm Package Outline Drawing



TOP VIEW



BOTTOM VIEW



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.203 REF		
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	1.90	2.00	2.10
E	3.90	4.00	4.10
E2	1.90	2.00	2.10
e	0.50 BSC		
L	0.30	0.40	0.50

Notes:
1. ALL DIMENSIONS ARE IN MILLIMETER
2. REFER TO JEDEC STD MO-220

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