RICOH

Li-ION/POLYMER 3/4/5-CELL PROTECTOR

R5432Vxxxxx SERIES

Preliminary

EA-263 -11605

OVERVIEWS

The R5432V Series are high voltage CMOS-based process protection ICs against over-charge, over-discharge, and over current of Li-ion/Li polymer secondary batteries. The R5432V series can detect over-charge voltage and excess charge current, over-discharge voltage and excess discharge current of 3,4,or 5-stacked cells
of Li-ion/Li polymer batteries. The R5432VXXXXX consists of voltage detectors, a short detector, reference units, an oscillator, counters, delay circuits, logic circuits. The output type of COUT pin is Pch open drain, and DOUT is CMOS.

When the over-charge voltage or current is detected, after the IC internally prefixed delay time, the output of COUT becomes "Hi-Z". When the over-discharge voltage or excess discharge current is detected, after the setting delay time by an external capacitor, the output of DOUT becomes "L". When the short circuit is detected, after the IC internally prefixed delay time, the output of DOUT becomes "L".

After detecting over-charge, when the cell voltage becomes lower than the over-charge released voltage, the over-charge state is released and the output of COUT becomes "H". While after detecting over-charge current, after disconnecting the charger and connecting a load, then the over-charge current state is released, the output of COUT becomes "H". After detecting over-discharge, when the cell voltage becomes equal or more than the over-discharge released voltage, then the over-discharge state is released, and the output of DOUT becomes "H". After detecting excess discharge current or short circuit, when the load is removed, by the output of DRAIN pin, an external MOSFET turns on, and by the resistance connected to VSS pulls down the VMP pin voltage, and excess discharge current or short circuit detector is released and the output of DOUT becomes "H".

Further, by the input a certain voltage to SEl1 or SEL2 pin, the test time of protection circuit board can be shortened. Each delay time for the over-charge, over-discharge voltage and excess discharge current can be shortened by 1/80.

The R5432V series can be a protector IC for more than 6-stacked cell by cascade connection of two R5432V ICs. Specifically, COUT pin and DOUT pin of the high voltage side IC must be connected to the CTLC and CTLD pin of the low voltage side IC, by the cascade connection, signals are transmitted from not directly connected COUT and DOUT pin to the FETs for charge and discharge, and the FETs can be controlled.

The R5432V series have cell-balance function which can operates for multi-secondary cells to solve the

unbalance. If the cell voltage is beyond the cell-balance voltage, by the output of the cell-balance control pin, an external NMOSFET turns on and a current path is made. During the charge cycle, the charge current is bypassed. If charge is not executed, discharge from the battery will be done. Until the cell voltage becomes to the cell-balance released voltage, the current path is maintained.

If breaking wire between the cell and protection board, the wire breaking is detected, and the output of COUT becomes "Hi-Z". After detecting the breaking wire, the cell and the protection is connected again, the wire breaking detector is released and the output of COUT becomes "H".

FEATURES

- Manufactured with High Voltage Tolerant Process ...Absolute Maximum Rating 30V
- Low supply current .....Under operation, for 5-cell Typ. 12.0μA
- High accuracy detector threshold .....Over-charge detector (Topt=25°C) ±25mV
  Over-discharge detector ±2.5%
  Excess discharge-current detector ±20mV
- Variety of detector threshold

Over-charge detector threshold	3.6V-4.5V step of 0.005V(VDET1n) (n=1,2,3,4,5)
Over-discharge detector threshold	2.0V-3.0V step of 0.005V(VDET2n) (n=1,2,3,4,5)
Excess discharge-current threshold1	0.05V to 0.30V step of 0.01V
Excess discharge-current threshold2	0.6V (Fixed)
Short detector threshold	1.0V (Fixed)
Excess charge-current threshold	-0.05V ± 30mV
	-0.1V ±30mV
	-0.2V ±30mV
	-0.4V ±40mV
Over-charge released voltage	VDET1n-0.1V to 0.4V step of 0.05V (VREL1n) (n=1,2,3,4,5)
Over-discharge released voltage	VDET2n+(0.2V to 0.7V, step of 0.1V) (VREL2n) (n=1,2,3,4,5)
Cell balance threshold voltage	3.45V to 4.45V step of 0.005V (VC_{BDn}) (n=1,2,3,4,5)
Cell balance released voltage	CBDETn-0.0V to 0.4V step of 50mV (VC_{BR1n}) (n=1,2,3,4,5)

- Setting of Output delay time.....Over-charge detector Output Delay 1.0s
  Over-discharge detector Output Delay setting by an external capacitor C_{CT1}
  Excess discharge-current detector Output Delay 1 setting by an external capacitor C_{CT2}
  Excess discharge-current detector Output Delay2 setting by an external capacitor C_{CT2}

Excess charge-current detector Output Delay 8ms

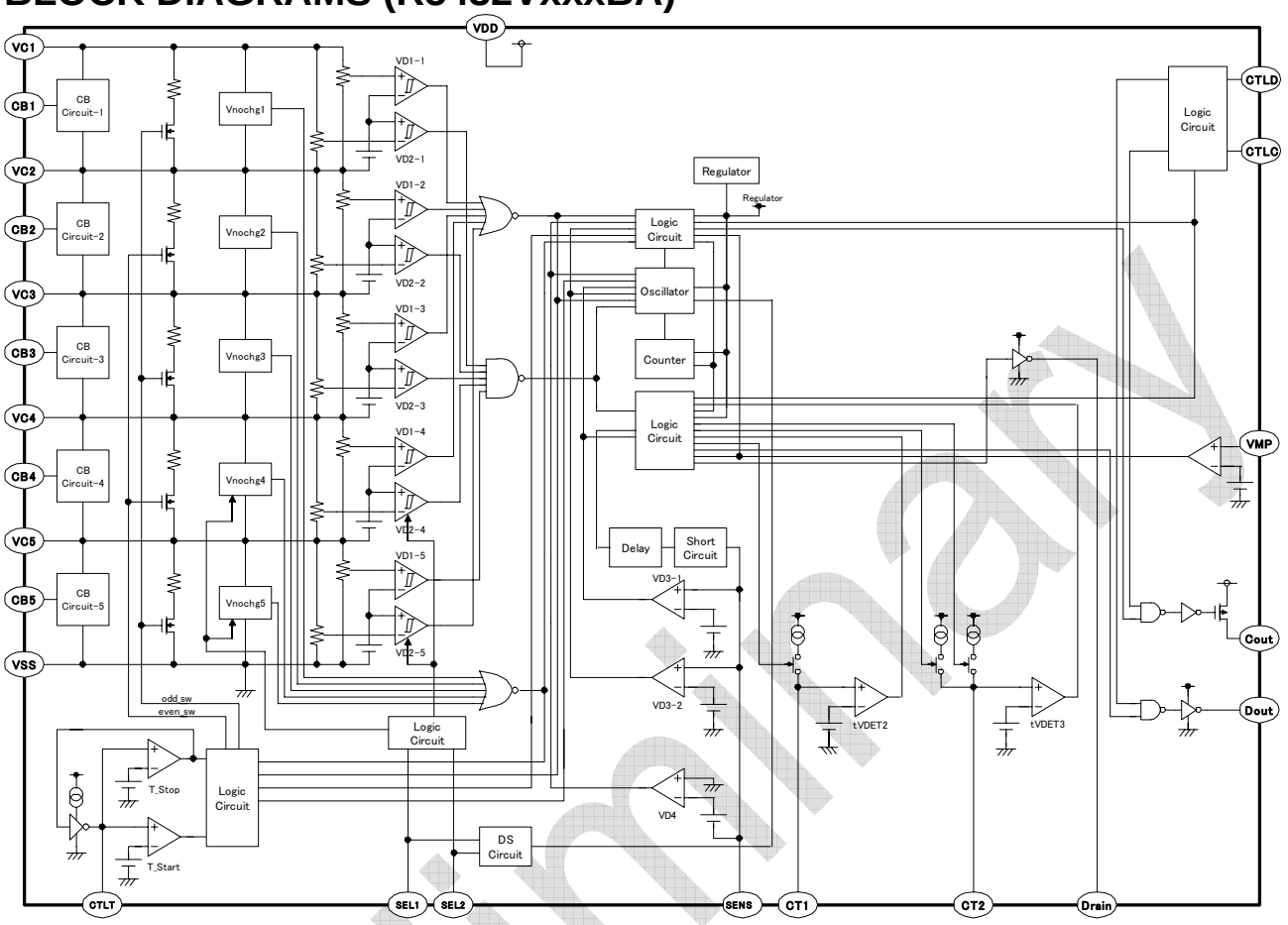
Short Circuit detector Output Delay 300μs

- Output Delay Time Shortening Function. By forcing a designated level to SEL pin, the output delay time of detect and release of the over-charge/discharge, voltage the excess-charge/discharge current can be reduced into approximately 1/80.
  By forcing in the range from 4.0V to VDD/2-0.5V, the Delay Time for over-charge becomes 4ms.)
- 0V-battery charge..... Acceptable
- Over-charge/discharge/short current..... Threshold level can be set by an external resister.
- Cascade connection..... available if 6-cell or more serial connection is necessary.
  ..... Refer to the typical application circuit.
- 3/4/5 cell protection enabler.....By the signal to SEL1 and SEL2 pins, 3-cell protection,
  .....4-cell protection, or 5-cell protection can be selected.
- Built-in Cell balance function
- Cell unbalance condition .....Either of cells detects over-charge and at least one of serial cells detects over-discharge, the both output of COUT becomes "Hi-Z" and DOUT becomes "L".
- Over-charge/discharge released condition ....Released by voltage type
- C_{OUT} output/D_{OUT} output.....COUT: VDD power source Pch open drain output
  Normal state "H" (VDD) Detected state H
  DOUT: 12V regulator output source CMOS output
  Normal state "H"(12V), Detected state "L"

Breaking wire Detector Function (Option).....Breaking wire detector function between VDD, VSS, VCx pin of the IC and the battery pack

- Small package SSOP-24

BLOCK DIAGRAMS (R5432VxxxBA)



SELECTION GUIDE

In the R5432Vxxxx Series, input threshold of over-charge, over-discharge, excess charge/discharge current, and output delay time can be designated according to the application.

Part Number is designated as follows:

(ex.)

R5432V 501BA ←Part Number
↑ ↑ ↑↑
a b c d

Code	Contents
a	Package Type V: SSOP-24
b	Serial Number for the R5432 Series designating input threshold for over-charge, over-discharge, excess charge/discharge-current detectors.
c	Designation of Output delay option
d	Designation of version symbols.

***Function Table**

Code	Over-charge Released condition	Over-discharge Released condition	0V battery charge	Cascade connection	Breaking wire detector
R5432VxxxxA	By voltage	By voltage	acceptable	available	Built-in

Delay Time table

Code	Over-charge detector output delay time tVdet1 (s)	Over-discharge detector output delay time tVdet2 (ms)	Excess-discharge current detector threshold output delay time 1 tVdet3-1(ms)	Excess-discharge current detector threshold output delay time 2 tVdet3-2 (ms)	Excess-charge current detector threshold output delay time tVdet4 (ms)	Short detector threshold output delay time Tshort(μ s)
R5432VxxxBx	1.0	38.8×C_{CT1}(nF)	32.6×C_{CT2}(nF)	tVDET31/6	8	300

***Capacitor for CT1 pin: C_{CT1}, Capacitor for CT2 pin: C_{CT2}. In terms of tVDET2, tVDET31, tVDET32, refer to the item "OPERATION".**

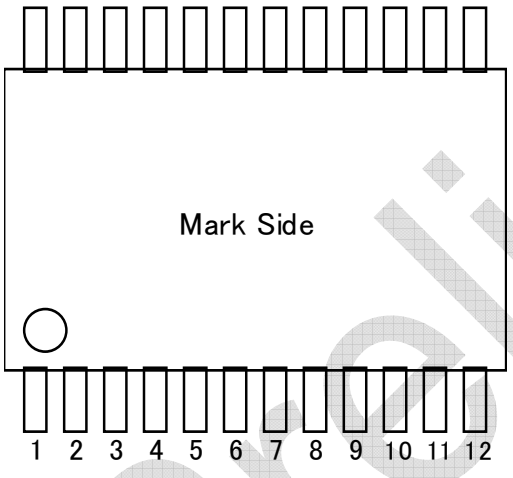
***Product name list**

Code	Over charge detector threshold VDET1n (V) *1	Over charge Released voltage VREL1n (V) *1	Cell balance detector threshold VCBDn (V)*1	Cell balance detector released voltage VCBRn(V)*1	Over discharge detector threshold VDET2n (V) *1	Over discharge Released voltage VREL2n (V) *1	Excess discharge Current detector threshold 1 VDET31(V)	Excess discharge current detector threshold 2 VDET32(V)	Short Detector Threshold Vshort (V)	Excess charge current detector threshold VDET4(V)
R5432V402BA	4.350	4.050	4.200	4.200	2.400	2.700	0.200	0.600	1.000	-0.100
R5432V403BA	3.900	3.800	3.500	3.500	2.500	3.000	0.100	0.600	1.000	-0.100
R5432V404BA	4.250	4.100	4.200	4.200	2.500	3.000	0.200	0.600	1.000	-0.200
R5432V405BA	3.900	3.800	3.650	3.650	2.000	2.300	0.100	0.600	1.000	-0.200
R5432V406BA	3.650	3.550	3.500	3.500	2.500	3.000	0.300	0.600	1.000	-0.200
R5432V501BA	3.900	3.700	3.800	3.600	2.000	2.300	0.200	0.600	1.000	-0.200

***1: n=1,2,3,4,5**

PIN CONFIGURATIONS

SSOP-24



PIN DESCRIPTION

Pin No.	Symbol	Description
1	CTLC	COUT FET charge-discharge control pin
2	CTLD	DOUT FET charge-discharge control pin
3	C_{OUT}	Output pin of over-charge detection, Pch open drain output
4	VMP	Charger voltage input pin
5	DRAIN	Excess discharge current release FET gate connect pin
6	D_{OUT}	Output pin of over-discharge detection, CMOS output
7	SENS	Current sense pin
8	CTLT	Capacitor setting pin for time interval of breaking wire detector function
9	V_{SS}	Vss pin. Ground pin for the IC
10	CT1	tVDET2 capacitor setting pin
11	CT2	tVDET3 capacitor setting pin
12	SEL1	selector pin for 3-cell/4-cell/5-cell protection
13	SEL2	selector pin for 3-cell/4-cell/5-cell protection
14	CB5	Cell balance control pin for Cell-5
15	VC5	Positive terminal pin for Cell-5
16	CB4	Cell balance control pin for Cell-4
17	V_{C4}	Positive terminal Pin for Cell-4
18	CB3	Cell balance control pin for Cell-3
19	V_{C3}	Positive terminal Pin for Cell-3
20	CB2	Cell balance control pin for Cell-2
21	V_{C2}	Positive terminal pin for Cell-2
22	CB1	Cell balance control pin for Cell-1
23	V_{C1}	Positive terminal pin for Cell-1
24	V_{DD}	V_{DD} Pin

ABSOLUTE MAXIMUM RATINGS

Topt=25°C, Vss=0V

Symbol	Item	Ratings	Unit
V_{DD}	Supply voltage	-0.3 to 30	V
	Input Voltage		
VC_1	Positive input pin voltage for Cell-1	VC_2 –0.3 to VC_2+6.5	
VC_2	Positive input pin voltage for Cell-2	VC_3 –0.3 to VC_3+6.5	
VC_3	Positive input pin voltage for Cell-3	VC_4 –0.3 to VC_4+6.5	
VC_4	Positive input pin voltage for Cell-4	VC_5 –0.3 to VC_5+6.5	
VC_5	Positive input pin voltage for Cell-5	Vss –0.3 to Vss+6.5	
VMP	Charger negative terminal input pin voltage	-0.3 to 30	
VSEL1	SEL1 pin voltage	-0.3 to V_{DD}+0.3	V
VSEL2	SEL2 pin voltage	-0.3 to V_{DD}+0.3	
VCTLC	CTLC pin voltage	-0.3 to VDD+25 and up to 48	
VCTLD	CTLD pin voltage	-0.3 to VDD+25 and up to 48	
VCTLT	Breaking Wire Detector Interval setting pin voltage	-0.3 to 3.5	
VSENS	Current sense pin voltage	-0.3 to V_{DD}+0.3	
VCT1	Output delay time setting pin 1 voltage	-0.3 to 3.5	
VCT2	Output delay time setting pin 2 voltage	-0.3 to 3.5	
	Output voltage		
VC_{OUT}	C_{OUT} pin	VDD –30 to VDD+0.3	
VD_{OUT}	D_{OUT} pin	-0.3 to VOH2+0.3	
VDRAIN	DRAIN pin voltage	-0.3 to VOH3+0.3	
VCB1	CB pin voltage for Cell-1	VC_2-0.3 to VC_2+6.5	V
VCB2	CB pin voltage for Cell-2	VC_3-0.3 to VC_3+6.5	
VCB3	CB pin voltage for Cell-3	VC_4-0.3 to VC_4+6.5	
VCB4	CB pin voltage for Cell-4	VC_5-0.3 to VC_5+6.5	
VCB5	CB pin voltage for Cell-5	-0.3 to 6.5	
P_D	Power dissipation	770	mW
Topt	Operating temperature range	-40 to 85	°C
Tstg	Storage temperature range	-55 to 125	°C

ELECTRICAL CHARACTERISTICS

R5432VXXXBA Unless otherwise specified, Topt=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
V_{DD1}	Operating input voltage	Voltage defined as V_{DD}-V_{SS}	2		25	V	-
V_{DET1n}	CELLn Over-charge threshold (n=1,2,3,4,5)	Detect rising edge of supply voltage	V_{DET1n}-0.025	V_{DET1n}	V_{DET1n}+0.025	V	A
V_{REL1n}	CELLn Over-charge released voltage (n=1,2,3,4,5)	Detect falling edge of supply voltage	V_{REL1n}-0.050	V_{REL1n}	V_{REL1n}+0.050	V	A
tV_{DET1}	Output delay of over-charge	V_{DD}=V_{C1}, Vc_{ELL}n=3.5V, V_{CELL1}=3.5V to 4.5V (n=2,3,4,5)	0.7	1.0	1.3	s	B
tVREL1	Output delay of release from over-charge	V_{DD}=V_{C1}, V_{CELL}n=3.5V, V_{CELL1}=4.5V to 3.5V (n=2,3,4,5)	11	16	21	ms	B
V_{CBDn}	CELLn cell balance detector threshold (n=1,2,3,4,5)	Detect rising edge	VC_{BDn}-0.025V	VC_{BDn}	VC_{BDn}+0.025V	V	C
V_{CBRn}	CELLn cell balance released voltage (n=1,2,3,4,5)	Detect falling edge	VC_{BRn}-0.050V	VC_{BRn}	VC_{BRn}+0.050 V	V	C
V_{DET2n}	CELLn Over-discharge threshold (n=1,2,3,4,5)	Detect falling edge of supply voltage	V_{DET2n}×0.975	V_{DET2n}	V_{DET20}×1.025	V	D
V_{REL2n}	CELLn Released Voltage from Over-discharge (n=1,2,3,4,5)	Detect rising edge of supply voltage	V_{REL2n}×0.975	V_{REL2n}	V_{REL2n}×1.025	V	D
ICT_1	CT1 charge current	V_{DD}=V_{C1}, V_{CELLn}=3.5V(n=2,3,4,5), V_{CELL1}=3.5V to 1.5V	350	500	650	nA	E
$VDCT_1$	CT1 detector threshold	V_{DD}=V_{C1}, V_{CELLn}=3.5V(n=2,3,4,5), V_{CELL1}=1.5V	1.48	1.85	2.22	V	F
tV_{DET2}	Output delay of over-discharge	tV_{DET2}=C_{CT1} x V_{DCT1}/I_{CT1} CCT1=33nF	89	128	167	ms	-
tV_{REL2}	Output delay of release from over-discharge	V_{DD}=V_{C1}, V_{CELLn}=3.5V, V_{CELL1}=1.5V to 3.5V, (n=2,3,4,5)	0.7	1.2	1.7	ms	G
V_{DET31}	Excess discharge-current threshold 1	V_{DD}=V_{C1} V_{CELLn}=3.5V(n=1,2,3,4,5) VMP=4.0V, Detect rising edge	V_{DET31}-0.020	V_{DET31}	V_{DET31}+0.020	V	H
V_{DET32}	Excess discharge-current threshold 2	V_{DD}=V_{C1} V_{CELLn}=3.5V(n=1,2,3,4,5) VMP=4.0V, Detect rising edge	0.500	0.600	0.700	V	I
V_{REL3}	Excess discharge-current released voltage	V_{DD}=V_{C1} V_{CELLn}=3.5V(n=1,2,3,4,5) SENS=0.0V, Detect falling edge	V_{DET31}x0.50	V_{DET31}x0.75	V_{DET31} x1.00	V	H
ICT_{231}	CT2 charge current 1	V_{DD}=V_{C1} V_{CELLn}=3.5V(n=1,2,3,4,5) SENS=VSS to 0.4V	350	500	650	nA	I
ICT_{232}	CT2 charge current 2	V_{DD}=V_{C1} V_{CELLn}=3.5V(n=1,2,3,4,5) SENS=VSS to 0.7V	2.0	3.0	4.0	μA	I
$VDCT_2$	CT2 detector threshold	V_{DD}=V_{C1} V_{CELLn}=3.5V(n=2,3,4,5) SENS=0.4V, VMP=4.0V	1.23	1.55	1.87	V	J
tV_{DET31}	Output delay of excess discharge current 1	tV_{DET31}=C_{CT2} x V_{DCT2}/ICT231, CCT2=3.3nF	7.3	10.8	14.7	ms	-
tV_{DET32}	Output delay of excess discharge current 2	tV_{DET32}=$C_{CT2x}V_{DCT2}$/ICT232 CCT2=3.3nF	1.25	1.80	2.40	ms	-
tV_{REL3}	Output delay of release from excess discharge-current	V_{DD}=V_{C1}, V_{CELLn}=3.5V, SENS=V_{SS} VMP=4.0V to V_{SS} (n=1,2,3,4,5)	0.7	1.2	1.7	ms	H
V_{DET4}	Excess charge-current threshold	V_{DD}=V_{C1}, V_{CELLn}=3.5V (n=1,2,3,4,5) Detect rising edge, the value is V_{SS} base.	V_{DET4}-0.030	V_{DET4}	V_{DET4}+0.030	V	L
tV_{DET4}	Output delay of excess charge-current	V_{DD}=V_{C1}, V_{CELLn}=3.5V, SENS=VSS to -1.0V, (n=1,2,3,4,5)	5	8	11	ms	L

tV_{REL4}	Output delay of release from excess charge-current	$V_{DD}=V_{C1}$, V_{CELLn}=3.5V, SENS=Vss, VMP=-1.0V to 1.0V (n=1,2,3,4,5)	0.7	1.2	1.7	ms	L
Vshort	Short protection voltage	$V_{DD}=V_{C1}$, V_{CELLn}=3.5V, V_{SS} base (n=1,2,3,4,5)	0.7	1.0	1.3	V	K
tshort	Output Delay of Short protection	$V_{DD}=V_{C1}$, V_{CELLn}=3.5V, SENS=V_{SS} to V_{SS}+2.0V, (n=1,2,3,4,5) VMP=4.0V	180	300	550	µs	K
VIH1	SEL1 pin "H" input voltage	$V_{DD}=V_{C1}$, V_{CELLn}=3.2V (n=1,2,3,4,5)	V_{DD} -1.0		V_{DD} +0.3	V	M
VIM1	SEL1 pin "Middle" input voltage	$V_{DD}=V_{C1}$, V_{CELLn}=3.2V (n=1,2,3,4,5)	4.0		$V_{DD}/2$ - 0.5	V	M
VIL1	SEL1 pin "L" input voltage	$V_{DD}=V_{C1}$, V_{CELLn}=3.2V (n=1,2,3,4,5)	Vss -0.3		V_{SS} +1.0	V	M
VIH2	SEL2 pin "H" input voltage	$V_{DD}=V_{C1}$, V_{CELLn}=3.2V (n=1,2,3,4,5)	V_{DD} -1.0		V_{DD} +0.3	V	N
VIM2	SEL2 pin "Middle" input voltage	$V_{DD}=V_{C1}$, V_{CELLn}=3.2V (n=1,2,3,4,5)	4.0		$V_{DD}/2$ - 0.5	V	N
VIL2	SEL2 pin "L" input voltage	$V_{DD}=V_{C1}$, V_{CELLn}=3.2V (n=1,2,3,4,5)	V_{SS} -0.3		V_{SS} +1.0	V	N
CTLC1H	CTLC pin "H" input voltage 1	$V_{DD}=V_{C1}$, V_{CELLn}=3.2V (n=1,2,3,4,5)	V_{DD}+ 2.0			V	O
CTLC2H	CTLC pin "H" input voltage 2	$V_{DD}=V_{C1}$, V_{CELLn}=3.2V (n=1,2,3,4,5)	V_{DD} -0.3		V_{DD} +0.3	V	O
CTLC1L	CTLC pin "L" input voltage	$V_{DD}=V_{C1}$, V_{CELLn}=3.2V (n=1,2,3,4,5)	Vss -0.3		V_{SS} +0.3	V	O
CTLD1H	CTLD pin "H" input voltage 1	$V_{DD}=V_{C1}$, V_{CELLn}=3.2V (n=1,2,3,4,5)	V_{DD}+ 2.0			V	P
CTLD2H	CTLD pin "H" input voltage 2	$V_{DD}=V_{C1}$, V_{CELLn}=3.2V (n=1,2,3,4,5)	V_{DD} -0.3		V_{DD} +0.3	V	P
CTLD1L	CTLD pin "L" input voltage	$V_{DD}=V_{C1}$, V_{CELLn}=3.2V (n=1,2,3,4,5)	Vss -0.3		V_{SS} +0.3	V	P
VOH1	COUT Pch ON voltage	I_{OH}=-50µA, V_{DD}=VC1, V_{CELLn}=3.2V, (n=1,2,3,4,5), CTLC=Vss	VDD -0.5	VDD -0.1		V	T
VVR12	VR12V Output Voltage	I_{OH}=-5µA, V_{DD}=VC1, V_{CELLn}=3.2V, (n=1,2,3,4,5), CTLD=Vss Current sink from D_{OUT}	10	12	14	V	U
VOH2	DOUT Pch ON voltage	I_{OH}=-50µA, V_{DD}=VC1, V_{CELLn}=3.2V, (n=1,2,3,4,5), CTLD=Vss	VVR12 -0.5	VVR12 -0.1		V	U
VOH3	DRAIN Pch ON voltage	I_{OH}=-50µA, V_{DD}=VC1, V_{CELLn}=3.2V, (n=1,2,3,4,5), SENS=VMP=4.0V	VVR12 -0.5	VVR12 -0.1		V	V
VOH4	CB1 Pch ON voltage	I_{OH}=-50µA, V_{DD}=VC1, VC1=4.5V, VCELLn=3.2V (n=2,3,4,5)	VC1 -0.5	VC1 -0.3		V	W
VOH5	CB2 Pch ON voltage	I_{OH}=-50µA, V_{DD}=VC1, VC2=4.5V, VCELLn=3.2V (n=1,3,4,5)	VC2 -0.5	VC2 -0.3		V	W
VOH6	CB3 Pch ON voltage	I_{OH}=-50µA, V_{DD}=VC1, VC3=4.5V, VCELLn=3.2V (n=1,2,4,5)	VC3 -0.5	VC3 -0.3		V	W
VOH7	CB4 Pch ON voltage	I_{OH}=-50µA, V_{DD}=VC1, VC4=4.5V, VCELLn=3.2V (n=1,2,3,5)	VC4 -0.5	VC4 -0.3		V	W

VOH8	CB5 Pch ON voltage	I_{OH}=-50μA, V_{DD}=VC1, VC5=4.5V, VCELLn=3.2V (n=1,2,3,4)	VC5 -0.5	VC5 -0.3		V	W
VOL2	DOUT Nch ON voltage	I_{OL}=50μA, V_{DD}=VC1, V_{CELLn}=3.2V, (n=1,2,3,4,5), CTLD=VDD		0.1	0.5	V	Q
VOL3	DRAIN Nch ON voltage	I_{OL}=50μA, V_{DD}=VC1, V_{CELLn}=3.2V, (n=1,2,3,4,5)		0.1	0.5	V	R
VOL4	CB1 Nch ON voltage	I_{OL}=50μA, V_{DD}=VC1, V_{CELLn}=3.2V, (n=1,2,3,4,5)		VC2 +0.2	VC2 +0.5	V	S
VOL5	CB2 Nch ON voltage	I_{OL}=50μA, V_{DD}=VC1, V_{CELLn}=3.2V, (n=1,2,3,4,5)		VC3 +0.2	VC3 +0.5	V	S
VOL6	CB3 Nch ON voltage	I_{OL}=50μA, V_{DD}=VC1, V_{CELLn}=3.2V, (n=1,2,3,4,5)		VC4 +0.2	VC4 +0.5	V	S
VOL7	CB4 Nch ON voltage	I_{OL}=50μA, V_{DD}=VC1, V_{CELLn}=3.2V, (n=1,2,3,4,5)		VC5 +0.2	VC5 +0.5	V	S
VOL8	CB5 Nch ON voltage	I_{OL}=50μA, V_{DD}=VC1, V_{CELLn}=3.2V, (n=1,2,3,4,5)		0.2	0.5	V	S
ILCOUT	COUT pin off leakage current	V_{DD}=VC1, V_{CELLn}=3.2V, (n=1,2,3,4,5) CTLC=VDD, COUT=-14V	-0.1			μA	X
ICTLT	CTLT charge current	V_{DD}=VC1, V_{CELLn}=3.2V, (n=1,2,3,4,5)	145	205	264	nA	Y
VDTLT	CTLT detector threshold	V_{DD}=VC1, V_{CELLn}=3.2V, (n=1,2,4,5) VC3=VD1+0.2V	1.58	2.00	2.42	V	Z
VRTLT	CTLT released voltage	V_{DD}=VC1, V_{CELLn}=3.2V, (n=1,2,3,4,5)	0.07	0.13	0.19	V	Z
tLT	Breaking wire detector test interval	C_{CTLT}x(VDTLT-VRTLT)/ICTLT, CCTLT=3.3uF	21	30	39	s	-
I_{SS1}	Supply current1	V_{DD}=V_{C1}, C_{OUT}=Open, V_{CELLn}=VDET1n-0.4V (n=1,2,3,4,5)		12	30	μA	a
I_{SS2}	Supply current2	V_{DD}=V_{C1}, C_{OUT}=Open, V_{CELLn}=1.5V (n=1,2,3,4,5)		10	25	μA	a

*Note: VCELLn means Cell-n's voltage. n=1,2,3,4,5

OPERATION

- **VDET1n / Over-Charge Detectors (n=1, 2, 3, 4, 5)**

  While the cell is charged, the voltage between VC1 pin and VC2 pin (voltage of the Cell-1), the voltage between VC2 pin and VC3 pin (voltage of the Cell-2), the voltage between VC3 pin and VC4 pin (voltage of the Cell-3), the voltage of VC4 pin and VC5 pin (voltage of Cell-4), and the voltage between VC5 pin and VSS pin (voltage of the Cell-5) are supervised. If at least one of the cells' voltage becomes equal or more than the over-charge detector threshold, the over-charge is detected, and C_{OUT} pin connected to an external pull down resistance outputs "Hi-Z", and by turning off the external Nch MOSFET by the pull-down resister, charge cycle stops.

To reset the over-charge and make the C_{OUT} pin level to "H" again after detecting over-charge, in such conditions that a time when all the cells' voltages are down to a level lower than over-charge released voltage. The output voltage of C_{OUT} pin becomes "H", and it makes an external Nch MOSFET turns on, and charge cycle is available. The over-charge detectors have hysteresis.

Internal fixed output delay times for over-charge detection and release from over-charge exist. Even if one of voltage of Cells keeps its level more than the over-charge detector threshold, and output delay time passes, over-charge voltage is detected. Even when the voltage of each cell becomes equal or higher level than V_{DET1} if these voltages would be back to a level lower than the over-charge detector threshold within a time period of the output delay time, the over-charge is not detected. Besides, after detecting over-charge, each cell voltage is lower than the over-charge detector released voltage, even if just one of cells' voltage becomes equal or more than the over-charge released voltage within the released output delay time, over-charge is not released.

The output type of the C_{OUT} pin is Pch open drain and "H" level of C_{OUT} pin is VDD pin voltage.

- **VDET2n / Over-Discharge Detectors (n=1, 2, 3, 4, 5)**

  While the cells are discharged, the voltage between VC1 pin and VC2 pin (the voltage of Cell-1), the voltage between VC2 pin and VC3 pin (Cell-2 voltage), the voltage between VC3 pin and VC4 pin (Cell-3 voltage), the voltage between VC4 pin and VC5 pin (Cell-4 voltage), and the voltage between VC5 pin and Vss pin (Cell-5 voltage) are supervised. If at least one of the cells' voltage becomes equal or less than the over-discharge detector threshold, the over-discharge is detected and discharge stops by the external discharge control Nch MOSFET turning off with the D_{OUT} pin being at "L".

The condition to release over-discharge voltage detector is that after detecting over-discharge voltage, all the cells' voltage becomes higher than the over-discharge released voltage, DOUT pin becomes "H" level, and by turning on the external Nch MOSFET, discharge becomes possible. The over-discharge detectors have hysteresis.

The output delay time for over-discharge detect is set with an external capacitor C_{CT1} connected to

CT1 pin. If at least one of the voltage of Cells is down to equal or lower than the over-discharge detector threshold, if the voltage of each Cell would be back to a level higher than the over-discharge detector threshold within a time period of the output delay time, the over-discharge is not detected. Output delay time for release from over-discharge is also set internally.
After detecting over-discharge, supply current would be reduced and be into standby by halting un-necessary circuits and consumption current of the IC itself is made as small as possible.

When a cell voltage equals to zero, if the voltage of each cell is lower than charge inhibit maximum voltage, charge is not acceptable. All the cell voltages are higher than charge inhibit maximum voltage, C_{OUT} pin becomes "H" and a system is allowable to charge.

The output type of D_{OUT} pin is CMOS having "H" level around 12V of the internal regulator and "L" level of V_{SS}.

- **VDET3-n (n=1, 2) /Excess discharge-current Detector, Short Circuit Protector**

  When the charge and discharge is acceptable, SENS pin voltage is supervised, if the load is short and SENS pin voltage becomes equal or more than excess discharge current threshold, and equal or less than short detector threshold, the status becomes excess discharge current detected condition. If SENS pin voltage becomes equal or more than short circuit detector threshold, the status becomes short circuit detected, then DOUT pin outputs "L" and by turning off the external MOSFET, large current flow is prevented. The excess discharge current detector has two thresholds, and each threshold has the output delay time. In terms of the output delay times, the delay time for the excess discharge current detector 2 is set shorter than the excess discharge current 1.

  The output delay times for the excess discharge-current detectors are set by an external capacitor C_{CT2} connected to CT2 pin.

A quick recovery of SENS pin level from a value between the excess discharge current detector and short circuit detector threshold within the delay time, may keep the status as before excess discharge current detected. Output delay time for the release from excess discharge-current detection is also set internally.

When the short circuit protector is enabled, the delay time is also set.

Between the drain of the external FET connected to DRAIN pin, and the drain of an external FET connected to COUT and DOUT, an external resistor should be mounted to release from over-discharge.

After an excess discharge-current or short circuit protection is detected, an external FET connected to DRAIN pin turns on and the resistance of release from excess-discharge current, is connected to VSS. After detecting the excess discharge current or short circuit, load is removed and opened, VMP pin level is connected to the VSS pin level, through the pulled down resistor for release from excess discharge, and when the VMP pin becomes equal or less than VREL3, the circuit is released from excess discharge

or short automatically. When the excess-discharge current is released, the external FET connected to DRAIN pin turns off and resisters for release from excess-discharge current status is separated from Vss.

- **VDET4/ Excess charge-current detector**

When the battery pack is chargeable and discharge is also possible, VDET4 senses SENS pin voltage. For example, in case that a battery pack is charged by an inappropriate charger, an excess current flows, then the voltage of SENS pin becomes equal or less than the excess charge-current detector threshold, then the output of COUT pin outputs "Hi-Z", and by turning off the external Nch MOSFET with the pull-down resister, flowing excess current in the circuit is prevented.

Output delay of excess charge current is internally fixed. Even the voltage level of SENS pin becomes equal or lower than the excess charge-current detector threshold, if the voltage becomes higher than the excess charge current threshold within the delay time, the excess charge current is not detected. Output delay for the release from excess charge current is also set.

VDET4 can be released with disconnecting a charger and connecting a load and when the VMP pin voltage becomes equal or more than VREL3.

- **Operation against cell unbalance**

If one of the cells detects over-charge and either of the cells detect over-discharge, both outputs of COUT and DOUT become "L".

- **CTLC/CTLD pin**

If the ICs are stacked and function with two chips, by connecting COUT and CTLC, and connecting DOUT and CTLD shown as in the example circuit (10-cell protection), over-charge, over-discharge, breaking wire state can be transferred. If stacked connection is unnecessary, CTLC/CTLD pins must be set at VSS voltage level.

If CTLC/CTLD pins are in the range of Vss ± 0.3V, or larger than VDD+2.0V, the IC operates in normal way.

By forcing VDD voltage level (between VDD-0.3V and VDD+0.3V) to CTLC pin, the output of COUT connected an external pull-down resister can be forcibly set to "L". However, if short circuit is detected, the output of COUT cannot be made "L".

By forcing VDD voltage level (between VDD-1.0V and VDD+3.0V) to CTLD pin, the output of DOUT can be forcibly set to "L".

If a voltage in the range from Vss+0.3V to VDD-0.3V is forced to the CTLC/CTLD pin, the operation may change by the voltage between VDD and Vss.

The voltage in the range from Vss + 0.3V to VDD-0.3V should not be forced to CTLC/CTLD con-

tinuously.

CTL pin input and outputs of COUT and DOUT

CTLC/CTLD pin input	C_{OUT}/D_{OUT} external FET
equal or more than VDD+2.0	Normal Operation
VDD-0.3V to VDD+0.3V	forced off
VSS-0.3 to Vss+0.3	Normal Operation
Open, other than the above	Indefinite

- **SEL1, SEL2 pin**

SEL1 and SEL2 pins are used as switch over 3-cell protector, 4-cell protector and 5-cell protector.

If 4-cell protection is selected, by forcing VSS voltage level to SEL1 pin and forcing VDD voltage level to SEL2 pin, the operation of 5th cell's protection circuit, the signal is shut down, therefore, even if the VC5 is shortened to GND, over-discharge is not detected and operates as a 4-cell protector IC.

3-cell protection is selected, by forcing VDD voltage level to SEL1 pin, VSS voltage level to SEL2 pin, the operation of 5th cell and 4th cell stop, and cut off the signal. Therefore, if VC4, VC5 and VSS is shorted, over-discharge is not detected and operates as a 3-cell protector IC.

SEL pin must be set as V_{DD} voltage or V_{SS} voltage level.

Depending on the combination of SEL1 pin and SEL2 pin's input, delay time shortening function mode1 (down to 1/100 delay) or delay time shortening function mode 2 (over-charge detector threshold delay time is shortened into 4ms) is realized.

Middle voltage of the table below is in the range from 4.0V to VDD/2-0.5V.

SEL1 and SEL2 pin input combination, and the operation mode

SEL1 pin input	SEL2 pin input	Operation Mode
High	High	5-cell protector
Low	High	4-cell protector
High	Low	3-cell protector
Low	Low	Delay shortening mode 1 for 5-cell protector
Low	Middle	Delay shortening mode 1 for 4-cell protector
Middle	Low	Delay shortening mode 1 for 3-cell protector
Middle	Middle	Delay shortening mode 2 for 5-cell protector
Middle	High	Delay shortening mode 2 for 4-cell protector
High	Middle	Delay time shortening mode 2 for 3-cell protector

- **CT1, CT2 pin**

CT1 and CT2 pins are used for setting the output delay time of over-discharge (tVDET2), excess discharge current 1 (tVDET31), and excess discharge current 2 (tVDET32) by connecting external capacitors C_{CT1} and C_{CT2}.

tVDET2 can be set with CT1 pin. tVDET31 and tVDET32 can be set with CT2 pin.

tVDET2, tVDET31, and tVDET32 can be set according to the equation of CV=iΔt.

(1) tVDET2 external capacitor C_{CT1} setting

tVDET2 can be set as in the next formula.

$tVDET2=C_{CT1}(nF)\times VDCT1/ICT1$

For example, if C_{CT1}=33nF, VDCT1=1.85V, ICT1=500nA, tVDET2 =122ms

(2) tVDET31 and tVDET32 external capacitor C_{CT2} setting

tVDET31 and tVDET32 can be set as in the next fomulas.

$tVDET31=C_{CT2}(nF)\times VDCT2/ICT2$

tVDET32=tVDET31/6

For example, if C_{CT2}=3.3nF, VDCT2=1.55V, ICT2=500nA, then tVDET31=10.2ms, tVDET32=1.7ms.

- **Cell balance function CB circuit-n (n=1,2,3,4,5)**

While a battery is being charged, and the cell voltage is beyond the cell balance voltage VC_{BDn}(n=1,2,3,4,5) , against the cell which becomes equal or more than the cell balance voltage VC_{BDn}, the output of CBn pin (n=1,2,3,4,5) becomes "H" and an external Nch transistor for cell balance turns on, and discharge path is connected in parallel with the cell and charge current is reduced. When the cell voltage becomes equal or less than the cell balance released voltage VCBRn (n=1,2,3,4,5), then cell balance function is released and the output of CBn pin (n=1,2,3,4,5) becomes "L".

The resister used for the discharge path, absolute ratings must be cared.

If the cell balance function is unnecessary, CBn pin must be left open.

- **Breaking Wire Detector Function**

Breaking wire detect of VDD(VC1) and Vss for 5-cell protector

If VDD line is cut, the voltage between VC1 and VC2 is less than 0V.

If VSS line is cut, the voltage between VC5 and VSS is less than 0V.

The voltage is detected by the 0V-detector circuit.

If breaking wire is detected, the Pch open drain of the COUT turns off.

Breaking wire detect of VC2, VC3, VC4, VC5 for 5-cell protection

In case of the 3.3uF capacitor is attached to the CTLT pin, breaking wire detector operates every 30 seconds. The built in switch of VC1, VC3, VC5 cell, and the switch attached to the VC2 and VC4 turn on alternatively by the even_sw and the odd_sw signal.

The internal impedance of the cell whose switch turns on becomes low for about 1.2 seconds by the low resistance connected to the switch. If the wire is not broken, the capacitor of the CTLT is discharged and the next cycle starts for checking.

While the wire is broken, the difference of the internal impedance of the IC generated by the switch's tuning on makes VC shift and the change is detected by the comparator for VDET1. If the breaking wire is detected and the condition continues for about 4ms, then even_sw and odd_sw turn off and the capacitor of CTLT is discharged and the P-channel open drain of the COUT turns off. While the over-discharge voltage is detected, the breaking wire of VC2, VC3, VC4 and VC5 does not operate.

Breaking wire detect of VDD (VC1) and VSS for 10-cell protection

If the ICs are connected in cascade, the VDD of the high side IC and VSS (VSS2) of the low side IC, the breaking wire detector is able to work as well as 5-cell protection type.

If the VSS (VSS1) of high side IC and VDD(VDD2) of low side IC are connected with a wire from the battery, and the line is broken, the two lines, VSS1 and VDD2 break the wire and breaking wire may not be able to be detected correctly. Connect with two wires to realize either of the VSS1 or VDD2 is connected to the battery, and the pull-down resistance of COUT of high side is connected to the VDD2 of the low side IC, if either of VSS1 or VDD2 breaks the wire, the breaking wire detector is able to operate.

Refer to the typical application circuit. (10-cell, cell-balance, breaking wire detector are in use.)

***Limitation of the breaking-wire detector for VC2, VC3, VC4, VC5.**

If the breaking-wire detecting function is necessary, confirm the limitations below;

External components must be

C_{CTLT}=3.3μF

C_{CT1} range: from 0.47μF to 1.0μF

C_{VCx}=0.1μF

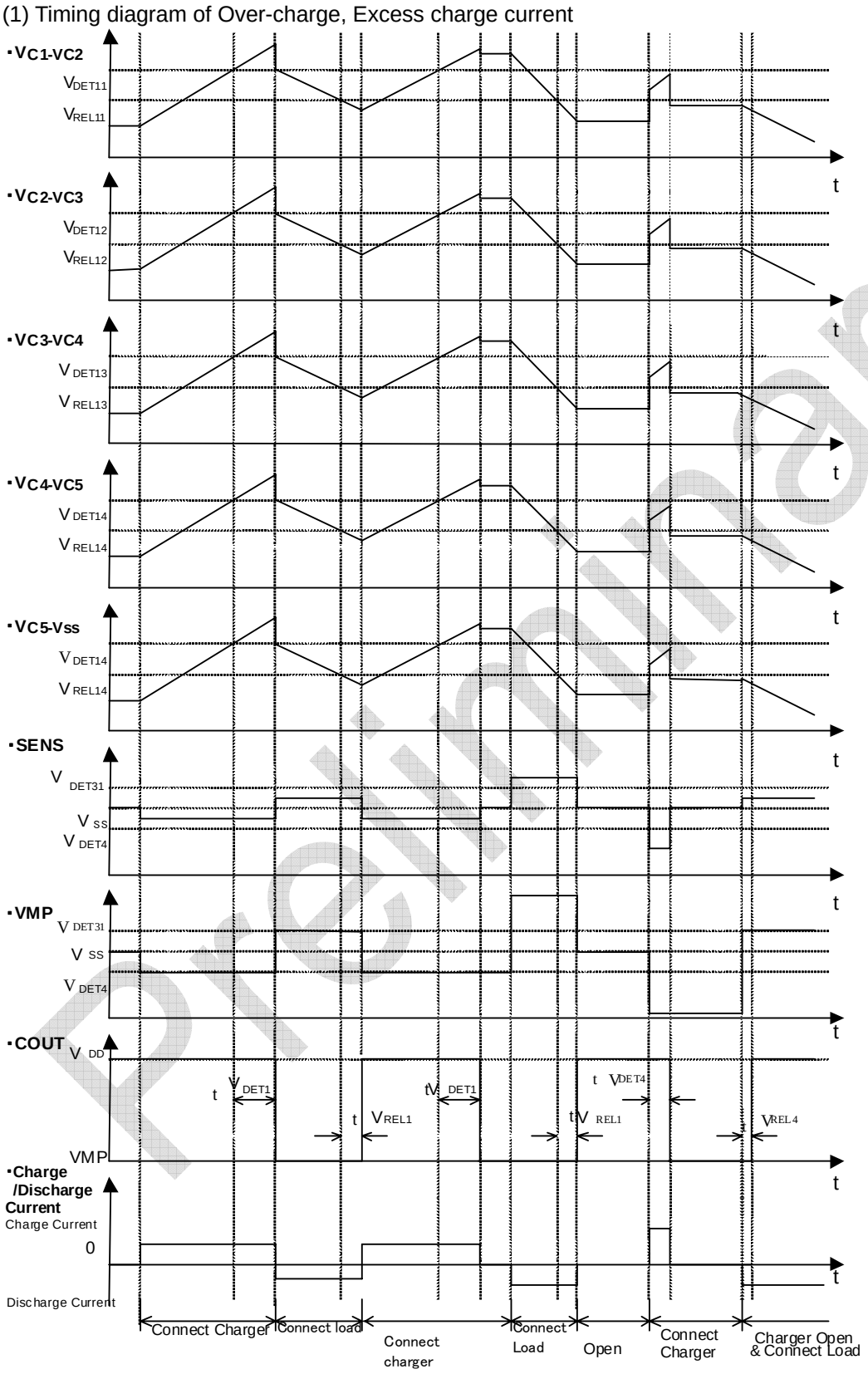
Even if the protection IC does not detect over-discharge, if the cell voltage is low, depending on the distribution of the ICs, cell balance state, the operating environment, the characteristics of the external components, breaking wire function may not operate correctly.

During the delay time of over-charge voltage, if the breaking wire is detected, the over-charge detect operation is once cancelled, and the breaking wire operation will be dominant. During the breaking wire detection, even if the cell voltage becomes equal or more than the over-charge detector threshold, over-charge is not detected. In this case, after detecting breaking wire operation, if the cell voltage is still equal or more than the over-charge detector threshold, over-charge detector operation starts again. For this reason, over-charge detector output delay time may longer than 1s. (Refer to the timing chart.)

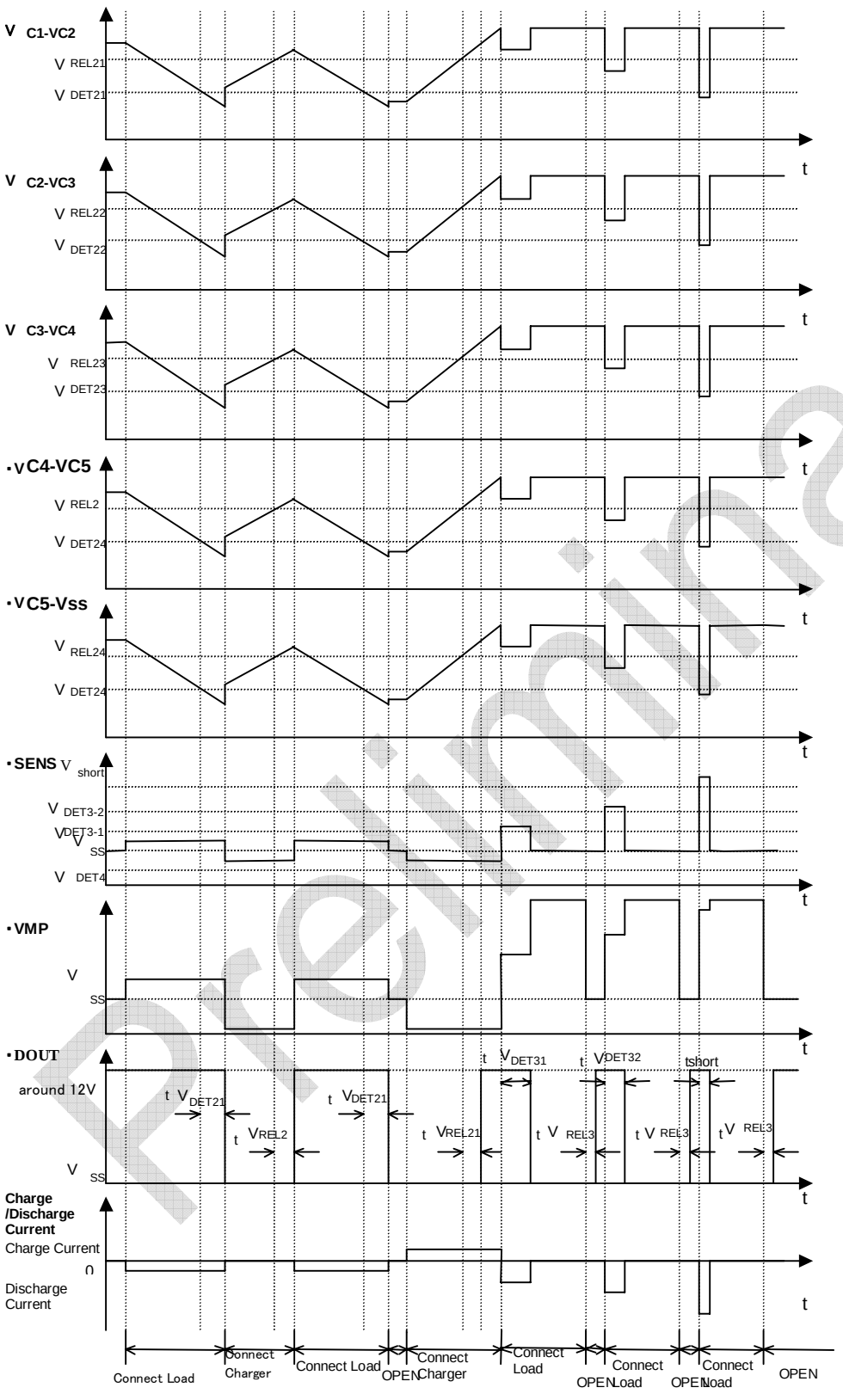
During the over-discharge delay time, if the breaking wire detector's operation starts, the over-discharge detector's operation is once cancelled and the breaking wire operation will be dominant. During the breaking wire detector's operation is active, even if the cell voltage becomes equal or less than the over-discharge detector threshold, the over-discharge detector does not start. In this case, after detecting breaking wire operation, if the cell voltage is still equal or less than the over-discharge detector threshold, over-discharge detector operation starts again. For this reason, the output delay time of over-discharge detector may be longer than the preset value. (Refer to the timing chart.)

TIMING CHART

(1) Timing diagram of Over-charge, Excess charge current

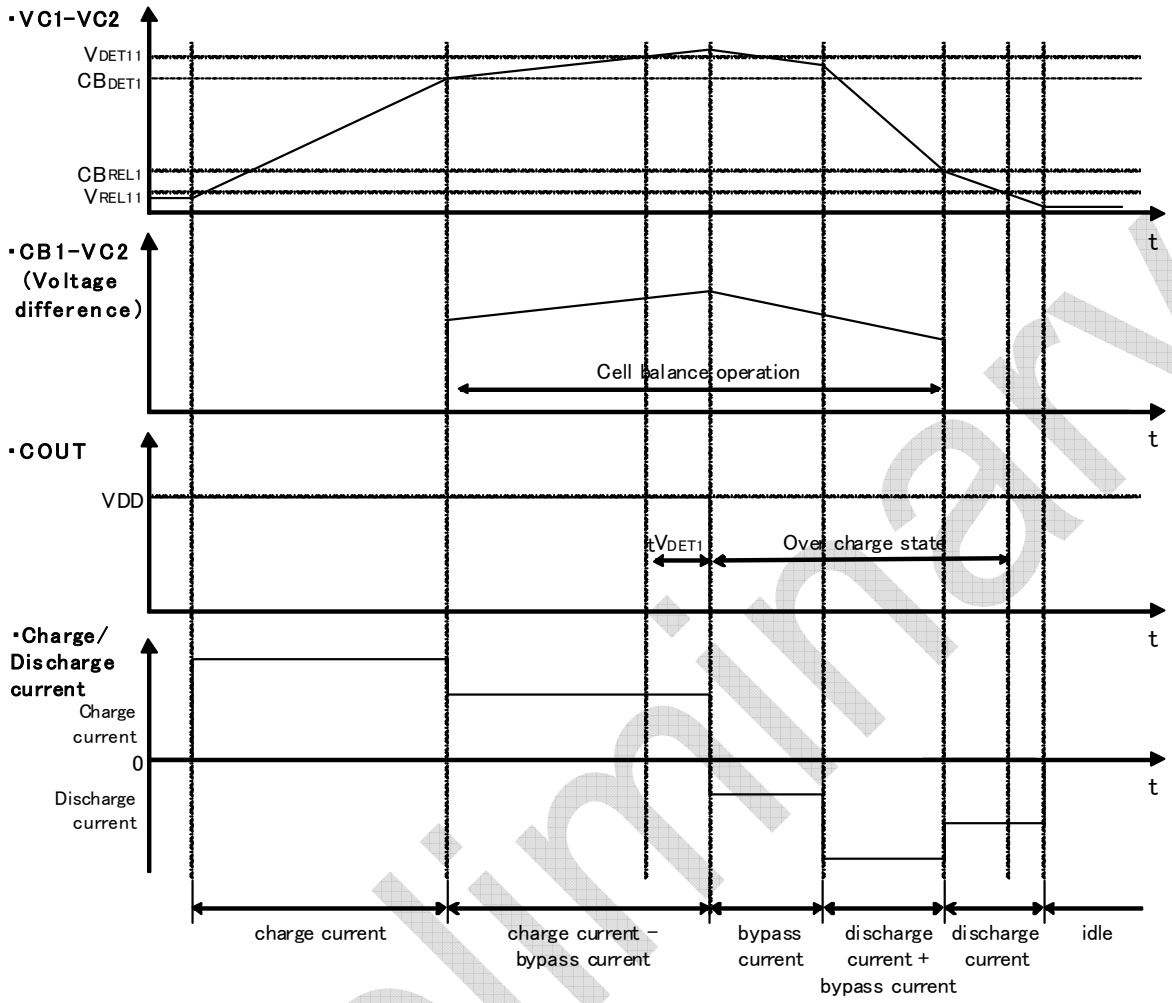


(2) Over-discharge, Excess discharge current1, 2, Short circuit

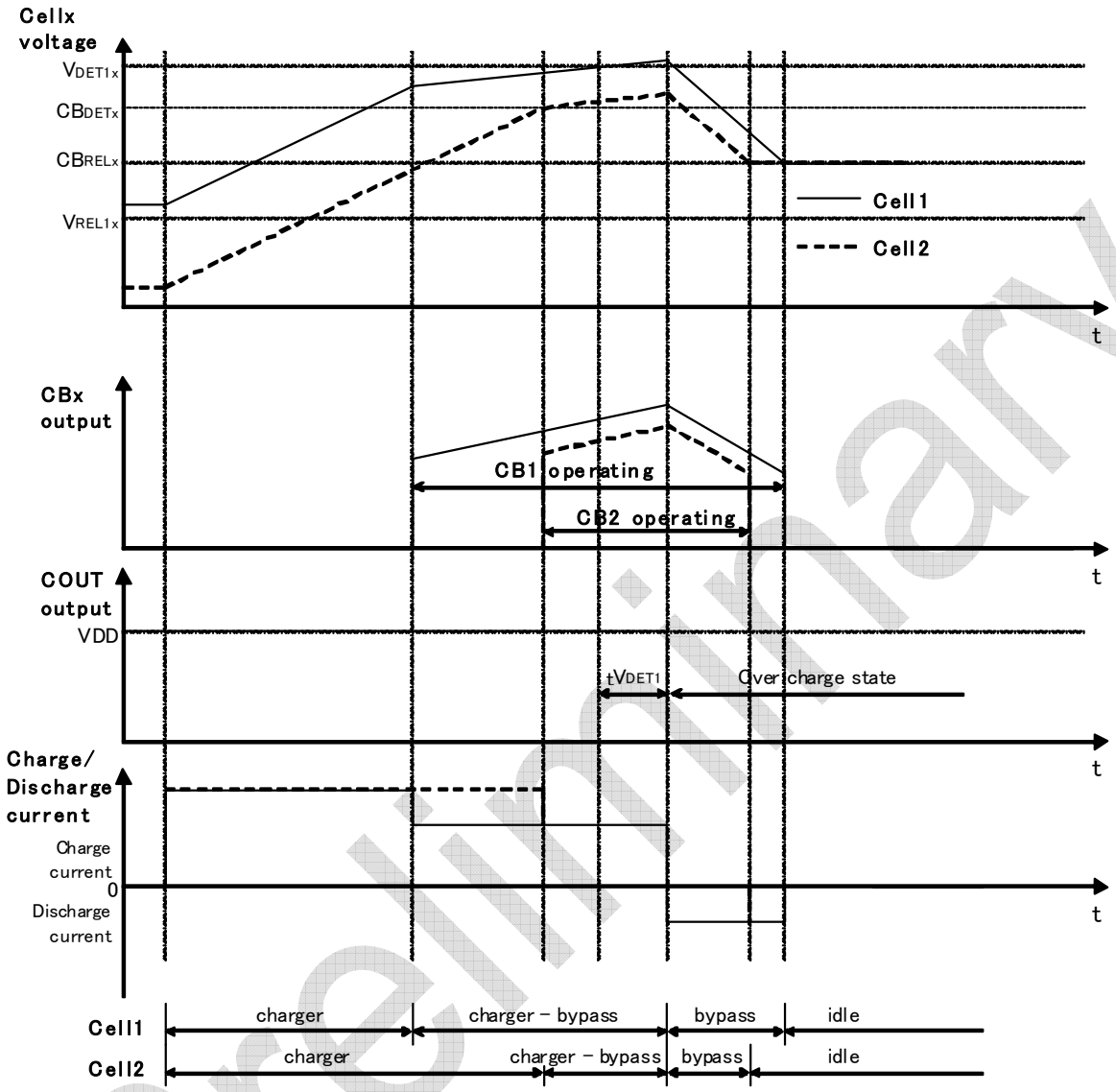


Cell balance operation

The Cell balance operation of the Cell 1



Balance operation with cell 1 and cell2



Breaking wire detector operation

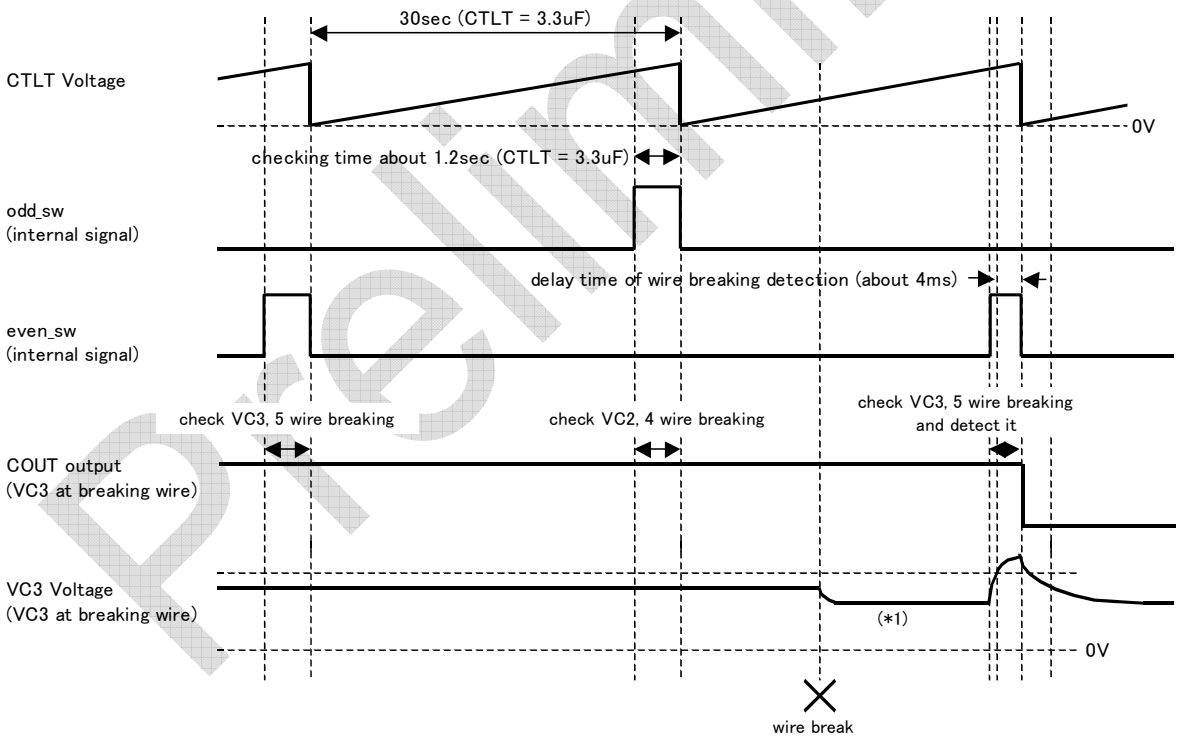
Breaking wire detector's operation of VC2, VC3, VC4, and VC5 for 5-cell protector

In case of the 3.3uF capacitor is attached to the CTLT pin, breaking wire detector operates every 30 seconds. The built in switch of VC1, VC3, VC5 cell, and the switch attached to the VC2 and VC4 turn on alternatively by the even_sw and the odd_sw signal.

The internal impedance of the cell whose switch turns on becomes low for about 1.2 seconds by the low resistance connected to the switch in serial. If the wire is not broken, the capacitor of the CTLT is discharged and the next cycle starts for checking.

While the wire is broken, the difference of the internal impedance of the IC generated by the switch's tuning on makes VC shift and the change is detected by the comparator for VDET1. If the breaking wire is detected and the condition continues for about 4ms, then even_sw and odd_sw turn off and the capacitor of CTLT is discharged and the P-channel open drain of the COUT turns off. While the over-discharge voltage is detected, the breaking wire of VC2, VC3, VC4 and VC5 does not operate.

The timing chart of breaking wire of VC2, VC3, VC4, VC5 is shown below:



(Note1) The change of VC is not always increasing. Depending on the cell balance or the internal impedance, the VC increases or decreases.

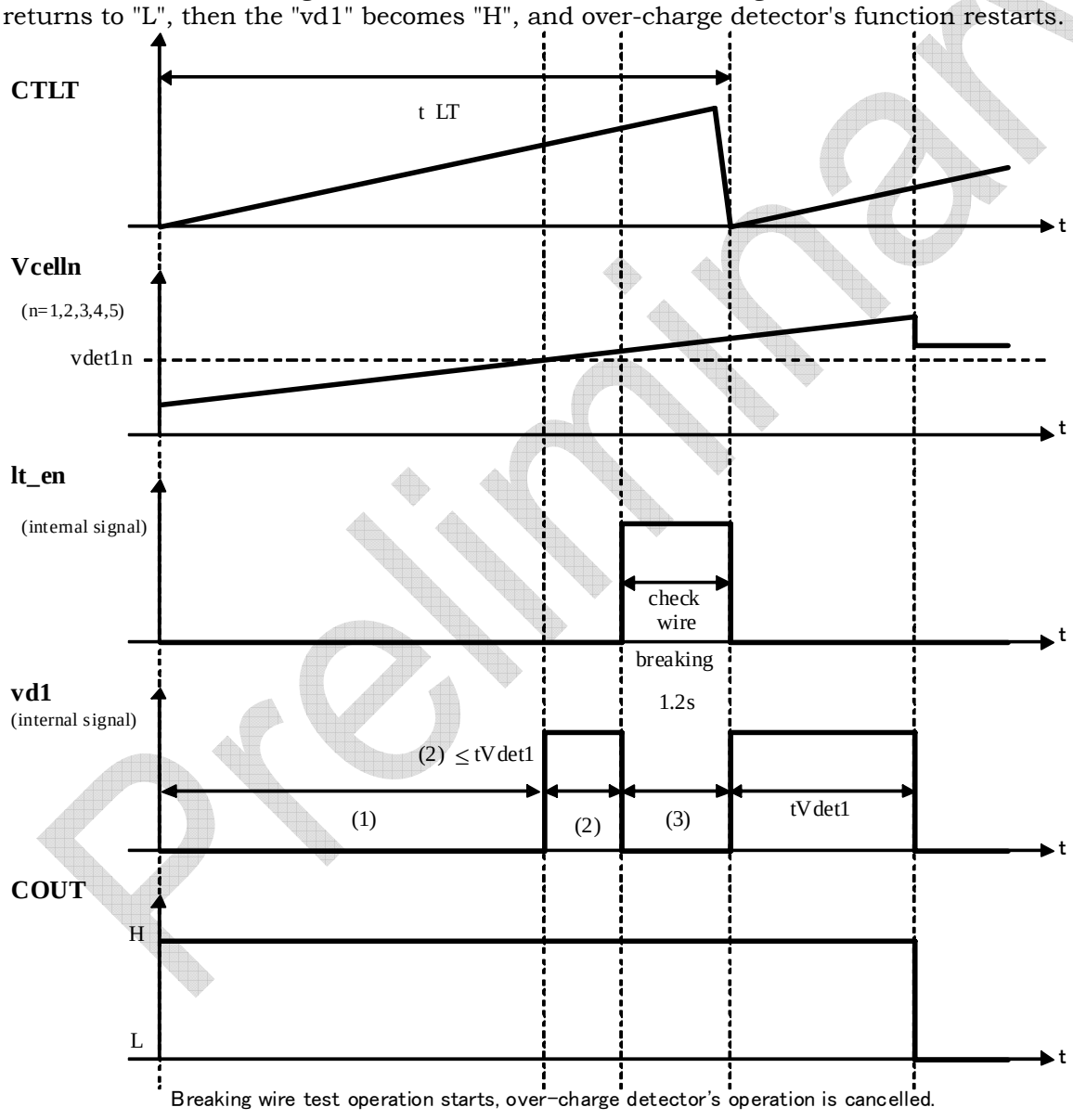
Over-charge detector operation and breaking wire detector operation

The output delay time of over-charge is normally set at 1s, however, the effect of the breaking wire detector, the output delay time may be longer than 1s.

Case 1: During the operation of detecting over-charge, if the breaking wire is detected, once the operation of the over-charge detector is cancelled, and after detecting the breaking wire, the operation of the over-charge detector starts again.

Case 2: During the operation of the breaking wire detector, if the cell voltage becomes more than the over-charge detector threshold, after detecting the breaking wire, the operation of the over-charge detector starts.

The timing chart shown below is for the operation of the case 1. When the over-charge is detected, internal node "vd1" becomes "H", then, if the breaking wire is detected, the internal node "It_en" becomes "H", then "vd1" signal returns to "L". After the breaking wire detector is released, then "It_en" returns to "L", then the "vd1" becomes "H", and over-charge detector's function restarts.



Over charge detector's maximum output delay time: Max_tVdet1 = (2)＋(3)＋tVdet1

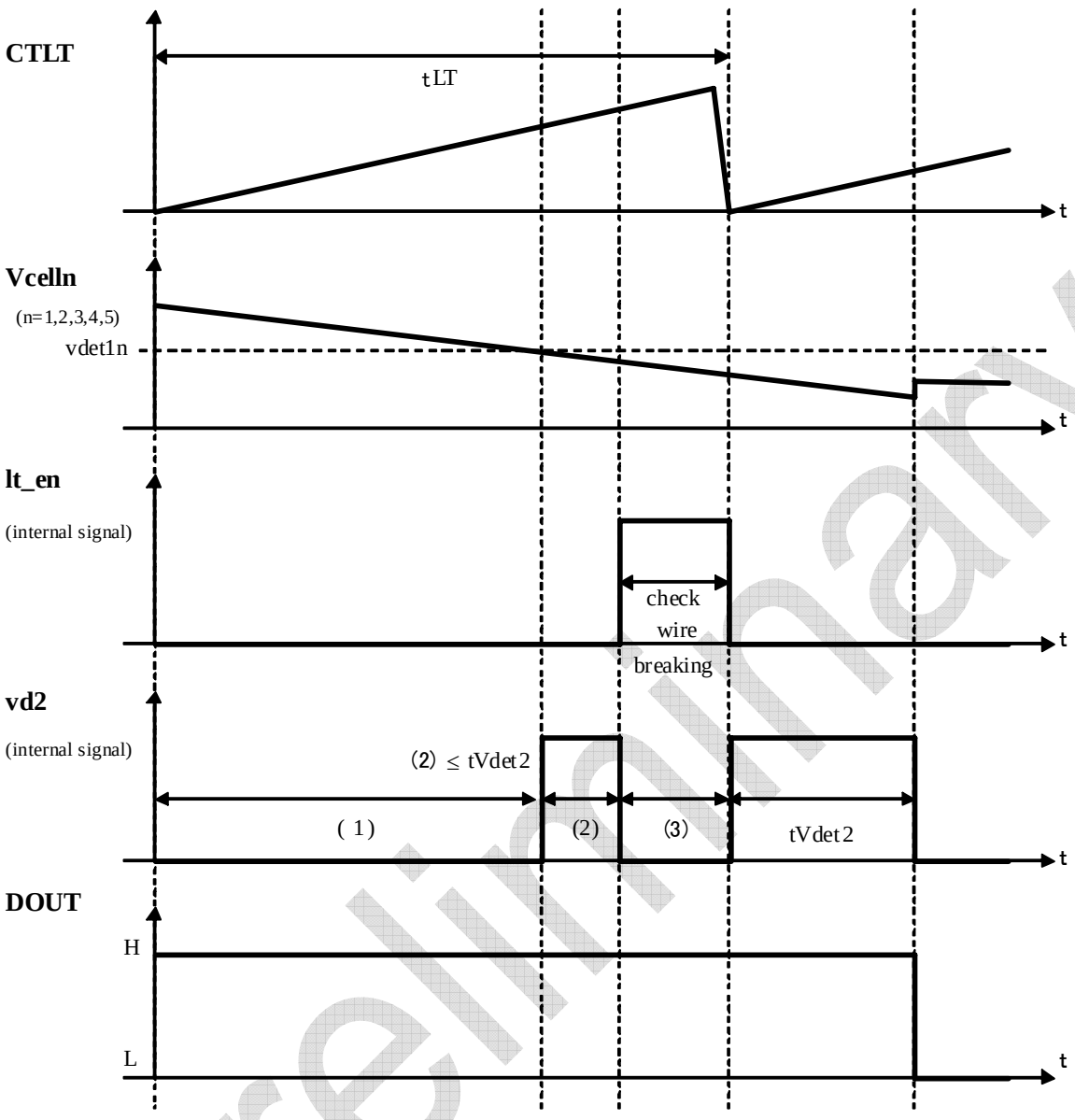
Over-discharge detector's operation and the breaking wire detector's operation

The output delay time of the over-discharge detector can be set by an external capacitor, but the delay time might be longer than the preset value due to the breaking wire detector' s operation.

Case 1: During the operation of detecting over-discharge, if the breaking wire is detected, once the operation of the over-discharge detector is cancelled, and after detecting the breaking wire's operation, the operation of the over-discharge detector starts again.

Case 2: During the operation of the breaking wire detector, if the cell voltage becomes less than the over-discharge detector threshold, after detecting the breaking wire, the operation of the over-discharge detector starts.

The timing chart shown below is for the operation of the case 1. When the over-discharge is detected, internal node "vd2" becomes "H", then, if the breaking wire is detected, the internal node "It_en" becomes "H", then "vd2" signal returns to "L". After the breaking wire detector is released, then "It_en" returns to "L", then the "vd2" becomes "H", and the over-discharge detector's function restarts.



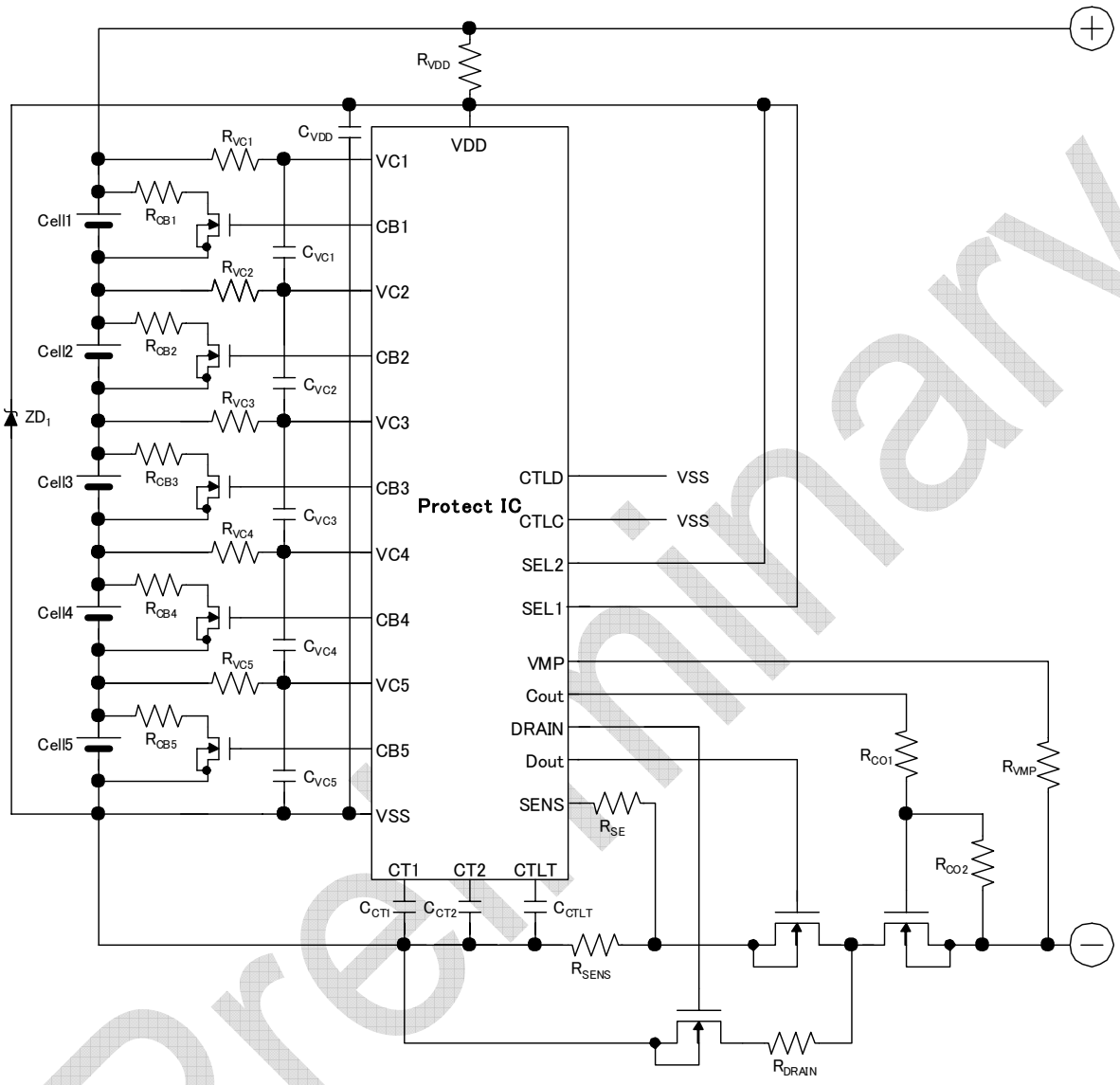
When the breaking wire test operation starts, over-discharge operation is cancelled.

Maximum output delay time of over-discharge detector: Max_tVdet2 = (2)+(3)+tVdet2

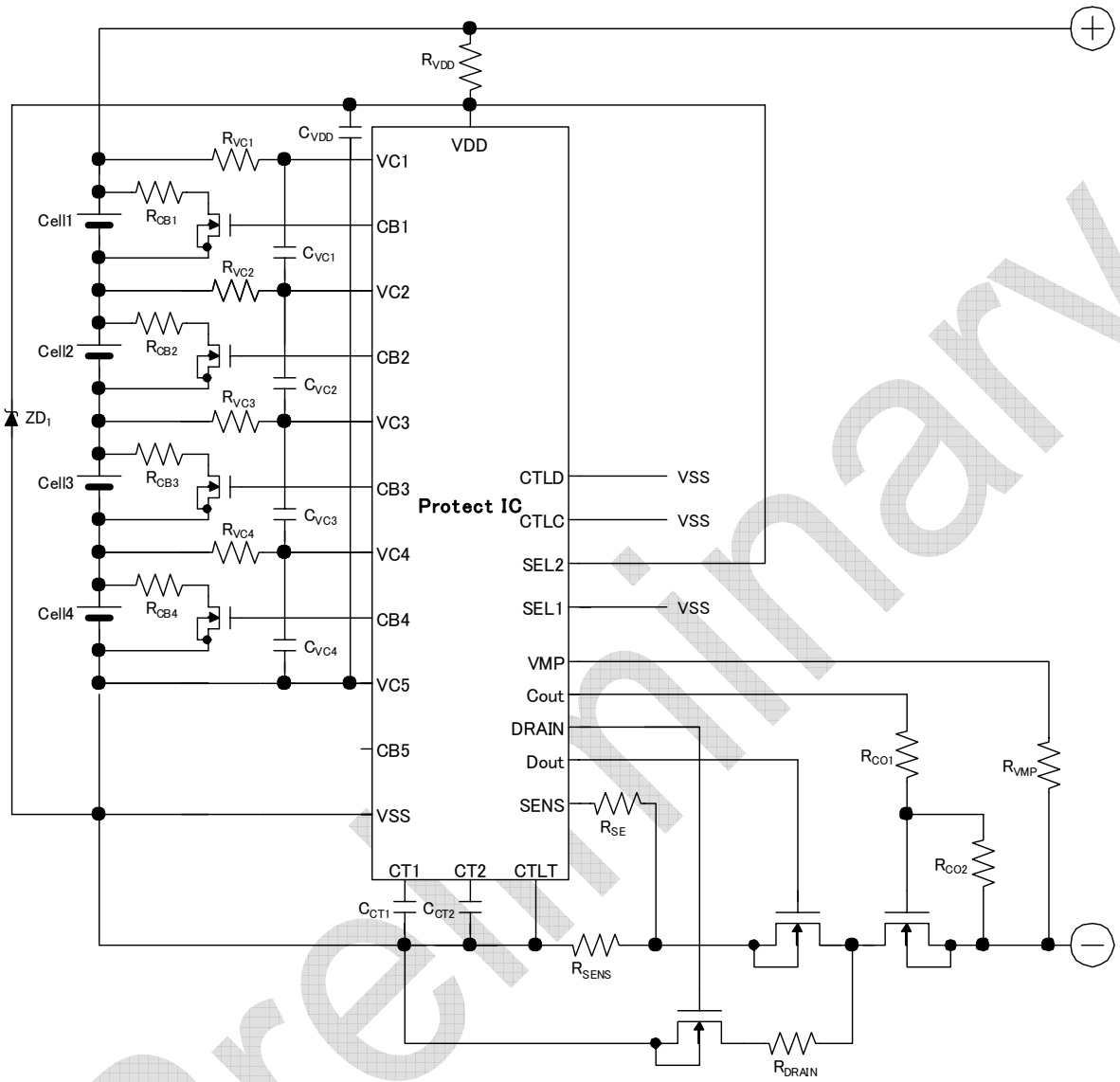
TYPICAL APPLICATION AND TECHNICAL NOTES

*Circuit example (R5432VxxxBA)

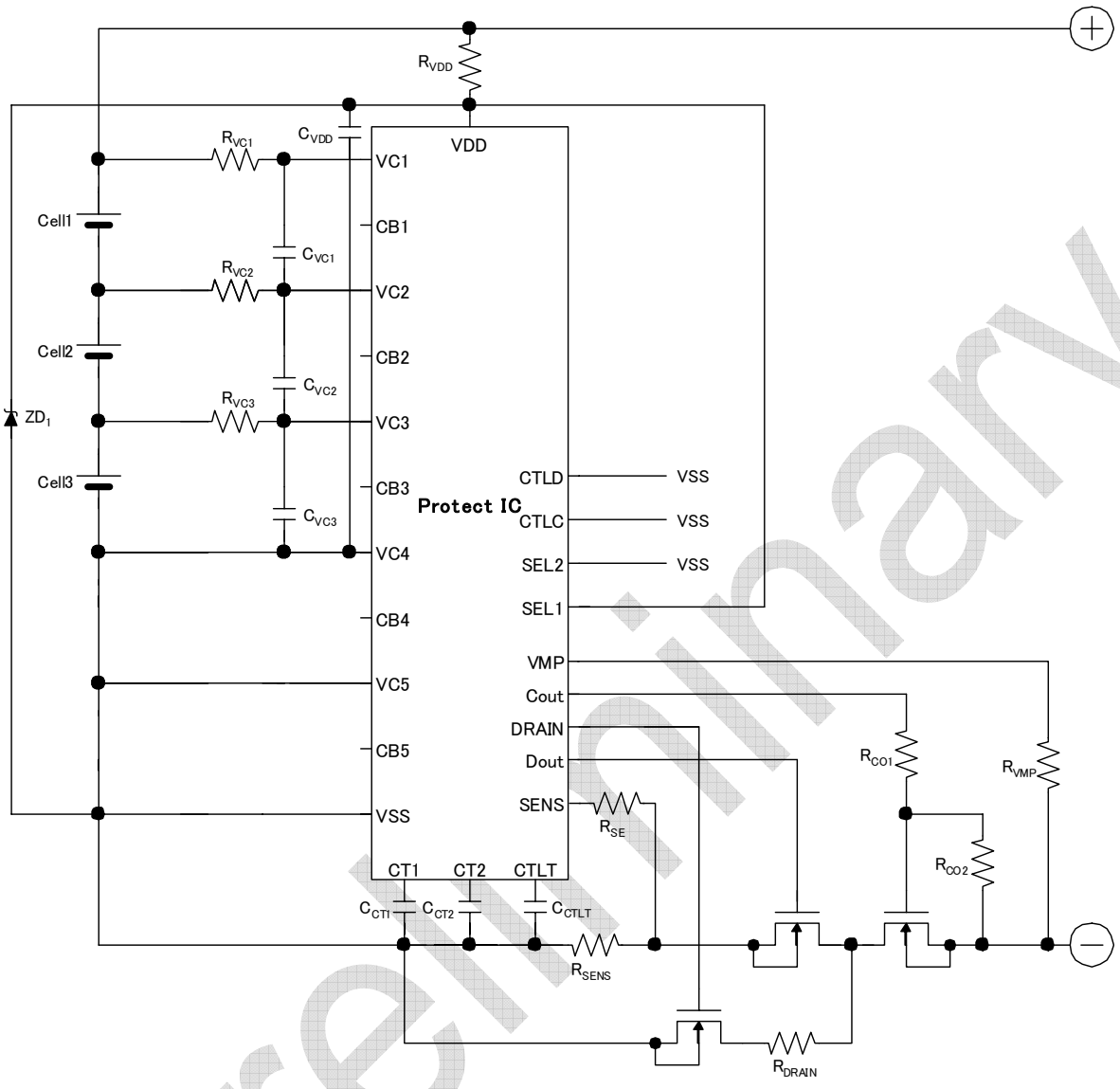
5-cell protection, with breaking wire and cell balance function



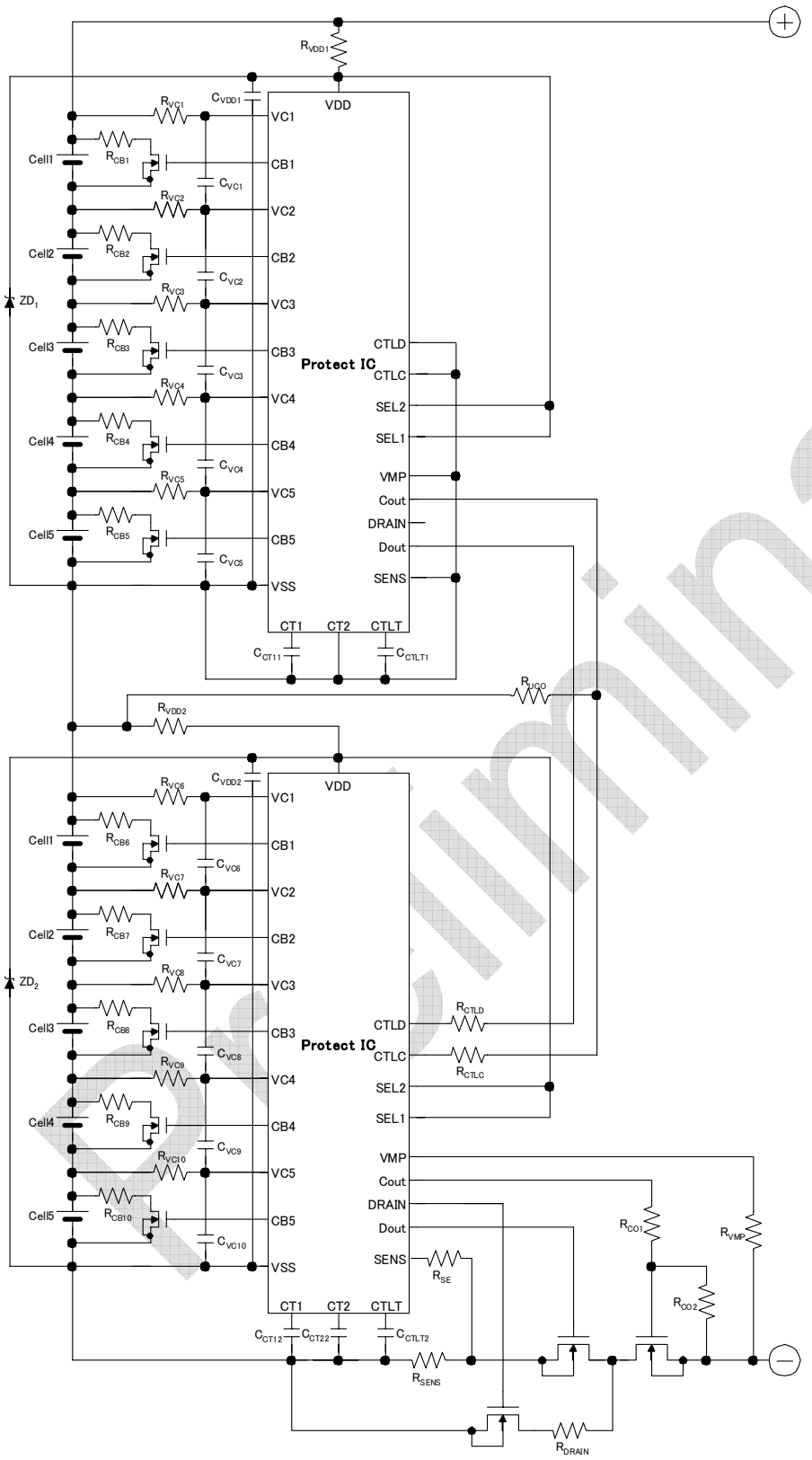
*Circuit example (for 4-cell protection with breaking wire detector without cell balance function)



*Circuit example (for 3-cell protection with breaking wire detector without cell balance function)



∗Circuit Example (for 10-cell protection, with cell balance function and breaking wire detector



If the breaking wire detector is used, for Vss of the high side IC or VDD of the low side IC, these two

lines must be separated. If they are common, the both pins' breaking wire cannot be detected. Refer to the operation explanation.

External Components values

Symbol	Value	Unit	Estimated Range	Notes
R_{VDD}	330	Ω	330 to 1000	*1
R_{VC1}	330	Ω	330 to 1000	*2
R_{VC2}	330	Ω	330 to 1000	*2
R_{VC3}	330	Ω	330 to 1000	*2
R_{VC4}	330	Ω	330 to 1000	*2
R_{VC5}	330	Ω	330 to 1000	*2
R_{CB1}	100	Ω	40 or more	*3
R_{CB2}	100	Ω	40 or more	*3
R_{CB3}	100	Ω	40 or more	*3
R_{CB4}	100	Ω	40 or more	*3
R_{CB5}	100	Ω	40 or more	*3
R_{SENS}	100	mΩ	1 or more	determined by the value of over current
R_{SE}	10	kΩ	10 or more	*4
R_{DRAIN}	10	kΩ	*5	*5
R_{CO1}	1	MΩ	*5	*5
R_{CO2}	2	MΩ	*5	*5
R_{VMP}	10	MΩ	0.01 to 10	*6
R_{CTLC}	1	kΩ	1 to 10	
R_{CTLD}	1	kΩ	1 to 10	
R_{UCO}	3	MΩ		*7
C_{VDD}	1	µF	0.1 to 1	*1
C_{VC1}	0.1	µF	0.1	*2
C_{VC2}	0.1	µF	0.1	*2
C_{VC3}	0.1	µF	0.1	*2
C_{VC4}	0.1	µF	0.1	*2
C_{VC5}	0.1	µF	0.1	*2
C_{CT1}	0.47	µF	0.01 to 1.0	*8
C_{CT2}	0.0033	µF	0.0022 or more	*9
C_{CTLT}	3.3	µF	3.3	*10
ZD_1	30	V		*11

Technical Notes on the external circuits and components

*1) The voltage fluctuation is stabilized with R_{VDD} and C_{VDD}. If a small R_{VDD} is set, in the case of the large transient may happen to the cell voltage, by the flowing current, the IC may be unstable. If a large R_{VDD} is set, by the consumption current of the IC itself, the voltage difference between VDD pin and VC1 pin is generated, and unexpected operation may result. Therefore, the appropriate value range of R_{VDD} is from 330Ω to 1kΩ. To make a stable operation of the IC, the appropriate value range of C_{VDD} is from 0.1μF to 1.0μF.

*2) R_{VC1} to R_{VC10}, C_{VC1} to C_{VC10} stabilize the voltage fluctuation. If large R_{VC1} to R_{VC10} is set, the detector threshold will be high because of the internal conduction current of the IC. The operation error of breaking wire detector function may happen easily by the distribution of the ICs or environment. If small R_{VC1} to R_{VC10} is set, the effect by noise will be large. Therefore the appropriate value range of R_{VC1} to R_{VC10} is from 330Ω to 1kΩ. To make stable operation, use 0.1μF as C_{VC1} to C_{VC10}.

*3) When the cell balance function is necessary, RCB1 to RCB10 must be chosen carefully with considering the bypass current, and consumption power by the bypass current, and the external MOSFET. Especially, if a small resistance (to set the large bypass current) is set, fully evaluation is necessary. If a large resistance (to set the small bypass current) is set, the time for cell balance will be long.

*4) When the cascade connection is used, if short circuit is happened, by the short current and the RSENS enlarges the voltage, and as a result, if the voltage of SENS pin becomes larger than the VDD of the IC, during the short circuit output delay time, the current flows into SENS pin. Therefore, if a small R_{SE} is set, a large current may flow into SENS pin. If a large R_{SE} is set, the over-current detector threshold may shift. Therefore the appropriate value is around 10kΩ.

*5) Choose appropriate values for R_{DRAIN}, R_{CO1}, and R_{CO2} to satisfy the next formula, otherwise, the release from excess discharge current and short may be impossible.

$R_{DRAIN} < V_{DET31} \times (R_{CO1}+R_{CO2})/50$

If small R_{CO1} or R_{CO2} is set, when the output of C_{OUT} is "H", the consumption current of protection circuit board increases. If large R_{CO1} or R_{CO2} is set, when the output of C_{OUT} is "Hi-Z", the speed for pull-down the gate of the charge FET becomes slow and turning off the FET will be slow. Not only that, by dividing between the "Hi-Z" output and the resistance, turning off the charge FET may be difficult.

If a small R_{DRAIN} is set, when the excess discharge current and short circuit is detected, the large current may flow until the load is removed.

*6) In terms of R_{VMP}, when the cascade connection is made, if D_{OUT} turns off, VMP pin is pulled up via R_{VMP} to the top cell. In this case, the current flows via R_{VMP} and the internal diode, therefore, appropriate value must be chosen. If the cascade connection is not used, around 10kΩ is acceptable.

*7) Set R_{UCO} to satisfy $R_{UCO}=R_{CO1}+R_{CO2}$. If a extremely large resistance is set, when the output of C_{OUT} is "Hi-Z", by the dividing resistance, CTLC pin may not be pulled down. If a small resistance is used, when the output of C_{OUT} is "H", the consumption current via R_{UCO} increases.

*8) If the breaking wire detector function of VC2 to VC5 is used, use 0.47μF to 1μF as C_{CT1}. If the breaking wire detector function is unnecessary, use a capacitor of 0.01μF or more.

*9) If a too small C_{CT2} is set, excess discharge current detector output delay time 2 becomes shorter than the short circuit output delay time. Therefore, use a capacitor with 0.0022μF or more.

*10) If the breaking wire detector of VC2 to VC5 is used, use 3.3μF as C_{CTLT}. If the breaking wire detector of VC2 to VC5 is not necessary, pull down to VSS.

*11) Considering the break down of the resistors and capacitors to stabilize the fluctuation of the voltage, to avoid that the high voltage is directly forced to the IC, adding a zener diode is our recommendation. Connect the zener diode between VDD pin of the IC and VSS pin directly. (Refer to the typical application circuits.)

To set the number of connecting cells, SEL1/SEL2 pin must be connected to VDD level. In these cases, connect the pin inside the filter for stabilizing VDD pin voltage. If SEL1/SEL2 is connected outside the filter, during the operation, the voltage difference between SEL1/SEL2 and VDD may be generated, and unstable operation or excess current flow may result.

The typical application circuit diagrams are just examples. This circuit performance largely de-

pends on the PCB layout and external components. In the actual application, fully evaluation is necessary.

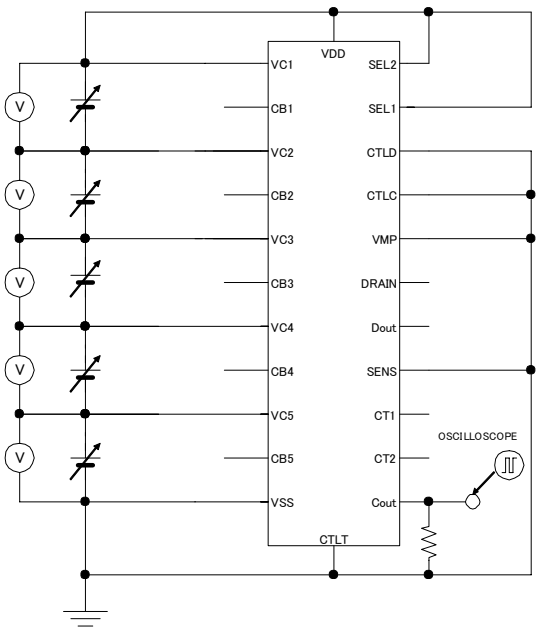
Over-voltage and the over current beyond the absolute maximum rating should not be forced to the protection IC and external components.

Ricoh cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Ricoh product. If technical notes are not complied with the circuit which is used Ricoh product, Ricoh is not responsible for any damages and any accidents.

To connect the protection IC and cells, connect VSS pin first. If the connect order is wrong, by flowing unexpected current, the IC may be damaged.

TEST CIRCUITS

A



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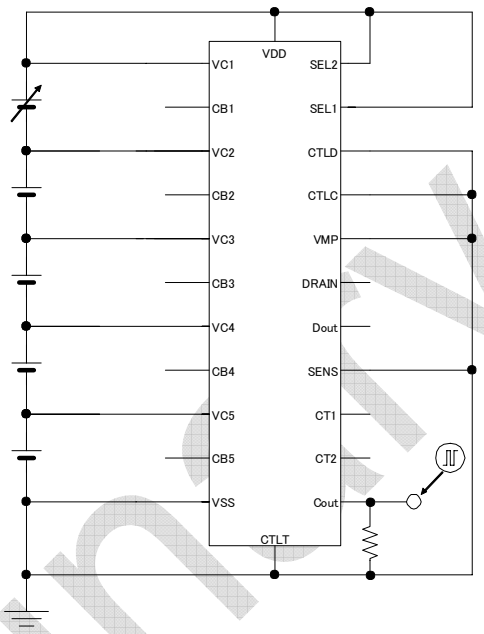

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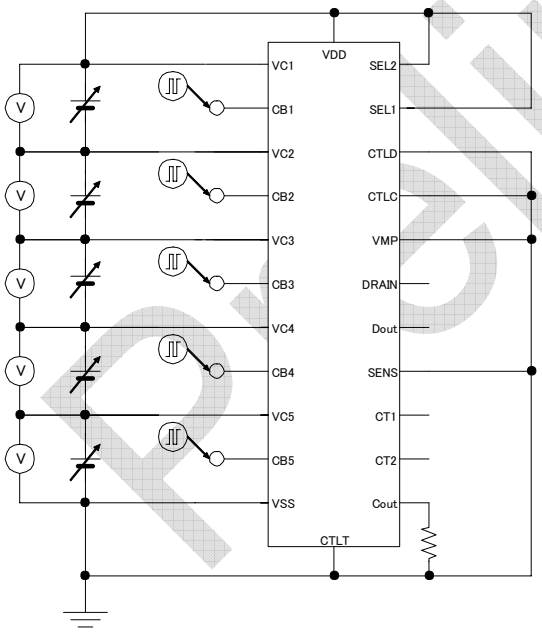

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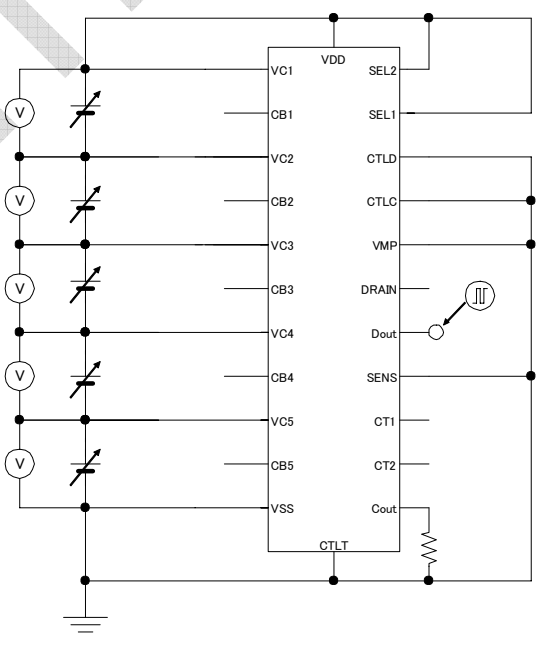

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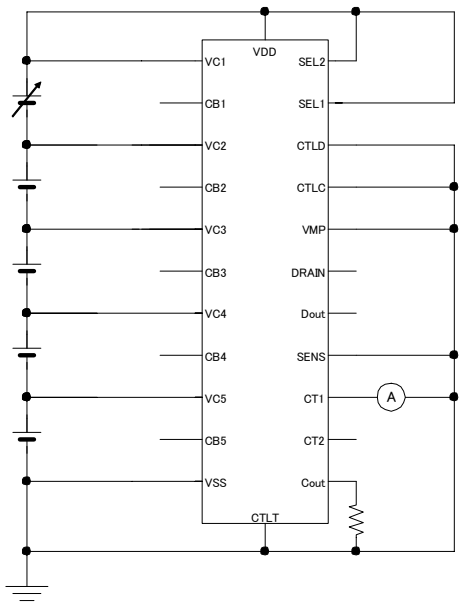

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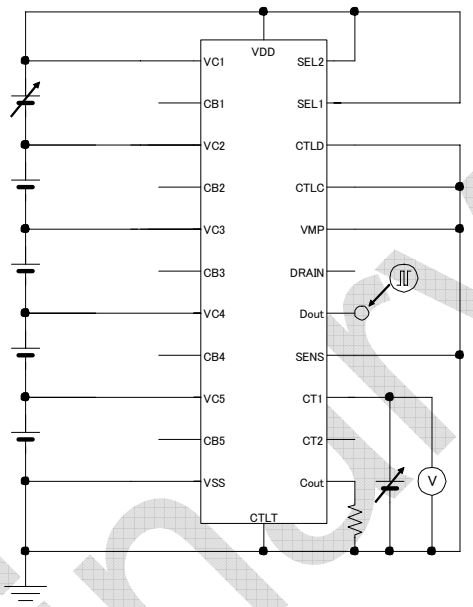

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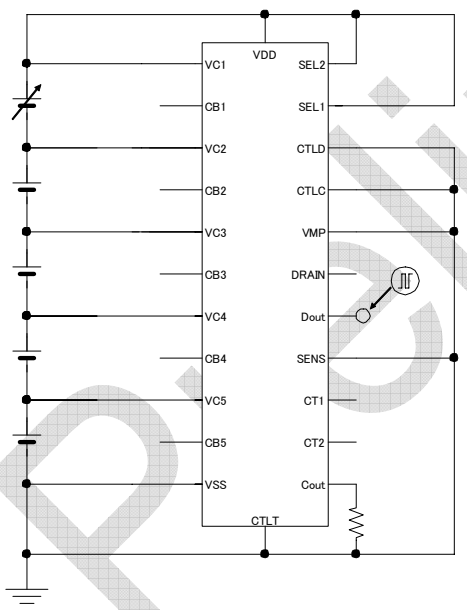

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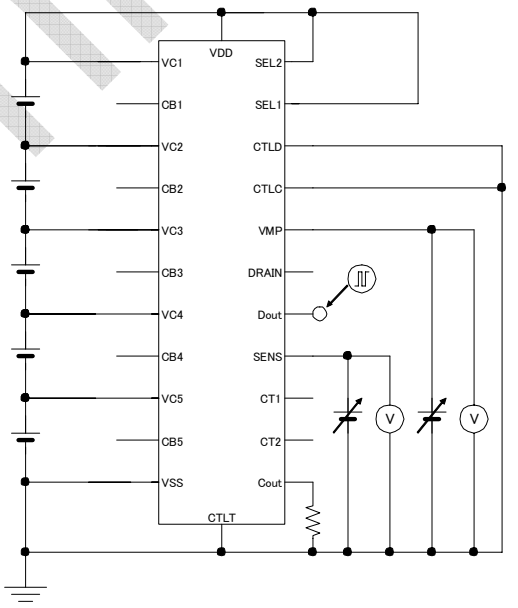

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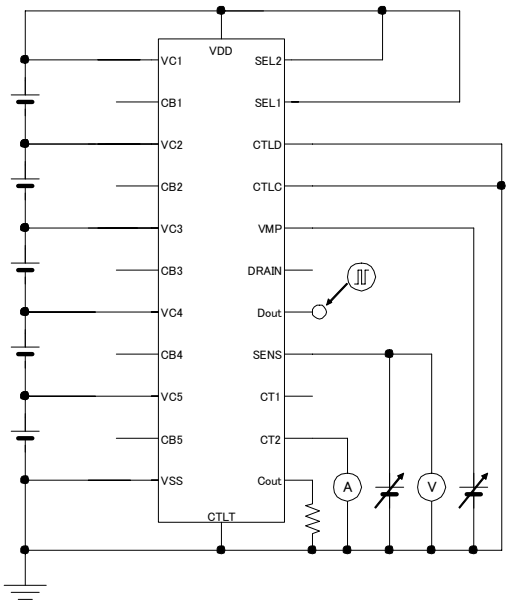

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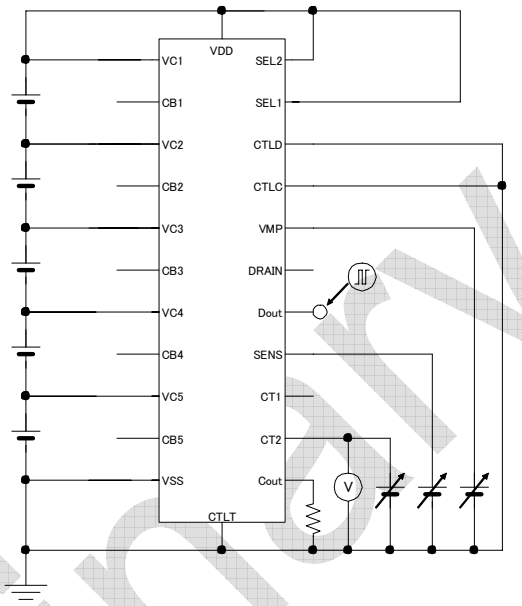

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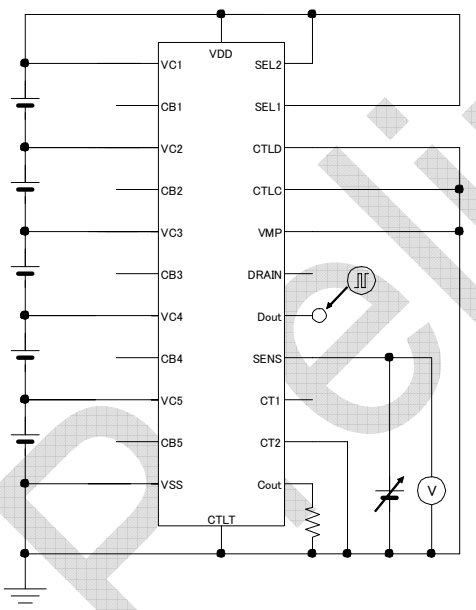

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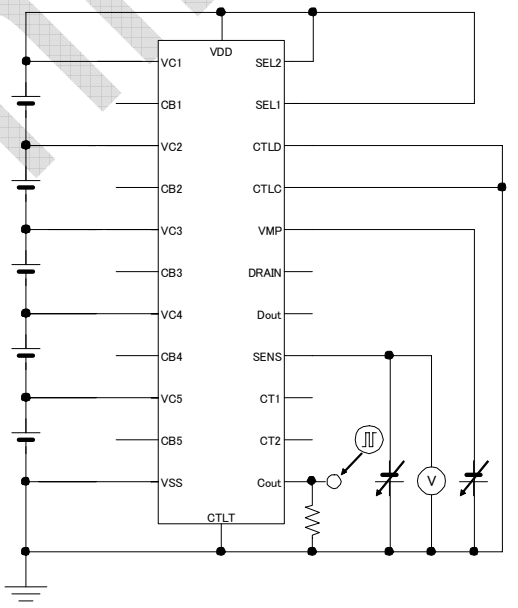

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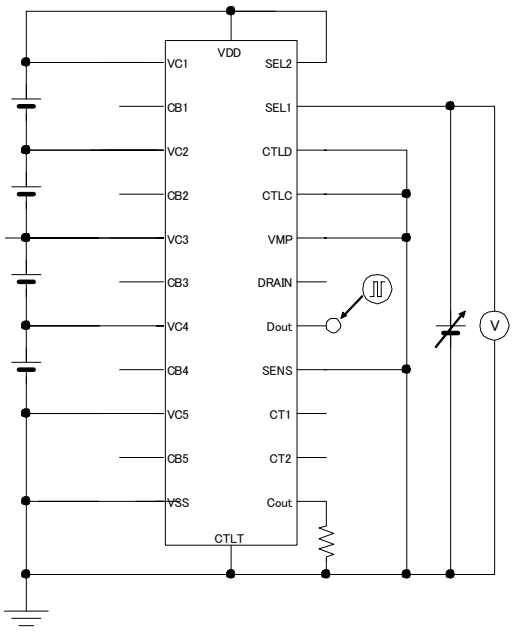

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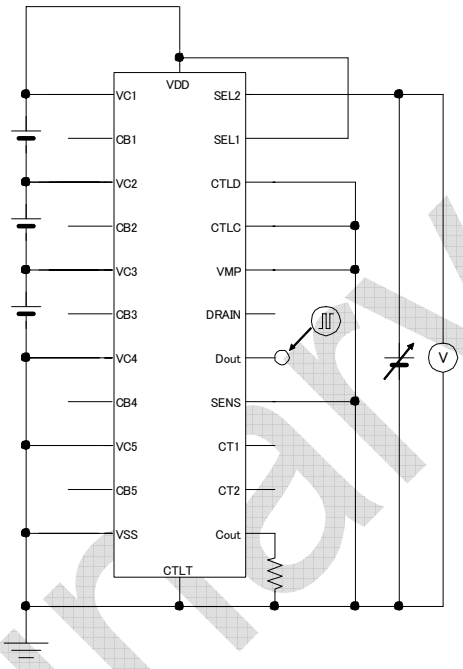

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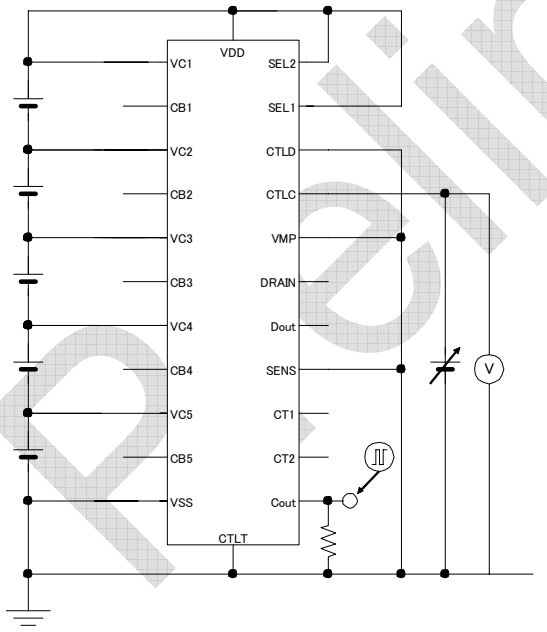

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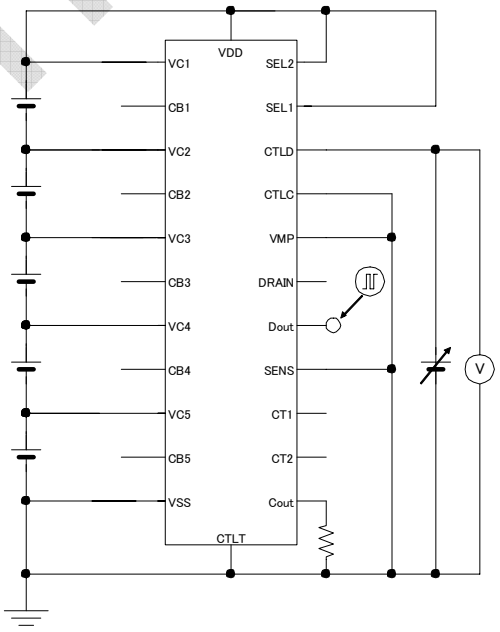

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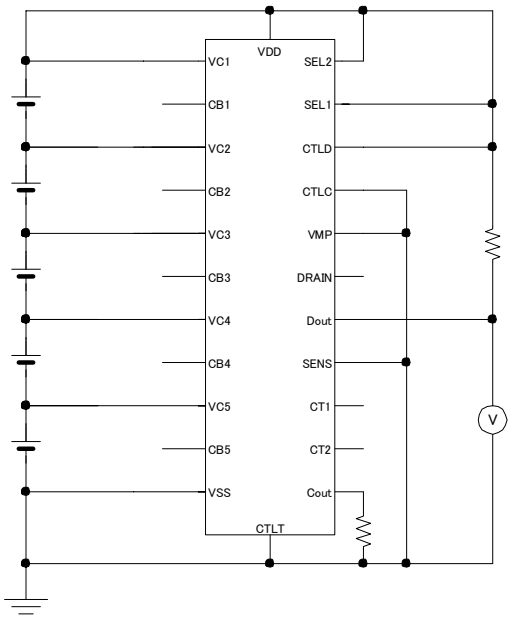

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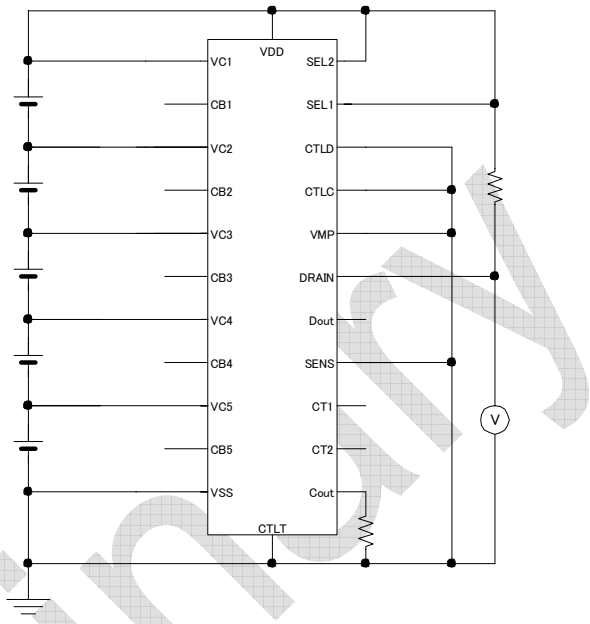

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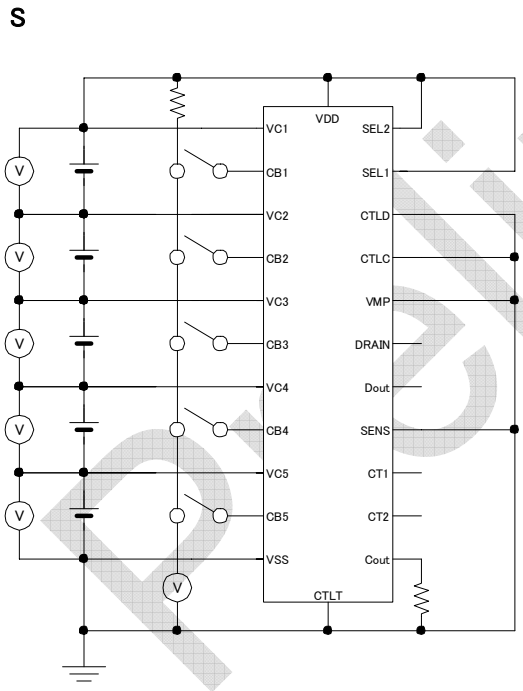

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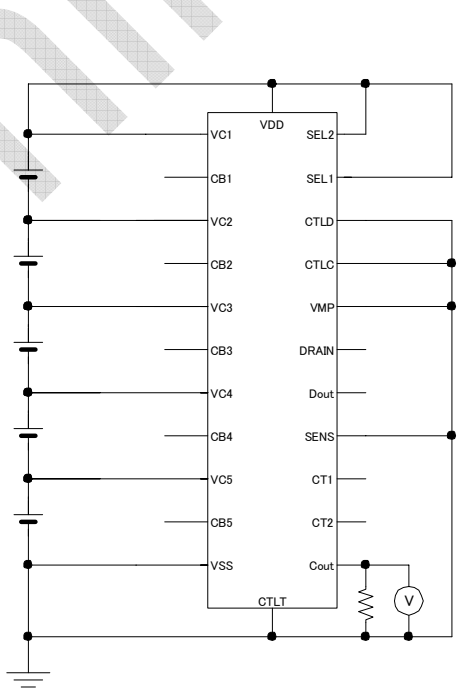

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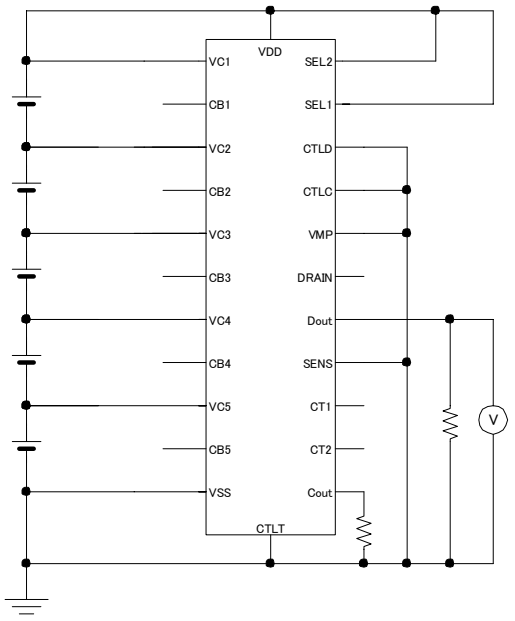

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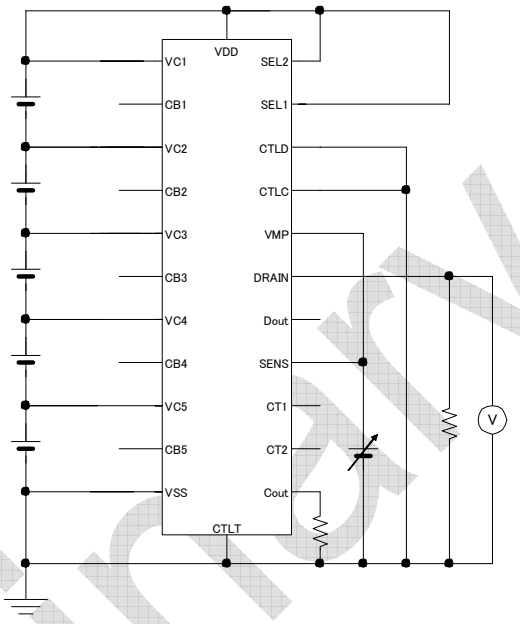

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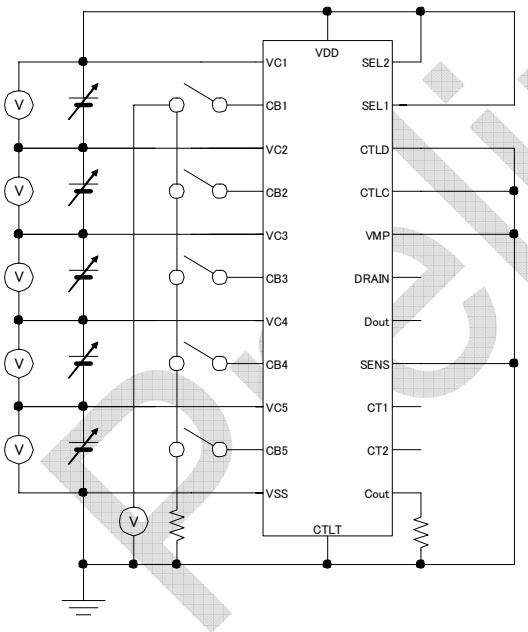

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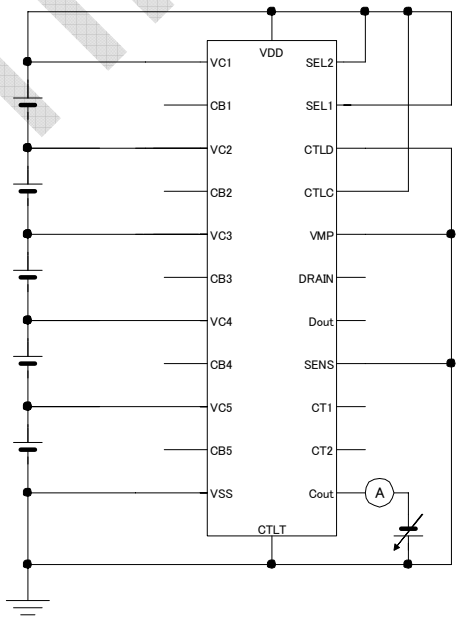

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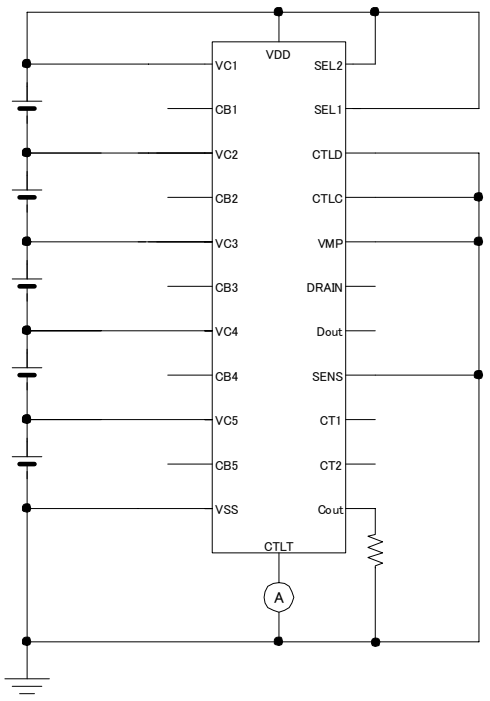

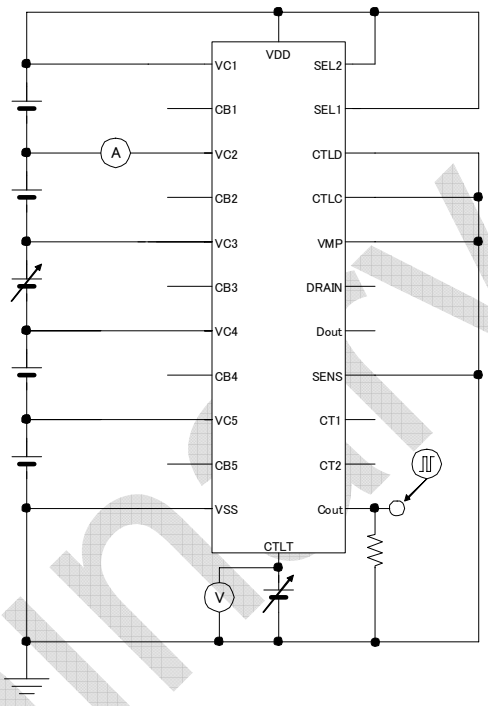

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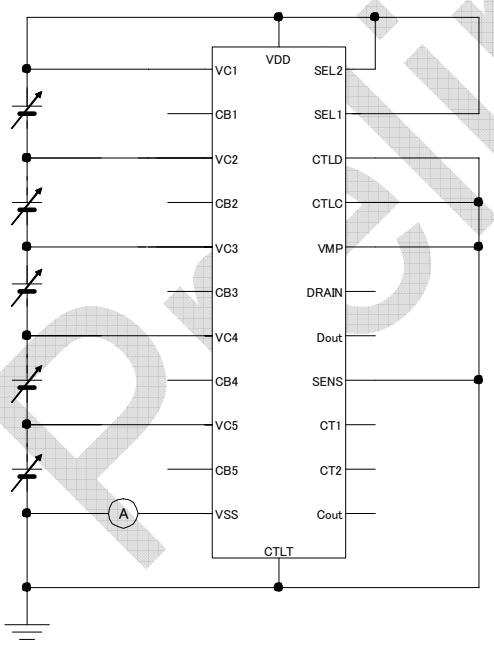
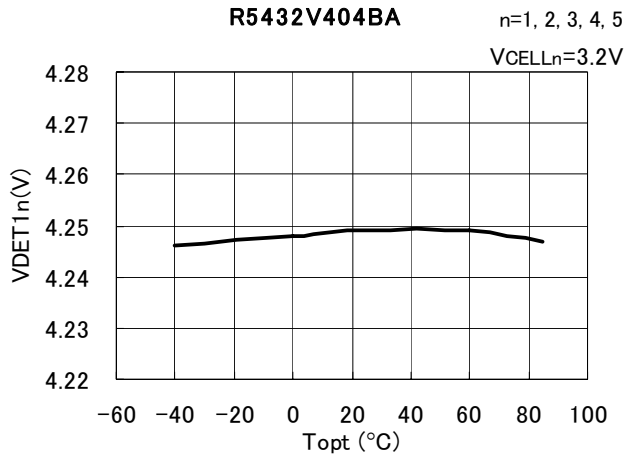


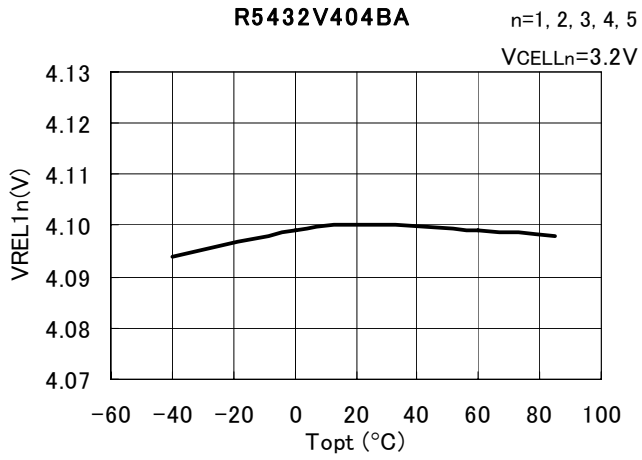
TYPICAL CHARACTERISTICS

Part1. Temperature Characteristics

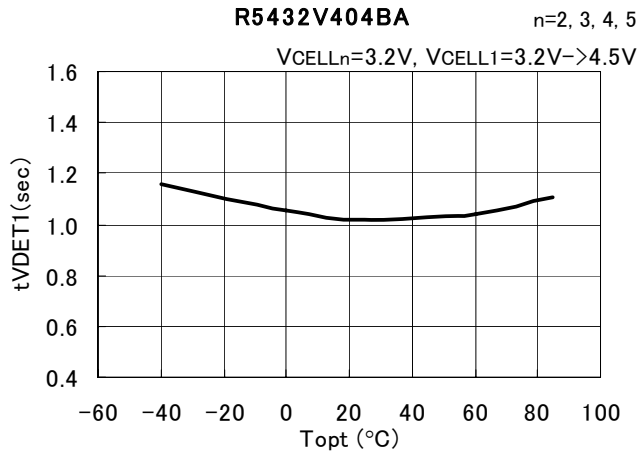
1)Cell-n Over-charge detector threshold



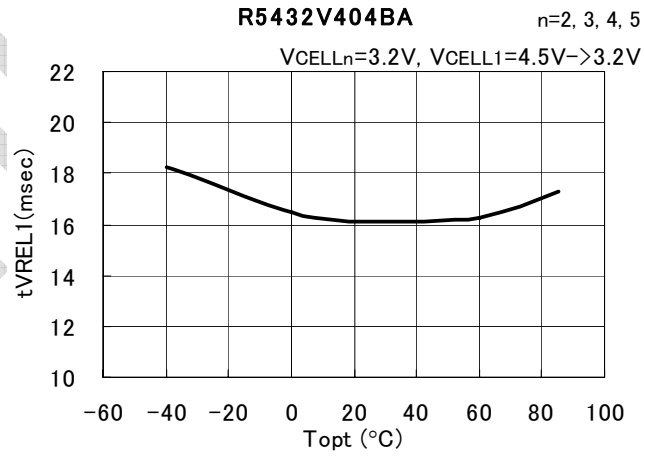
2) Cell-n Over-charge released voltage



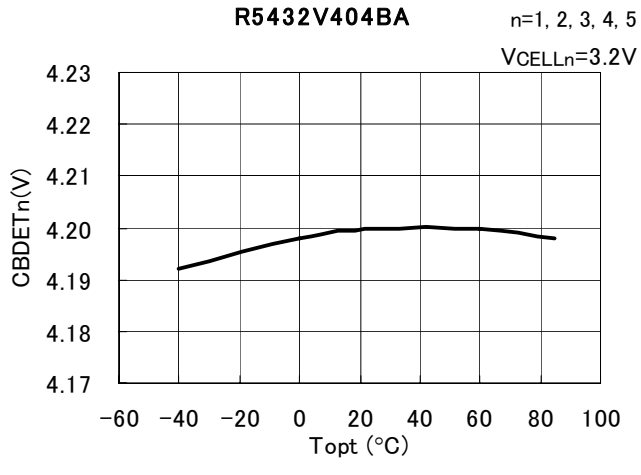
3) Cell-n Output delay time of Over-charge detector



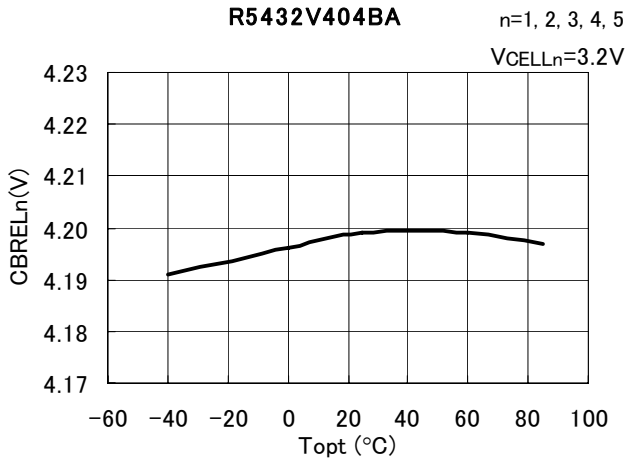
4) Cell-n output delay time for release from over-charge



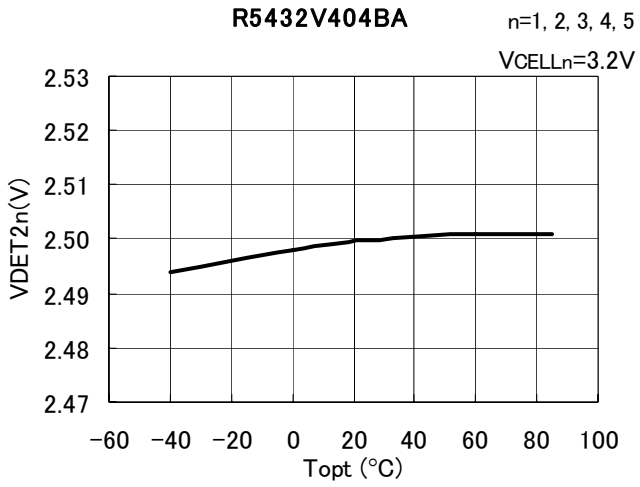
5) Cell-n cell balance detector threshold



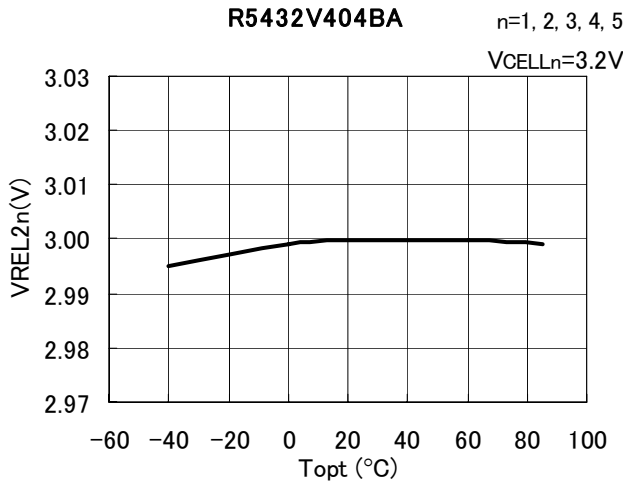
6) Cell-n cell balance released voltage



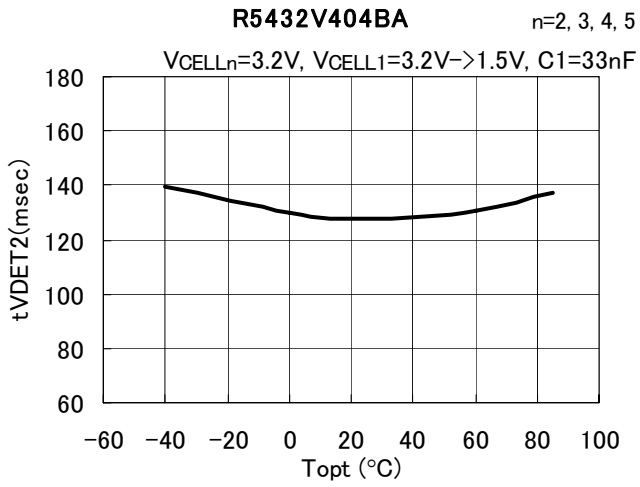
7) Cell-n over-discharge detector threshold



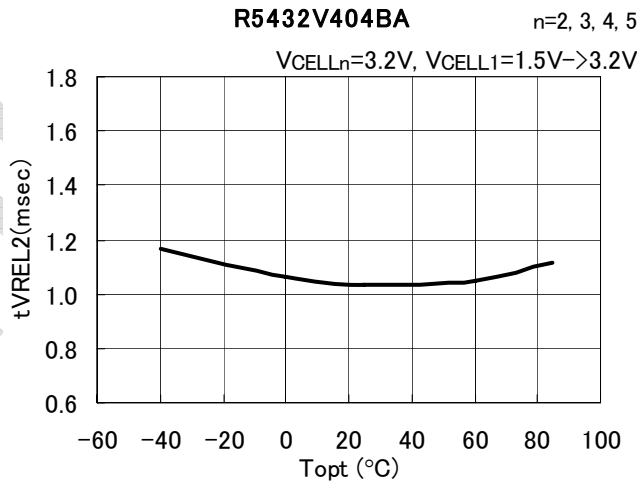
8) Cell-n released voltage from over-discharge



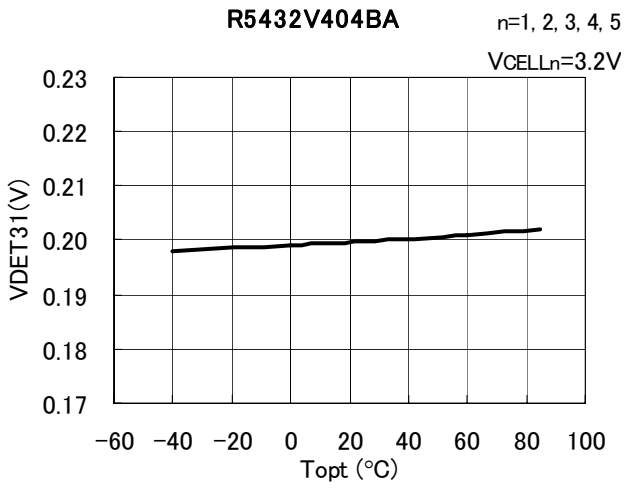
9) Cell-n over-discharge output delay time



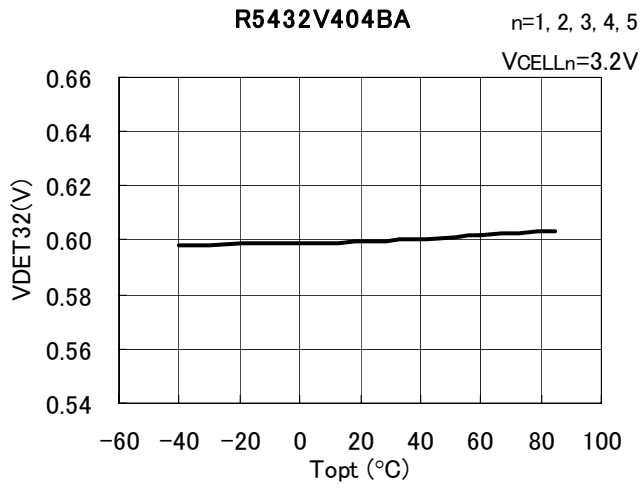
10) Cell-n over-discharge released delay time



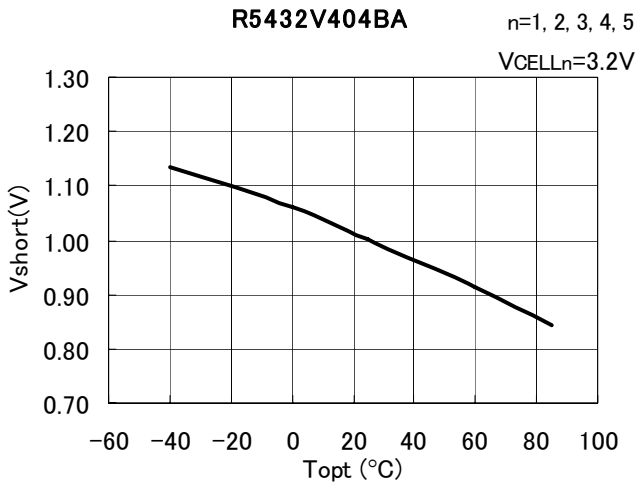
11) Over-discharge current detector threshold 1



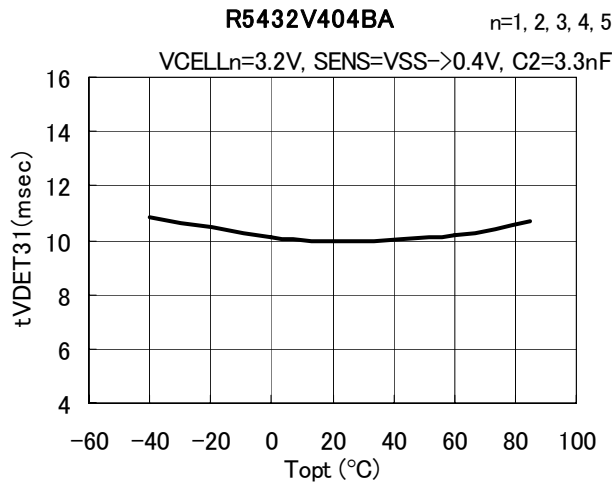
12) Over-discharge current detector threshold 2



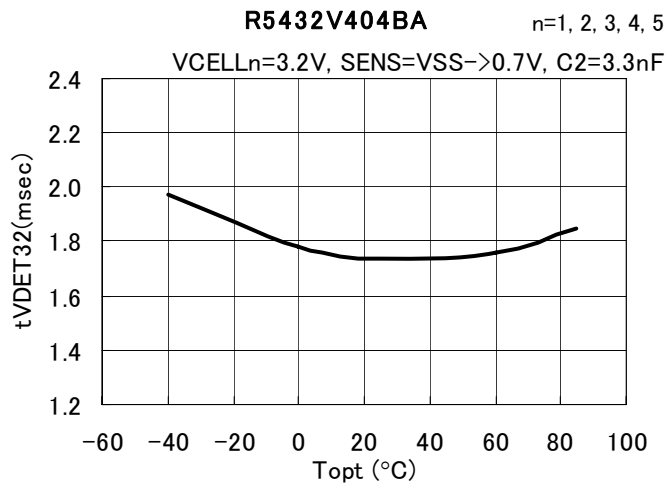
13) Short detector threshold



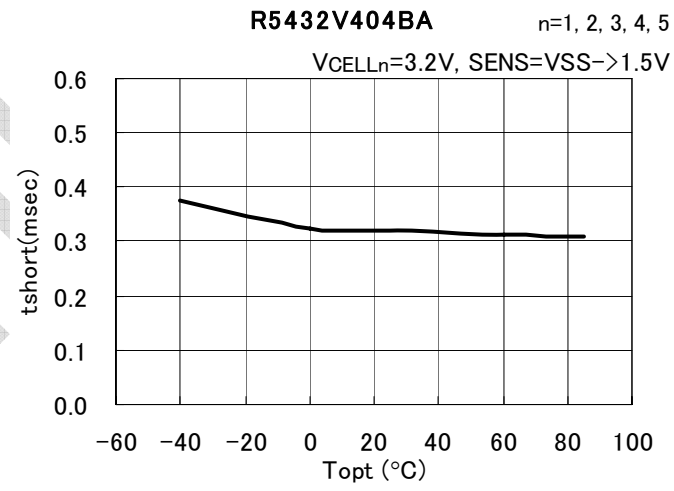
14) Excess discharge current detector output delay time 1



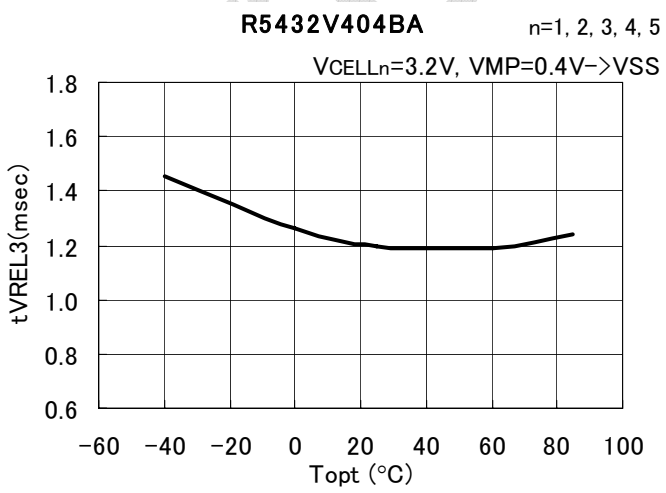
15) Excess discharge current detector output delay time 2



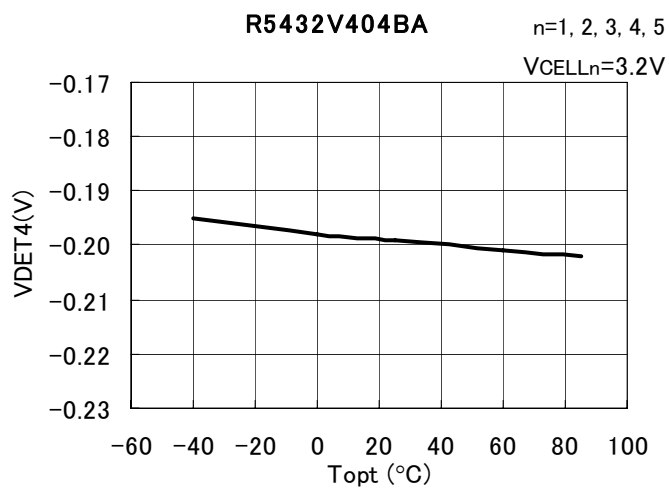
16) Short detector output delay time



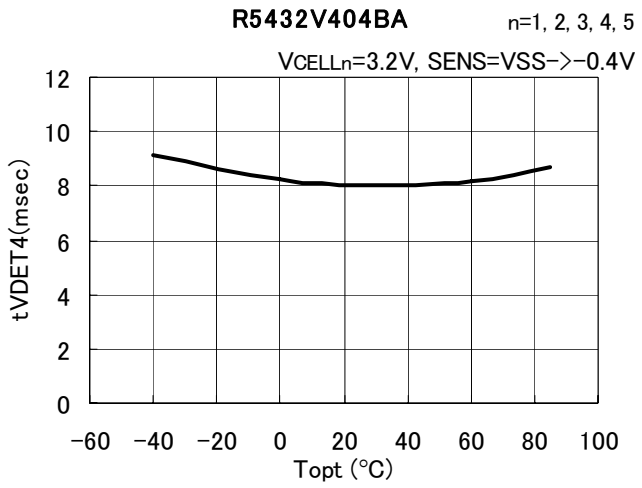
17) Excess discharge current released delay time



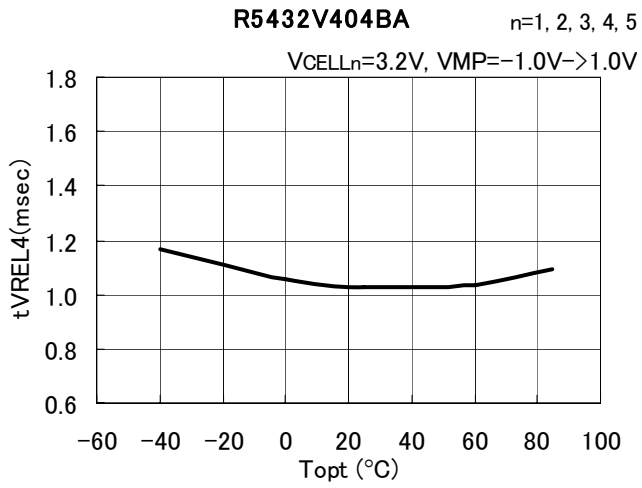
18) Excess charge current detector threshold



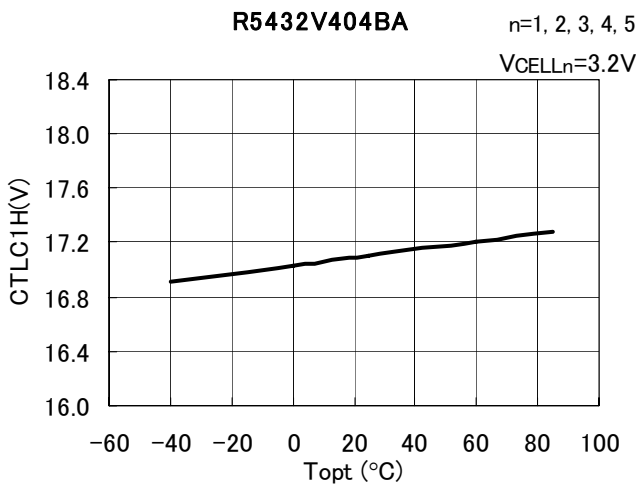
19) Excess charge current output delay time



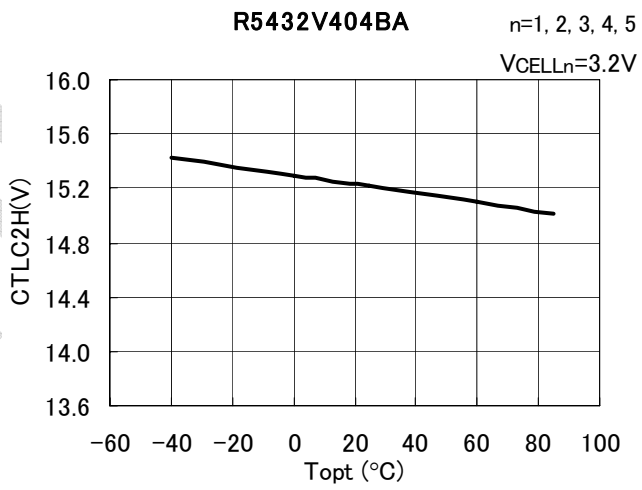
20) Excess charge current released delay time



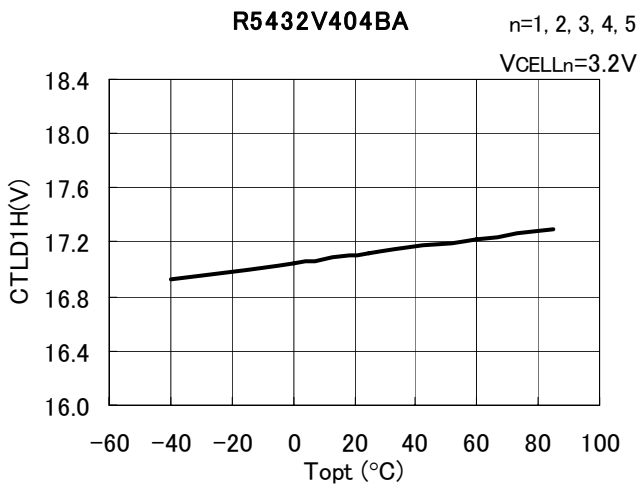
21) CTLC pin Hi1 input voltage



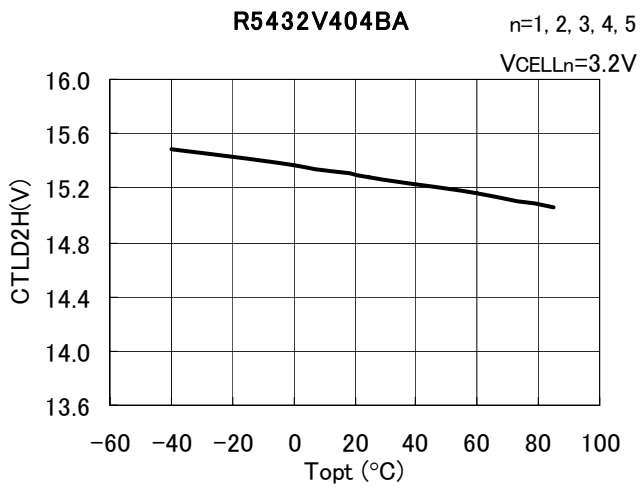
22) CTLC pin Hi2 input voltage



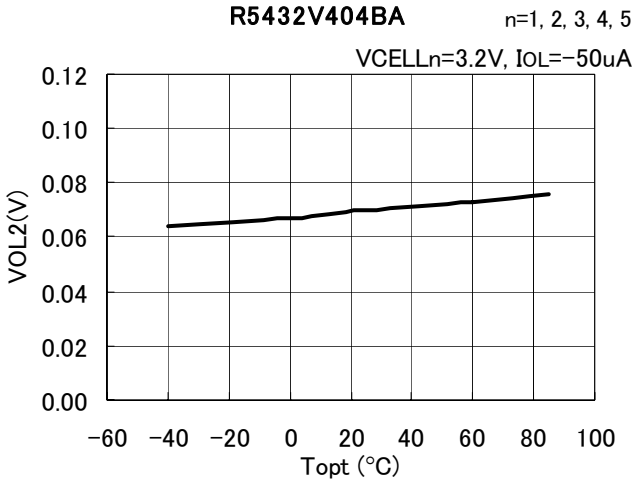
23) CTLD pin Hi1 input voltage



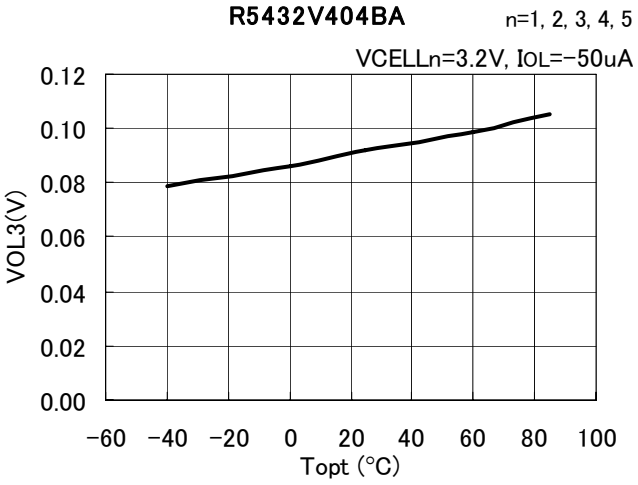
24) CTLD pin Hi2 input voltage



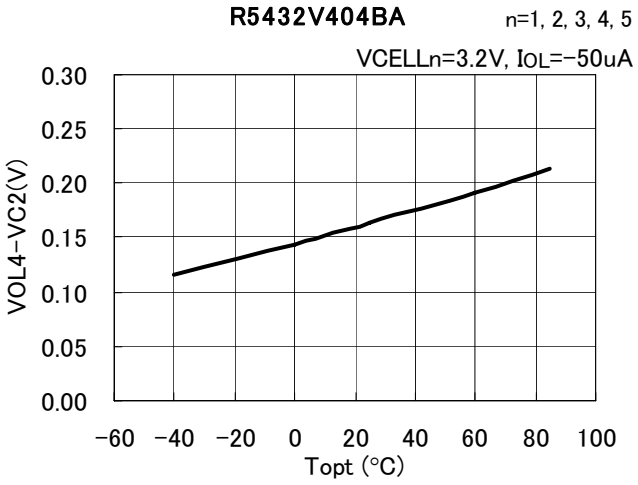
25) DOUT N-channel on voltage



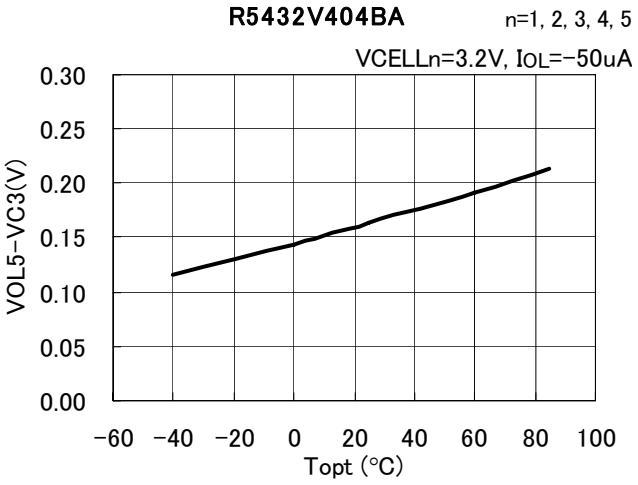
26) DRAIN N-channel on voltage



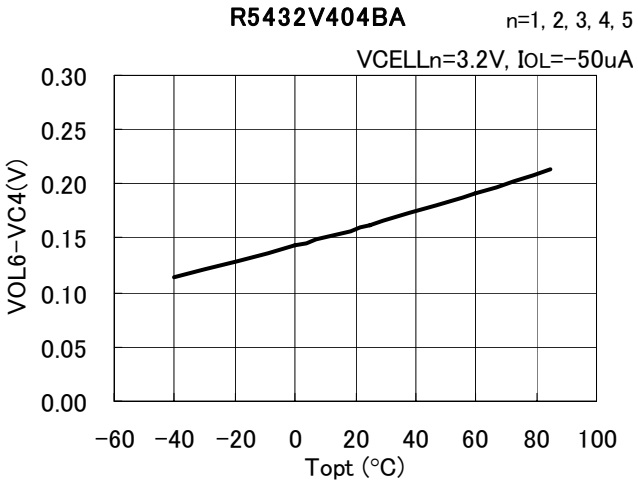
27) CB1 N-channel on voltage



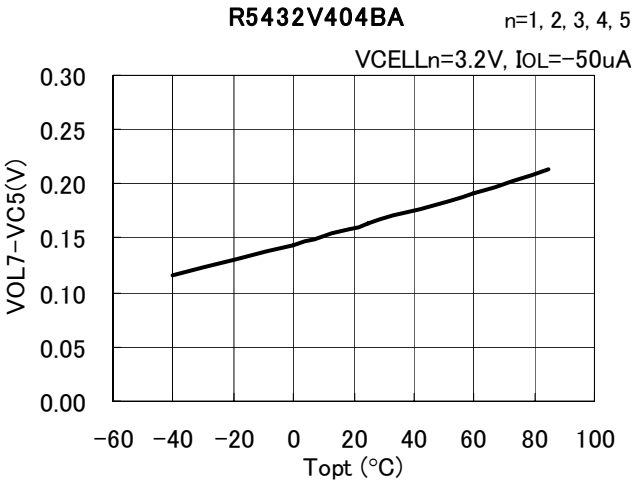
28) CB2 N-channel on voltage



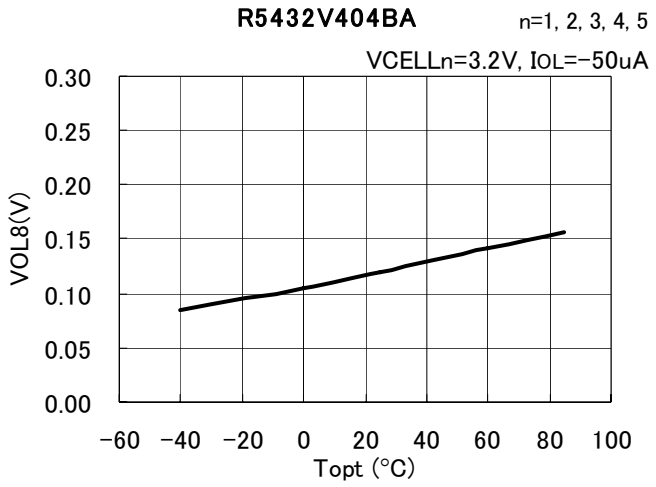
29) CB3 N-channel on voltage



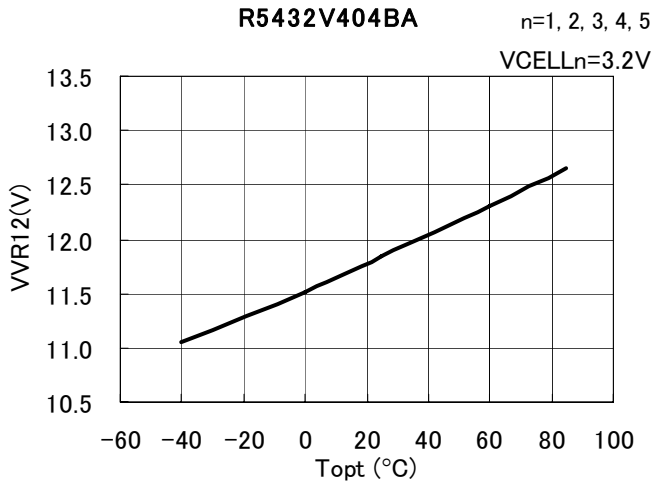
30) CB4 N-channel on voltage



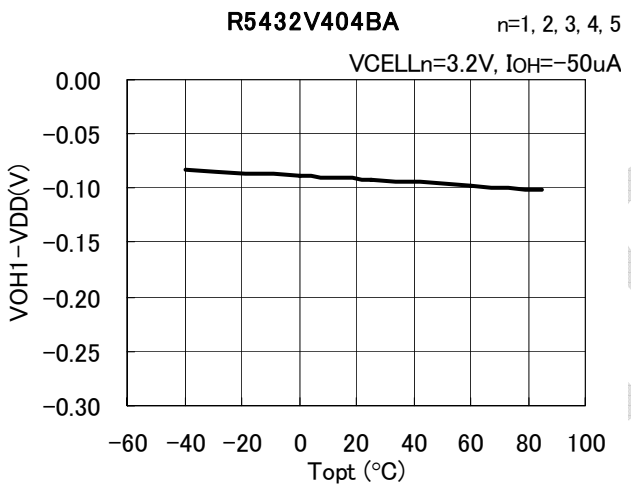
31) CB5 N-channel on voltage



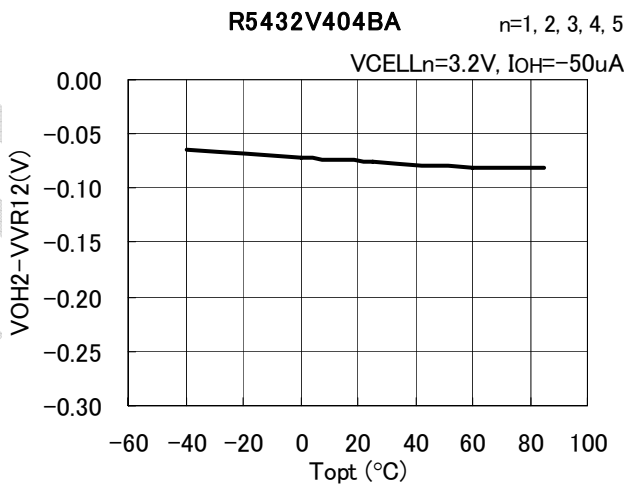
32) VR 12V output voltage



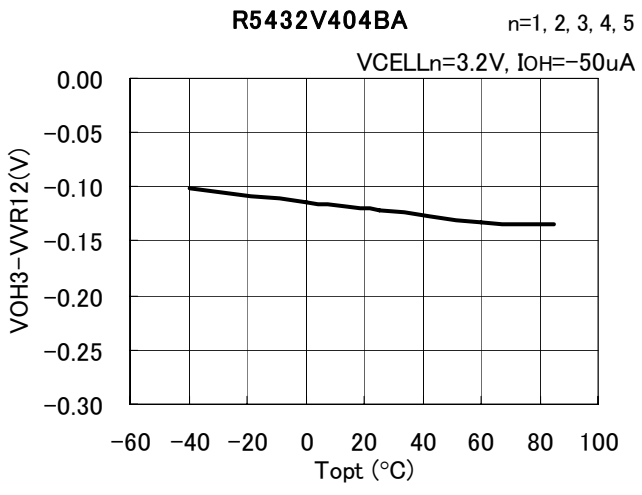
33) C_{OUT} P-channel on voltage



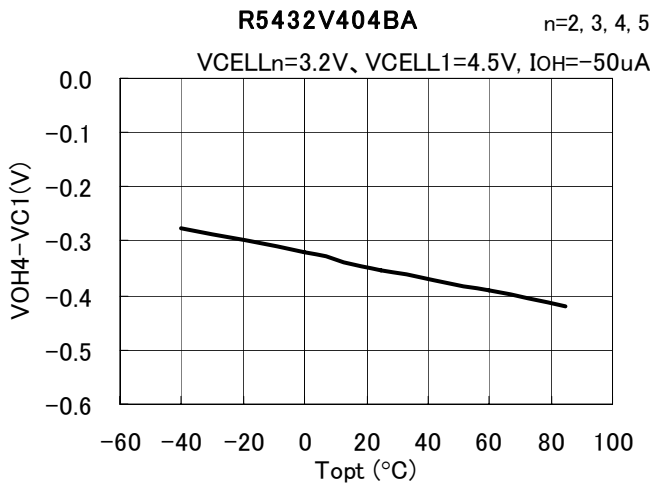
34) D_{OUT} P-channel on voltage



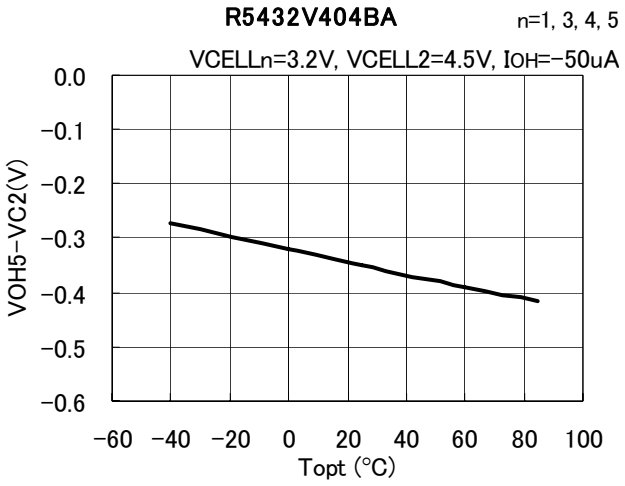
35) DRAIN P-channel on voltage



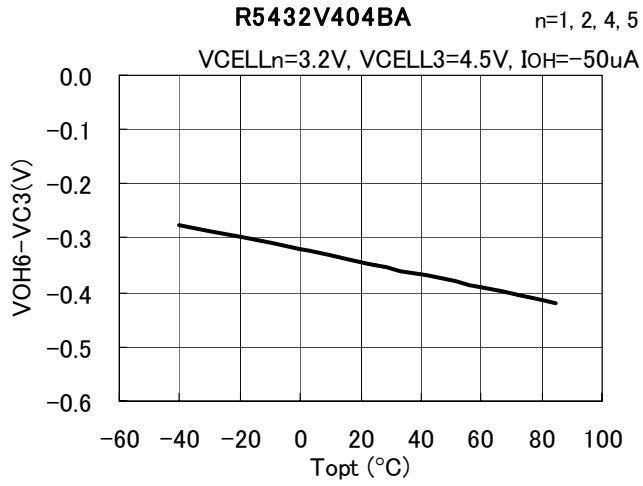
36) CB1 P-channel on voltage



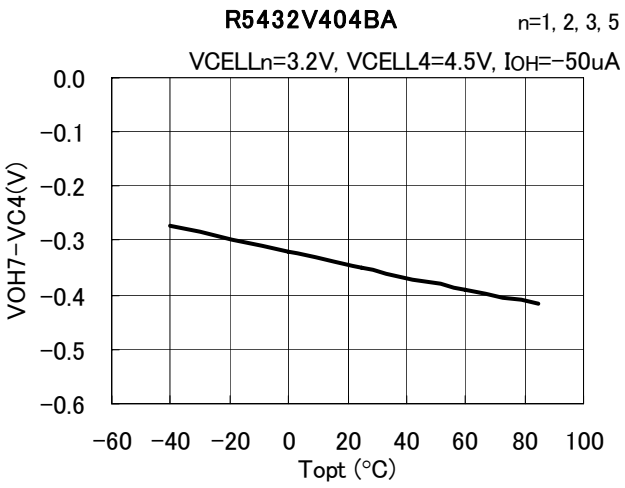
37) CB2 P-channel on voltage



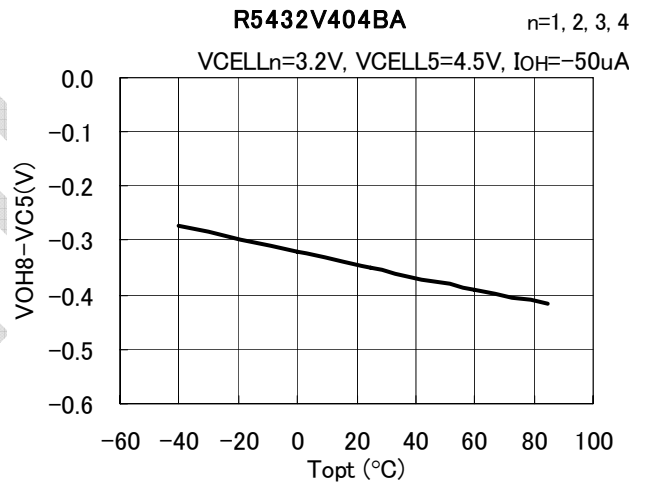
38) CB3 P-channel on voltage



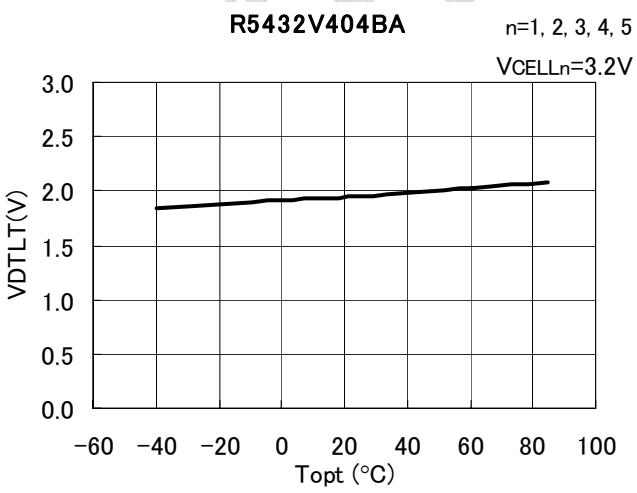
39) CB4 P-channel on voltage



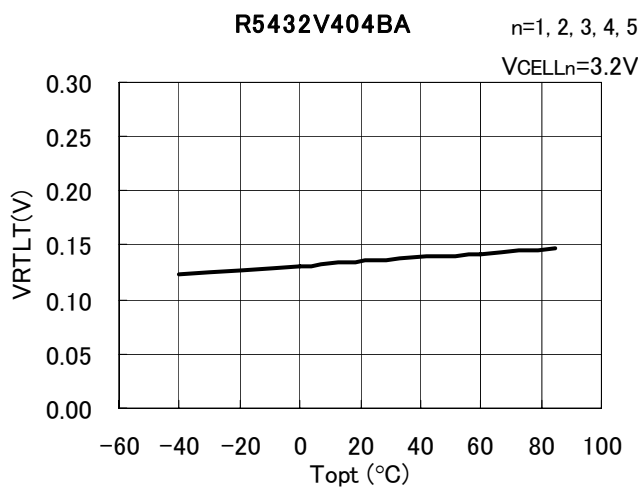
40) CB5 P-channel on voltage



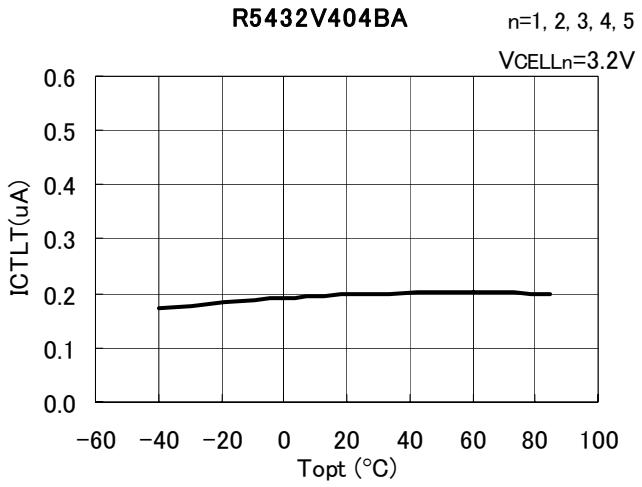
41) CTLT detector threshold



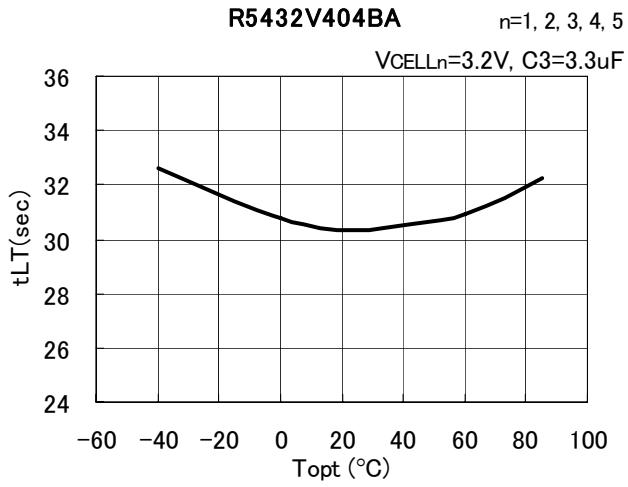
42) CTLT released voltage



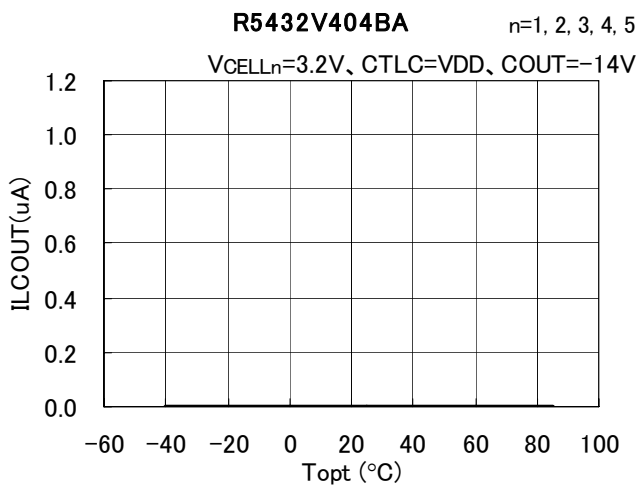
43) CTLT charge current



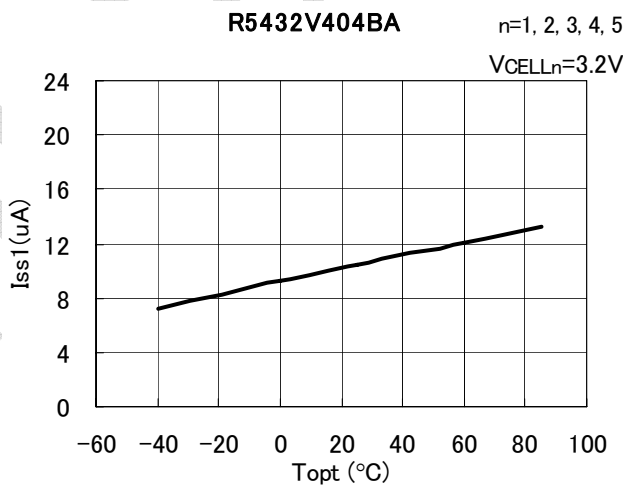
44) Breaking wire test interval time



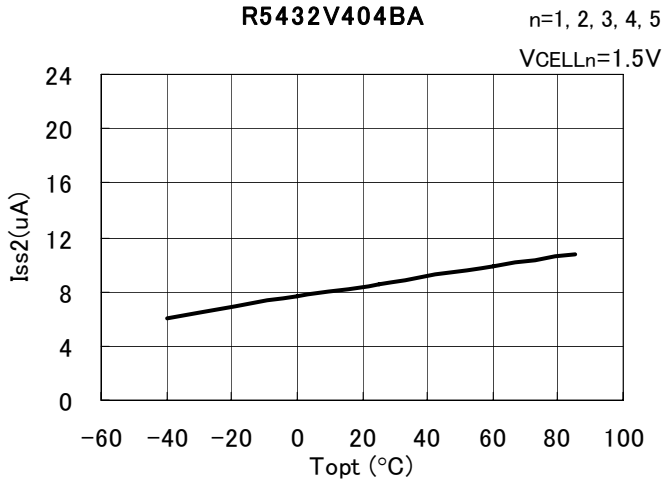
45) C_{OUT} off leakage current



46) Supply Current 1

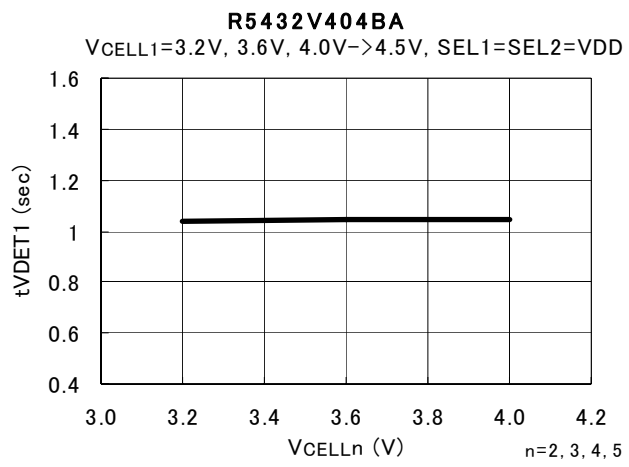


47) Supply current 2

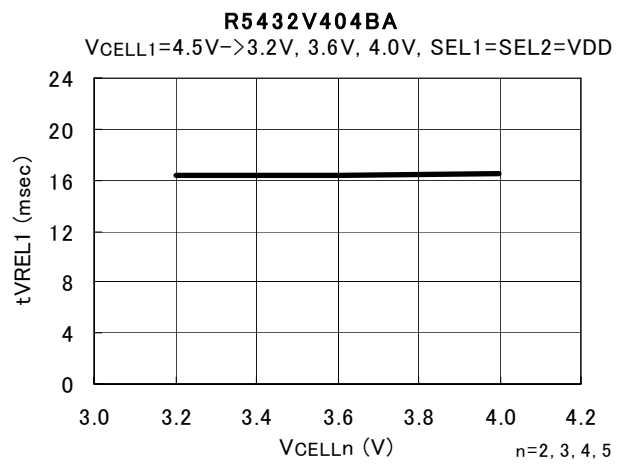


Part 2. Output Delay Time V_{DD} dependence

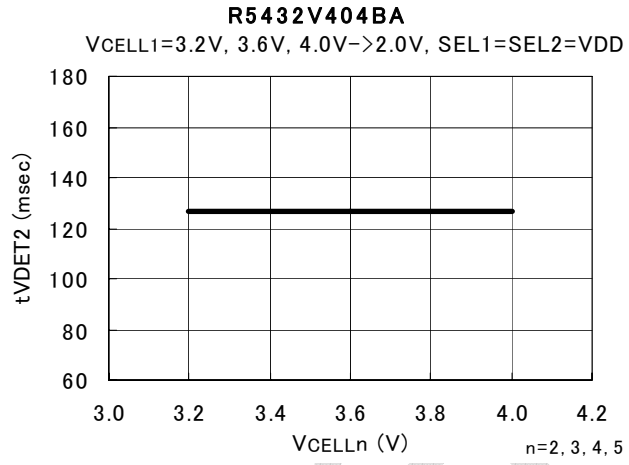
Over-charge detector output delay time



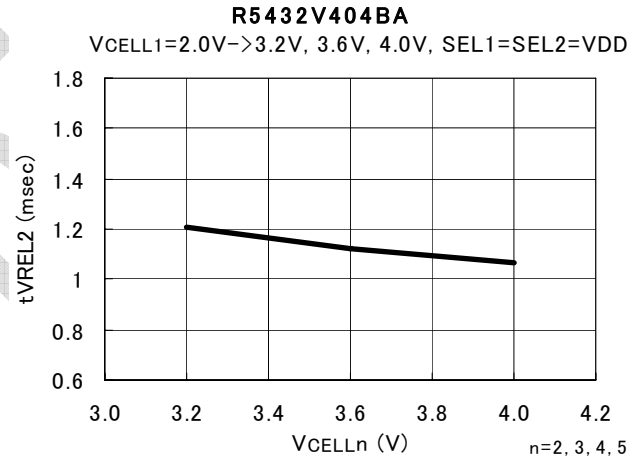
Over-charge released delay time



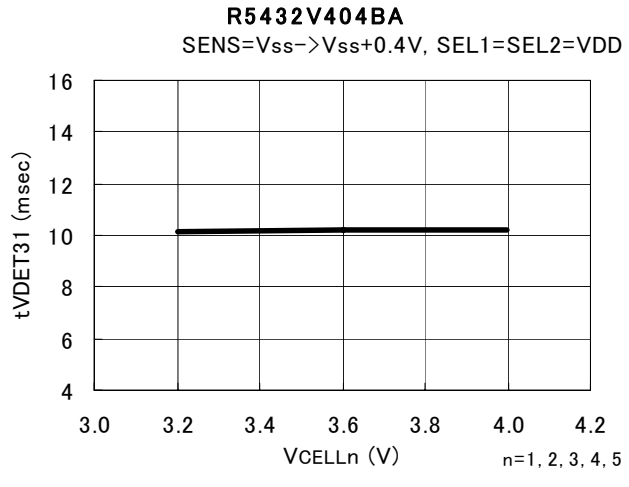
Over-discharge detector output delay time



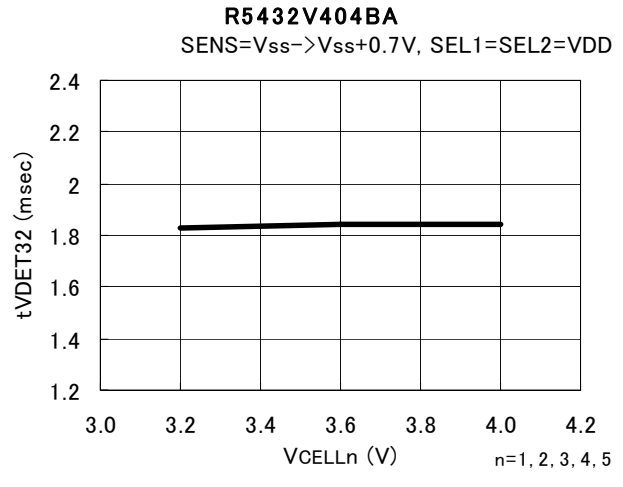
Over-discharge released delay time



Excess discharge current detector output delay time 1



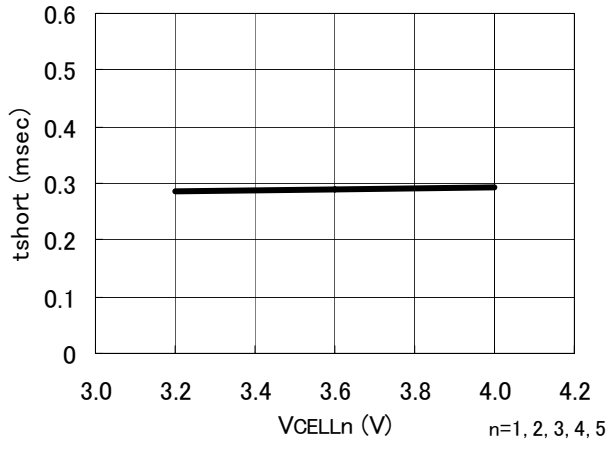
Excess discharge current detector output delay time 2



Short detector output delay time 1

R5432V404BA

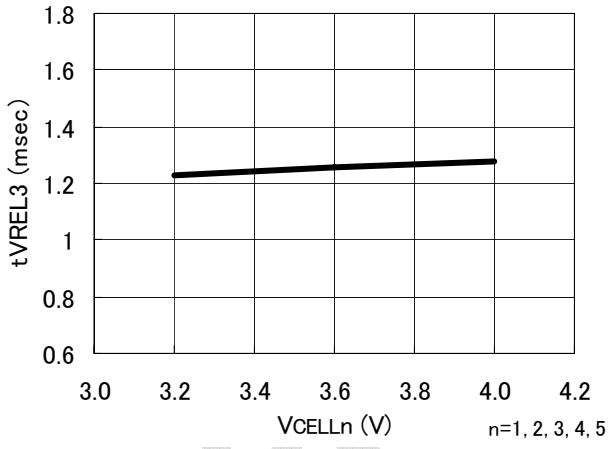
SENS=Vss->Vss+1.5V, SEL1=SEL2=VDD



Excess discharge current released delay time 2

R5432V404BA

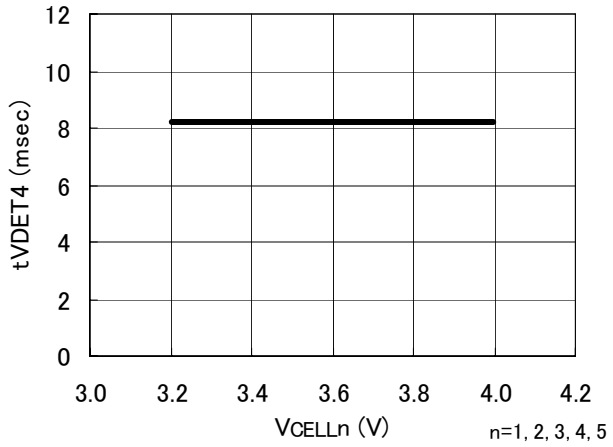
V-=Vss+0.4V->Vss, SEL1=SEL2=VDD



Excess charge current detector output delay time

R5432V404BA

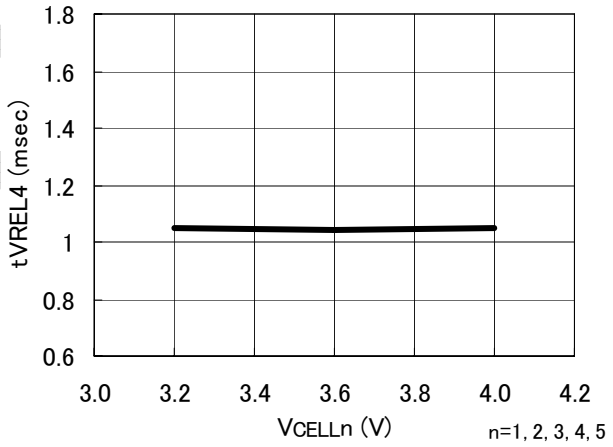
V-=Vss->Vss-0.4V, SEL1=SEL2=VDD



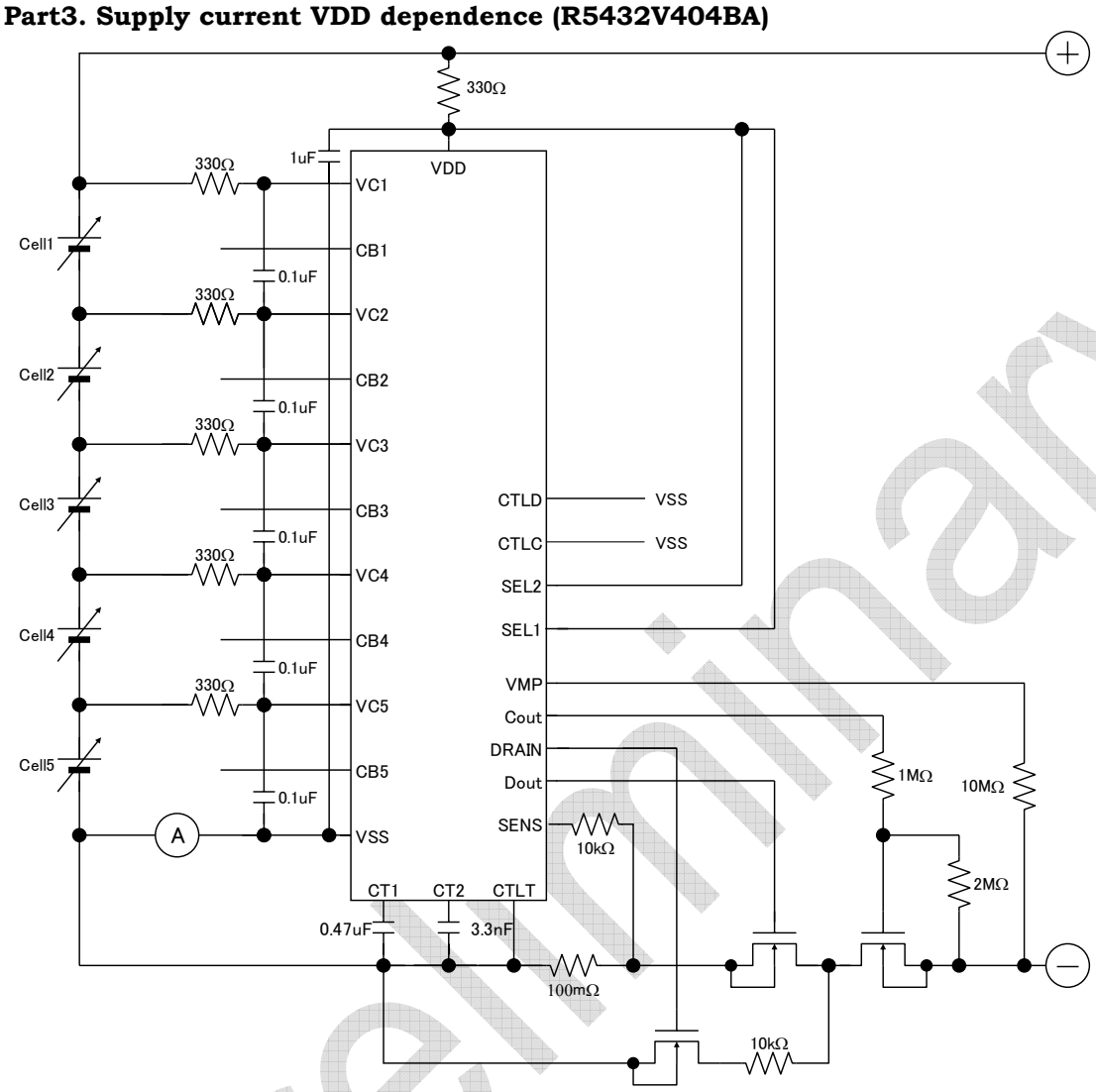
Excess charge current released delay time

R5432V404BA

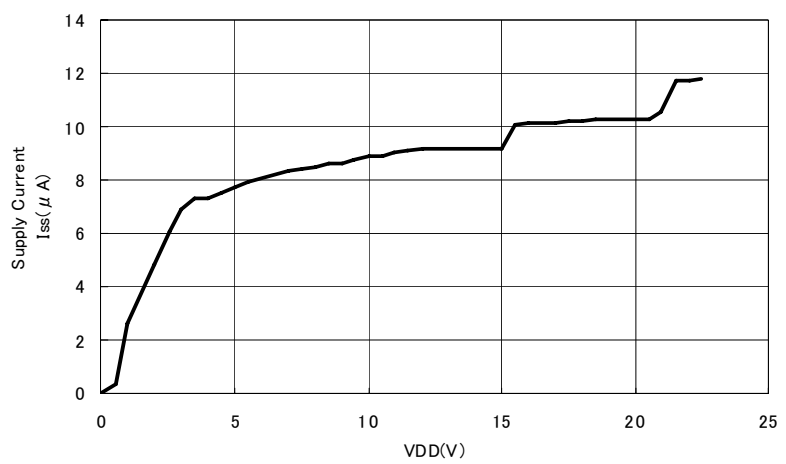
V-=Vss-0.4V->Vss+0.4V, SEL1=SEL2=VDD



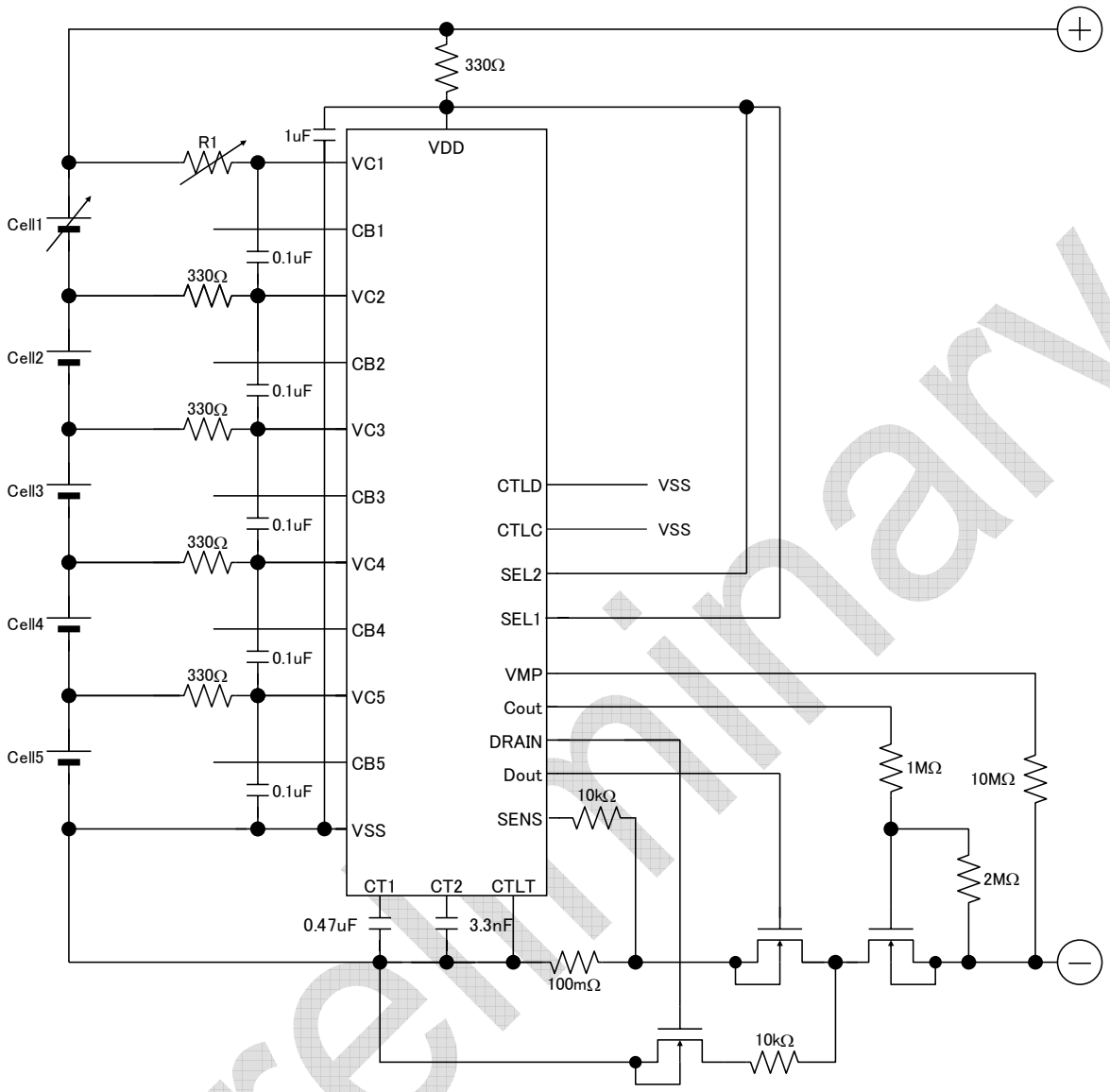
Part3. Supply current VDD dependence (R5432V404BA)



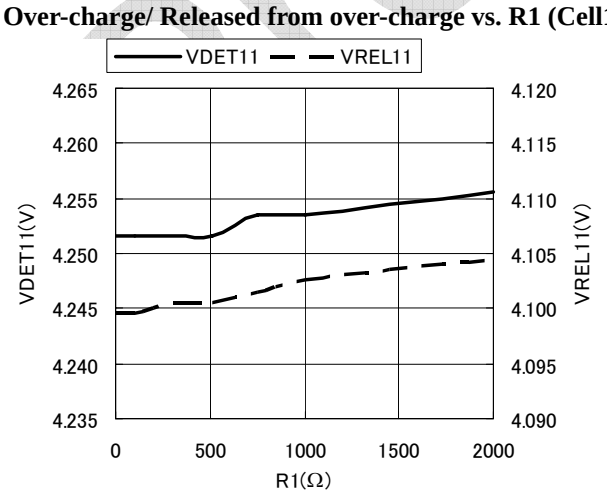
Supply current for 5-cell protection



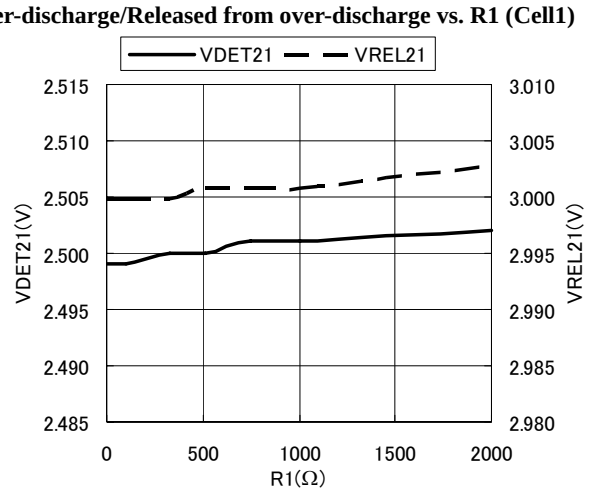
Part4. External resistance dependence (R5432V404BA)



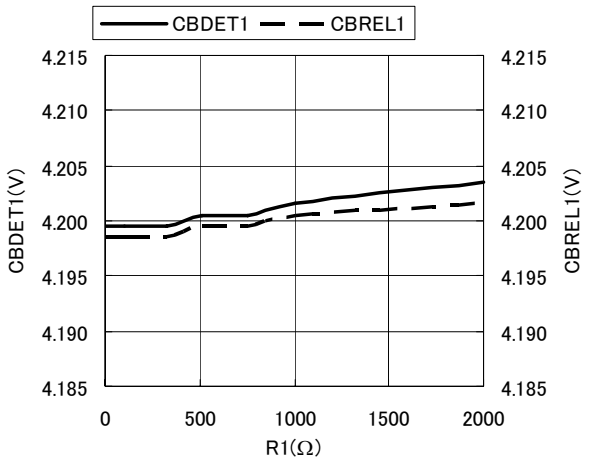
Over-charge/ Released from over-charge vs. R1 (Cell1)



Over-discharge/Released from over-discharge vs. R1 (Cell1)



Cell balance detector/Released voltage of cell balance vs. R1 (Cell1)



PACKAGE DIMENSIONS

♦VSOP-24P (24 pin SSOP (0.65mm pitch)