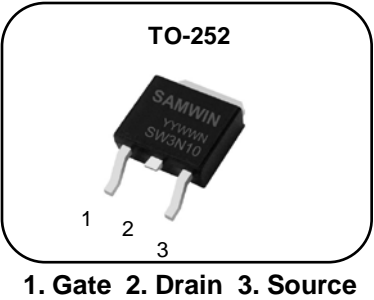


N-channel Enhanced mode TO-252 MOSFET

Features

- High ruggedness
- Low $R_{DS(ON)}$ (Typ 80mΩ) @ $V_{GS}=10V$
- Low Gate Charge (Typ 21nC)
- Improved dv/dt Capability
- 100% Avalanche Tested
- Application:DC-DC



BV_{DSS} : 100V
 I_D : 3A
 $R_{DS(ON)}$: 80mΩ

General Description

This power MOSFET is produced with advanced technology of SAMWIN. This technology enable the power MOSFET to have better characteristics, including fast switching time, low on resistance, low gate charge and especially excellent avalanche characteristics.



Order Codes

Item	Sales Type	Marking	Package	Packaging
1	SW D 3N10	SW3N10	TO-252	REEL

Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to source voltage	100	V
I_D	Continuous drain current (@ $T_C=25^{\circ}C$)	3*	A
	Continuous drain current (@ $T_C=100^{\circ}C$)	1.9*	A
I_{DM}	Drain current pulsed (note 1)	12	A
V_{GS}	Gate to source voltage	± 16	V
E_{AS}	Single pulsed avalanche energy (note 2)	187	mJ
E_{AR}	Repetitive avalanche energy (note 1)	40	mJ
dv/dt	Peak diode recovery dv/dt (note 3)	5	V/ns
P_D	Total power dissipation (@ $T_C=25^{\circ}C$)	44	W
	Derating factor above 25°C	0.35	W/°C
T_{STG}, T_J	Operating junction temperature & storage temperature	-55 ~ + 150	°C
T_L	Maximum lead temperature for soldering purpose, 1/8 from case for 5 seconds.	300	°C

*. Drain current is limited by junction temperature.

Thermal characteristics

Symbol	Parameter	Value	Unit
R_{thjc}	Thermal resistance, Junction to case	2.84	°C/W
R_{thja}	Thermal resistance, Junction to ambient		°C/W

Electrical characteristic ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	$V_{GS}=0V, I_D=250\mu A$	100			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown voltage temperature coefficient	$I_D=250\mu A$, referenced to 25°C		0.11		$V/^\circ\text{C}$
I_{DSS}	Drain to source leakage current	$V_{DS}=100V, V_{GS}=0V$			1	μA
		$V_{DS}=80V, T_C=125^\circ\text{C}$			50	μA
I_{GSS}	Gate to source leakage current, forward	$V_{GS}=16V, V_{DS}=0V$			11	nA
	Gate to source leakage current, reverse	$V_{GS}=-16V, V_{DS}=0V$			-11	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.5		2.5	V
$R_{DS(ON)}$	Drain to source on state resistance	$V_{GS}=10V, I_D=1.5A$		80	100	m Ω
G_{fs}	Forward transconductance	$V_{DS}=20V, I_D=1.5A$		6.2		S
Dynamic characteristics						
C_{iss}	Input capacitance	$V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$		1050		pF
C_{oss}	Output capacitance			65		
C_{rss}	Reverse transfer capacitance			40		
$t_{d(on)}$	Turn on delay time	$V_{DS}=50V, I_D=3A, V_{GS}=10V, R_G=25\Omega$ (note 4,5)		8		ns
t_r	Rising time			20		
$t_{d(off)}$	Turn off delay time			36		
t_f	Fall time			18		
Q_g	Total gate charge	$V_{DS}=80V, V_{GS}=10V, I_D=3A$ (note 4,5)		21		nC
Q_{gs}	Gate-source charge			3		
Q_{gd}	Gate-drain charge			5		

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET			3	A
I_{SM}	Pulsed source current				12	A
V_{SD}	Diode forward voltage drop.	$I_S=3A, V_{GS}=0V$			1.4	V
t_{rr}	Reverse recovery time	$I_S=3A, V_{GS}=0V, di/dt=100A/\mu s$		28		ns
Q_{rr}	Reverse recovery charge			38		nC

※. Notes

1. Repeattive rating : pulse width limited by junction temperature.
2. $L = 41.6\text{mH}, I_{AS} = 3A, V_{DD} = 50V, R_G=25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 3A, di/dt = 100A/\mu s, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. Essentially independent of operating temperature.

Fig. 1. On-state characteristics

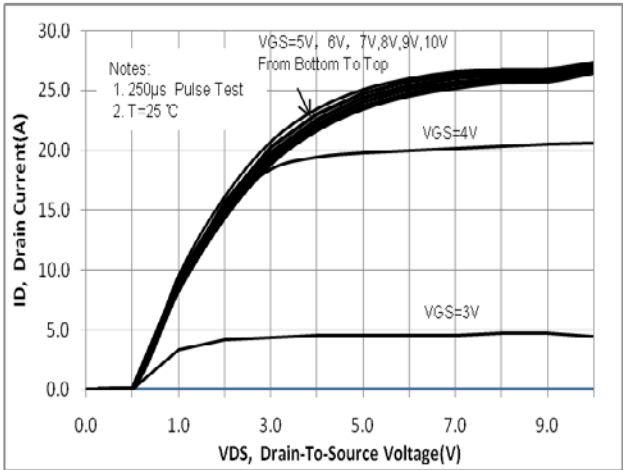


Fig. 2. On-resistance variation vs. drain current and gate voltage

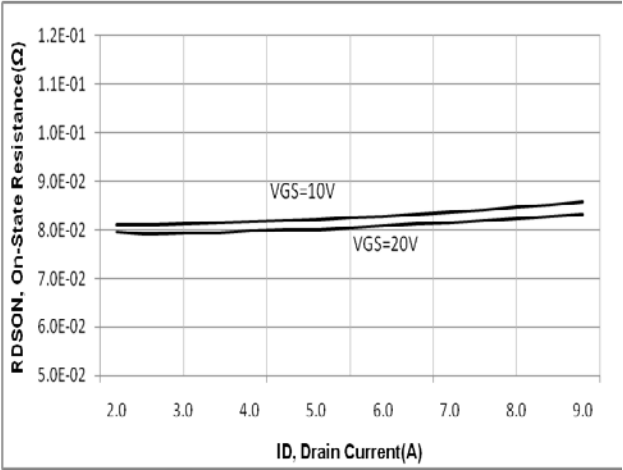


Fig. 3. Gate charge characteristics

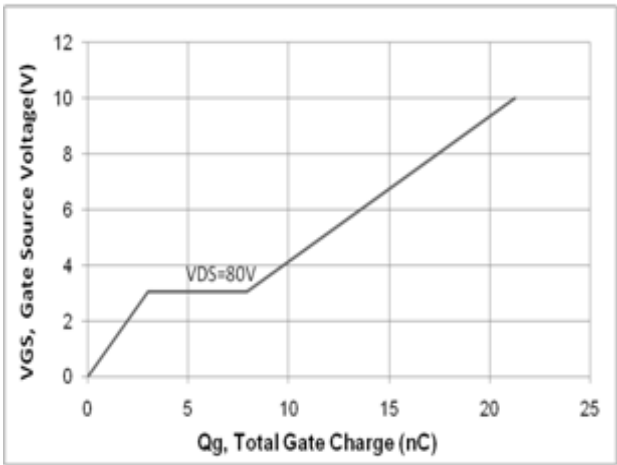


Fig. 4. On state current vs. diode forward voltage

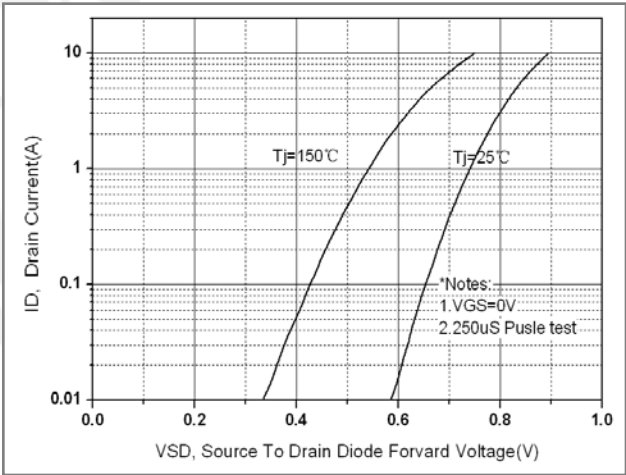


Fig 5. Breakdown Voltage Variation vs. Junction Temperature

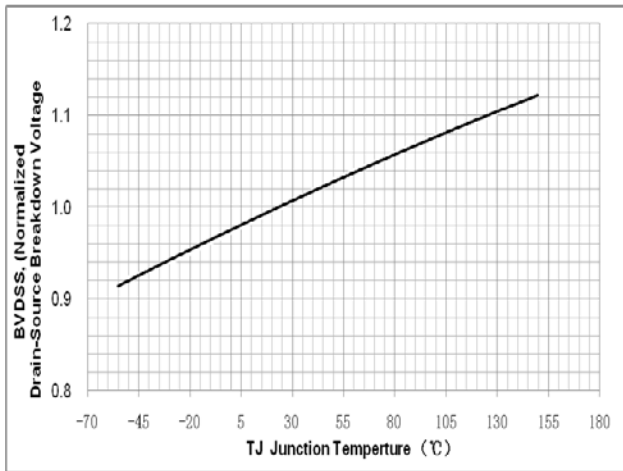


Fig. 6. On resistance variation vs. junction temperature

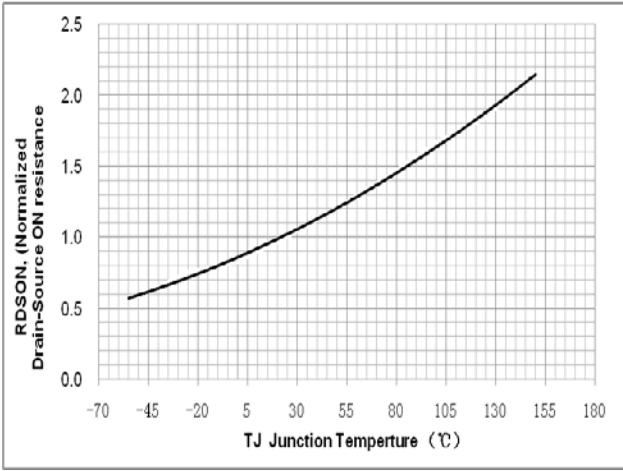


Fig. 7. Maximum safe operating area

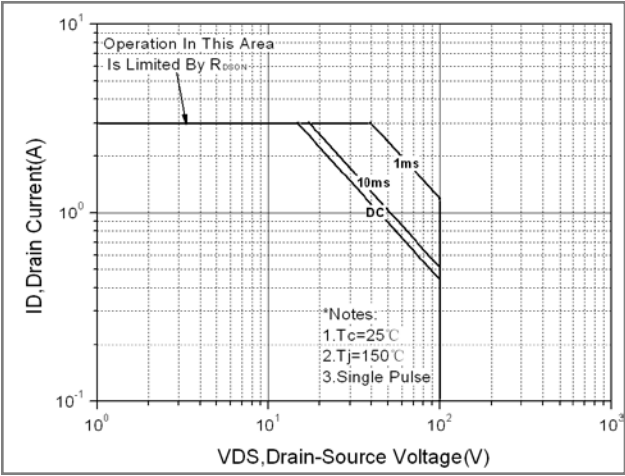


Fig. 8. Transient thermal response curve

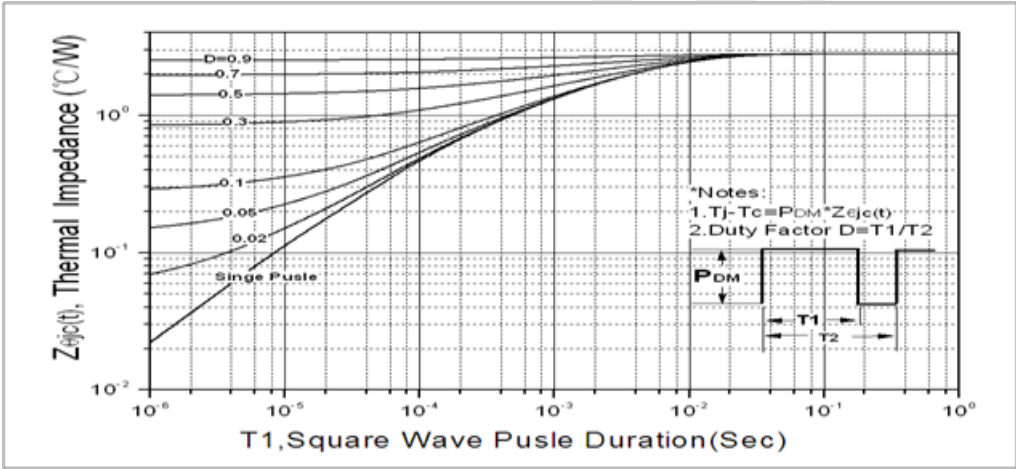


Fig. 9. Gate charge test circuit & waveform

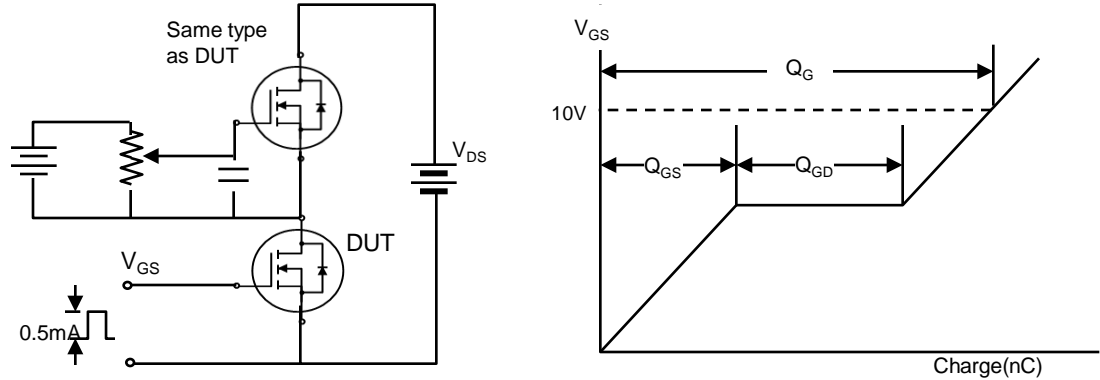


Fig. 10. Switching time test circuit & waveform

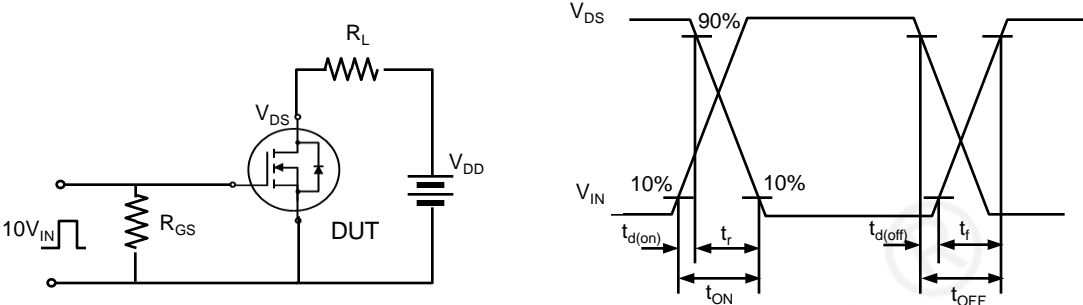


Fig. 11. Unclamped Inductive switching test circuit & waveform

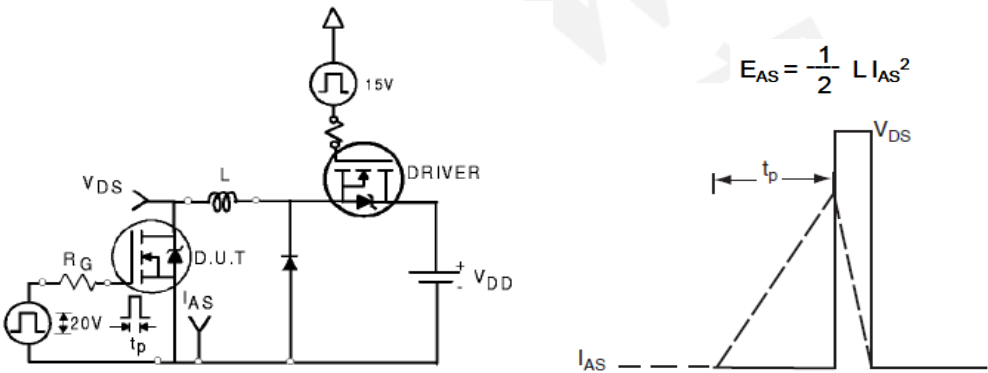
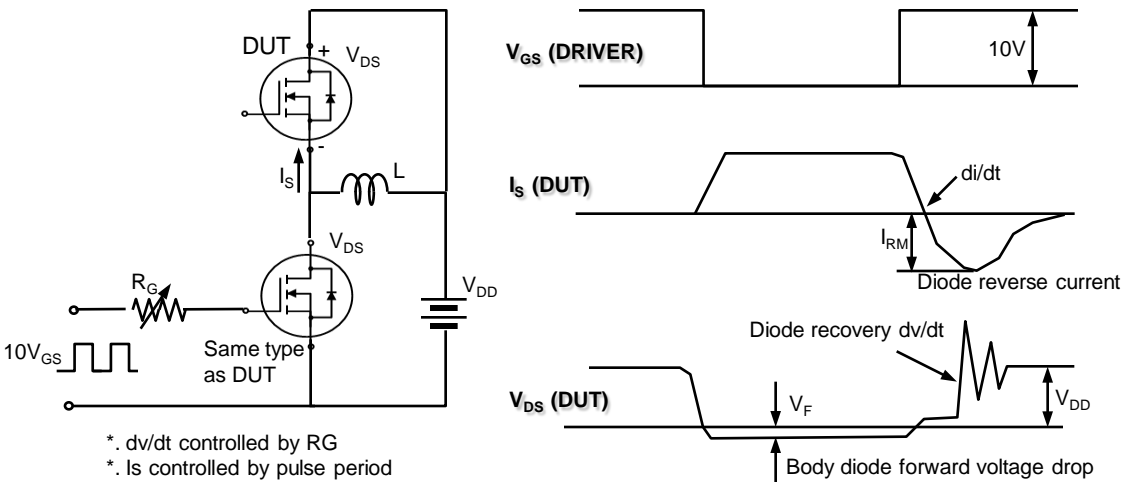


Fig. 12. Peak diode recovery dv/dt test circuit & waveform



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DISCLAIMER

- * All the data & curve in this document was tested in XI'AN SEMIPOWER TESTING & APPLICATION CENTER.
- * This product has passed the PCT,TC,HTRB,HTGB,HAST,PC and Solderdunk reliability testing.
- * Qualification standards can also be found on the Web site (<http://www.semipower.com.cn>) 
- * Suggestions for improvement are appreciated, Please send your suggestions to samwin@samwinsemi.com