



ADM3251E

FUNCTIONAL BLOCK DIAGRAM

20 Lead WSOIC package

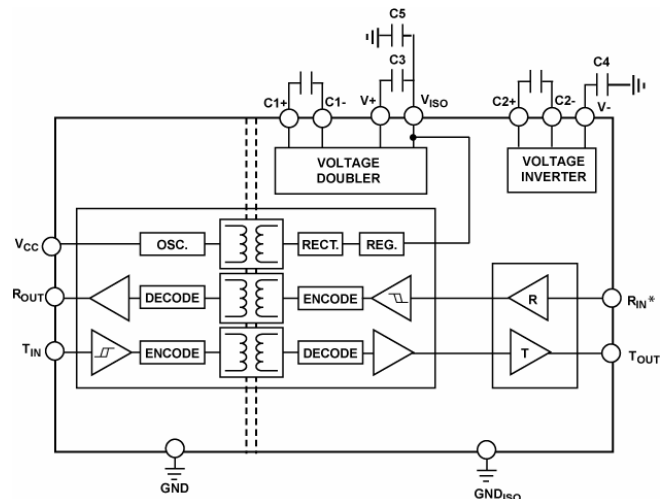


Figure 1.

Industrial/Telecom Diagnostic Ports

The ADM3251E is available in a 20 lead Wide Body SOIC package.

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TARGET SPECIFICATIONS

All voltages are relative to their respective ground. All min/max specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications in Table 1 are at $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC CHARACTERISTICS					
V_{CC} Operating Voltage Range	4.5		5.5	V	
DC-to-DC Converter Enable Threshold, $V_{CC(\text{Enable})}$ ¹	4.5			V	
DC-to-DC Converter Disable Threshold, $V_{CC(\text{Disable})}$ ¹			3.7	V	
DC-to-DC CONVERTER ENABLED					
Input Supply Current			TBD	mA	No Load
			TBD	mA	$R_L = 3\text{k}\Omega$
V_{ISO} Output ²		5.0		V	$I_{ISO} = 0\mu\text{A}$
DC-to-DC CONVERTER DISABLED					
Primary Side Supply Input Current, $I_{CC(\text{Disable})}$			TBD	mA	$V_{ISO} = 3.3\text{V}$, $V_{CC} \leq 3.7\text{V}$
LOGIC					
Transmitter Input, T_{IN}					
Logic Input Current, I_{TIN}	-10	+0.01	+10	μA	
Logic Low Input Threshold, V_{TINL}	$0.3 V_{CC}$			V	
Logic High Input Threshold, V_{TINH}			$0.7 V_{CC}$	V	
Receiver Output, R_{OUT}					
Logic High Output V_{ROUTH}	$V_{CC} - 0.1$	V_{CC}		V	$I_{ROUTH} = -20\mu\text{A}$
	$V_{CC} - 0.5$	$V_{CC} - 0.2$		V	$I_{ROUTH} = -4\text{mA}$
Logic Low Output V_{ROUTL}		0.0	0.1	V	$I_{ROUTH} = 20\mu\text{A}$
		0.0	0.4	V	$I_{ROUTH} = 4\text{mA}$
RS-232					
RECEIVER					
EIA-232 Input Voltage Range ³	-30		+30	V	
EIA-232 Input Threshold Low	0.6	1.3		V	
EIA-232 Input Threshold High		1.6	2.4	V	
EIA-232 Input Hysteresis		0.4		V	
EIA-232 Input Resistance	3	5	7	$\text{k}\Omega$	
TRANSMITTER					
Output Voltage Swing (RS-232)	± 5	± 5.7		V	$R_L = 3\text{k}\Omega$ to Gnd
Transmitter Output Resistance	300			Ω	$V_{ISO} = 0\text{V}$
RS-232 Output Short Circuit Current		TBD		mA	
TIMING CHARACTERISTICS					
Maximum Data Rate	460			kbps	$R_L = 3\text{k}\Omega$ to $7\text{k}\Omega$, $C_L = 50\text{pF}$ to 1000pF
Receiver Propagation Delay					
t_{PHL}		190		μs	
t_{PLH}		135		μs	
Transmitter Propagation Delay		650		μs	$R_L = 3\text{k}\Omega$, $C_L = 1000\text{pF}$
Transmitter Skew		80		ns	
Receiver Skew		70		ns	
Transition Region Slew Rate ³	5.5	10	30	V/ μs	+3V to -3V or -3V to 0.3V, $V_{CC} = +3.3\text{V}$, $R_L = +3\text{k}\Omega$, $C_L = 1000\text{pF}$, $T_A = 25^\circ\text{C}$.
AC SPECIFICATIONS					
Output Rise, t_R /Fall time, t_F (10% to 90%)		2.3		ns	$C_L = 15\text{pF}$, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output		TBD		KV/ μs	
Common-Mode Transient Immunity at Logic Low Output		TBD		KV/ μs	
ESD PROTECTION (R_{IN} and T_{OUT} Pins)					
		± 15		kV	Human Body Model Air Discharge
		± 8		kV	Human Body Model Contact Discharge

¹ Enable/disable threshold is the V_{CC} voltage at which the internal DC-to-DC converter is enabled/disabled.

² To maintain datasheet specifications no current should be drawn from V_{ISO} .

³ Guaranteed by design

TARGET SPECIFICATIONS

All voltages are relative to their respective ground. All min/max specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications in Table 2 are at $T_A = 25^\circ\text{C}$, $V_{CC} = 3.3\text{V}$ (DC-to-DC converter disabled), the secondary side is powered externally by $V_{ISO}=3.3\text{V}$, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments	
DC CHARACTERISTICS						
V_{CC} Operating Voltage Range	3.0		3.7	V	No Load $R_L=3\text{k}\Omega$	
DC-to-DC Converter Disable Threshold, $V_{CC(Disable)}^1$			3.7	V		
DC-to-DC CONVERTER DISABLED						
V_{ISO}	3.0		5.5	V		
Primary Side Supply Input Current, $I_{CC(Disable)}$			TBD	mA		
Secondary Side Supply Input Current, $I_{SO(Disable)}$			TBD	mA		
LOGIC						
Transmitter Input, T_{IN}					$I_{ROUTH} = -20\text{ }\mu\text{A}$ $I_{ROUTH} = -4\text{ mA}$ $I_{ROUTH} = 20\text{ }\mu\text{A}$ $I_{ROUTH} = 4\text{ mA}$	
Logic Input Current, I_{TIN}	-10	+0.01	+10	μA		
Logic Low Input Threshold, V_{TINL}	0.3 V_{CC}			V		
Logic High Input Threshold, V_{TINH}			0.7 V_{CC}	V		
Receiver Output, R_{OUT}						
Logic High Output V_{ROUTH}	$V_{CC} - 0.1$	V_{CC}		V		
	$V_{CC} - 0.5$	$V_{CC} - 0.2$		V		
Logic Low Output V_{ROUTL}		0.0	0.1	V		
		0.0	0.4	V		
RS-232						
RECEIVER						
EIA-232 Input Voltage Range ²	-30		+30	V	$V_{ISO} = 3.3\text{V}$, $R_L = 3\text{k}\Omega$ to Gnd $V_{ISO} = 0\text{V}$	
EIA-232 Input Threshold Low	0.6	1.3		V		
EIA-232 Input Threshold High		1.6	2.4	V		
EIA-232 Input Hysteresis		0.4		V		
EIA-232 Input Resistance	3	5	7	$\text{k}\Omega$		
TRANSMITTER						
Output Voltage Swing (RS-232)	± 5	± 5.7		V		
Transmitter Output Resistance	300			Ω		
RS-232 Output Short Circuit Current		TBD		mA		
TIMING CHARACTERISTICS						
Maximum Data Rate	460			kbps	$V_{ISO} = 3.3\text{V}$, $R_L = 3\text{k}\Omega$ to $7\text{k}\Omega$, $C_L=50\text{ pF}$ to 1000pF	
Receiver Propagation Delay					$R_L = 3\text{k}\Omega$, $C_L=1000\text{ pF}$ $+3\text{V}$ to -3V , or -3V to $+3\text{V}$, $V_{CC} = 3.3\text{V}$, $R_L=3\text{k}\Omega$, $C_L=1000\text{pF}$, $T_A=25^\circ\text{C}$.	
t_{PHL}		190		μs		
t_{PLH}		135		μs		
Transmitter Propagation Delay		650		μs		
Transmitter Skew		80		ns		
Receiver Skew		55		ns		
Transition Region Slew Rate ²	5.5	10	30	V/ μs		
AC SPECIFICATIONS						
Output Rise, t_r /Fall time, t_f (10% to 90%)		2.3		ns	$C_L = 15\text{ pF}$, CMOS signal levels	
Common-Mode Transient Immunity at Logic High Output		TBD		KV/ μs		
Common-Mode Transient Immunity at Logic Low Output		TBD		KV/ μs		
ESD PROTECTION (R_{IN} and T_{OUT} Pins)						
		± 15		kV	Human Body Model Air Discharge	
		± 8		kV	Human Body Model Contact Discharge	

1 Enable/disable threshold is the V_{CC} voltage at which the internal DC-to-DC converter is enabled/disabled.

2 Guaranteed by design

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ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
V_{CC}	–0.3 V to +6 V
$V+$	$(V_{CC} - 0.3 \text{ V})$ to +13 V
$V-$	+0.3 V to –13 V
Input Voltages	
T_{IN}	–0.3 V to $(V+, +0.3 \text{ V})$
R_{IN}	$\pm 30 \text{ V}$
Output Voltages	
T_{OUT}	$\pm 15 \text{ V}$
R_{OUT}	–0.3 V to $(V_{CC} + 0.3 \text{ V})$
Short Circuit Duration	
T_{OUT}	Continuous
Power Dissipation	
Power dissipation CP-12	TBD
θ_{JA} , Thermal Impedance	TBD
Operating Temperature Range	
Industrial	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Pb-Free Temperature (Soldering, 30 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

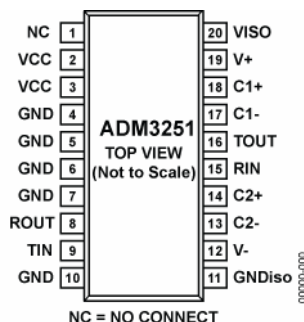
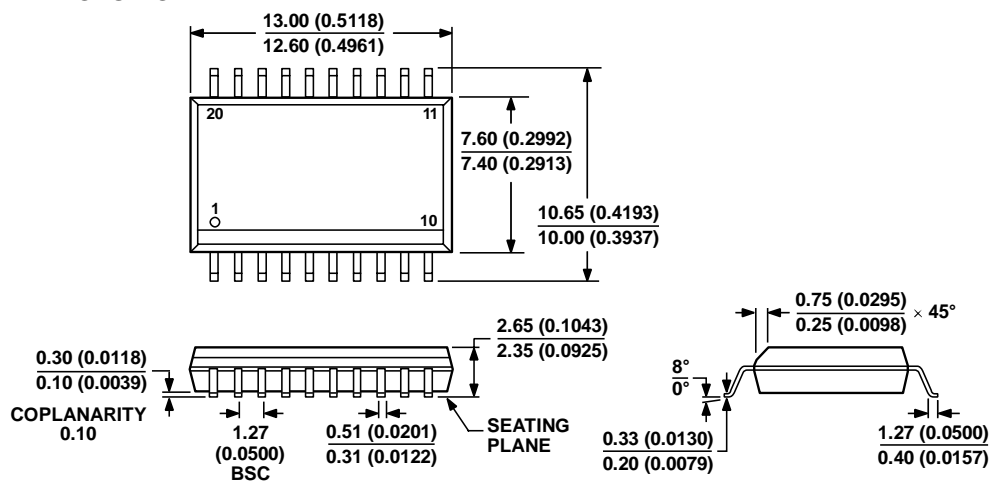


Figure 2. ADM3251E Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	Not Connected
2	V _{CC}	Power Supply Input
3	V _{CC}	Power Supply Input
4	GND	Ground Pin
5	GND	Ground Pin
6	GND	Ground Pin
7	GND	Ground Pin
8	R _{OUT}	Receiver Output. This outputs CMOS output logic levels.
9	T _{IN}	Transmitter (Driver) Input. This input accepts TTL/CMOS levels.
10	GND	Ground Pin
11	GND _{ISO}	Ground reference for Isolator Primary Side.
12	V ₋	Internally Generated Negative Supply
13	C2 ₋	External Capacitor 2 is connected between pins 13 and 14. A 0.1μF capacitor is recommended but larger capacitors up to 47μF may be used.
14	C2 ₊	External Capacitor 2 is connected between pins 13 and 14. A 0.1μF capacitor is recommended but larger capacitors up to 47μF may be used.
15	R _{IN}	Receiver Input. This input accepts RS-232 signal levels.
16	T _{OUT}	Transmitter (Driver) Output. This outputs RS-232 signal levels.
17	C1 ₋	External Capacitor 1 is connected between pins 17 and 18. A 0.1μF capacitor is recommended but larger capacitors up to 47μF may be used.
18	C1 ₊	External Capacitor 1 is connected between pins 17 and 18. A 0.1μF capacitor is recommended but larger capacitors up to 47μF may be used.
19	V ₊	Internally Generated Positive Supply
20	V _{ISO}	Isolated Supply Voltage for Isolator Secondary Side.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AC
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060706-A

Figure 5. 20-Lead Standard Small Outline Package. Dimensions shown in millimeters and (inches).