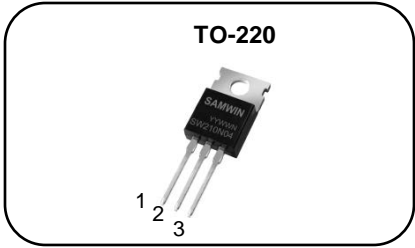


N-channel Enhanced mode TO-220 MOSFET

Features

- High ruggedness
- Low  $R_{DS(ON)}$  (Typ 3.7mΩ) @  $V_{GS}=10V$
- Low Gate Charge (Typ 256nC)
- Improved dv/dt Capability
- 100% Avalanche Tested
- Application:DC-DC Converter, Motor Control, Synchronous Rectification



1. Gate 2. Drain 3. Source

**$BV_{DSS}$  : 40V**  
 **$I_D$  : 210A**  
 **$R_{DS(ON)}$  : 3.7mΩ**

A schematic symbol for an N-channel MOSFET. It shows a circle with a horizontal line on the left (gate), a vertical line on the right (drain), and a diagonal line at the bottom (source). The gate is connected to the drain and source. The pins are labeled 1, 2, and 3.

General Description

This power MOSFET is produced with advanced technology of SAMWIN. This technology enable the power MOSFET to have better characteristics, including fast switching time, low on resistance, low gate charge and especially excellent avalanche characteristics.



Order Codes

| Item | Sales Type  | Marking  | Package | Packaging |
|------|-------------|----------|---------|-----------|
| 1    | SW P 210N04 | SW210N04 | TO-220  | TUBE      |

Absolute maximum ratings

| Symbol         | Parameter  | Value       | Unit |
|----------------|--|-------------|------|
| $V_{DSS}$      | Drain to source voltage  | 40          | V    |
| $I_D$          | Continuous drain current (@ $T_C=25^{\circ}C$ )                              | 210*        | A    |
|                | Continuous drain current (@ $T_C=100^{\circ}C$ )                             | 132.3*      | A    |
| $I_{DM}$       | Drain current pulsed (note 1)  | 840         | A    |
| $V_{GS}$       | Gate to source voltage   | $\pm 20$    | V    |
| $E_{AS}$       | Single pulsed avalanche energy (note 2)                                      | 750         | mJ   |
| $E_{AR}$       | Repetitive avalanche energy (note 1)   | 258         | mJ   |
| dv/dt          | Peak diode recovery dv/dt (note 3)   | 5           | V/ns |
| $P_D$          | Total power dissipation (@ $T_C=25^{\circ}C$ )                               | 388.5       | W    |
|                | Derating factor above 25°C   | 3.1         | W/°C |
| $T_{STG}, T_J$ | Operating junction temperature & storage temperature                         | -55 ~ + 150 | °C   |
| $T_L$          | Maximum lead temperature for soldering purpose, 1/8 from case for 5 seconds. | 300         | °C   |

\*. Drain current is limited by junction temperature.

Thermal characteristics

| Symbol     | Parameter                               | Value | Unit |
|------------|---|-------|------|
| $R_{thjc}$ | Thermal resistance, Junction to case    | 0.3   | °C/W |
| $R_{thja}$ | Thermal resistance, Junction to ambient | 50    | °C/W |

Electrical characteristic (  $T_C = 25^\circ\text{C}$  unless otherwise specified )

| Symbol                         | Parameter                                 | Test conditions   | Min. | Typ.  | Max. | Unit               |
|--------------------------------|---|---|------|-------|------|--------------------|
| <b>Off characteristics</b>     |   |   |      |       |      |                    |
| $BV_{DSS}$                     | Drain to source breakdown voltage         | $V_{GS}=0V, I_D=250\mu A$                                     | 40   |       |      | V                  |
| $\Delta BV_{DSS} / \Delta T_J$ | Breakdown voltage temperature coefficient | $I_D=250\mu A$ , referenced to $25^\circ\text{C}$             |      | 0.06  |      | $V/^\circ\text{C}$ |
| $I_{DSS}$                      | Drain to source leakage current           | $V_{DS}=40V, V_{GS}=0V$                                       |      |       | 1    | $\mu A$            |
|                                |   | $V_{DS}=32V, T_C=125^\circ\text{C}$                           |      |       | 50   | $\mu A$            |
| $I_{GSS}$                      | Gate to source leakage current, forward   | $V_{GS}=20V, V_{DS}=0V$                                       |      |       | 100  | nA                 |
|                                | Gate to source leakage current, reverse   | $V_{GS}=-20V, V_{DS}=0V$                                      |      |       | -100 | nA                 |
| <b>On characteristics</b>      |   |   |      |       |      |                    |
| $V_{GS(TH)}$                   | Gate threshold voltage                    | $V_{DS}=V_{GS}, I_D=250\mu A$                                 | 2    |       | 4    | V                  |
| $R_{DS(ON)}$                   | Drain to source on state resistance       | $V_{GS}=10V, I_D=100A$  |      | 3.7   | 4.5  | m $\Omega$         |
| $G_{fs}$                       | Forward transconductance                  | $V_{DS}=8V, I_D=30A$  |      | 82    |      | S                  |
| <b>Dynamic characteristics</b> |   |   |      |       |      |                    |
| $C_{iss}$                      | Input capacitance                         | $V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$                        |      | 11450 |      | pF                 |
| $C_{oss}$                      | Output capacitance                        |   |      | 895   |      |                    |
| $C_{rss}$                      | Reverse transfer capacitance              |   |      | 1462  |      |                    |
| $t_{d(on)}$                    | Turn on delay time                        | $V_{DS}=20V, I_D=25A, V_{GS}=10V, R_G=25\Omega$<br>(note 4,5) |      | 105   |      | ns                 |
| $t_r$                          | Rising time                               |   |      | 246   |      |                    |
| $t_{d(off)}$                   | Turn off delay time                       |   |      | 538   |      |                    |
| $t_f$                          | Fall time                                 |   |      | 294   |      |                    |
| $Q_g$                          | Total gate charge                         | $V_{DS}=35V, V_{GS}=10V, I_D=25A$<br>(note 4,5)               |      | 256   |      | nC                 |
| $Q_{gs}$                       | Gate-source charge                        |   |      | 38    |      |                    |
| $Q_{gd}$                       | Gate-drain charge                         |   |      | 93    |      |                    |

### Source to drain diode ratings characteristics

| Symbol   | Parameter                   | Test conditions                                   | Min. | Typ. | Max. | Unit |
|----------|-----------------------------|---|------|------|------|------|
| $I_S$    | Continuous source current   | Integral reverse p-n Junction diode in the MOSFET |      |      | 210  | A    |
| $I_{SM}$ | Pulsed source current       |   |      |      | 840  | A    |
| $V_{SD}$ | Diode forward voltage drop. | $I_S=100A, V_{GS}=0V$                             |      |      | 1.4  | V    |
| $t_{rr}$ | Reverse recovery time       | $I_S=25A, V_{GS}=0V, di/dt=100A/\mu s$            |      | 49   |      | ns   |
| $Q_{rr}$ | Reverse recovery charge     |   |      | 82   |      | nC   |

※. Notes

1. Repeattive rating : pulse width limited by junction temperature.
2.  $L = 1.7\text{mH}, I_{AS} = 30A, V_{DD} = 30V, R_G=25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 25A, di/dt = 100A/\mu s, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse Width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature.

Fig. 1. On-state characteristics

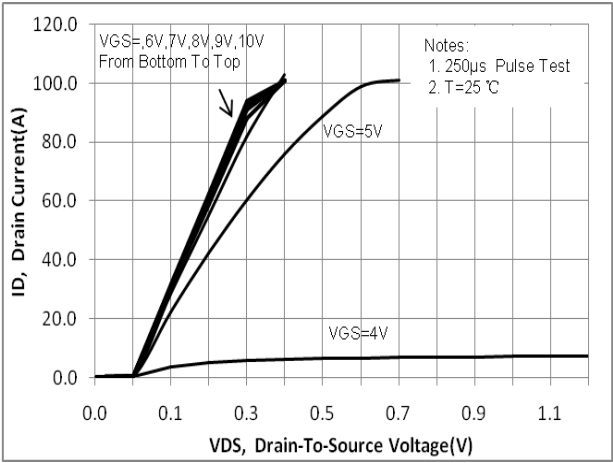


Fig. 2. On-resistance variation vs. drain current and gate voltage

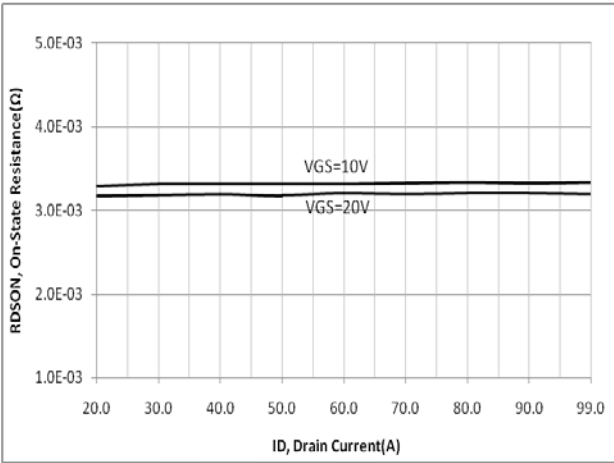


Fig. 3. Gate charge characteristics

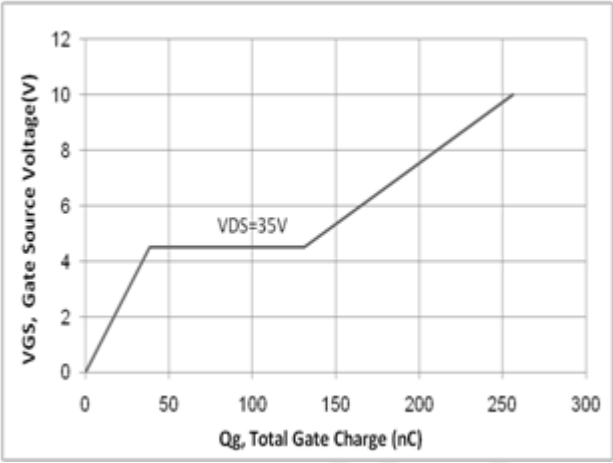


Fig. 4. On state current vs. diode forward voltage

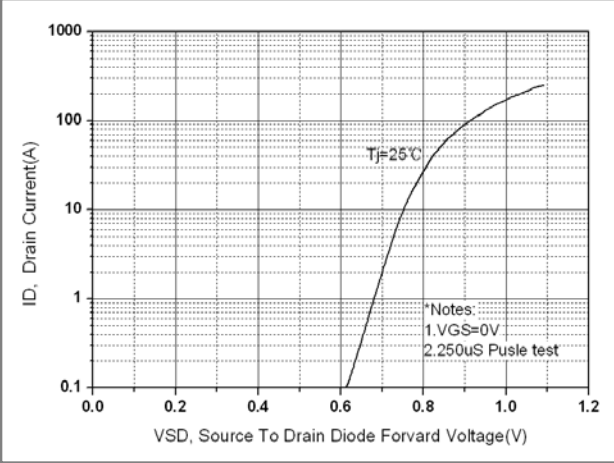


Fig 5. Breakdown Voltage Variation vs. Junction Temperature

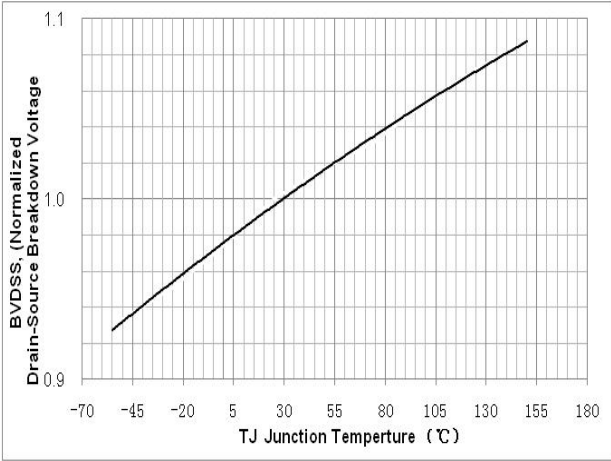


Fig. 6. On resistance variation vs. junction temperature

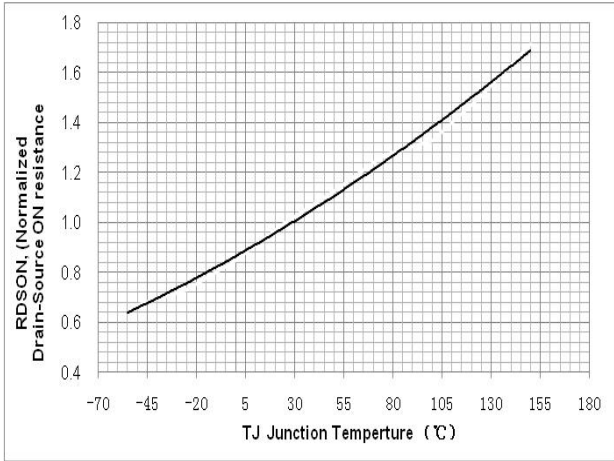


Fig. 7. Maximum safe operating area

Fig. 8. Capacitance Characteristics

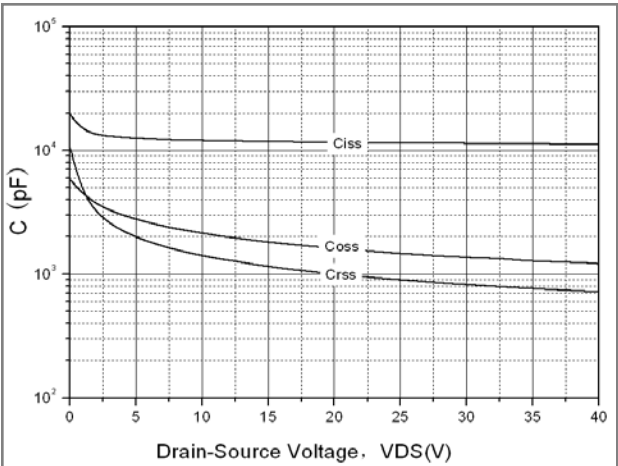
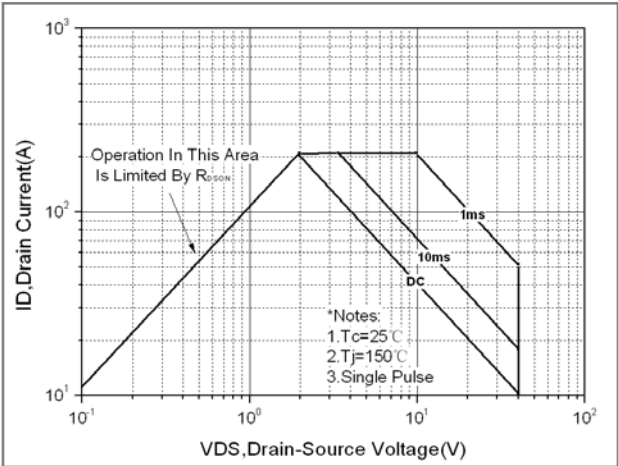


Fig. 9. Transient thermal response curve

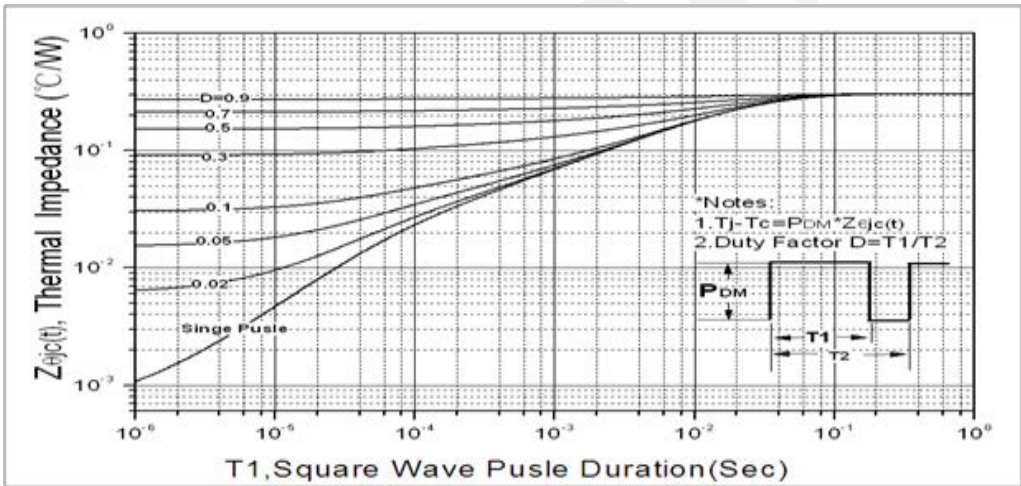


Fig. 10. Gate charge test circuit & waveform

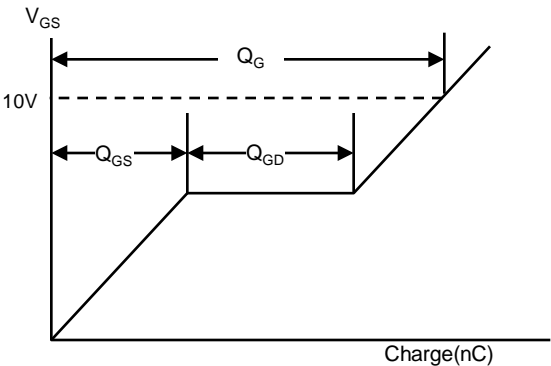
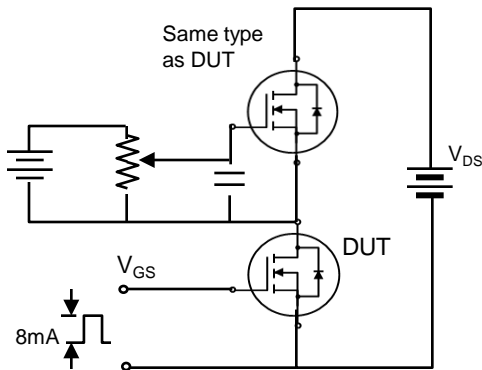


Fig. 11. Switching time test circuit & waveform



Fig. 12. Unclamped Inductive switching test circuit & waveform

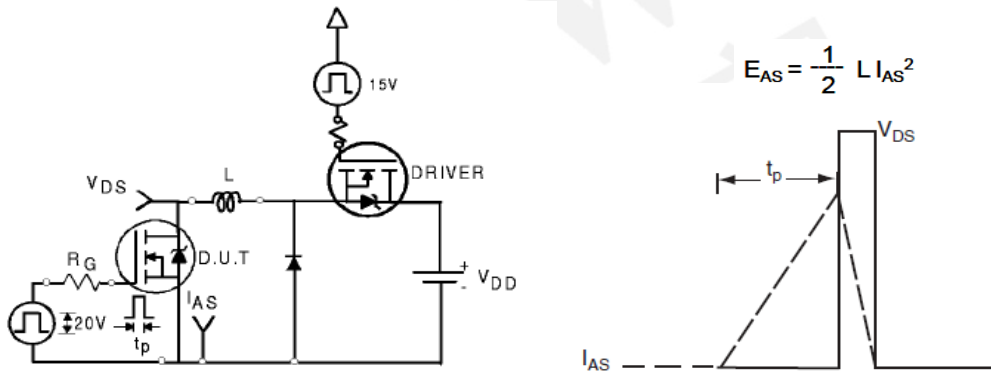
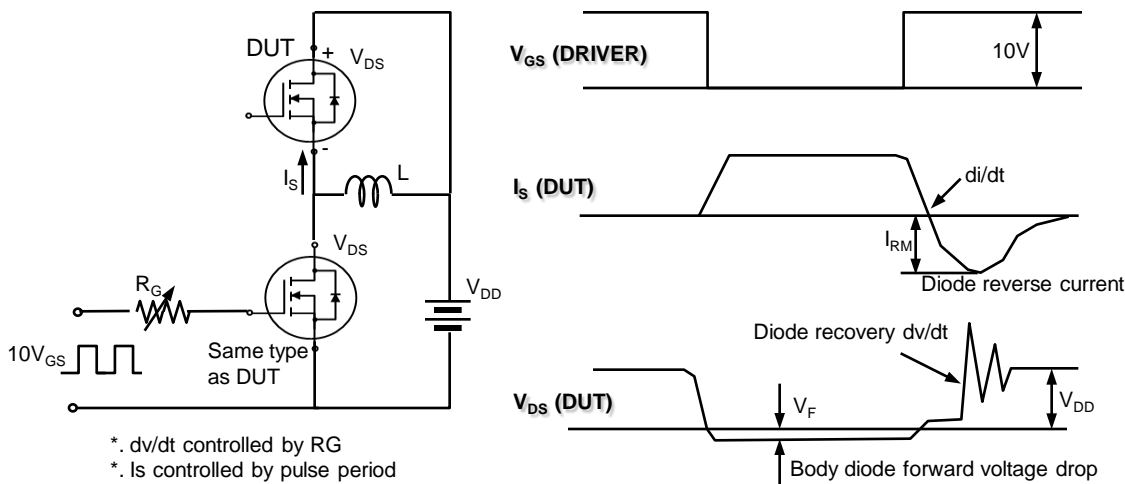



Fig. 13. Peak diode recovery dv/dt test circuit & waveform



Samwin®  
内部保密

### DISCLAIMER

- \* All the data & curve in this document was tested in XI'AN SEMIPOWER TESTING & APPLICATION CENTER.
- \* This product has passed the PCT,TC,HTRB,HTGB,HAST,PC and Solderdunk reliability testing.
- \* Qualification standards can also be found on the Web site (<http://www.semipower.com.cn>) 
- \* Suggestions for improvement are appreciated, Please send your suggestions to [samwin@samwinsemi.com](mailto:samwin@samwinsemi.com)