# STM32F372xx
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## ARM Cortex-M4F 32b MCU+FPU, up to 256KB Flash+32KB SRAM timers, 4 ADCs (12/16-bit), 3 DACs, 2 comp., 2.0-3.6 V operation

**Datasheet − production data**

## Features

- Core: ARM 32-bit Cortex™-M4F CPU (72 MHz max), single-cycle multiplication and HW division, DSP instruction with FPU (floating-point unit) and MPU (memory protection unit)
- Memories
  - 64 to 256 Kbytes of Flash memory
  - 32 Kbytes of SRAM with HW parity check
- CRC calculation unit
- Reset and power management
  - Voltage range: 2.0 to 3.6 V
  - Power-on/Power down reset (POR/PDR)
  - Programmable voltage detector (PVD)
  - Low power modes: Sleep, Stop, Standby
  - $V_{BAT}$ supply for RTC and backup registers
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x16 PLL option
  - Internal 40 kHz oscillator
- Up to 84 fast I/Os
  - All mappable on external interrupt vectors
  - Up to 45 I/Os with 5 V tolerant capability
- 12-channel DMA controller
- One 12-bit, 1.0 µs ADC (up to 16 channels)
  - Conversion range: 0 to 3.6 V
  - Separate analog supply from 2.4 up to 3.6
- Up to three 16-bit Sigma Delta ADC
  - Separate analog supply from 2.2 to 3.6 V, up to 21 single/ 11 diff channels
- Up to three 12-bit DAC channels
- Two fast rail-to-rail analog comparators with programmable input and output
- Up to 24 capacitive sensing channels supporting touchkey, linear and rotary touchsensors

LQFP48 (7 × 7 mm)
LQFP64 (10 × 10 mm)
LQFP100 (14 × 14 mm)

UFBGA100 (7 x 7 mm)
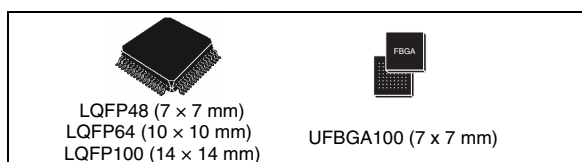
- 17 timers
  - Two 32-bit timer and three 16-bit timers with up to 4 IC/OC/PWM or pulse counter
  - Two 16-bit timers with up to 2 IC/OC/PWM or pulse counter
  - Four 16-bit timers with up to 1 IC/OC/PWM or pulse counter
  - Independent and system watchdog timers
  - SysTick timer: 24-bit downcounter
  - Three 16-bit basic timers to drive the DAC
- Calendar RTC with Alarm and periodic wakeup from Stop/Standby
- Communication interfaces
  - CAN interface (2.0B Active)
  - Two I2C interfaces; one supporting Fast Mode Plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus, wakeup from STOP
  - Three USARTs supporting master synchronous SPI and modem control; with ISO7816 interface, LIN, IrDA capability, auto baud rate detection, wakeup feature
  - Three SPIs (18 Mbit/s) with 4 to 16 programmable bit frame, muxed I2S
  - HDMI-CEC bus interface
  - USB 2.0 full speed interface
- Serial wire devices, JTAG, Cortex-M4F ETM
- 96-bit unique ID

### Table 1. Device summary

| Reference | Part number |
|---|---|
| STM32F372xx | STM32F372C8, STM32F372R8, STM32F372V8, STM32F372CB, STM32F372RB, STM32F372VB, STM32F372CC, STM32F372RC, STM32F372VC |
| STM32F373xx | STM32F373C8, STM32F373R8, STM32F373V8, STM32F373CB, STM32F373RB, STM32F373VB, STM32F373CC, STM32F373RC, STM32F373VC |

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# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F37x microcontrollers.

This STM32F37x datasheet should be read in conjunction with the STM32F37x reference manual. The reference manual is available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M4F core please refer to the Cortex™-M4F Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.subset.cortexm.m4/index.html

# 2 Description

The STM32F37x family is based on the high-performance ARM® Cortex™-M4F 32-bit RISC core operating at a frequency of up to 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an embedded trace macrocell (ETM). The family incorporates high-speed embedded memories (up to 256 Kbyte of Flash memory, up to 32 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The STM32F37x devices offer one fast 12-bit ADC (1 Msps), up to three 16-bit Sigma delta ADCs, up to two Comparators, up to two DACs (DAC1 with 2 channels and DAC2 with 1 channel), a low-power RTC, 9 general-purpose 16-bit timers, two general-purpose 32-bit timers, three basic timers.

They also feature standard and advanced communication interfaces: up to two I2Cs, three SPIs, all with muxed I2Ss, three USARTs, CAN and USB.

The STM32F37x family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F37x family offers devices in five packages ranging from 48 pins to 100 pins. The set of included peripherals changes with the device chosen.

**Table 2. Device overview**

| Peripheral | | STM32F 372Cx | | | STM32F 372Rx | | | STM32F 372Vx | | | STM32F 373Cx | | | STM32F 373Rx | | | STM32F 373Vx | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Flash (Kbytes) | | 64 | 128 | 256 | 64 | 128 | 256 | 64 | 128 | 256 | 64 | 128 | 256 | 64 | 128 | 256 | 64 | 128 | 256 |
| SRAM (Kbytes) | | 16 | 24 | 32 | 16 | 24 | 32 | 16 | 24 | 32 | 16 | 24 | 32 | 16 | 24 | 32 | 16 | 24 | 32 |
| Timers | General purpose | 9 (16-bit) 2 (32 bit) | | | | | | | | | 9 (16-bit) 2 (32 bit) | | | | | | | | |
| | Basic | 3 (16-bit) | | | | | | | | | 3 (16-bit) | | | | | | | | |
| Comm. interfaces | SPI/I2S | 3 | | | | | | | | | 3 | | | | | | | | |
| | I$^2$C | 2 | | | | | | | | | 2 | | | | | | | | |
| | USART | 3 | | | | | | | | | 3 | | | | | | | | |
| | CAN | 1 | | | | | | | | | 1 | | | | | | | | |
| | USB | 1 | | | | | | | | | 1 | | | | | | | | |
| GPIOs | Normal I/Os (TC, TTa) | 36 | | | 52 | | | 84 | | | 36 | | | 52 | | | 84 | | |
| | 5 volts Tolerant I/Os (FT, Ftf) | 20 | | | 28 | | | 45 | | | 20 | | | 28 | | | 45 | | |
| 12-bit ADCs | | 1 | | | | | | | | | 1 | | | | | | | | |
| 16-bit ADCs Sigma- Delta | | 1 | | | | | | | | | 3 | | | | | | | | |
| 12-bit DACs outputs | | 1 | | | | | | | | | 3 | | | | | | | | |
| Analog comparator | | 1 | | | | | | | | | 2 | | | | | | | | |
| CPU frequency | | 72 MHz | | | | | | | | | 72 MHz | | | | | | | | |
| Main operating voltage | | 2.0 to 3.6 V | | | | | | | | | 2.0 to 3.6 V | | | | | | | | |
| 16-bit SDADC operating voltage | | 2.2 to 3.6 V | | | | | | | | | 2.2 to 3.6 V | | | | | | | | |
| Operating temperature | | Ambient operating temperature: −40 to 85 °C / −40 to 105 °C Junction temperature: −40 to 125 °C | | | | | | | | | Ambient operating temperature: −40 to 85 °C / −40 to 105 °C Junction temperature: −40 to 125 °C | | | | | | | | |
| Packages | | LQFP48 | | | LQFP64 | | | LQFP100, UFBGA100[1] | | | LQFP48 | | | LQFP64 | | | LQFP100, UFBGA100[1] | | |

1. UFBGA100 package available on 256-KB versions only.

## Figure 1.    Block diagram
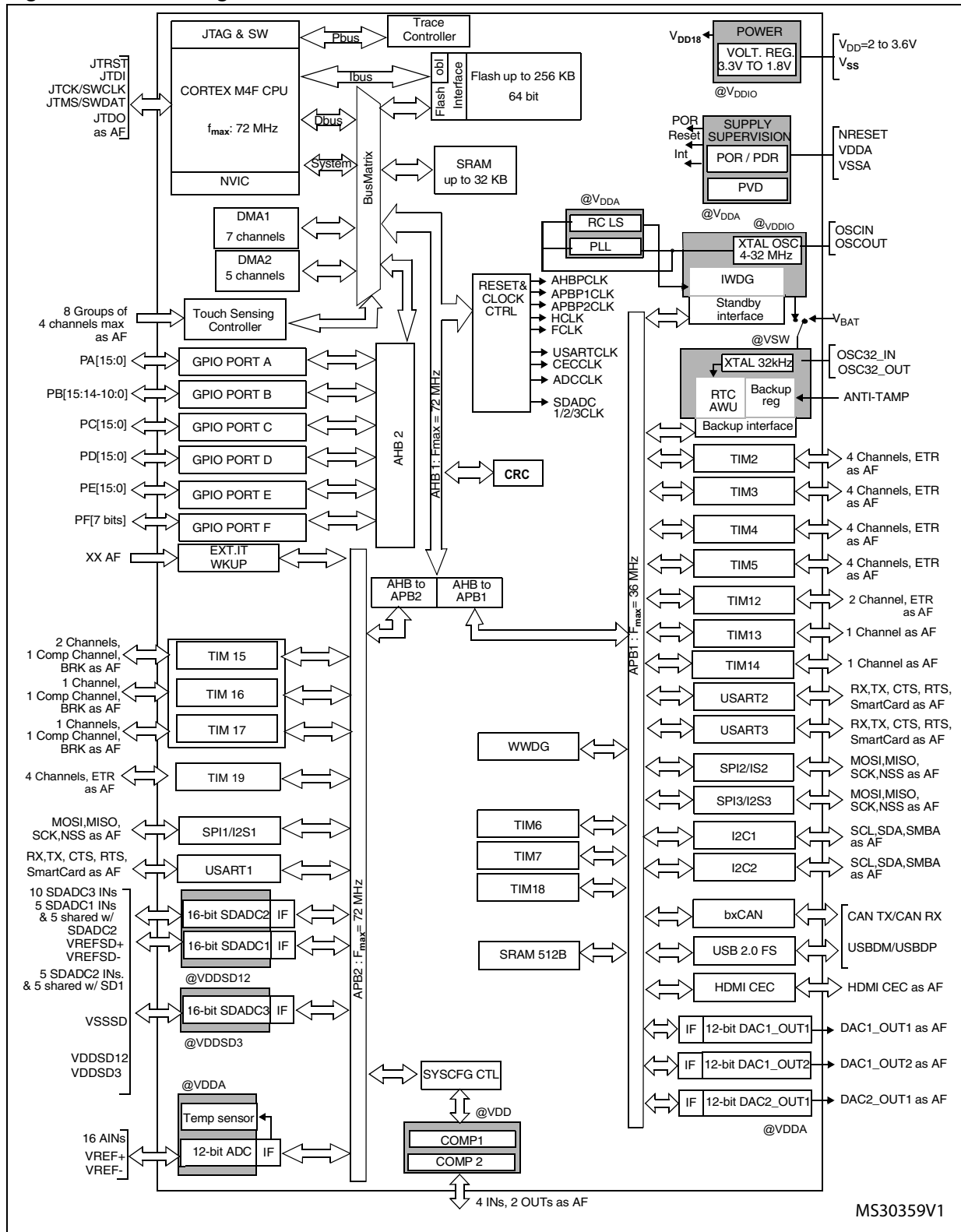


1.   AF: alternate function on I/O pins.

2.   Example given for STM32F373xx device.

# 3 Functional overview

## 3.1 ARM® Cortex™-M4F core with embedded Flash and SRAM

The ARM Cortex-M4F processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4F 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F37x family is compatible with all ARM tools and software.

*Figure 1* shows the general block diagram of the STM32F37x family.

## 3.2 Memory protection unit

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU can manage up to 8 protection areas that can all be further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

The Cortex-M4F processor is a high performance 32-bit processor designed for the microcontroller market. It offers significant benefits to developers, including:

● Outstanding processing performance combined with fast interrupt handling
● Enhanced system debug with extensive breakpoint and trace capabilities
● Efficient processor core, system and memories
● Ultralow power consumption with integrated sleep modes
● Platform security robustness with optional integrated memory protection unit (MPU).

With its embedded ARM core, the STM32F37x devices are compatible with all ARM development tools and software.

## 3.3 Embedded Flash memory

All STM32F37x devices feature up to 256 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

## 3.4 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

## 3.5 Embedded SRAM

All STM32F37x devices feature up to 32 Kbytes of embedded SRAM with hardware parity check. The memory can be accessed in read/write at CPU clock speed with 0 wait states.

## 3.6 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:
● Boot from user Flash
● Boot from system memory
● Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1, USART2 or USB.

## 3.7 Power management

### 3.7.1 Power supply schemes

● $V_{DD}$: external power supply for I/Os and the internal regulator. It is provided externally through $V_{DD}$ pins, and can be 2.0 to 3.6 V.
● $V_{DDA}$ = 2.0 to 3.6 V:
  – external analog power supplies for Reset blocks, RCs and PLL
  – supply voltage for 12-bit ADC, DACs and comparators (minimum voltage to be applied to $V_{DDA}$ is 2.4 V when the 12-bit ADC and DAC are used).
● VDDSD12 and VDDSD3= 2.2 V to 3.6: supply voltages for SDADC1/2 and SDADCD3 sigma delta ADCs. Independent from $V_{DD}/V_{DDA}$.
● $V_{BAT}$ = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.

### 3.7.2 Power supply supervisor

- The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit. The POR monitors only the $V_{DD}$ supply voltage. During the startup phase it is required that $V_{DDA}$ should arrive first and be greater than or equal to $V_{DD}$.

- The PDR monitors both the $V_{DD}$ and $V_{DDA}$ supply voltages, however the $V_{DDA}$ power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that $V_{DDA}$ is higher than or equal to $V_{DD}$.

The device features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}$ power supply and compares it to the $V_{PVD}$ threshold. An interrupt can be generated when $V_{DD}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.7.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR), and power-down.

- The MR mode is used in the nominal regulation mode (Run)
- The LPR mode is used in Stop mode.
- The power-down mode is used in Standby mode: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The voltage regulator is always enabled after reset. It is disabled in Standby mode.

### 3.7.4 Low-power modes

The STM32F37x supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the USARTs, the I2Cs, the CEC, the USB wakeup, and the RTC alarm.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering

Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

*Note:*       *The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

## 3.8       Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

## 3.9       GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Do not reconfigure GPIO pins which are not present on 48 and 64 pin packages to the analog mode. Additional current consumption in the range of tens of µA per pin can be observed if $V_{DDA}$ is higher than $V_{DDIO}$.

## 3.10      DMA (direct memory access)

The flexible 12-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The two DMAs can be used with the main peripherals: SPIs, I2Cs, USARTs, DACs, ADC, SDADCs, general-purpose timers.

## 3.11 Interrupts and events

### 3.11.1 Nested vectored interrupt controller (NVIC)

The STM32F37x devices embed a nested vectored interrupt controller (NVIC) able to handle up to 60 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:
● Closely coupled NVIC gives low latency interrupt processing
● Interrupt entry vector table address passed directly to the core
● Closely coupled NVIC core interface
● Allows early processing of interrupts
● Processing of late arriving higher priority interrupts
● Support for tail chaining
● Processor state automatically saved
● Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

### 3.11.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 29 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 84 GPIOs can be connected to the 16 external interrupt lines.

## 3.12 12-bit ADC (analog-to-digital converter)

The 12-bit analog-to-digital converter is based on a successive approximation register (SAR) architecture. It has up to 16 external channels (AIN15:0) and 3 internal channels (temperature sensor, voltage reference, $V_{BAT}$ voltage measurement) performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the timers (TIMx) can be internally connected to the ADC start and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

### 3.12.1 Temperature sensor

The temperature sensor (TS) generates a voltage $V_{SENSE}$ that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

**Table 3.    Temperature sensor calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| TS_CAL1 | TS ADC raw data acquired at temperature of 30 °C, $V_{DDA}$= 3.3 V | 0x1FFF F7B8 - 0x1FFF F7B9 |
| TS_CAL2 | TS ADC raw data acquired at temperature of 110 °C $V_{DDA}$= 3.3 V | 0x1FFF F7C2 - 0x1FFF F7C3 |

### 3.12.2 Internal voltage reference ($V_{REFINT}$)

The internal voltage reference ($V_{REFINT}$) provides a stable (bandgap) voltage output for the ADC and Comparators. $V_{REFINT}$ is internally connected to the ADC_IN17 input channel. The precise voltage of $V_{REFINT}$ is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

**Table 4.    Temperature sensor calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| VREFINT_CAL | Raw data acquired at temperature of 30 °C $V_{DDA}$= 3.3 V | 0x1FFF F7BA - 0x1FFF F7BB |

### 3.12.3 $V_{BAT}$ battery voltage monitoring

This embedded hardware feature allows the application to measure the $V_{BAT}$ battery voltage using the internal ADC channel ADC_IN18. As the $V_{BAT}$ voltage may be higher than $V_{DDA}$, and thus outside the ADC input range, the $V_{BAT}$ pin is internally connected to a divider by 2. As a consequence, the converted digital value is half the $V_{BAT}$ voltage.

## 3.13 16-bit sigma delta analog-to-digital converters (SDADC)

Up to three 16-bit sigma-delta analog-to-digital converters are embedded in the STM32F37x. They have up to two separate supply voltages allowing the analog function voltage range to be independent from the STM32F37x power supply. They share up to 21 input pins which may be configured in any combination of single-ended (up to 21) or differential inputs (up to 11).

The conversion speed is up to 16.6 ksps for each SDADC when converting multiple channels and up to 50 ksps per SDADC if single channel conversion is used. There are two conversion modes: single conversion mode or continuous mode, capable of automatically scanning any number of channels. The data can be automatically stored in a system RAM buffer, reducing the software overhead.

A timer triggering system can be used in order to control the start of conversion of the three SDADCs and/or the 12-bit fast ADC. This timing control is very flexible, capable of triggering simultaneous conversions or inserting a programmable delay between the ADCs.

Up to two external reference pins (VREFSD+, VREFSD-) and an internal 1.2/1.8V reference can be used in conjunction with a programmable gain (x0.5 to x32) in order to fine-tune the input voltage range of the SDADC.

## 3.14 DAC (digital-to-analog converter)

The devices feature up to two 12-bit buffered DACs with three output channels that can be used to convert three digital signals into three analog voltage signal outputs. The internal structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital Interface supports the following features:

● Up to two DAC converters with three output channels:
    – DAC1 with two output channels
    – DAC2 with one output channel.
● 8-bit or 12-bit monotonic output
● Left or right data alignment in 12-bit mode
● Synchronized update capability
● Noise-wave generation
● triangular-wave generation
● Dual DAC channel independent or simultaneous conversions (DAC1 only)
● DMA capability for each channel
● External triggers for conversion

## 3.15 Fast comparators

The STM32F37x embeds up to 2 comparators with rail-to-rail inputs and high-speed output. The reference voltage can be internal or external (delivered by an I/O).

The threshold can be one of the following:

● DACs channel outputs
● External I/O
● Internal reference voltage ($V_{REFINT}$) or submultiple (1/4 $V_{REFINT}$, 1/2 $V_{REFINT}$ and 3/4 $V_{REFINT}$)

The comparators can be combined into a window comparator.

Both comparators can wake up the device from Stop mode and generate interrupts and breaks for the timers.

## 3.16 Touch sensing controller (TSC)

The device has an embedded independent hardware controller (TSC) for controlling touch sensing acquisitions on the I/Os.

Up to 24 touch sensing electrodes can be controlled by the TSC. The touch sensing I/Os are organized in 8 acquisition groups, with up to 4 I/Os in each group.

**Table 5. Capacitive sensing GPIOs available on STM32F37x devices**

| Pin name | Capacitive sensing signal name | Pin name | Capacitive sensing signal name |
|----------|--------------------------------|----------|--------------------------------|
| PA0 | TSC_G1_IO1 | PA9 | TSC_G4_IO1 |
| PA1 | TSC_G1_IO2 | PA10 | TSC_G4_IO2 |
| PA2 | TSC_G1_IO3 | PA13 | TSC_G4_IO3 |
| PA3 | TSC_G1_IO4 | PA14 | TSC_G4_IO4 |
| PA4 | TSC_G2_IO1 | PB3 | TSC_G5_IO1 |
| PA5 | TSC_G2_IO2 | PB4 | TSC_G5_IO2 |
| PA6 | TSC_G2_IO3 | PB6 | TSC_G5_IO3 |
| PA7 | TSC_G2_IO4 | PB7 | TSC_G5_IO4 |
| PC4 | TSC_G3_IO1 | PB14 | TSC_G6_IO1 |
| PC5 | TSC_G3_IO2 | PB15 | TSC_G6_IO2 |
| PB0 | TSC_G3_IO3 | PD8 | TSC_G6_IO3 |
| PB1 | TSC_G3_IO4 | PD9 | TSC_G6_IO4 |
| PE2 | TSC_G7_IO1 | PD12 | TSC_G8_IO1 |
| PE3 | TSC_G7_IO2 | PD13 | TSC_G8_IO2 |
| PE4 | TSC_G7_IO3 | PD14 | TSC_G8_IO3 |
| PE5 | TSC_G7_IO4 | PD15 | TSC_G8_IO4 |

**Table 6.    No. of capacitive sensing channels available on STM32F37x devices**

| Analog I/O group | Number of capacitive sensing channels | | |
|---|---|---|---|
| | STM32F37xCx | STM32F37xRx | STM32F37xVx |
| G1 | 3 | 3 | 3 |
| G2 | 2 | 3 | 3 |
| G3 | 1 | 3 | 3 |
| G4 | 3 | 3 | 3 |
| G5 | 3 | 3 | 3 |
| G6 | 2 | 2 | 3 |
| G7 | 0 | 0 | 3 |
| G8 | 0 | 0 | 3 |
| Number of capacitive sensing channels | 14 | 17 | 24 |

## 3.17    Timers and watchdogs

The STM32F37x includes two 32-bit and nine 16-bit general-purpose timers, three basic timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

**Table 7.    Timer feature comparison**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/ compare Channels | Complementary outputs |
|---|---|---|---|---|---|---|---|
| General-purpose | TIM2 TIM5 | 32-bit | Up, Down, Up/Down | Any integer between 1 and 65536 | Yes | 4 | 0 |
| General-purpose | TIM3, TIM4, TIM19 | 16-bit | Up, Down, Up/Down | Any integer between 1 and 65536 | Yes | 4 | 0 |
| General-purpose | TIM12 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | 0 |
| General-purpose | TIM15 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 2 | 1 |
| General-purpose | TIM13, TIM14 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | 0 |

**Table 7.     Timer feature comparison (continued)**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/ compare Channels | Complementary outputs |
|---|---|---|---|---|---|---|---|
| General-purpose | TIM16, TIM17 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 1 | 1 |
| Basic | TIM6, TIM7, TIM18 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | 0 |

### 3.17.1     General-purpose timers (TIM2 to TIM5, TIM12 to TIM17, TIM19)

There are eleven synchronizable general-purpose timers embedded in the STM32F37x (see *Table 7* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

● TIM2, 3, 4, 5 and 19

These five timers are full-featured general-purpose timers:

– TIM2 and TIM5 have 32-bit auto-reload up/downcounters and 32-bit prescalers

– TIM3, 4, and 19 have 16-bit auto-reload up/downcounters and 16-bit prescalers.

These timers all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

The counters can be frozen in debug mode.

All have independent DMA request generation and support quadrature encoders.

● TIM12, 13, 14, 15, 16, 17

These six timers general-purpose timers with mid-range features:

They have 16-bit auto-reload upcounters and 16-bit prescalers.

– TIM12 has 2 channels

– TIM13 and TIM14 have 1 channel

– TIM15 has 2 channels and 1 complementary channel

– TIM16 and TIM17 have 1 channel and 1 complementary channel

All channels can be used for input capture/output compare, PWM or one-pulse mode output.

The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

The counters can be frozen in debug mode.

### 3.17.2     Basic timers (TIM6, TIM7, TIM18)

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

### 3.17.3 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### 3.17.4 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB1 clock (PCLK1) derived from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 3.17.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

● A 24-bit down counter
● Autoreload capability
● Maskable system interrupt generation when the counter reaches 0.
● Programmable clock source

## 3.18 Real-time clock (RTC) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on $V_{DD}$ supply when present or through the $V_{BAT}$ pin.The backup registers are thirty two 32-bit registers used to store 128 bytes of user application data when $V_{DD}$ power is not present.

They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

● Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
● Automatically correction for 28, 29 (leap year), 30, and 31 day of the month.
● 2 programmable alarms with wake up from Stop and Standby mode capability.
● Periodic wakeup unit with programmable resolution and period.
● On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
● Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
● 3 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
● Timestamp feature which can be used to save the calendar content. This function can triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

● A 32.768 kHz external crystal

● A resonator or oscillator

● The internal low-power RC oscillator (typical frequency of 40 kHz)

● The high-speed external clock divided by 32

## 3.19 I$^2$C bus

Up to two I2C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes with 20 mA output drive. They support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

**Table 8.    Comparison of I2C analog and digital filters**

|  | **Analog filter** | **Digital filter** |
|---|---|---|
| Pulse width of suppressed spikes | ≥ 50 ns | Programmable length from 1 to 15 I2C peripheral clocks |
| Benefits | Available in Stop mode | 1. Extra filtering capability vs. standard requirements. 2. Stable length |
| Drawbacks | Variations depending on temperature, voltage, process | Disabled when Wakeup from Stop mode is enabled |

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeout verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the application to wake up the MCU from Stop mode on address match.

The I2C interfaces can be served by the DMA controller

Refer to *Table 9* for the differences between I2C1 and I2C2.

**Table 9.    STM32F37x I$^2$C implementation**

| I2C features[1] | I2C1 | I2C2 |
|---|---|---|
| 7-bit addressing mode | X | X |
| 10-bit addressing mode | X | X |
| Standard mode (up to 100 kbit/s) | X | X |
| Fast mode (up to 400 kbit/s) | X | X |
| Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s) | X | |
| Independent clock | X | |
| SMBus | X | |
| Wakeup from STOP | X | |

1.   X = supported.

## 3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F37x embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

All USARTs interfaces are able to communicate at speeds of up to 9 Mbit/s.

They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode, Smart Card mode (ISO 7816 compliant), autobaudrate feature and have LIN Master/Slave capability. The USART interfaces can be served by the DMA controller.

Refer to *Table 10* for the features of USART1, USART2 and USART3.

**Table 10. STM32F37x USART implementation**

| USART modes/features[1] | USART1 | USART2 | USART3 |
|---|---|---|---|
| Hardware flow control for modem | X | X | X |
| Continuous communication using DMA | X | X | X |
| Multiprocessor communication | X | X | X |
| Synchronous mode | X | X | X |
| Smartcard mode | X | X | X |
| Single-wire half-duplex communication | X | X | X |
| IrDA SIR ENDEC block | X | X | X |
| LIN mode | X | X | X |
| Dual clock domain and wakeup from Stop mode | X | X | X |
| Receiver timeout interrupt | X | X | X |
| Modbus communication | X | X | X |
| Auto baud rate detection | X | X | X |
| Driver Enable | X | X | X |

1.   X = supported.

## 3.21 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I²S)

Up to three SPIs are able to communicate at up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPIs can be served by the DMA controller.

Three standard I²S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I²S interfaces is/are configured in

master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

Refer to *Table 11* for the features between SPI1 and SPI2.

**Table 11.    STM32F37x SPI/I2S implementation**

| SPI features[1] | SPI1 | SPI2 | SPI3 |
|---|---|---|---|
| Hardware CRC calculation | X | X | X |
| Rx/Tx FIFO | X | X | X |
| NSS pulse mode | X | X | X |
| I2S mode | X | X | X |
| TI mode | X | X | X |

1.   X = supported.

## 3.22    High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

## 3.23    Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

## 3.24    Universal serial bus (USB)

The STM32F37x embeds an USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

## 3.25 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

## 3.26 Embedded trace macrocell™

The ARM embedded trace macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F37x through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

# 4     Pinouts and pin description

**Figure 2. STM32F37x LQFP48 pinout**
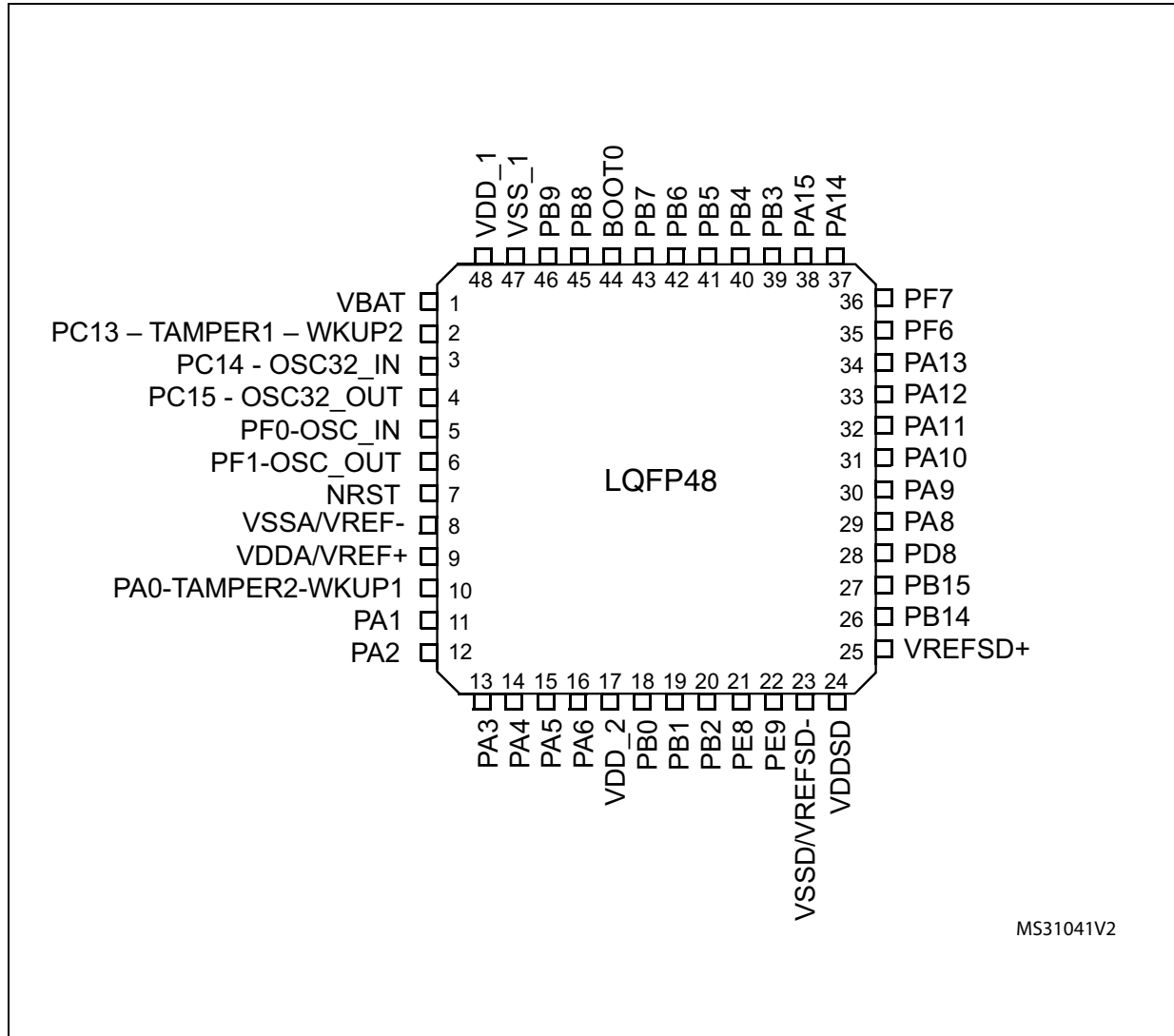
**Figure 3. STM32F37x LQFP64 pinout**



MS31045V1
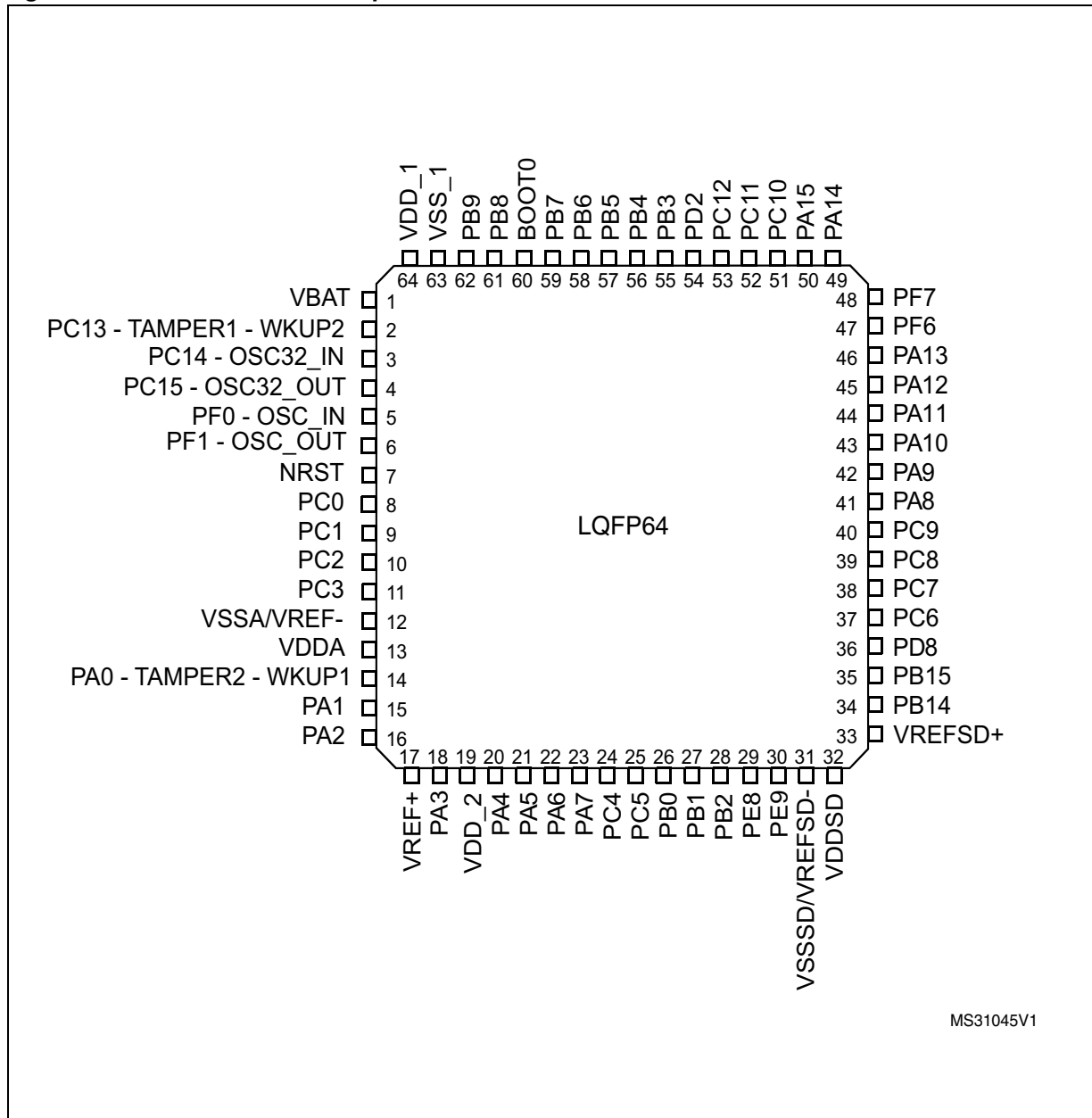
**Figure 4.    STM32F37x LQFP100 pinout**



LQFP100
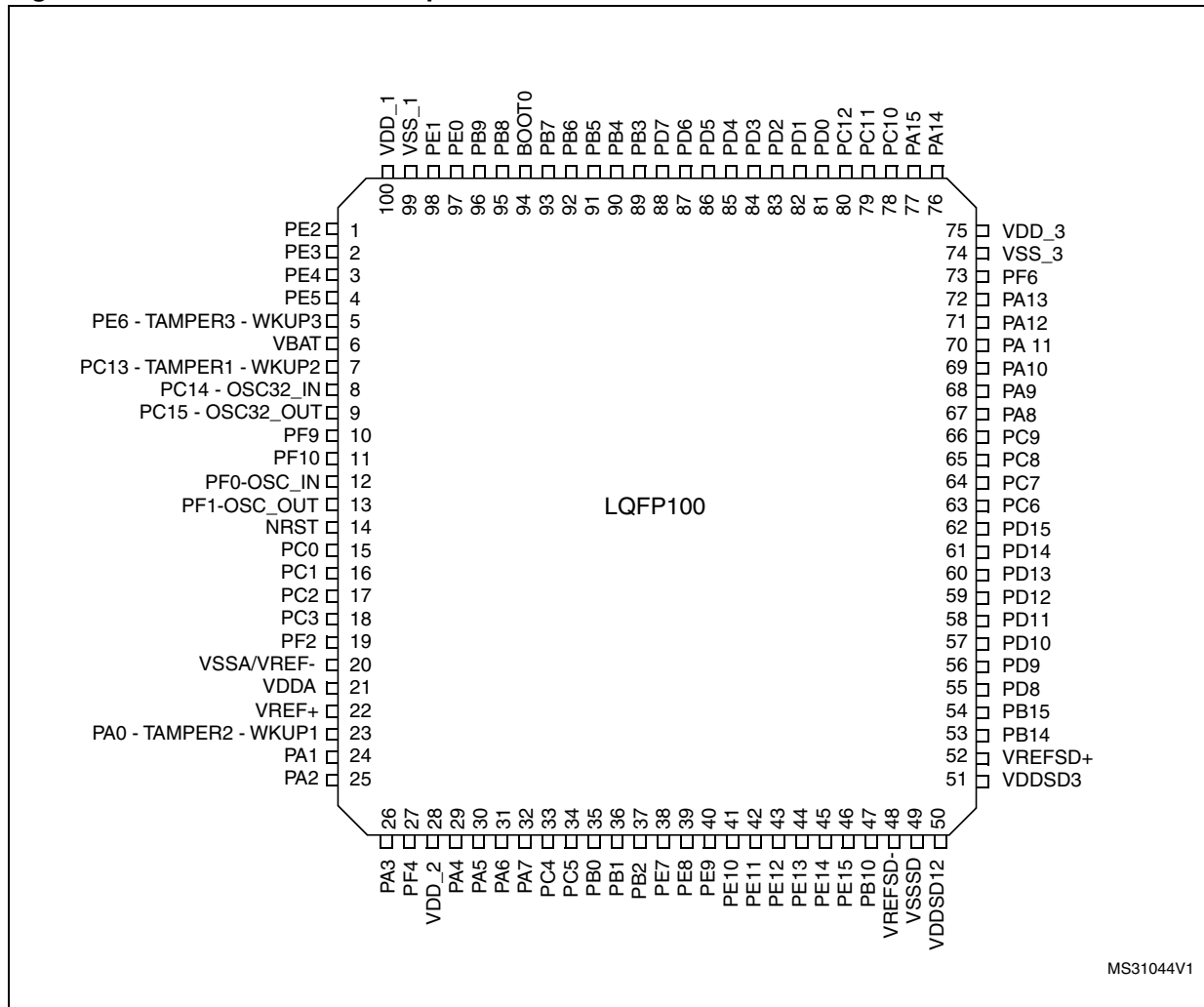
MS31044V1

**Figure 5. STM32F37x BGA100 pinout**
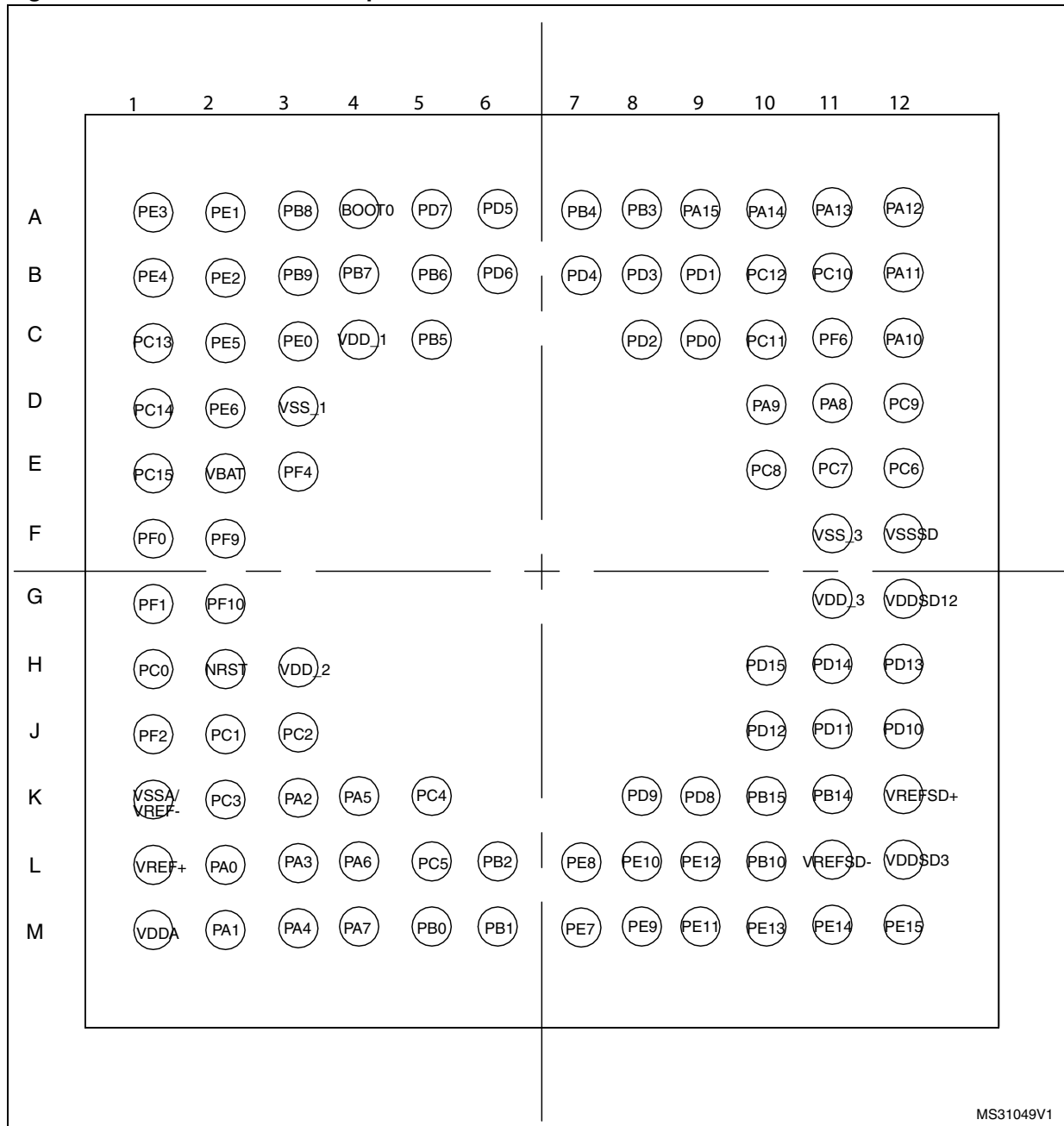


MS31049V1

**Table 12.    Legend/abbreviations used in the pinout table**

| Name | Abbreviation | Definition |
|---|---|---|
| Pin name | | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name |
| Pin type | S | Supply pin |
| | I | Input only pin |
| | I/O | Input / output pin |
| I/O structure | FT | 5 V tolerant I/O |
| | FTf | 5 V tolerant I/O, FM+ capable |
| | TTa | 3.3 V tolerant I/O directly connected to ADC |
| | TC | Standard 3.3V I/O |
| | B | Dedicated BOOT0 pin |
| | RST | Bidirectional reset pin with embedded weak pull-up resistor |
| Notes | | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset |
| Pin functions | Alternate functions | Functions selected through GPIOx_AFR registers |
| | Additional functions | Functions directly selected/enabled through peripheral registers |

**Table 13.    STM32F37x pin definitions**

| Pin numbers | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | BGA100 | LQFP64 | LQFP48 | | | | | Alternate function | Additional functions |
| 1 | B2 | | | PE2 | I/O | FT | (1) | TSC_G7_IO1, TRACECLK | |
| 2 | A1 | | | PE3 | I/O | FT | (1) | TSC_G7_IO2, TRACED0 | |
| 3 | B1 | | | PE4 | I/O | FT | (1) | TSC_G7_IO3, TRACED1 | |
| 4 | C2 | | | PE5 | I/O | FT | (1) | TSC_G7_IO4, TRACED2 | |
| 5 | D2 | | | PE6 - TAMPER3 - WKUP3 | I/O | FT | (1) | TRACED3 | WKUP3, RTC_TAMPER3 |
| 6 | E2 | 1 | 1 | VBAT | S | | | | |
| 7 | C1 | 2 | 2 | PC13 - TAMPER1 - WKUP2 | I/O | TC | | | WKUP2_ALARM_OUT_ CALIB_OUT_TIMESTAMP, RTC_TAMPER1 |
| 8 | D1 | 3 | 3 | PC14 - OSC32_IN | I/O | TC | | | OSC32_IN |

**Table 13.    STM32F37x pin definitions (continued)**

| Pin numbers | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | BGA100 | LQFP64 | LQFP48 | | | | | Alternate function | Additional functions |
| 9 | E1 | 4 | 4 | PC15 - OSC32_OUT | I/O | TC | | | OSC32_OUT |
| 10 | F2 | | | PF9 | I/O | FT | (1) | TIM14_CH1 | |
| 11 | G2 | | | PF10 | I/O | FT | (1) | | |
| 12 | F1 | 5 | 5 | PF0 - OSC_IN | I/O | FTf | | I2C2_SDA | OSC_IN |
| 13 | G1 | 6 | 6 | PF1 - OSC_OUT | I/O | FTf | | I2C2_SCL | OSC_OUT |
| 14 | H2 | 7 | 7 | NRST | I/O | RST | | | |
| 15 | H1 | 8 | | PC0 | I/O | TTa | (1) | TIM5_CH1_ETR | ADC_IN10 |
| 16 | J2 | 9 | | PC1 | I/O | TTa | (1) | TIM5_CH2 | ADCIN11 |
| 17 | J3 | 10 | | PC2 | I/O | TTa | (1) | SPI2_MISO/I2S2_MCK, TIM5_CH3 | ADC_IN12 |
| 18 | K2 | 11 | | PC3 | I/O | TTa | (1) | SPI2_MOSI/I2S2_SD, TIM5_CH4 | ADC_IN13 |
| 19 | J1 | | | PF2 | I/O | FT | (1) | I2C2_SMBAI | |
| 20 | K1 | 12 | 8 | VSSA/VREF- | S | | | | |
| | | | 9 | VDDA/VREF+ | S | | (1) | | |
| 21 | M1 | 13 | | VDDA | S | | (1) | | |
| 22 | L1 | 17 | | VREF+ | S | | (1) | | |
| 23 | L2 | 14 | 10 | PA0 - TAMPER2 - WKUP1 | I/O | TTa | | USART2_CTS, TIM2_CH1_ETR, TIM5_CH1_ETR, TIM19_CH1, TSC_G1_IO1, COMP1_OUT | RTC_ TAMPER2, WKUP1, ADC_IN0,COMP1_INn |
| 24 | M2 | 15 | 11 | PA1 | I/O | TTa | | SPI3_SCK/I2S3_CK, USART2_RTS, TIM2_CH2, TIM15_CH1N, TIM5_CH2, TIM19_CH2, TSC_G1_IO2, | ADC_IN1,COMP1_INp, RTC_REF_CLK_IN |
| 25 | K3 | 16 | 12 | PA2 | I/O | TTa | | COMP2_OUT, SPI3_MISO/I2S3_MCK, USART2_TX, TIM2_CH3, TIM15_CH1, TIM5_CH3, TIM19_CH3, TSC_G1_IO3 | ADC_IN2, COMP2_INn |
| 26 | L3 | 18 | 13 | PA3 | I/O | TTa | | SPI3_MOSI/I2S3_SD, USART2_RX, TIM2_CH4, TIM15_CH2, TIM5_CH4, TIM19_CH4, TSC_G1_IO4 | ADC_IN3, COMP2_Inp |
| 27 | E3 | | | PF4 | I/O | FT | (1) | | |

**Table 13. STM32F37x pin definitions (continued)**

| Pin numbers | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | BGA100 | LQFP64 | LQFP48 | | | | | Alternate function | Additional functions |
| 28 | H3 | 19 | 17 | VDD_2 | S | | | | |
| 29 | M3 | 20 | 14 | PA4 | I/O | TTa | | SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, TIM3_CH2, TIM12_CH1, TSC_G2_IO1, | ADC_IN4, DAC1_OUT1 |
| 30 | K4 | 21 | 15 | PA5 | I/O | TTa | | SPI1_SCK/I2S1_CK, CEC, TIM2_CH1_ETR, TIM14_CH1, TIM12_CH2, TSC_G2_IO2 | ADC_IN5, DAC1_OUT2 |
| 31 | L4 | 22 | 16 | PA6 | I/O | TTa | | SPI1_MISO/I2S1_MCK, COMP1_OUT, TIM3_CH1, TIM13_CH1, TIM16_CH1, TSC_G2_IO3 | ADC_IN6, DAC2_OUT1, |
| 32 | M4 | 23 | | PA7 | I/O | TTa | (1) | TSC_G2_IO4, TIM14_CH1, SPI1_MOSI/I2S1_SD, TIM17_CH1, TIM3_CH2, COMP2_OUT | ADC_IN7 |
| 33 | K5 | 24 | | PC4 | I/O | TTa | (1) | TIM13_CH1, TSC_G3_IO1, USART1_TX | ADC_IN14 |
| 34 | L5 | 25 | | PC5 | I/O | TTa | (1) | TSC_G3_IO2, USART1_RX | ADC_IN15 |
| 35 | M5 | 26 | 18 | PB0 | I/O | TTa | | SPI1_MOSI/I2S1_SD, TIM3_CH3, TSC_G3_IO3, TIM3_CH2 | ADC_IN8, SDADC1_ADC_IN6P |
| 36 | M6 | 27 | 19 | PB1 | I/O | TTa | | TIM3_CH4, TSC_G3_IO4 | ADC_IN9, SDADC1_5P, SDADC1_AIN6M |
| 37 | L6 | 28 | 20 | PB2 | I/O | TC | (2) | | SDADC1_AIN4P, SDADC2_AIN6P |
| 38 | M7 | | | PE7 | I/O | TC | (2)(1) | | SDADC1_AIN3P, SDADC1_AIN4M, SDADC2_AIN5P, SDADC2_AIN6M |
| 39 | L7 | 29 | 21 | PE8 | I/O | TC | (2) | | SDADC1_AIN8P, SDADC2_AIN8P |
| 40 | M8 | 30 | 22 | PE9 | I/O | TC | (2) | | SDADC1_AIN7P, SDADC1_AIN8M, SDADC2_AIN7P, SDADC2_AIN8M |
| 41 | L8 | | | PE10 | I/O | TC | (2)(1) | | SDADC1_AIN2P |
| 42 | M9 | | | PE11 | I/O | TC | (2)(1) | | SDADC1_AIN1P, SDADC1_AIN2M, SDADC2_AIN4P |

**Table 13. STM32F37x pin definitions (continued)**

| Pin numbers | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | BGA100 | LQFP64 | LQFP48 | | | | | Alternate function | Additional functions |
| 43 | L9 | | | PE12 | I/O | TC | (2)(1) | | SDADC1_AIN0P, SDADC2_AIN3P, SDADC2_AIN4M |
| 44 | M10 | | | PE13 | I/O | TC | (2)(1) | | SDADC1_AIN0M , SDADC2_AIN2P |
| 45 | M11 | | | PE14 | I/O | TC | (2)(1) | | SDADC2_AIN1P, SDADC2_AIN2M |
| 46 | M12 | | | PE15 | I/O | TC | (2)(1) | USART3_RX | SDADC2_AIN0P |
| 47 | L10 | | | PB10 | I/O | TC | (2)(1) | SPI2_SCK/I2S2_CK, USART3_TX, CEC, TSC_SYNC, TIM2_CH3 | SDADC2_AIN0M |
| 48 | L11 | | | VREFSD- | S | | (1) | | |
| 49 | F12 | | | VSSSD | S | | (1) | | |
| | | 31 | 23 | VSSSD/ VREFSD- | S | | | | |
| 50 | G12 | | | VDDSD12 | S | | (1) | | |
| | | 32 | 24 | VDDSD | S | | | | |
| 51 | L12 | | | VDDSD3 | S | | (1) | | |
| 52 | K12 | 33 | 25 | VREFSD+ | S | | | | |
| 53 | K11 | 34 | 26 | PB14 | I/O | TC | (3) | SPI2_MISO/I2S2_MCK, USART3_RTS, TIM15_CH1, TIM12_CH1, TSC_G6_IO1 | SDADC3_AIN8P |
| 54 | K10 | 35 | 27 | PB15 | I/O | TC | (3) | SPI2_MOSI/I2S2_SD, TIM15_CH1N, TIM15_CH2, TIM12_CH2, TSC_G6_IO2 | SDADC3_7P, SDADC3_AIN8M, RTC_REFCLKIN |
| 55 | K9 | 36 | 28 | PD8 | I/O | TC | (3) | SPI2_SCK/I2S2_CK, USART3_TX, TSC_G6_IO3 | SDADC3_AIN6P |
| 56 | K8 | | | PD9 | I/O | TC | (3)(1) | USART3_RX, TSC_G6_IO4 | SDADC3_AIN5P, SDADC3_AIN6M |
| 57 | J12 | | | PD10 | I/O | TC | (3)(1) | USART3_CK | SDADC3_AIN4P |
| 58 | J11 | | | PD11 | I/O | TC | (3)(1) | USART3_CTS | SDADC3_AIN3P, SDADC3_AIN4M |
| 59 | J10 | | | PD12 | I/O | TC | (3)(1) | USART3_RTS, TIM4_CH1, TSC_G8_IO1 | SDADC3_AIN2P |
| 60 | H12 | | | PD13 | I/O | TC | (3)(1) | TIM4_CH2, TSC_G8_IO2 | SDADC3_AIN1P, SDADC3_AIN2M |
| 61 | H11 | | | PD14 | I/O | TC | (3)(1) | TIM4_CH3, TSC_G8_IO3 | SDADC3_AIN0P |
| 62 | H10 | | | PD15 | I/O | TC | (3)(1) | TIM4_CH4, TSC_G8_IO4 | SDADC3_AIN0M |

**Table 13.    STM32F37x pin definitions (continued)**

| LQFP100 | BGA100 | LQFP64 | LQFP48 | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate function | Additional functions |
|---------|--------|--------|--------|--------------------------------|----------|---------------|-------|--------------------|----------------------|
| 63 | E12 | 37 | | PC6 | I/O | FT | (1) | TIM3_CH1, SPI1_NSS/I2S1_WS | |
| 64 | E11 | 38 | | PC7 | I/O | FT | (1) | TIM3_CH2, SPI1_SCK/I2S1_CK, | |
| 65 | E10 | 39 | | PC8 | I/O | FT | (1) | SPI1_MISO/I2S1_MCK, TIM3_CH3 | |
| 66 | D12 | 40 | | PC9 | I/O | FT | (1) | SPI1_MOSI/I2S1_SD, TIM3_CH4 | |
| 67 | D11 | 41 | 29 | PA8 | I/O | FT | | SPI2_SCK/I2S2_CK, I2C2_SMBAI, USART1_CK, TIM4_ETR, TIM5_CH1_ETR, MCO | |
| 68 | D10 | 42 | 30 | PA9 | I/O | FTf | | SPI2_MISO/I2S2_MCK, I2C2_SCL, USART1_TX, TIM2_CH3, TIM15_BKIN, TIM13_CH1, TSC_G4_IO1 | |
| 69 | C12 | 43 | 31 | PA10 | I/O | FTf | | SPI2_MOSI/I2S2_SD, I2C2_SDA, USART1_RX, TIM2_CH4, TIM17_BKIN, TIM14_CH1, TSC_G4_IO2 | |
| 70 | B12 | 44 | 32 | PA11 | I/O | FT | | SPI2_NSS/I2S2_WS, SPI1_NSS/I2S1_WS, USART1_CTS, CAN_RX, TIM4_CH1, USBDM, TIM5_CH2, COMP1_OUT | |
| 71 | A12 | 45 | 33 | PA12 | I/O | FT | | SPI1_SCK/I2S1_CK, USART1_RTS, CAN_TX, USBDP, TIM16_CH1, TIM4_CH2, TIM5_CH3, COMP2_OUT | |
| 72 | A11 | 46 | 34 | PA13 | I/O | FT | | SPI1_MISO/I2S1_MCK, USART3_CTS, IR_OUT, TIM16_CH1N, TIM4_CH3, TIM5_CH4, TSC_G4_IO3, SWDAT-JTMS | |
| 73 | C11 | 47 | 35 | PF6 | I/O | FTf | | SPI1_MOSI/I2S1_SD, USART3_RTS, TIM4_CH4, I2C2_SCL | |
| 74 | F11 | | | VSS_3 | S | | (1) | | |
| 75 | G11 | | | VDD_3 | S | | (1) | | |
| | | 48 | 36 | PF7 | I/O | FTf | | I2C2_SDA, USART2_CK | |

**Table 13.    STM32F37x pin definitions (continued)**

| Pin numbers | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | BGA100 | LQFP64 | LQFP48 | | | | | Alternate function | Additional functions |
| 76 | A10 | 49 | 37 | PA14 | I/O | FTf | | I2C1_SDA, TIM12_CH1, TSC_G4_IO4, SWCLK-JTCK | |
| 77 | A9 | 50 | 38 | PA15 | I/O | FTf | | SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, I2C1_SCL, TIM2_CH1_ETR, TIM12_CH2, TSC_SYNC, JTDI | |
| 78 | B11 | 51 | | PC10 | I/O | FT | (1) | SPI3_SCK/I2S3_CK, USART3_TX, TIM19_CH1 | |
| 79 | C10 | 52 | | PC11 | I/O | FT | (1) | SPI3_MISO/I2S3_MCK, USART3_RX, TIM19_CH2 | |
| 80 | B10 | 53 | | PC12 | I/O | FT | (1) | SPI3_MOSI/I2S3_SD, USART3_CK, TIM19_CH3 | |
| 81 | C9 | | | PD0 | I/O | FT | (1) | CAN_RX, TIM19_CH4 | |
| 82 | B9 | | | PD1 | I/O | FT | (1) | CAN_TX, TIM19_ETR | |
| 83 | C8 | 54 | | PD2 | I/O | FT | (1) | TIM3_ETR | |
| 84 | B8 | | | PD3 | I/O | FT | (1) | SPI2_MISO/I2S2_MCK, USART2_CTS | |
| 85 | B7 | | | PD4 | I/O | FT | (1) | SPI2_MOSI/I2S2_SD, USART2_RTS | |
| 86 | A6 | | | PD5 | I/O | FT | (1) | USART2_TX | |
| 87 | B6 | | | PD6 | I/O | FT | (1) | SPI2_NSS/I2S2_WS, USART2_RX | |
| 88 | A5 | | | PD7 | I/O | FT | (1) | SPI2_SCK/I2S2_CK, USART2_CK | |
| 89 | A8 | 55 | 39 | PB3 | I/O | FT | | SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, USART2_TX, TIM2_CH2, TIM3_ETR, TIM4_ETR, TIM13_CH1, TSC_G5_IO1, JTDO-TRACESWO | |
| 90 | A7 | 56 | 40 | PB4 | I/O | FT | | SPI1_MISO/I2S1_MCK, SPI3_MISO/I2S3_MCK, USART2_RX, TIM16_CH1, TIM3_CH1, TIM17_BKIN, TIM15_CH1N, TSC_G5_IO2, JNTRST | |

**Table 13.    STM32F37x pin definitions (continued)**

| Pin numbers | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | BGA100 | LQFP64 | LQFP48 | | | | | Alternate function | Additional functions |
| 91 | C5 | 57 | 41 | PB5 | I/O | FT | | SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, I2C1_SMBAl, USART2_CK, TIM16_BKIN, TIM3_CH2, TIM17_CH1, TIM19_ETR | |
| 92 | B5 | 58 | 42 | PB6 | I/O | FTf | | I2C1_SCL, USART1_TX, TIM16_CH1N, TIM3_CH3, TIM4_CH1, TIM19_CH1, TIM15_CH1, TSC_G5_IO3 | |
| 93 | B4 | 59 | 43 | PB7 | I/O | FTf | | I2C1_SDA, USART1_RX, TIM17_CH1N, TIM3_CH4, TIM4_CH2, TIM19_CH2, TIM15_CH2, TSC_G5_IO4 | |
| 94 | A4 | 60 | 44 | BOOT0 | I | B | | Boot memory selection | |
| 95 | A3 | 61 | 45 | PB8 | I/O | FTf | | SPI2_SCK/I2S2_CK, I2C1_SCL, USART3_TX, CAN_RX, CEC, TIM16_CH1, TIM4_CH3, TIM19_CH3, COMP1_OUT, TSC_SYNC | |
| 96 | B3 | 62 | 46 | PB9 | I/O | FTf | | SPI2_NSS/I2S2_WS, I2C1_SDA, USART3_RX, CAN_TX, IR_OUT, TIM17_CH1, TIM4_CH4, TIM19_CH4, COMP2_OUT | |
| 97 | C3 | | | PE0 | I/O | FT | [1] | USART1_TX,TIM4_ETR | |
| 98 | A2 | | | PE1 | I/O | FT | [1] | USART1_RX | |
| 99 | D3 | 63 | 47 | VSS_1 | S | | | Ground | |
| 100 | C4 | 64 | 48 | VDD_1 | S | | | Digital power supply | |

1.  When using the small packages (48 and 64 pin packages), the GPIO pins which are not present on these packages, must not be configured in analog mode.

2.  these pins are powered by VDDSD12.

3.  these pins are powered by VDDSD3.

**Table 14.    Alternate functions for port PA**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PA0 | | TIM2_CH1_ETR | TIM5_CH1_ETR | TSC_G1_IO1 | | | | USART2_CTS | COMP1_OUT | | | TIM19_CH1 | | EVENT OUT |
| PA1 | | TIM2_CH2 | TIM5_CH2 | TSC_G1_IO2 | | | SPI3_SCK / I2S3_CK | USART2_RTS | | TIM15_CH1N | | TIM19_CH2 | | EVENT OUT |
| PA2 | | TIM2_CH3 | TIM5_CH3 | TSC_G1_IO3 | | | SPI3_MISO/ I2S3_MCK | USART2_TX | COMP2_OUT | TIM15_CH1 | | TIM19_CH3 | | EVENT OUT |
| PA3 | | TIM2_CH4 | TIM5_CH4 | TSC_G1_IO4 | | | SPI3_MOSI / I2S3_SD | USART2_RX | | TIM15_CH2 | | TIM19_CH4 | | EVENT OUT |
| PA4 | | | TIM3_CH2 | TSC_G2_IO1 | | SPI1_NSS / I2S1_WS | SPI3_NSS / I2S3_WS | USART2_CK | | | TIM12_CH1 | | | EVENT OUT |
| PA5 | | TIM2_CH1_ETR | | TSC_G2_IO2 | | SPI1_SCK / I2S1_CK | | CEC | | TIM14_CH1 | TIM12_CH2 | | | EVENT OUT |
| PA6 | | TIM16_CH1 | TIM3_CH1 | TSC_G2_IO3 | | SPI1_MISO / I2S1_MCK | | | COMP1_OUT | TIM13_CH1 | | | | EVENT OUT |
| PA7 | | TIM17_CH1 | TIM3_CH2 | TSC_G2_IO4 | | SPI1_MOSI / I2S1_SD | | | COMP2_OUT | TIM14_CH1 | | | | EVENT OUT |
| PA8 | MCO | | TIM5_CH1_ETR | | I2C2_SMBAI | SPI2_SCK / I2S2_CK | | USART1_CK | | | TIM4_ETR | | | EVENT OUT |
| PA9 | | | TIM13_CH1 | TSC_G4_IO1 | I2C2_SCL | SPI2_MISO / I2S2_MCK | | USART1_TX | | TIM15_BKIN | TIM2_CH3 | | | EVENT OUT |
| PA10 | | TIM17_BKIN | | TSC_G4_IO2 | I2C2_SDA | SPI2_MOSI / I2S2_SD | | USART1_RX | | TIM14_CH1 | TIM2_CH4 | | | EVENT OUT |
| PA11 | | | TIM5_CH2 | | | SPI2_NSS / I2S2_WS | SPI1_NSS / I2S1_WS | USART1_CTS | COMP1_OUT | CAN_RX | TIM4_CH1 | | USBDM | EVENT OUT |
| PA12 | | TIM16_CH1 | TIM5_CH3 | | | | SPI1_SCK / I2S1_CK | USART1_RTS | COMP2_OUT | CAN_TX | TIM4_CH2 | | USBDP | EVENT OUT |

**Table 14.    Alternate functions for port PA (continued)**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PA13 | JTMS-SWDAT | TIM16_CH1N | TIM5_CH4 | TSC_G4_IO3 | | IR-Out | SPI1_MISO / I2S1_MCK | USART3_CTS | | | TIM4_CH3 | | | EVENT OUT |
| PA14 | JTCK-SWCLK | | | TSC_G4_IO4 | I2C1_SDA | | | | | | TIM12_CH1 | | | EVENT OUT |
| PA15 | JTDI | TIM2_CH1_ETR | | TSC_SYNC | I2C1_SCL | SPI1_NSS / I2S1_WS | SPI3_NSS / I2S3_WS | | | | TIM12_CH2 | | | EVENT OUT |

**Table 15.    Alternate functions for port PB**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PB0 | | | TIM3_CH3 | TSC_G3_IO3 | | SPI_MOSI / I2S1_SD | | | | | TIM3_CH2 | | EVENTOUT |
| PB1 | | | TIM3_CH4 | TSC_G3_IO4 | | | | | | | | | EVENTOUT |
| PB2 | | | | | | | | | | | | | EVENTOUT |
| PB3 | JTDO/ TRACESWO | TIM2_CH2 | TIM4_ETR | TSC_G5_IO1 | | SPI1_SCK / I2S1_CK | SPI3_SCK/ I2S3_CK | USART2_TX | | TIM13_CH1 | TIM3_ETR | | EVENTOUT |
| PB4 | JTRST | TIM16_CH1 | TIM3_CH1 | TSC_G5_IO2 | | SPI1_MISO / I2S1_MCK | SPI3_MISO/ I2S3_MCK | USART2_RX | | TIM15_CH1N | TIM17_BKIN | | EVENTOUT |
| PB5 | | TIM16_BKIN | TIM3_CH2 | | I2C1_SMBAI | SPI1_MOSI / I2S1_SD | SPI3_MOSI / I2S3_SD | USART2_CK | | TIM17_CH1 | | TIM19_ETR | EVENTOUT |
| PB6 | | TIM16_CH1N | TIM4_CH1 | TSC_G5_IO3 | I2C1_SCL | | | USART1_TX | | TIM15_CH1 | TIM3_CH3 | TIM19_CH1 | EVENTOUT |
| PB7 | | TIM17_CH1N | TIM4_CH2 | TSC_G5_IO4 | I2C1_SDA | | | USART1_RX | | TIM15_CH2 | TIM3_CH4 | TIM19_CH2 | EVENTOUT |
| PB8 | | TIM16_CH1 | TIM4_CH3 | TSC_SYNC | I2C1_SCL | SPI2_SCK / I2S2_CK | CEC | USART3_TX | COMP1_OUT | CAN_RX | | TIM19_CH3 | EVENTOUT |
| PB9 | | TIM17_CH1 | TIM4_CH4 | | I2C1_SDA | SPI2_NSS / I2S2_WS | IR-Out | USART3_RX | COMP2_OUT | CAN_TX | | TIM19_CH4 | EVENTOUT |
| PB10 | | TIM2_CH3 | | TSC_SYNCH | | SPI2_SCK / I2S2_CK | CEC | USART3_TX | | | | | EVENTOUT |
| PB14 | | TIM15_CH1 | | TSC_G6_IO1 | | SPI2_MISO / I2S2_MCK | | USART3_RTS | | TIM12_CH1 | | | EVENTOUT |
| PB15 | | TIM15_CH2 | TIM15_CH1N | TSC_G6_IO2 | | SPI2_MOSI / I2S2_SD | | | | TIM12_CH2 | | | EVENTOUT |

**Table 16.    Alternate functions for port PC**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|----------|-----|-----|-----|-----|-----|-----|-----|-----|
| PC0 | | EVENTOUT | TIM5_CH1_ETR | | | | | |
| PC1 | | EVENTOUT | TIM5_CH2 | | | | | |
| PC2 | | EVENTOUT | TIM5_CH3 | | | SPI2_MISO / I2S2_MCK | | |
| PC3 | | EVENTOUT | TIM5_CH4 | | | SPI2_MOSI / I2S2_SD | | |
| PC4 | | EVENTOUT | TIM13_CH1 | TSC_G3_IO1 | | | | USART1_TX |
| PC5 | | EVENTOUT | | TSC_G3_IO2 | | | | USART1_RX |
| PC6 | | EVENTOUT | TIM3_CH1 | | | SPI1_NSS / I2S1_WS | | |
| PC7 | | EVENTOUT | TIM3_CH2 | | | SPI1_SCK / I2S1_CK | | |
| PC8 | | EVENTOUT | TIM3_CH3 | | | SPI1_MISO/I2S1_MCK | | |
| PC9 | | EVENTOUT | TIM3_CH4 | | | SPI1_MOSI / I2S1_SD | | |
| PC10 | | EVENTOUT | TIM19_CH1 | | | | SPI3_SCK / I2S3_CK | USART3_TX |
| PC11 | | EVENTOUT | TIM19_CH2 | | | | SPI3_MISO /I2S3_MCK | USART3_RX |
| PC12 | | EVENTOUT | TIM19_CH3 | | | | SPI3_MOSI / I2S3_SD | USART3_CK |
| PC13 | | | | | | | | |
| PC14 | | | | | | | | |
| PC15 | | | | | | | | |

**Table 17. Alternate functions for port PD**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|
| PD0 | | EVENTOUT | TIM19_CH4 | | | | | CAN_RX |
| PD1 | | EVENTOUT | TIM19_ETR | | | | | CAN_TX |
| PD2 | | EVENTOUT | TIM3_ETR | | | | | |
| PD3 | | EVENTOUT | | | | SPI2_MISO / I2S2_MCK | | USART2_CTS |
| PD4 | | EVENTOUT | | | | SPI2_MOSI / I2S2_SD | | USART2_RTS |
| PD5 | | EVENTOUT | | | | | | USART2_TX |
| PD6 | | EVENTOUT | | | | SPI2_NSS / I2S2_WS | | USART2_RX |
| PD7 | | EVENTOUT | | | | SPI2_SCK / I2S2_CK | | USART2_CK |
| PD8 | | EVENTOUT | | TSC_G6_IO3 | | SPI2_SCK / I2S2_CK | | USART3_TX |
| PD9 | | EVENTOUT | | TSC_G6_IO4 | | | | USART3_RX |
| PD10 | | EVENTOUT | | | | | | USART3_CK |
| PD11 | | EVENTOUT | | | | | | USART3_CTS |
| PD12 | | EVENTOUT | TIM4_CH1 | TSC_G8_IO1 | | | | USART3_RTS |
| PD13 | | EVENTOUT | TIM4_CH2 | TSC_G8_IO2 | | | | |
| PD14 | | EVENTOUT | TIM4_CH3 | TSC_G8_IO3 | | | | |
| PD15 | | EVENTOUT | TIM4_CH4 | TSC_G8_IO4 | | | | |

**Table 18. Alternate functions for port PE**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|----------|-----|-----|-----|-----|-----|-----|-----|-----|
| PE0 | | EVENTOUT | TIM4_ETR | | | | | USART1_TX |
| PE1 | | EVENTOUT | | | | | | USART1_RX |
| PE2 | TRACECLK | EVENTOUT | | TSC_G7_IO1 | | | | |
| PE3 | TRACED0 | EVENTOUT | | TSC_G7_IO2 | | | | |
| PE4 | TRACED1 | EVENTOUT | | TSC_G7_IO3 | | | | |
| PE5 | TRACED2 | EVENTOUT | | TSC_G7_IO4 | | | | |
| PE6 | TRACED3 | EVENTOUT | | | | | | |
| PE7 | | EVENTOUT | | | | | | |
| PE8 | | EVENTOUT | | | | | | |
| PE9 | | EVENTOUT | | | | | | |
| PE10 | | EVENTOUT | | | | | | |
| PE11 | | EVENTOUT | | | | | | |
| PE12 | | EVENTOUT | | | | | | |
| PE13 | | EVENTOUT | | | | | | |
| PE14 | | EVENTOUT | | | | | | |
| PE15 | | EVENTOUT | | | | | | USART3_RX |

**Table 19.    Alternate functions for port PF**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|----------|-----|-----|-----|-----|-----|-----|-----|-----|
| PF0 | | | | | I2C2_SDA | | | |
| PF1 | | | | | I2C2_SCL | | | |
| PF2 | | EVENTOUT | | | I2C2_SMBAI | | | |
| PF4 | | EVENTOUT | | | | | | |
| PF6 | | EVENTOUT | TIM4_CH4 | | I2C2_SCL | SPI1_MOSI / I2S1_SD | | USART3_RTS |
| PF7 | | EVENTOUT | | | I2C2_SDA | | | USART2_CK |
| PF9 | | EVENTOUT | TIM14_CH1 | | | | | |
| PF10 | | EVENTOUT | | | | | | |

# 5 Memory mapping

**Figure 6.** **STM32F37x memory map**
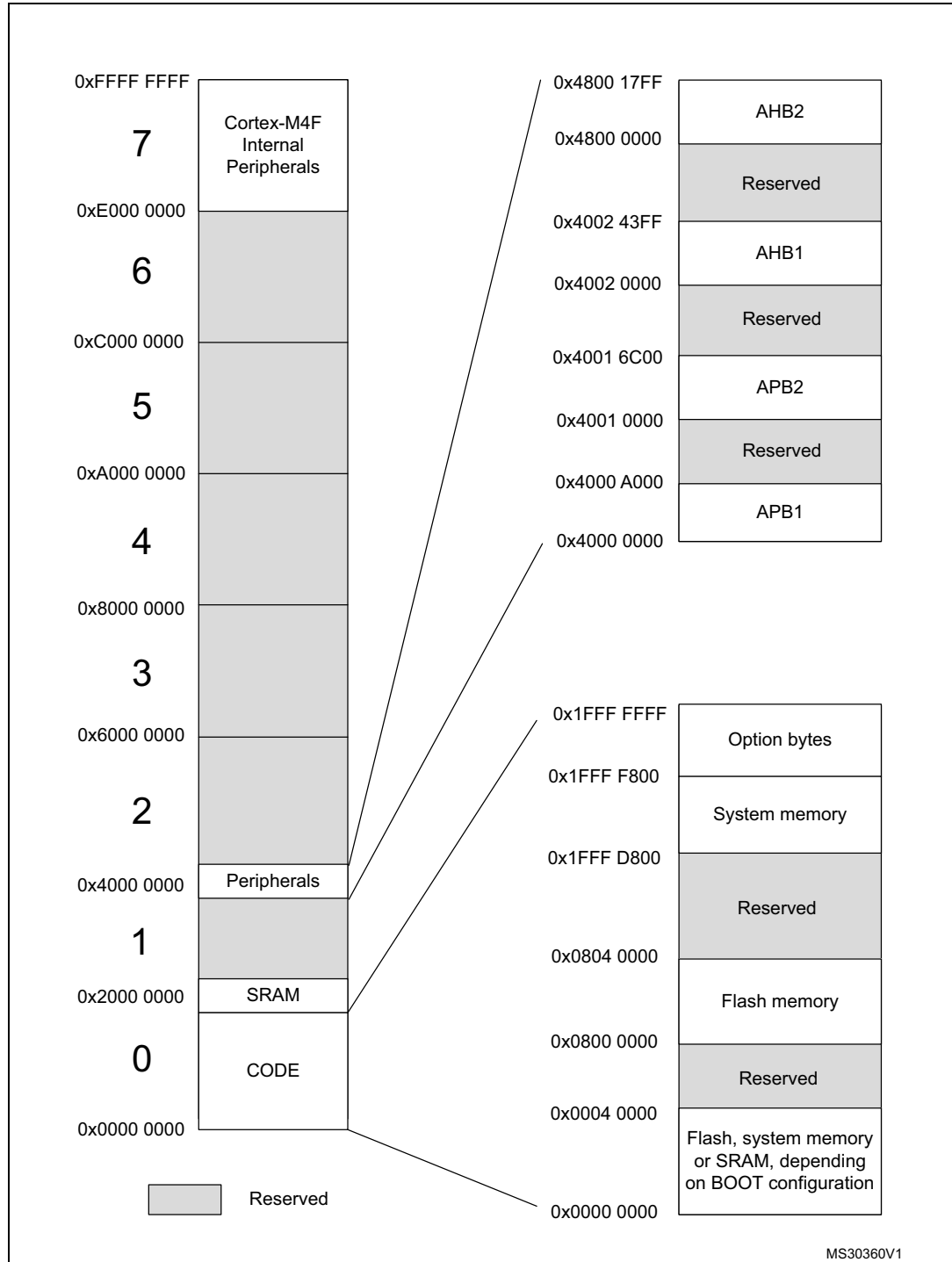
**Table 20.    STM32F37x peripheral register boundary addresses**

| Bus | Boundary address | Size | Peripheral |
|---|---|---|---|
| AHB2 | 0x4800 1400 - 0x4800 17FF | 1KB | GPIOF |
| | 0x4800 1000 - 0x4800 13FF | 1KB | GPIOE |
| | 0x4800 0C00 - 0x4800 0FFF | 1KB | GPIOD |
| | 0x4800 0800 - 0x4800 0BFF | 1KB | GPIOC |
| | 0x4800 0400 - 0x4800 07FF | 1KB | GPIOB |
| | 0x4800 0000 - 0x4800 03FF | 1KB | GPIOA |
| | 0x4002 4400 - 0x47FF FFFF | ~128 MB | Reserved |
| AHB1 | 0x4002 4000 - 0x4002 43FF | 1 KB | TSC |
| | 0x4002 3400 - 0x4002 3FFF | 3 KB | Reserved |
| | 0x4002 3000 - 0x4002 33FF | 1 KB | CRC |
| | 0x4002 2400 - 0x4002 2FFF | 3 KB | Reserved |
| | 0x4002 2000 - 0x4002 23FF | 1 KB | FLASH memory interface |
| | 0x4002 1400 - 0x4002 1FFF | 3 KB | Reserved |
| | 0x4002 1000 - 0x4002 13FF | 1 KB | RCC |
| | 0x4002 0800- 0x4002 0FFF | 2 KB | Reserved |
| | 0x4002 0400 - 0x4002 07FF | 1 KB | DMA2 |
| | 0x4002 0000 - 0x4002 03FF | 1 KB | DMA1 |
| | 0x4001 6C00 - 0x4001 FFFF | 37 KB | Reserved |

**Table 20.  STM32F37x peripheral register boundary addresses (continued)**

| Bus | Boundary address | Size | Peripheral |
|---|---|---|---|
| APB2 | 0x4001 6800 - 0x4001 6BFF | 1 KB | SDADC3 |
| | 0x4001 6400 - 0x4001 67FF | 1 KB | SDADC2 |
| | 0x4001 6000 - 0x4001 63FF | 1 KB | SDADC1 |
| | 0x4001 5C00 - 0x4001 5FFF | 1 KB | TIM19 |
| | 0x4001 4C00 - 0x4001 5BFF | 4 KB | Reserved |
| | 0x4001 4800 - 0x4001 4BFF | 1 KB | TIM17 |
| | 0x4001 4400 - 0x4001 47FF | 1 KB | TIM16 |
| | 0x4001 4000 - 0x4001 43FF | 1 KB | TIM15 |
| | 0x4001 3C00 - 0x4001 3FFF | 1 KB | Reserved |
| | 0x4001 3800 - 0x4001 3BFF | 1 KB | USART1 |
| | 0x4001 3400 - 0x4001 37FF | 1 KB | Reserved |
| | 0x4001 3000 - 0x4001 33FF | 1 KB | SPI1/I2S1 |
| | 0x4001 2800 - 0x4001 2FFF | 1 KB | Reserved |
| | 0x4001 2400 - 0x4001 27FF | 1 KB | ADC |
| | 0x4001 0800 - 0x4001 23FF | 7 KB | Reserved |
| | 0x4001 0400 - 0x4001 07FF | 1 KB | EXTI |
| | 0x4001 0000 - 0x4001 03FF | 1 KB | SYSCFG |
| | 0x4000 4000 - 0x4000 FFFF | 24 KB | Reserved |
| APB1 | 0x4000 9C00 – 0x4000 9FFF | 1 KB | TIM18 |
| | 0x4000 9800 - 0x4000 9BFF | 1 KB | DAC2 |
| | 0x4000 7C00 - 0x4000 97FF | 8 KB | Reserved |
| | 0x4000 7800 - 0x4000 7BFF | 1 KB | CEC |
| | 0x4000 7400 - 0x4000 77FF | 1 KB | DAC1 |
| | 0x4000 7000 - 0x4000 73FF | 1 KB | PWR |
| | 0x4000 6800 - 0x4000 6FFF | 2 KB | Reserved |
| | 0x4000 6400 - 0x4000 67FF | 1 KB | CAN |
| | 0x4000 6000 - 0x4000 63FF | 1 KB | USB packet SRAM |
| | 0x4000 5C00 - 0x4000 5FFF | 1 KB | USB FS |

**Table 20.    STM32F37x peripheral register boundary addresses (continued)**

| Bus | Boundary address | Size | Peripheral |
|---|---|---|---|
| APB1 | 0x4000 5800 - 0x4000 5BFF | 1 KB | I2C2 |
| | 0x4000 5400 - 0x4000 57FF | 1 KB | I2C1 |
| | 0x4000 4C00 - 0x4000 53FF | 2 KB | Reserved |
| | 0x4000 4800 - 0x4000 4BFF | 1 KB | USART3 |
| | 0x4000 4400 - 0x4000 47FF | 1 KB | USART2 |
| | 0x4000 4000 - 0x4000 43FF | 1 KB | Reserved |
| | 0x4000 3C00 - 0x4000 3FFF | 1 KB | SPI3/I2S3 |
| | 0x4000 3800 - 0x4000 3BFF | 1 KB | SPI2/I2S2 |
| | 0x4000 3400 - 0x4000 37FF | 1 KB | Reserved |
| | 0x4000 3000 - 0x4000 33FF | 1 KB | IWWDG |
| | 0x4000 2C00 - 0x4000 2FFF | 1 KB | WWDG |
| | 0x4000 2800 - 0x4000 2BFF | 1 KB | RTC |
| | 0x4000 2400 - 0x4000 27FF | 1 KB | Reserved |
| | 0x4000 2000 - 0x4000 23FF | 1 KB | TIM14 |
| | 0x4000 1C00 - 0x4000 1FFF | 1 KB | TIM13 |
| | 0x4000 1800 - 0x4000 1BFF | 1 KB | TIM12 |
| | 0x4000 1400 - 0x4000 17FF | 1 KB | TIM7 |
| | 0x4000 1000 - 0x4000 13FF | 1 KB | TIM6 |
| | 0x4000 0C00 - 0x4000 0FFF | 1 KB | TIM5 |
| | 0x4000 0800 - 0x4000 0BFF | 1 KB | TIM4 |
| | 0x4000 0400 - 0x4000 07FF | 1 KB | TIM3 |
| | 0x4000 0000 - 0x4000 03FF | 1 KB | TIM2 |

# 6 Electrical characteristics

## 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to $V_{SS}$.

### 6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25$ °C and $T_A = T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3$\Sigma$).

### 6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25$ °C, $V_{DD} = V_{DDA} = $ VDDSDx $= 3.3$ V. They are given only as design guidelines and are not tested.

Typical ADC and SDADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2$\Sigma$).

### 6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 7*.

### 6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 8*.

**Figure 7.    Pin loading conditions**          **Figure 8.    Pin input voltage**
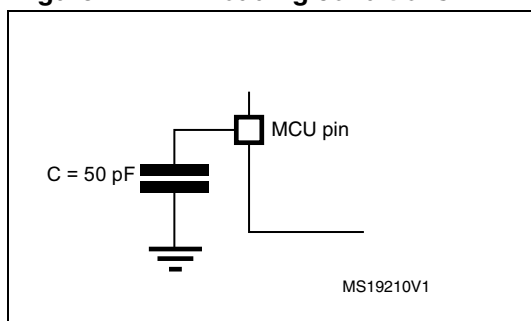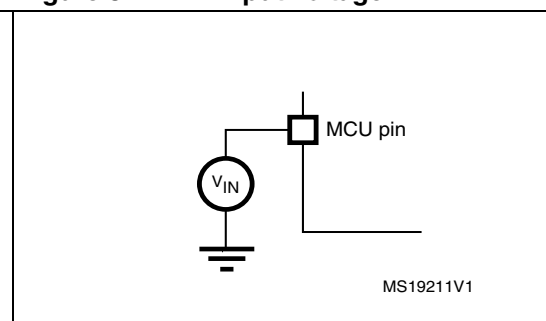
### 6.1.6 Power supply scheme

**Figure 9.    Power supply scheme**
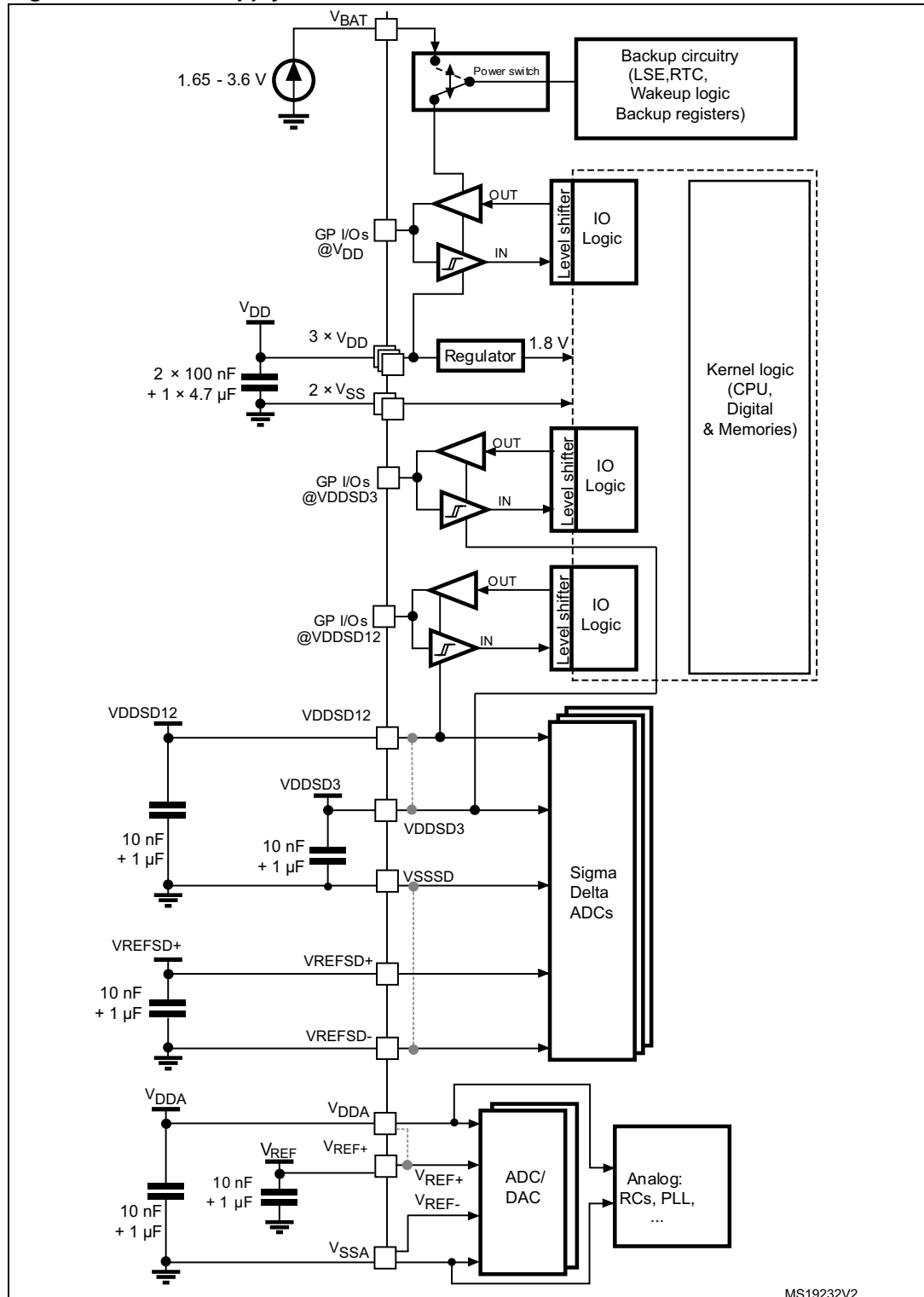


1. Dotted lines represent the internal connections on low pin count packages, joining the dedicated supply pins

**Caution:** Each power supply pair ($V_{DD}/V_{SS}$, $V_{DDA}/V_{SSA}$ etc..) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

### 6.1.7 Current consumption measurement

**Figure 10. Current consumption measurement scheme**
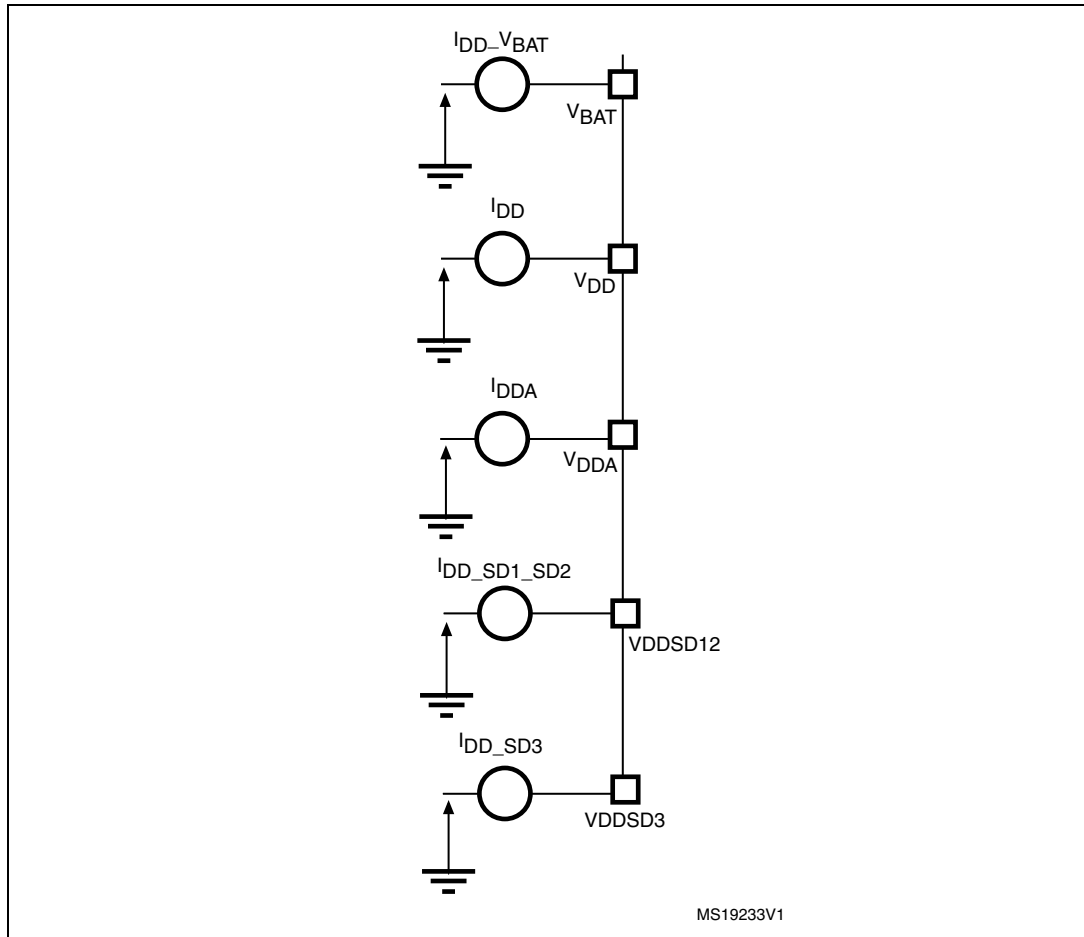
## 6.2      Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 21: Voltage characteristics*, *Table 22: Current characteristics*, and *Table 23: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 21.      Voltage characteristics[1]**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$–$V_{SS}$ | External main supply voltage (including $V_{DDA}$, VDDSDx, $V_{BAT}$ and $V_{DD}$) | − 0.3 | 4.0 | V |
| $V_{DD}$–$V_{DDA}$ | Allowed voltage difference for $V_{DD}$ > $V_{DDA}$ | | 0.4 | |
| VDDSDx − $V_{DDA}$ | Allowed voltage difference for VDDSDx > $V_{DDA}$ | | 0.4 | |
| VREFSD+ − VDDSD3 | Allowed voltage difference for VREFSD+ > VDDSD3 | | 0.4 | |
| $V_{REF+}$ − $V_{DDA}$ | Allowed voltage difference for $V_{REF+}$ > $V_{DDA}$ | | 0.4 | |
| $V_{IN}$[2] | Input voltage on FT and FTf pins | $V_{SS}$ − 0.3 | $V_{DD}$ + 4.0 | |
| | Input voltage on TTa pins | $V_{SS}$ − 0.3 | 4.0 | |
| | Input voltage on TC pins on SDADCx channels inputs[3] | $V_{SS}$ − 0.3 | 4.0 | |
| | Input voltage on any other pin | $V_{SS}$ − 0.3 | 4.0 | |
| $|V_{SSX}$ − $V_{SS}|$ | Variations between all the different ground pins | | 50 | mV |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see *Section 6.3.11: Electrical sensitivity characteristics* | | |

1.    All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.

2.    $V_{IN}$ maximum must always be respected. Refer to *Table 22: Current characteristics* for the maximum allowed injected current values.

3.    VDDSD12 is external power supply for PB2, PB10, and PE7 to PE15 I/O pins (I/O pin ground is internally connected to $V_{SS}$). VDDSD3 is external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (I/O pin ground is internally connected to $V_{SS}$)

All main power ($V_{DD}$, VDDSD12, VDDSD3 and $V_{DDA}$) and ground ($V_{SS}$, VSSSD, and $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.

The following relationship must be respected between $V_{DDA}$ and $V_{DD}$: $V_{DDA}$ must power on before or at the same time as $V_{DD}$ in the power up sequence. $V_{DDA}$ must be greater than or equal to $V_{DD}$.

The following relationship must be respected between $V_{DDA}$ and VDDSD12: $V_{DDA}$ must power on before or at the same time as VDDSD12 or VDDSD3 in the power up sequence. $V_{DDA}$ must be greater than or equal to VDDSD12 or VDDSD3.

The following relationship must be respected between VDDSD12 and VDDSD3: VDDSD3 must power on before or at the same time as VDDSD12 in the power up sequence. After power up (VDDSD12 > Vrefint = 1.2V) VDDSD3 can be higher or lower than VDDSD12.

The following relationship must be respected between VREFSD+ and VDDSD12, VDDSD3: VREFSD+ must be lower than VDDSD3.

Depending from the SDADCx operation mode, there can be more constrains between VREFSD+, VDDSD12 and VDDSD3 which are described in reference manual RM0313.

**Table 22. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $I_{VDD}$ | Total current into $V_{DD}$ and VDDSDx power lines (source)[1] | 100 | mA |
| $I_{VSS}$ | Total current out of $V_{SS}$ and VSSSD ground lines (sink)[1] | 100 | |
| $I_{IO(PIN)}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current source by any I/O and control pin | − 25 | |
| $\Sigma I_{IO(PIN)}$ | Total output current sunk by sum of all IOs and control pins | 75 | |
| | Total output current sourced by sum of all IOs and control pins | 75 | |
| $I_{INJ(PIN)}$ | Injected current on FT, FTf and B pins[2] | -5/+0 | |
| | Injected current on TC and RST pin[3] | ± 5 | |
| | Injected current on TTa pins[4] | ± 5 | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins)[5] | ± 25 | |

1. All main power ($V_{DD}$, VDDSD12, VDDSD3 and $V_{DDA}$) and ground ($V_{SS}$, VSSSD and $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.

2. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.

3. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 21: Voltage characteristics* for the maximum allowed input voltage values.

4. A positive injection is induced by $V_{IN}>V_{DDA}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ}$(PIN) must never be exceeded. Refer also to *Table 21: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note [2] below *Table 68*.

5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 23. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 150 | °C |

# 6.3 Operating conditions

## 6.3.1 General operating conditions

**Table 24. General operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | | 0 | 72 | MHz |
| $f_{PCLK1}$ | Internal APB1 clock frequency | | 0 | 36 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | | 0 | 72 | |
| $V_{DD}$ | Standard operating voltage | | 2 | 3.6 | V |
| $V_{DDA}$[1] | Analog operating voltage (ADC and DAC used) | Must have a potential equal to or higher than $V_{DD}$ | 2.4 | 3.6 | V |
| | Analog operating voltage (ADC and DAC not used) | | 2 | 3.6 | |
| VDDSD12 | VDDSD12 operating voltage (SDADC used) | | 2.2 | 3.6 | V |
| | VDDSD12 operating voltage (SDADC not used) | | 2.0 | 3.6 | |
| VDDSD3 | VDDSD3 operating voltage (SDADC used) | | 2.2 | 3.6 | V |
| | VDDSD3 operating voltage (SDADC not used) | | 2.0 | 3.6 | |
| $V_{BAT}$ | Backup operating voltage | | 1.65 | 3.6 | V |
| $P_D$ | Power dissipation at $T_A$ = 85 °C for suffix 6 or $T_A$ = 105 °C for suffix 7[2] | LQFP100 | | 434 | mW |
| | | LQFP64 | | 444 | |
| | | LQFP48 | | 364 | |
| | | BGA100 | | 338 | |
| $T_A$ | Ambient temperature for 6 suffix version | Maximum power dissipation | –40 | 85 | °C |
| | | Low power dissipation[3] | –40 | 105 | |
| | Ambient temperature for 7 suffix version | Maximum power dissipation | –40 | 105 | °C |
| | | Low power dissipation[3] | –40 | 125 | |
| $T_J$ | Junction temperature range | 6 suffix version | –40 | 105 | °C |
| | | 7 suffix version | –40 | 125 | |

1. When the ADC is used, refer to *Table 59: ADC characteristics*.

2. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_{Jmax}$ (see *Table 23: Thermal characteristics*).

3. In low power dissipation state, $T_A$ can be extended to this range as long as $T_J$ does not exceed $T_{Jmax}$ (see *Table 23: Thermal characteristics*).

### 6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 25* are derived from tests performed under the ambient temperature condition summarized in *Table 24*.

**Table 25.    Operating conditions at power-up / power-down**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------|-----------|------------|-----|-----|------|
| $t_{VDD}$ | $V_{DD}$ rise time rate | | 0 | ∞ | μs/V |
| | $V_{DD}$ fall time rate | | 20 | ∞ | |
| $t_{VDDA}$ | $V_{DDA}$ rise time rate | | 0 | ∞ | |
| | $V_{DDA}$ fall time rate | | 20 | ∞ | |

### 6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 26* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 24*.

**Table 26.    Embedded reset and power control block characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $V_{POR/PDR}$[1] | Power on/power down reset threshold | Falling edge | 1.8[2] | 1.88 | 1.96 | V |
| | | Rising edge | 1.84 | 1.92 | 2.0 | V |
| $V_{PDRhyst}$[3] | PDR hysteresis | | | 40 | | mV |
| $t_{RSTTEMPO}$[3] | Reset temporization | | 1.5 | 2.5 | 4.5 | ms |

1.  The PDR detector monitors $V_{DD}$, $V_{DDA}$ and VDDSD12 (if kept enabled in the option bytes). The POR detector monitors only $V_{DD}$.

2.  The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.

3.  Guaranteed by design, not tested in production.

**Table 27.    Programmable voltage detector characteristics**

| Symbol | Parameter | Conditions | Min[1] | Typ | Max[1] | Unit |
|--------|-----------|------------|--------|-----|--------|------|
| $V_{PVD0}$ | PVD threshold 0 | Rising edge | 2.1 | 2.18 | 2.26 | V |
| | | Falling edge | 2 | 2.08 | 2.16 | V |
| $V_{PVD1}$ | PVD threshold 1 | Rising edge | 2.19 | 2.28 | 2.37 | V |
| | | Falling edge | 2.09 | 2.18 | 2.27 | V |
| $V_{PVD2}$ | PVD threshold 2 | Rising edge | 2.28 | 2.38 | 2.48 | V |
| | | Falling edge | 2.18 | 2.28 | 2.38 | V |
| $V_{PVD3}$ | PVD threshold 3 | Rising edge | 2.38 | 2.48 | 2.58 | V |
| | | Falling edge | 2.28 | 2.38 | 2.48 | V |
| $V_{PVD4}$ | PVD threshold 4 | Rising edge | 2.47 | 2.58 | 2.69 | V |
| | | Falling edge | 2.37 | 2.48 | 2.59 | V |

**Table 27.    Programmable voltage detector characteristics (continued)**

| Symbol | Parameter | Conditions | Min[1] | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD5}$ | PVD threshold 5 | Rising edge | 2.57 | 2.68 | 2.79 | V |
| | | Falling edge | 2.47 | 2.58 | 2.69 | V |
| $V_{PVD6}$ | PVD threshold 6 | Rising edge | 2.66 | 2.78 | 2.9 | V |
| | | Falling edge | 2.56 | 2.68 | 2.8 | V |
| $V_{PVD7}$ | PVD threshold 7 | Rising edge | 2.76 | 2.88 | 3 | V |
| | | Falling edge | 2.66 | 2.78 | 2.9 | V |
| $V_{PVDhyst}$[2] | PVD hysteresis | | | 100 | | mV |
| IDD(PVD)[2] | PVD current consumption | | | 0.15 | 0.26 | µA |

1.  Data based on characterization results only, not tested in production.

2.  Guaranteed by design, not tested in production.

## 6.3.4    Embedded reference voltage

The parameters given in *Table 28* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 24*.

**Table 28.    Embedded internal reference voltage**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | −40 °C < $T_A$ < +105 °C | 1.16 | 1.21 | 1.26 | V |
| | | −40 °C < $T_A$ < +85 °C | 1.16 | 1.2 | 1.24[1] | |
| $T_{S\_vrefint}$[2] | ADC sampling time when reading the internal reference voltage | | 17.1 | - | - | µs |
| $V_{REFINT\_s}$[3] | Internal reference voltage spread over the temperature range | $V_{DD}$ = 3 V ±10 mV | - | | 10 | mV |
| $T_{Coeff}$[3] | Temperature coefficient | | - | | 100 | ppm/°C |
| $t_{START}$[3] | Startup time | | - | | 10 | µs |

1.  Data based on characterization results, not tested in production.

2.  Shortest sampling time can be determined in the application by multiple iterations.

3.  Guaranteed by design, not tested in production.

### 6.3.5    Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 10: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

#### Typical and maximum current consumption

The MCU is placed under the following conditions:

●    All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)

●    All peripherals are disabled except when explicitly mentioned

●    The Flash memory access time is adjusted to the $f_{HCLK}$ frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz)

●    Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)

●    When the peripherals are enabled $f_{APB1} = f_{AHB}/2$ , $f_{APB2} = f_{AHB}$

The parameters given in *Table 29* to *Table 35* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24*.

**Table 29.    Typical and maximum current consumption from $V_{DD}$ supply at $V_{DD}$ = 3.6 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | All peripherals enabled | | | | All peripherals disabled | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Max @ $T_A$[1] | | | Typ | Max @ $T_A$[1] | | | |
| | | | | | 25 °C | 85 °C | 105 °C | | 25 °C | 85 °C | 105 °C | |
| $I_{DD}$ | Supply current in Run mode, code executing from Flash | External clock (HSE bypass) | 72 MHz | 63.1 | 70.7 | 71.5 | 73.4 | 29.2 | 31.1 | 31.7 | 34.2 | mA |
| | | | 64 MHz | 56.3 | 63.3 | 64.1 | 64.9 | 26.1 | 27.8 | 28.4 | 30.4 | |
| | | | 48 MHz | 42.5 | 48.5 | 48.0 | 50.1 | 19.9 | 22.6 | 21.9 | 23.1 | |
| | | | 32 MHz | 28.8 | 31.4 | 32.2 | 34.3 | 13.1 | 16.1 | 14.9 | 16.2 | |
| | | | 24 MHz | 21.9 | 24.4 | 24.4 | 25.8 | 10.1 | 10.9 | 11.9 | 12.4 | |
| | | | 8 MHz | 7.3 | 8.0 | 9.3 | 9.3 | 3.7 | 4.1 | 4.4 | 5.0 | |
| | | | 1 MHz | 1.1 | 1.5 | 1.8 | 2.3 | 0.8 | 1.1 | 1.4 | 1.9 | |
| | | Internal clock (HSI) | 64 MHz | 51.7 | 57.7 | 58.0 | 60.4 | 25.8 | 27.6 | 28.1 | 30.1 | |
| | | | 48 MHz | 38.6 | 45.9 | 43.5 | 46.9 | 19.8 | 21.9 | 21.7 | 22.8 | |
| | | | 32 MHz | 26.4 | 31.1 | 29.7 | 31.9 | 13.1 | 15.7 | 14.8 | 16.2 | |
| | | | 24 MHz | 20.3 | 22.6 | 22.6 | 23.7 | 6.9 | 7.5 | 8.1 | 8.8 | |
| | | | 8 MHz | 7.0 | 7.6 | 8.8 | 8.8 | 3.7 | 4.1 | 4.4 | 5.0 | |

**Table 29. Typical and maximum current consumption from V_DD supply at V_DD = 3.6 V**

| Symbol | Parameter | Conditions | f_HCLK | All peripherals enabled | | | | All peripherals disabled | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Max @ T_A[1] | | | Typ | Max @ T_A[1] | | | |
| | | | | | 25 °C | 85 °C | 105 °C | | 25 °C | 85 °C | 105 °C | |
| I_DD | Supply current in Run mode, code executing from RAM | External clock (HSE bypass) | 72 MHz | 63.6 [2] | 70.7[2] | 75.7[2] | 72.3[2] | 30.0 [2] | 31.9[2] | 32.6[2] | 33.8[2] | mA |
| | | | 64 MHz | 56.7 | 62.5 | 67.1 | 64.0 | 26.7 | 28.6 | 29.3 | 30.0 | |
| | | | 48 MHz | 42.0 | 50.5 | 47.4 | 50.1 | 20.2 | 21.5 | 22.1 | 22.7 | |
| | | | 32 MHz | 28.3 | 32.1 | 31.8 | 33.7 | 13.4 | 14.6 | 14.8 | 15.7 | |
| | | | 24 MHz | 21.1 | 25.0 | 24.2 | 25.9 | 10.0 | 11.3 | 11.2 | 12.6 | |
| | | | 8 MHz | 6.9 | 7.4 | 8.3 | 8.7 | 3.4 | 3.7 | 4.1 | 4.8 | |
| | | | 1 MHz | 0.8 | 1.2 | 1.5 | 2.0 | 0.4 | 0.6 | 1.0 | 1.5 | |
| | | Internal clock (HSI) | 64 MHz | 51.9 | 59.5 | 59.4 | 58.6 | 26.4 | 28.1 | 28.7 | 29.5 | |
| | | | 48 MHz | 38.1 | 44.7 | 43.8 | 45.4 | 20.0 | 21.3 | 21.9 | 22.3 | |
| | | | 32 MHz | 25.9 | 31.2 | 29.4 | 30.5 | 13.2 | 14.3 | 14.6 | 15.5 | |
| | | | 24 MHz | 19.6 | 22.7 | 22.6 | 23.2 | 6.5 | 7.0 | 7.9 | 8.2 | |
| | | | 8 MHz | 6.6 | 7.1 | 8.0 | 8.4 | 3.3 | 3.7 | 4.0 | 4.7 | |
| | Supply current in Sleep mode, code executing from Flash or RAM | External clock (HSE bypass) | 72 MHz | 43.2 | 46.9 | 48.7 | 52.5 | 6.7 | 7.2 | 7.6 | 8.3 | |
| | | | 64 MHz | 38.5 | 41.6 | 43.7 | 46.6 | 5.9 | 6.5 | 6.8 | 7.5 | |
| | | | 48 MHz | 29.1 | 31.3 | 32.5 | 34.1 | 4.5 | 4.9 | 5.3 | 5.9 | |
| | | | 32 MHz | 19.4 | 21.1 | 24.6 | 23.0 | 3.0 | 3.4 | 3.8 | 4.4 | |
| | | | 24 MHz | 14.7 | 16.1 | 18.5 | 17.6 | 2.4 | 2.6 | 3.0 | 3.6 | |
| | | | 8 MHz | 4.9 | 5.3 | 6.1 | 6.6 | 0.8 | 1.0 | 1.4 | 1.9 | |
| | | | 1 MHz | 0.6 | 0.9 | 1.3 | 1.8 | 0.1 | 0.3 | 0.6 | 1.2 | |
| | | Internal clock (HSI) | 64 MHz | 34.5 | 37.1 | 39.6 | 42.0 | 5.6 | 6.1 | 6.5 | 7.1 | |
| | | | 48 MHz | 26.1 | 28.0 | 29.0 | 30.7 | 4.2 | 4.6 | 5.0 | 5.6 | |
| | | | 32 MHz | 17.4 | 19.1 | 21.1 | 20.8 | 2.9 | 3.2 | 3.6 | 4.2 | |
| | | | 24 MHz | 13.3 | 14.6 | 16.1 | 16.0 | 1.5 | 1.8 | 2.2 | 2.6 | |
| | | | 8 MHz | 4.5 | 4.9 | 5.5 | 6.1 | 0.7 | 0.9 | 1.3 | 1.8 | |

1. Data based on characterization results, not tested in production unless otherwise specified.

2. Data based on characterization results and tested in production with code executing from RAM.

**Table 30. Typical and maximum current consumption from V$_{DDA}$ supply**

| Symbol | Parameter | Conditions [1] | f$_{HCLK}$ | V$_{DDA}$= 2.4 V | | | | V$_{DDA}$= 3.6 V | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Max @ T$_A$[2] | | | Typ | Max @ T$_A$[2] | | | |
| | | | | | 25 °C | 85 °C | 105 °C | | 25 °C | 85 °C | 105 °C | |
| I$_{DDA}$ | Supply current in Run or Sleep mode, code executing from Flash or RAM | External clock (HSE bypass) | 72 MHz | 228 | 261 | 274 | 280 | 249 | 288 | 304 | 311 | µA |
| | | | 64 MHz | 201 | 235 | 247 | 251 | 220 | 257 | 269 | 275 | |
| | | | 48 MHz | 152 | 182 | 190 | 195 | 164 | 196 | 208 | 212 | |
| | | | 32 MHz | 104 | 132 | 137 | 141 | 112 | 141 | 147 | 150 | |
| | | | 24 MHz | 81 | 108 | 112 | 111 | 87 | 115 | 119 | 119 | |
| | | | 8 MHz | 2 | 4 | 4 | 5 | 3 | 5 | 5 | 6 | |
| | | | 1 MHz | 2 | 4 | 5 | 5 | 3 | 5 | 5 | 6 | |
| | | Internal clock (HSI) | 64 MHz | 270 | 307 | 320 | 326 | 298 | 337 | 353 | 361 | |
| | | | 48 MHz | 220 | 254 | 264 | 269 | 243 | 276 | 292 | 297 | |
| | | | 32 MHz | 172 | 203 | 211 | 214 | 191 | 222 | 232 | 235 | |
| | | | 24 MHz | 151 | 181 | 185 | 189 | 166 | 194 | 201 | 204 | |
| | | | 8 MHz | 70 | 85 | 87 | 87 | 81 | 93 | 96 | 98 | |

1. Current consumption from the V$_{DDA}$ supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I$_{DDA}$ is independent from the frequency.

2. Data based on characterization results, not tested in production unless otherwise specified.

**Table 31. Typical and maximum V$_{DD}$ consumption in Stop and Standby modes**

| Symbol | Parameter | Conditions | Typ@V$_{DD}$(V$_{DD}$=V$_{DDA}$) | | | | | | Max | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 2.0 V | 2.4 V | 2.7 V | 3.0 V | 3.3 V | 3.6 V | T$_A$= 25 °C | T$_A$= 85 °C | T$_A$= 105 °C | |
| I$_{DD}$ | Supply current in Stop mode | Regulators in run mode, all oscillators OFF | 20.1 | 20.4 | 20.7 | 20.4 | 19.9 | 20.1 | 46.5 | 480 | 1019 | µA |
| | | Regulators in low-power mode, all oscillators OFF | 8.3 | 8.3 | 8.5 | 8.5 | 8.4 | 8.0 | 31.8 | 451.4 | 966.0 | |
| | Supply current in Standby mode | LSI ON and IWDG ON | 1.44 | 1.55 | 2.1 | 1.83 | 1.6 | 1.56 | | | | |
| | | LSI OFF and IWDG OFF | 1.22 | 1.4 | 1.76 | 1.52 | 1.17 | 1.34 | 2.7 | 3.5 | 5.3 | |

Note: V$_{DDA}$ monitoring is OFF and VDDSD12 monitoring is OFF

**Table 32.     Typical and maximum V$_{DDA}$ consumption in Stop and Standby modes**

| Symbol | Parameter | Conditions | | Typ@V$_{DD}$(V$_{DD}$=V$_{DDA}$) | | | | | | Max[1] | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 2.0 V | 2.4 V | 2.7 V | 3.0 V | 3.3 V | 3.6 V | T$_A$= 25 °C | T$_A$= 85 °C | T$_A$= 105 °C | |
| I$_{DDA}$ | Supply current in Stop mode | V$_{DDA}$ and VDDSD12 monitoring ON[2] | Regulator in run mode, all oscillators OFF | 1.99 | 2.07 | 2.19 | 2.33 | 2.46 | 2.64 | 10.8 | 11.8 | 12.4 | μA |
| | | | Regulator in low-power mode, all oscillators OFF | 1.99 | 2.07 | 2.18 | 2.32 | 2.47 | 2.63 | 10.6 | 11.5 | 12.5 | |
| | Supply current in Standby mode | | LSI ON and IWDG ON | 2.44 | 2.53 | 2.7 | 2.89 | 3.09 | 3.33 | | | | |
| | | | LSI OFF and IWDG OFF | 1.87 | 1.94 | 2.06 | 2.19 | 2.35 | 2.51 | 4.1 | 4.5 | 4.8 | |
| IDDAmon | Supply current for VDDA and VDDSD12 monitoring | - | | 0.95 | 1.02 | 1.12 | 1.2 | 1.27 | 1.4 | | | | |

1. Data based on characterization results and tested in production.

2. To obtain data with monitoring OFF is necessary to substract the IDDAmon current.

**Table 33.     Typical and maximum current consumption from V$_{BAT}$ supply[1]**

| Symbol | Parameter | Conditions | Typ @ V$_{BAT}$ | | | | | | Max[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | = 1.65 V | = 1.8 V | = 2.4 V | = 2.7 V | = 3.3 V | = 3.6 V | T$_A$= 25 °C | T$_A$= 85 °C | T$_A$= 105 °C | |
| I$_{DD\_VBAT}$ | Backup domain supply current | LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00' | 0.44 | 0.47 | 0.59 | 0.65 | 0.8 | 0.9 | | | | μA |
| | | LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11' | 0.73 | 0.77 | 0.9 | 0.97 | 1.14 | 1.26 | | | | |

1. Crystal used: EPSON-TOYOCOM FC-135 with 6 pF of CL for typical values.

2. Data based on characterization results, not tested in production.

**Typical current consumption**

The MCU is placed under the following conditions:

● $V_{DD}$=$V_{DDA}$= VDDSD12 = VDDSD3 = 3.3 V
● All I/O pins are in analog input configuration
● The Flash access time is adjusted to $f_{HCLK}$ frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz)
● Prefetch is ON when the peripherals are enabled, otherwise it is OFF
● When the peripherals are enabled, $f_{APB1}$ = $f_{AHB/2}$, $f_{APB2}$ = $f_{AHB}$
● PLL is used for frequencies greater than 8 MHz
● AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively

**Table 34. Typical current consumption in Run mode, code with data processing running from Flash**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ | | Unit |
|---|---|---|---|---|---|---|
| | | | | Peripherals enabled | Peripherals disabled | |
| $I_{DD}$ | Supply current in Run mode from $V_{DD}$ supply | Running from HSE crystal clock 8 MHz, code executing from Flash | 72 MHz | 64 | 29.7 | mA |
| | | | 64 MHz | 57 | 26.6 | |
| | | | 48 MHz | 43.4 | 20.3 | |
| | | | 36 MHz | | | |
| | | | 32 MHz | 29.4 | 14 | |
| | | | 24 MHz | 22.4 | 10.74 | |
| | | | 16 MHz | | | |
| | | | 8 MHz | 8.01 | 3.97 | |
| | | | 4 MHz | | | |
| | | | 2 MHz | | | |
| | | | 1 MHz | 1.691 | 0.956 | |
| | | | 500 kHz | | | |
| $I_{DDA}$[1] | Supply current in Run mode from $V_{DDA}$ supply | | 72 MHz | 253.57 | 252.82 | µA |
| | | | 64 MHz | 223.48 | 222.55 | |
| | | | 48 MHz | 167.06 | 166.67 | |
| | | | 36 MHz | | | |
| | | | 32 MHz | 114.33 | 114.19 | |
| | | | 24 MHz | 88.44 | 88.36 | |
| | | | 16 MHz | | | |
| | | | 8 MHz | 1.28 | 1.27 | |
| | | | 4 MHz | | | |
| | | | 2 MHz | | | |
| | | | 1 MHz | 1.26 | 1.27 | |
| | | | 500 kHz | | | |
| ISDADC12 + ISDADC3 | Supply currents in Run mode from VDDSD12 and VDDSD3 (SDADCs are off) | | - | 2.5 | 1 | |

1. $V_{DDA}$ monitoring is off, VDDSD12 monitoring is off

**Table 35.    Typical current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | f$_{HCLK}$ | Typ | | Unit |
|---|---|---|---|---|---|---|
| | | | | Peripherals enabled | Peripherals disabled | |
| I$_{DD}$ | Supply current in Sleep mode from V$_{DD}$ supply | Running from HSE crystal clock 8 MHz, code executing from Flash or RAM | 72 MHz | 44.98 | 6.93 | mA |
| | | | 64 MHz | 40.08 | 6.13 | |
| | | | 48 MHz | 30 | 4.7 | |
| | | | 32 MHz | 20.2 | 3.21 | |
| | | | 24 MHz | 15.3 | 2.48 | |
| | | | 16 MHz | | | |
| | | | 8 MHz | 5.33 | 0.901 | |
| | | | 4 MHz | | | |
| | | | 2 MHz | | | |
| | | | 1 MHz | 0.993 | 0.264 | |
| | | | 500 kHz | | | |
| | | | 125 kHz | | | |
| I$_{DDA}$[1] | Supply current in Sleep mode from V$_{DDA}$ supply | | 72 MHz | 253.57 | 252.82 | µA |
| | | | 64 MHz | 223.48 | 222.55 | |
| | | | 48 MHz | 167.06 | 166.67 | |
| | | | 36 MHz | | | |
| | | | 32 MHz | 114.33 | 114.19 | |
| | | | 24 MHz | 88.44 | 88.36 | |
| | | | 16 MHz | | | |
| | | | 8 MHz | 1.28 | 1.27 | |
| | | | 4 MHz | | | |
| | | | 2 MHz | | | |
| | | | 1 MHz | 1.26 | 1.27 | |
| | | | 500 kHz | | | |
| | | | 125 kHz | | | |

1.  V$_{DDA}$ monitoring is off, VDDSD12 monitoring is off

### I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

**I/O static current consumption**

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 51: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC and SDADC input pins which should be configured as analog inputs.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode. Under reset conditions all I/Os are configured in input floating mode - so if some inputs do not have a defined voltage level then they can generate additional consumption. This consumption is visible on $V_{DD}$ supply and also on VDDSDx supply because some I/Os are powered from SDADCx supply (all I/Os which have SDADC analog input functionality).

**I/O dynamic current consumption**

In addition to the internal peripheral current consumption measured previously, the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} \ = \ V_{DD} \times f_{SW} \times C$$

where

$I_{SW}$ is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DD}$ is the MCU supply voltage

$f_{SW}$ is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

### On-chip peripheral current consumption

The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and $V_{DD}$ supply voltage conditions summarized in *Table 21*

## 6.3.6 External clock source characteristics

### High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 11*.

**Table 36.    High-speed external user clock characteristics**

| Symbol | Parameter[1] | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE\_ext}$ | User external clock source frequency | | 1 | 8 | 32 | MHz |
| $V_{HSEH}$ | OSC_IN input pin high level voltage | | $0.7V_{DD}$ | | $V_{DD}$ | V |
| $V_{HSEL}$ | OSC_IN input pin low level voltage | | $V_{SS}$ | | $0.3V_{DD}$ | |
| $t_{w(HSEH)}$ $t_{w(HSEL)}$ | OSC_IN high or low time | | 15 | | | ns |
| $t_{r(HSE)}$ $t_{f(HSE)}$ | OSC_IN rise or fall time | | | | 20 | |

1. Guaranteed by design, not tested in production.

**Figure 11. High-speed external clock source AC timing diagram**
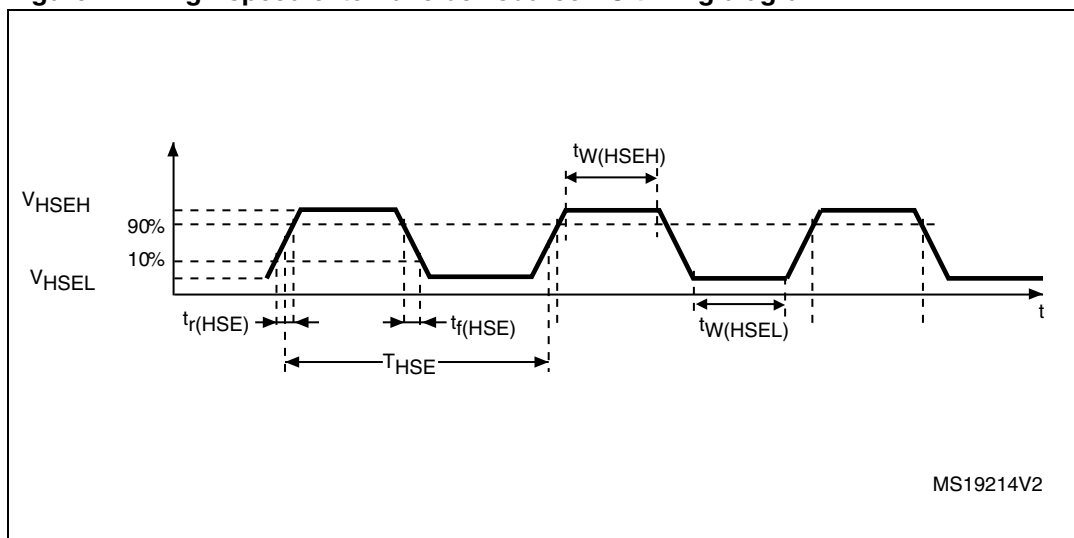


**Low-speed external user clock generated from an external source**

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 12*.

**Table 37. Low-speed external user clock characteristics**

| Symbol | Parameter[1] | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE\_ext}$ | User External clock source frequency | | | 32.768 | 1000 | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | | $0.7V_{DD}$ | | $V_{DD}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low level voltage | | $V_{SS}$ | | $0.3V_{DD}$ | |
| $t_{w(LSEH)}$ $t_{w(LSEL)}$ | OSC32_IN high or low time | | 450 | | | ns |
| $t_{r(LSE)}$ $t_{f(LSE)}$ | OSC32_IN rise or fall time | | | | 50 | |

1. Guaranteed by design, not tested in production.

**Figure 12.  Low-speed external clock source AC timing diagram**
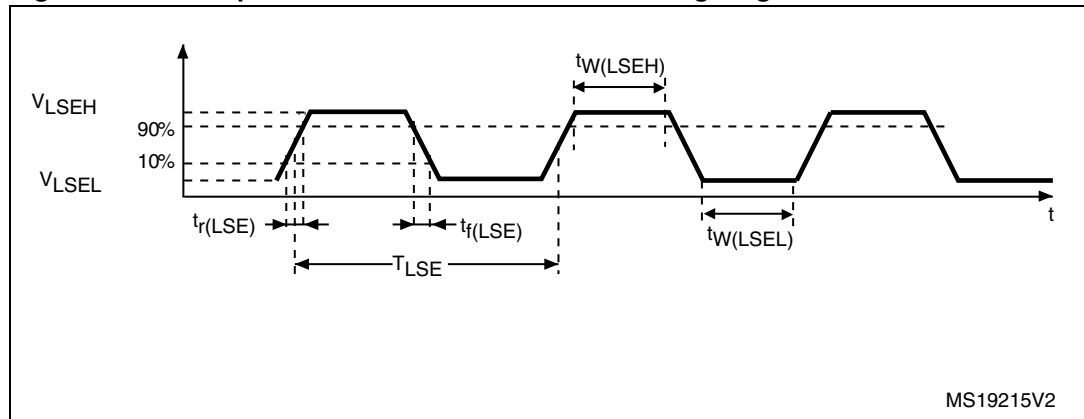


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### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 38*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 38.  HSE oscillator characteristics**

| Symbol | Parameter | Conditions[1] | Min[2] | Typ | Max[2] | Unit |
|--------|-----------|---------------|--------|-----|--------|------|
| $f_{OSC\_IN}$ | Oscillator frequency | | 4 | 8 | 32 | MHz |
| $R_F$ | Feedback resistor | | | 200 | | k$\Omega$ |
| $I_{DD}$ | HSE current consumption | During startup[3] | | | 8.5 | mA |
| | | $V_{DD}$=3.3 V, Rm= 30$\Omega$, CL=10 pF@8 MHz | | 0.4 | | |
| | | $V_{DD}$=3.3 V, Rm= 45$\Omega$, CL=10 pF@8 MHz | | 0.5 | | |
| | | $V_{DD}$=3.3 V, Rm= 30$\Omega$, CL=5 pF@32 MHz | | 0.8 | | |
| | | $V_{DD}$=3.3 V, Rm= 30$\Omega$, CL=10 pF@32 MHz | | 1 | | |
| | | $V_{DD}$=3.3 V, Rm= 30$\Omega$, CL=20 pF@32 MHz | | 1.5 | | |
| $g_m$ | Oscillator transconductance | Startup | 10 | | | mA/V |
| $t_{SU(HSE)}$[4] | Startup time | $V_{DD}$ is stabilized | | 2 | | ms |

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.

2. Guaranteed by design, not tested in production.

3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time

4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 13*). $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing $C_{L1}$ and $C_{L2}$.

*Note:* *For information on electing the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

**Figure 13.   Typical application with an 8 MHz crystal**
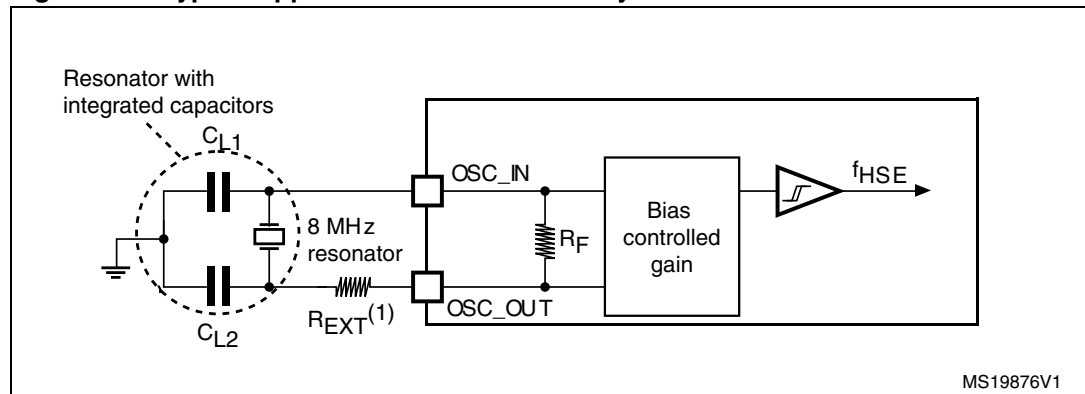


1. $R_{EXT}$ value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 39*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 39.  LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz)**

| Symbol | Parameter | Conditions[1] | Min[2] | Typ | Max[2] | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | LSE current consumption | LSEDRV[1:0]=00 lower driving capability | | 0.5 | 0.9 | µA |
| | | LSEDRV[1:0]= 01 medium low driving capability | | | 1 | |
| | | LSEDRV[1:0] = 10 medium high driving capability | | | 1.3 | |
| | | LSEDRV[1:0]=11 higher driving capability | | | 1.6 | |
| $g_m$ | Oscillator transconductance | LSEDRV[1:0]=00 lower driving capability | 5 | | | µA/V |
| | | LSEDRV[1:0]= 01 medium low driving capability | 8 | | | |
| | | LSEDRV[1:0] = 10 medium high driving capability | 15 | | | |
| | | LSEDRV[1:0]=11 higher driving capability | 25 | | | |
| $t_{SU(LSE)}$[3] | Startup time | $V_{DD}$ is stabilized | | 2 | | s |

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".

2. Guaranteed by design, not tested in production.

3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

*Note:*      *For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

**Figure 14. Typical application with a 32.768 kHz crystal**
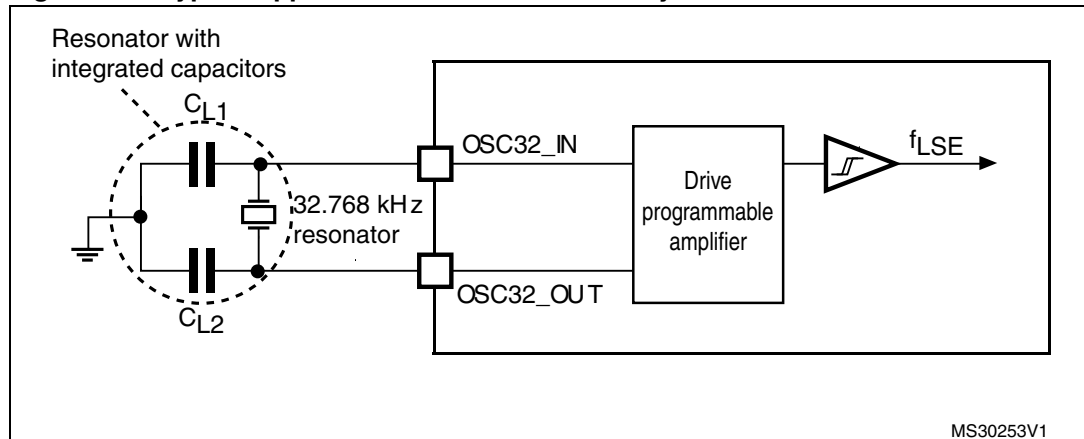


*Note:* *An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.*

### 6.3.7 Internal clock source characteristics

The parameters given in *Table 40* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24*.

**High-speed internal (HSI) RC oscillator**

**Table 40. HSI oscillator characteristics[1]**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $f_{HSI}$ | Frequency | | | 8 | | MHz |
| TRIM | HSI user trimming step | | | | 1[2] | % |
| $DuCy_{(HSI)}$ | Duty cycle | | 45[2] | | 55[2] | % |
| $ACC_{HSI}$ | Accuracy of the HSI oscillator (factory calibrated) | $T_A$ = −40 to 105 °C | −3.8[3] | | 4.6[3] | % |
| | | $T_A$ = −10 to 85 °C | 2.9[3] | | 2.9[3] | % |
| | | $T_A$ = 0 to 70 °C | −1.3[3] | | 2.2[3] | % |
| | | $T_A$ = 25 °C | −1 | | 1 | % |
| $t_{su(HSI)}$ | HSI oscillator startup time | | 1[3] | | 2[3] | µs |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | | | 80 | 100[3] | µA |

1. $V_{DDA}$ =3.3 V, $T_A$ = −40 to 105 °C unless otherwise specified.

2. Guaranteed by design, not tested in production.

3. Data based on characterization results, not tested in production.

### Low-speed internal (LSI) RC oscillator

**Table 41.    LSI oscillator characteristics[1]**

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|-----------|-----|-----|-----|------|
| $f_{LSI}$ | Frequency | 30 | 40 | 60 | kHz |
| $t_{su(LSI)}$[2] | LSI oscillator startup time | | | 85 | µs |
| $I_{DD(LSI)}$[2] | LSI oscillator power consumption | | 0.75 | 1.2 | µA |

1.  $V_{DDA}$ = 3.3 V, $T_A$ = –40 to 105 °C unless otherwise specified.

2.  Guaranteed by design, not tested in production.

### Wakeup time from low-power mode

The wakeup times given in *Table 42* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

● Stop or sleep mode: the wakeup event is WFE

● The wakeup pin used in stop and sleep mode is PA0 and in standby mode is the PA1.

All timings are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 24*.

**Table 42.    Low-power mode wakeup timings**

| Symbol | Parameter | Conditions | Typ @ $V_{DD}$ | | | | | Max | Unit |
|--------|-----------|------------|---------|---------|---------|--------|---------|-----|------|
| | | | = 2.0 V | = 2.4 V | = 2.7 V | = 3 V | = 3.3 V | | |
| $t_{WUSTOP}$ | Wakeup from Stop mode | Regulator in run mode | | | | | 4.1 | 4.5 | µs |
| | | Regulator in low power mode | | | | | 7.5 | 8.6 | |
| $t_{WUSTANDBY}$ | Wakeup from Standby mode | | 64 | 61 | 57 | 54 | 52 | 100 | |
| $t_{WUSLEEP}$ | Wakeup from Sleep mode | Fcpu = 8 MHz | 3.2 | 3.2 | 3.2 | 3.2 | 3.2 | | |

## 6.3.8    PLL characteristics

The parameters given in *Table 43* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24*.

**Table 43.    PLL characteristics**

| Symbol | Parameter | Value | | | Unit |
|--------|-----------|-------|-----|-----|------|
| | | Min | Typ | Max | |
| $f_{PLL\_IN}$ | PLL input clock[1] | 1[2] | | 24[2] | MHz |
| | PLL input clock duty cycle | 40[2] | | 60[2] | % |

**Table 43. PLL characteristics (continued)**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $f_{PLL\_OUT}$ | PLL multiplier output clock | 16[2] | | 72 | MHz |
| $t_{LOCK}$ | PLL lock time | | | 200[2] | µs |
| Jitter | Cycle-to-cycle jitter | | | 300[2] | ps |

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by $f_{PLL\_OUT}$.

2. Guaranteed by design, not tested in production.

## 6.3.9 Memory characteristics

**Flash memory**

The characteristics are given at $T_A$ = –40 to 105 °C unless otherwise specified.

**Table 44. Flash memory characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|
| $t_{prog}$ | 16-bit programming time | $T_A$ = –40 to +105 °C | 40 | 53.5 | 60 | µs |
| $t_{ERASE}$ | Page (1 KB) erase time | $T_A$ = –40 to +105 °C | 20 | | 40 | ms |
| $t_{ME}$ | Mass erase time | $T_A$ = –40 to +105 °C | 20 | | 40 | ms |
| $I_{DD}$ | Supply current | Write mode | | | 10 | mA |
| | | Erase mode | | | 12 | mA |

1. Guaranteed by design, not tested in production.

**Table 45. Flash memory endurance and data retention**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| | | | Min[1] | |
| $N_{END}$ | Endurance | $T_A$ = –40 to +85 °C (6 suffix versions)<br>$T_A$ = –40 to +105 °C (7 suffix versions) | 10 | kcycles |
| $t_{RET}$ | Data retention | 1 kcycle[2] at $T_A$ = 85 °C | 30 | Years |
| | | 1 kcycle[2] at $T_A$ = 105 °C | 10 | |
| | | 10 kcycles[2] at $T_A$ = 55 °C | 20 | |

1. Data based on characterization results, not tested in production.

2. Cycling performed over the whole temperature range.

### 6.3.10    EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

**Functional EMS (electromagnetic susceptibility)**

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

● **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.

● **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 46*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 46.    EMS characteristics**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25 °C, $f_{HCLK}$ = 72 MHz conforms to IEC 61000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25 °C, $f_{HCLK}$ = 72 MHz conforms to IEC 61000-4-4 | 4A |

**Designing hardened software to avoid noise problems**

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

**Software recommendations**

The software flowchart must include the management of runaway conditions such as:

● Corrupted program counter
● Unexpected reset
● Critical Data corruption (control registers...)

**Prequalification trials**

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

**Electromagnetic Interference (EMI)**

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 47. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [$f_{HSE}/f_{HCLK}$] 8/72 MHz | Unit |
|--------|-----------|------------|--------------------------|----------------------------------------|------|
| $S_{EMI}$ | Peak level | $V_{DD} = 3.3$ V, $T_A = 25$ °C, LQFP100 package compliant with IEC 61967-2 | 0.1 to 30 MHz | 9 | dBµV |
| | | | 30 to 130 MHz | 26 | |
| | | | 130 MHz to 1 GHz | 30 | |
| | | | SAE EMI Level | 4 | - |

## 6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

**Electrostatic discharge (ESD)**

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 48. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Class | Maximum value[1] | Unit |
|--------|---------|------------|-------|------------------|------|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A = +25$ °C, conforming to JESD22-A114 | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A = +25$ °C, conforming to JESD22-C101 | II | 500 | |

1. Data based on characterization results, not tested in production.

### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

● A supply overvoltage is applied to each power supply pin
● A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 49. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|--------|-----------|------------|-------|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | II level A |

## 6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 50*

**Table 50. I/O current injection susceptibility**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | **Negative injection** | **Positive injection** | |
| $I_{INJ}$ | Injected current on BOOT0 pin | -0 | NA | mA |
| | Injected current on other FT and FTf pins with current injection on adjacent pins < -5 µA | -5 | NA | |
| | Injected current on PC0 pin | -0 | +5 | |
| | Injected current on TC type I/O pins on VDDSD12 power domain: PB0, PB1, PB2, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB10 with current injection on other pins from this group limited to > -10 µA and < -50 µA | -5 | +5 | |
| | Injected current on TC type I/O pins on VDDSD3 power domain: PB14, PB15, PD8, PD9, PD10, PD12, PD13, PD14, PD15 with current injection on other pins from this group limited to > -10 µA and < -50 µA | -5 | +5 | |
| | Injected current on any other TC pins on $V_{DD}$ power domain: with current injection on adjacent pins < -5 µA | -5 | +5 | |
| | Injected current on TTa type pins: PA4, PA5, PA6 with current injection on adjacent pins > -5 µA and < -10 µA | -5 | +5 | |
| | Injected current on any other TTa pins with current injection on adjacent pins < -5 µA | -5 | +5 | |
| | Injected current on all other pins | -5 | +5 | |

*Note:* *It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*

### 6.3.13 I/O port characteristics

**General input/output characteristics**

Unless otherwise specified, the parameters given in *Table 51* are derived from tests performed under the conditions summarized in *Table 24*. All I/Os are CMOS and TTL compliant.

**Table 51. I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Standard I/O input low level voltage | | −0.3 | - | $0.3V_{DD}+0.07$ | V |
| | TTa I/O input low level voltage | | −0.3 | - | $0.3V_{DD}+0.07$ | |
| | FT and FTf[1] I/O input low level voltage | | −0.3 | - | $0.475V_{DD}-0.2$ | |
| | BOOT0 input low level voltage | | 0 | - | $0.3V_{DD}-0.3$ | |
| $V_{IH}$ | Standard I/O input high level voltage | | $0.445V_{DD}+0.398$ | - | $V_{DD}+0.3$ | |
| | TTa I/O input high level voltage | | $0.445V_{DD}+0.398$ | - | $V_{DD}+0.3$ | |
| | FT and FTf[1] I/O input high level voltage | | $0.5V_{DD}+0.2$ | - | 5.5 | |
| | BOOT0 input high level voltage | | $0.2V_{DD}+0.95$ | - | 5.5 | |
| $V_{hys}$ | Standard I/O Schmitt trigger voltage hysteresis[2] | | 200 | - | - | mV |
| | TTa I/O Schmitt trigger voltage hysteresis[2] | | 200 | - | - | |
| | FT and FTf I/O Schmitt trigger voltage hysteresis[2] | | 100 | - | - | |
| | BOOT0 input Schmitt trigger voltage hysteresis | | 300 | - | - | |

**Table 51. I/O static characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{lkg}$ | Input leakage current [3] | $V_{SS} \le V_{IN} \le V_{DD}$ I/O TC, FT and FTf | - | - | ±0.1 | μA |
| | | $V_{SS} \le V_{IN} \le V_{DD}$ $2\,V \le V_{DD} \le V_{DDA} \le 3.6\,V$ I/O TTa used in digital mode | - | - | ±0.1 | |
| | | $V_{IN} = 5\,V$ I/O FT and FTf | - | - | 10 | |
| | | $V_{IN} = 3.6\,V,$ $2\,V \le V_{DD} \le V_{IN}$ $V_{DDA} = 3.6\,V$ I/O TTa used in digital mode | - | - | 1 | |
| | | $V_{SS} \le V_{IN} \le V_{DDA}$ $2\,V \le V_{DD} \le V_{DDA} \le 3.6\,V$ I/O TTa used in analog mode | - | - | ±0.2 | |
| $R_{PU}$ | Weak pull-up equivalent resistor[4] | $V_{IN} = V_{SS}$ | 25 | 40 | 55 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistor[4] | $V_{IN} = V_{DD}$ | 25 | 40 | 55 | kΩ |
| $C_{IO}$ | I/O pin capacitance | | - | 5 | - | pF |

1. To sustain a voltage higher than $V_{DD}+0.3$ the internal pull-up/pull-down resistors must be disabled.

2. Hysteresis voltage between Schmitt trigger switching levels. Data based on characterization, not tested in production.

3. Leakage could be higher than max. if negative current is injected on adjacent pins.

4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

*Note:* I/O pins are powered from $V_{DD}$ voltage except pins which can be used as SDADC inputs:

- PB2, PB10 and PE7 to PE15 I/O pins are powered from VDDSD12.

- PB14 to PB15 and PD8 to PD15 I/O pins are powered from VDDSD3. All I/O ground pins are internally connected to $V_{SS}$.

$V_{DD}$ mentioned in the Table 51 represents power voltage for a given I/O pin ($V_{DD}$ or VDDSD12 or VDDSD3).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in Figure 15 and Figure 16 for standard I/Os, and in Figure 17 and Figure 18 for 5 V tolerant I/Os.

**Figure 15. TC and TTa I/O input characteristics - CMOS port**
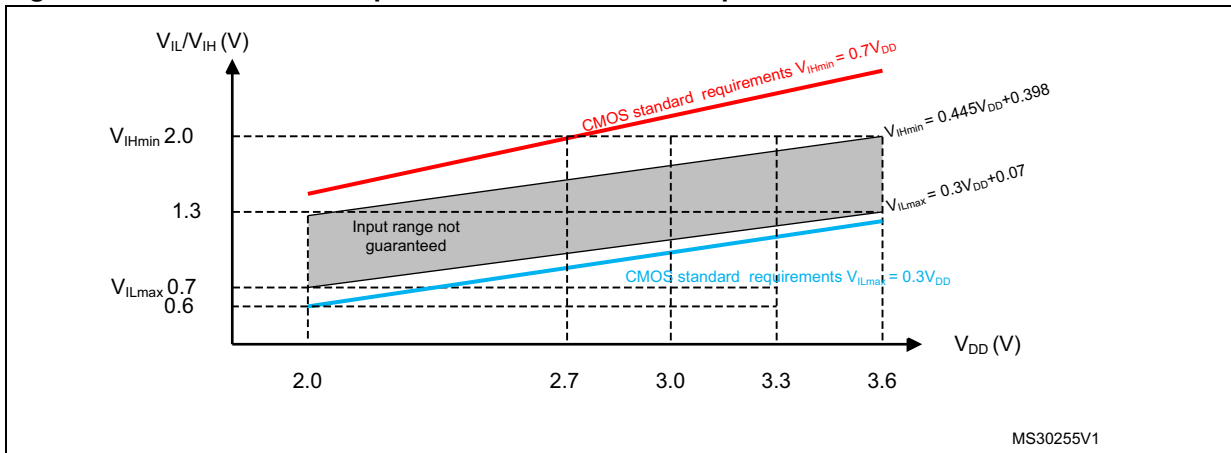


**Figure 16. TC and TTa I/O input characteristics - TTL port**
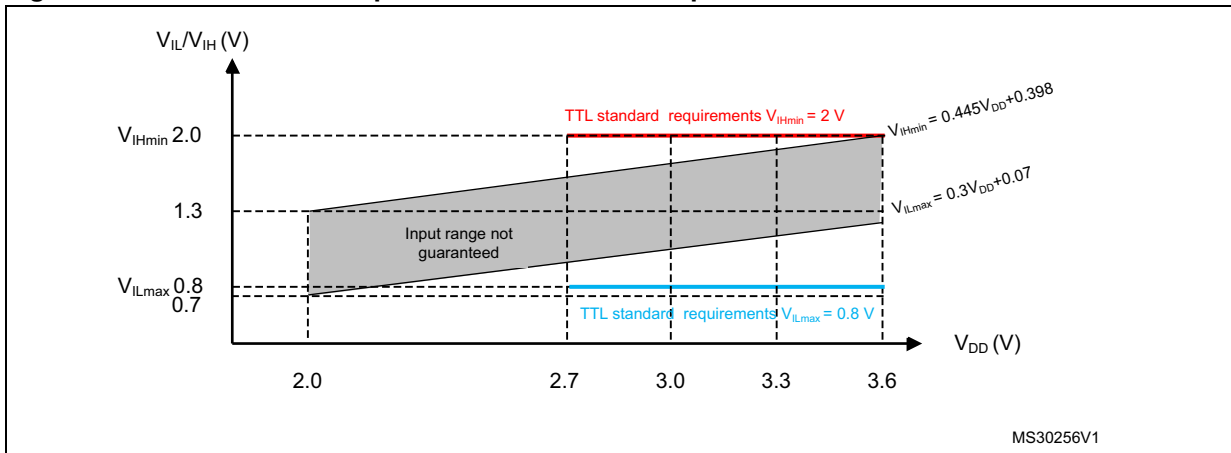


**Figure 17. Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port**
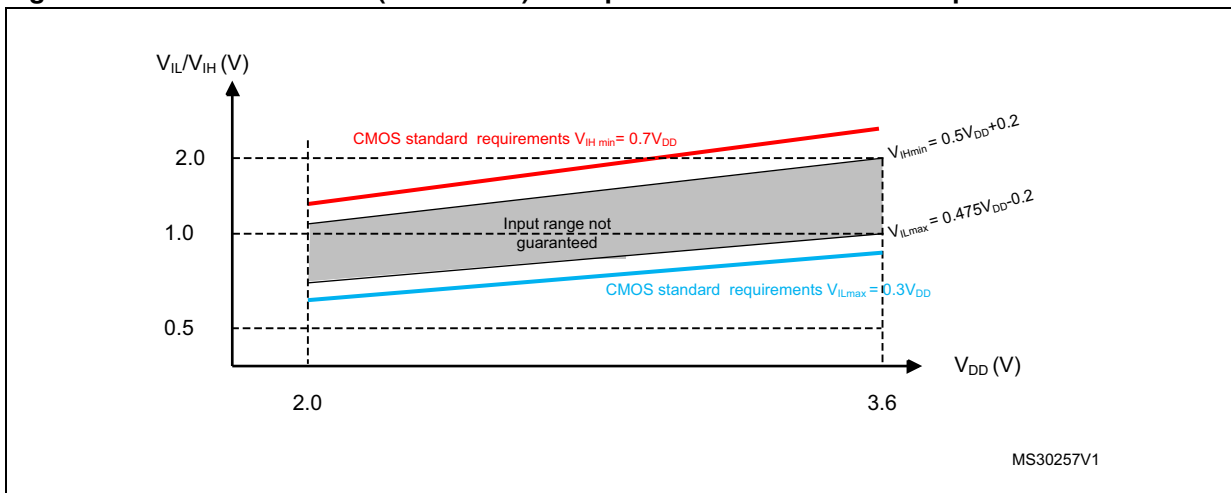
**Figure 18. Five volt tolerant (FT and FTf) I/O input characteristics - TTL port**
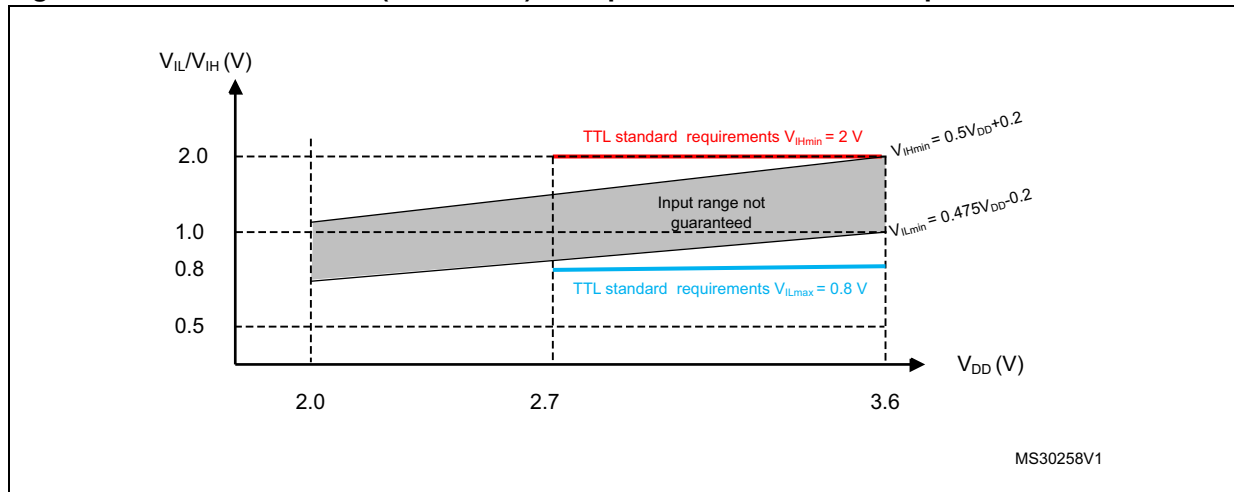


## Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed $V_{OL}/V_{OH}$).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

● The sum of the currents sourced by all the I/Os on $V_{DD}$, plus the maximum Run consumption of the MCU sourced on $V_{DD}$, cannot exceed the absolute maximum rating $I_{VDD}$ (see *Table 22*).

● The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $I_{VSS}$ (see *Table 22*).

## Output voltage levels

Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 24*. All I/Os are CMOS and TTL compliant (FT, TTa or TC unless otherwise specified).

**Table 52.     Output voltage characteristics**

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| | | STM32F37xVx | STM32F37xCx, STM32F37xRx | | | |
| $V_{OL}$ [1] | Output low level voltage for an I/O pin when 8 pins are sunk at the same time | CMOS port[2] $I_{IO}$ = +8 mA 2.7 V < $V_{DD}$ < 3.6 V | CMOS port[2] $I_{IO}$ = +8 mA 2.7 V < $V_{DD}$ < 3.6 V | | 0.4 | V |
| $V_{OH}$ [3] | Output high level voltage for an I/O pin when 8 pins are sourced at the same time | | CMOS port[2] $I_{IO}$ = +4 mA 2.7 V < $V_{DD}$ < 3.6 V | $V_{DD}$–0.4 | | |
| $V_{OL}$ [1] | Output low level voltage for an I/O pin when 8 pins are sunk at the same time | TTL port[2] $I_{IO}$ = +8 mA 2.7 V < $V_{DD}$ < 3.6 V | TTL port[2] $I_{IO}$ =+ 8 mA 2.7 V < $V_{DD}$ < 3.6 V | | 0.4 | |
| $V_{OH}$ [3] | Output high level voltage for an I/O pin when 8 pins are sourced at the same time | | TTL port[2] $I_{IO}$ =+ 4 mA 2.7 V < $V_{DD}$ < 3.6 V | 2.4 | | |
| $V_{OL}$ [1][4] | Output low level voltage for a TTL pin when 4 pins are sunk at the same time | $I_{IO}$ = +20 mA 2.7 V < $V_{DD}$ < 3.6 V | $I_{IO}$ = +20 mA 2.7 V < $V_{DD}$ < 3.6 V | | 1.3 | |
| $V_{OH}$ [3][4] | Output high level voltage for an I/O pin when 4 pins are sourced at the same time | | $I_{IO}$ = +10 mA 2.7 V < $V_{DD}$ < 3.6 V | $V_{DD}$–1.3 | | |
| $V_{OL}$ [1][4] | Output low level voltage for an I/O pin when 8 pins are sunk at the same time | $I_{IO}$ = +6 mA 2 V < $V_{DD}$ < 2.7 V | $I_{IO}$ = +5 mA 2 V < $V_{DD}$ < 2.7 V | | 0.4 | |
| $V_{OH}$ [3][4] | Output high level voltage for an I/O pin when 8 pins are sourced at the same time | | | $V_{DD}$–0.4 | | |
| $V_{OLFM+}$ | Output low level voltage for a FTf I/O pins in FM+ mode | $I_{IO}$ = +20 mA 2.7 V < $V_{DD}$ < 3.6 V | $I_{IO}$ = +20 mA 2.7 V < $V_{DD}$ < 3.6 V | | 0.4 | |

1. The $I_{IO}$ current sunk by the device must always respect the absolute maximum rating specified in *Table 22* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.

2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.

3. The $I_{IO}$ current sourced by the device must always respect the absolute maximum rating specified in *Table 22* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.

4. Data based on characterization results, not tested in production.

*Note:*        *I/O pins are powered from $V_{DD}$ voltage except pins which can be used as SDADC inputs:*

*- PB2, PB10 and PE7 to PE15 I/O pins are powered from VDDSD12.*

*- PB14 to PB15 and PD8 to PD15 I/O pins are powered from VDDSD3. All I/O ground pins are internally connected to $V_{SS}$.*

*$V_{DD}$ mentioned in the Table 52 represents power voltage for a given I/O pin ($V_{DD}$ or VDDSD12 or VDDSD3).*

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 19* and *Table 53*, respectively.
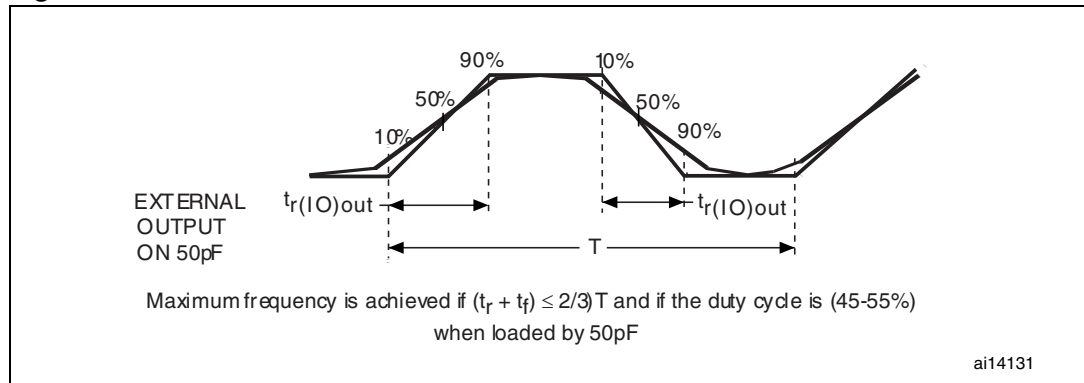
Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 24*.

**Table 53. I/O AC characteristics[1]**

| OSPEEDRy [1:0] value[1] | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| x0 | $f_{max(IO)out}$ | Maximum frequency[2] | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | | 2 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | | 125[3] | ns |
| | $t_{r(IO)out}$ | Output low to high level rise time | | | 125[3] | |
| 01 | $f_{max(IO)out}$ | Maximum frequency[2] | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | | 10 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | | 25[3] | ns |
| | $t_{r(IO)out}$ | Output low to high level rise time | | | 25[3] | |
| 11 | $f_{max(IO)out}$ | Maximum frequency[2][3] | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 50 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 30 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | | 20 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 5[3] | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 8[3] | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | | 12[3] | |
| | $t_{r(IO)out}$ | Output low to high level rise time | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 5[3] | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 8[3] | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | | 12[3] | |
| FM+ configuration [4] | $f_{max(IO)out}$ | Maximum frequency[2] | TBD | | TBD | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | TBD | | TBD | ns |
| | $t_{r(IO)out}$ | Output low to high level rise time | TBD | | TBD | |
| | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | | 10 | | ns |

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0313 reference manual for a description of GPIO Port configuration register.

2. The maximum frequency is defined in *Figure 19*.

3. Guaranteed by design, not tested in production.

4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the STM32F37xx and STM32F38xx reference manual RM0313 for a description of FM+ I/O mode configuration

**Figure 19.  I/O AC characteristics definition**



### 6.3.14  NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see *Table 51*).

Unless otherwise specified, the parameters given in *Table 54* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 24*.

**Table 54.  NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $V_{IL(NRST)}$[1] | NRST Input low level voltage | | −0.5 | | 0.8 | V |
| $V_{IH(NRST)}$[1] | NRST Input high level voltage | | 2 | | $V_{DD}$+0.5 | |
| $V_{hys(NRST)}$[1] | NRST Schmitt trigger voltage hysteresis | | | 200 | | mV |
| $R_{PU}$ | Weak pull-up equivalent resistor[2] | $V_{IN} = V_{SS}$ | 25 | 40 | 55 | kΩ |
| $V_{F(NRST)}$[1] | NRST Input filtered pulse | | | | 100 | ns |
| $V_{NF(NRST)}$[1] | NRST Input not filtered pulse | | 300 | | | ns |

1. Guaranteed by design, not tested in production.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

**Figure 20. Recommended NRST pin protection**



1. The reset network protects the device against parasitic resets.

2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 54*. Otherwise the reset will not be taken into account by the device.
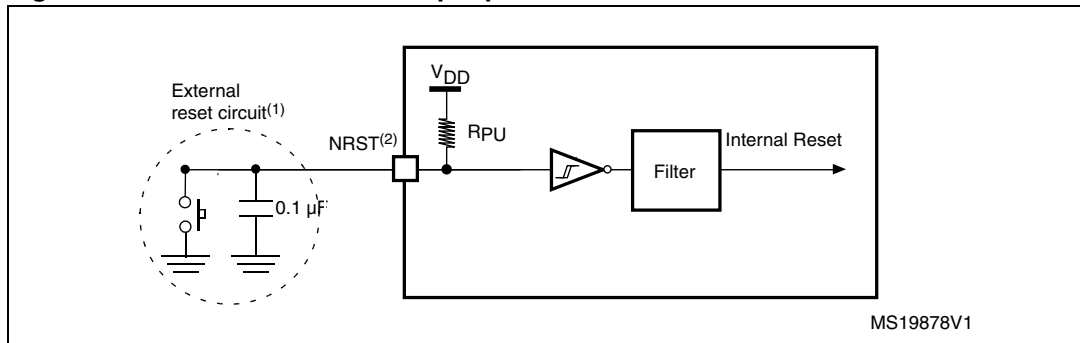
### 6.3.15 Communications interfaces

#### I$^2$C interface characteristics

Unless otherwise specified, the parameters given in *Table 55* are derived from tests performed under ambient temperature, $f_{PCLK1}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 24*.

The I$^2$C interface meets the requirements of the standard I$^2$C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and $V_{DD}$ is disabled, but is still present.

The I$^2$C characteristics are described in *Table 55*. Refer also to *Section 6.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

**Table 55.    I$^2$C characteristics[1]**

| Symbol | Parameter | Standard mode | | Fast mode | | Fast mode Plus | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | | 1.3 | | 0.5 | | μs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | | 0.6 | | 0.26 | | |
| $t_{su(SDA)}$ | SDA setup time | 250 | | 100 | | 50 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0[2] | 3450[3] | 0[2] | 900[3] | 0[4] | 450[3] | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | | 1000 | | 300 | | 120 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | | 300 | | 300 | | 120 | |
| $t_{h(STA)}$ | Start condition hold time | 4.0 | | 0.6 | | 0.26 | | μs |
| $t_{su(STA)}$ | Repeated Start condition setup time | 4.7 | | 0.6 | | 0.26 | | |
| $t_{su(STO)}$ | Stop condition setup time | 4.0 | | 0.6 | | 0.26 | | μs |
| $t_{w(STO:STA)}$ | Stop to Start condition time (bus free) | 4.7 | | 1.3 | | 0.5 | | μs |
| $C_b$ | Capacitive load for each bus line | | 400 | | 400 | | 550 | pF |

1. The I2C characteristics are the requirements from I2C bus specification rev03. They are guaranteed by design when I2Cx_TIMING register is correctly programmed (Refer to reference manual). These characteristics are not tested in production.

2. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.

4. The device must internally provide a hold time of at least 120ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

**Table 56.** **I2C analog filter characteristics**[1]

| Symbol | Parameter | Min | Max | Unit |
|--------|-----------|-----|-----|------|
| $t_{SP}$ | Pulse width of spikes that are suppressed by the analog filter | 50 | 260 | ns |

1. Guaranteed by design, not tested in production.

**Figure 21.** **I²C bus AC waveforms and measurement circuit**
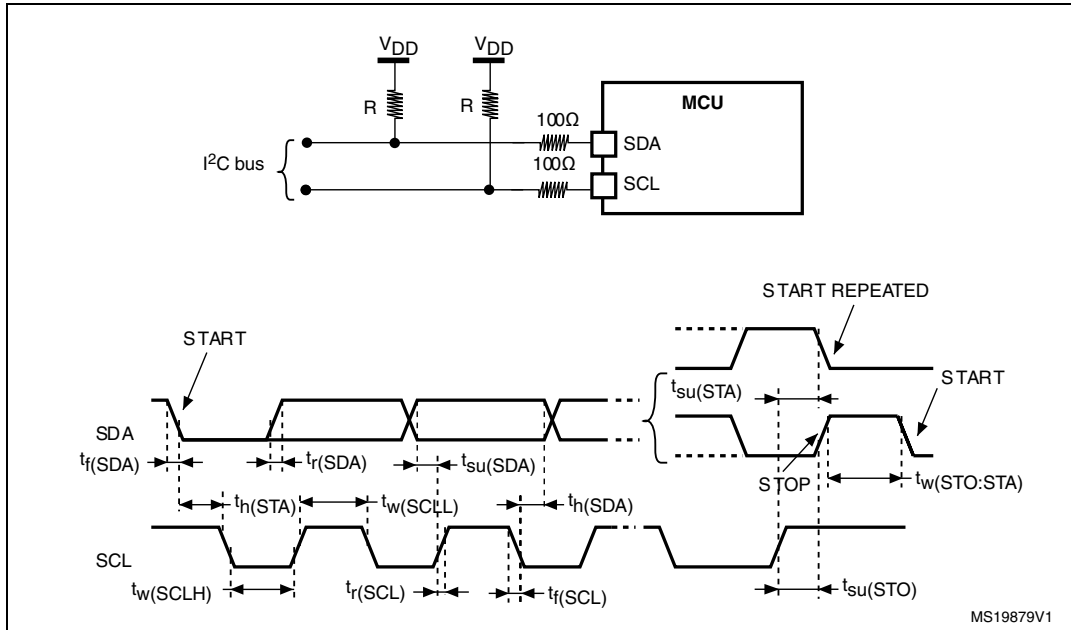


1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

## SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 57* for SPI or in *Table 58* for I²S are derived from tests performed under ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 24*.

Refer to *Section 6.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

**Table 57.    SPI characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$ $1/t_{c(SCK)}$[1] | SPI clock frequency | Master mode | | 18 | MHz |
| | | Slave mode | | 18 | |
| $t_{r(SCK)}$ $t_{f(SCK)}$[1] | SPI clock rise and fall time | Capacitive load: C = 30 pF | | 8 | ns |
| DuCy(SCK)[1] | SPI slave input clock duty cycle | Slave mode | 30 | 70 | % |
| $t_{su(NSS)}$[1] | NSS setup time | Slave mode | 2Tpclk | | ns |
| $t_{h(NSS)}$[1] | NSS hold time | Slave mode | 4Tpclk | | |
| $t_{w(SCKH)}$[1] $t_{w(SCKL)}$[1] | SCK high and low time | Master mode, $f_{PCLK}$ = 36 MHz, presc = 4 | Tpclk/2 - 3 | Tpclk/2 + 3 | |
| $t_{su(MI)}$[1] $t_{su(SI)}$[1] | Data input setup time | Master mode | 5.5 | | |
| | | Slave mode | 6.5 | | |
| $t_{h(MI)}$[1] | Data input hold time | Master mode | 5 | | |
| $t_{h(SI)}$[1] | | Slave mode | 5 | | |
| $t_{a(SO)}$[1][2] | Data output access time | Slave mode, $f_{PCLK}$ = 24 MHz | 0 | 4Tpclk | |
| $t_{dis(SO)}$[1][3] | Data output disable time | Slave mode | 0 | 24 | |
| $t_{v(SO)}$[1] | Data output valid time | Slave mode (after enable edge) | | 39 | |
| $t_{v(MO)}$[1] | Data output valid time | Master mode (after enable edge) | | 3 | |
| $t_{h(SO)}$[1] | Data output hold time | Slave mode (after enable edge) | 15 | | |
| $t_{h(MO)}$[1] | | Master mode (after enable edge) | 4 | | |

1. Data based on characterization results, not tested in production.

2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.

3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

**Figure 22.    SPI timing diagram - slave mode and CPHA = 0**
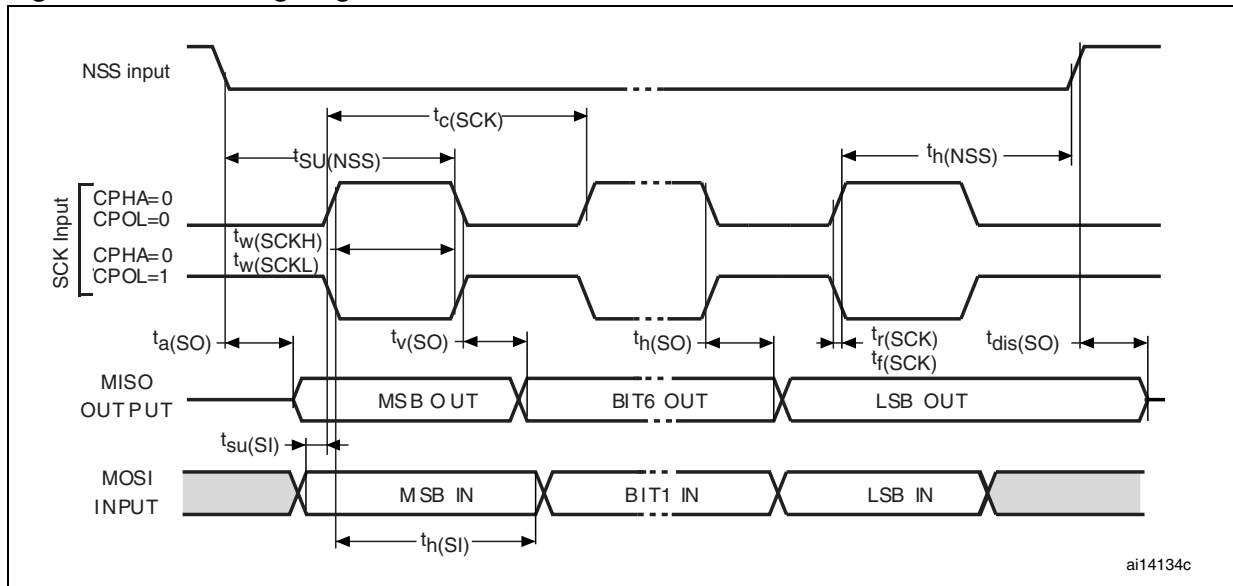


**Figure 23.    SPI timing diagram - slave mode and CPHA = 1[1]**
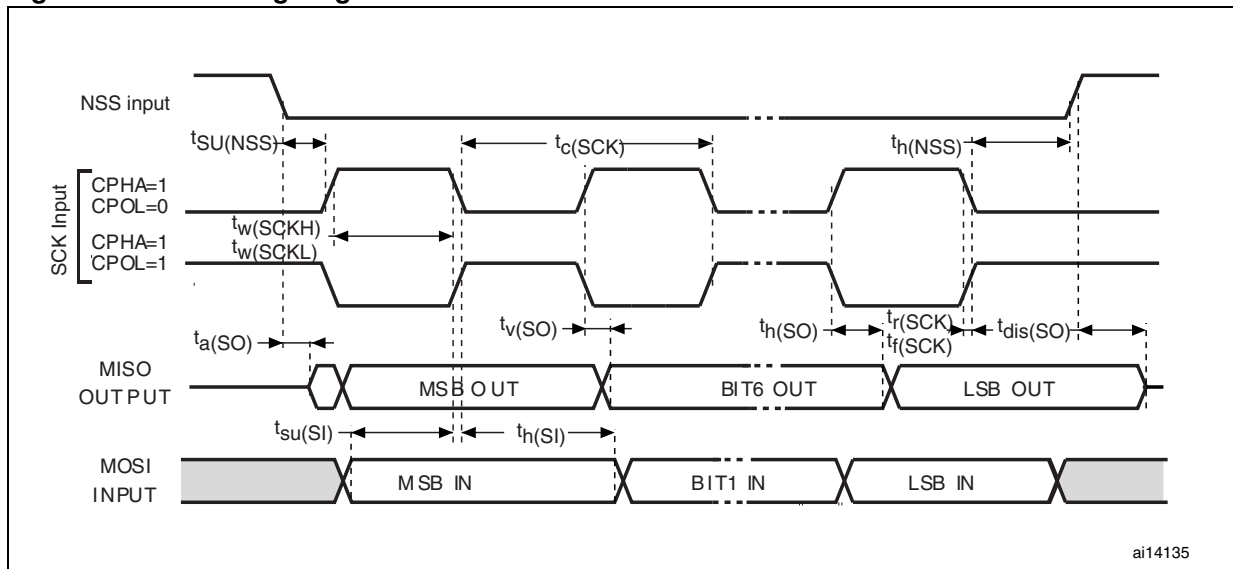


1.    Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Figure 24. SPI timing diagram - master mode[1]**
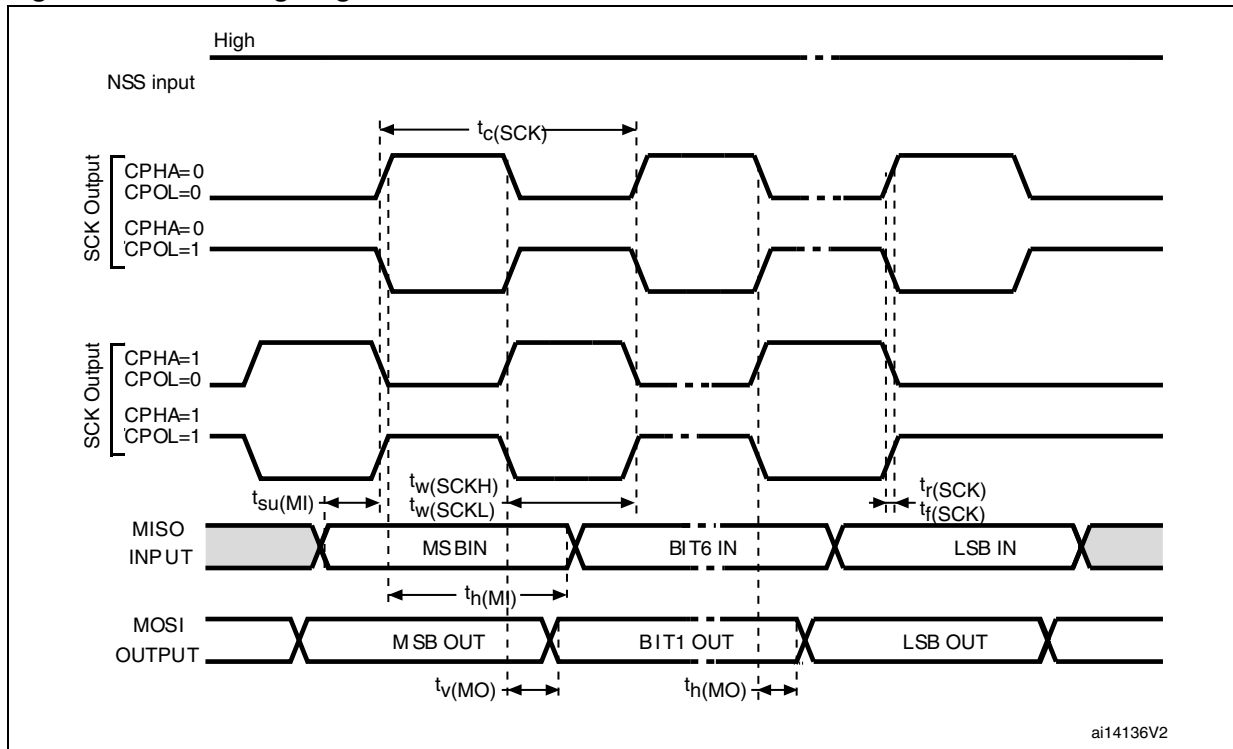


1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Table 58.     I$^2$S characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------|-----------|------------|-----|-----|------|
| DuCy(SCK) | I2S slave input clock duty cycle | Slave mode | 30 | 70 | % |
| $f_{CK}$ $1/t_{c(CK)}$ | I$^2$S clock frequency | Master mode (data: 16 bits, Audio frequency = 48 kHz) | 1.528 | 1.539 | MHz |
|  |  | Slave mode | 0 | 12.288 |  |
| $t_{r(CK)}$[1] $t_{f(CK)}$ | I$^2$S clock rise and fall time | Capacitive load $C_L$ = 30 pF |  | 8 | ns |
| $t_{v(WS)}$ [1] | WS valid time | Master mode | 4 |  |  |
| $t_{h(WS)}$ [1] | WS hold time | Master mode | 4 |  |  |
| $t_{su(WS)}$ [1] | WS setup time | Slave mode | 2 |  |  |
| $t_{h(WS)}$ [1] | WS hold time | Slave mode |  |  |  |
| $t_{w(CKH)}$ [1] | I2S clock high time | Master $f_{PCLK}$= 16 MHz, audio frequency = 48 kHz | 306 |  |  |
| $t_{w(CKL)}$ [1] | I2S clock low time |  | 312 |  |  |
| $t_{su(SD\_MR)}$ [1] | Data input setup time | Master receiver | 6 |  |  |
| $t_{su(SD\_SR)}$ [1] |  | Slave receiver | 3 |  |  |
| $t_{h(SD\_MR)}$ [1][2] | Data input hold time | Master receiver | 1.5 |  |  |
| $t_{h(SD\_SR)}$ [1][2] |  | Slave receiver | 1.5 |  |  |
| $t_{v(SD\_ST)}$ [1][2] | Data output valid time | Slave transmitter (after enable edge) |  | 16 |  |
| $t_{h(SD\_ST)}$ [1] | Data output hold time | Slave transmitter (after enable edge) | 16 |  |  |
| $t_{v(SD\_MT)}$ [1][2] | Data output valid time | Master transmitter (after enable edge) |  | 2 |  |
| $t_{h(SD\_MT)}$ [1] | Data output hold time | Master transmitter (after enable edge) | 0 |  |  |

1. Data based on design simulation and/or characterization results, not tested in production.

2. Depends on $f_{PCLK}$. For example, if $f_{PCLK}$=8 MHz, then $T_{PCLK}$ = 1/$f_{PLCLK}$ =125 ns.

**Figure 25. I²S slave timing diagram (Philips protocol)[1]**
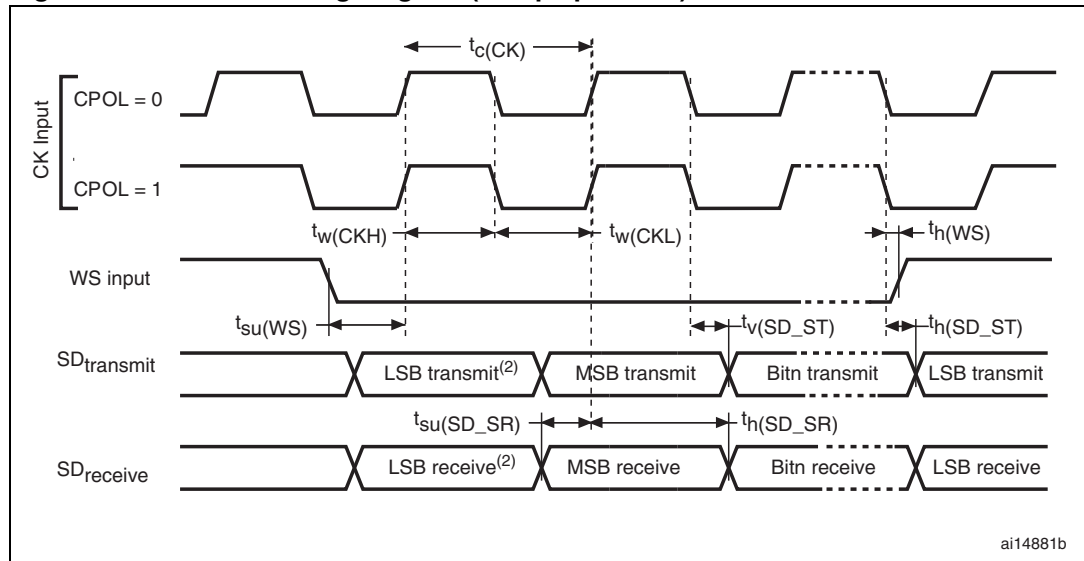


1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.

2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

**Figure 26. I²S master timing diagram (Philips protocol)[1]**
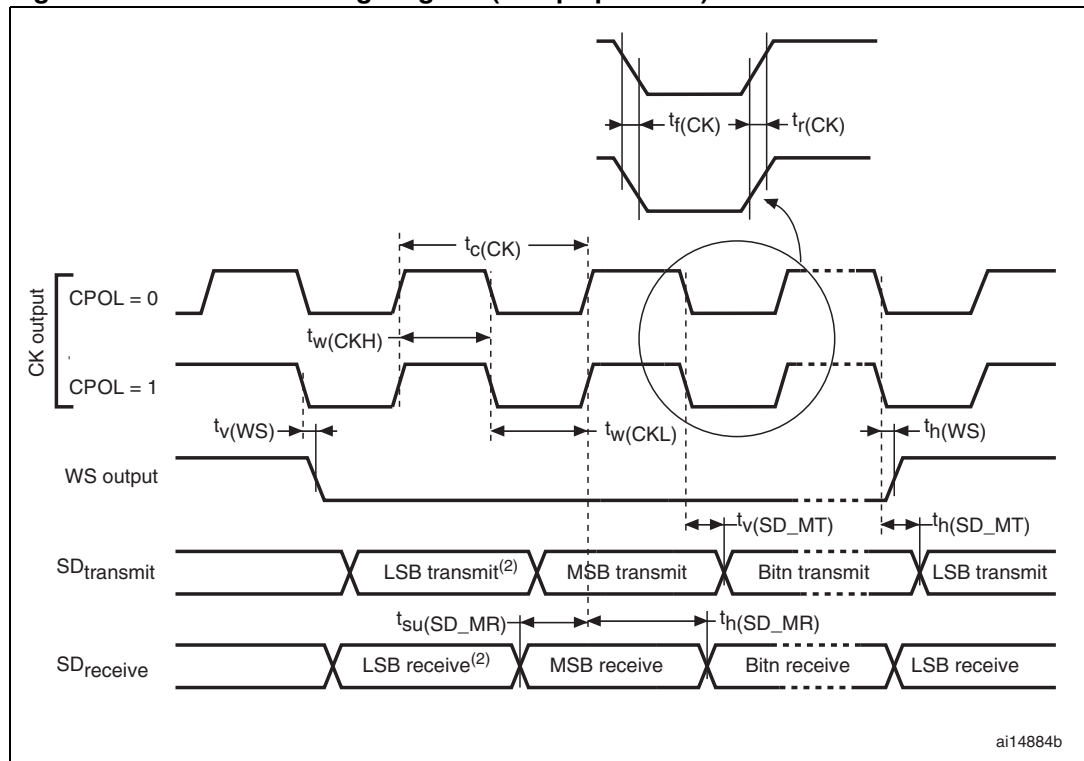


1. Data based on characterization results, not tested in production.

2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

### 6.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 59* are preliminary values derived from tests performed under ambient temperature, $f_{PCLK2}$ frequency and $V_{DDA}$ supply voltage conditions summarized in *Table 24*.

*Note:* *It is recommended to perform a calibration after each power-up.*

**Table 59. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Power supply | | 2.4 | | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | | 2.4 | | $V_{DDA}$ | V |
| $I_{VREF}$ | Current on the $V_{REF}$ input pin | | | 160[1] | 220[1] | µA |
| $f_{ADC}$ | ADC clock frequency | | 0.6 | | 14 | MHz |
| $f_S$[2] | Sampling rate | | 0.05 | | 1 | MHz |
| $f_{TRIG}$[2] | External trigger frequency | $f_{ADC}$ = 14 MHz | | | 823 | kHz |
| | | | | | 17 | $1/f_{ADC}$ |
| $V_{AIN}$ | Conversion voltage range | | 0 ($V_{SSA}$ or $V_{REF-}$ tied to ground) | | $V_{REF+}$ | V |
| $R_{SRC}$[2] | Signal source impedance | See *Equation 1* and *Table 60* for details | | | 50 | kΩ |
| $R_{ADC}$[2] | Sampling switch resistance | | | | 1 | kΩ |
| $C_{ADC}$[2] | Internal sample and hold capacitor | | | | 8 | pF |
| $t_{CAL}$[2] | Calibration time | $f_{ADC}$ = 14 MHz | 5.9 | | | µs |
| | | | 83 | | | $1/f_{ADC}$ |
| $t_{lat}$[2] | Injection trigger conversion latency | $f_{ADC}$ = 14 MHz | | | 0.214 | µs |
| | | | | | 2[3] | $1/f_{ADC}$ |
| $t_{latr}$[2] | Regular trigger conversion latency | $f_{ADC}$ = 14 MHz | | | 0.143 | µs |
| | | | | | 2[3] | $1/f_{ADC}$ |
| $t_S$[2] | Sampling time | $f_{ADC}$ = 14 MHz | 0.107 | | 17.1 | µs |
| | | | 1.5 | | 239.5 | $1/f_{ADC}$ |
| $t_{STAB}$[2] | Power-up time | | 0 | 0 | 1 | µs |
| $t_{CONV}$[2] | Total conversion time (including sampling time) | $f_{ADC}$ = 14 MHz | 1 | | 18 | µs |
| | | | 14 to 252 ($t_S$ for sampling +12.5 for successive approximation) | | | $1/f_{ADC}$ |

1. Based on characterization, not tested in production.

2. Guaranteed by design, not tested in production.

3. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 59*

**Equation 1: R$_{SRC}$ max formula**

$$R_{SRC} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external signal source impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

**Table 60.    R$_{SRC}$ max for f$_{ADC}$ = 14 MHz[1]**

| T$_s$ (cycles) | t$_S$ (µs) | R$_{SRC}$ max (kΩ) |
|---|---|---|
| 1.5 | 0.11 | 0.4 |
| 7.5 | 0.54 | 5.9 |
| 13.5 | 0.96 | 11.4 |
| 28.5 | 2.04 | 25.2 |
| 41.5 | 2.96 | 37.2 |
| 55.5 | 3.96 | 50 |
| 71.5 | 5.11 | 50 |
| 239.5 | 17.1 | 50 |

1. Guaranteed by design, not tested in production.

**Table 61.    ADC accuracy[1][2] [3]**

| Symbol | Parameter | Test conditions | Typ | Max[4] | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | f$_{ADC}$ = 14 MHz, R$_{SRC}$ < 10 kΩ, V$_{DDA}$ = 3 V to 3.6 V T$_A$ = 25 °C | ±1.3 | ±3 | LSB |
| EO | Offset error | | ±1 | ±2 | |
| EG | Gain error | | ±0.5 | ±1.5 | |
| ED | Differential linearity error | | ±0.7 | ±1 | |
| EL | Integral linearity error | | ±0.8 | ±1.5 | |
| ET | Total unadjusted error | f$_{ADC}$ = 14 MHz, R$_{SRC}$ < 10 kΩ, V$_{DDA}$ = 2.5 V to 3.6 V T$_A$ = -40 to 105 °C [5] | ±2 | ±5 | LSB |
| EO | Offset error | | ±1.5 | ±2.5 | |
| EG | Gain error | | ±1.5 | ±3 | |
| ED | Differential linearity error | | ±1 | ±2 | |
| EL | Integral linearity error | | ±1.5 | ±3 | |

1. ADC DC accuracy values are measured after internal calibration.

2. ADC accuracy vs. negative injection current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.
   Any positive injection current within the limits specified for I$_{INJ(PIN)}$ and ΣI$_{INJ(PIN)}$ in *Section 6.3.13* does not affect the ADC accuracy.

3. Better performance may be achieved in restricted V$_{DDA}$, frequency and temperature ranges.

4. Data based on characterization results, not tested in production.

5. V$_{DDA}$ = 2.4 to 3.6 V if T$_A$ = 0 to 105 °C

**Figure 27. ADC accuracy characteristics**



$$1 \text{ LSB}_{IDEAL} = \frac{V_{DDA}}{4096}$$

(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

$E_T$=Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.

$E_O$=Offset Error: deviation between the first actual transition and the first ideal one.

$E_G$=Gain Error: deviation between the last ideal transition and the last actual one.

$E_D$=Differential Linearity Error: maximum deviation between actual steps and the ideal one.

$E_L$=Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

**Figure 28. Typical connection diagram using the ADC**



1. Refer to *Table 59* for the values of $R_{SRC}$, $R_{ADC}$ and $C_{ADC}$.

2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

### General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 9*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

## 6.3.17 DAC electrical specifications

**Table 62.    DAC characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | 2.4 | - | 3.6 | V | |
| $V_{REF+}$ | Reference supply voltage | 2.4 | - | 3.6 | V | $V_{REF+}$ must always be below $V_{DDA}$ |
| $V_{SSA}$ | Ground | 0 | - | 0 | V | |
| $R_{LOAD}$[1] | Resistive load with buffer ON | 5 | - | | kΩ | |
| $R_O$[1] | Impedance output with buffer OFF | - | - | 15 | kΩ | When the buffer is OFF, the Minimum resistive load between DAC_OUT and $V_{SS}$ to have a 1% accuracy is 1.5 MΩ |
| $C_{LOAD}$[1] | Capacitive load | - | - | 50 | pF | Maximum capacitive load at DAC_OUT pin (when the buffer is ON). |
| DAC_OUT min[1] | Lower DAC_OUT voltage with buffer ON | 0.2 | - | - | V | It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{REF+}$ = 3.6 V and (0x155) and (0xEAB) at $V_{REF+}$ = 2.4 V |
| DAC_OUT max[1] | Higher DAC_OUT voltage with buffer ON | - | - | $V_{DDA} - 0.2$ | V | |
| DAC_OUT min[1] | Lower DAC_OUT voltage with buffer OFF | - | 0.5 | | mV | It gives the maximum output excursion of the DAC. |
| DAC_OUT max[1] | Higher DAC_OUT voltage with buffer OFF | - | | $V_{REF+} - 1LSB$ | V | |
| $I_{DDVREF+}$[2] | DAC DC current consumption in quiescent mode (Standby mode) | - | | 220 | µA | With no load, worst code (0xF1C) at $V_{REF+}$ = 3.6 V in terms of DC consumption on the inputs |
| $I_{DDA}$[2] | DAC DC current consumption in quiescent mode (Standby mode) | - | | 380 | µA | With no load, middle code (0x800) on the inputs |
| | | - | | 480 | µA | With no load, worst code (0xF1C) at $V_{REF+}$ = 3.6 V in terms of DC consumption on the inputs |
| DNL[2] | Differential non linearity Difference between two consecutive code-1LSB) | - | | ±0.5 | LSB | Given for the DAC in 10-bit configuration |
| | | - | | ±2 | LSB | Given for the DAC in 12-bit configuration |
| INL[2] | Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023) | - | - | ±1 | LSB | Given for the DAC in 10-bit configuration |
| | | - | - | ±4 | LSB | Given for the DAC in 12-bit configuration |

**Table 62. DAC characteristics (continued)**

| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| Offset[2] | Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$) | - | - | ±10 | mV | Given for the DAC in 12-bit configuration |
| | | - | - | ±3 | LSB | Given for the DAC in 10-bit at $V_{REF+}$ = 3.6 V |
| | | - | - | ±12 | LSB | Given for the DAC in 12-bit at $V_{REF+}$ = 3.6 V |
| Gain error[2] | Gain error | - | - | ±0.5 | % | Given for the DAC in 12bit configuration |
| $t_{SETTLING}$[2] | Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB | - | 3 | 4 | µs | $C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ |
| Update rate[2] | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB) | - | - | 1 | MS/s | $C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ |
| $t_{WAKEUP}$[2] | Wakeup time from off state (Setting the ENx bit in the DAC Control register) | - | 6.5 | 10 | µs | $C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ input code between lowest and highest possible ones. |
| PSRR+ [1] | Power supply rejection ratio (to $V_{DDA}$) (static DC measurement | - | -67 | -40 | dB | No $R_{LOAD}$, $C_{LOAD}$ = 50 pF |

1. Guaranteed by design, not tested in production.

2. Guaranteed by characterization, not tested in production.

**Figure 29. 12-bit buffered /non-buffered DAC**
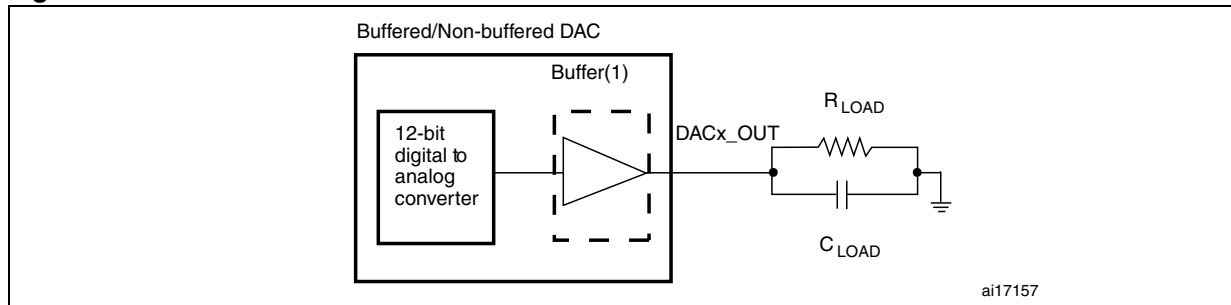


1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

## 6.3.18 Comparator characteristics

**Table 63.     Comparator characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | | | 2 | | 3.6 | V |
| $V_{IN}$ | Comparator input voltage range | | | 0 | | $V_{DDA}$ | V |
| $V_{BG}$ | Scaler input voltage | | | | 1.2 | | |
| $V_{SC}$ | Scaler offset voltage | | | | ±5 | ±10 | mV |
| $t_{S\_SC}$ | Scaler startup time from power down | | | | | 0.1 | ms |
| $t_{START}$ | Comparator startup time | Startup time to reach propagation delay specification | | | | 60 | µs |
| $t_D$ | Propagation delay for 200 mV step with 100 mV overdrive | Ultra-low power mode | | | 2 | 4.5 | µs |
| | | Low power mode | | | 0.7 | 1.5 | µs |
| | | Medium power mode | | | 0.3 | 0.6 | µs |
| | | High speed power mode | $V_{DDA} \geq 2.7$ V | | 50 | 100 | ns |
| | | | $V_{DDA} < 2.7$ V | | 100 | 240 | ns |
| | Propagation delay for full range step with 100 mV overdrive | Ultra-low power mode | | | 2 | 7 | µs |
| | | Low power mode | | | 0.7 | 2.1 | µs |
| | | Medium power mode | | | 0.3 | 1.2 | µs |
| | | High speed power mode | $V_{DDA} \geq 2.7$ V | | 90 | 180 | ns |
| | | | $V_{DDA} < 2.7$ V | | 110 | 300 | ns |
| $V_{offset}$ | Comparator offset error | | | | ±4 | ±10 | mV |
| $dV_{offset}/dT$ | Offset error temperature coefficient | | | | 18 | | µV/°C |
| $I_{DD(COMP)}$ | COMP current consumption | Ultra-low power mode | | | 1.2 | 1.5 | µA |
| | | Low power mode | | | 3 | 5 | µA |
| | | Medium power mode | | | 10 | 15 | µA |
| | | High speed power mode | | | 75 | 100 | µA |

**Table 63.    Comparator characteristics (continued)**

| Symbol | Parameter | Conditions | | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|---|
| $V_{hys}$ | Comparator hysteresis | No hysteresis (COMPxHYST[1:0]=00) | | | 0 | | mV |
| | | Low hysteresis (COMPxHYST[1:0]=01) | High speed power mode | 3 | 8 | 13 | |
| | | | All other power modes | 5 | | 10 | |
| | | Medium hysteresis (COMPxHYST[1:0]=10) | High speed power mode | 7 | 15 | 26 | |
| | | | All other power modes | 9 | | 19 | |
| | | High hysteresis (COMPxHYST[1:0]=11) | High speed power mode | 18 | 31 | 49 | |
| | | | All other power modes | 19 | | 40 | |

1. Guaranteed by design, not tested in production.

### 6.3.19 Temperature sensor characteristics

**Table 64. TS characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_L$ | $V_{SENSE}$ linearity with temperature | | ±1 | ±2 | °C |
| Avg_Slope[1] | Average slope | 4.0 | 4.3 | 4.6 | mV/°C |
| $V_{25}$ | Voltage at 25 °C | 1.34 | 1.43 | 1.52 | V |
| $t_{START}$[1] | Startup time | 4 | | 10 | µs |
| $T_{S\_temp}$[2][1] | ADC sampling time when reading the temperature | 17.1 | | | µs |

1. Guaranteed by design, not tested in production.

2. Shortest sampling time can be determined in the application by multiple iterations.

### 6.3.20 $V_{BAT}$ monitoring characteristics

**Table 65. $V_{BAT}$ monitoring characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| R | Resistor bridge for $V_{BAT}$ | - | 50 | - | KΩ |
| Q | Ratio on $V_{BAT}$ measurement | - | 2 | - | |
| Er[1] | Error on Q | -1 | - | +1 | % |
| $T_{S\_vbat}$[2] | ADC sampling time when reading the $V_{BAT}$ 1mV accuracy | 5 | - | - | µs |

1. Guaranteed by design, not tested in production.

2. Shortest sampling time can be determined in the application by multiple iterations.

### 6.3.21 Timer characteristics

The parameters given in *Table 66* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 66. TIMx[1] [2]characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | | 1 | | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72 MHz | 13.9 | | ns |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | | 0 | $f_{TIMxCLK}$/2 | MHz |
| | | $f_{TIMxCLK}$ = 72 MHz | 0 | 24 | MHz |
| $Res_{TIM}$ | Timer resolution | TIMx (except TIM2) | | 16 | bit |
| | | TIM2 | | 32 | |

**Table 66.    TIMx**[1] [2]**characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------|-----------|------------|-----|-----|------|
| $t_{COUNTER}$ | 16-bit counter clock period | | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72 MHz | 0.0139 | 910 | µs |
| $t_{MAX\_COUNT}$ | Maximum possible count with 32-bit counter | | | 65536 × 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72 MHz | | 59.65 | s |

1.  TIMx is used as a general term to refer to the TIM2, TIM3, TIM4, TIM5, TIM6, TIM7, TIM12, TIM13, TIM14, TIM15, TIM16 , TIM17, TIM18 and TIM19 timers.

2.  Data based on characterization results, not tested in production.

**Table 67.    IWDG min/max timeout period at 40 kHz (LSI)** [1][2]

| Prescaler divider | PR[2:0] bits | Min timeout (ms) RL[11:0]= 0x000 | Max timeout (ms) RL[11:0]= 0xFFF |
|-------------------|--------------|----------------------------------|----------------------------------|
| /4 | 0 | 0.1 | 409.6 |
| /8 | 1 | 0.2 | 819.2 |
| /16 | 2 | 0.4 | 1638.4 |
| /32 | 3 | 0.8 | 3276.8 |
| /64 | 4 | 1.6 | 6553.6 |
| /128 | 5 | 3.2 | 13107.2 |
| /256 | 7 | 6.4 | 26214.4 |

1.  These timings are given for a 40 kHz clock but the microcontroller's internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

2.  Data based on characterization results, not tested in production.

**Table 68.    WWDG min-max timeout value @72 MHz (PCLK)**

| Prescaler | WDGTB | Min timeout value | Max timeout value |
|-----------|-------|-------------------|-------------------|
| 1 | 0 | 0.05687 | 3.6409 |
| 2 | 1 | 0.1137 | 7.2817 |
| 4 | 2 | 0.2275 | 14.564 |
| 8 | 3 | 0.4551 | 29.127 |

## 6.3.22    USB characteristics

**Table 69.    USB startup time**

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $t_{STARTUP}$[1] | USB transceiver startup time | 1 | µs |

1. Guaranteed by design, not tested in production.

**Table 70.    USB DC electrical characteristics**

| Symbol | Parameter | Conditions | Min.[1] | Max.[1] | Unit |
|---|---|---|---|---|---|
| **Input levels** | | | | | |
| $V_{DD}$ | USB operating voltage[2] | | 3.0[3] | 3.6 | V |
| $V_{DI}$[4] | Differential input sensitivity (for USB compliance) | I(USBDP, USBDM) | 0.2 | | V |
| $V_{CM}$[4] | Differential common mode range | Includes $V_{DI}$ range | 0.8 | 2.5 | |
| $V_{SE}$[4] | Single ended receiver threshold | | 1.3 | 2.0 | |
| **Output levels** | | | | | |
| $V_{OL}$ | Static output level low | $R_L$ of 1.5 kΩ to 3.6 V[5] | | 0.3 | V |
| $V_{OH}$ | Static output level high | $R_L$ of 15 kΩ to $V_{SS}$[5] | 2.8 | 3.6 | |

1. All the voltages are measured from the local ground potential.

2. To be compliant with the USB 2.0 full-speed electrical specification, the USBDP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.

3. The STM32F3xxx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V $V_{DD}$ voltage range.

4. Guaranteed by design, not tested in production.

5. $R_L$ is the load connected on the USB drivers

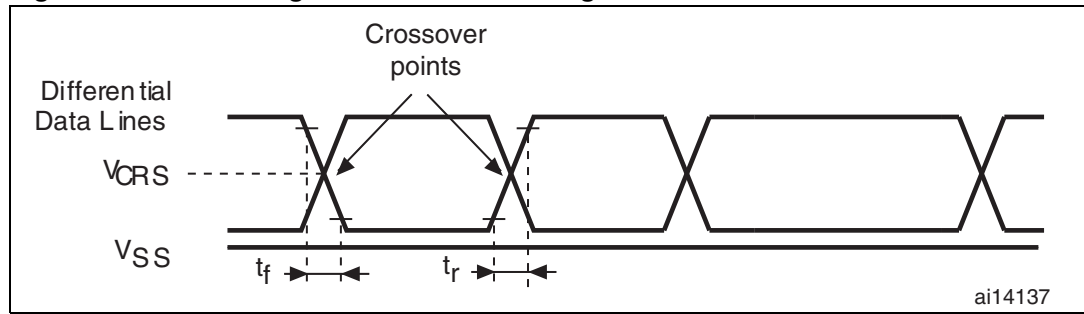**Figure 30. USB timings: definition of data signal rise and fall time**



**Table 71. USB: Full-speed electrical characteristics[1]**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| **Driver characteristics** | | | | | | |
| $t_r$ | Rise time[2] | $C_L$ = 50 pF | 4 | - | 20 | ns |
| $t_f$ | Fall time[2] | $C_L$ = 50 pF | 4 | - | 20 | ns |
| $t_{rfm}$ | Rise/ fall time matching | $t_r/t_f$ | 90 | - | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage | | 1.3 | - | 2.0 | V |
| Output driver Impedance[3] $Z_{DRV}$ | | driving high and low | 28 | 40 | 44 | Ω |

1. Guaranteed by design, not tested in production.

2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

3. No external termination series resistors are required on USBDP (D+) and USBDM (D-), the matching impedance is already included in the embedded driver.

## 6.3.23 CAN (controller area network) interface

Refer to *Section 6.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

## 6.3.24 SDADC characteristics

**Table 72. SDADC characteristics [1]**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | Note |
|--------|-----------|------------|-----|-----|-----|------|------|
| VDDSDx | Power supply | Slow mode ($f_{ADC}$ = 1.5 MHz) | 2.2 | | $V_{DDA}$ | V | |
| | | Fast mode ($f_{ADC}$ = 6 MHz) | 2.4 | | $V_{DDA}$ | | |
| $f_{ADC}$ | SDADC clock frequency | Slow mode ($f_{ADC}$ = 1.5 MHz) | 0.5 | 1.5 | 1.65 | MHz | |
| | | Fast mode ($f_{ADC}$ = 6 MHz) | 0.5 | 6 | 6.3 | | |
| VREFSD+ | Positive ref. voltage | | 1.1 | | VDDSDx | V | |
| VREFSD- | Negative ref. voltage | | | VSSA | | V | |

**Table 72.     SDADC characteristics  (continued)[1]**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| $V_{DDSD}$ | Supply current (VDDSDx = 3.3V) | Fast mode ($f_{ADC}$ = 6 MHz) | | 800 | 1200 | µA | |
| | | Slow mode ($f_{ADC}$ = 1.5 MHz) | | | 600 | | |
| | | Standby | | | 200 | | |
| | | Power down | | | 2.5 | | |
| | | SD_ADC off | | | 1 | | |
| $V_{AIN}$ | Common input voltage range | Single ended mode (zero reference) | $V_{SSA}$ | | VREFSD+ /gain | V | Voltage on AINP or AINN pin |
| | | Single ended offset mode | $V_{SSA}$ | | VREFSD+ /gain/2 | | |
| | | Differential mode | $V_{SSA}$ | | VDDSDx | | |
| $V_{DIFF}$ | Differential input voltage | Differential mode only | -VREFSD+/ gain/2 | | VREFSD+ /gain/2 | | Differential voltage between AINP and AINN |
| $f_S$ | Sampling rate | Slow mode ($f_{ADC}$ = 1.5 MHz) | | 4.166 | | kHz | $f_{ADC}/360$ |
| | | Slow mode one channel only ($f_{ADC}$ = 1.5 MHz) | | 12.5 | | | $f_{ADC}/120$ |
| | | Fast mode multiplexed channel ($f_{ADC}$ = 6 MHz) | | 16.66 | | | $f_{ADC}/360$ |
| | | Fast mode one channel only ($f_{ADC}$ = 6 MHz) | | 50 | | | $f_{ADC}/120$ |
| $t_{CONV}$ | Conversion time | | | 1/fs | | s | |
| Rain | Analog input impedance | One channel, gain = 0.5, $f_{ADC}$ = 1.5 MHz | | 540 | | kΩ | see reference manual for detailed description |
| | | One channel, gain = 0.5, $f_{ADC}$ = 6 MHz | | 135 | | | |
| | | One channel, gain = 8, $f_{ADC}$ = 6 MHz | | 47 | | | |
| $t_{CALIB}$ | Calibration time | $f_{ADC}$ = 6 MHz, one offset calibration | | 5120 | | µs | $30720/f_{ADC}$ |
| $t_{STAB}$ | Stabilization time | From power down $f_{ADC}$ = 6 MHz | | 100 | | µs | $600/f_{ADC}$, $75/f_{ADC}$ if SLOWCK=1 |
| $t_{STANDBY}$ | Wakeup from standby time | $f_{ADC}$ = 6 MHz | | 50 | | µs | $300/f_{ADC}$ |
| | | $f_{ADC}$ = 1.5 MHz | | 50 | | | $75/f_{ADC}$ if SLOWCK=1 |

**Table 72.    SDADC characteristics  (continued)[1]**

| Symbol | Parameter | Conditions | | | | | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| EO | Offset error | Differential mode | gain =1 | $f_{ADC}$ = 1.5 MHz | VDDSDx = 3.3 | SDVREF+ = 3.3 | | | 110 | uV | after offset calibration |
| | | | | $f_{ADC}$ = 6 MHz | | SDVREF+ = 1.2 | | | 110 | | |
| | | | | | | SDVREF+ = 3.3 | | | 100 | | |
| | | | gain =8 | $f_{ADC}$ = 6 MHz | | SDVREF+ = 1.2 | | | 70 | | |
| | | | | | | SDVREF+ = 3.3 | | | 100 | | |
| | | | | $f_{ADC}$ = 1.5 MHz | | SDVREF+ = 3.3 | | | 90 | | |
| | | Single ended mode | gain =1 | | | SDVREF+ = 1.2 | | | 2100 | | |
| | | | | | | SDVREF+ = 3.3 | | | 2000 | | |
| | | | gain =8 | | | SDVREF+ = 1.2 | | | 1500 | | |
| | | | | | | SDVREF+ = 3.3 | | | 1800 | | |
| Dvoffsettemp | Offset drift with temperature | Differential or single ended mode, gain = 1, VDDSDx = 3.3 V | | | | | | 10 | 15 | uV/K | |
| EG | Gain error | All gains, differential mode, single ended mode | | | | | -2.4 | -2.7 | -3.1 | % | |
| EGT | Gain drift with temperature | gain = 1, differential mode, single ended mode | | | | | | 0 | | ppm/K | |

**Table 72.    SDADC characteristics  (continued)[1]**

| Symbol | Parameter | Conditions | | | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| EL | Integral linearity error | Differential mode | gain =1 | VDDSDx= 3.3 | SDVREF+ = 1.2 | | | 16 | LSB | |
| | | | | | SDVREF+ = 3.3 | | | 14 | | |
| | | | gain =8 | | SDVREF+ = 1.2 | | | 26 | | |
| | | | | | SDVREF+ = 3.3 | | | 14 | | |
| | | Single ended mode | gain =1 | | SDVREF+ = 1.2 | | | 31 | | |
| | | | | | SDVREF+ = 3.3 | | | 23 | | |
| | | | gain =8 | | SDVREF+ = 1.2 | | | 80 | | |
| | | | | | SDVREF+ = 3.3 | | | 35 | | |
| ED | Differential linearity error | Differential mode | gain =1 | VDDSDx= 3.3 | SDVREF+ = 1.2 | | | 2.4 | LSB | |
| | | | | | SDVREF+ = 3.3 | | | 1.8 | | |
| | | | gain =8 | | SDVREF+ = 1.2 | | | 3.6 | | |
| | | | | | SDVREF+ = 3.3 | | | 2.9 | | |
| | | Single ended mode | gain =1 | | SDVREF+ = 1.2 | | | 3.2 | | |
| | | | | | SDVREF+ = 3.3 | | | 2.8 | | |
| | | | gain =8 | | SDVREF+ = 1.2 | | | 4.1 | | |
| | | | | | SDVREF+ = 3.3 | | | 3.3 | | |

**Table 72. SDADC characteristics (continued)[1]**

| Symbol | Parameter | Conditions | | | | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| SNR[4] | Signal to noise ratio | Differential mode | gain =1 | $f_{ADC}$ = 1.5 MHz | SDVREF+ = 3.3[2] | 84 | 85 | | dB | |
| | | | | $f_{ADC}$ = 6 MHz | SDVREF+ = 1.2[3] | 86 | 88 | | | |
| | | | | | SDVREF+ = 3.3 | 88 | 92 | | | |
| | | | gain =8 | $f_{ADC}$ = 6 MHz | SDVREF+ = 1.2[3] | 76 | 78 | | | |
| | | | | | SDVREF+ = 3.3 | 82 | 86 | | | |
| | | Single ended mode | gain =1 | $f_{ADC}$ = 1.5 MHz | SDVREF+ = 3.3[2] | 76 | 80 | | | |
| | | | | $f_{ADC}$ = 1.5MHz | SDVREF+ = 3.3 | 80 | 84 | | | |
| | | | | $f_{ADC}$ = 6 MHz | SDVREF+ = 1.2[3] | 77 | 81 | | | |
| | | | | | SDVREF+ = 3.3 | 85 | 90 | | | |
| | | | gain =8 | $f_{ADC}$ = 6 MHz | SDVREF+ = 1.2[3] | 66 | 71 | | | |
| | | | | | SDVREF+ = 3.3 | 74 | 78 | | | |
| SINAD [4] | Signal to noise and distortion ratio | Differential mode | gain =1 | $f_{ADC}$ = 1.5 MHz | $V_{REF}$ = 3.3[2] | 76 | 77 | | dB | ENOB = SINAD/6.02 -0.292 |
| | | | | $f_{ADC}$ = 6 MHz | $V_{REF}$ = 1.2[3] | 75 | 76 | | | |
| | | | | | $V_{REF}$ = 3.3 | 76 | 77 | | | |
| | | | gain =8 | $f_{ADC}$ = 6 MHz | $V_{REF}$ = 1.2[3] | 70 | 74 | | | |
| | | | | | $V_{REF}$ = 3.3 | 79 | 85 | | | |
| | | Single ended mode | gain =1 | $f_{ADC}$ = 1.5 MHz | $V_{REF}$ = 3.3[2] | 75 | 81 | | | |
| | | | | $f_{ADC}$ = 1.5MHz | $V_{REF}$ = 3.3 | 72 | 73 | | | |
| | | | | $f_{ADC}$ = 6 MHz | $V_{REF}$ = 1.2[3] | 68 | 71 | | | |
| | | | | | $V_{REF}$ = 3.3 | 72 | 73 | | | |
| | | | gain =8 | $f_{ADC}$ = 6 MHz | $V_{REF}$ = 1.2[3] | 60 | 64 | | | |
| | | | | | $V_{REF}$ = 3.3 | 67 | 72 | | | |

Note: The condition VDDSDx = 3.3 spans the SNR block and the SINAD block.

**Table 72. SDADC characteristics (continued)[1]**

| Symbol | Parameter | Conditions | | | | | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| THD[4] | Total harmonic distortion | Differential mode | gain =1 | $f_{ADC}$ = 1.5 MHz | VDDSDx = 3.3 | $V_{REF}$ = 3.3[2] | | -77 | -76 | dB | |
| | | | | $f_{ADC}$ = 6 MHz | | $V_{REF}$ = 1.2[3] | | -77 | -76 | | |
| | | | | | | $V_{REF}$ = 3.3 | | -77 | -76 | | |
| | | | gain =8 | $f_{ADC}$ = 6 MHz | | $V_{REF}$ = 1.2[3] | | -85 | -70 | | |
| | | | | | | $V_{REF}$ = 3.3 | | -93 | -80 | | |
| | | | | $f_{ADC}$ = 1.5 MHz | | $V_{REF}$ = 3.3[2] | | -93 | -83 | | |
| | | Single ended mode | gain =1 | $f_{ADC}$ = 6 MHz | | $V_{REF}$ = 1.2[3] | | -72 | -68 | | |
| | | | | | | $V_{REF}$ = 3.3 | | -74 | -72 | | |
| | | | gain =8 | $f_{ADC}$ = 6 MHz | | $V_{REF}$ = 1.2[3] | | -66 | -61 | | |
| | | | | | | $V_{REF}$ = 3.3 | | -75 | -70 | | |

1. Data based on characterization results, not tested in production.

2. For $f_{ADC}$ lower than 5 MHz, there will be a performance degradation of around 2 dB due to flicker noise increase.

3. If the reference value is lower than 2.4 V, there will be a performance degradation proportional to the reference supply drop, according to this formula: $20*\log10(V_{REF}/2.4)$ dB

4. SNR, THD, SINAD parameters are valid for frequency bandwidth 20Hz - 1kHz. Input signal frequency is 300Hz (for $f_{ADC}$=6MHz) and 100Hz (for $f_{ADC}$=1.5MHz).

**Table 73. VREFSD+ pin characteristics[1]**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | Buffered embedded reference voltage (1.2 V) | | 1.2 | | V | See *Section 6.3.4: Embedded reference voltage on page 56* |
| | | Embedded reference voltage amplified by factor 1.5 | | 1.8 | | | |
| $C_{VREFSD+}$[2] | Reference voltage filtering capacitor | $V_{REFSD+}$ = $V_{REFINT}$ | 1000 | | 10000 | nF | |
| $R_{VREFSD+}$ | Reference voltage input impedance | Fast mode ($f_{ADC}$ = 6 MHz) | | 238 | | kΩ | See RM0313 reference manual for detailed description |
| | | Slow mode ($f_{ADC}$ = 1.5 MHz) | | 952 | | | |

1. Data based on characterization results, not tested in production.

2. If internal reference voltage is selected then this capacitor is charged through internal resistance - typ. 300 ohm. If internal reference source is selected through the reference voltage selection bits (REFV<>"00" in SDADC_CR1 register), the application must first configure REFV bits and then wait for capacitor charging. Recommended waiting time is 3 ms if 1 μF capacitor is used.

# 7 Package characteristics

## 7.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

**Figure 31.   UFBGA100 – ultra fine pitch ball grid array, 7 x 7 mm, 0.50 mm pitch, package outline**
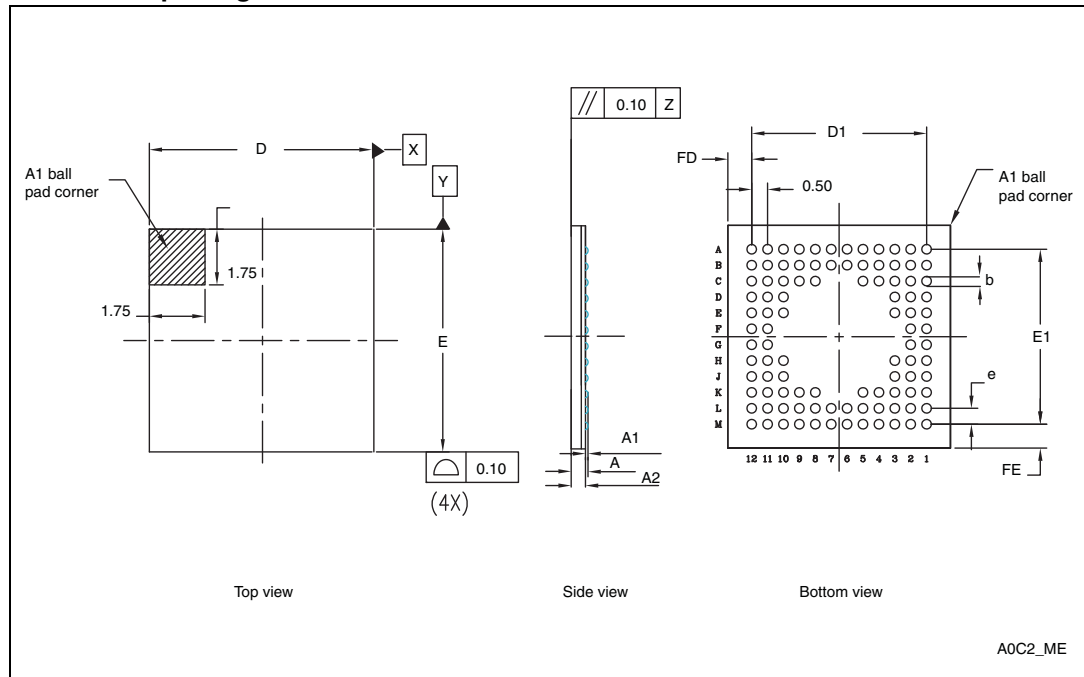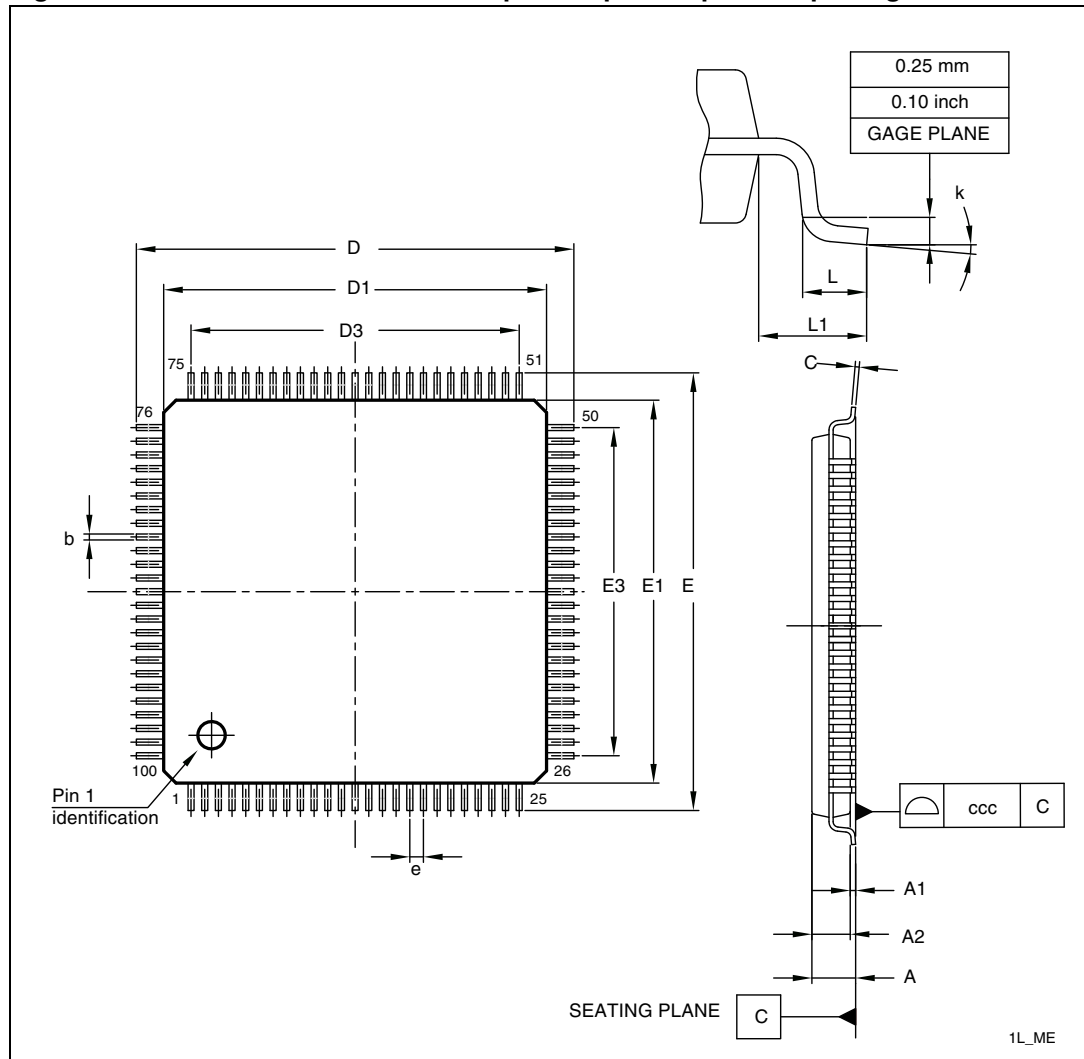


1.   Drawing is not to scale.

**Table 74.   UFBGA100 – ultra fine pitch ball grid array, 7 x 7 mm, 0.50 mm pitch, package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.46 | 0.53 | 0.6 | 0.0181 | 0.0209 | 0.0236 |
| A1 | 0.06 | 0.08 | 0.1 | 0.0024 | 0.0031 | 0.0039 |
| A2 | 0.4 | 0.45 | 0.5 | 0.0157 | 0.0177 | 0.0197 |
| b | 0.2 | 0.25 | 0.3 | 0.0079 | 0.0098 | 0.0118 |
| D | | 7 | | | 0.2756 | |
| D1 | | 5.5 | | | 0.2165 | |
| E | | 7 | | | 0.2756 | |
| E1 | | 5.5 | | | 0.2165 | |
| e | | 0.5 | | | 0.0197 | |
| FD | | 0.75 | | | 0.0295 | |
| FE | | 0.75 | | | 0.0295 | |

1.   Values in inches are converted from mm and rounded to 4 decimal digits.

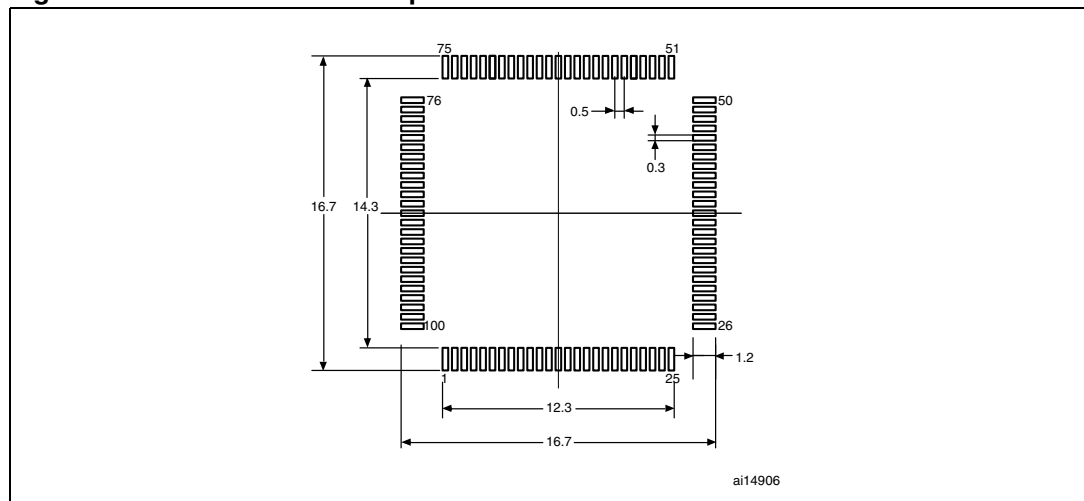**Figure 32. LQFP100 –14 x 14 mm 100-pin low-profile quad flat package outline**



1. Drawing is not to scale.

**Table 75. LQPF100 – 14 x 14 mm 100-pin low-profile quad flat package mechanical data**

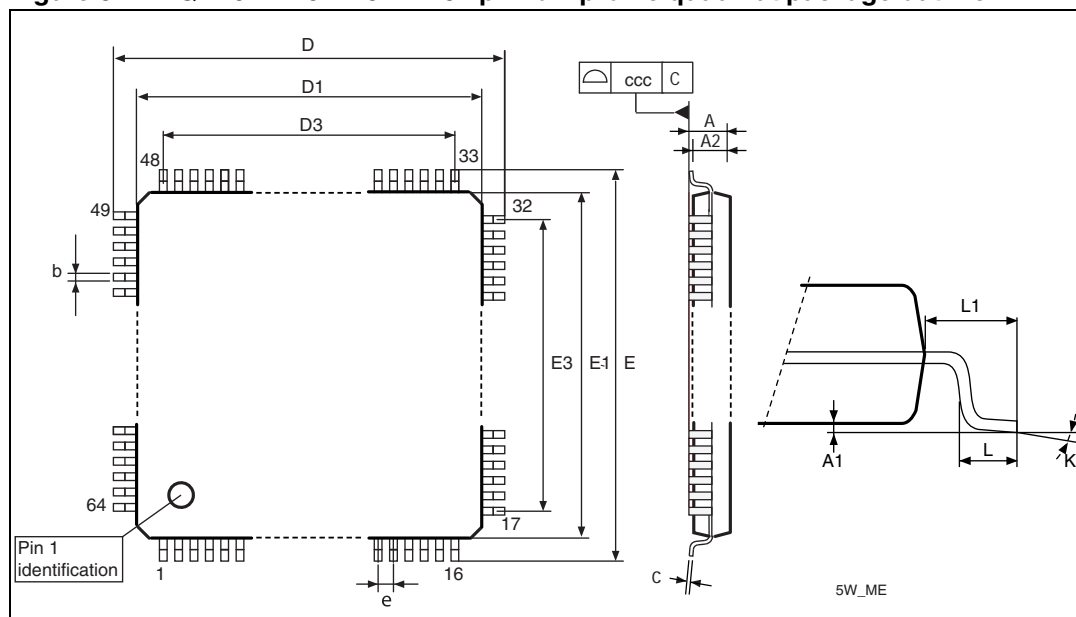| Symbol | millimeters | | | inches[1] | | |
|--------|-----|-----|-----|-----|-----|-----|
| | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** |
| A | | | 1.60 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.0059 |
| A2 | 1.35 | 1.40 | 1.45 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.17 | 0.22 | 0.27 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.09 | | 0.20 | 0.0035 | | 0.0079 |
| D | 15.80 | 16.00 | 16.20 | 0.622 | 0.6299 | 0.6378 |
| D1 | 13.80 | 14.00 | 14.20 | 0.5433 | 0.5512 | 0.5591 |
| D3 | | 12.00 | | | 0.4724 | |
| E | 15.80 | 16.00 | 16.20 | 0.622 | 0.6299 | 0.6378 |
| E1 | 13.80 | 14.00 | 14.20 | 0.5433 | 0.5512 | 0.5591 |
| E3 | | 12.00 | | | 0.4724 | |
| e | | 0.50 | | | 0.0197 | |
| L | 0.45 | 0.60 | 0.75 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.00 | | | 0.0394 | |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | | 0.08 | | | 0.0031 | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 33. Recommended footprint**



1. Dimensions are in millimeters.

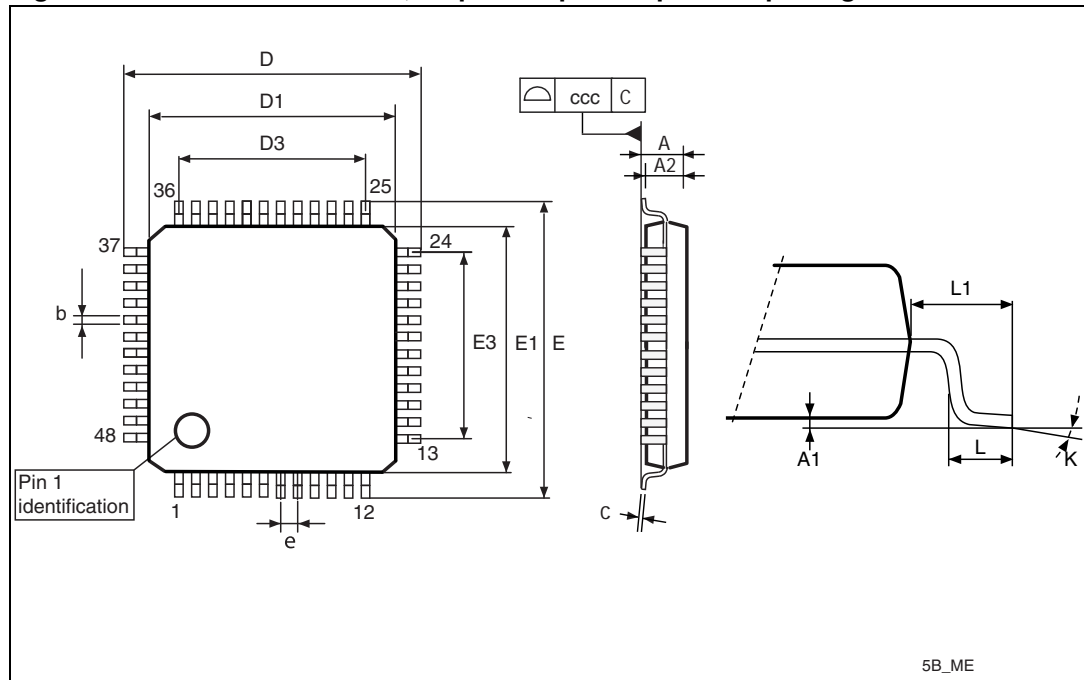**Figure 34.   LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline**



1.   Drawing is not to scale.

**Table 76.   LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.600 | | | 0.0630 |
| A1 | 0.050 | | 0.150 | 0.0020 | | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | | 0.200 | 0.0035 | | 0.0079 |
| D | 11.800 | 12.000 | 12.200 | 0.4646 | 0.4724 | 0.4803 |
| D1 | 9.800 | 10.000 | 10.200 | 0.3858 | 0.3937 | 0.4016 |
| D. | | 7.500 | | | | |
| E | 11.800 | 12.000 | 12.200 | 0.4646 | 0.4724 | 0.4803 |
| E1 | 9.800 | 10.00 | 10.200 | 0.3858 | 0.3937 | 0.4016 |
| e | | 0.500 | | | 0.0197 | |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.450 | 0.600 | 0.75 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.000 | | | 0.0394 | |
| ccc | | 0.080 | | | 0.0031 | |
| N | **Number of pins** | | | | | |
| | 64 | | | | | |

1.   Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 35. Recommended footprint**



1. Dimensions are in millimeters.

**Figure 36. LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package outline**



1. Drawing is not to scale.

**Table 77. LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.600 | | | 0.0630 |
| A1 | 0.050 | | 0.150 | 0.0020 | | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | | 0.200 | 0.0035 | | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | | 5.500 | | | 0.2165 | |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | | 5.500 | | | 0.2165 | |
| e | | 0.500 | | | 0.0197 | |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.000 | | | 0.0394 | |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | | 0.080 | | | 0.0031 | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 37. Recommended footprint**
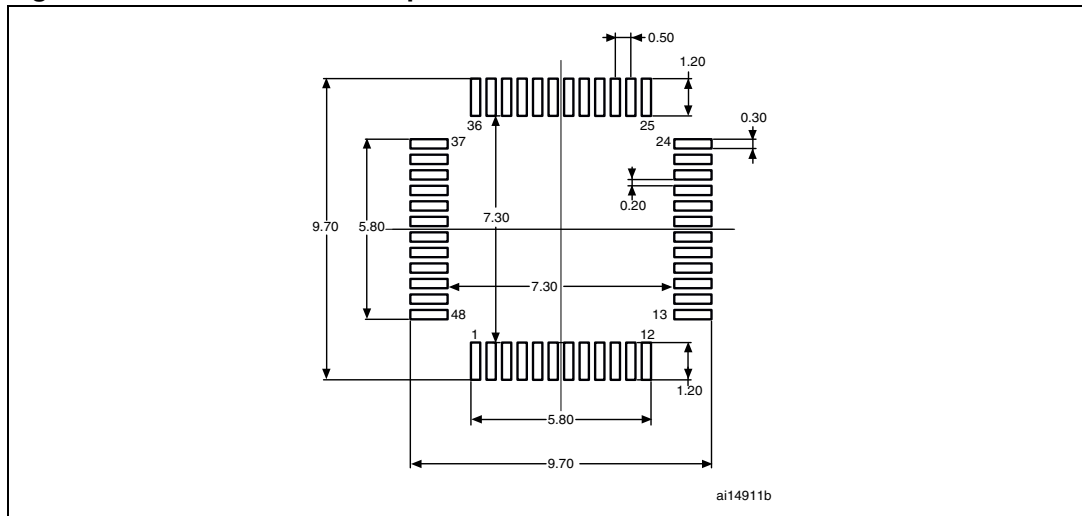


1. Dimensions are in millimeters.

## 7.2 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 24: General operating conditions on page 54*.

The maximum chip-junction temperature, $T_J$ max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

● $T_A$ max is the maximum ambient temperature in °C,

● $\Theta_{JA}$ is the package junction-to-ambient thermal resistance, in °C/W,

● $P_D$ max is the sum of $P_{INT}$ max and $P_{I/O}$ max ($P_D$ max = $P_{INT}$ max + $P_{I/O}$max),

● $P_{INT}$ max is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = $\Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH})$,

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low and high level in the application.

**Table 78.    Package thermal characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | **Thermal resistance junction-ambient**<br>LQFP64 - 10 × 10 mm / 0.5 mm pitch | 45 | °C/W |
| | **Thermal resistance junction-ambient**<br>LQFP48 - 7 × 7 mm | 55 | |
| | **Thermal resistance junction-ambient**<br>LQFP100 - 14 × 14 mm / 0.5 mm pitch | 46 | |
| | **Thermal resistance junction-ambient**<br>BGA100 - 7 x 7 mm | 59 | |

### 7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

### 7.2.2       Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F37x at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

**Example 1: High-performance application**

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax}$ = 82 °C (measured according to JESD51-2), $I_{DDmax}$ = 50 mA, $V_{DD}$ = 3.5 V, maximum 3 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$ = 0.4 V and maximum 2 I/Os used at the same time in output at low level with $I_{OL}$ = 20 mA, $V_{OL}$ = 1.3 V

$P_{INTmax}$ = 50 mA $\times$ 3.5 V= 175 mW

$P_{IOmax}$ = 3 $\times$ 8 mA $\times$ 0.4 V + 2 $\times$ 20 mA $\times$ 1.3 V = 61.6 mW

This gives: $P_{INTmax}$ = 175 mW and $P_{IOmax}$ = 61.6 mW:

$P_{Dmax}$ = 175+ 61.6 = 236.6 mW

Thus: $P_{Dmax}$ = 236.6 mW

Using the values obtained in *Table 78* $T_{Jmax}$ is calculated as follows:

–      For LQFP64, 45°C/W

$T_{Jmax}$ = 82 °C + (45°C/W $\times$ 236.6 mW) = 82 °C + 10.65 °C = 92.65 °C

This is within the range of the suffix 6 version parts (–40 < $T_J$ < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Part numbering*).

**Example 2: High-temperature application**

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature $T_J$ remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax}$ = 115 °C (measured according to JESD51-2), $I_{DDmax}$ = 20 mA, $V_{DD}$ = 3.5 V, maximum 9 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$ = 0.4 V

$P_{INTmax}$ = 20 mA $\times$ 3.5 V= 70 mW

$P_{IOmax}$ = 9 $\times$ 8 mA $\times$ 0.4 V = 28.8 mW

This gives: $P_{INTmax}$ = 70 mW and $P_{IOmax}$ = 28.8 mW:

$P_{Dmax}$ = 70 + 28.8 = 98.8 mW

Thus: $P_{Dmax}$ = 98.8 mW

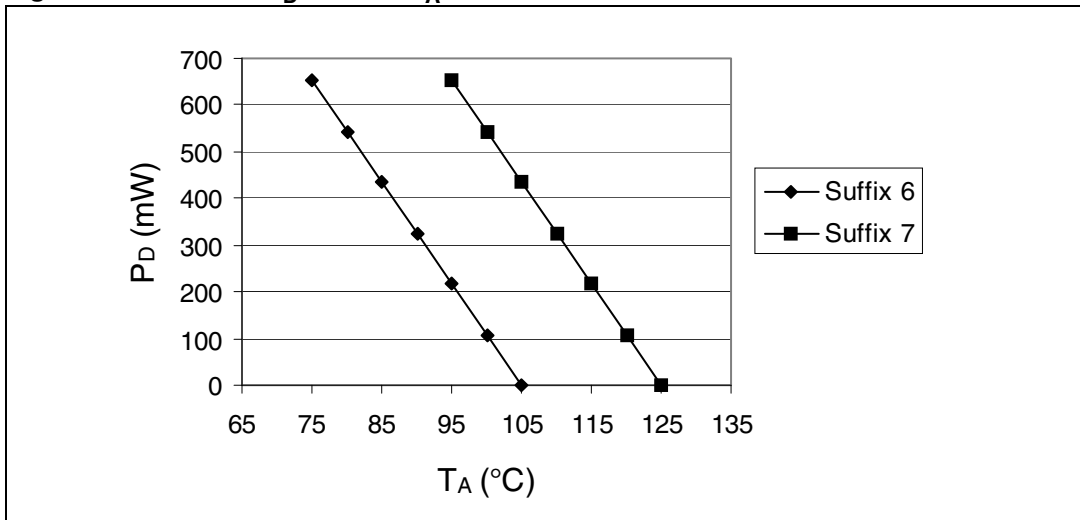Using the values obtained in *Table 78* $T_{Jmax}$ is calculated as follows:

    –   For LQFP100, 46°C/W

$T_{Jmax}$ = 115 °C + (46°C/W × 98.8 mW) = 115 °C + 4.54 °C = 119.5 °C

This is within the range of the suffix 7 version parts (–40 < $T_J$ < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Part numbering*).

**Figure 38. LQFP64 $P_D$ max vs. $T_A$**

# 8　　Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

**Table 79.　Ordering information scheme**

**Example**:　　　　　　　　　　　　　　　　　STM32　F　372　R　8　T　6　x

**Device family**

STM32 = ARM-based 32-bit microcontroller

**Product type**

F = General-purpose

**Sub-family**

372 = STM32F372xx
373 = STM32F373xx

**Pin count**

C = 48 pins
R = 64 pins
V = 100 pins

**Code size**

8 = 64 Kbytes of Flash memory
B = 128 Kbytes of Flash memory
C = 256 Kbytes of Flash memory

**Package**

T = LQFP
H = BGA

**Temperature range**

6 = Industrial temperature range, –40 to 85 °C
7 = Industrial temperature range, –40 to 105 °C

**Options**

xxx = programmed parts
TR = tape and real

# 9 Revision history

**Table 80. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 18-Jun-2012 | 1 | Initial release. |
| 07-Sep-2012 | 2 | Added 'F' to all 'Cortex-M4' occurences<br>Modified the shapes of *Figure 2: STM32F37x LQFP48 pinout* to *Figure 4: STM32F37x LQFP100 pinout*<br>Added two rows 'VREFSD+ - VDDSD3' and 'VREF+ - VDDA' in *Table 21: Voltage characteristics*<br>Removed PB0 in footnote of *Table 21: Voltage characteristics* and in *Section 6.3.13: I/O port characteristics*<br>Added a paragraph after '...power up sequence' in *Table 6.2: Absolute maximum ratings* and after '...in output mode' in *I/O system current consumption*<br>Corrected SDAC_VREF+ in *Figure 9: Power supply scheme*<br>Modified *Table 22: Current characteristics*<br>Added BGA100 in *Table 24: General operating conditions*<br>Added values in *Table 28: Embedded internal reference voltage*<br>Filled values in *Table 29: Typical and maximum current consumption from VDD supply at VDD = 3.6 V*<br>Filled values in *Table 30: Typical and maximum current consumption from VDDA supply*<br>Filled values in *Table 31: Typical and maximum VDD consumption in Stop and Standby modes*<br>Removed table: "Typical and maximum VDDA consumption in Stop modes"<br>Filled values in *Table 32: Typical and maximum VDDA consumption in Stop and Standby modes*<br>Added VBAT values in *Table 33: Typical and maximum current consumption from VBAT supply*<br>Added typ values in *Table 34: Typical current consumption in Run mode, code with data processing running from Flash* and *Table 35: Typical current consumption in Sleep mode, code running from Flash or RAM*<br>Added max value in *Table 39: LSE oscillator characteristics (fLSE = 32.768 kHz)*<br>Modified min and max values in *Table 40: HSI oscillator characteristics*<br>Added values in *Table 42: Low-power mode wakeup timings*<br>Added Class values in *Table 46: EMS characteristics*<br>Modified values in *Table 47: EMI characteristics*<br>Added values in *Table 48: ESD absolute maximum ratings*<br>Added class value in *Table 49: Electrical sensitivities*<br>modified values and descriptions in *Table 50: I/O current injection susceptibility* |

**Table 80.    Document revision history**

| Date | Revision | Changes |
|------|----------|---------|
| 07-Sep-2012 | 2 (cont'd) | Filled values in *Table 68: WWDG min-max timeout value @72 MHz (PCLK)* |
| | | Filled values in *Table 57: SPI characteristics* |
| | | Filled values in *Table 58: I2S characteristics* |
| | | Replaced *Table 59: ADC characteristics* |
| | | Added values in *Table 72: SDADC characteristics* |
| | | Modified footnote in *Table 73: VREFSD+ pin characteristics* |
| | | Replaced 'AIN' with 'SRC' in *Table 60: RSRC max for fADC = 14 MHz* and *Figure 28: Typical connection diagram using the ADC* |
| | | Reordered chapters and Cover page features. |
| | | Added subsection to GPIOS in *Table 2: Device overview* |
| | | Aligned SRAM with USB in *Figure 1: Block diagram* |
| | | Added "Do not reconfigure..." sentence in *Section 3.9: GPIOs (general-purpose inputs/outputs)* |
| | | Added *Table 9: STM32F37x I2C implementation* |
| | | Added *Table 10: STM32F37x USART implementation* |
| | | Merged SPI and I2S into one section |
| | | Reshaped *Figure 5: STM32F37x BGA100 pinout* and removed ADC10 |
| | | Added notes column, modified I/O structure values and pin, function names, removed TIM1_TX & TIM1_RX in *Table 13: STM32F37x pin definitions* |
| | | Added the note "do not reconfigure..." after *Table 13: STM32F37x pin definitions* |
| | | Modified "x_CK" occurences to "I2Sx_CK" in *Table 14: Alternate functions for port PA* to *Table 19: Alternate functions for port PF* |
| | | Added two GP I/Os in *Table 9: Power supply scheme* |
| | | Added Caution after *Table 9: Power supply scheme* |
| | | Added Max values in *Table 25: Operating conditions at power-up / power-down* |
| | | Modified [1] footnote in *Table 26: Embedded reset and power control block characteristics* |
| | | Added row to *Table 28: Embedded internal reference voltage* |
| | | Added the note " It is recommended..." under *Table 50: I/O current injection susceptibility* |
| | | Modified *Table 50: I/O current injection susceptibility* |
| | | Modified temperature and current values in *Section 7.2.2: Selecting the product temperature range* |
| | | Added crystal EPSON-TOYOCOM bullet under *Typical current consumption* |
| | | Modified *Figure 9: Power supply scheme* |
| | | Removed Boot 0 section |
| | | Modified *Table 71: USB: Full-speed electrical characteristics* |

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