



ISSC/台湾创杰，2014 年已并入美国微芯（MICROCHIP，简称 MCHP），多年来专注于蓝牙芯片开发与设计，经过多年耕耘，ISSC 已成为蓝牙芯片领导品牌。

我司是 ISSC 最资深的代理，从卖出 ISSC 品牌的第一颗芯片至今，协助 ISSC 方案为全球用户所熟知和认可，亦辅佐和见证了数家蓝牙成品工厂从初创到跻身为知名企业的成长历程。我司既提供性价比优越和交期及时的 IC 或 Module，也在香港和深圳配备有多名资深软硬件工程师，协助客人进行产品开发和设计，从 PCB layout 到试产、量产的导入，全程提供贴心服务，是蓝牙方案公司或成品工厂的优秀合作伙伴。请保留以下联系方式，欢迎洽询，共襄盛举！

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Bluetooth 4.1 Multimedia SOC

GENERAL DESCRIPTION

IS2020S is a compact, highly integrated, CMOS single-chip RF and baseband IC for preliminary Bluetooth v4.1 with Enhanced Data Rate 2.4GHz applications. This chip is fully compliant with Bluetooth specification and completely backward-compatible with Bluetooth 3.0, 2.0 or 1.2 systems.

It incorporates Bluetooth 1M/2M/3Mbps RF, single-cycle MCU, MODEM, UART interface, and ISSC's own Bluetooth software stack to achieve the required BT v4.1 with EDR functions.

To provide the superior audio and voice quality, it also integrates a DSP co-processor, a PLL, and a CODEC dedicated for voice and audio applications.

For voice, not only the basic CVSD encoding and decoding but also the enhanced noise reduction and echo cancellation are implemented by the built-in DSP to reach the better quality in the both sending and receiving sides. For enhanced audio applications, SBC and AAC (optional) decoding functions can be also carried out by DSP to satisfy Bluetooth A2DP requirements.

In addition, to minimize the external components required for portable devices, a voltage sensor for battery, battery charger, a switching regulator and LDO are integrated to reduce BOM cost for various Bluetooth applications.

FEATURES

- Support preliminary Bluetooth v4.1 function and backward compatible with BT3.0, 2.0 and 1.2.
- ISSC's own Bluetooth software stack for the headset or speaker application. It supports following profiles :
 - Hands Free 1.6
 - Headset 1.1
 - A2DP 1.2
 - AVRCP 1.5
 - SPP 1.0
- Integrated 16/32 bits DSP core running up to 72MHz that supports:
 - Dual microphone noise suppression
 - Echo cancelation
 - SBC/AAC_LC audio format decoding
 - Automatic volume control for speaker output
- Integrated a 20-bit 98dB SNR (A-weighted) stereo DAC
- Connections to two phones with HFP/A2DP profiles
- Built-in four languages (Chinese/ English/ Spanish/ French) voice prompts
- Ultra low power consumption under 10mA for SCO/A2DP link
- Capable charging voltage from an empty battery and sustain a direct DC input voltage up to 7V
- Charging current up to 350mA
- 7 mm x 7 mm 56 QFN package

APPLICATIONS

- Bluetooth stereo headset
- Bluetooth stereo speaker
- Bluetooth stereo speaker phone
- Bluetooth car audio unit

Bluetooth 4.1 Multimedia SOC

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1 Key Features

System Specification

- Compliant with Bluetooth Specification v.4.1 (EDR) in 2.4 GHz ISM band

Baseband Hardware

- 16MHz main clock input
- Built-in internal ROM for program memory
- Support to connect to two hosts (phones, tablets...) with HFP or A2DP profiles simultaneously
- Adaptive Frequency Hopping (AFH) avoids occupied RF channels
- Fast Connection supported

RF Hardware

- Fully Bluetooth 4.1 (EDR) system in 2.4 GHz ISM band.
- Combined TX/RX RF terminal simplifies external matching and reduces external antenna switches.
- Max. +4dBm output power with 20 dB level control from register control.
- Built-in T/R switch for Class 2/3 application
- To avoid temperature variation, temperature sensor with temperature calibration is utilized into bias current and gain control.
- Fully integrated synthesizer has been created. There requires no external VCO, varactor diode, resonator and loop filter.
- Crystal oscillation with built-in digital trimming for temperature/process variations.

Audio processor

- Support 64 kb/s A-Law or μ -Law PCM format, or CVSD (Continuous Variable Slope Delta Modulation) for SCO channel operation.

- Noise suppression for dual analog microphone inputs
- Echo cancelation
- SBC and optional AAC decoding
- Packet loss concealment
- Build-in four languages (Chinese/ English/ Spanish/ French) voice prompts and 20 events for each one

Audio Codec

- 20 bit codec
- 98dB SNR DAC playback
- Dual microphone input
- Integrate headphone amplifier for 16/32 Ω speakers

Peripherals

- Built-in Lithium-ion battery charger
- Integrate 3V, 1.8V LDO and Switching mode regulator
- Built-in ADC for battery monitor and voltage sense.
- Two LED drivers

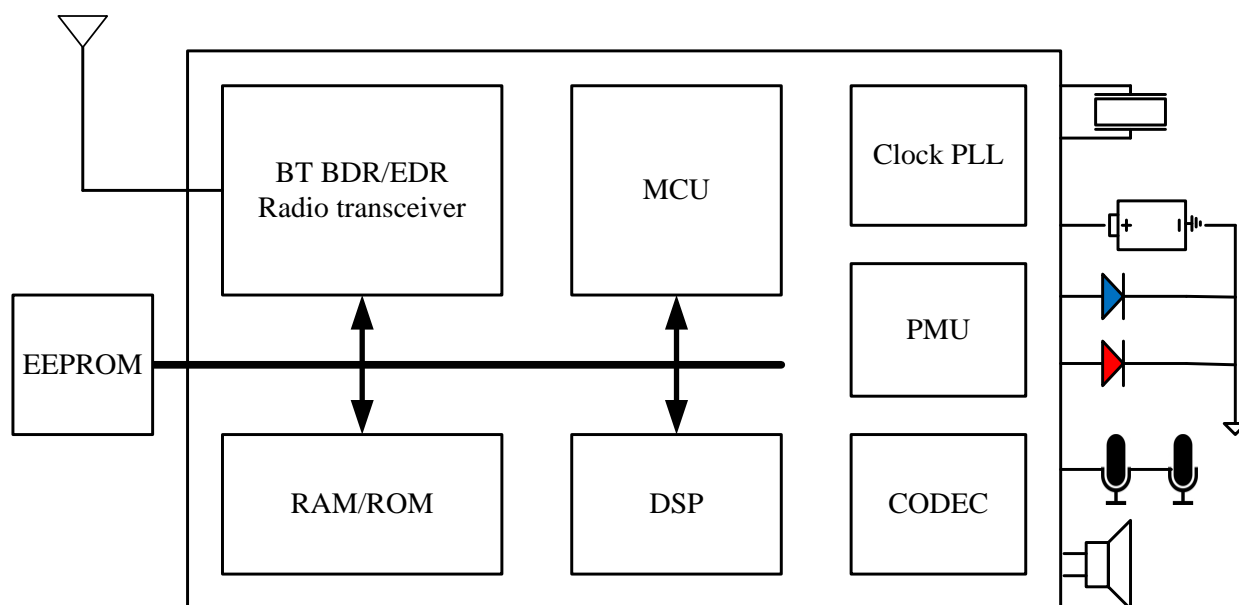
Flexible HCI interface

- High speed HCI-UART (Universal Asynchronous Receiver Transmitter) interface

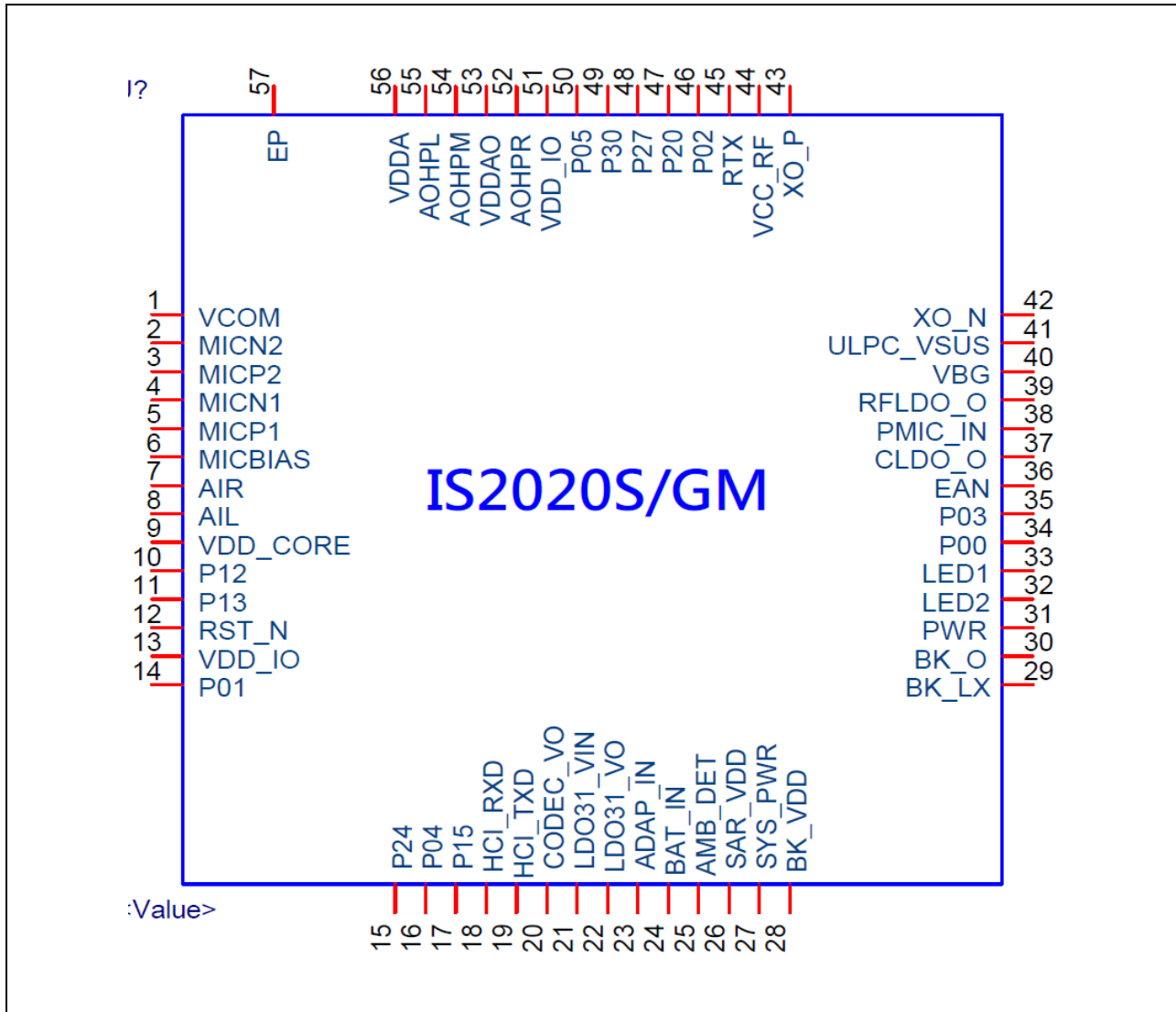
Package

- 7x7mm² 56QFN package

Functional Diagram



2 PIN ASSIGNMENTS



Pin No.	I/O	Pin Name	Pin Descriptions
1	P	VCOM	Internal biasing voltage for CODEC
2	I	MICN2	Mic 2 mono differential analog negative input
3	I	MICP2	Mic 2 mono differential analog positive input
4	I	MICN1	Mic 1 mono differential analog negative input
5	I	MICP1	Mic 1 mono differential analog positive input
6	P	MIC_BIAS	Electric microphone biasing voltage
7	I	AIR	R-channel single-ended analog inputs
8	I	AIL	L-channel single-ended analog inputs
9	P	VDD_CORE	Core 1.2V power input
10	I/O	P1_2	GPIO, default pull-high input 1. KEY PIN for FT Test 2. EEPROM clock SCL 3. Clock signal for OLED
11	I/O	P1_3	GPIO, default pull-high input 1. KEY PIN for FT Test 2. EEPROM data SDA 3. Data signal for OLED
12	I	RST_N	KEY PIN for FT Test System Reset Pin
13	P	VDD_IO	I/O power supply input
14	I/O	P0_1	GPIO, default pull-high input 1. FWD key when class 2 RF 2. Class1 TX Control signal of external TR switch when class 1 RF 3. Serial flash control.
15	I/O	P2_4	GPIO, default pull-high input 1. KEY PIN for FT Test 2. System Configuration, L: Boot Mode with P2_0 low combination
16	I/O	P0_4	GPIO, default pull-high input. 1. NFC detection pin 2. Out_Ind_0

Pin No.	I/O	Pin Name	Pin Descriptions
17	I/O	P1_5	GPIO, default pull-high input 1. NFC detection pin 2. Out_Ind_0 3. Slide Switch Detector.
18	I/O	HCI_RXD	KEY PIN for FT Test HCI RX data
19	I/O	HCI_TXD	KEY PIN for FT Test HCI TX data
20	P	CODEC_VO	3.1V LDO output for CODEC power
21	P	LDO31_VIN	3.1V LDO input
22	P	LDO31_VO	3.1V LDO output
23	P	ADAP_IN	Power adaptor input
24	P	BAT_IN	Battery input
25	P	AMB_DET	ADC analog input 1
26	P	SAR_VDD	SAR 1.8V input
27	P	SYS_PWR	System Power Output
28	P	BK_VDD	Buck VDD Power Input
29	P	BK_LX	Buck feedback input
30	P	BK_O	Buck output
31	I	PWR	Multi-Function Push Button key
32	I	LED2	LED Driver 2
33	I	LED1	LED Driver 1
34	I/O	P0_0	GPIO, default pull-high input 1. Slide Switch Detector. 2. UART TX_IND
35	I/O	P0_3	GPIO, default pull-high input 1. REV key 2. Buzzer Signal Output 3. Out_Ind_1 4. Class1 RX Control signal of external TR switch when class 1 RF 5. Serial flash control.
36	I	EAN	Embedded ROM/External Flash enable H: Embedded; L: External Flash

Pin No.	I/O	Pin Name	Pin Descriptions
37	P	CLDO_O	1.2V core LDO output
38	P	PMIC_IN	PMU blocks power input.
39	P	RFLDO_O	1.28V RF LDO output
40	P	VBG	Bandgap output reference for decoupling interference
41	P	ULPC_VSUS	ULPC 1.2V output power, maximum loading 1mA.
42	I	XO_N	16MHz Crystal input negative
43	I	XO_P	16MHz Crystal input positive
44	RP	VCC_RF	RF power input for both synthesizer and TX/RX block
45	I/O	RTX	RF RTX path
46	I/O	P0_2	GPIO, default pull-high input Play/Pause key as the default setting
47	I/O	P2_0	GPIO, default pull-high input 1. KEY PIN for FT Test 2. System Configuration, H: Application L: Baseband(IBDK Mode)
48	I/O	P2_7	GPIO, default pull-high input Volume up key (default)
49	I/O	P3_0	GPIO, default pull-high input Line-in Detector
50	I/O	P0_5	GPIO, default pull-high input Volume down (default)
51	P	VDD_IO	I/O power supply input
52	O	AOHPR	R-channel analog headphone output
53	P	VDDAO	Positive power supply dedicated to CODEC output amplifiers.
54	O	AOHPM	Headphone common mode output/sense input.
55	O	AOHPL	L-channel analog headphone output
56	P	VDDA	Positive power supply/reference voltage for CODEC
57	P	EP	Exposed pad as ground

3 TRANSCEIVER

IS2020S is design optimized for use in Bluetooth 2.4 GHz system. It contains a complete radio frequency transmitter/receiver section. An internal synthesizer generates a stable clock for synchronize with another device.

TRANSMITTER

The internal PA has a maximum output power of +4dBm with level control 20dB from amplitude control. This is applied into Class2/3 radios without external RF PA.

The transmitter features IQ direct conversion to minimize the frequency drift. And it can excess 30dB power range with temperature compensation machine.

RECEVIER

The LNA operates with TR-combined mode for single port application.

The ADC is utilized to sample input analogue wave to convert into digital for de-modulator analysis. Before the ADC, a channel filter has been integrated into receiver channel that can reduce the external component count and increase the anti-interference capability.

The image rejection filter is to reject image frequency for low-IF architecture. This filter for low-IF architecture is implied to reduce external BPF component for super heterodyne architecture.

There is an RSSI signal to the processor that it can control the power to make a good tradeoff for effective distance and current consumption.

SYNTHESIZER

A synthesizer generates a clock for radio transceiver operation. There is a VCO inside with tunable internal LC tank. It can reduce variation for components. A crystal oscillation with internal digital trimming circuit provides a stable clock for synthesizer.

MODEM

On the Bluetooth v1.2 specification and below, 1 Mbps was the standard data rate based on Gaussian Frequency Shift Keying (GFSK) modulation scheme. This basic rate modem meets BDR requirements of Bluetooth v2.0 with EDR specification.

On the Bluetooth v2.0 with EDR specification, Enhanced Data Rate (EDR) has been introduced to provide 2 and 3 Mbps data rates as well as 1 Mbps. This enhanced data rate modem meets EDR requirements of Bluetooth v2.0 with EDR specification. For the viewpoint of baseband, both BDR and EDR utilize the same 1MHz symbol rate and 1.6 KHz slot rate. For BDR, 1 symbol represents 1 bit. However each symbol in the payload part of EDR packets represents 2 or 3 bits. This is achieved by using two different modulations, $\pi/4$ DQPSK and 8DPSK.

4 MICROPROCESSOR

A single-cycle 8-bit MCU is inside IS2020S to carry out the required Bluetooth protocols. It can run at the range from 16MHz to a higher clock so that MCU firmware can dynamically consider the tradeoff between computing power and power consumption. MCU firmware is implemented in ROM (Read-Only-Memory) to minimize the power consumption of program execution and to save the cost of external flash.

MEMORY

A single-port synchronous interface is provided to memory. There are enough ROM and RAM to fulfill the requirement of processor. In addition, attached to the embedded processor bus are a register bank, a dedicated single-port memory, and flash memory. The processor coordinates all link control procedures and data movement using a set of pointer registers.

EXTERNAL RESET

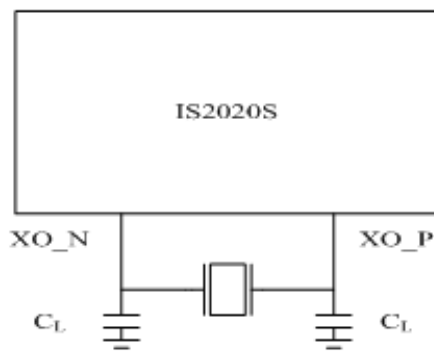
A watchdog timer capable of reset the chip. It has an integrated Power-On Reset (POR) circuit that resets all circuits to a known power-on state. This action can also be driven by an external reset signal that can be used to externally control the device, forcing it into a power-on reset state. The RST signal input is active low and no connection is required in most applications.

REFERENCE CLOCK

IS2020S is composed of an integrated crystal oscillation function. It used a 16 MHz external crystal and two specified load capacitors that a high quality system reference timer source is obtained. This feature is typically used to remove the initial tolerance frequency errors associated with the crystal and its equivalent load capacitance in mass production. Frequency trim is achieved by adjusting the crystal load capacitance through on-chip trim capacitors C_{trim} integrated in chip.

The value of trimming capacitance is around 200fF per LSB at 5 bits word, therefore the overall adjustable clock frequency is around 40 KHz.

$$C_{trim} = 200\text{fF} * (1 \sim 31)$$



5 AUDIO

There are several stages for input and output that all can be programmed for varying gain response characteristics. At the microphone input side, you may use single-end input or differential input. One critical point in maintaining a high quality signal is to provide a stable bias voltage source for the condenser microphone's FET. DC blocking capacitors may be used at both positive and negative sides of input. Internally, this analog signal is converted to 16-bit 8 kHz linear PCM data.

The voice data taken from common memory is converted to an analogue value by a DAC. A multistage amplifier drives the audio signal and provides a differential signal between Line_out+ and Line_out-. The output amplifier is capable of driving a speaker directly if its impedance is 16/32Ω.

DIGITAL SIGNAL PROCESSOR

A digital signal processor (DSP) cooperates with MCU to deal with audio section. It provides audio processing with some advanced features. The DSP includes the capability to cancel the acoustic echo that may be present in a headset or speaker. All processing is performed by a DSP with low power consumption. This technique will most effectively cancel the incoming echo signal without impact to the desired voice signal. An outgoing signal to the speaker which level exceeds a certain threshold (and therefore deemed likely to create echo) will result in suppression of signal along the input path from the microphone. Filtering is also applied and provides for a smoother transition for a more natural user experience.

DUAL MICROPHONE NOISE REDUCTION

This noise reduction technology virtually eliminates distracting background noise, including crowds, wind, vehicles and other interruptions to your conversations. It support dual microphone inputs that one for main vocal input and the other for background noise. Of course, it can use only main vocal input for single microphone application.

CODEC

This built-in codec contains a high Signal/Noise performance. This built-in codec contains a analog to digital converter (ADC), a digital to analog converter (DAC) and additional analog circuitry.

Signal to noise ratio (SNR) is the supreme facts of a CODEC. It provides a very low noise level for background white noise. The main music stream and vocal become clear with this low noise level.

6 POWER MANAGE UNIT

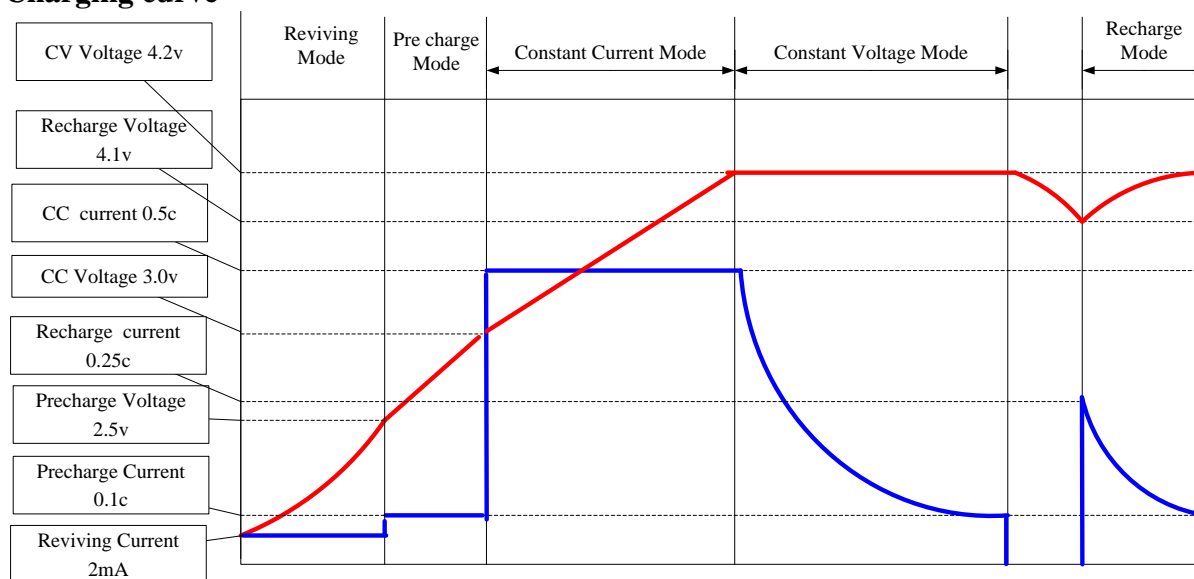
The PMU inside the chip has two main features, charging a Li-ion battery and some regulators for voltage translation. A power switch is used to switch over the power source between battery and adaptor automatically. It also provides two LED drivers.

CHARGING A BATTERY

IS2020S includes a built-in battery charger optimized for use with lithium polymer batteries. The charger features a current sensor for charging control, user programmable current regulation and high accuracy voltage regulation.

The charging current is configured in the EEPROM. Whenever the adaptor is plug-in, charging circuit is active. Reviving, Pre-charging, Constant Current and Constant Voltage modes are implemented and re-charging function is also included. The maximum charging current is 350mA.

Charging curve



VOLTAGE MONITING

A 10-bit Successive-Approximation-Register analog to digital converter (SAR ADC) provides one dedicated channel for battery voltage level detection. The warning level is programmable and stored in the EEPROM. This ADC provides a good resolution that MCU can control the charging process.

VOLTAGE REGULATION

The built-in voltage converter is used to convert the battery or adaptor power for power supply. It also integrates hardware architecture to control power on/off procedure. The built-in programmable LDOs provide power for codec and digital IO pads. It is used to buffer the high

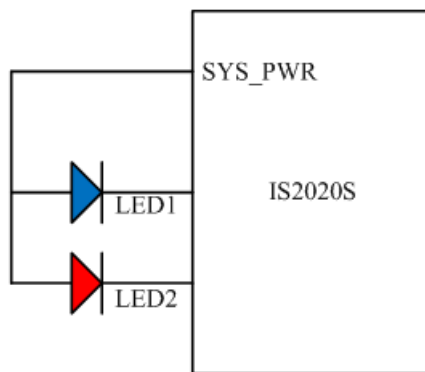
input voltage from battery or adapter. This LDO needs 1uF bypass capacitor.

SWITCHING REGULATOR

There is a bulk voltage convert generating the voltage for RF and baseband core power. This converter has good conversion efficiency to save power and fast transient response.

LED DRIVER

There are two dedicated LED drivers to control the LEDs. They provide enough sink current that LED can be connected directly with IS2020S.



7 GENERAL PURPOSE IOs

IS2020S provides six general purpose IOs for keys setting and saved in the EEPROM. The first button must be power key. The power on/off functions only can be set on MFB pin. There are four different operations for every button. They are short click, long click, double click and combinations.

GPIOs for Buttons

Button Name	Default Functions	GPIO name	Pin
Button 0	Power / MFB	MFB	27
Button 1	Volume UP	P2_7	42
Button 2	Volume DN	P0_5	43
Button 3	PLAY/PAUSE	P0_2	40
Button 4	REV	P0_3	30
Button 5	FWD	P0_1	12

Some signals were generated to indicate or control outside devices. The most popular applications are NFC for easy pairing, external audio amplifier for louder speaker and buzzer for indication.

GPIOs for added functions

Functions	GPIO configurable features	Pins
Slide switch	P0_0	44
Buzzer	P0_4 / P2_0 / P0_3	45 / 41 / 30
NFC detect	P0_4 / P1_5	45 / 13
External AMP enable	P1_6 / P1_5	33 / 13

8 SPECIFICATIONS

Table 1: Absolute Maximum Voltages

Symbol	Parameter	Min	Max	Unit
VDD_CORE	Digital core supply voltage	1.14	1.26	V
AVDD_PLL	PLL supply voltage			
VCC_RF	RF supply voltage	1.28		V
AVDD_SAR	SAR ADC supply voltage	1.62	1.98	V
VDD_AUDIO	CODEC supply voltage	2.7	3.0	V
VDD_IO	I/O supply voltage		3.6	V
BK_VDD	BUCK supply voltage		4.5	V
3V1_VIN	Supply voltage		4.5	V
BAT_IN	Input voltage for battery	3.0	4.5	V
ADP_IN	Input voltage for adaptor	4.5	7.0	V
T _{STORE}	Storage temperature	-40	+85	°C

Table 2: Recommended operate condition

Symbol	Parameter	Min	Typical	Max	Unit
VDD_CORE	Digital core supply voltage	1.14	1.2	1.26	V
AVDD_PLL	PLL supply voltage				
VCC_RF	RF supply voltage		1.28		V
AVDD_SAR	SAR ADC supply voltage	1.62	1.8	1.98	V
VDD_AUDIO	CODEC supply voltage	2.7	2.7	3.0	V
VDD_IO	I/O supply voltage	2.7	3.0	3.3	V
BK_VDD	BUCK supply voltage	3		4.5	V
3V1_VIN	Supply voltage	3		4.5	V
BAT_IN	Input voltage for battery	3		4.2	V
ADP_IN	Input voltage for adaptor	4.5		7	V
T _{STORE}	Storage temperature	-10	+25	+60	°C

Table 3: BUCK switching regulator

Parameter		Min	Typical	Max	Unit
Input Voltage		3.0	3.8	4.5	V
Output Voltage ($I_{load}=70mA$, $V_{in}=4V$)		1.7	1.8	2.05	V
Output Voltage Accuracy			$\pm 5\%$		%
Output Voltage Adjustable Step			50		mV/Step
Output Adjustment Range		-0.1		+0.25	V
Output ripple			10	15	mV _{RMS}
Average Load Current (I_{LOAD})		120			mA
Conversion efficiency (BAT=3.8V, $I_{load} = 50mA$)			88		%
Switching frequency			800		KHz
Quiescent Current				1000	μA
Output Current (peak)		200			mA
Load Regulation ($I_{load} = 10 \sim 100mA$)			1		mV/mA
Line Regulation ($3.2V < V_{in} < 4.2V$)			0.03 (30)		%/V (mV/V)
EN threshold	Logic Low Voltage			0.4	V
	Logic High Voltage	1.62			V
EN current				10	nA
Shutdown Current				<1	μA

Table 4: Low Drop Regulation

Parameter		Min	Typical	Max	Unit
Input Voltage		3.0		4.5	V
Output Voltage	V _{OUT CODEC}		2.9		V
	V _{OUT IO}		1.8		
Output Accuracy (V _{IN} =3.7V, I _{LOAD} =100mA, 27°C)			±5		%
Output current (average)				100	mA
Drop-out voltage (I _{load} = maximum output current)				300	mV
Quiescent Current (excluding load, I _{load} < 1mA)			45		μ A
Load Regulation (I _{load} = 0mA to 100mA)				40	mV
Line Regulation (V _{out} +0.3V<V _{in} <4.5V)			7	10	mV/V
EN threshold	Logic Low Voltage			0.4	V
	Logic High Voltage	1.62			V
EN current				10	nA
Shutdown Current				<1	μ A

Table 5: Battery Charger

Parameter		Min	Typical	Max	Unit
Input Voltage		4.5	5.0	7.0	V
Supply current to charger only			3	4.5	mA
Battery trickle charge current (BAT_IN < trickle charge voltage threshold)			0.1C		mA
Maximum Battery Fast Charge Current Note: ENX2=0	Headroom > 0.7V (ADAP_IN=5V)	170	200	240	mA
	Headroom = 0.3V (ADAP_IN=4.5V)	160	180	240	mA
Maximum Battery Fast Charge Current Note: ENX2=1	Headroom > 0.7V (ADAP_IN=5V)	330	370	420	mA
	Headroom = 0.3V (ADAP_IN=4.5V)	180	220	270	mA
Trickle Charge Voltage Threshold			3		V
Float Voltage		4.158	4.2	4.242	V
Battery Charge Termination Current, (% of Fast Charge Current)			10		%

Note:

(1) C is set in EEPROM

(2) Headroom = $V_{ADAP_IN} - V_{BAT}$

(3) ENX2 is not allowed to be enabled when $V_{ADAP_IN} - V_{BAT} > 2V$

Table 6: LED driver

Parameter	Min	Typical	Max	Unit
Supply Voltage	1.7	1.8	1.98	V
Open-drain Voltage			5.1	V
Open-drain Current			5.5	mA
Intensity Control		16		step
Current Step		0.35		mA
Power Down Open-drain Current			1	μA
Shutdown Current			1	μA

Table 7: Audio codec - Digital to Analogue Converter

T= 25°C, Vdd=3.0V, 1KHz sine wave input, Bandwidth = 20~20KHz				
Parameter (Condition)	Min.	Typ.	Max.	Unit
Over-sampling rate		128		f_s
Resolution	16			Bits
Output Sample Rate	8		48	KHz
Signal to Noise Ratio Note: 1 (SNR @cap-less mode) for 48kHz		96		dB
Signal to Noise Ratio Note: 1 (SNR @single-end mode) for 48kHz		98		dB
Digital Gain	-54		4.85	dB
Digital Gain Resolution		2~6		dB
Analog Gain	-28		3	dB
Analog Gain Resolution		1		dB
Output Voltage Full-scale Swing (AVDD=2.8V)	495	742.5		mV rms
Maximum Output Power (16Ω load)		34.5		mW
Maximum Output Power (32Ω load)		17.2		mW
Allowed Load (Resistive)	8	16	O.C.	Ω
THD+N (16Ω load)			0.05	%
Signal to Noise Ratio (SNR @ 16Ω load)			96	dB

Note: (1) f_{in} =1KHz, B/W=20~20KHz, A-weighted, THD+N < 0.01%, 0dBFS signal, Load=100KΩ

Table 8: Audio codec - Analogue to Digital Converter

T= 25°C, Vdd=3.0V, 1KHz sine wave input, Bandwidth = 20~20KHz					
Parameter (Condition)		Min.	Typ.	Max.	Unit
Resolution			16		Bits
Output Sample Rate		8		48	KHz
Signal to Noise Ratio Note: 1 (SNR @MIC or Line-in mode)	8KHz		88		
	16KHz		88		
	32KHz		88		
	44.1KHz		87		
	48KHz		87		dB
Digital Gain		-54		4.85	dB
Digital Gain Resolution			2~6		dB
MIC Boost Gain			20		
Analog Gain				60	dB
Analog Gain Resolution			2.0		dB
Input full-scale at maximum gain (differential)			4		mV rms
Input full-scale at minimum gain (differential)			800		mV rms
3dB bandwidth			20		KHz
Microphone mode (input impedance)			6	10	KΩ
Microphone mode (input capacitance)				20	pF
THD+N (microphone input) @30mVrms input			0.02		%

Note: (1) f_{in} =1KHz, B/W=20~20KHz, A-weighted, THD+N < 1%, 150mVpp input

Table 9: Transmitter section for BDR

Parameter		Min	Typ	Max	Bluetooth specification	Unit
Maximum RF transmit power			4.0	5.0	-6 to 4	dBm
RF power variation over temperature range with compensation disabled			± 2.0			dB
RF power control range			18		≥ 16	dB
RF power range control resolution			± 0.5			dB
20dB bandwidth for modulated carrier			925		≤ 1000	KHz
ACP Note: $F_0 = 2441\text{MHz}$	$F = F_0 \pm 2\text{MHz}$		-42	-40	≤ -20	dBm
	$F = F_0 \pm 3\text{MHz}$		-49	-48	≤ -40	dBm
	$F = F_0 \pm > 3\text{MHz}$		-57	-53	≤ -40	dBm
$\Delta f_{1\text{avg}}$ maximum modulation		150		165	$140 < \Delta f_{1\text{avg}} < 175$	KHz
$\Delta f_{2\text{max}}$ maximum modulation		120		140	≥ 115	KHz
$\Delta f_{2\text{avg}} / \Delta f_{1\text{avg}}$		0.92	0.94		≥ 0.80	
ICFT		4.5	8	10.5	± 75	KHz
Drift rate		3.3	5	7.0	≤ 20	KHz/50us
Drift (single slot packet)			12		≤ 40	KHz
2 nd harmonic content			-42		≤ -30	dBm
3 rd harmonic content			-45		≤ -30	dBm

Table 10: Transmitter section for EDR

		Min	Typ	Max	Bluetooth specification	Unit
Relative transmit power			-1.2		-4 to 1	dB
$\pi/4$ DQPSK max carrier frequency stability	$ \omega_o $ freq. error		2.5	5	≤ 10 for all blocks	KHz
	$ \omega_i $ initial freq. error		2.5	5	≤ 75 for all blocks	KHz
	$ \omega_o + \omega_i $ block freq. error		5	10	≤ 75 for all blocks	KHz
8DPSK max carrier frequency stability	$ \omega_o $ freq. error		2.5	5	≤ 10 for all blocks	KHz
	$ \omega_i $ initial freq. error		2.5	5	≤ 75 for all blocks	KHz
	$ \omega_o + \omega_i $ block freq. error		5	10	≤ 75 for all blocks	KHz
$\pi/4$ DQPSK modulation accuracy	RMS DEVM		7		≤ 20	%
	99% DEVM		PASS		≤ 30	%
	Peak DEVM			25	≤ 35	%
8DQPSK modulation accuracy	RMS DEVM		7		≤ 13	%
	99% DEVM		PASS		≤ 20	%
	Peak DEVM			20	≤ 25	%
In-band spurious emissions Note: $F_0 = 2441\text{MHz}$	$F > F_0 + 3\text{MHz}$		< -52		≤ -40	dBm
	$F < F_0 - 3\text{MHz}$		< -53		≤ -40	dBm
	$F = F_0 - 3\text{MHz}$		-46		≤ -40	dBm
	$F = F_0 - 2\text{MHz}$		-34		≤ -20	dBm
	$F =$		-34		≤ -26	dBm

	$F_0 - 1\text{MHz}$					
	$F = F_0 + 1\text{MHz}$		-37		≤ -26	dBm
	$F = F_0 + 2\text{MHz}$		-34		≤ -20	dBm
	$F = F_0 + 3\text{MHz}$		-46		≤ -40	dBm
EDR differential phase encoding			100		≥ 99	%

Table 11: Receiver section for BDR

	Frequency (GHz)	Min	Typ	Max	Bluetooth specification	Unit
Sensitivity at 0.1% BER	2.402		-90		≤ -70	dBm
	2.441		-90			
	2.480		-89			
Maximum received signal at 0.1% BER			0	0	≥ -20	dBm
Continuous power required to block Bluetooth reception (for input power of -67dBm with 0.1% BER) measured at the unbalanced port of the balun	0.030–2.000		-7		-10	dBm
	2.000-2.400		-10		-27	
	2.500-3.000		-11		-27	
	3.000-12.75		-7		-10	
C/I co-channel			6		≤ 11	dB
Adjacent channel selectivity C/I Note: $F_0=2441\text{MHz}$	$F = F_0+1\text{MHz}$		-6		≤ 0	dB
	$F = F_0-1\text{MHz}$		-6.5		≤ 0	dB
	$F = F_0+2\text{MHz}$		-36		≤ -30	dB
	$F = F_0-2\text{MHz}$		-28		≤ -9	dB
	$F = F_0-3\text{MHz}$		-31		≤ -20	dB
	$F = F_0+5\text{MHz}$		-48		≤ -40	dB
	$F = F_{\text{image}}$		-28		≤ -9	dB
Maximum level of intermodulation interferers			-37		≥ -39	dBm
Spurious output level			N/A			dBm/Hz

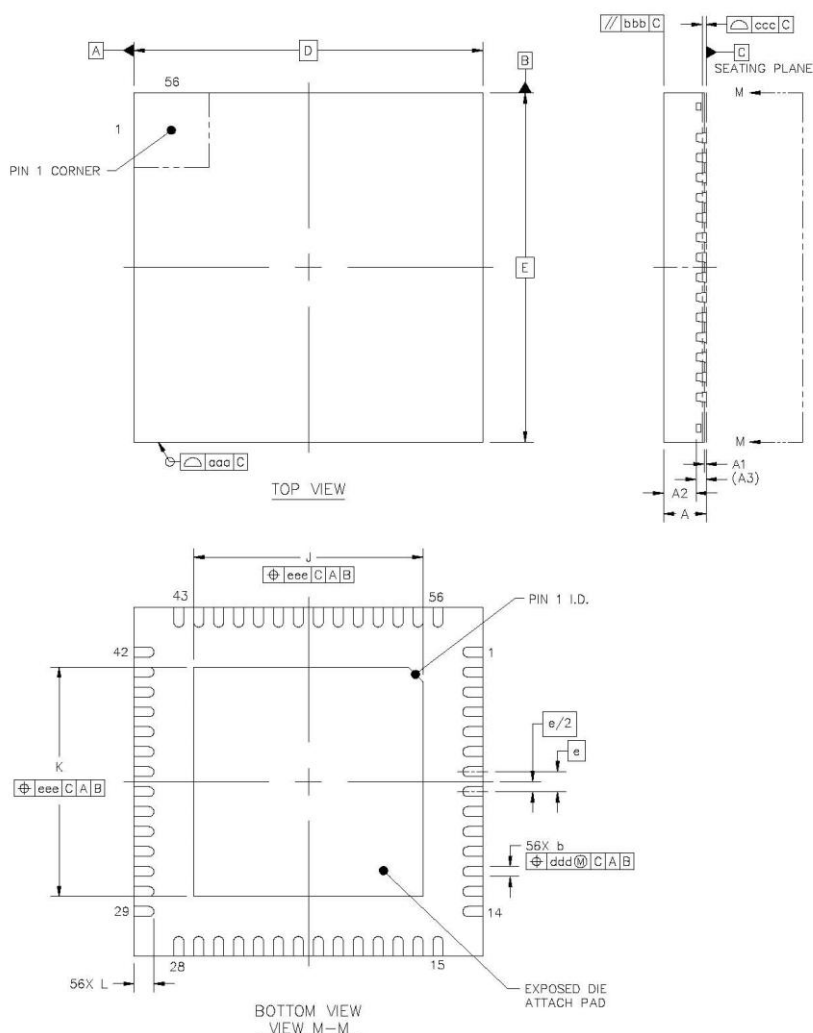
Table 12: Receiver section for EDR

	Freq. (GHz)	Modulation	Min	Typ	Max	Bluetooth specification	Unit
Sensitivity at 0.01% BER	2.402	$\pi/4$ DQPSK		-90		≤ -70	dBm
	2.441	$\pi/4$ DQPSK		-90			
	2.480	$\pi/4$ DQPSK		-89			
	2.402	8DPSK		-83		≤ -70	dBm
	2.441	8DPSK		-83			
	2.480	8DPSK		-82			
Maximum received signal at 0.1% BER		$\pi/4$ DQPSK		-10		≥ -20	dBm
		8DPSK		-10		≥ -20	
C/I co-channel at 0.1% BER		$\pi/4$ DQPSK		5		≤ 13	dB
		8DPSK		5		≤ 21	dB
Adjacent channel selectivity C/I	F = $F_0 + 1\text{MHz}$	$\pi/4$ DQPSK		-11		≤ 0	dB
		8DPSK		-5		≤ 5	dB
	F = $F_0 - 1\text{MHz}$	$\pi/4$ DQPSK		-8		≤ 0	dB
		8DPSK		-4		≤ 5	dB
	F = $F_0 + 2\text{MHz}$	$\pi/4$ DQPSK		-38.5		≤ -30	dB
		8DPSK		-33.5		≤ -25	dB
	F = $F_0 - 2\text{MHz}$	$\pi/4$ DQPSK		-29		≤ -7	dB
		8DPSK		-25		≤ 0	dB
	F = $F_0 - 3\text{MHz}$	$\pi/4$ DQPSK		-32.5		≤ -20	dB
		8DPSK		-27		≤ -13	dB
	F = $F_0 + 5\text{MHz}$	$\pi/4$ DQPSK		-49.5		≤ -40	dB

Note:
 $F_0 = 2441\text{MHz}$

		8DPSK		-43.5		≤ -33	dB
	$F = F_{\text{image}}$	$\pi/4$ DQPSK		-29		≤ -7	dB
		8DPSK		-25		≤ 0	dB

9 PACKAGE



		SYMBOL	MIN		NOM	MAX
TOTAL THICKNESS		A	0.8		0.85	0.9
STAND OFF		A1	0		0.035	0.05
MOLD THICKNESS		A2	---		0.65	0.67
L/F THICKNESS		A3	0.203 REF			
LEAD WIDTH		b	0.15		0.2	0.25
BODY SIZE	X	D	7 BSC			
	Y	E	7 BSC			
LEAD PITCH		e	0.4 BSC			
EP SIZE	X	J	4.5	4.6	4.7	
	Y	K	4.5	4.6	4.7	
LEAD LENGTH		L	0.35	0.4	0.45	
PACKAGE EDGE TOLERANCE		aaa	0.1			
MOLD FLATNESS		bbb	0.1			
COPLANARITY		ccc	0.08			
LEAD OFFSET		ddd	0.1			
EXPOSED PAD OFFSET		eee	0.1			