



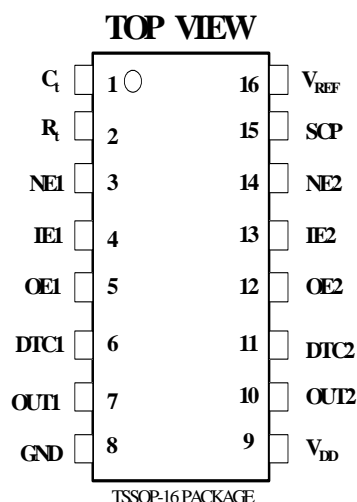
Details are subject to change without notice

## 2-CHANNEL SWITCHING REGULATOR

### FEATURES

- Complete PWM Power Control Circuitry
- Precision Reference :  $2.5V \pm 1\%$  ( $25^{\circ}C$ )
- Under-Voltage Lockout (UVLO) Protection
- Open Drain Output
- Output Short Circuit Protection
- Low Dissipation Current : 1.6mA
- Dead-Time Control : 0 % to 100%
- Wide Operating Frequency :  
10kHz to 800kHz
- $V_{DD}$  Range : 4.0V to 14.0V

### PIN CONFIGURATION



### GENERAL DESCRIPTION

The AAT1343 provides an integrated two-channel pulse-width-modulation (PWM) solution for the power supply of DC-DC system; this device offers the systems engineer flexibility to tailor-make the power supply circuitry for specific applications. Each channel contains its own error amplifier, PWM comparator, dead-time control (DTC) and output driver. The under-voltage protection, oscillator, short circuit protection and voltage reference circuit are the common features for these two channels.

Both channels of AAT1343 can be used for DC-DC converter operations including step-up, step-down, and inverting. Dead-time control can be set to provide 0% to 100% dead-time through a resistive divider network. Soft-start can be implemented by paralleling the DTC resistor with a capacitor. Two dead-time control inputs are assigned for channel 1 (CH1) and channel 2 (CH2) individually, and dead-time control inputs can be used to control on / off operation.

With a minimal number of external components, the AAT1343 offers a simple and cost effective solution.



## PIN DESCRIPTION

PIN NO.	NAME	I/O	DESCRIPTION
1	$C_t$	I	External Timing Capacitor
2	$R_t$	I	External Timing Resistor
3	NE1	I	Noninverting Input of Error Amplifier 1
4	IE1	I	Inverting Input of Error Amplifier 1
5	OE1	I	Output of Error Amplifier 1
6	DTC1	I	Output 1 Dead-Time / Soft-Start Setting
7	OUT1	O	Output 1
8	GND		Ground
9	$V_{DD}$	I	Power Supply
10	OUT2	O	Output 2
11	DTC2	I	Output 2 Dead-Time / Soft-Start Setting
12	OE2	I	Output of Error Amplifier 2
13	IE2	I	Inverting Input of Error Amplifier 2
14	NE2	I	Noninverting Input of Error Amplifier 2
15	SCP	I	Timer Latch Setting
16	$V_{REF}$	O	Reference Voltage (2.5V) Output



## ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{DD}$	14.0	V
Input Voltage (IE –, DTC)	$V_I$	$V_{DD}$	V
Output Voltage	$V_O$	$V_{DD}+0.3$	V
Output Current	$I_O$	120	mA
Operating Free-Air Temperature Range	$T_C$	– 20 to + 85	°C
Storage Temperature Range	$T_{storage}$	– 45 to + 125	°C
Power Dissipation	$P_d$	500	mW

## RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	SYMBOL	MIN	MAX	UNIT
Supply Voltage, $V_{DD}$	$V_{DD}$	4.0	14.0	V
Input Voltage at IE1 and IE2	$V_{cm}$	0.5	1.6	V
Output Voltage	$V_O$	0	$V_{DD}$	V
Oscillation (OSC) Capacitance	$C_{OSC}$	100	15,000	pF
Oscillation (OSC) Resistance	$R_{OSC}$	5.1	50.0	k $\Omega$
Oscillation (OSC) Frequency	$f_{OSC}$	10	800	kHz
Output Current, $I_{OUT1}$ , $I_{OUT2}$	$I_O$	-	100	mA
Operating Free-Air Temperature	$T_C$	– 20	85	°C

**ELECTRICAL CHARACTERISTICS,  $V_{DD} = 6.0V$  (UNLESS OTHERWISE SPECIFIED) (SEE NOTE 1)****OSCILLATOR**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Frequency	$f_{OSC}$	$C_{OSC} = 220pF$ , $R_{OSC} = 10k\Omega$	320	400	480	kHz
Frequency Changes with $V_{DD}$	$f_{\Delta V}$	$V_{DD} = 4.0V$ to $14.0V$ , $T_C = 25^\circ C$ , $C_{OSC} = 220pF$ , $R_{OSC} = 10k\Omega$	-	1	-	%

**UNDER VOLTAGE PROTECTION**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Upper Threshold Voltage	$V_{UPH}$	$T_C = 25^\circ C$	2.6	2.9	3.2	V
Lower Threshold Voltage	$V_{UPL}$	$T_C = 25^\circ C$	2.23	2.53	2.83	V
Hysteresis ( $V_{UPH} - V_{UPL}$ )	$V_{HYS}$	$T_C = 25^\circ C$	-	0.37	-	V

**SHORT CIRCUIT PROTECTION CONTROL**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Input Threshold Voltage	$V_{r1}$	CH1, CH2	0.95	1.05	1.15	V
Short-Circuit Detection Threshold Voltage	$V_{r2}$		1.48	1.64	1.80	V
SCP Terminal Source Current	$I_{SCP}$		-3.5	-2.5	-1.5	$\mu A$
Stand-by Voltage	$V_{STB}$		-	50	100	mV
Latch Voltage	$V_{LT}$		-	30	100	mV

Note 1: Typical values of all parameters are specified at  $T_C = 25^\circ C$ .

**ELECTRICAL CHARACTERISTICS,  $V_{DD} = 6.0V$  (UNLESS OTHERWISE SPECIFIED) (SEE NOTE 1) (CONT.)****REFERENCE VOLTAGE**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Reference Voltage	$V_{REF}$	$I_{REF} = -1mA$ , $T_C = 25^\circ C$	2.480	2.505	2.530	V
Input Voltage Regulation	$V_{RI}$	$I_{REF} = -1mA$ , $V_{DD} = 4.0V$ to $14.0V$	-	1	5	mV
Output Voltage Regulation	$V_{RO}$	$I_{REF} = -0.1mA$ to $-3.0mA$	-	1	10	mV

**EA (ERROR AMPLIFIER)**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Input Offset Voltage	$V_{IO}$	CH1, CH2, Unity Gain	-	-	6	mV
Input Bias Current	$I_{IB}$	CH1, CH2	-	$\pm 15$	$\pm 100$	nA
Input Voltage Range	$V_{IR}$	CH1, CH2	0.5	-	1.6	V
Open-Loop Voltage Gain	$A_{VO}$		70	85	-	dB
Output Voltage Swing	$V_{OS+}$		2.3	2.5	-	V
	$V_{OS-}$		-	0.7	0.9	
Output Sink Current	$I_{OS+}$	OE=1.25V	3	20	-	mA
Output Source Current	$I_{OS-}$	OE=1.25V	-75	-45	-	$\mu A$
Common-Mode Rejection Ratio	CMRR		60	80	-	dB

**ELECTRICAL CHARACTERISTICS,  $V_{DD} = 6.0V$  (UNLESS OTHERWISE SPECIFIED) (SEE NOTE 1) (CONT.)****DEAD-TIME CONTROL & PWM**

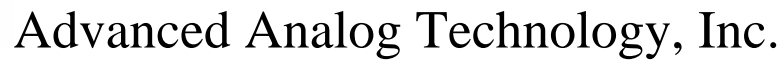
PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Input Bias Current	$I_{IB}$	$V_{DTC} = 2.0V$	-	0.1	1.0	$\mu A$
Input Threshold Voltage (DTC)	$V_{d0}$	Duty = 0%, $f_{OSC} = 10kHz$	1.87	1.97	2.07	V
	$V_{d100}$	Duty = 100%, $f_{OSC} = 10kHz$	1.38	1.48	1.58	
Latch Input Voltage	$V_{DTC}$	$I_{DTC} = 40\mu A$	2.28	2.48	-	V
Latch Mode Source Current	$I_{DTC}$	DTC1, DTC2 = 0V	-560	-200	-	$\mu A$

**OUTPUT STAGE**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Saturation Voltage	$V_{SAT}$	$I_O = 75mA$ ( CH1, CH2 )	-	0.8	1.2	V
Leakage Current	$I_{LEAK}$	$V_O = 14.0V$	-	-	5	$\mu A$

**OPERATING CURRENT**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Supply Current	$I_{DD-OFF}$	Output "OFF" State	-	1.3	1.8	mA
	$I_{DD-ON}$	$R_{OSC} = 10k\Omega$	-	1.6	2.3	mA

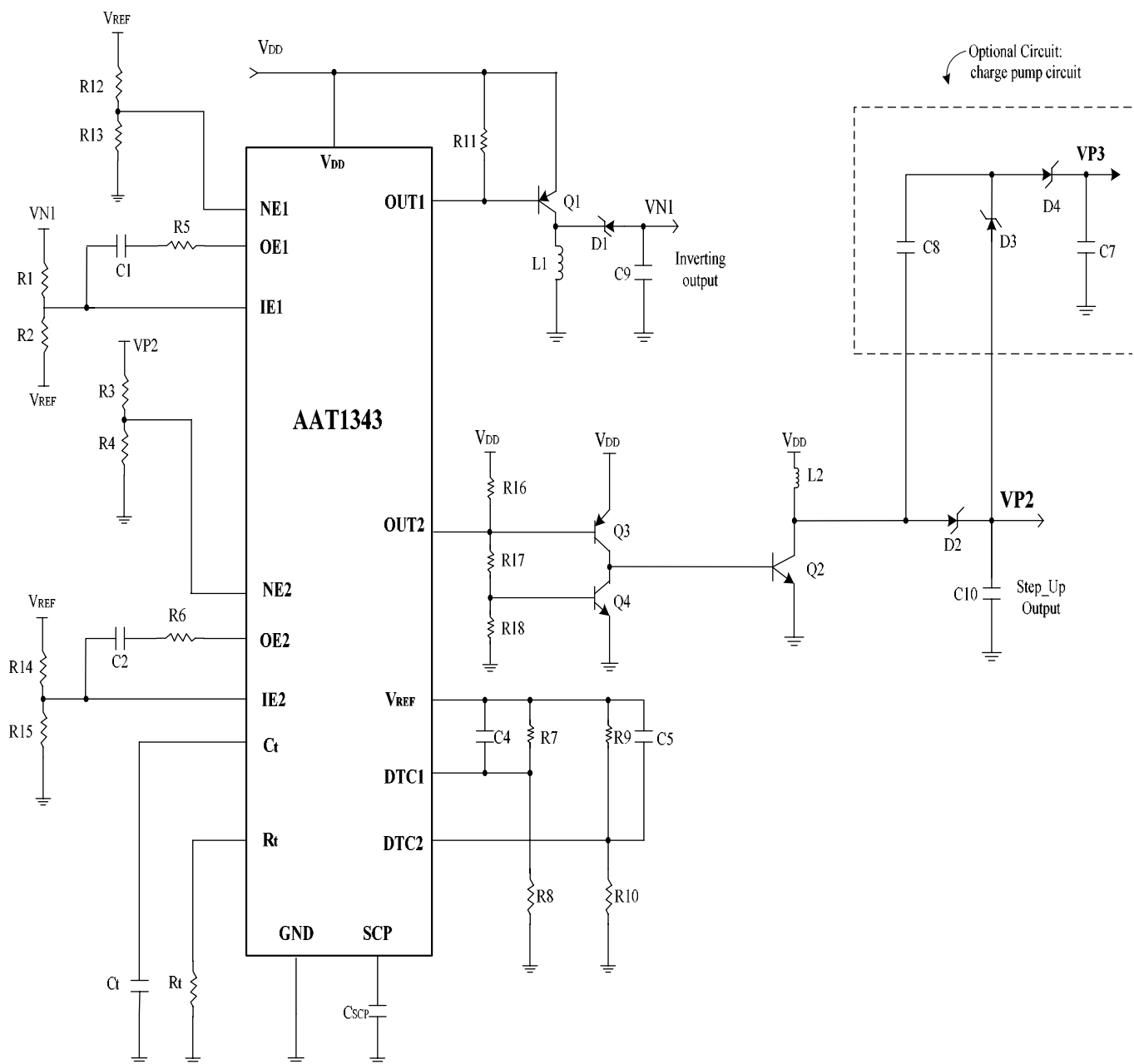


## BLOCK DIAGRAM





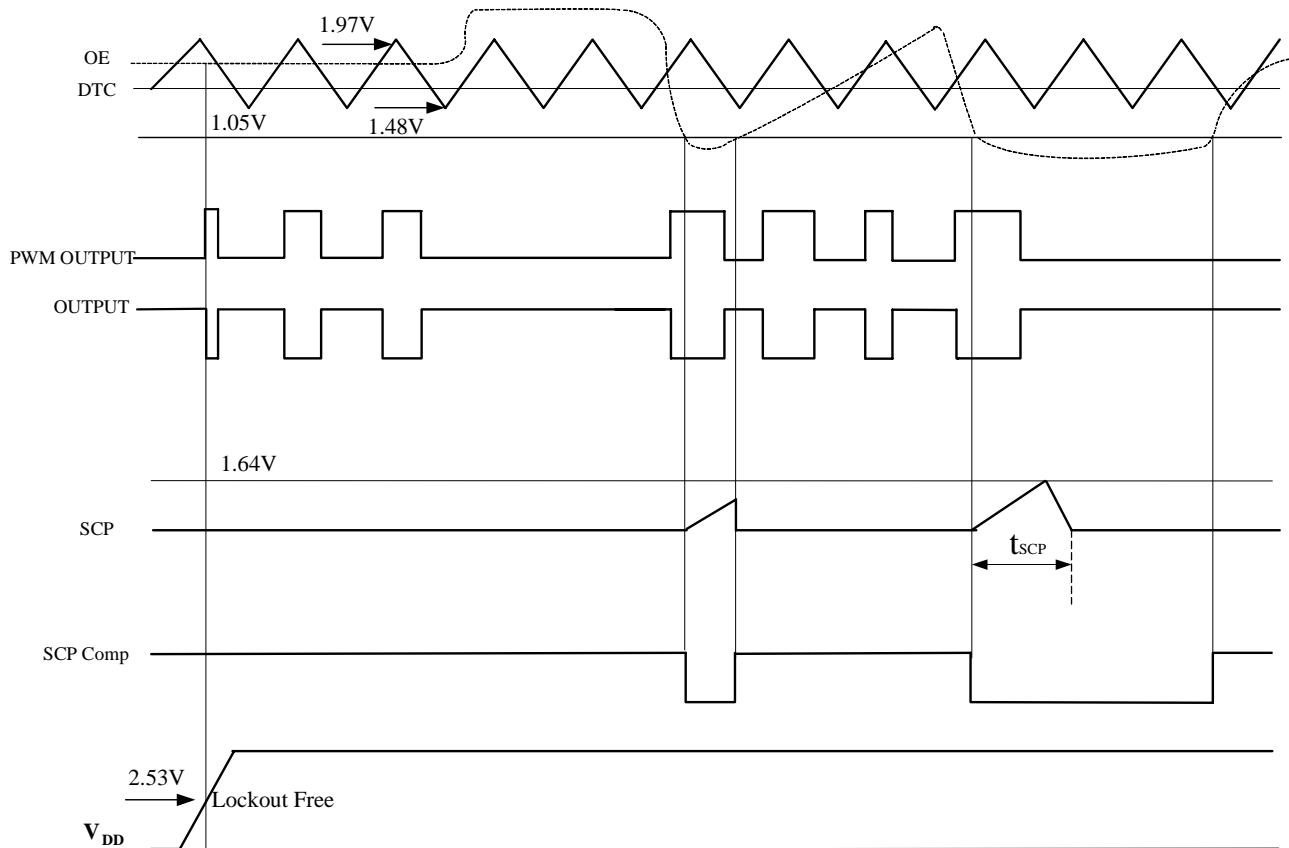
# APPLICATION CIRCUIT







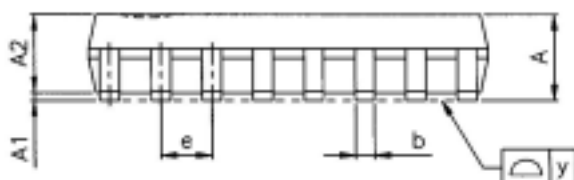
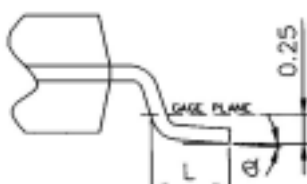
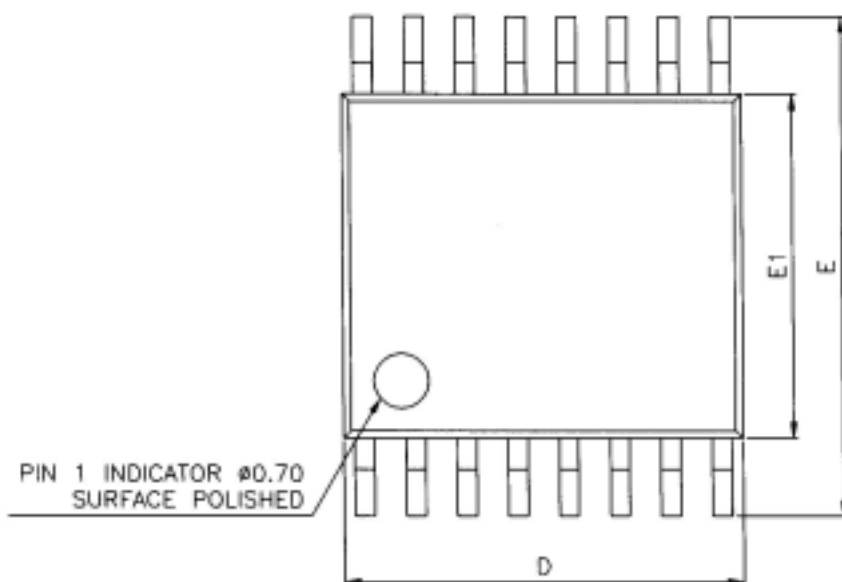
## TIMING CHART



Note:  $t_{SCP} \cong \frac{C_{SCP} V_{r2}}{I_{SCP}}$

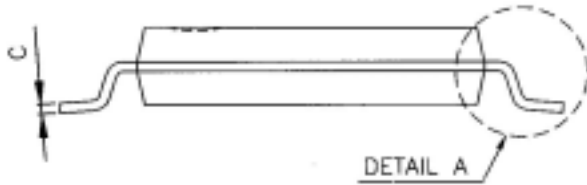


**PACKAGE DIMENSION**  
**16-PIN TSSOP**





**PACKAGE DIMENSION (CONT.)**



SYMBOLS	DIMENSIONS IN MILLIMETERS			DEMINSIONS IN INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A	1.05	1.10	1.20	0.041	0.043	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	-----	1.00	1.05	-----	0.039	0.041
b	0.20	0.25	0.28	0.008	0.010	0.011
C	-----	0.127	-----	-----	0.005	-----
D	4.900	5.075	5.100	0.1930	0.1998	0.2000
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.170	0.173	0.177
e	-----	0.65	-----	-----	0.026	-----
L	0.50	0.60	0.70	0.020	0.024	0.028
y	-----	-----	0.076	-----	-----	0.003
θ	0°	4°	8°	0°	4°	8°

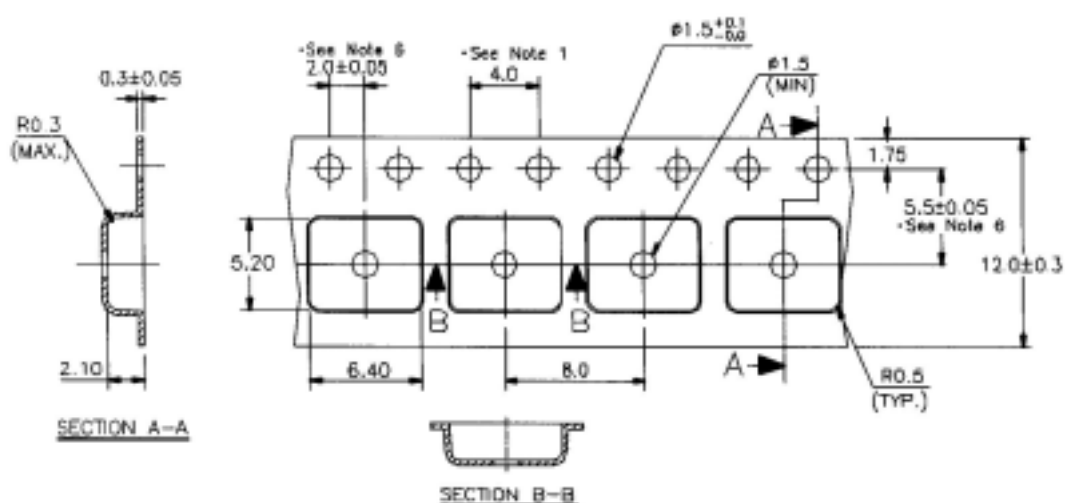
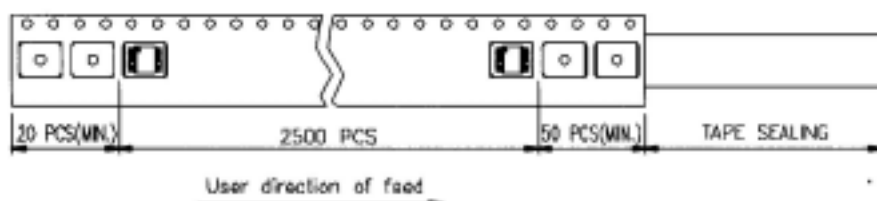
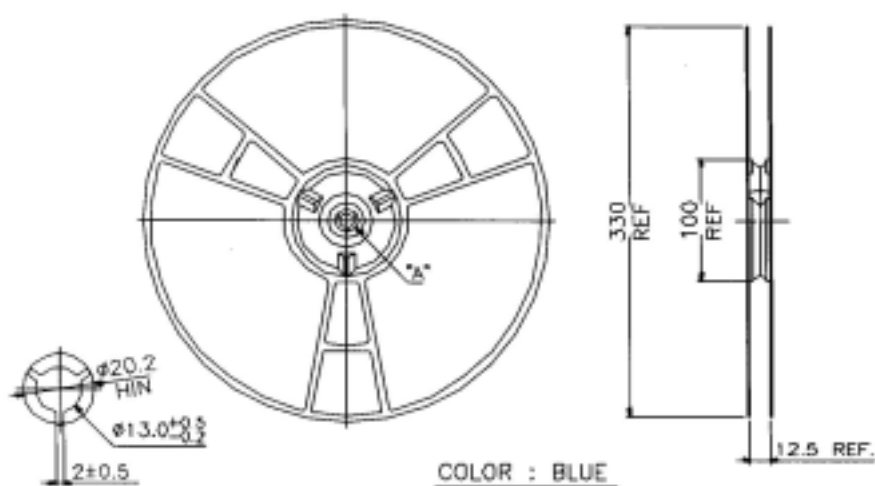
**NOTE:**

1. CONTROLLING DIMENSION: MILLIMETERS
2. LEAD FRAME MATERIAL: OLIN C7025/EFTEC 64T
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006" [0.15 MILLIMETERS] PER END. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" [0.25 MILLIMETERS] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003" [0.08 MILLIMETERS] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028" [0.07 MILLIMETERS].
5. TOLERANCE:  $\pm 0.010$  [0.25 MILLIMETERS] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT: JEDEC SPEC MO-153.



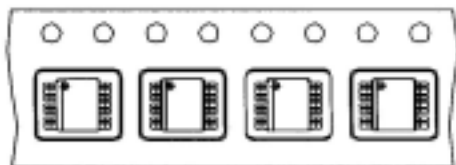
**TAPE AND REEL**

**PACKING METHOD: 2,500PCS/REEL, 1 REEL/BOX**





## TAPE AND REEL (CONT.)



TSSOP 14L / 16L

### NOTE:

1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE  $\pm 0.2$  MILLIMETERS.
2. CAMBER NOT TO EXCEED 1 MILLIMETER IN 100 MILLIMETERS.
3. MATERIAL: ANTI-STATIC BLACK ADVANTEK POLYSTYRENE.
4.  $A_0$  AND  $B_0$  MEASURED ON A PLANE 0.3 MILLIMETERS ABOVE THE BOTTOM OF THE POCKET.
5.  $K_0$  MEASURED FROM A PLANE ON THE INSIDE BOTTOM OF THE POCKET TO THE TOP SURFACE OF THE CARRIER.
6. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.

## PART MARKING

### TSSOP16 TOP MARKING

AAT1343  
XXXXXX

### TSSOP16 BACK MARKING

YYWW



ORDERING INFORMATION

