

MOS FIELD EFFECT TRANSISTOR μ PA2463T1Q

N-CHANNEL MOS FIELD EFFECT TRANSISTOR FOR SWITCHING

DESCRIPTION

The μ PA2463T1Q is a switching device, which can be driven directly by a 2.5 V power source.

The μ PA2463T1Q features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power switch of portable machine and so on.

FEATURES

- 2.5 V drive available
- · Low on-state resistance

RDS(on)1 = $20.0 \text{ m}\Omega$ MAX. (Vgs = 4.5 V, ID = 3.0 A)

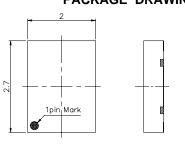
 $R_{DS(on)2} = 21.0 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 4.0 \text{ V, ID} = 3.0 \text{ A)}$

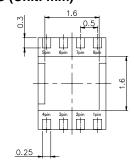
 $R_{DS(on)3} = 24.0 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 3.1 \text{ V, Ip} = 3.0 \text{ A)}$

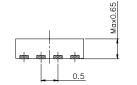
 $R_{DS(on)4} = 28.5 \text{ m}\Omega \text{ MAX.} \text{ (VGS} = 2.5 \text{ V, ID} = 3.0 \text{ A)}$

• Built-in G-S protection diode against ESD

PACKAGE DRAWING (Unit: mm)







1,2,3 : Source 1 4 : Gate 1 6,7,8 : Source 2 5 : Gate 2

Lead surface metal is Gold. Hatching area is Cu.

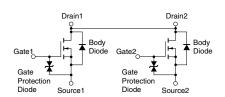
ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

VDSS	20.0	V
Vgss	±12.0	V
ID(DC)	$\pm~6.0$	Α
D(pulse)	± 50	Α
P _{T1}	1.0	W
Tch	150	°C
Tstg	-55 to +150	°C
	VGSS ID(DC) ID(pulse) PT1 Tch	VGSS ± 12.0 ID(DC) ± 6.0 ID(pulse) ± 50 PT1 1.0 Tch 150

Notes 1. Mounted on FR-4 board of 25.4mm \times 25.4mm \times 0.8mmt

2. PW \leq 10 μ s, Duty Cycle \leq 1%

EQUIVALENT CIRCUIT



ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
μ PA2463T1Q-E1-A ^{Note}	Au	Reel	
μ PA2463T1Q-E2-A ^{Note}		3000 p/reel	8PIN HUSON (2720)

Note Pb-free (This product does not contain Pb in the external electrode and other parts.)

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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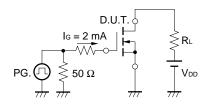
ELECTRICAL CHARACTERISTICS (TA = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 20.0 V, V _{GS} = 0 V			1.0	μΑ
Gate Leakage Current	Igss	V _{GS} = ±12.0 V, V _{DS} = 0 V			±10.0	μΑ
Gate to Source Cut-off Voltage	V _{GS(off)}	Vps = 10.0 V, lp = 1.0 mA	0.50		1.50	V
Forward Transfer Admittance Note	yfs	V _{DS} = 10.0 V, I _D = 3.0 A	T.B.D.			S
Drain to Source On-state Resistance Note	RDS(on)1	Vgs = 4.5 V, ID = 3.0 A	12.0	16.0	20.0	mΩ
	RDS(on)2	Vgs = 4.0 V, ID = 3.0 A	13.0	16.5	21.0	mΩ
	RDS(on)3	Vgs = 3.1V, ID = 3.0 A	13.5	18.0	24.0	mΩ
	RDS(on)4	V _G S = 2.5 V, I _D = 3.0 A	15.0	21.0	28.5	mΩ
Input Capacitance	Ciss	Vps = 10.0 V,		540		pF
Output Capacitance	Coss	V _G S = 0 V,		105		pF
Reverse Transfer Capacitance	Crss	f = 1.0 MHz		25		pF
Turn-on Delay Time	td(on)	VDD = 10.0 V,		T.B.D.		us
Rise Time	tr	ID = 3.0 A,		T.B.D.		us
Turn-off Delay Time	td(off)	Vgs = 4.0 V,		T.B.D.		us
Fall Time	tr	$R_G = 6 \Omega$		T.B.D.		us
Total Gate Charge	Q _G	VDD = 16.0 V,		6.0		nC
Gate to Source Charge	Q _G s	Vgs = 4.0 V,		1.5		nC
Gate to Drain Charge	Q _{GD}	ID = 6.0A		2.5		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	IF = 6.0 A, VGS = 0 V		0.82		V

Note Pulsed: PW \leq 350 μ s, Duty Cycle \leq 2%

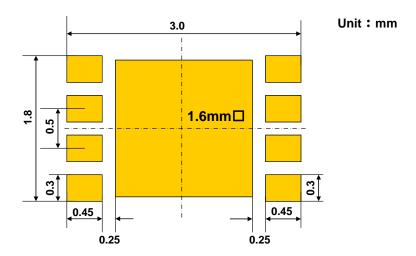
TEST CIRCUIT 1 SWITCHING TIME

TEST CIRCUIT 2 GATE CHARGE



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(Mount Pad Design example)



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