EE288 Data Conversions/Analog Mixed-Signal ICs
Spring 2020

Project Description

May 11, 2020

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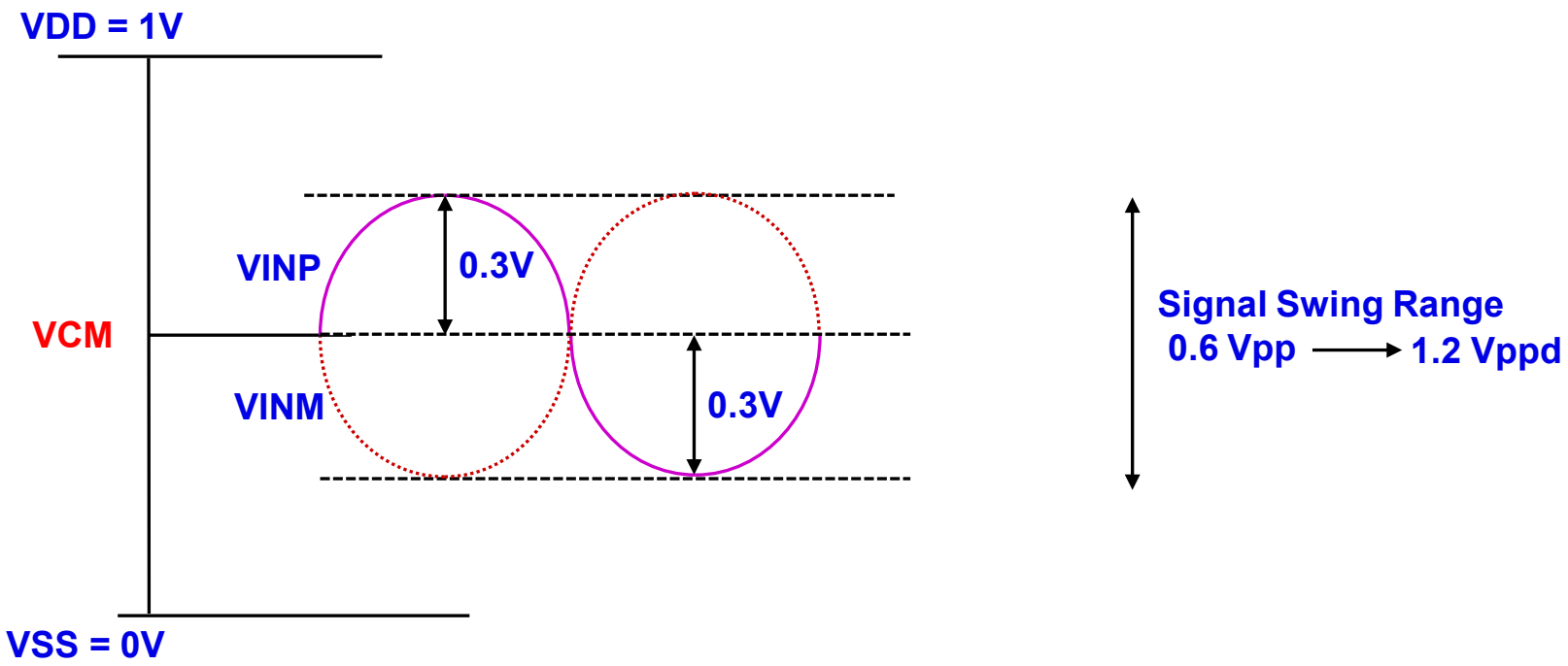
ENG-259

Target Spec

You may not be able to meet all the target spec.
Do your best to meet the spec as much as you can.

▪ Process Technology	45nm CMOS with 1V device only
▪ Supply Voltage	VDD = 1V
▪ Resolution	8 bits
▪ Sampling Rate, fs	10 MS/s
▪ Input Range, VFS	1.2 Vppd
▪ Input Frequency	(7/64)*fs MHz
▪ Input Clock, MCLK	100 MHz with 0.1ns rise and fall time
▪ Walden FoM	10 fJ/conversion-step

Differential Input Signal



Project Logistic

- Due May 16, 11PM
- 2 students per group
- Single student per group is fine
- Reference schematics: Async_SAR_ADC_tb2 in 288lib
- Score - 25% of the total course score
  - Report in IEEE format & neatness 20%
  - Verilog-A code for every block 20%
  - Clear Transistor level schematics 20%
  - Functionality and performance 20%
    - Design1CIDxxyy.tbz2 file will be used to check the circuit function
  - Additional effort and creativity 20%

Project Submission

Report file - EE288ReportCIDxxyy.pdf

- Prepare your project report in IEEE 2-column Word format
- Total pages should be between 4 and 6 pages
- Include the following sections in the report
  Abstract, Introduction, Circuit Design, Simulation Results, Conclusions, References

Slide file - EE288SlideCIDxxyy.pdf

- Include as many additional pages as you like in power point slide format
- Include Verilog-A codes, schematics, simulation setup and results

Design file - Design1CIDxxyy.tbz2

- Create Design1.tbz2 and rename it to Design1CIDxxyy.tbz2
- See the instruction described in EE288_Design_file_for_Instructor_Review.pdf

Submission

- Upload 3 files to Canvas by 11PM on the due date
- File name:
  - EE288ReportCIDxxyy.pdf
  - EE288SlideCIDxxyy.pdf
  - Design1CIDxxyy.tbz2

    where xx and yy are CIDs of your group

Implementation Detail

- Architecture
  - Fully-differential Asynchronous SAR
  - Top-plate sampling with monotonic switching scheme
  - Use VDD as VREF
  - Assume 100MHz Ideal clock with reasonable clock edges
- Capacitive DAC
  - Optimize the unit capacitor value based on kT/C noise, mismatch, and other considerations
  - Optimize the top plate parasitic capacitor value, CH
  - Choose switches based on RC delay, linearity, and switching scheme to optimize power
- Comparator
  - Design comparator based on the offset you can tolerate for the SAR ADC
  - You must simulate the comparator separately to ensure functionality
- Asynchronous clock generator
  - You should optimize the delay timing between Clkc and Valid
  - You can try a different asynchronous circuit to optimize the overall design
- SAR Logic
  - You should implement the SAR logic in Verilog code first and then in transistor level

Simulations

- Run at the following simulation condition
  - Process TT
  - Voltage 1 V
  - Temperature 27 C

- Use an ideal DAC to create FFT spectrum of the ADC with an input frequency of (7/64)*fs MHz

- Report dynamic and static performance as well as ADC figure of merit based on FoM = Power / (fs x 2^EBOB)

References

1. Olga Kardonik, *MS Thesis, University of Texas, Austin*, A study of SAR ADC and implementation of 10-bit asynchronous design, 2013

2. Albert Hsu Ting Chang, *PhD Thesis, MIT*, Low-power high-performance SAR ADC with redundancy and digital background calibration, 2013

3. C. Liu, S. Chang, G. Huang, Y. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, pp. 731–740, April 2010

4. Pieter Harpe, Cui Zhou, et. al. "A 26 W 8 bit 10 MS/s asynchronous SAR ADC for low energy radios," *IEEE J. Solid-State Circuits*, pp. 1585–1595, July 2011

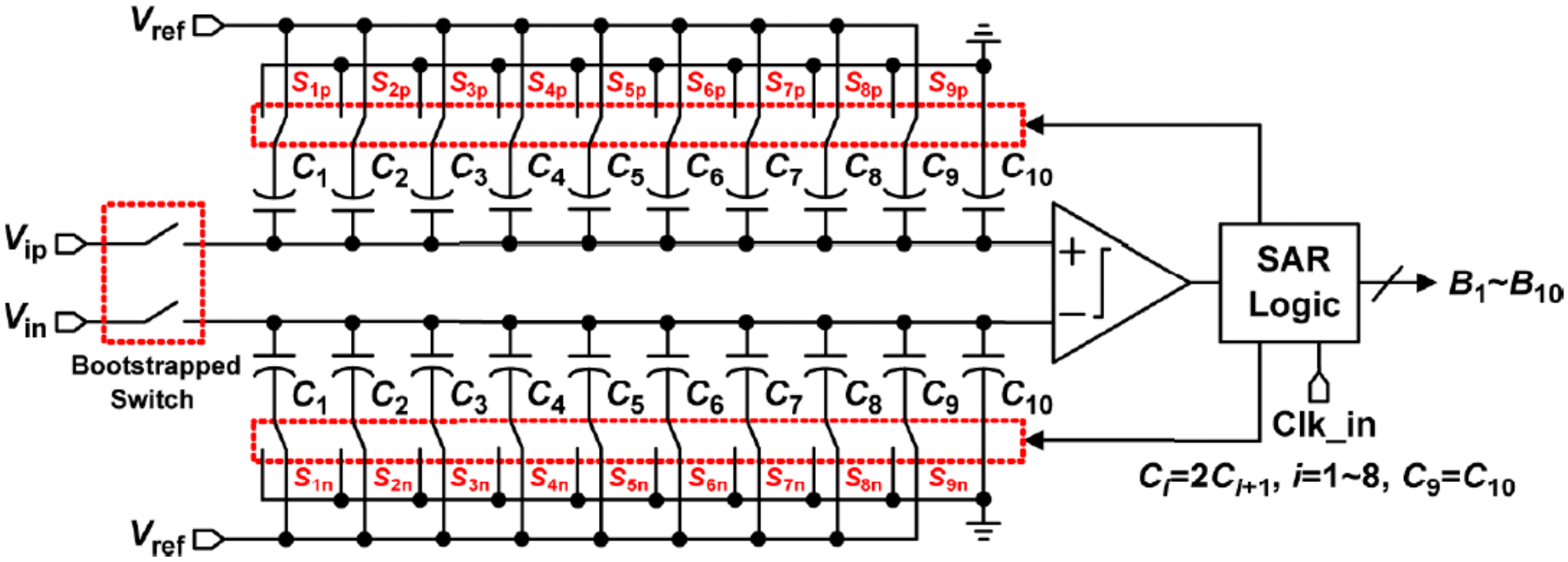
5. T. Cao, S. Aunet, T. Ytterdal, "A 9-bit 50MS/s asynchronous SAR ADC in 28nm CMOS," NORCHIP 2012

6. Brian P. Ginsburg and Anantha P. Chandrakasan, "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC," *IEEE ISCAS* 2005

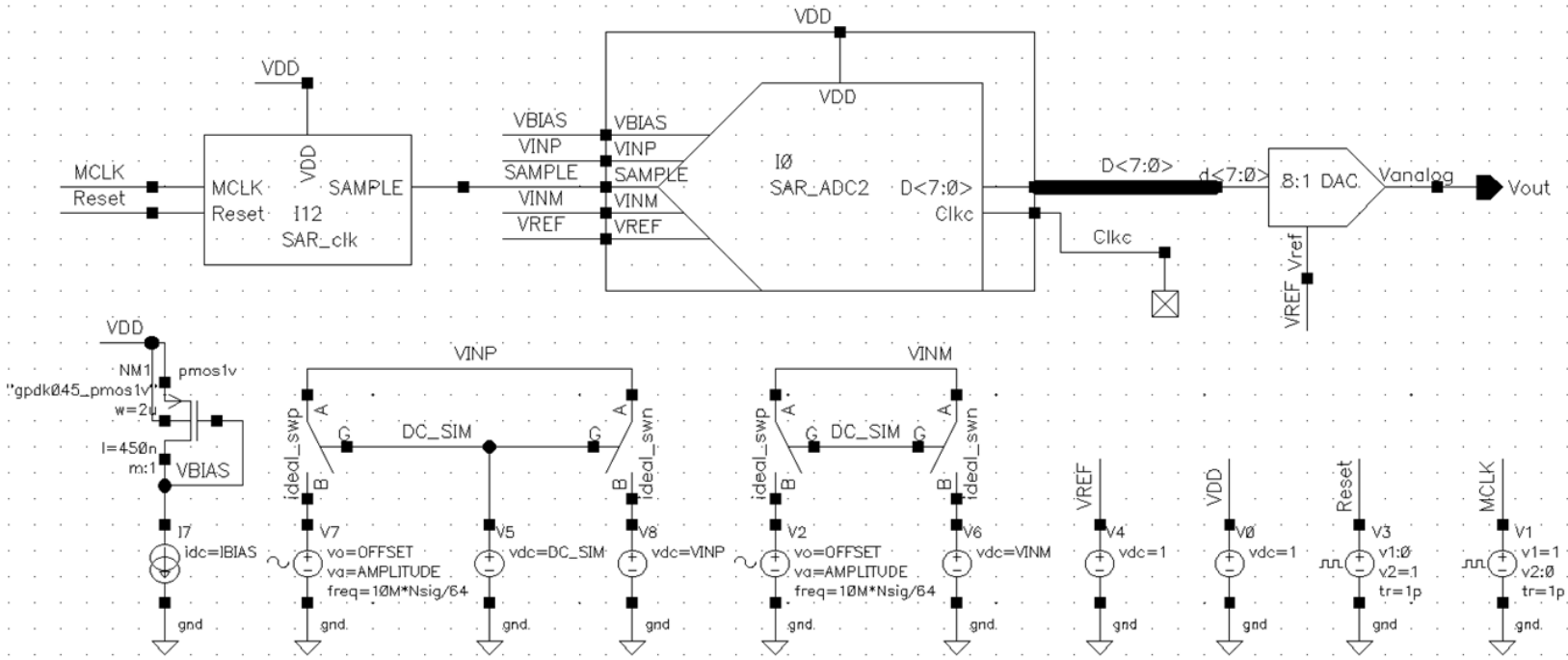
7. Victor Gylling, *MS Thesis, Lund University, Sweden*, Implementation of a 200 MSps 12-bit SAR ADC, 2015

10-bit SAR ADC Example

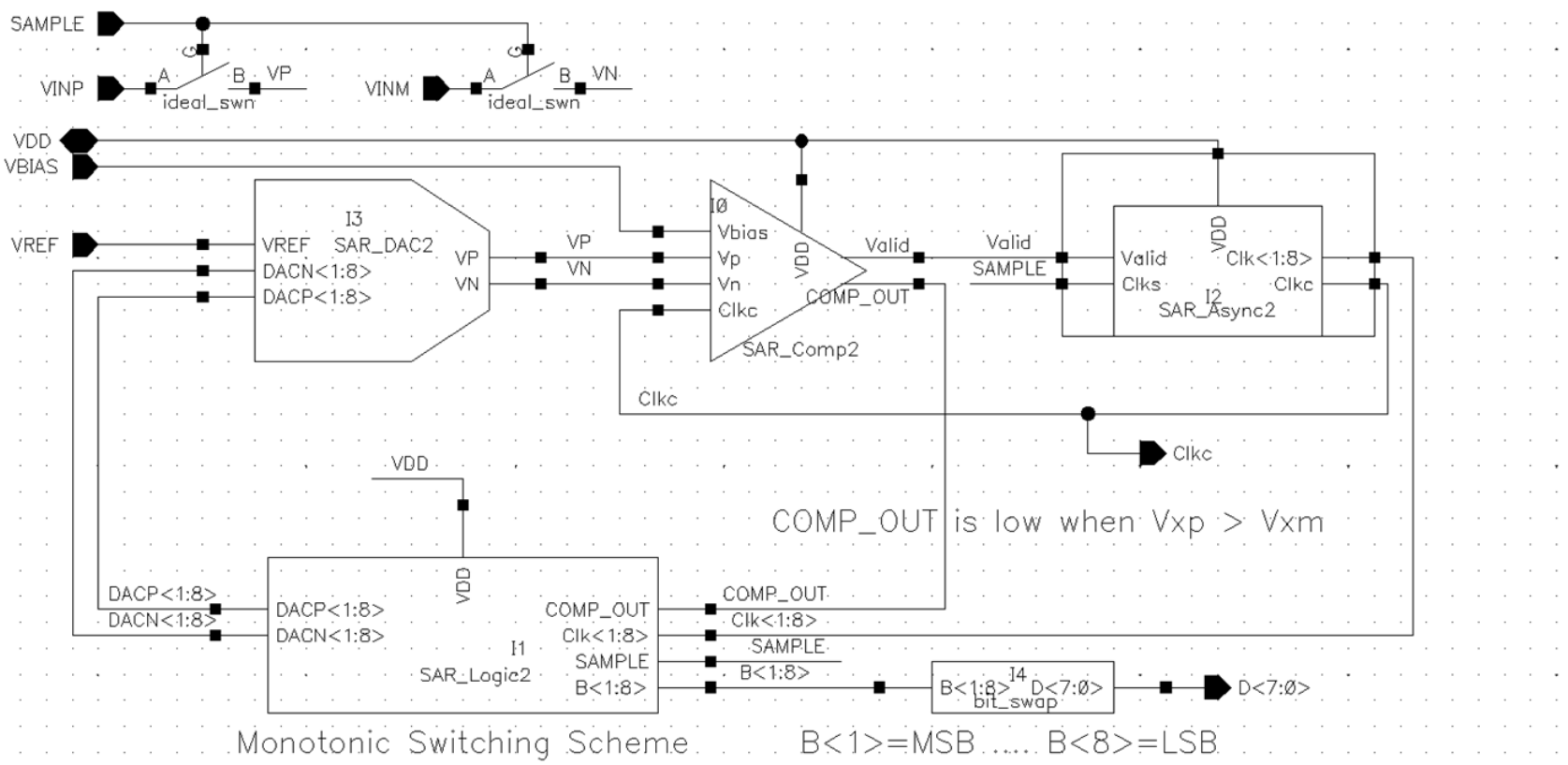
C. Liu, S. Chang, G. Huang, Y. Lin, “A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure,” *IEEE J. Solid-State Circuits*, pp. 731–740, April 2010



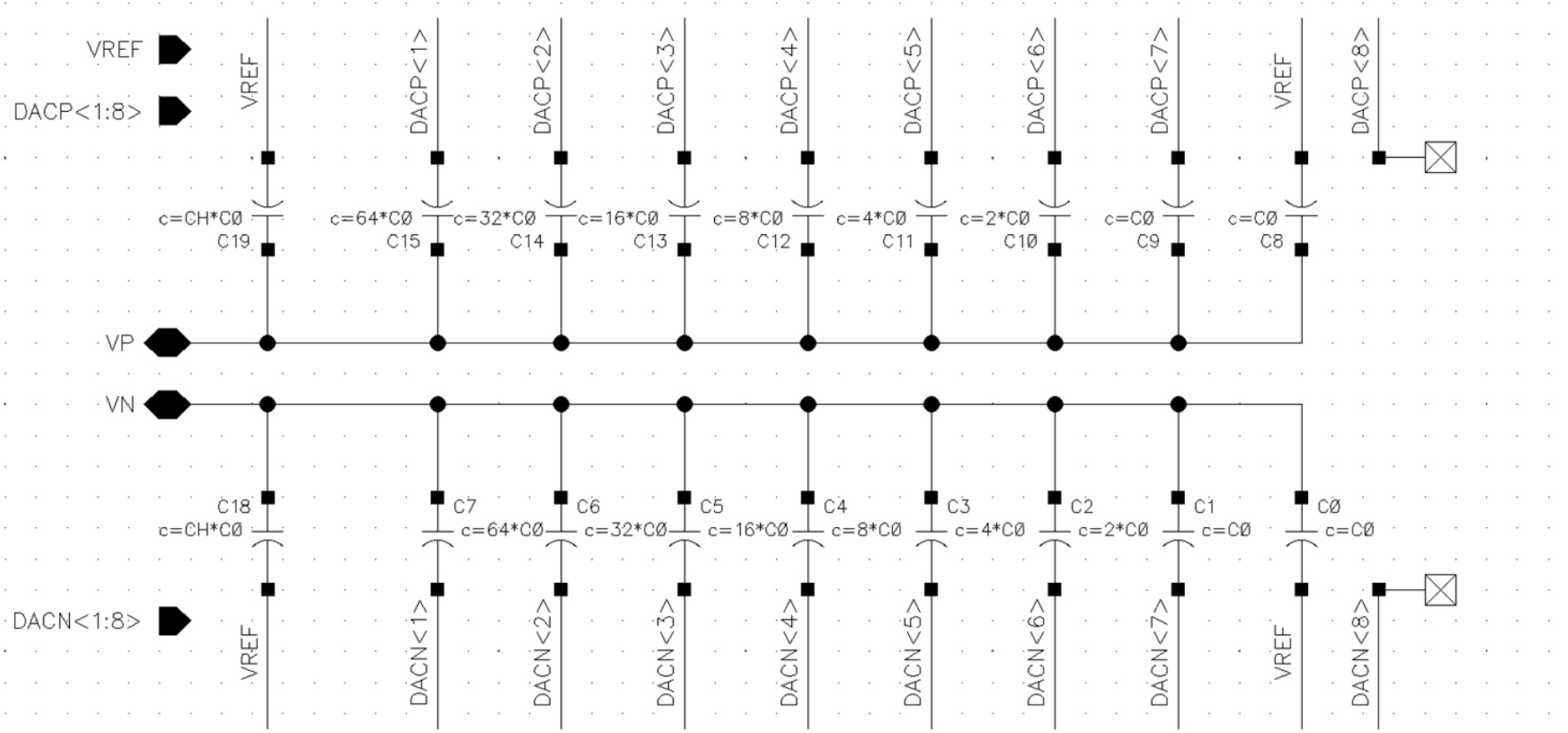
Async_SAR_ADC_tb2 in 288lib



SAR_ADC2

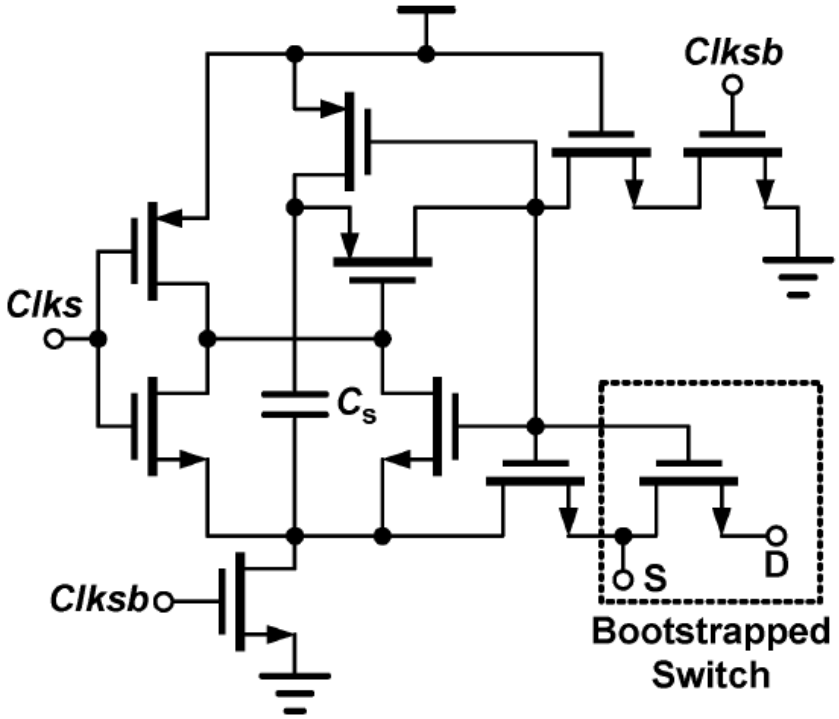

SAMPLE
VINP
A
B
VP
ideal_swn
VINM
A
B
VN
ideal_swn
VDD
VBIAS
VREF
I3
VREF SAR_DAC2
DACN<1:8>
DACP<1:8>
VP
VN
VP
VN
I0
Vbias
Vp
Vn
Clkc
VDD
COMP_OUT
SAR_Comp2
Valid
Valid
SAMPLE
VDD
Valid
Clks
Clk<1:8>
Clkc
I2
SAR_Async2
Clkc
Clkc
VDD
COMP_OUT is low when Vxp > Vxm
DACP<1:8>
DACN<1:8>
DACP<1:8>
DACN<1:8>
VDD
I1
SAR_Logic2
COMP_OUT
Clk<1:8>
SAMPLE
B<1:8>
COMP_OUT
Clk<1:8>
SAMPLE
B<1:8>
I4
B<1:8> D<7:0>
bit_swap
D<7:0>
Monotonic Switching Scheme
B<1>=MSB ..... B<8>=LSB

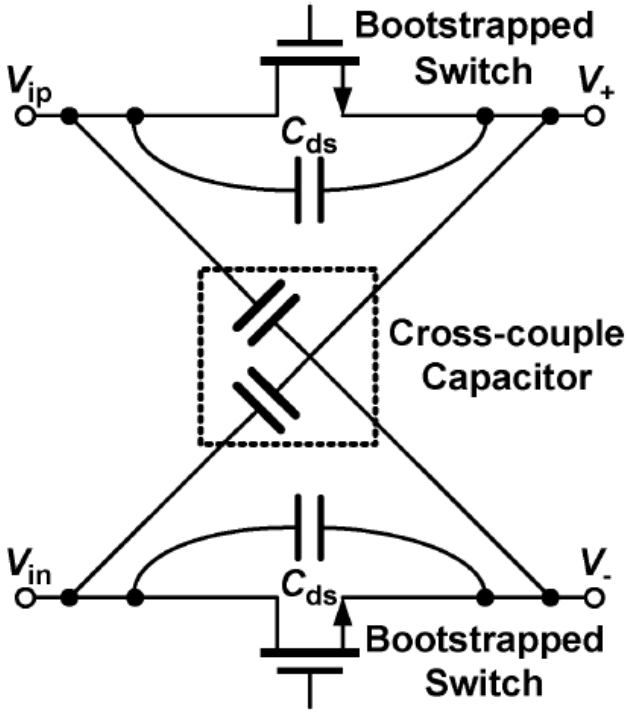
8-bit DAC Array with C_H



Bootstrapped Switch Example

C. Liu, S. Chang, G. Huang, Y. Lin, “A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure,” *IEEE J. Solid-State Circuits*, pp. 731–740, April 2010



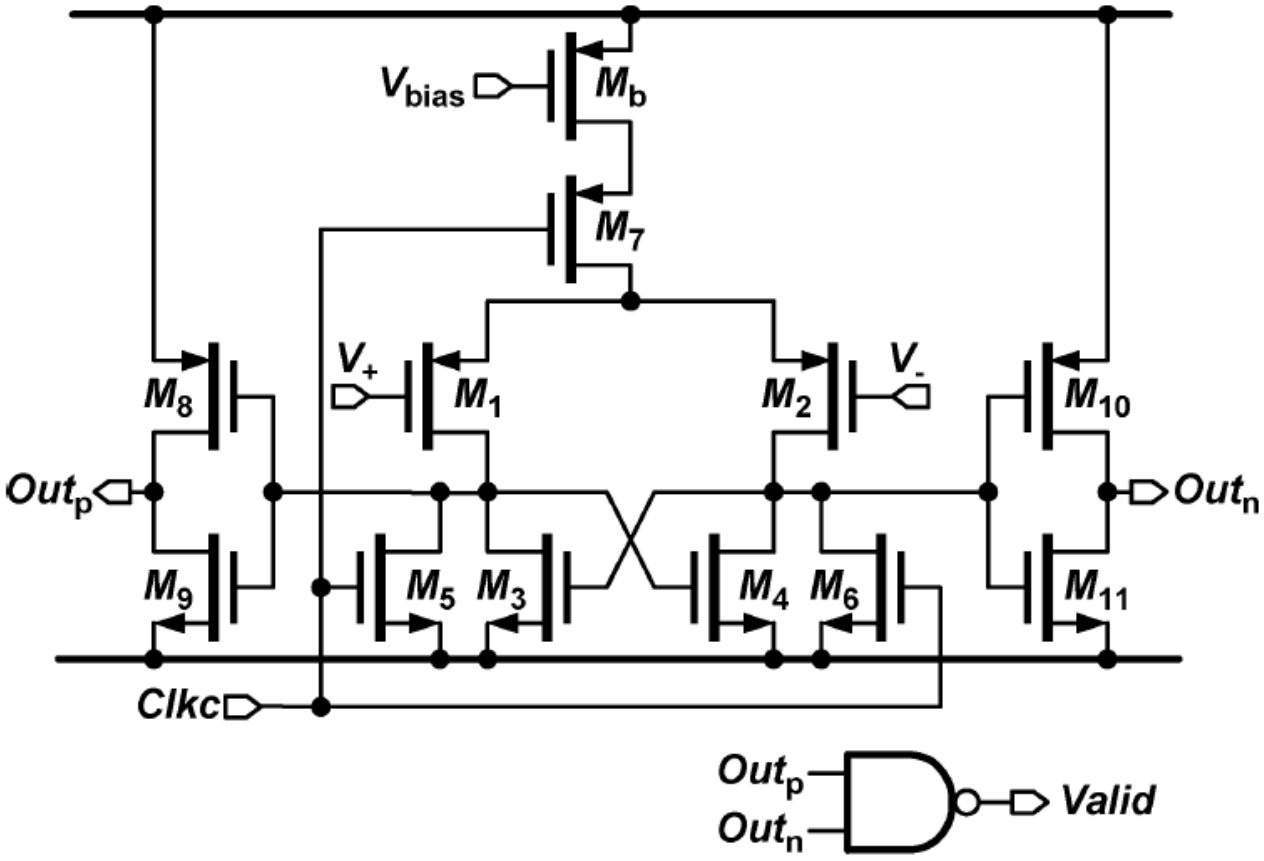


Will not be required to use bootstrapped switch in the project

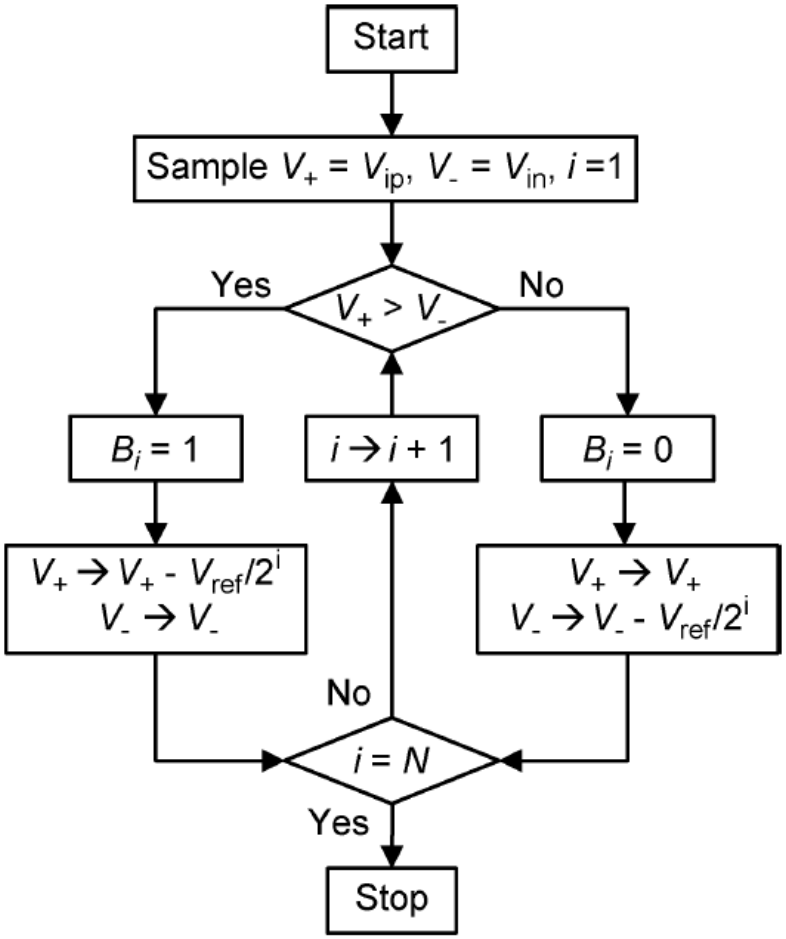
→Use ideal_swn

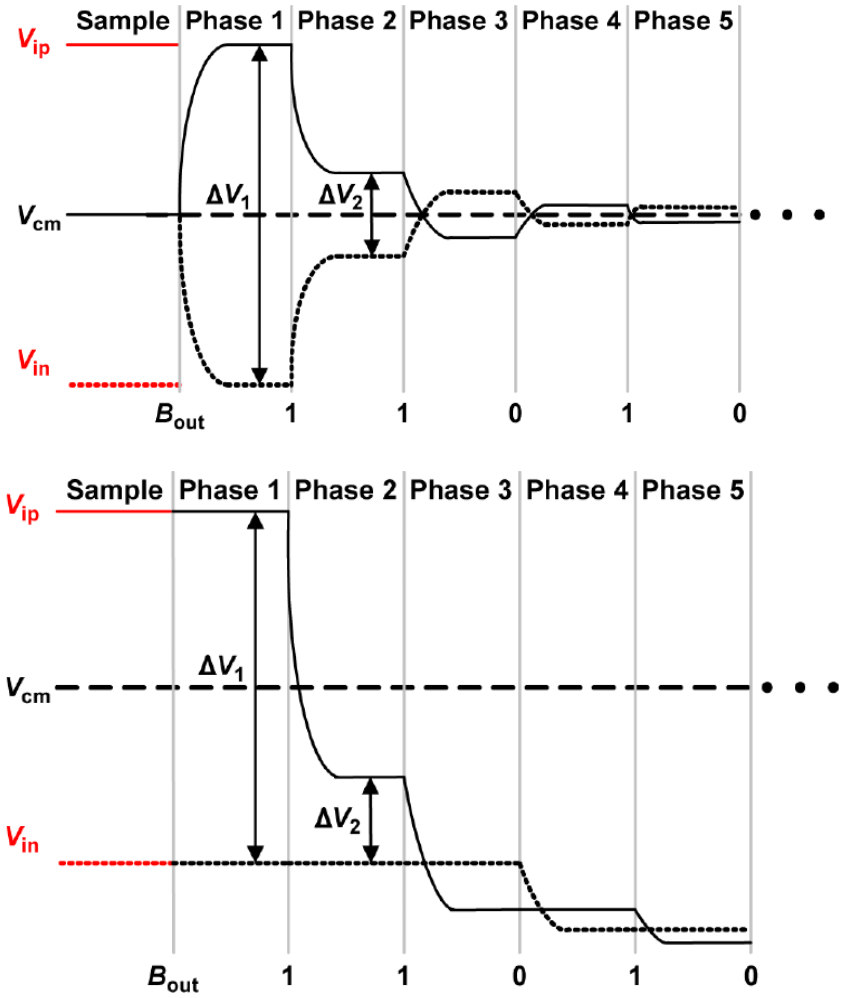
Dynamic Comparator Example

C. Liu, S. Chang, G. Huang, Y. Lin, “A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure,” *IEEE J. Solid-State Circuits*, pp. 731–740, April 2010

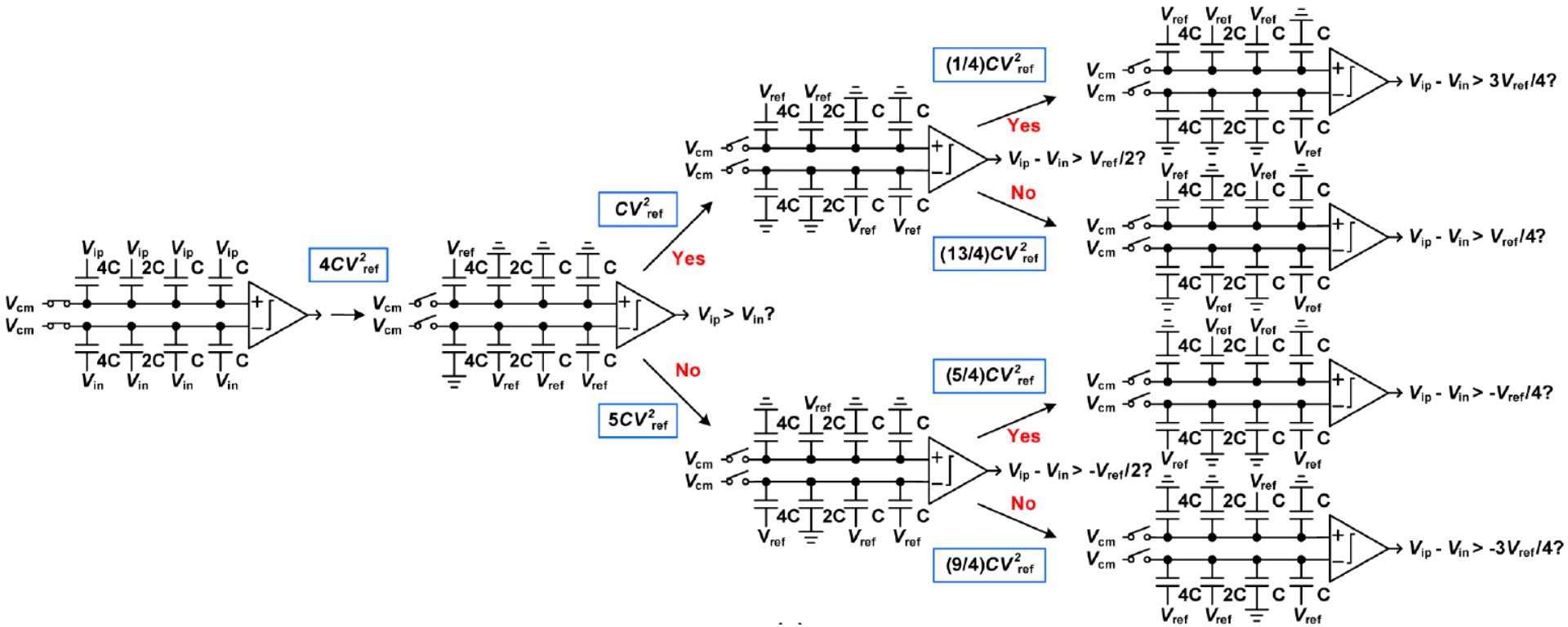


Flow Chart and Switching Schemes

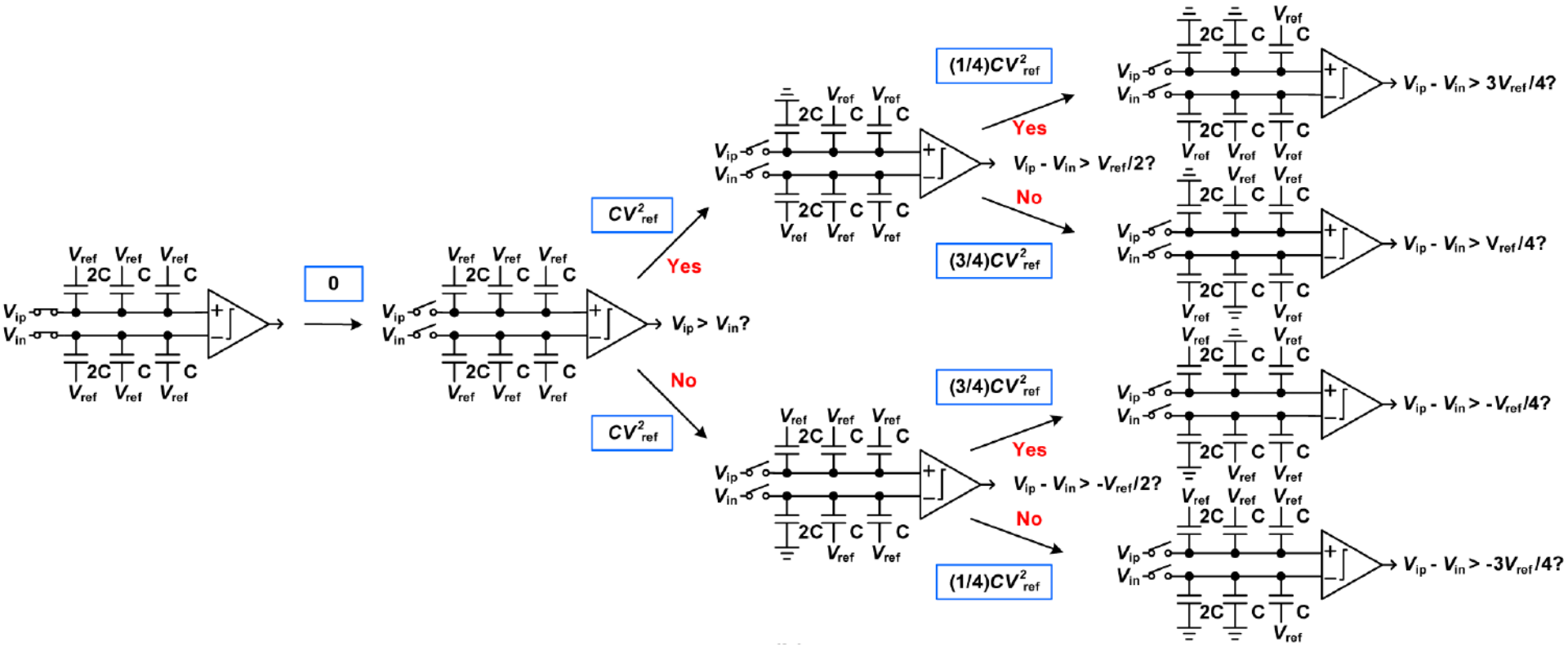




Conventional Switching Scheme

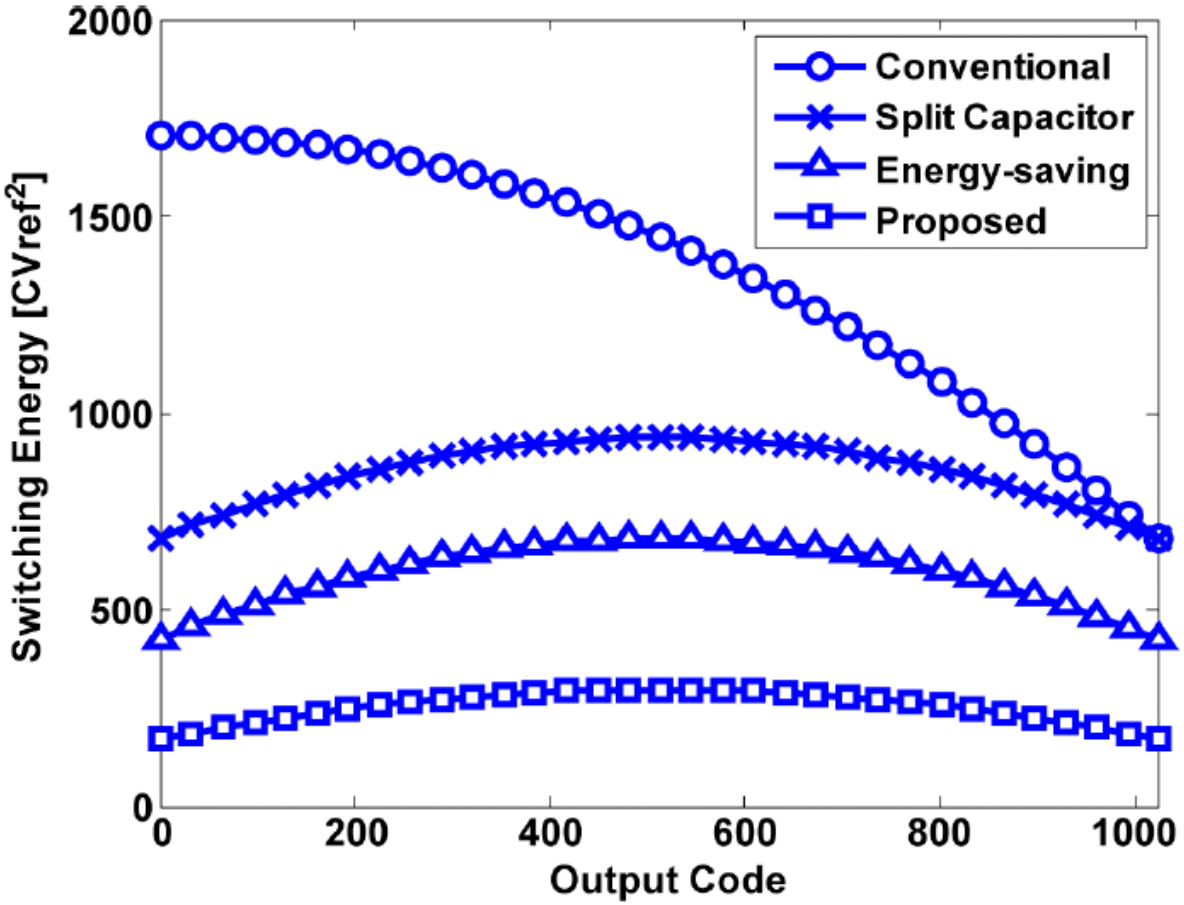


Monotonic Switching Scheme



Switching Energy vs Output Code

C. Liu, S. Chang, G. Huang, Y. Lin, “A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure,” *IEEE J. Solid-State Circuits*, pp. 731–740, April 2010



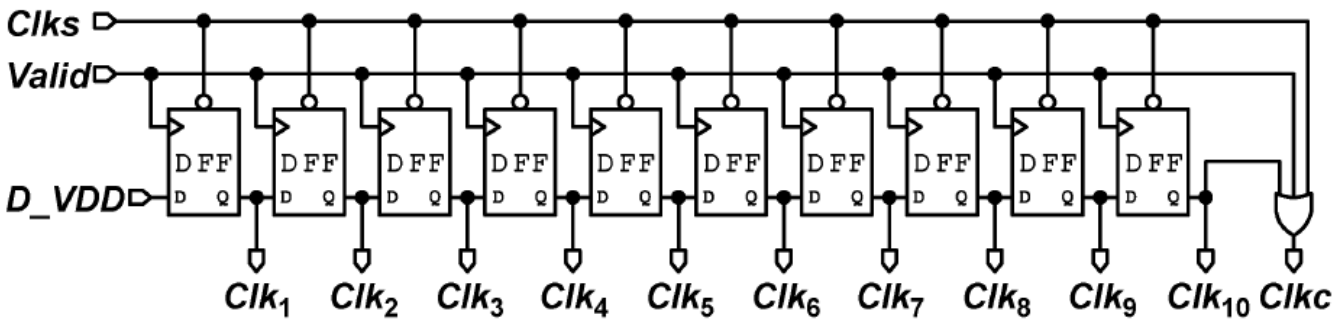
Comparison of Switching Procedures

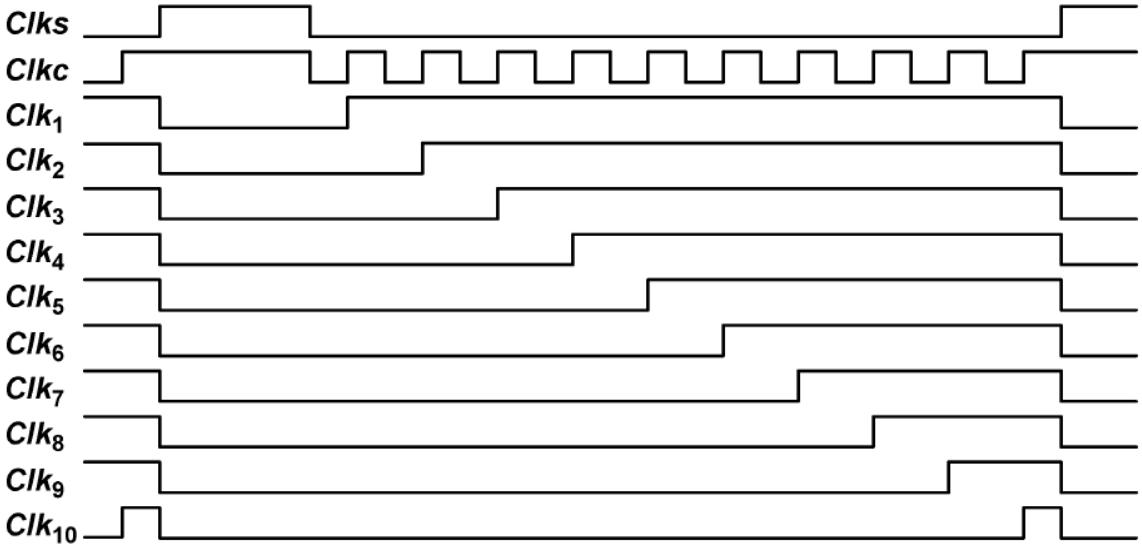
C. Liu, S. Chang, G. Huang, Y. Lin, “A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure,” *IEEE J. Solid-State Circuits*, pp. 731–740, April 2010

Switching Procedure	Conventional	Split Capacitor	Energy-saving	Proposed
Normalized Switching Power	1	0.63	0.44	0.19
No. of Switches	$4N+10$	$8N+6$	$8N+2$	$4N$
No. of Capacitors	$2N+2$	$4N$	$4N-2$	$2N$
No. of Unit Capacitors in Capacitor Array	2^N	2^N	2^N	2^{N-1}

Asynchronous Control Logic and Timing

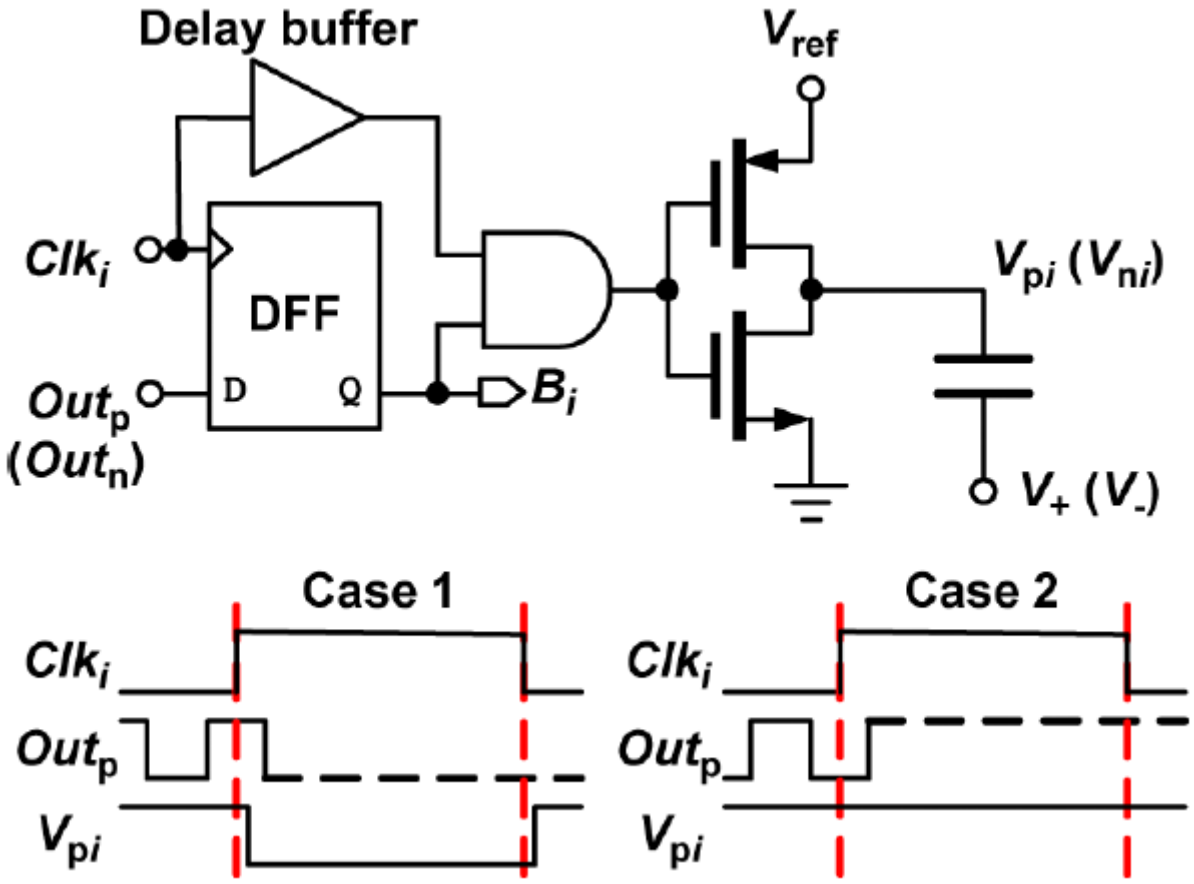
C. Liu, S. Chang, G. Huang, Y. Lin, “A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure,” *IEEE J. Solid-State Circuits*, pp. 731–740, April 2010





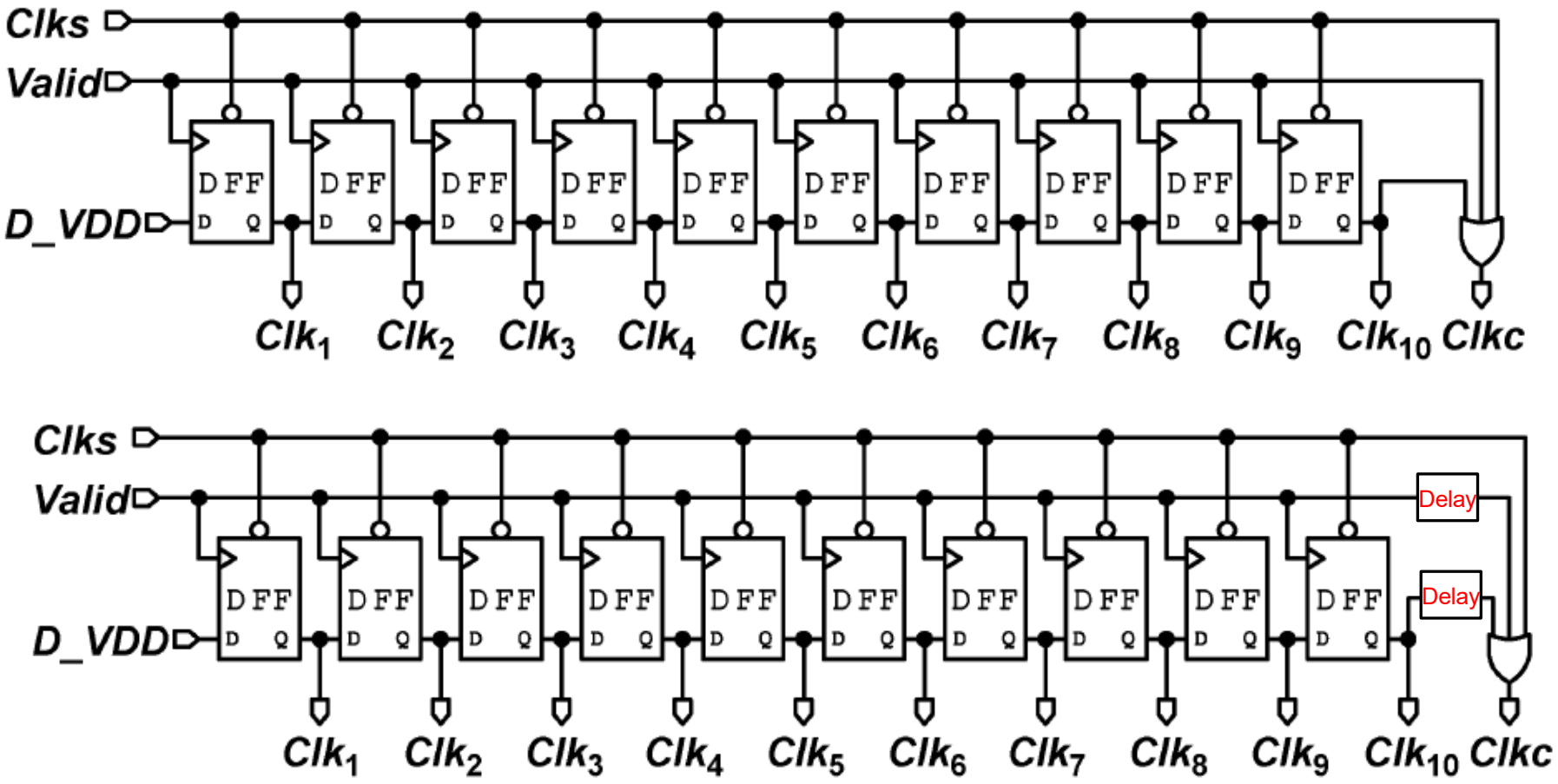
DAC Control Logic

C. Liu, S. Chang, G. Huang, Y. Lin, “A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure,” *IEEE J. Solid-State Circuits*, pp. 731–740, April 2010

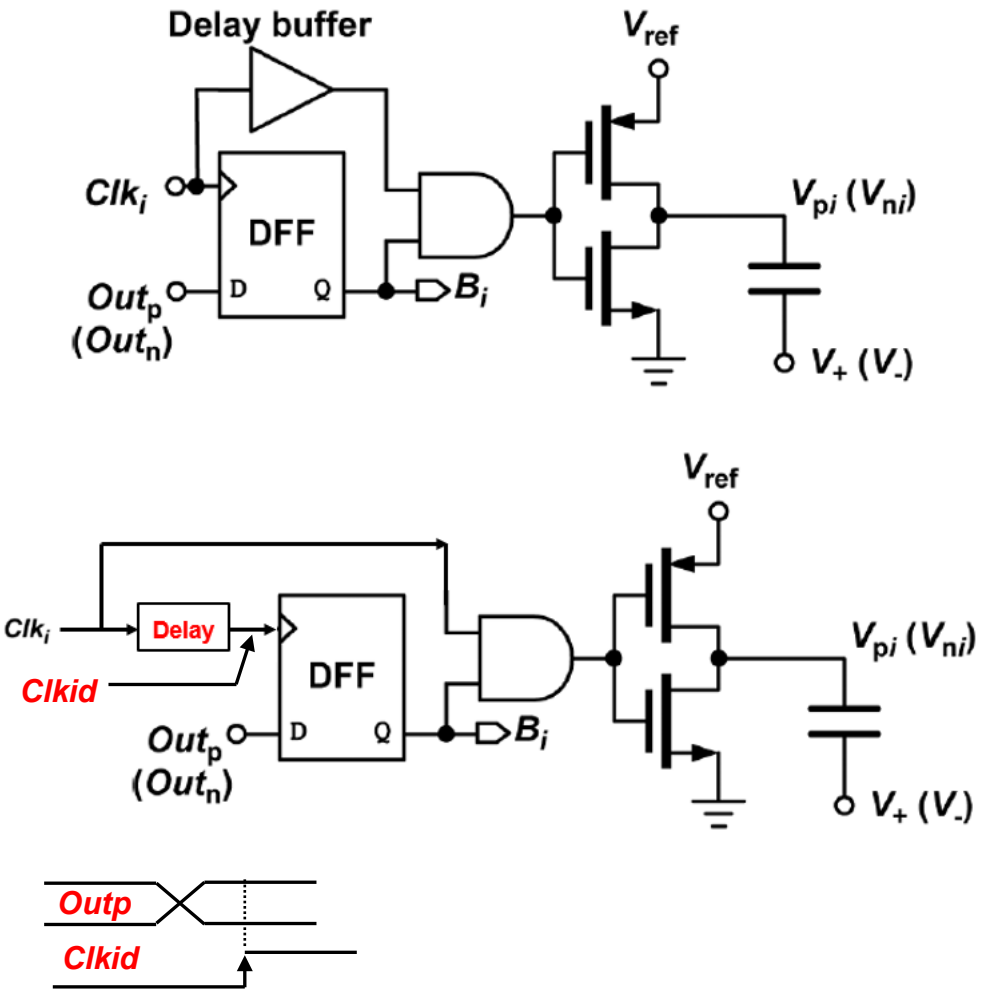


Change in Asynchronous Control Logic and Timing

C. Liu, S. Chang, G. Huang, Y. Lin, “A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure,” *IEEE J. Solid-State Circuits*, pp. 731–740, April 2010



Change in DAC Control Logic



Make sure that Outp is settled to a new value before Clkid goes high.

ADC Summary

C. Liu, S. Chang, G. Huang, Y. Lin, “A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure,” *IEEE J. Solid-State Circuits*, pp. 731–740, April 2010

Specification (Unit)	Experimental Result
Supply Voltage (V)	1.2
Input CM Voltage (V)	0.6
Input Range (V_{p-p})	2
Sampling Capacitance (pF)	2.5
Sampling Rate (MS/s)	50
Active Area (mm^2)	0.052
DNL (LSB)	0.91 / -0.63
INL (LSB)	1.27 / -1.36
SNDR/SFDR (dB)	57.0 / 65.9 (0.5 MHz)
	56.5 / 64.6 (10 MHz)
	54.4 / 61.8 (50 MHz)
ENOB (bit)	9.18
ERBW (MHz)	50
Power (mW)	0.826

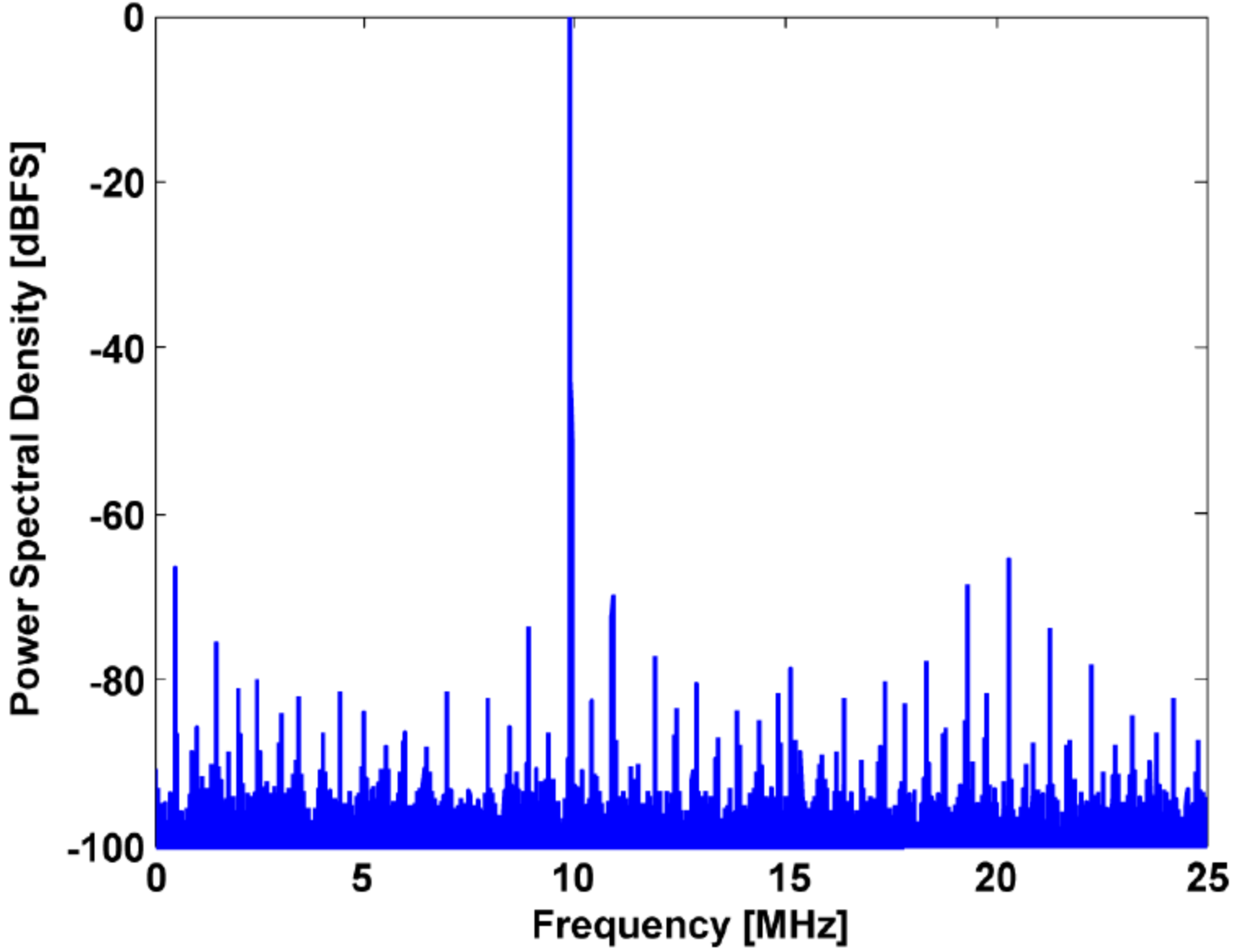


Fig. 15. Measured ~~32,768~~ 64-point FFT spectrum at 50 MS/s.

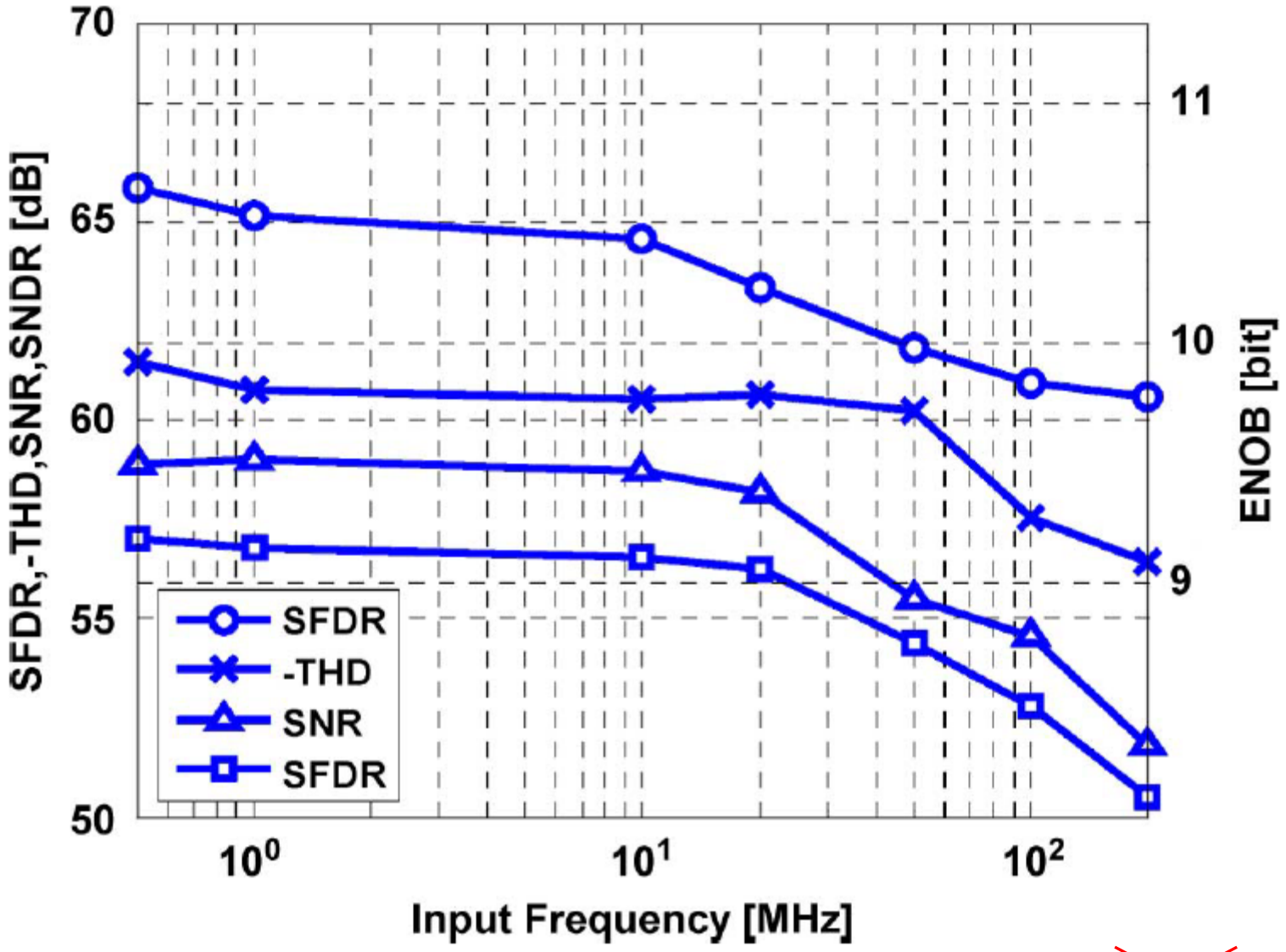


Fig. 16. Measured dynamic performance versus input frequency at 1.2 V and 50 MS/s.

~~1.2 V~~ VDD=1V

~~50~~ 10

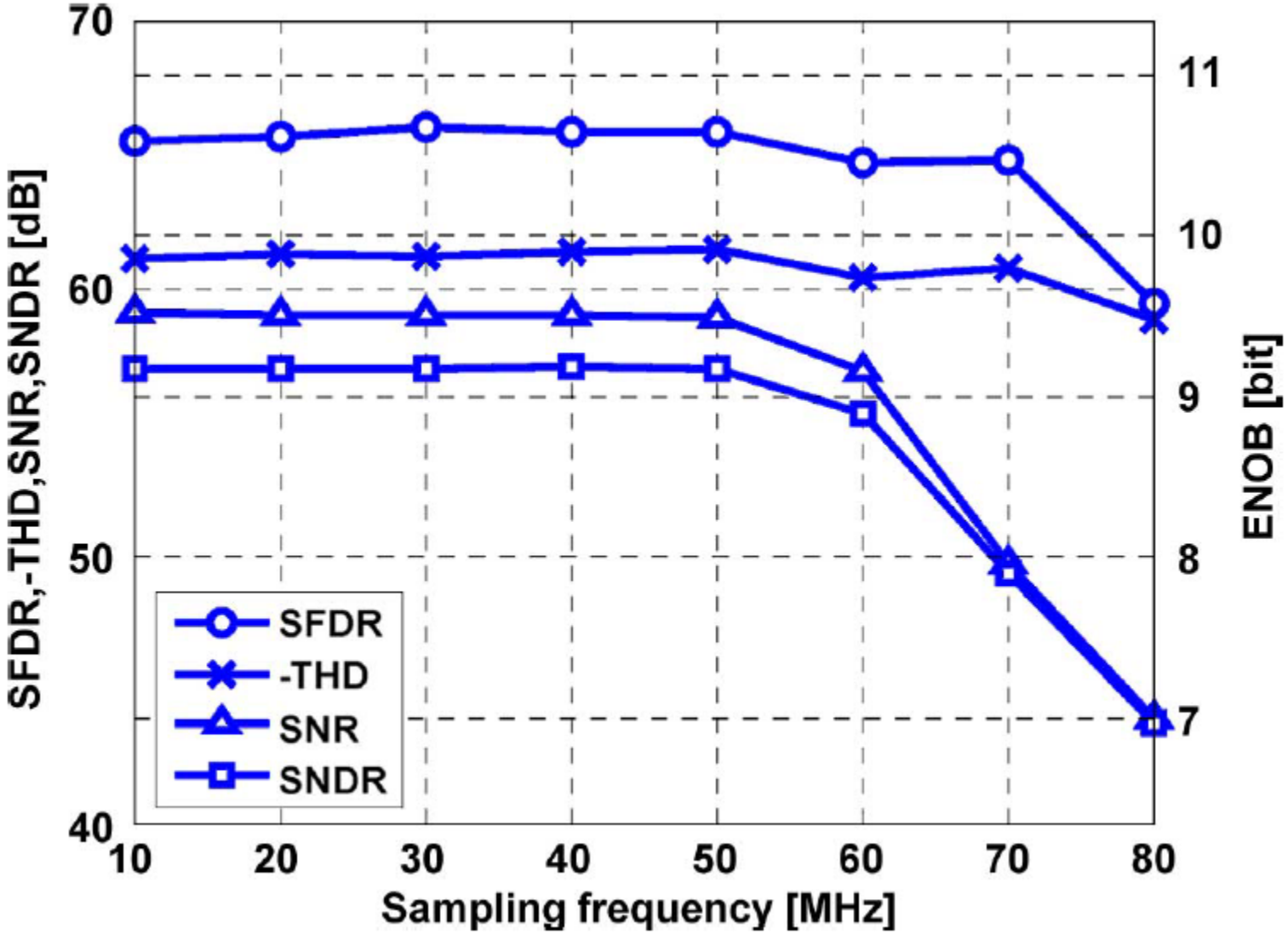
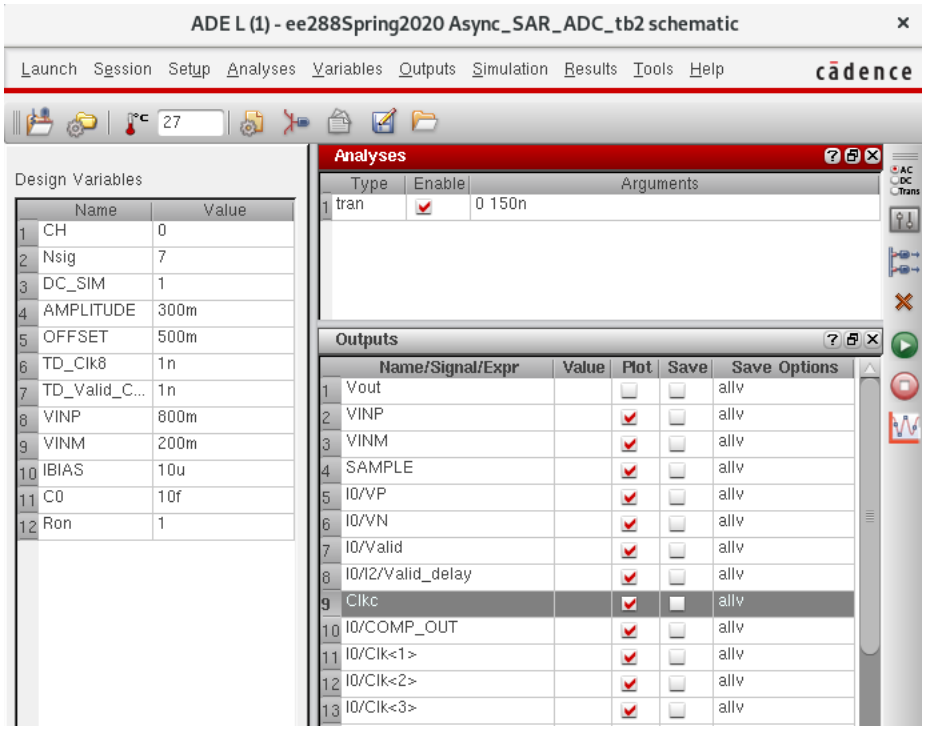
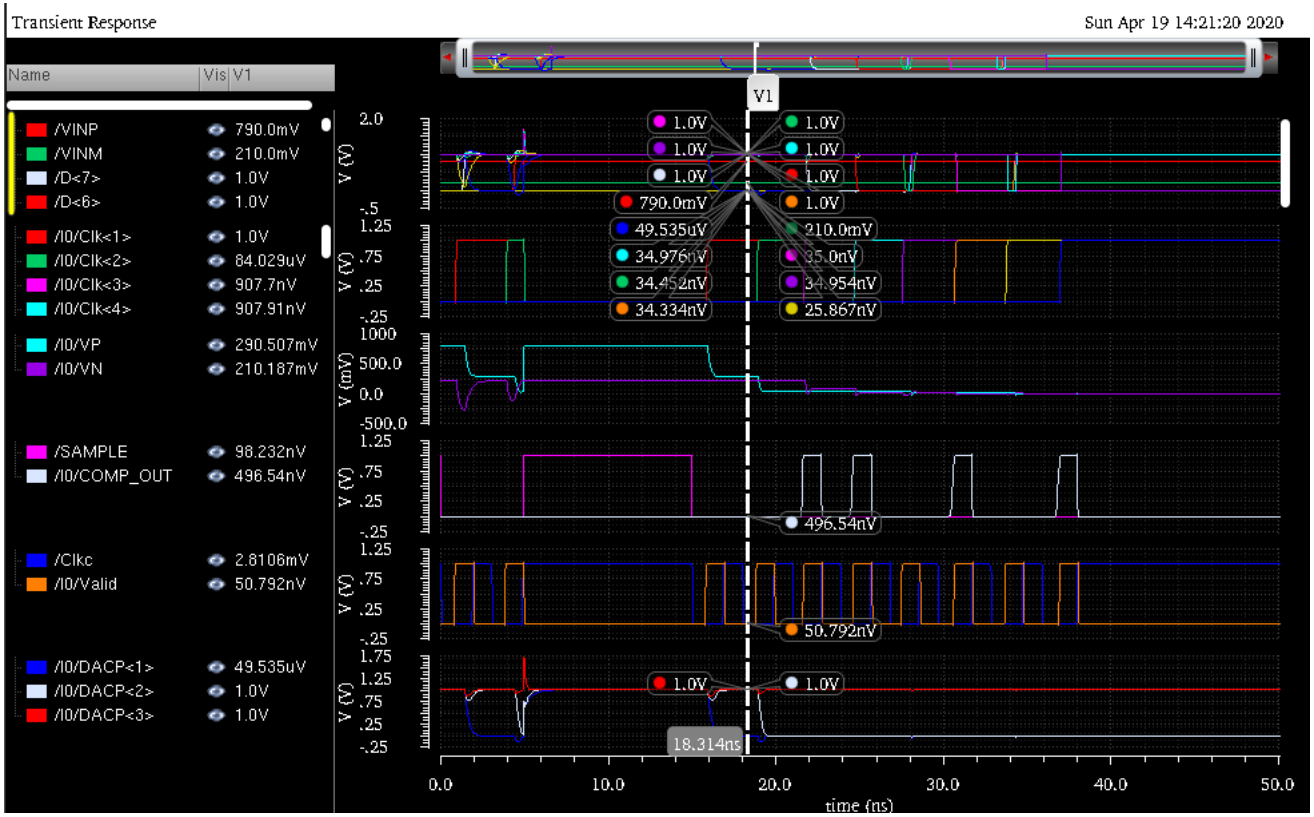


Fig. 17. Measured dynamic performance versus sampling frequency.

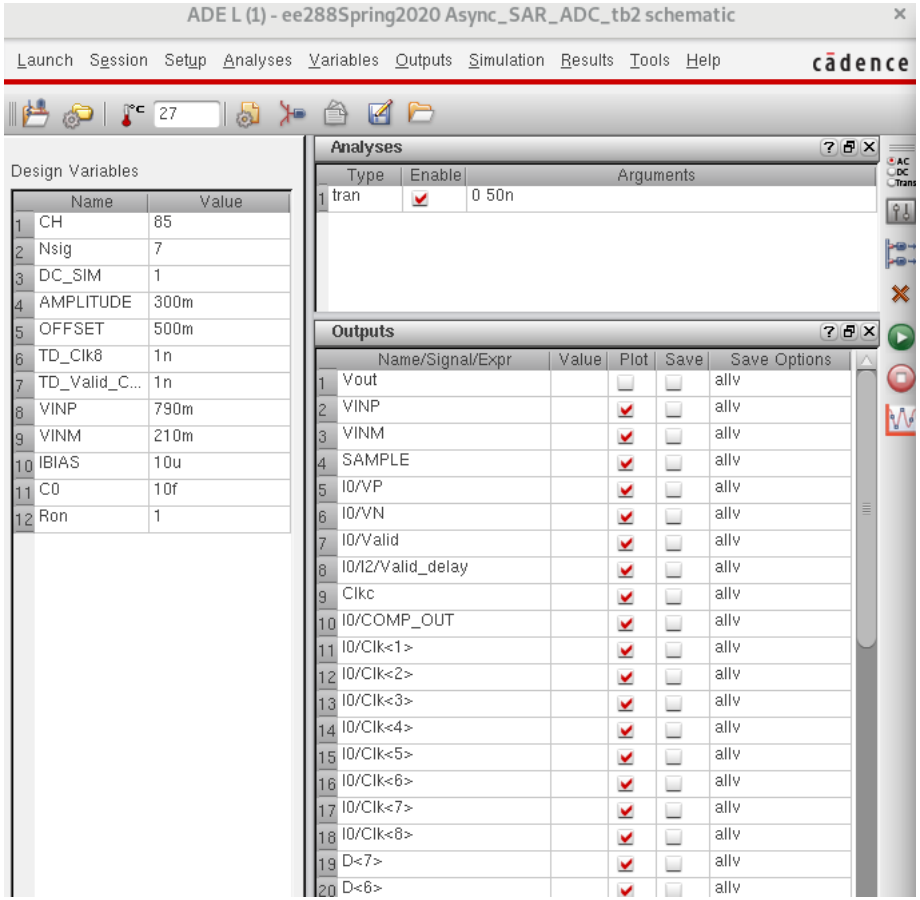
Simulation Setup with $C_H = 0$



Simulation Result with $C_H = 0$



Simulation Setup with C_H = 85



Simulation Result with C_H = 85