Design of a Low-Power Asynchronous SAR ADC in 45 nm CMOS Technology

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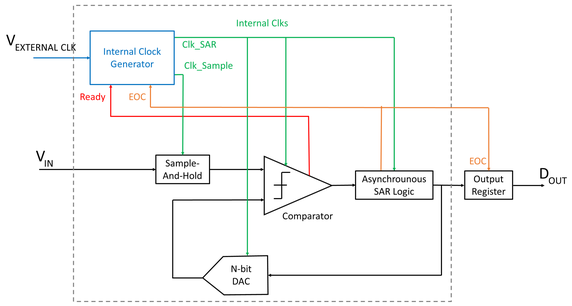
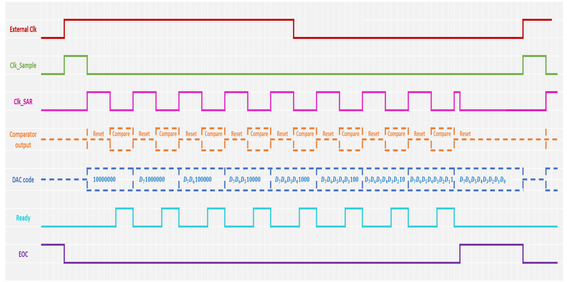
Introduction

This project is about the design process of an 8-bit asynchronous successive approximation register (SAR) analog-to-digital converter (ADC) using 45nm CMOS technology. SAR ADCs are attractive circuits for applications that require low power with medium resolution and medium speed like in computing-in-memory cores for AI applications and in sensors for biomedical applications. The asynchronous architecture allow the ADC to operate without the need for an oversampled clock reducing the design complexities associated with higher frequencies. The top-level block diagram of the asynchronous SAR ADC is shown below, along with the timing diagram of the important signals.

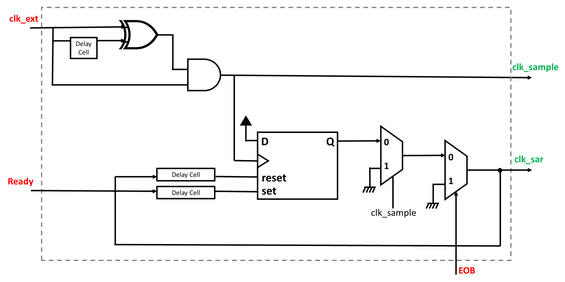




Circuit Design

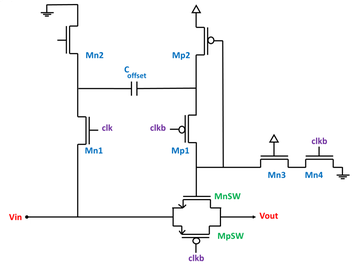
1) Internal Clock Generator

The internal clock generator is the block responsible for providing the rest of the system with the clock signals to operate. This block produces 2 output signals, “clk_sample” and “clk_sar”, and receives 3 inputs “clk_ext”, “Ready”, and “EOC”.



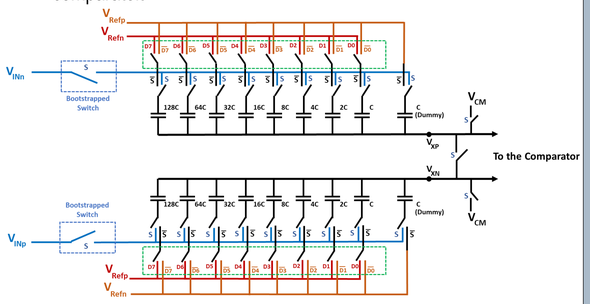
2) Bootstrapped Sample-And-Hold Switches

The sample-and-hold circuit is basically a switch that captures the value of an analog signal at a certain moment and holds it constant for a certain amount of time. The bootstrapped switch help mitigate some of the switch non-idealities by keeping the switch’s V_{GS} fixed during the sampling phase.



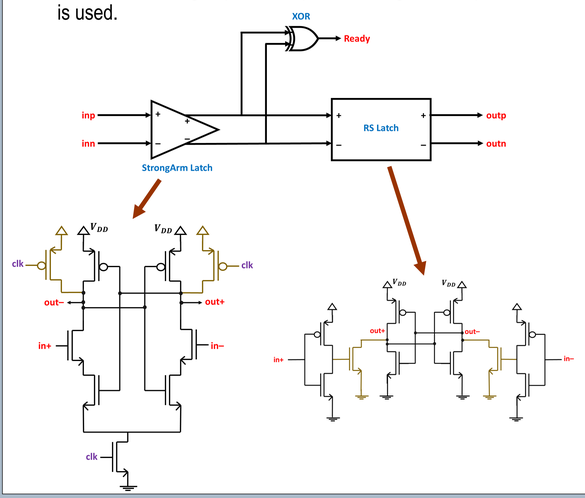
3) Capacitive DAC

The capacitive DAC uses charge redistribution to convert the digital code coming from the SAR logic into the corresponding analog voltage level to be compared by the comparator.



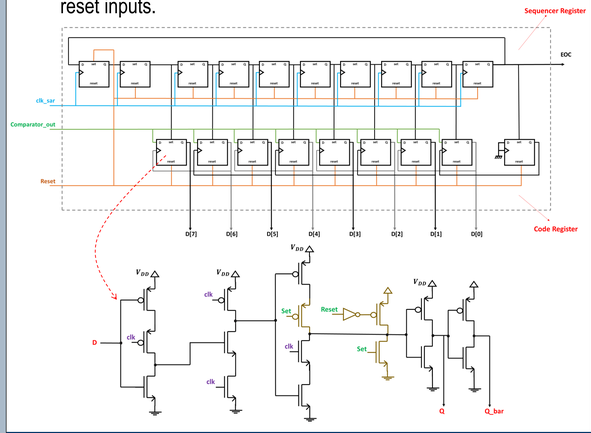
4) Dynamic Comparator

The comparator’s function is to compare the analog input levels coming from the DAC and to produce a digital output bit (either high or low) representing the result of the comparison. A high-speed low-power strongarm comparator is used.



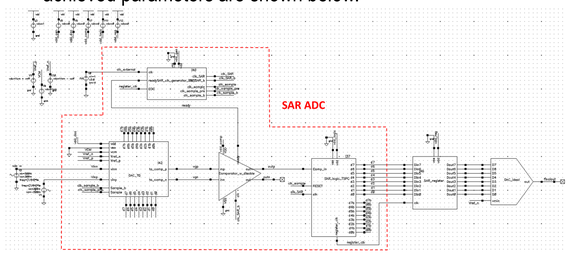
5) SAR Logic

The SAR logic generates the digital code for the DAC in each comparison stage. At the end of the conversion cycle, the final digital code is outputted by an output register. The flipflops used are TSPC flipflops with asynchronous set and reset inputs.

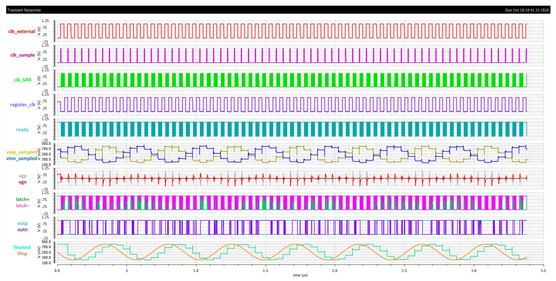


Analysis and Results

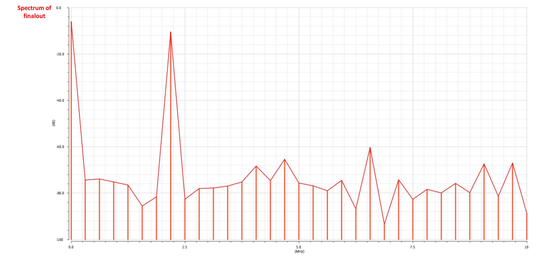
The testbench, the waveforms, and a summary of the achieved parameters are shown below.



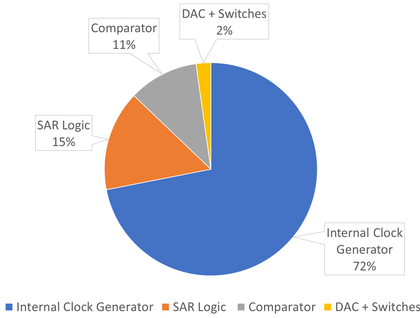
Asynchronous SAR ADC Testbench



Transient Waveforms



Output Spectrum



Power Consumption per Block

Parameter	Value
Technology	45 nm CMOS
Power Supply	1 V
Resolution	8 bits
Sampling Rate	20 MS/s
Common-Mode Voltage	0.5 V
Differential Input Range	1.2 V
Sampling Unit Cap	2 fF
SINAD	46.00 dB
SFDR	49.91 dB
ENOB	7.35 bits
Total Power	49.124 uW
$FOM = \frac{P_{total}}{2^{ENOB} \cdot f_s}$	15.06 fJ/ conversion-step

Final Parameters Achieved

Summary/Conclusions

A low-power 20 MS/s 8-bit asynchronous SAR ADC, with a clock input of 20MHz and designed using CMOS 45nm technology at 1 V, is presented. The proposed system achieves an ENOB of 7.35 bits, SNR of 46 dB, and a total power consumption of 49.12 uW, resulting in an FOM of 15 fJ/conversion-step. This design offers an energy and FOM-efficient ADC without the use of an oversampled clock for low-power medium-speed applications.

Key References

[1] O. Kardonik, "A study of SAR ADC and implementation of 10-bit asynchronous design," M.S. Thesis, Department of Electrical and Computer Engineering, University of Texas at Austin, 2013.

[2] P. J. A. Harpe et al., "A 26 uW 8 bit 10 MS/s Asynchronous SAR ADC for Low Energy Radios," IEEE Journal of Solid-State Circuits, vol. 46, no. 7, pp. 1585-1595, July 2011.

[3] M. Al-Qadasi, A. Alshehri, A. S. Almansouri, T. Al-Attar, and H. Fariborzi, "A High Speed Dynamic StrongARM Latch Comparator," 2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS), Windsor, ON, Canada, 2018, pp. 540-541.

[4] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio ΔΣ modulator with 88-dB dynamic range using local switch bootstrapping," IEEE Journal of Solid-State Circuits, vol. 36, no. 3, pp. 349-355, March 2001.

Acknowledgements

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