EE288 Data Conversions/Analog Mixed-Signal ICs
Spring 2018

Lecture 18: SAR ADC

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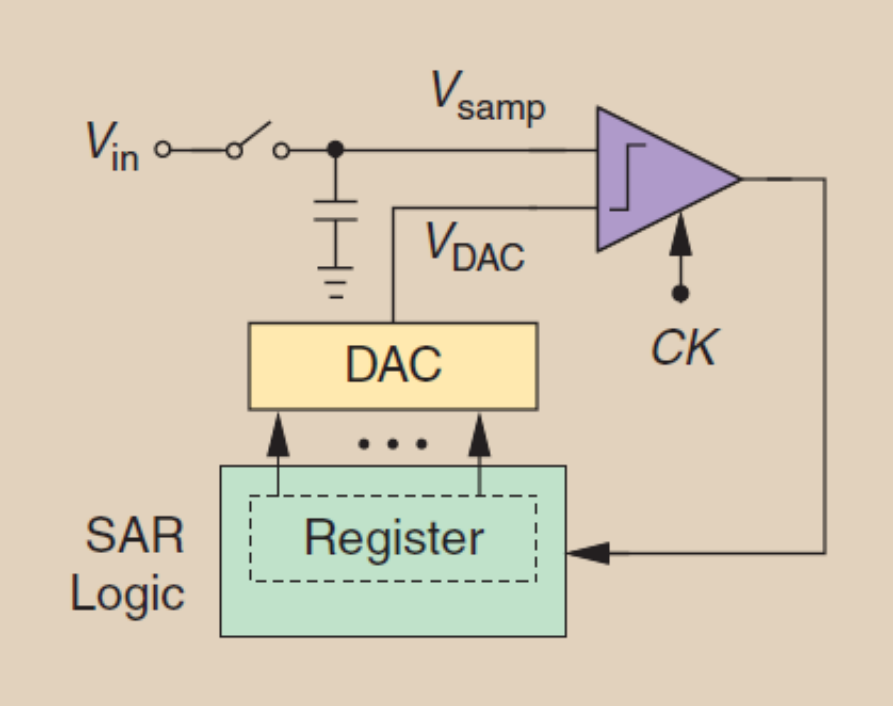
Course Schedule – Subject to Change

Date	Topics
24-Jan	Course introduction and ADC architectures
29-Jan	Converter basics: AAF, Sampling, Quantization, Reconstruction
31-Jan	ADC dynamic performance metrics, Spectrum analysis using FFT
5-Feb	ADC & DAC static performance metrics, INL and DNL
7-Feb	OPAMP and bias circuits review
12-Feb	SC circuits review
14-Feb	Sample and Hold Amplifier - Reading materials
19-Feb	Flash ADC and Comparators: Regenerative Latch
21-Feb	Comparators: Latch offset, preamp, auto-zero
26-Feb	~~Finish Flash ADC~~
28-Feb	~~DAC Architectures - Resistor, R-2R~~
5-Mar	~~DAC Architectures - Current steering, Segmented~~
7-Mar	~~DAC Architectures - Capacitor-based~~
12-Mar	~~SAR ADC with bottom plate sampling~~
14-Mar	~~SAR ADC with top plate sampling~~
19-Mar	~~Midterm Review~~
21-Mar	Midterm exam
26-Mar	Spring break
28-Mar	Spring break
2-Apr	~~Pipelined ADC stage - comparator, MDAC, x2 gain~~
4-Apr	~~Pipelined ADC bit sync and alignment using Full adders~~
9-Apr	Pipelined ADC 1.5bit vs multi-bit structures
11-Apr	Fully-differential OPAMP and Switched-capacitor CMFB
16-Apr	Single-slope ADC
18-Apr	Oversampling & Delta-Sigma ADCs
23-Apr	Second- and higher-order Delta-Sigma Modulator.
25-Apr	Hybrid ADC - Pipelined SAR
30-Apr	Hybrid ADC - Time-Interleaving
2-May	ADC testing and FoM
7-May	Project presentation 1
8-May	Project presentation 2
14-May	Final Review
20-May	Project Report Due by 6 PM

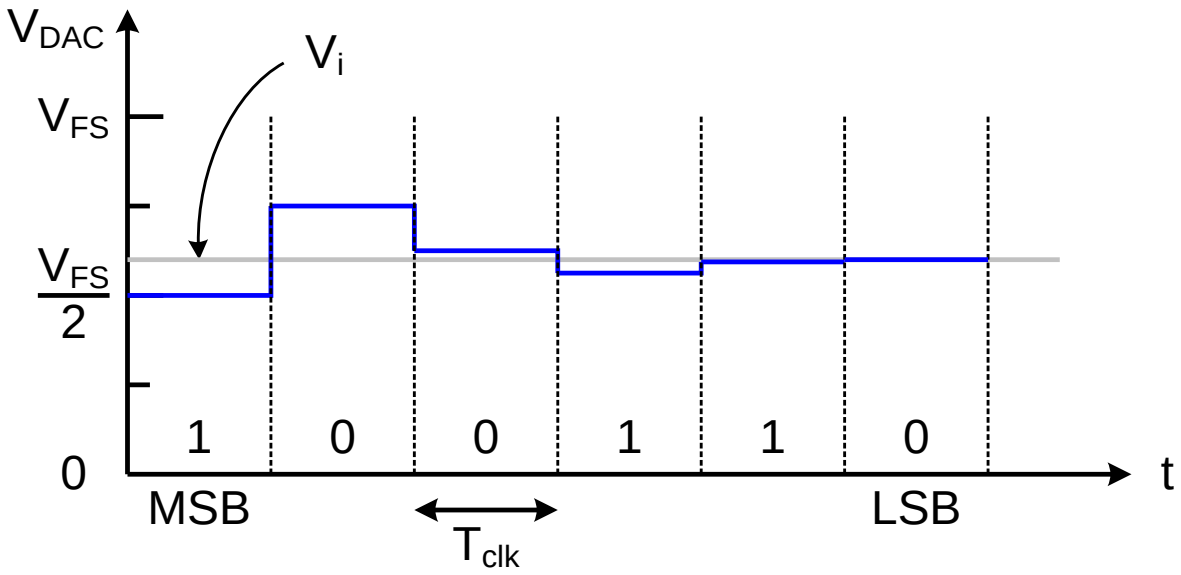
SAR ADC

Successive Approximation Register (SAR) ADC



- Binary search algorithm → $N*T_{clk}$ to complete N bits
- Conversion speed is limited by comparator, DAC, and digital logic (successive approximation register or SAR)

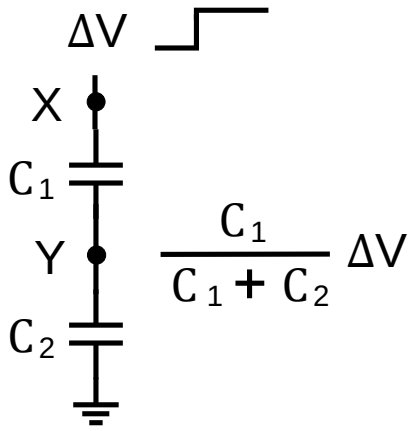
Binary Search Algorithm



- DAC output gradually approaches the input voltage
- Comparator differential input gradually approaches zero

Capacitive Divider

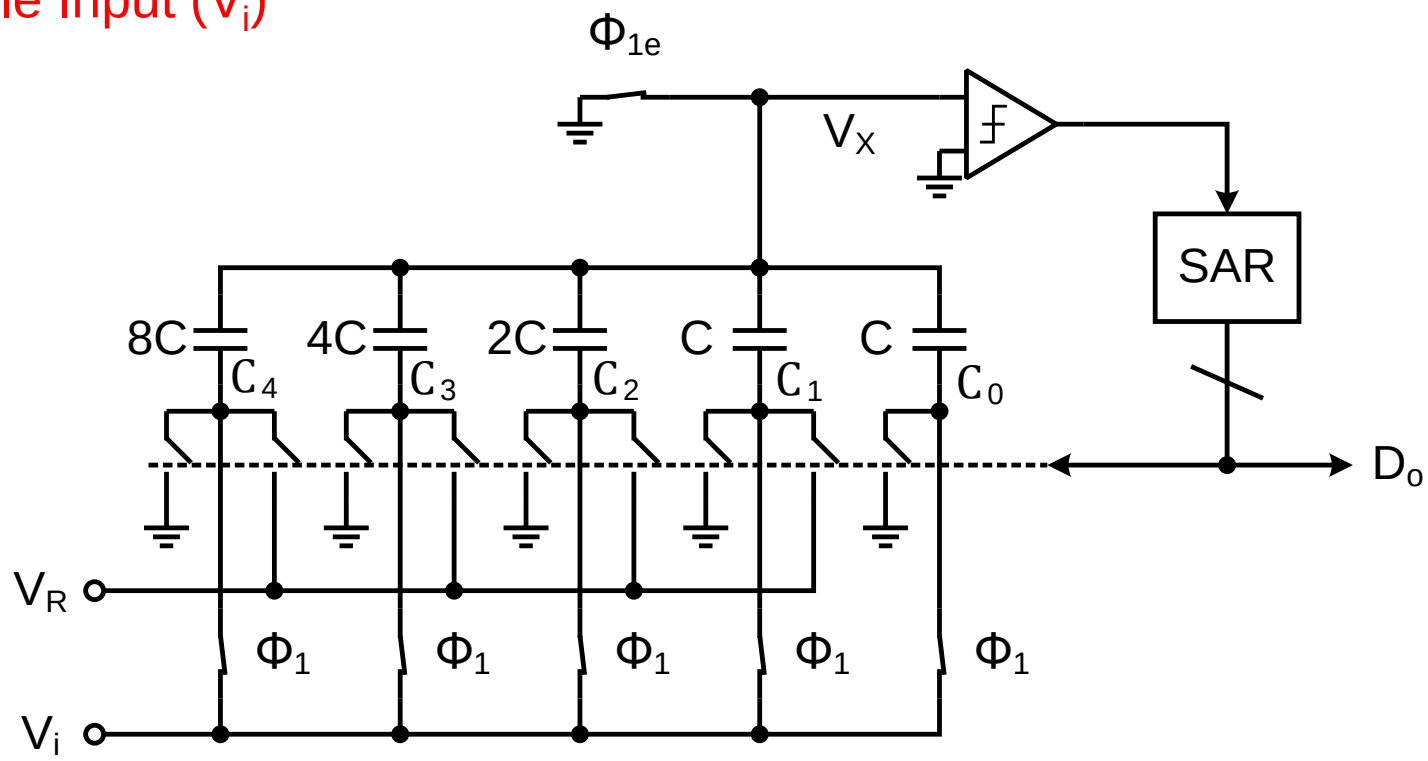
When the voltage at node X changes by ΔV, the node at Y will change by $\Delta V \cdot C_1/(C_1+C_2)$



If $C_1 >> C_2$, the voltage change at node Y will be approximately ΔV

Charge Redistribution SAR ADC

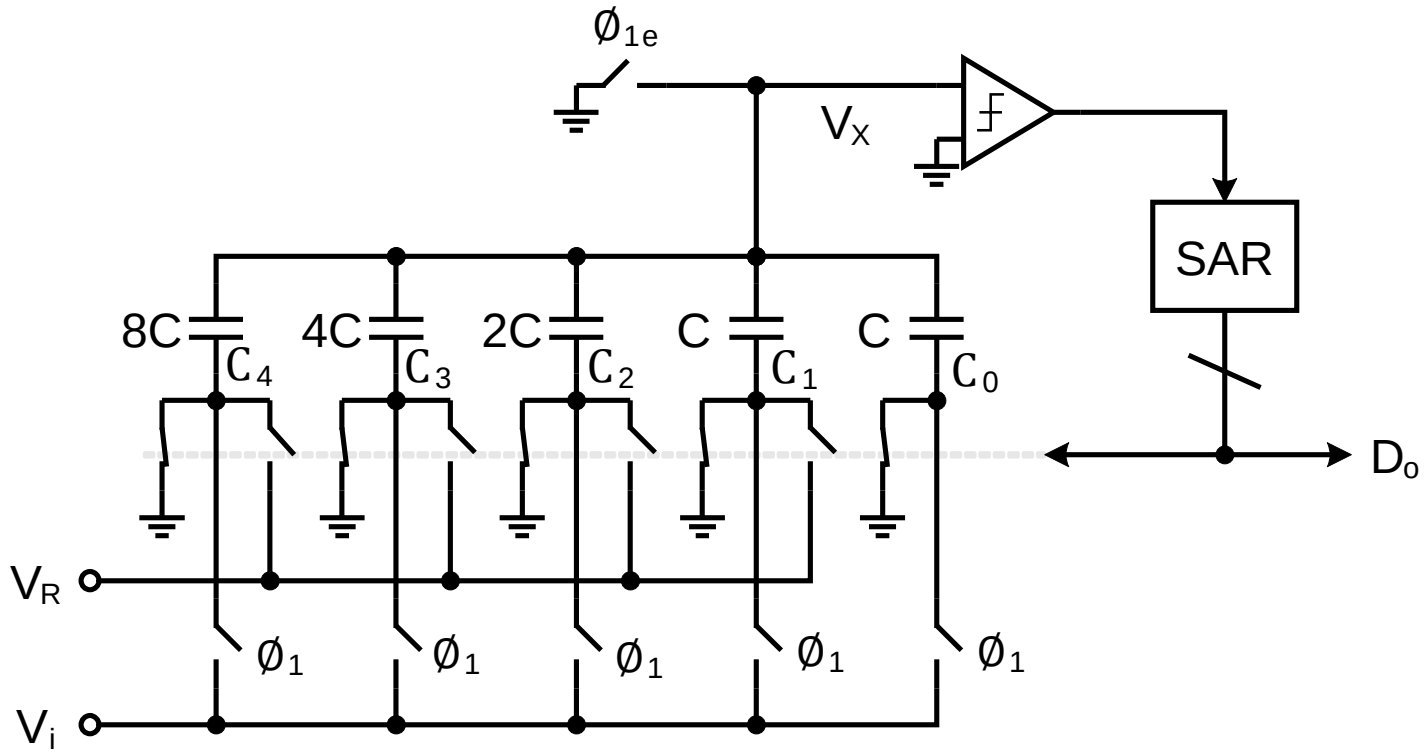
Sample Input (V_i)



- 4-bit binary-weighted capacitor array DAC
- Capacitor array samples input during Φ_1

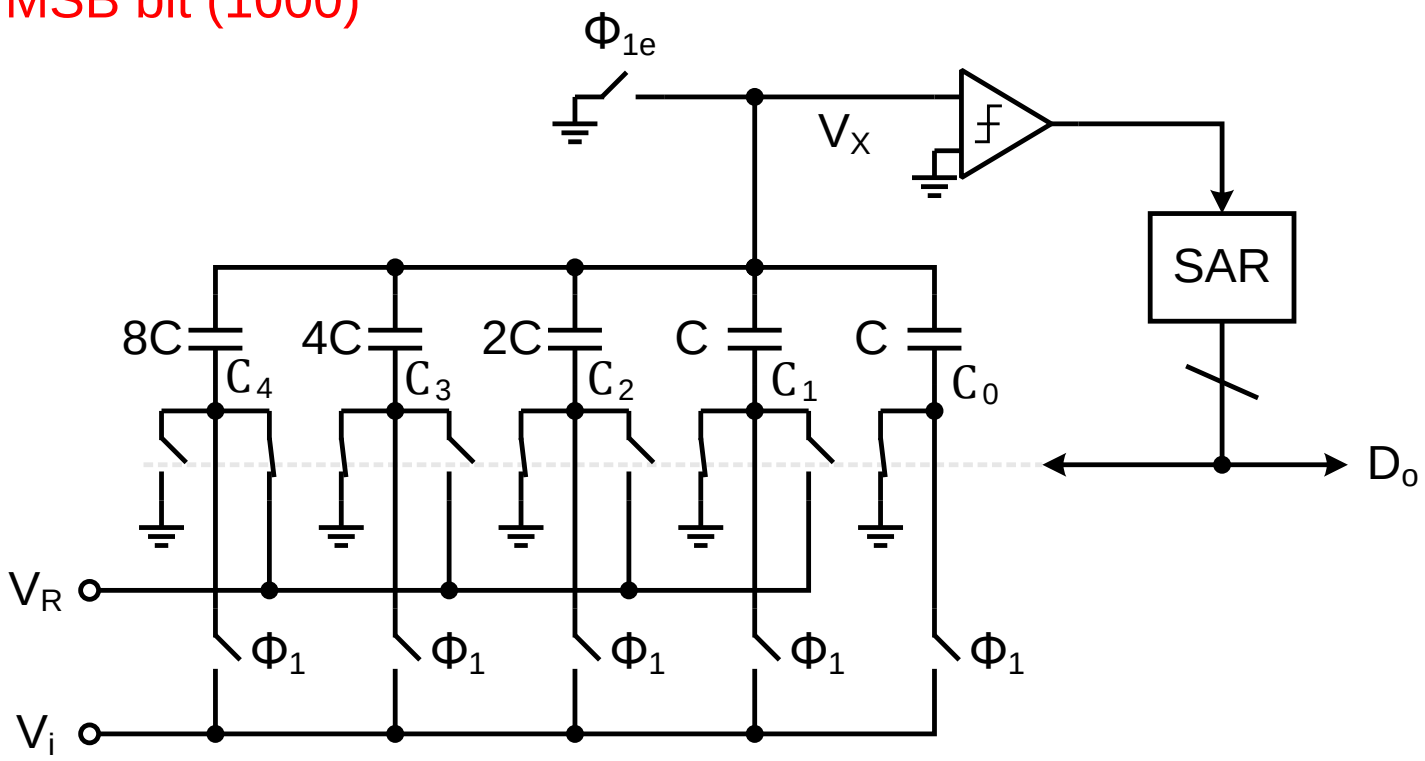
Charge Redistribution SAR ADC

Open $\emptyset_1$ and Apply 0000 → $V_x = -V_i$



Charge Redistribution SAR ADC

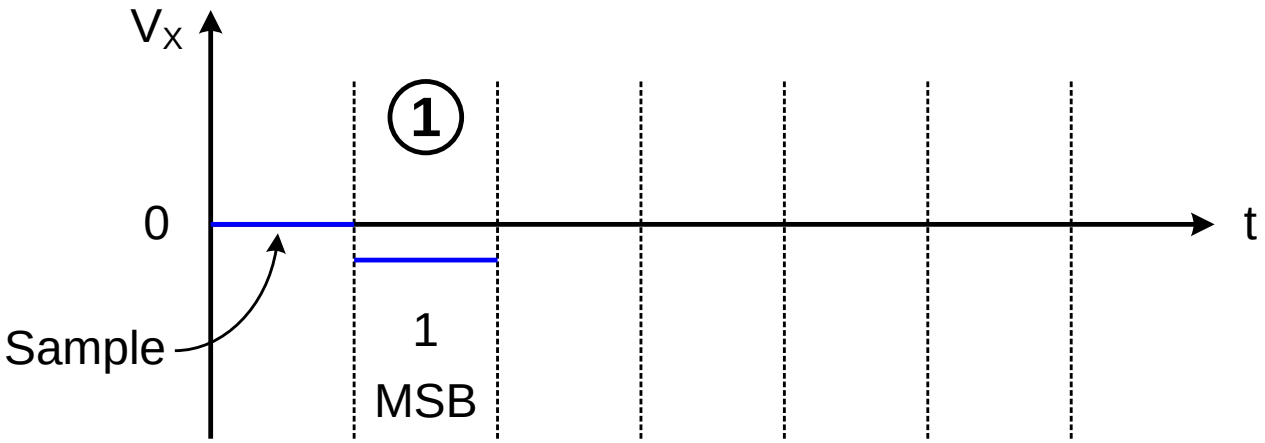
Apply MSB bit (1000)



$$V_x = -V_i + \frac{8C}{16C} V_R = -V_i + \frac{V_R}{2}$$

Charge Redistribution SAR ADC

Decide MSB bit position

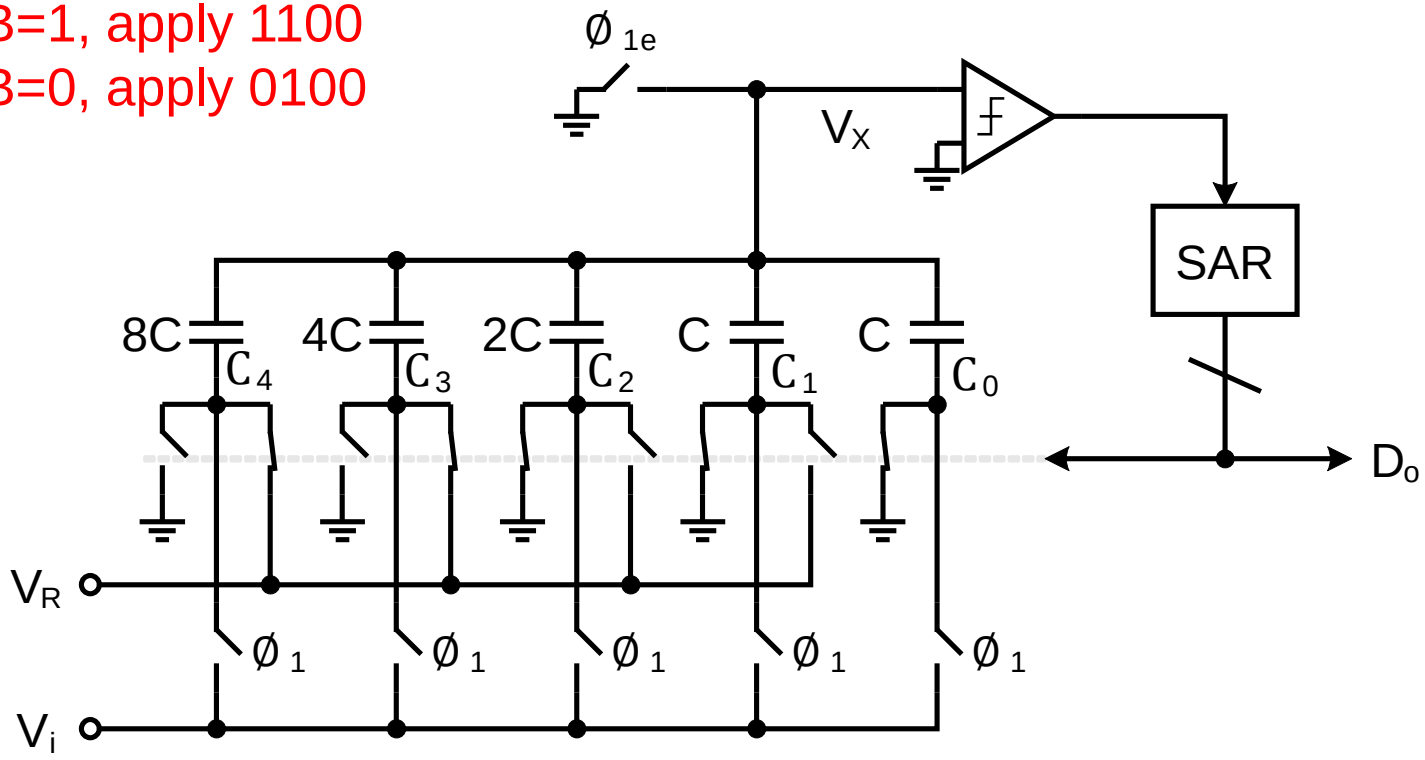


$$\text{MSB TEST}: \; V_X = \frac{V_R}{2} - V_i$$

- If $V_X < 0$, then $V_i > V_R/2$, and MSB = 1, C_4 (=8C) remains connected to V_R
- If $V_X > 0$, then $V_i < V_R/2$, and MSB = 0, C_4 is switched to ground

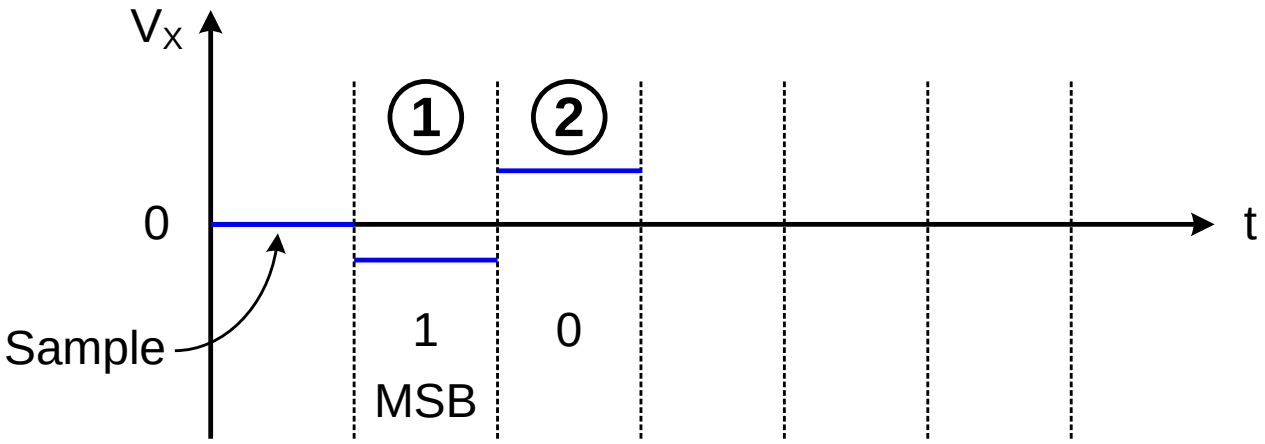
Charge Redistribution SAR ADC

Continue next bit decision.
If MSB=1, apply 1100
If MSB=0, apply 0100



$$V_x = -V_i + \frac{V_R}{2} + \frac{4C}{16C}V_R = -V_i + \frac{3V_R}{4}$$

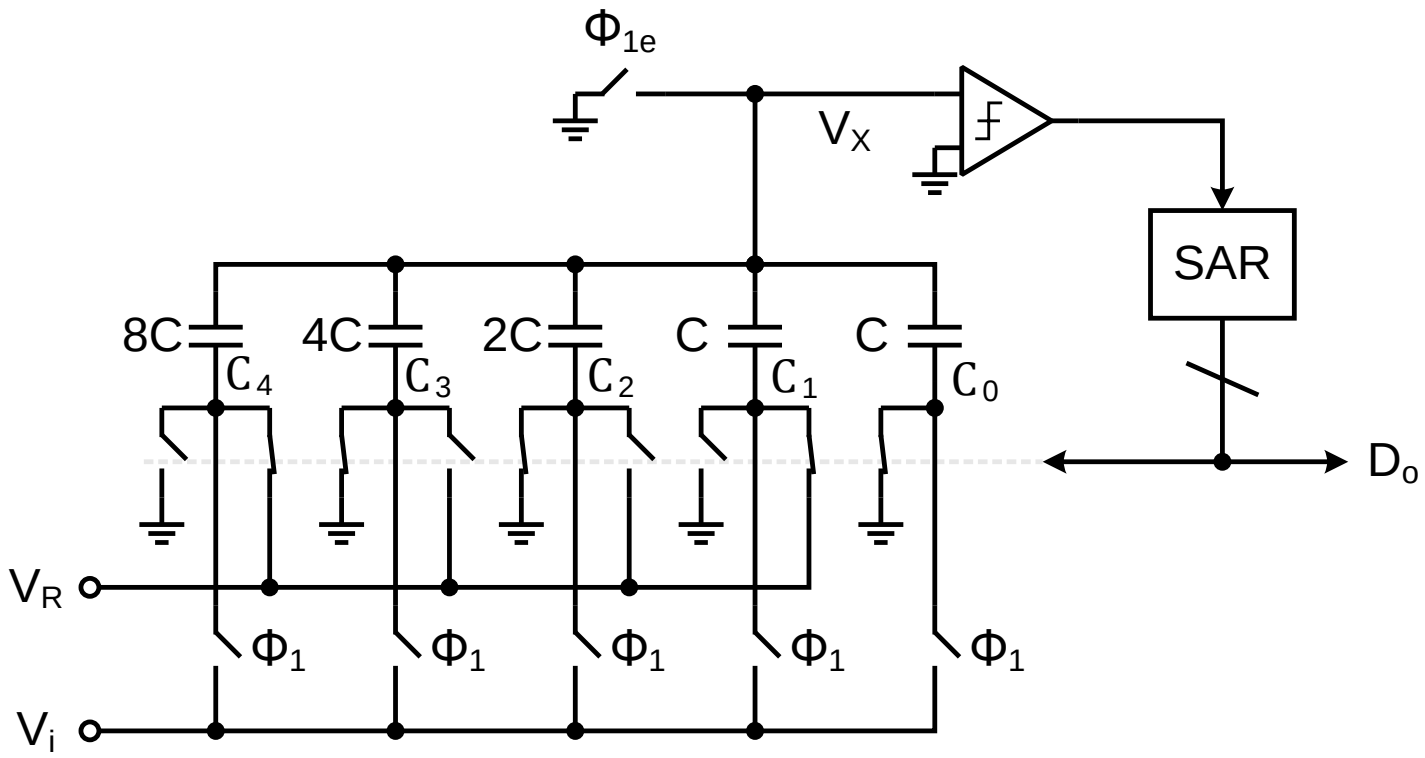
Charge Redistribution SAR ADC



$$(\text{MSB-1})\ \text{TEST}:\ V_X = \frac{3}{4}V_R - V_i$$

- If $V_X < 0$, then $V_i > 3V_R/4$, and MSB-1 = 1, C_3 remains connected to V_R
- If $V_X > 0$, then $V_i < 3V_R/4$, and MSB-1 = 0, C_3 is switched to ground

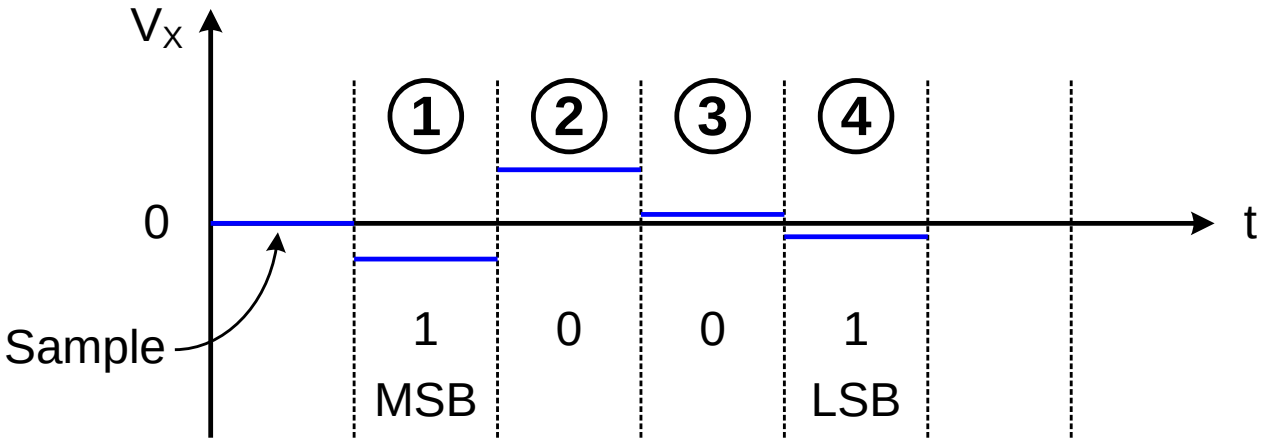
Charge Redistribution SAR ADC



Test completes when all four bits are determined w/ four charge redistributions and comparisons

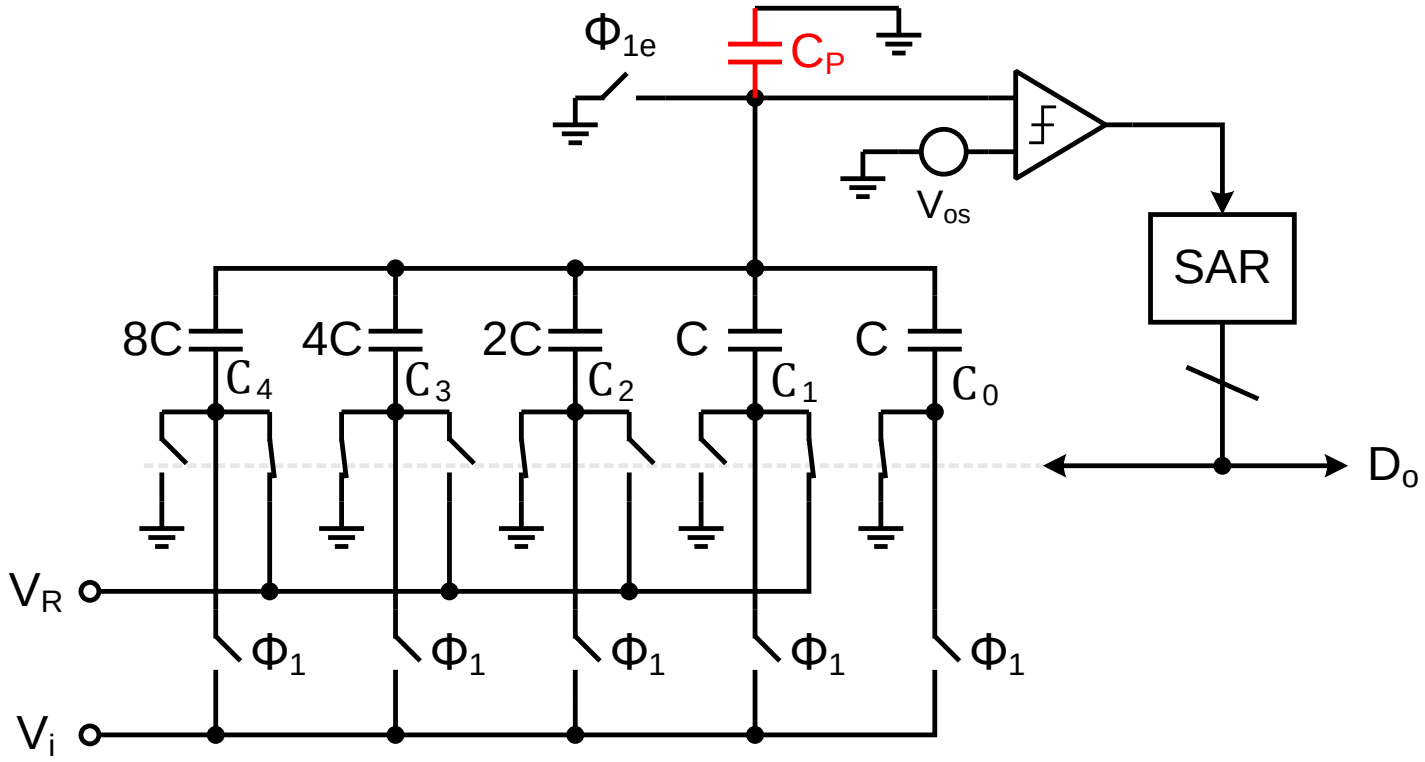
Charge Redistribution SAR ADC

After 4-bit decision



- Usually, half T_{clk} is allocated for charge redistribution and half for comparison + digital logic
- V_X always converges to 0 (V_{os} if comparator has nonzero offset)

Summing Node Parasitic



- If V_{os} = 0, C_P has no effect eventually; otherwise, C_P attenuates V_X
- Auto-zeroing can be applied to the comparator to reduce offset

Charge Redistribution SAR ADC

- Power efficiency
  - Only comparator consumes DC power
- Switching Energy can be significant
  - Reducing switching energy is an active research area
- DAC nonlinearity limits the INL and DNL of the SAR ADC
  - N-bit precision requires N-bit matching from the cap array
  - Calibration can be performed to remove mismatch errors
- Binary search is sensitive to intermediate errors made during the search
  - DAC must settle into ±½ LSB bound within the time allowed
  - Comparator offset must be constant (no hysteresis or time-dependent offset)