Systematic Design for a Successive Approximation ADC

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Outline

- Background
- Principles of Operation
- System and Circuit Design
- Case Study
  - Simulations
  - Layout Generation
  - Performance Evaluation
- Conclusion
- Perspectives

The Successive Approximation ADC « The Return»

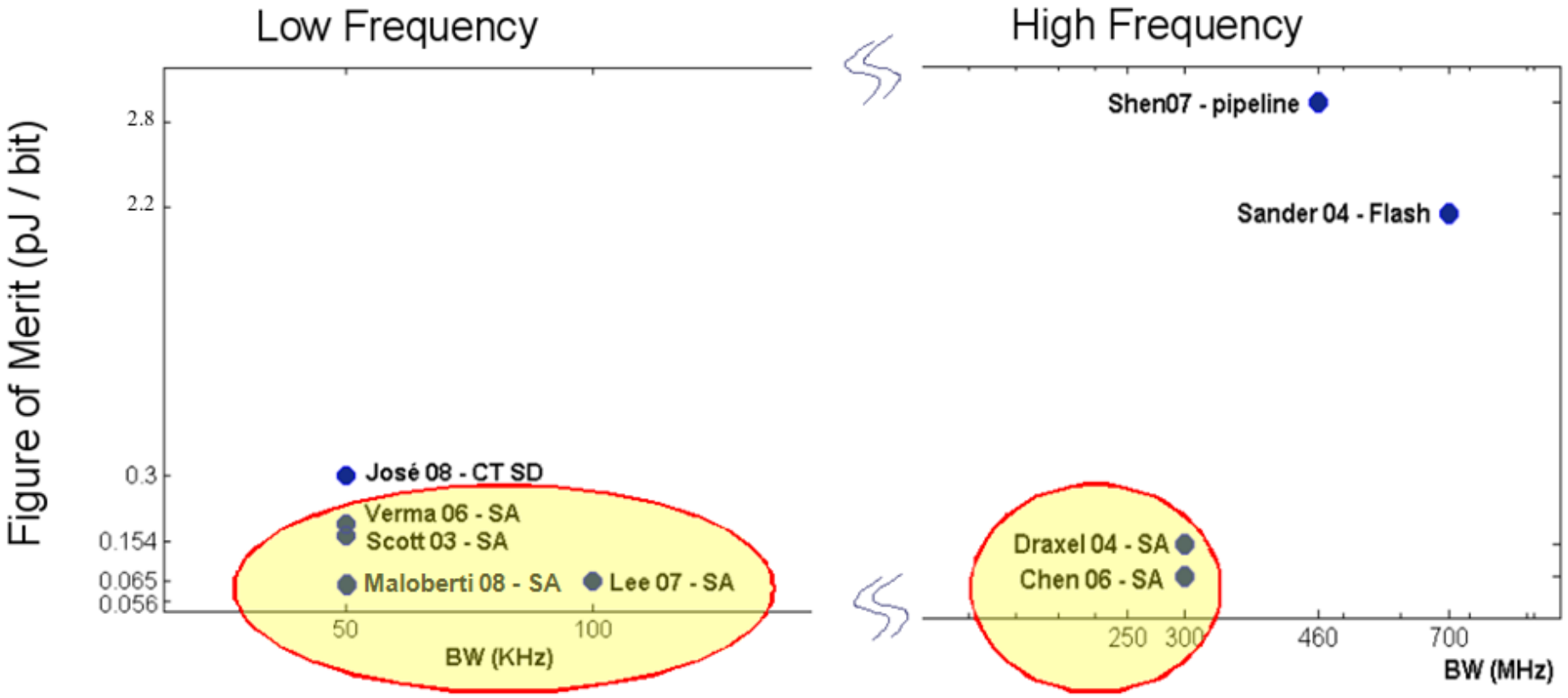
- Emerging new Applications
  - MEMS Sensor Interface:

    Resolution: 7-8 bits, BW=50kHz [Scott 2003]
  - Multi-standards RF receiver

    Resolution: 8 bits, BW = 20 MHz [Montaudon 2008]
  - Ultra Wide Band (wireless UWB):

    Resolution: 5-6 bits, BW=300MHz [Chen 2006]

Figure of Merit

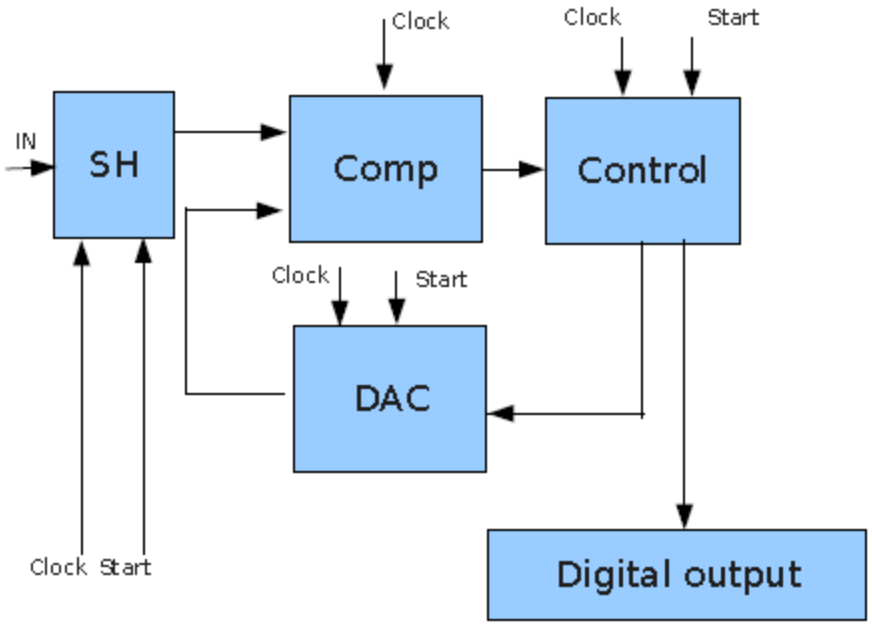


$$\text{FOM} = \frac{P}{2^{\text{Resolution}} * 2 * BW}$$

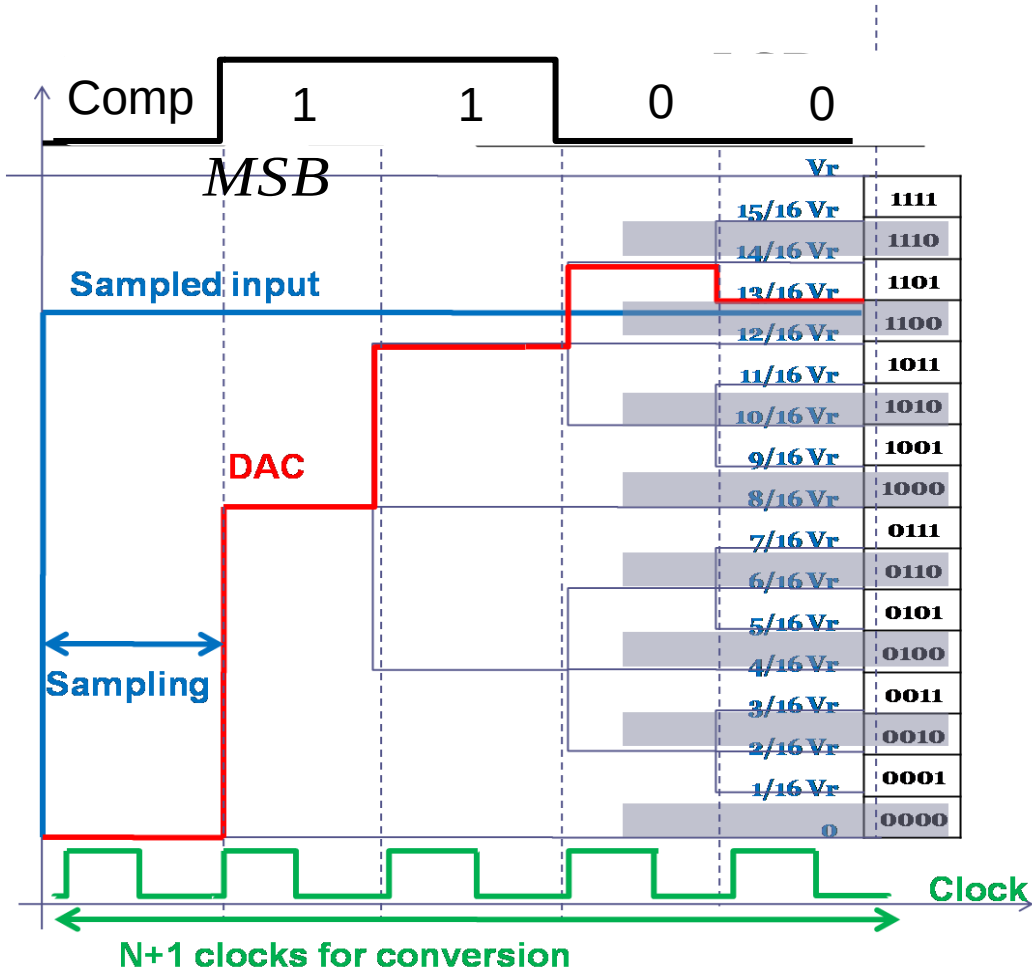
Objectives

- Develop a systematic design method for successive approximation ADC from system to layout level .
- Develop a general simulation environment with different levels of abstraction and programmed performance analysis.
- Emphasis on analog design automation and reuse techniques:
  - Automatic sizing
  - Layout generation
- Optimizing Layout for best matching

Principle of Operation



$$Vin = b_1 \frac{V_{REF}}{2} + b_2 \frac{V_{REF}}{4} + b_3 \frac{V_{REF}}{8} + b_4 \frac{V_{REF}}{16}$$



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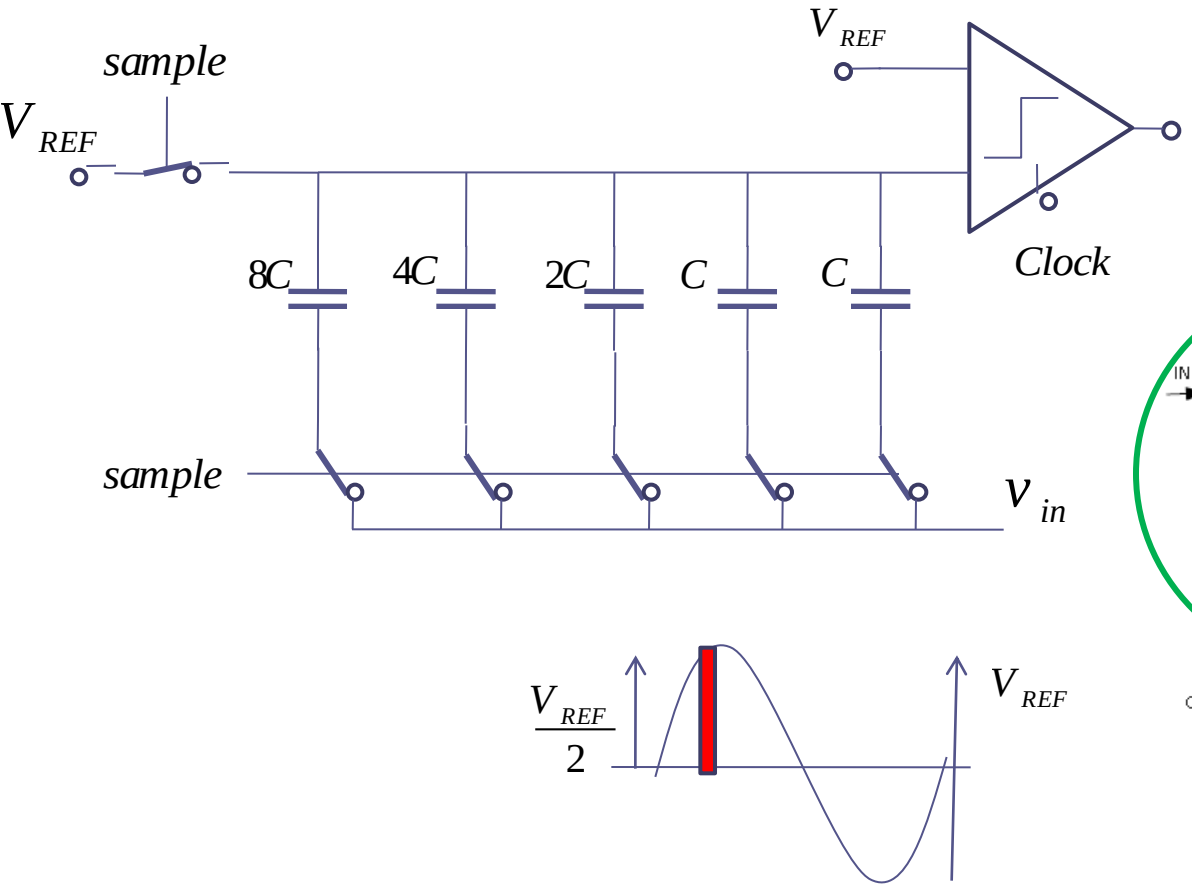
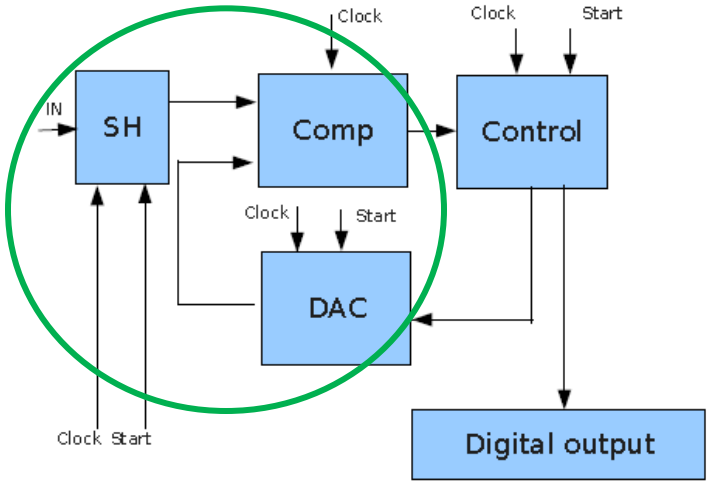
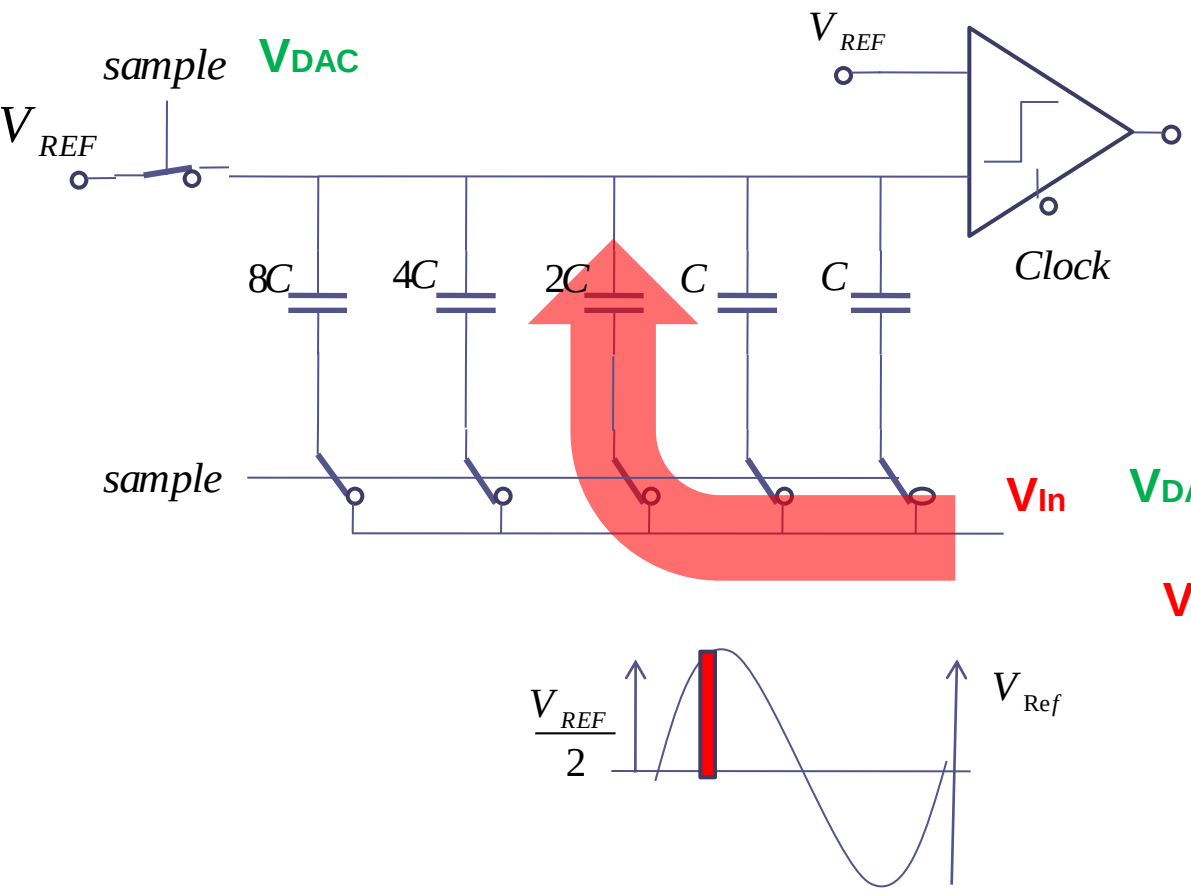
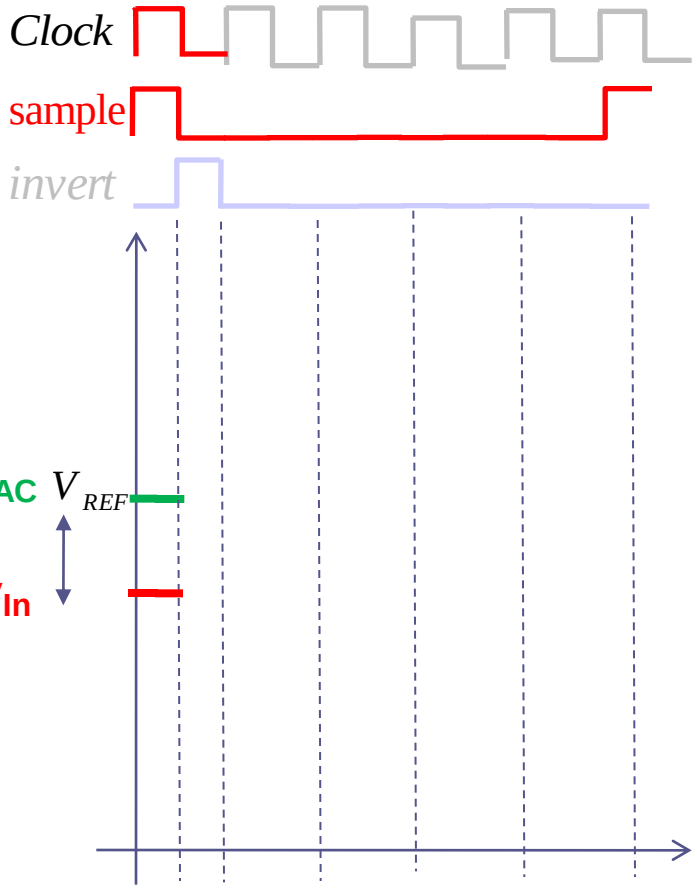
Single Ended SAR-ADC.



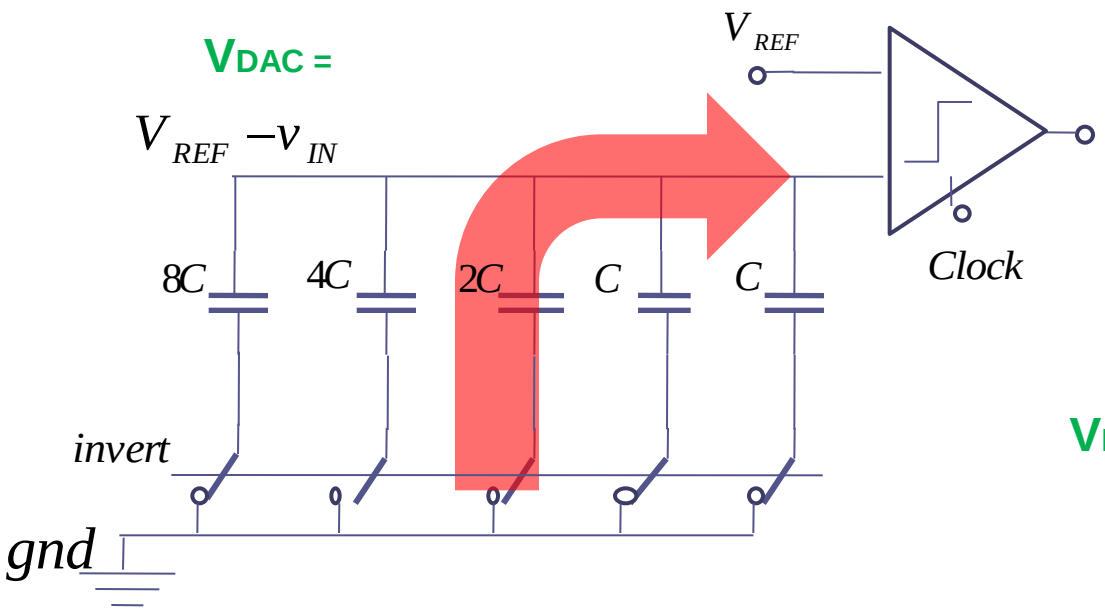


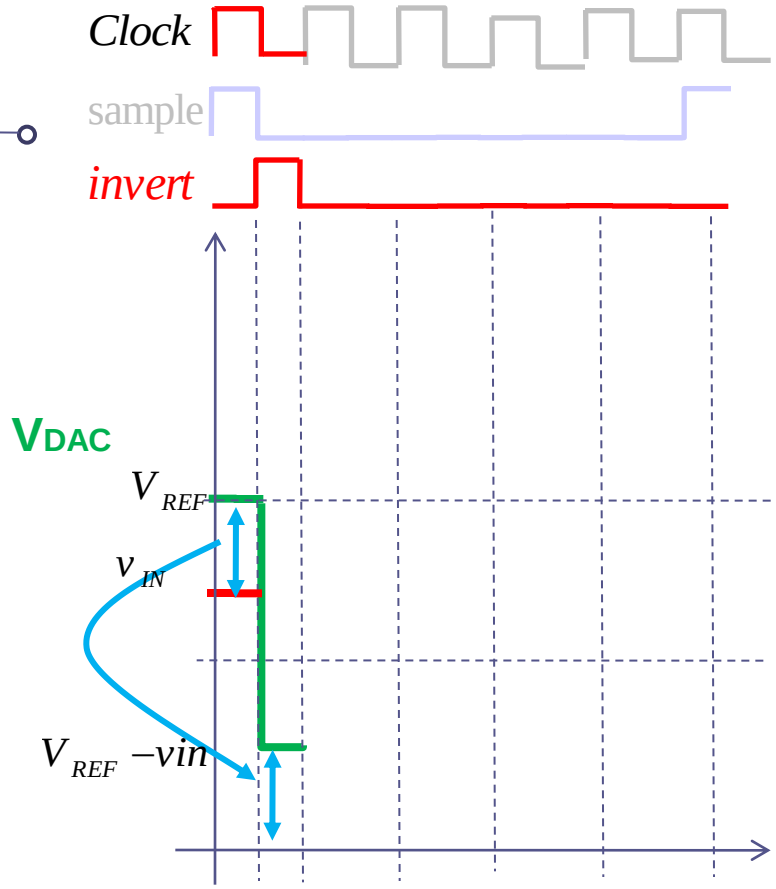
Sampling Mode



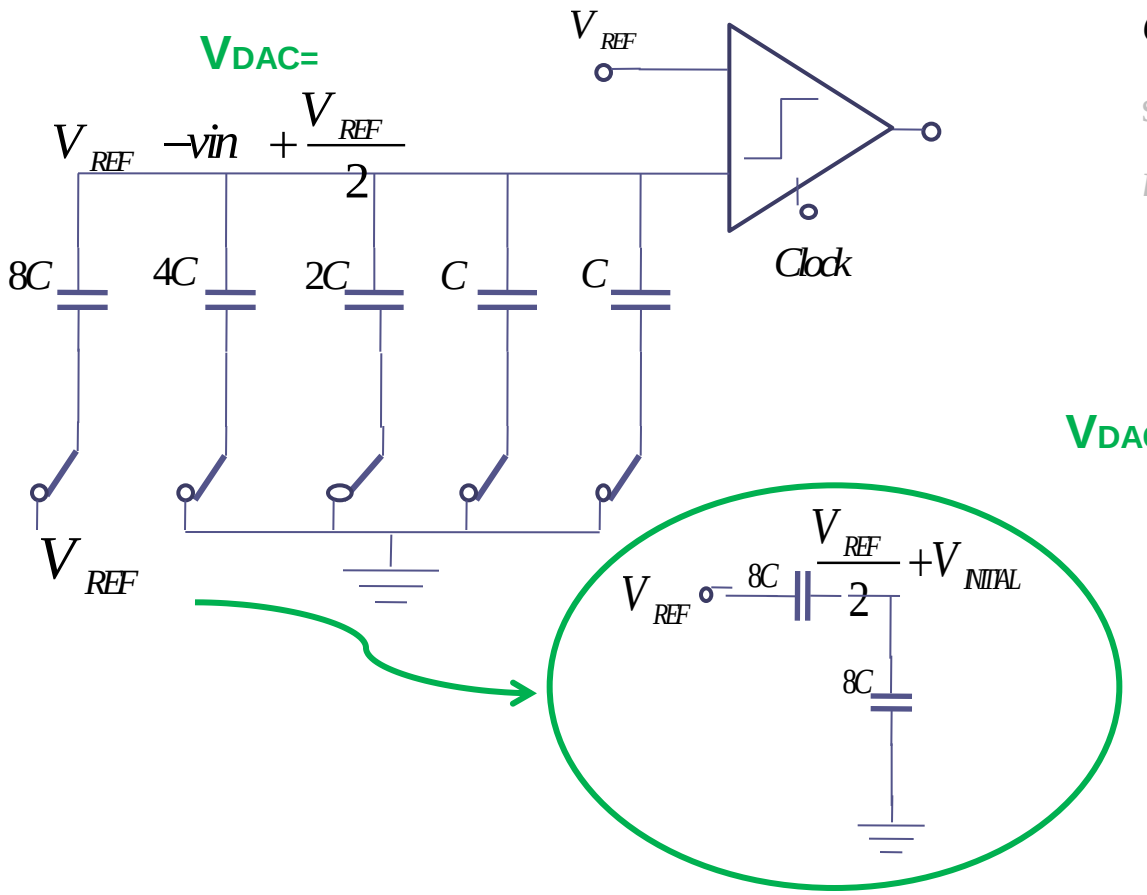


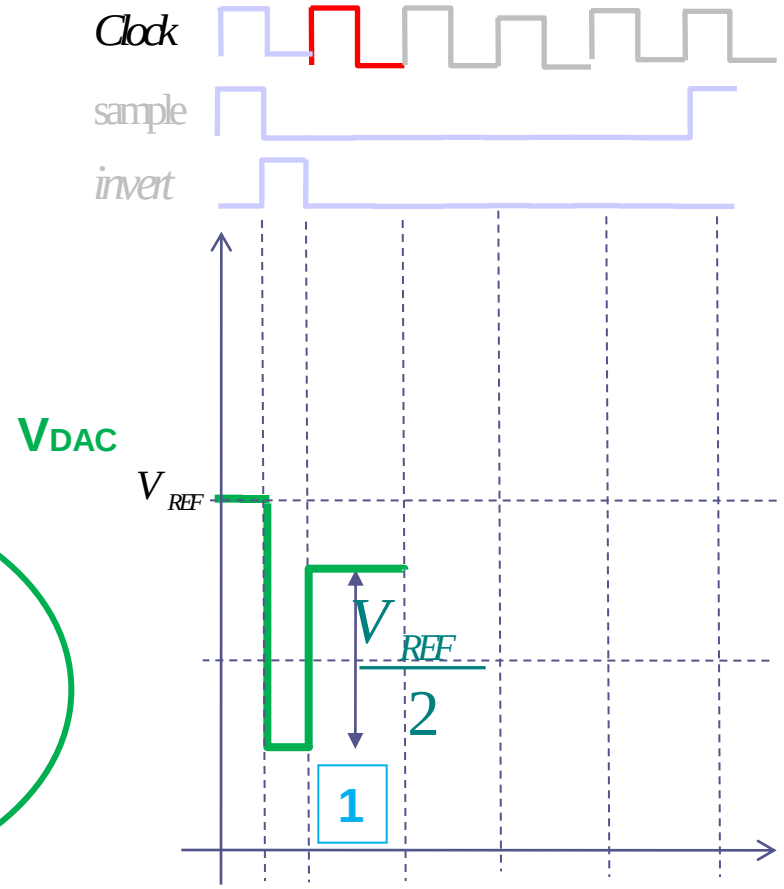
Inversion Mode



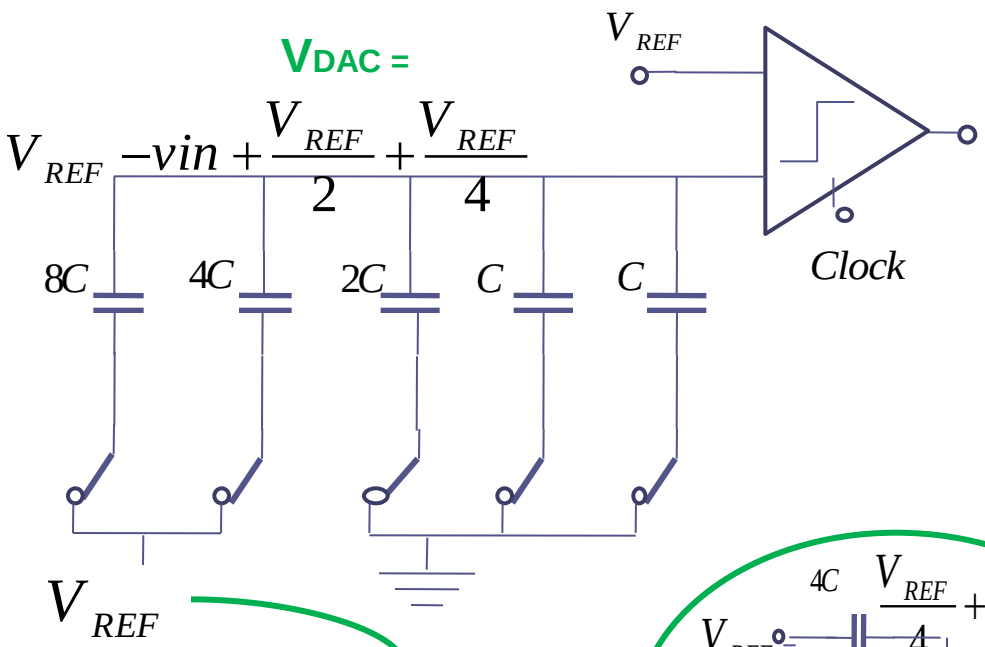


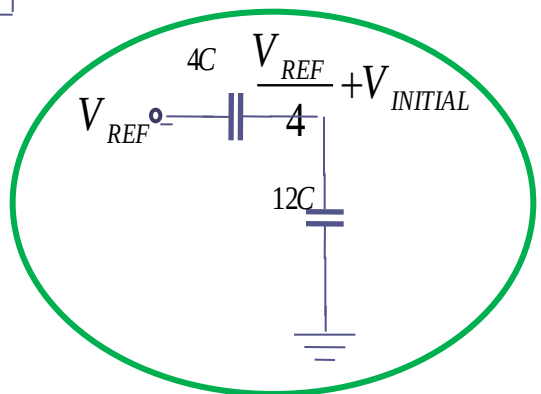
Charge redistribution mode (MSB)

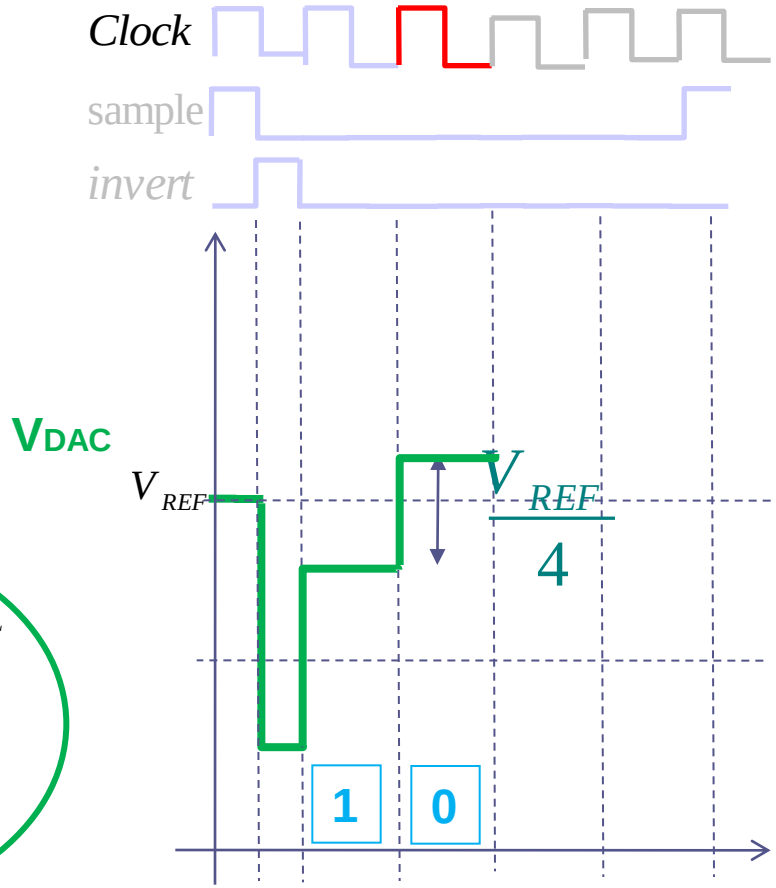




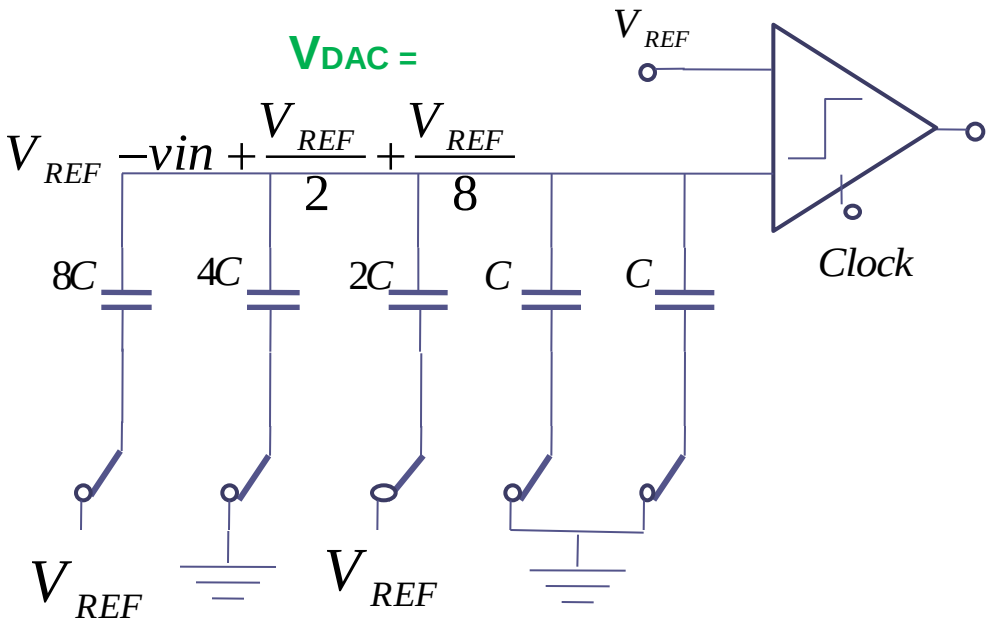
Charge redistribution mode (MSB-1)

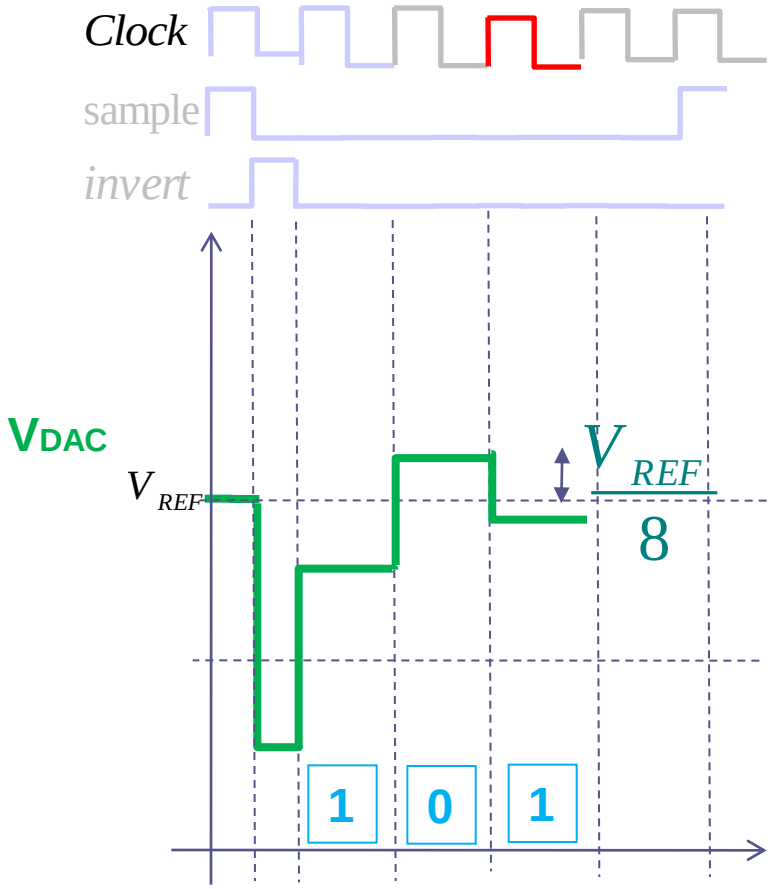






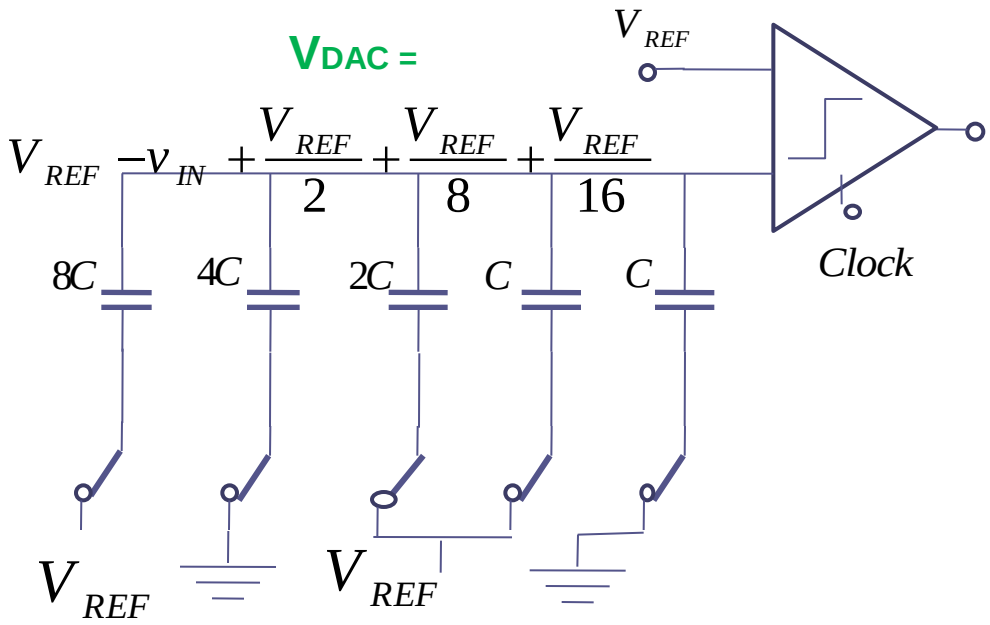
Mode Redistribution de la charge (MSB-2)



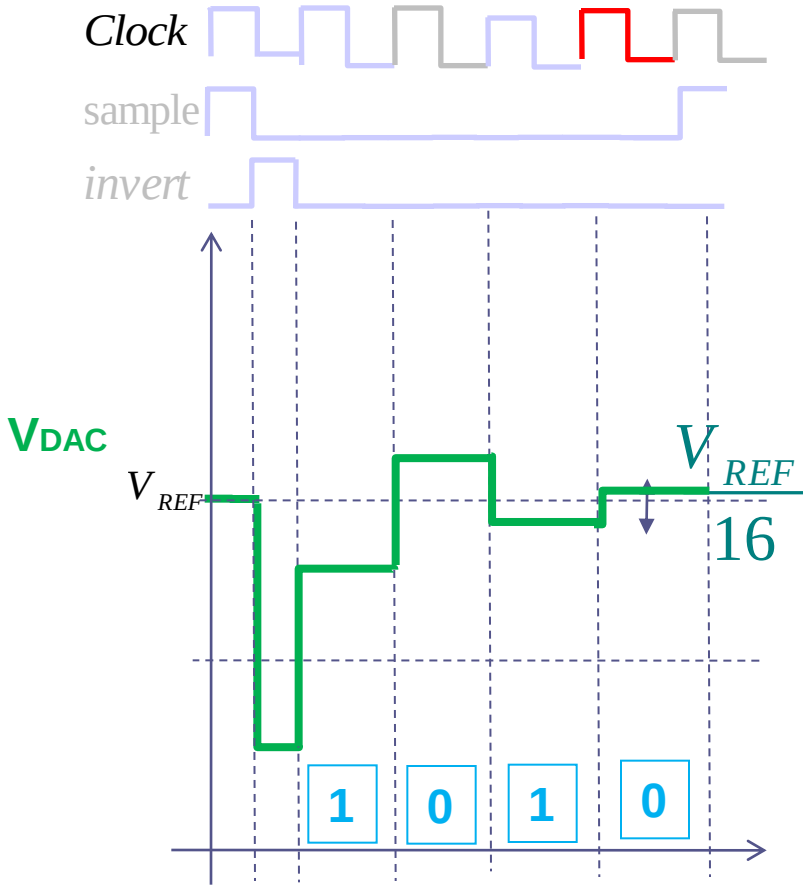


$$Vin = b_1 \frac{V_{REF}}{2} + b_2 \frac{V_{REF}}{4} + b_3 \frac{V_{REF}}{8} + b_4 \frac{V_{REF}}{16}$$

Mode Redistribution de la charge (LSB)

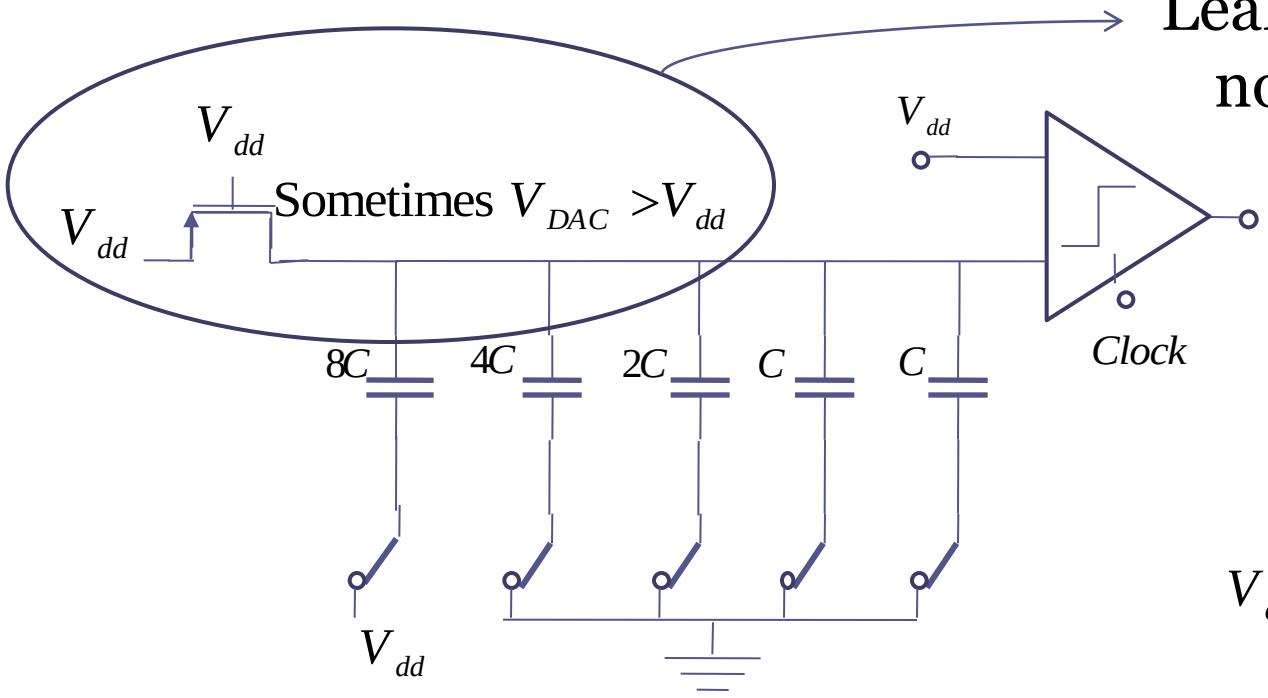


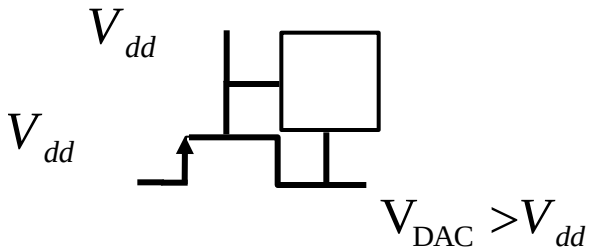
$$Vin = b_1 \frac{V_{REF}}{2} + b_2 \frac{V_{REF}}{4} + b_3 \frac{V_{REF}}{8} + b_4 \frac{V_{REF}}{16}$$



Problem

Selecting $V_{REF} = V_{dd}$ To increase the dynamic range

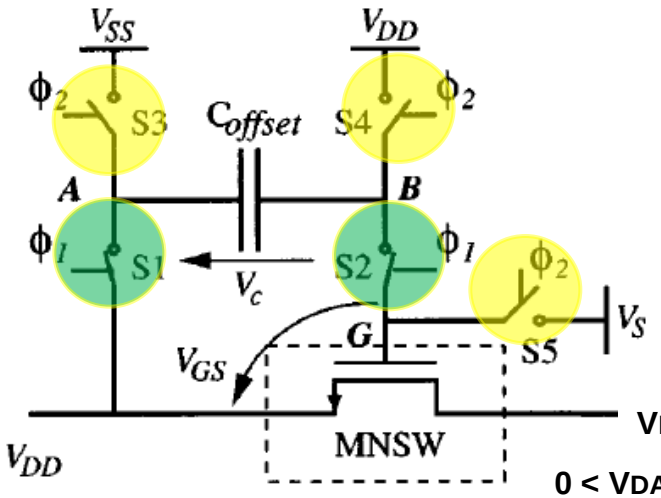




Possible Solution: Switched *charge-pump* [scott03] or *Bootstrap [dessouky01]*

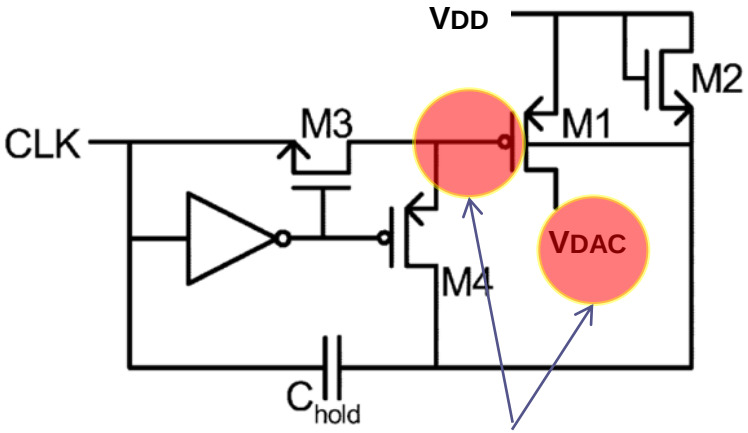
Possible solutions - Leakage

Bootstrap Switch

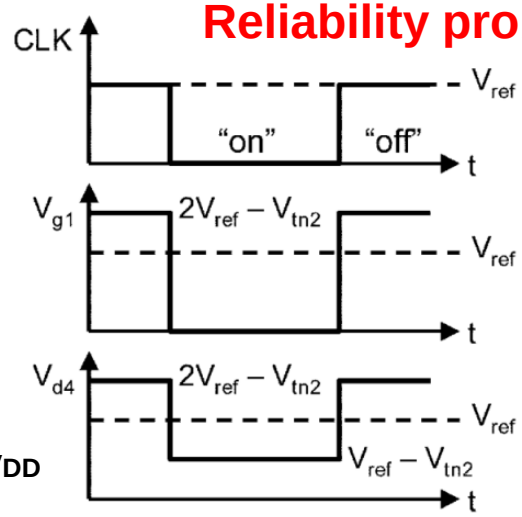


0 < VDAC < 1.5 VDD

Charge pump Switch

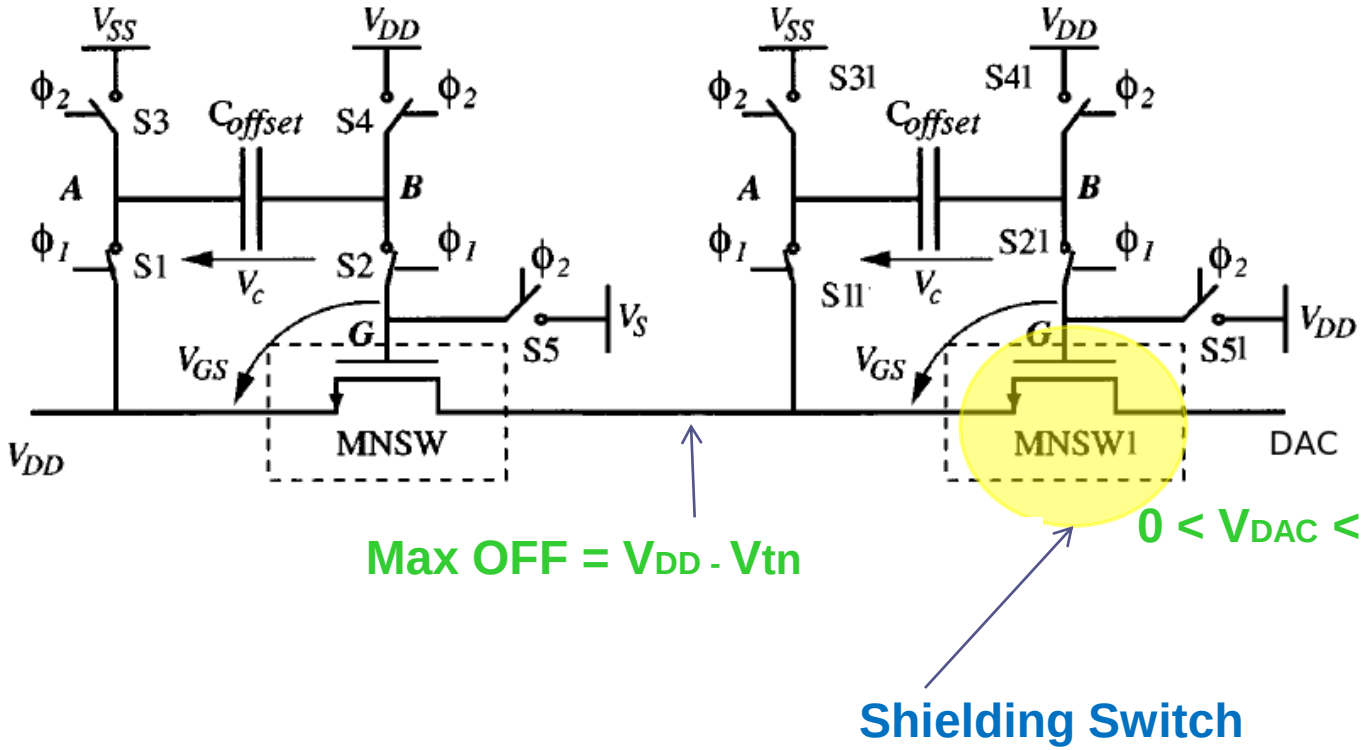


Reliability problem

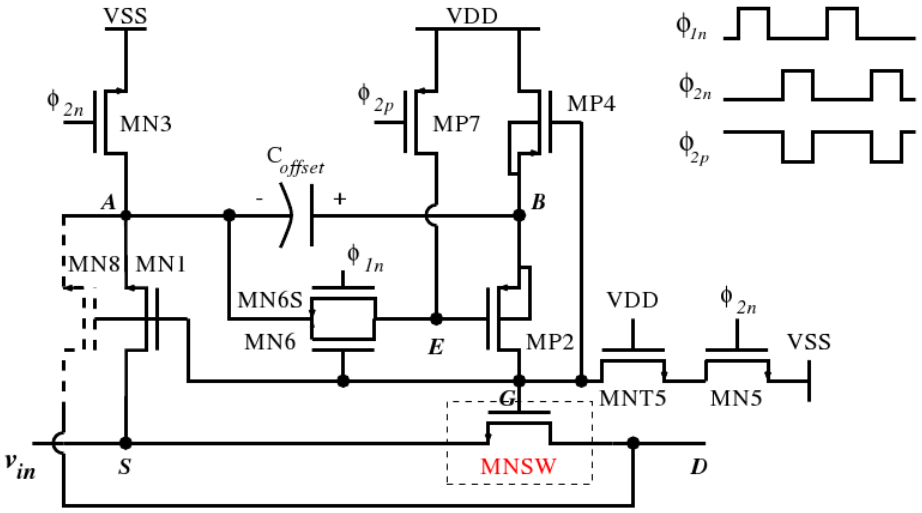


Since sometimes VDAC value=1.5 VDD
While VG1 = 0 when M1 is ON, VGD,M1 exceeds VDD

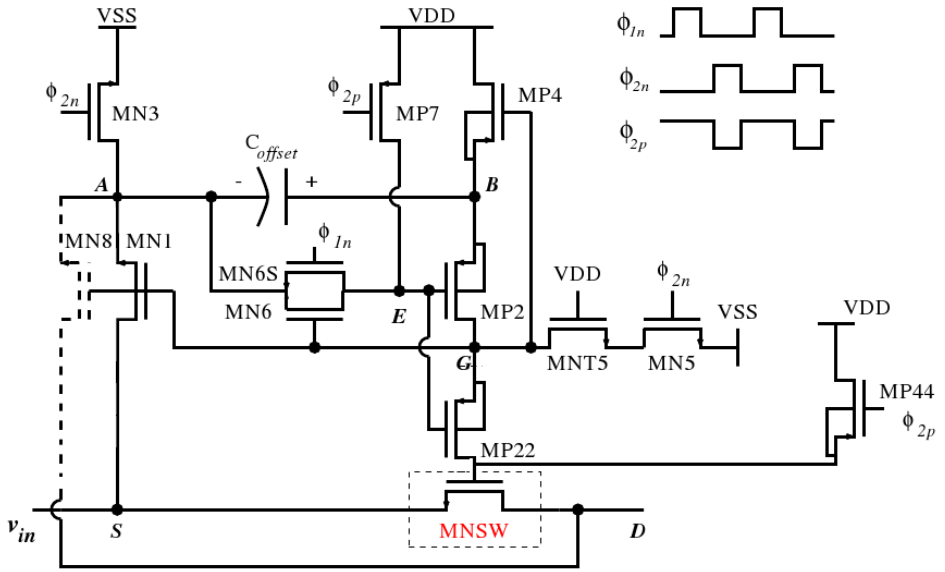
Possible solutions - Reliability



Possible solutions - Circuitry

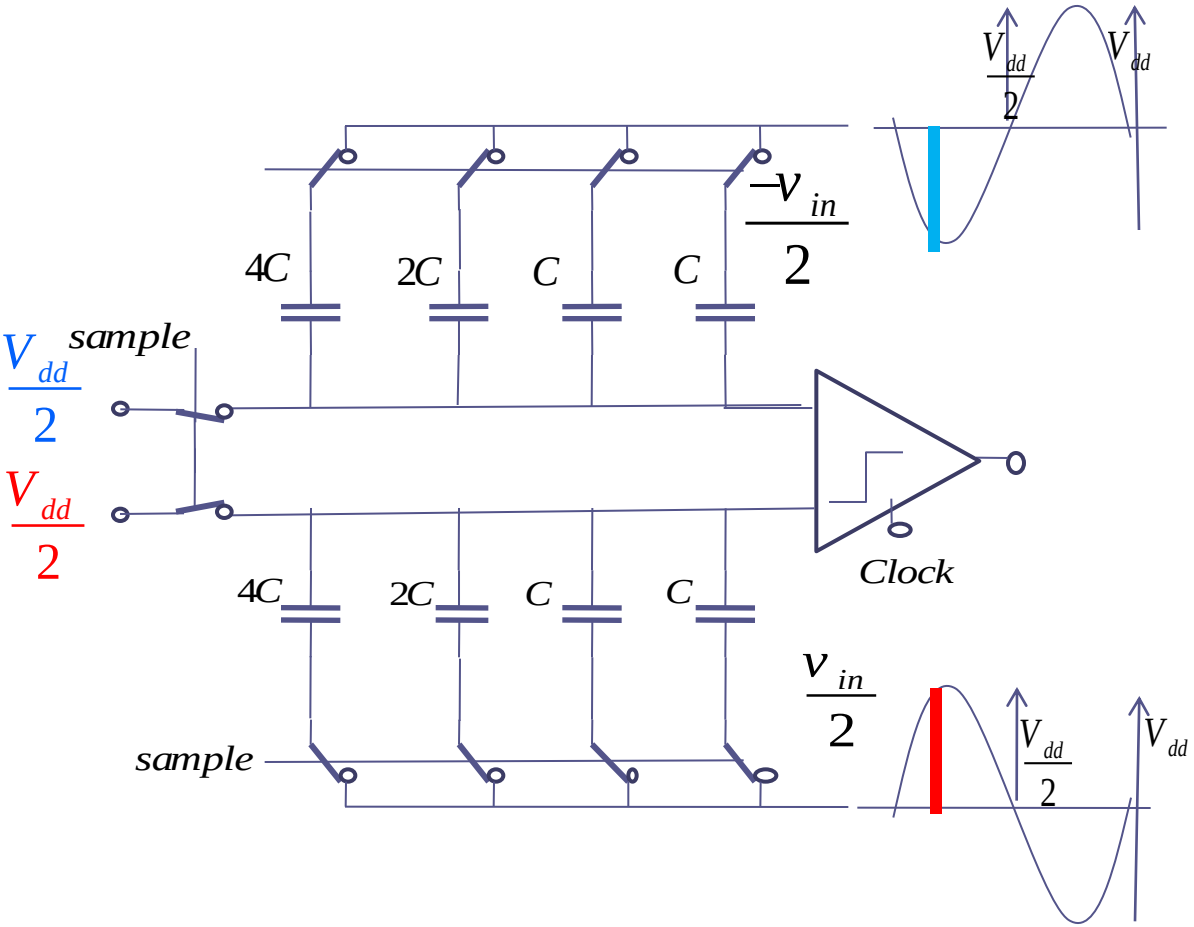


Bootstrap [dessouky01]



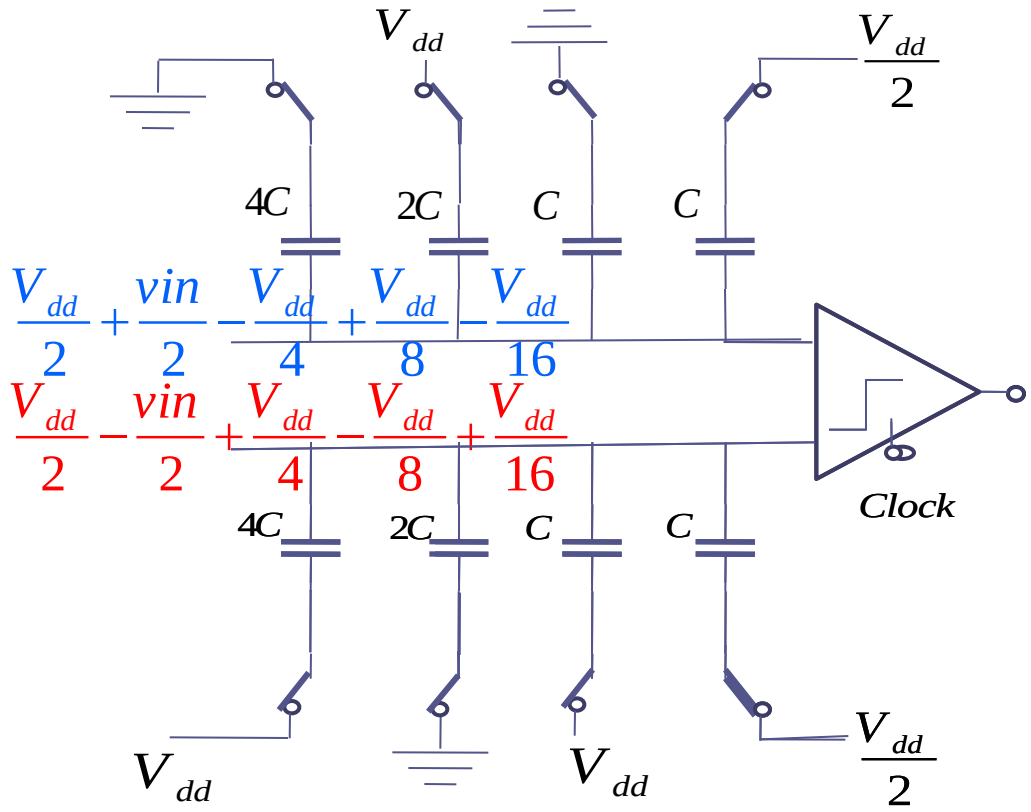
Modified Shielding Bootstrap

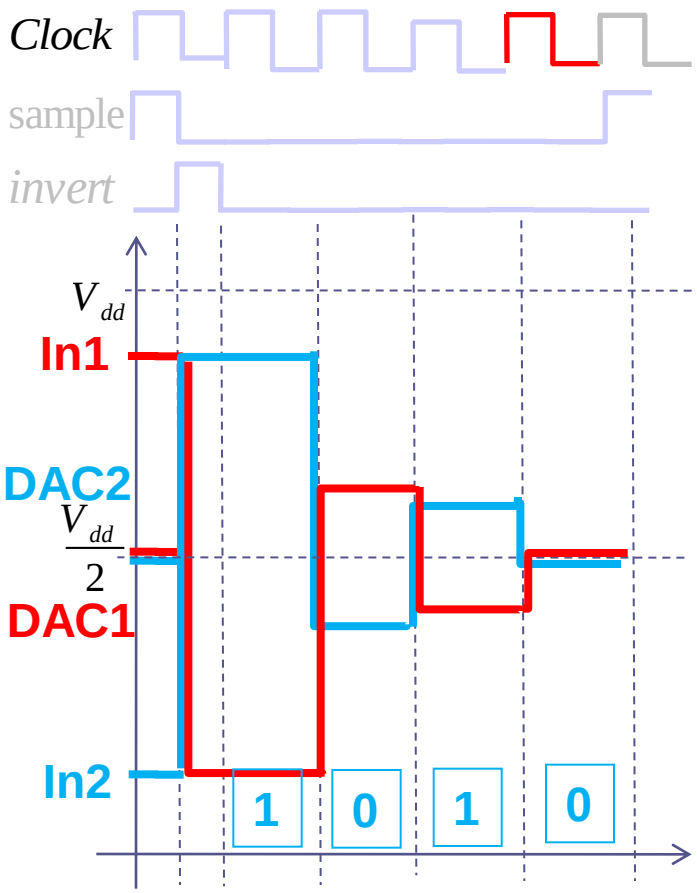
Differential SAR-ADC



Triple Reference

Differential SAR-ADC





Operation – Summary

Single Ended Double reference	Differential Triple reference
	2 times the numbers of capacitors 6 times the numbers of switches
Special Switch (*charge-pump - bootstrap)*	No need for special switch
	Differential architectures advantages : - Suppressing even harmonics -Common mode rejection -Offset removal
Lower power consumption	Better performance at high frequencies

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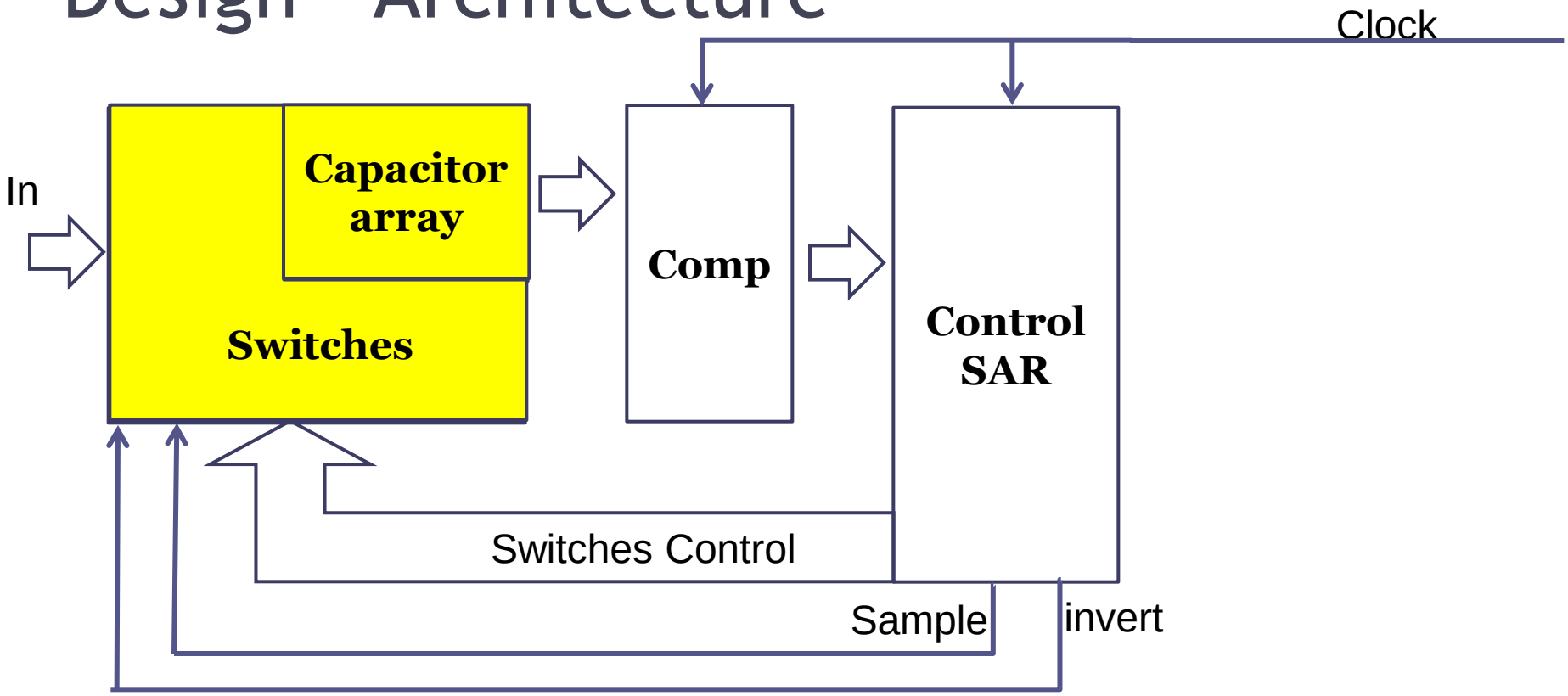
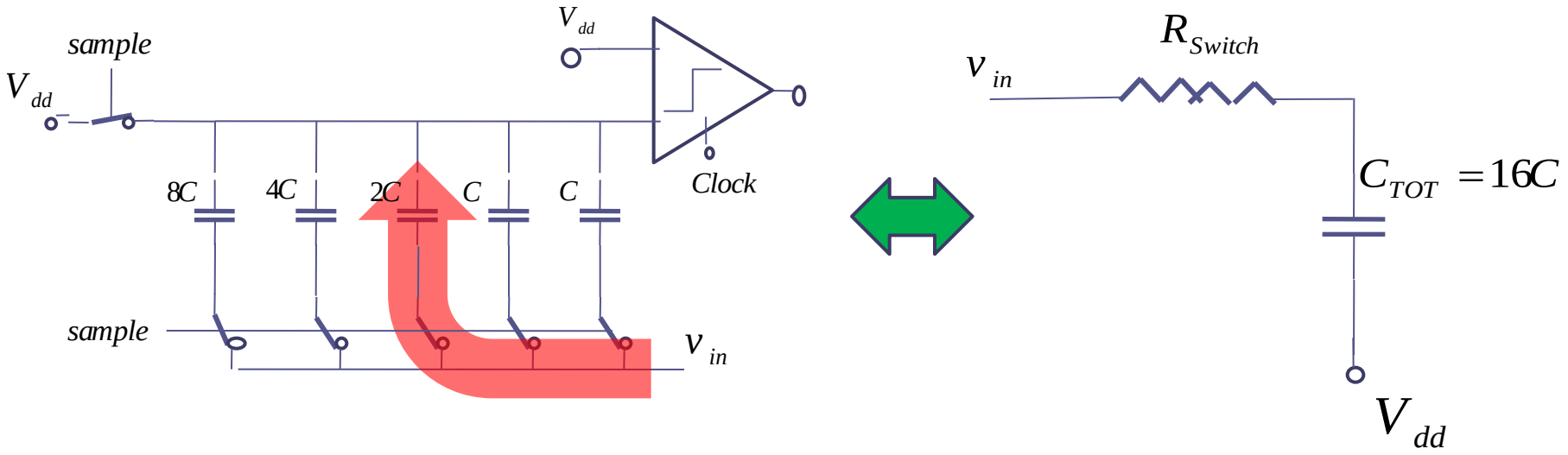
Design - Architecture



Capacitor array design issues - Noise

1- Thermal noise [$\frac{kT}{C_{TOT}}$], due to Sampling

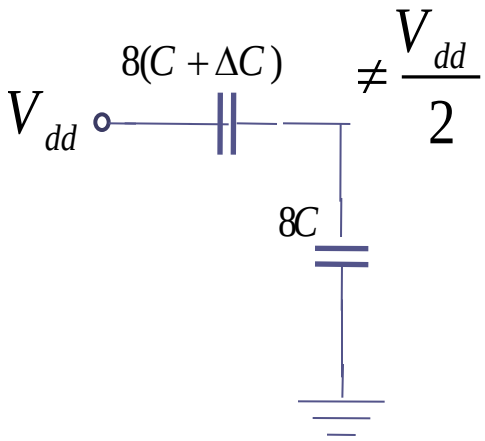


C_{Unit} increases, thermal noise decreases

Capacitor array design issues - Mismatch

2 – Capacitor Mismatch (Introduced in fabr ication)

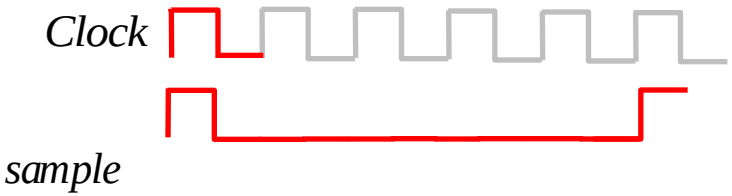
- Affects Generated comparison levels of the capacitve DAC

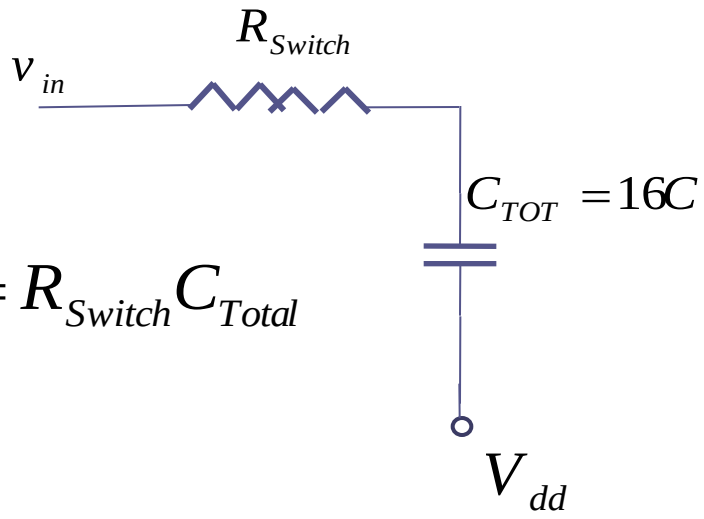


C_{Unit} increases, mismatch effect decreases

Capacitor array design issues - $f_{Sampling}$

3- Sampling Frequency





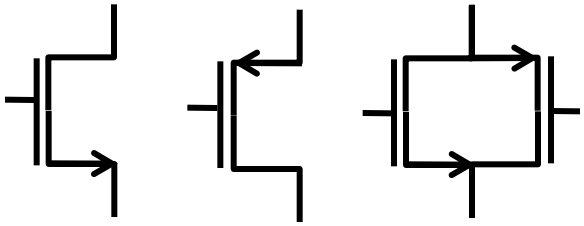
$$\tau = R_{Switch} C_{Total}$$

$$t_{sampling} \approx \frac{T_{Clock}}{2} >> \tau$$

For an accurate sampling

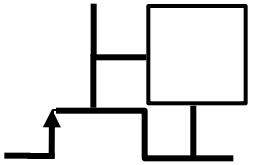
C_{Unit} decreases, bandwidth increases

Switches



1) Switches selection

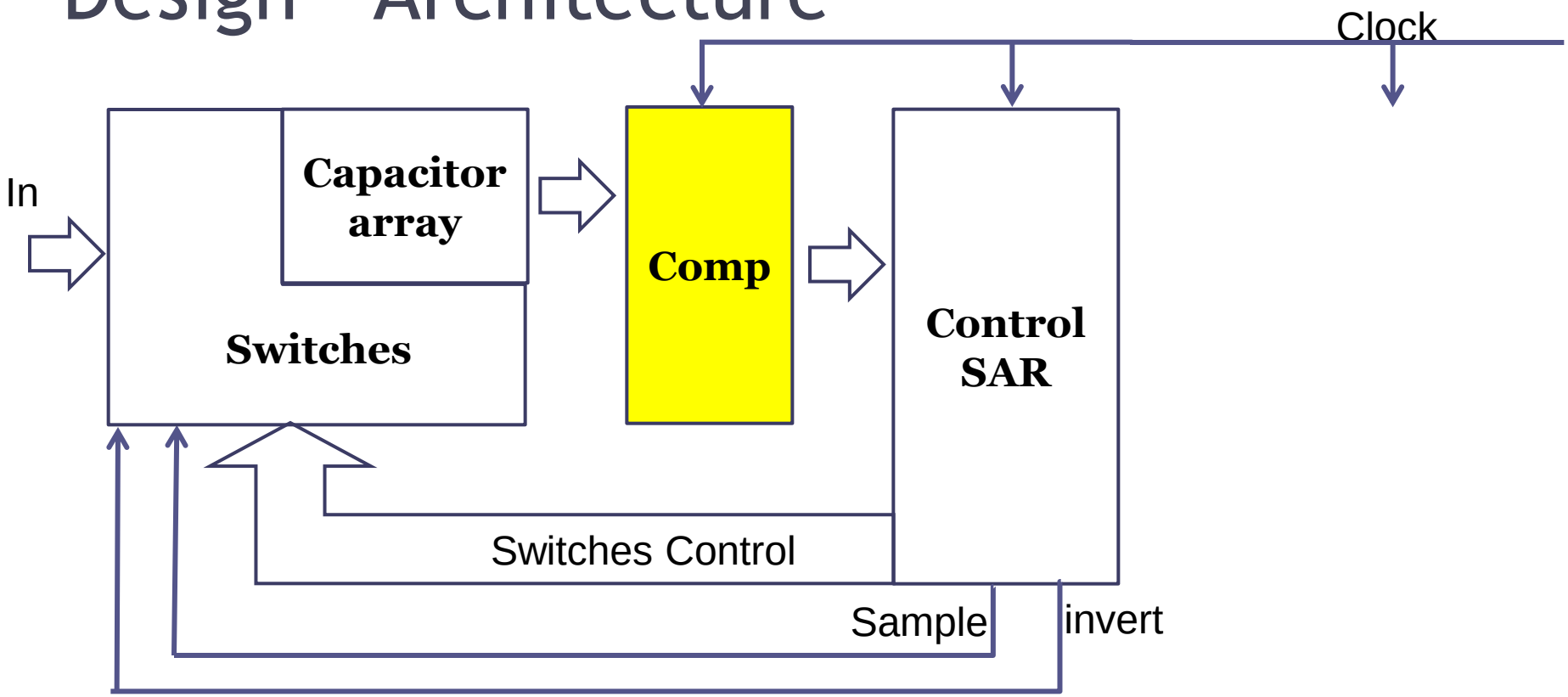
- NMOS to switch V_{gnd} and V_{cm}
- PMOS to switch V_{dd}
- CMOS to switch V_{in}
- Bootstrap to force deep off-state of critical switches



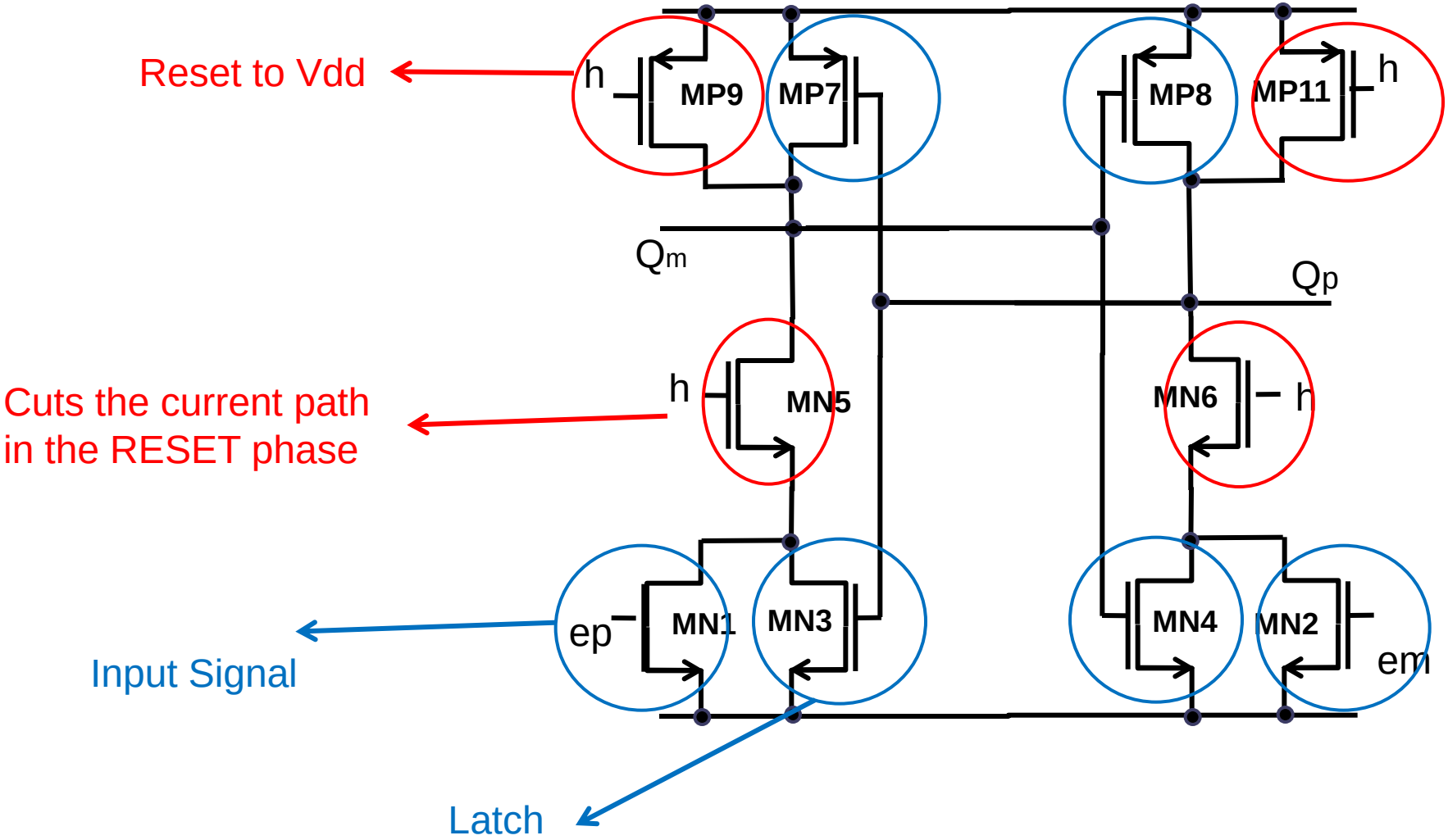
2) Sizing switches (compromise)

- Increasing W/L reduces Rswitch and so τ, on the account of increasing switch parasitcs.
- In the used DAC, this will be of minor importance if operating in low frequency because the switches are all connected to the bottom plates

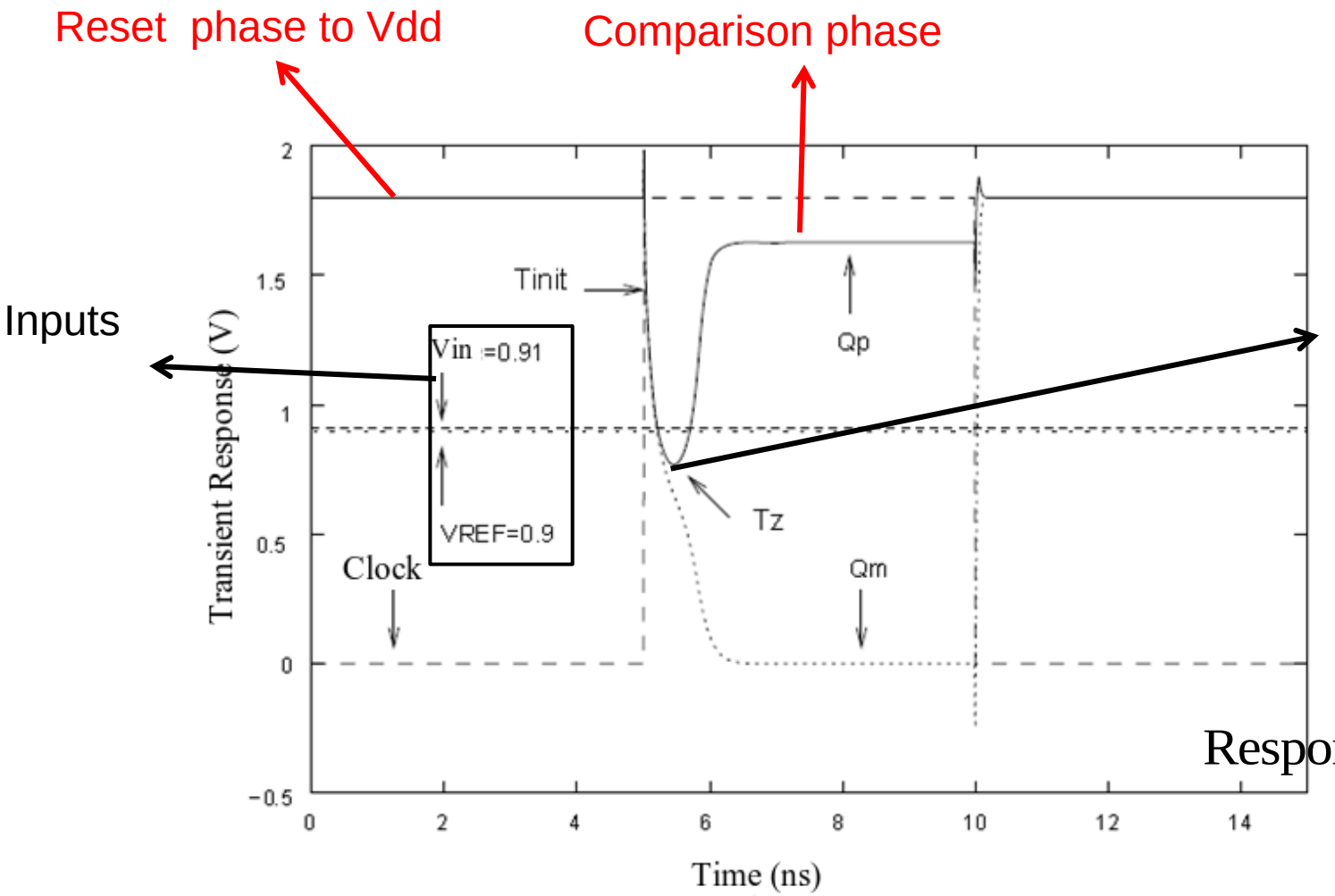
Design - Architecture



Comparator Circuit



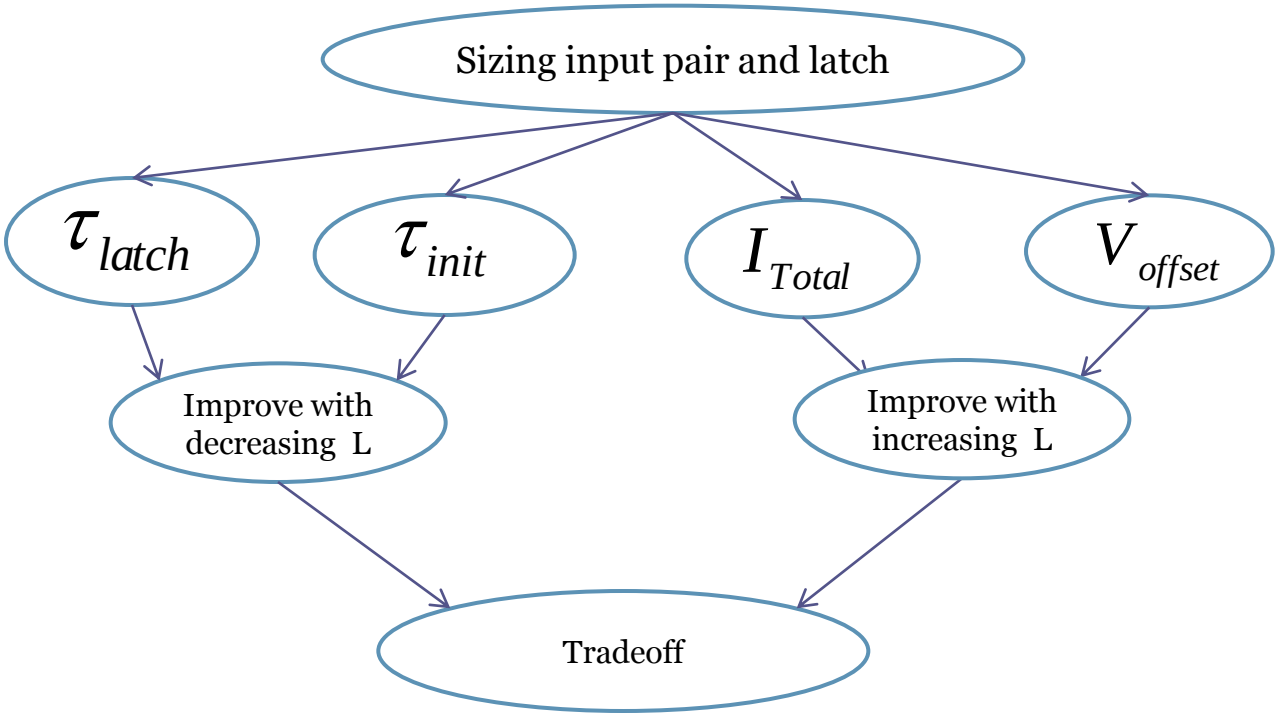
Comparator – Operation phases



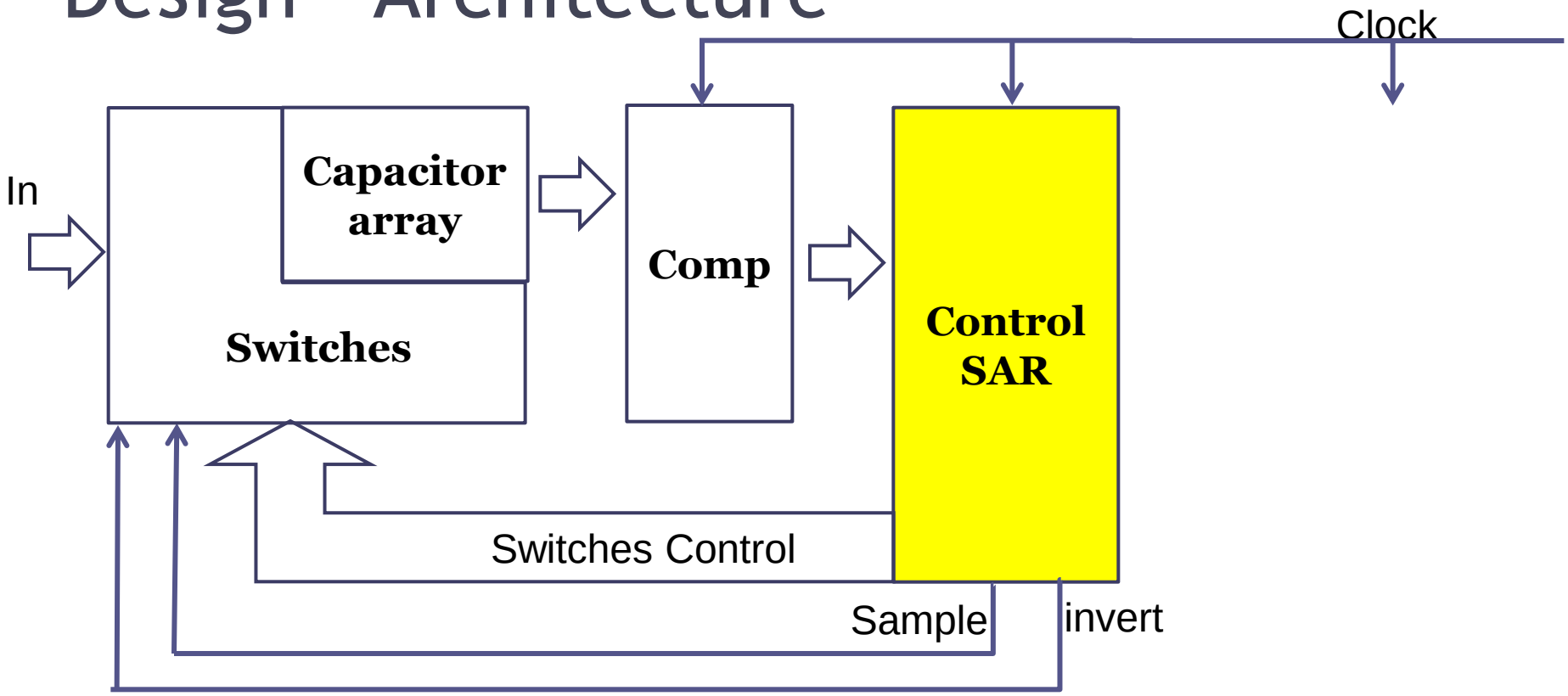
$$\text{Resolution} > \frac{V_{LSB}}{2}$$

$$\text{Response time} < 0.5\ T_H$$

Comparator – Design tradeoff

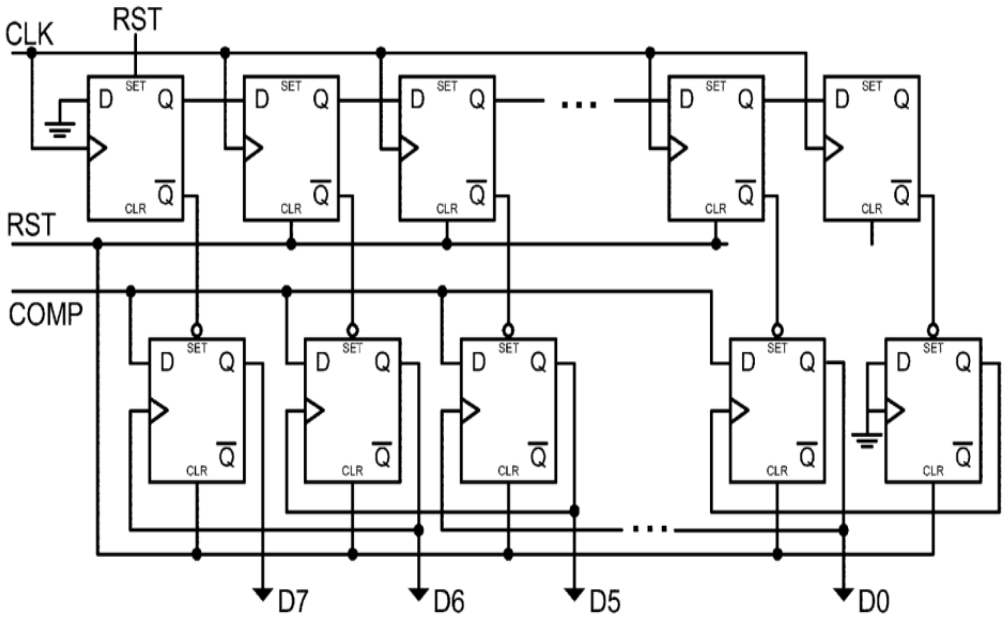


Design - Architecture



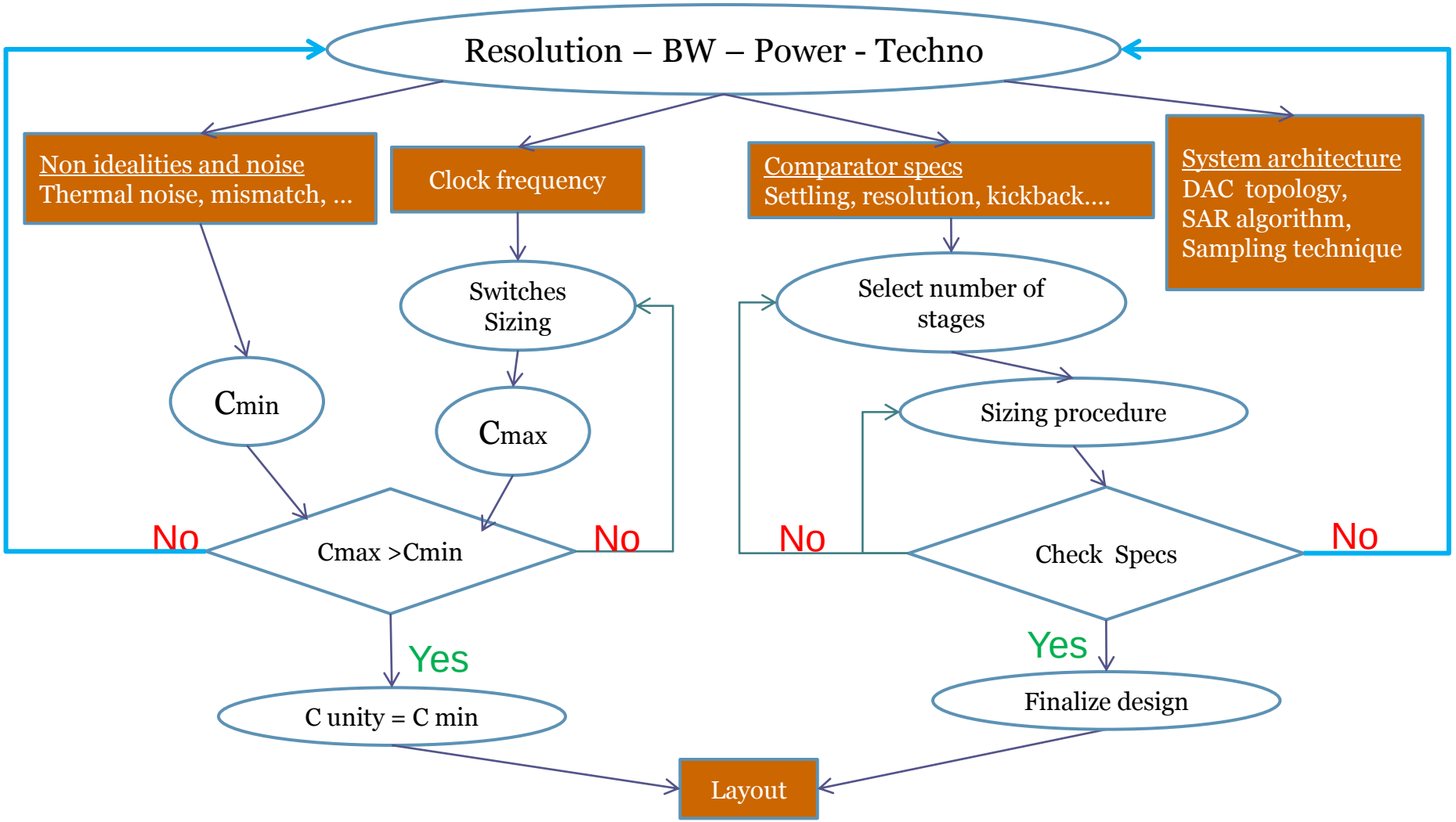
SAR algorithm - Implementation

LFSR: Linear Feedback Shift Register



	DAC outputs								C
0	0	0	0	0	0	0	0	0	X
1	1	0	0	0	0	0	0	0	a8
2	a8	1	0	0	0	0	0	0	a7
3	a8	a7	1	0	0	0	0	0	a6
4	a8	a7	a6	1	0	0	0	0	a5
5	a8	a7	a6	a5	1	0	0	0	a4
6	a8	a7	a6	a5	a4	1	0	0	a3
7	a8	a7	a6	a5	a4	a3	1	0	a2
8	a8	a7	a6	a5	a4	a3	a2	1	a1

Systematic design for SA-ADC



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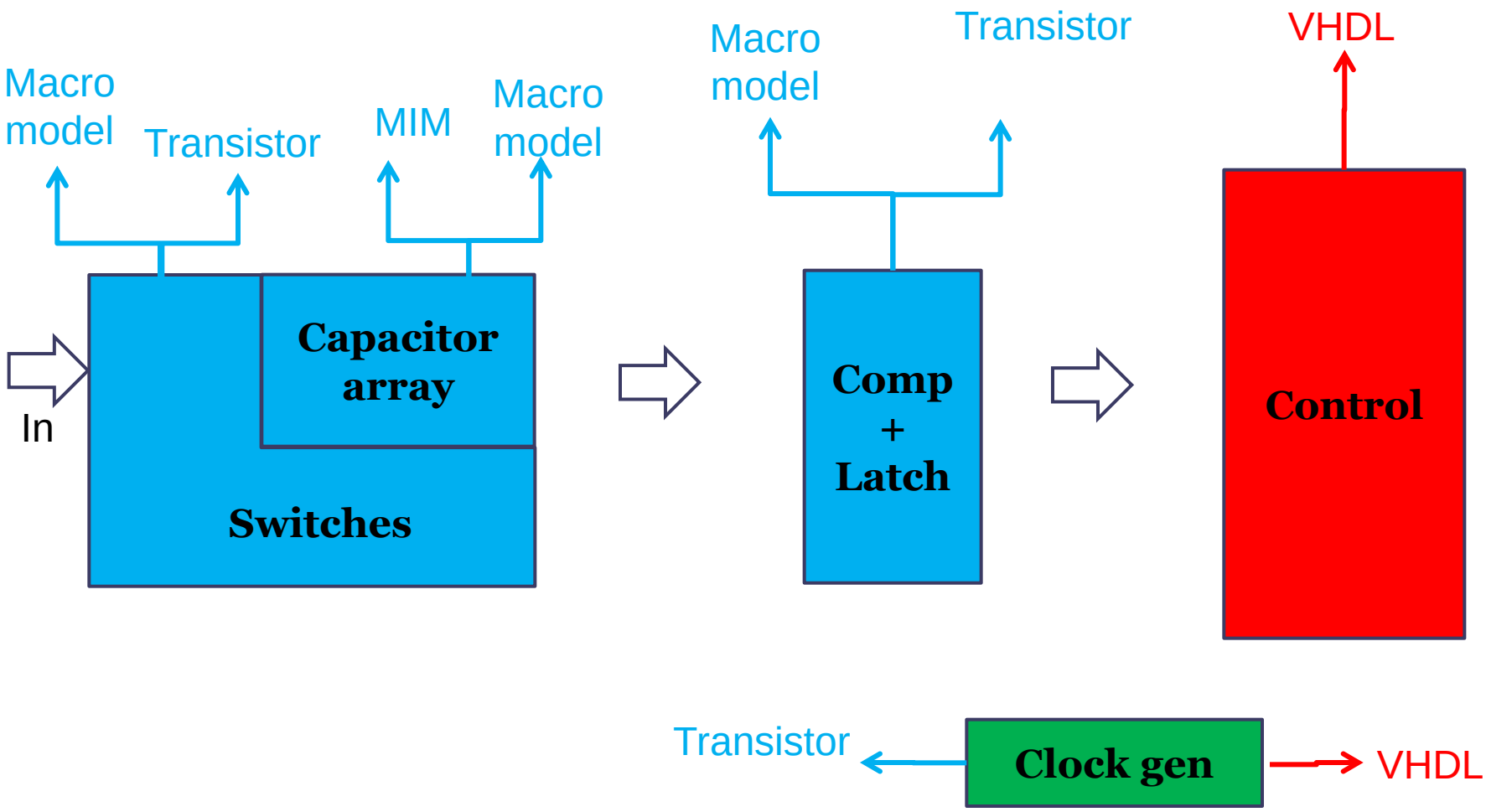
Case Study

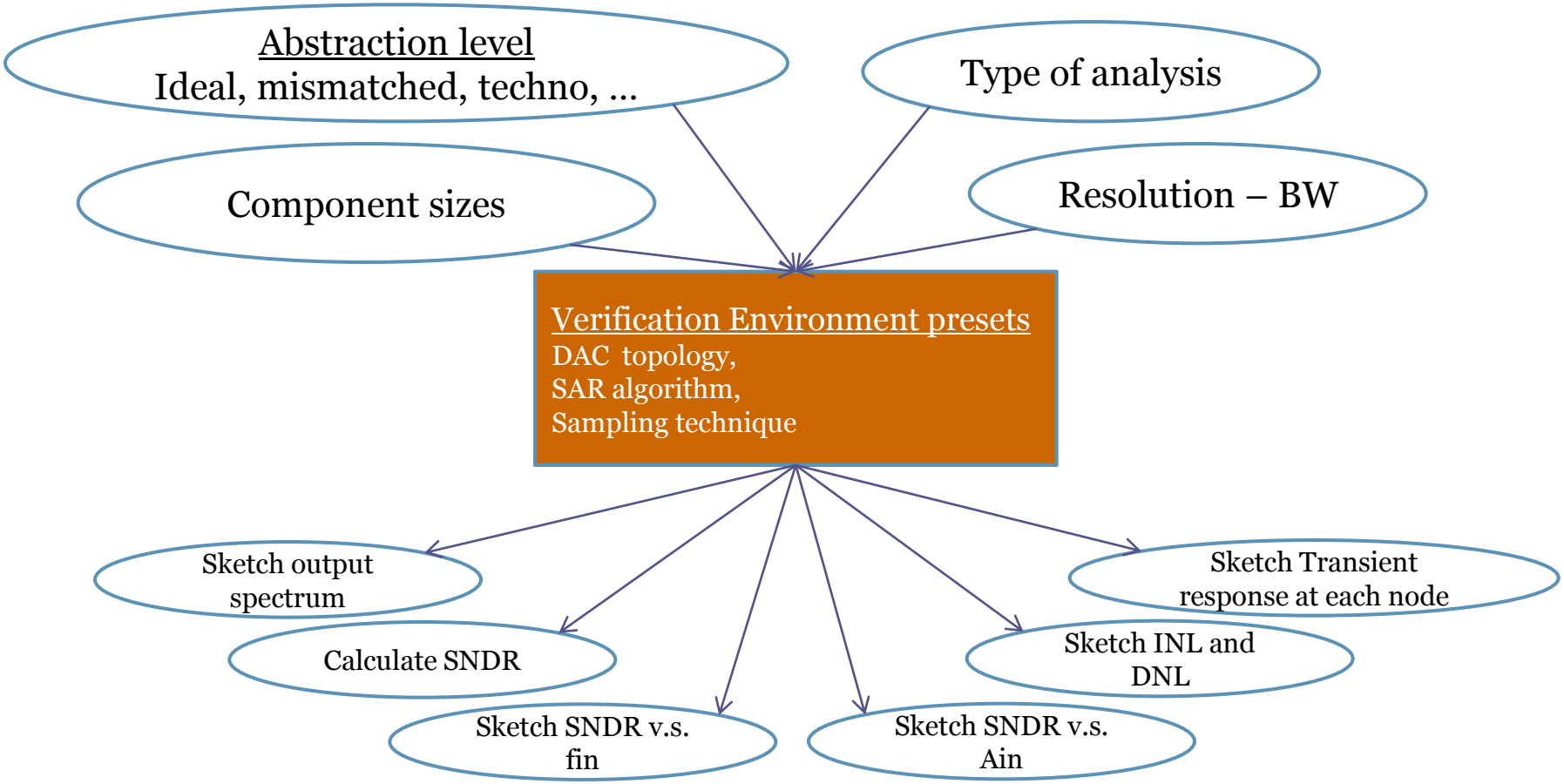
- Case Study
  - Differential Architecture
  - Resolution: 8bit
  - BW: 50 KHz
  - F_{clock}: 1MHz
  - Technology: 0.13u ST, MIM Capacitors

- Verification
  - VHDL AMS used for verification with simulation
  - Different levels of abstraction (Behavioral , gates, transistor, …)
  - Mixed blocs simulation (Analog / Digital)

Multiple abstractions



Verification Environment



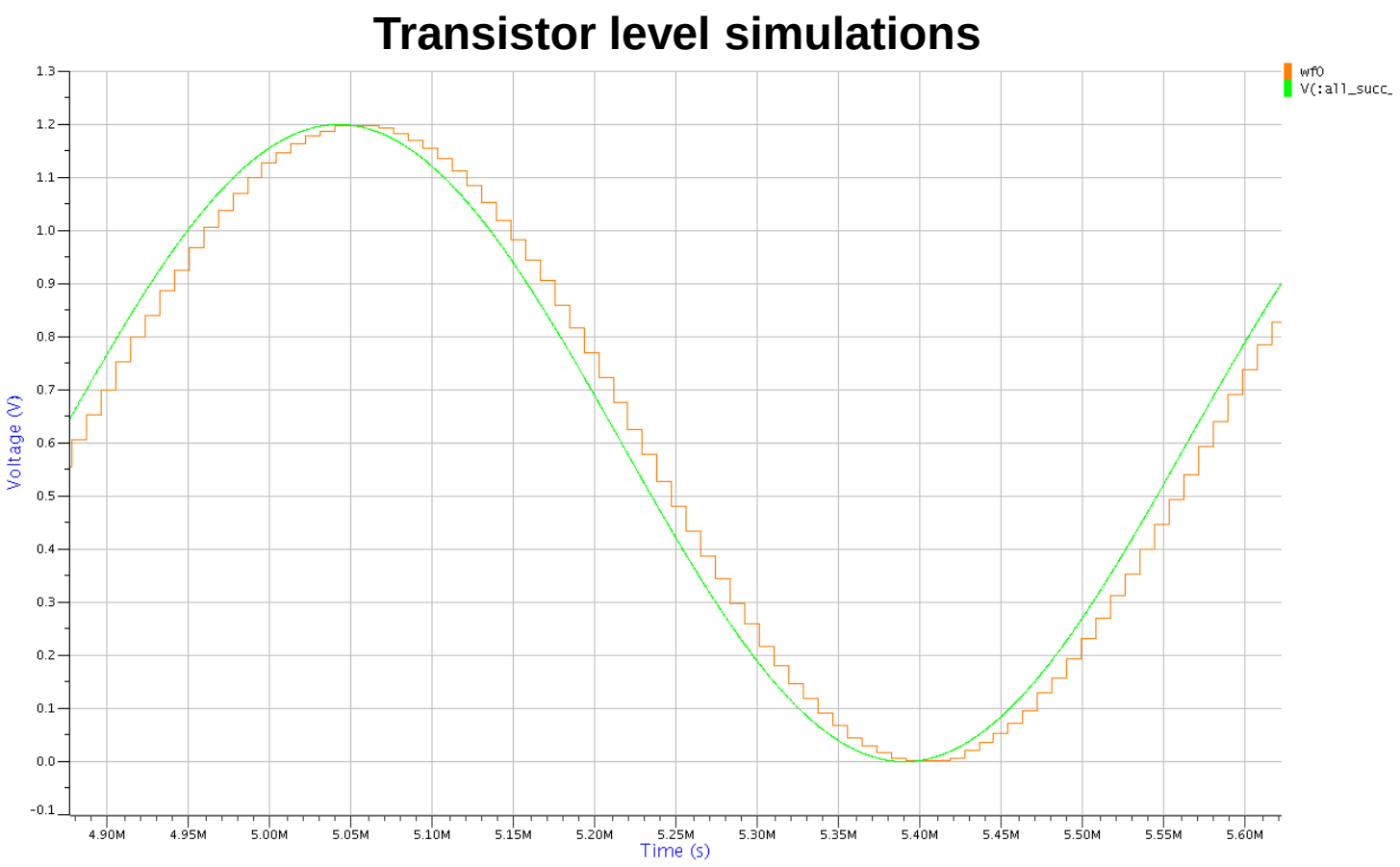
Transiant – Single Ended - Output

Vdd 1.2V

Fin 1.4KHz

Fclk 1MHz

Vin_{p-p} 1.2V



Transiant – Differential - Output

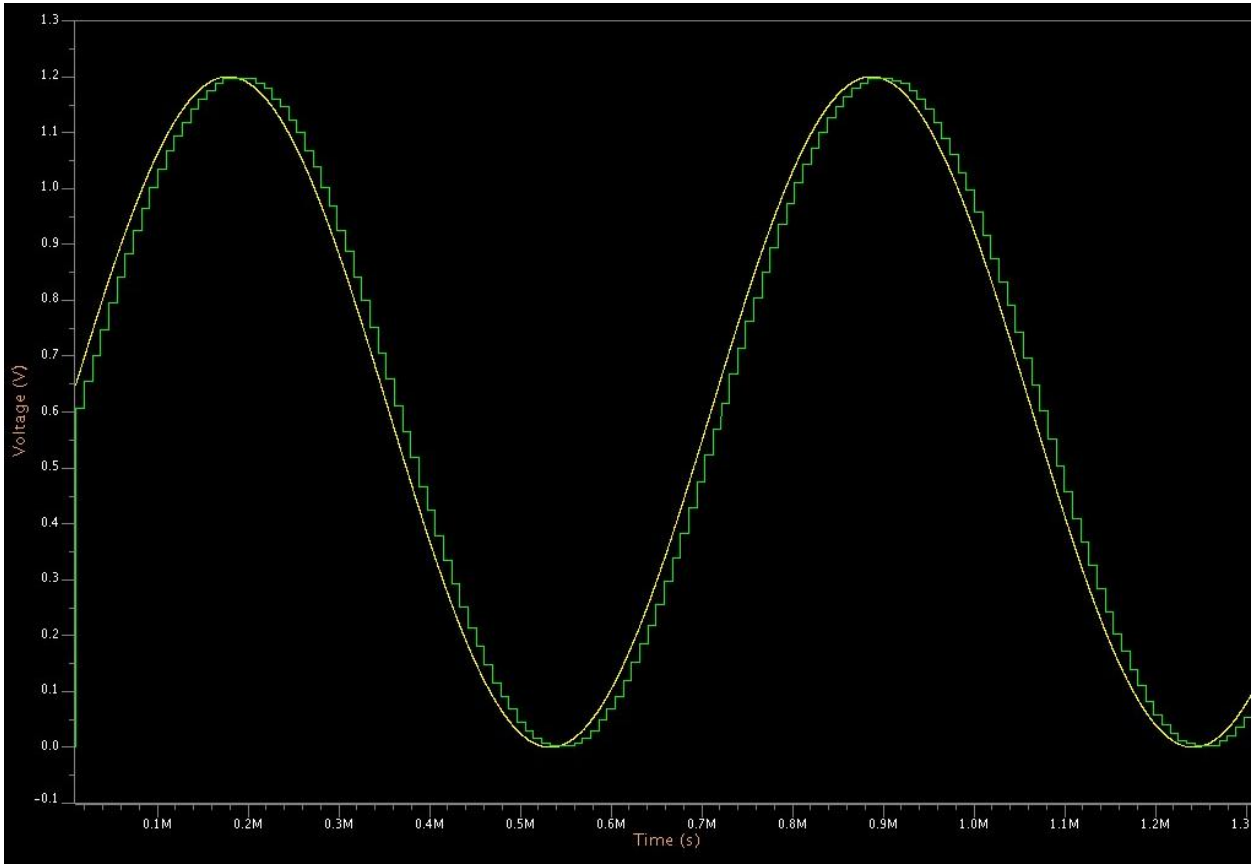
Vdd 1.2V

Fin 1.4KHz

Fclk 1MHz

Vin_{p-p} 1.2V

Transistor level simulations



Transiant – Differential - DACs

Vdd 1.2V

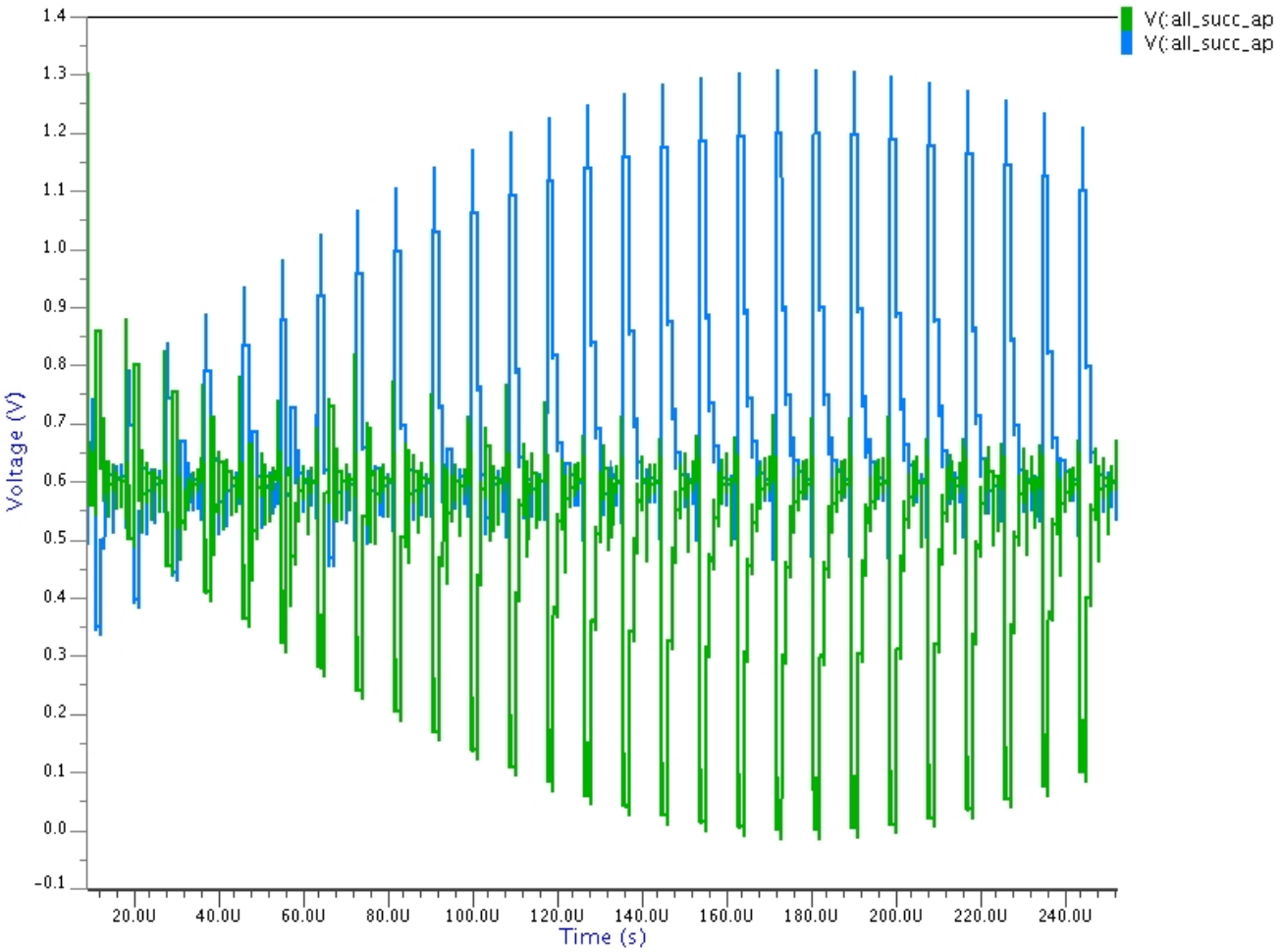
Fin 1.4KHz

Fclk 1MHz

Vin_{p-p} 1.2V

Differential DACs output

Transistor level simulations



Transiant – Differential - Comparator

Full conversion: Differential DACs output – Comparator output

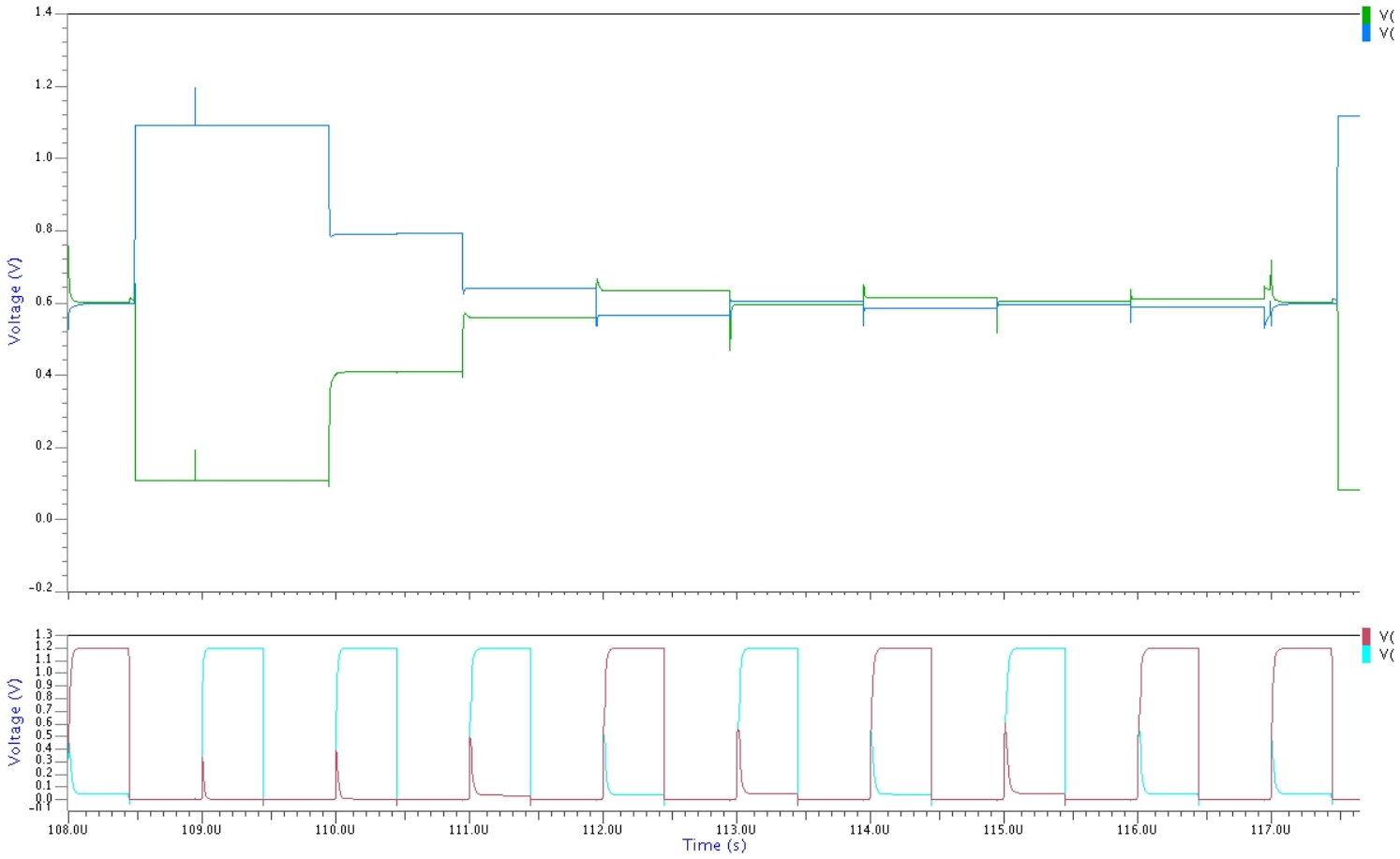
Transistor level simulations

Vdd 1.2V

Fin 1.4KHz

Fclk 1MHz

Vin_{p-p} 1.2V



Transient – SAR control

Control block turning ON and OFF DAC switches [case of 0 input]

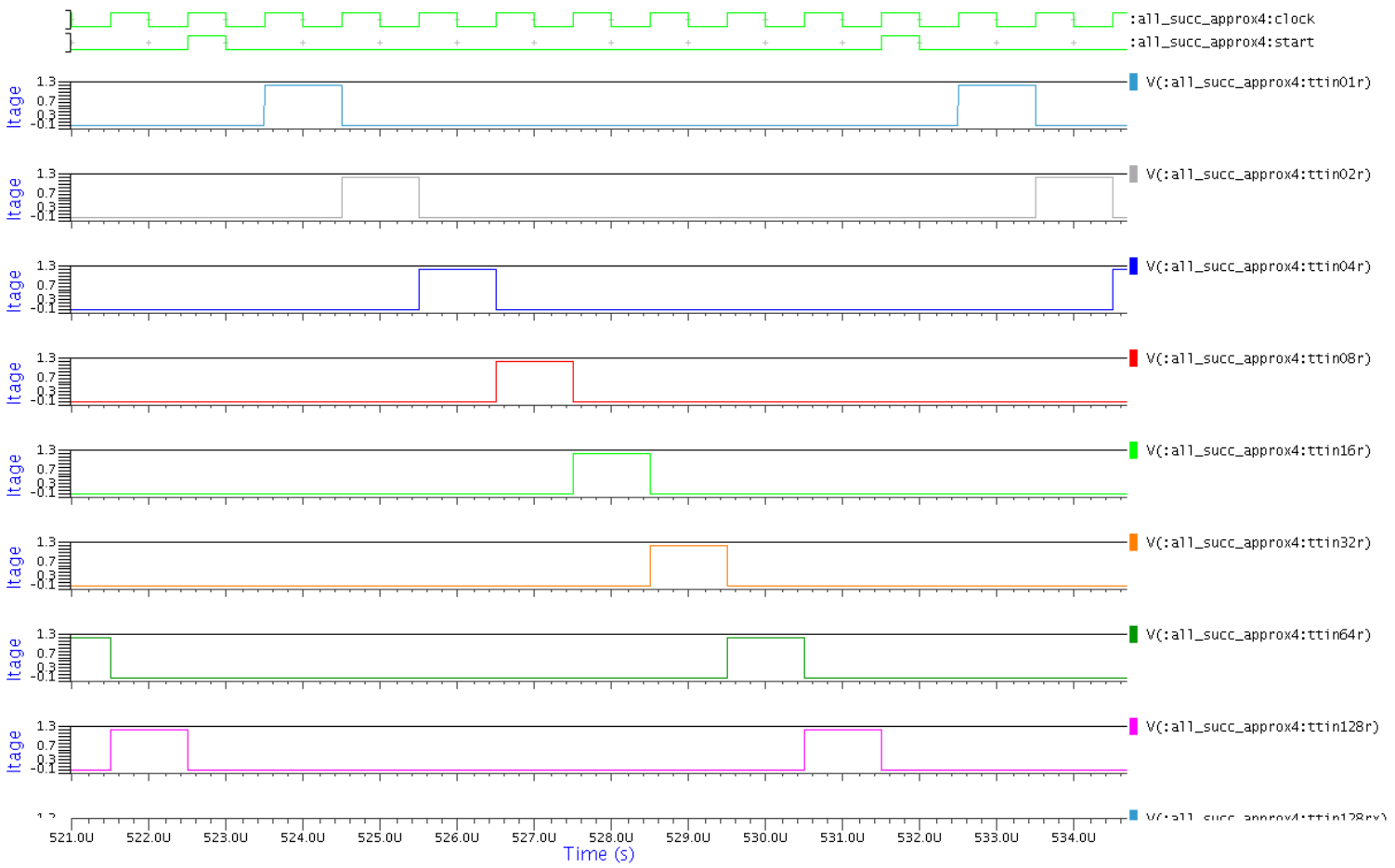
Vdd 1.2V

Fin 1.4KHz

Fclk 1MHz

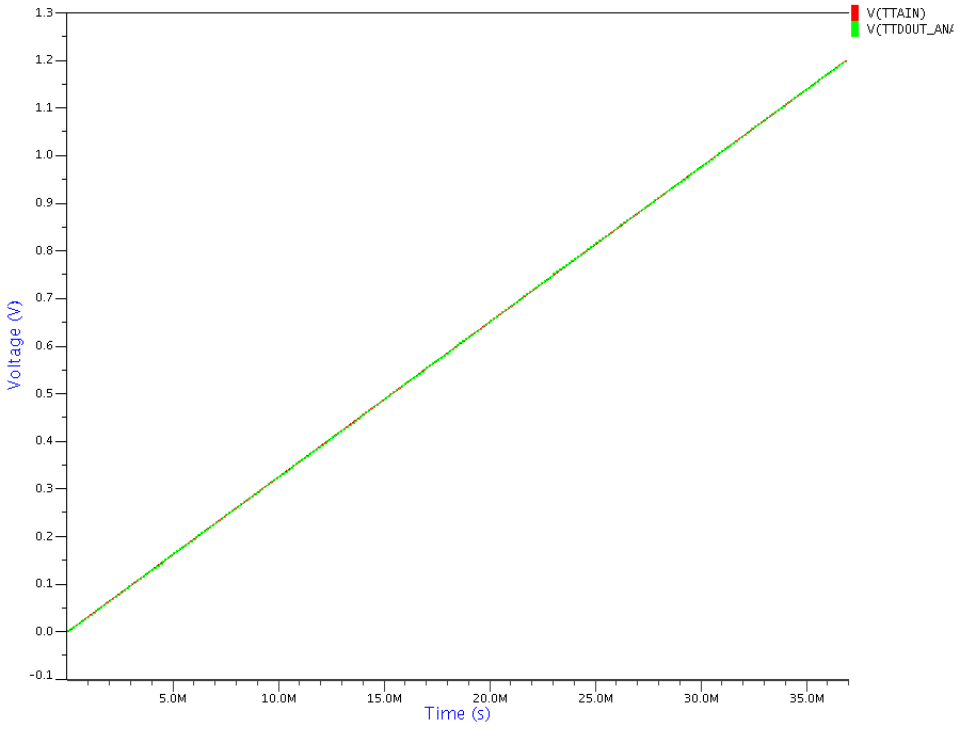
Vin$_{p-p}$ 1.2V

VHDL Description



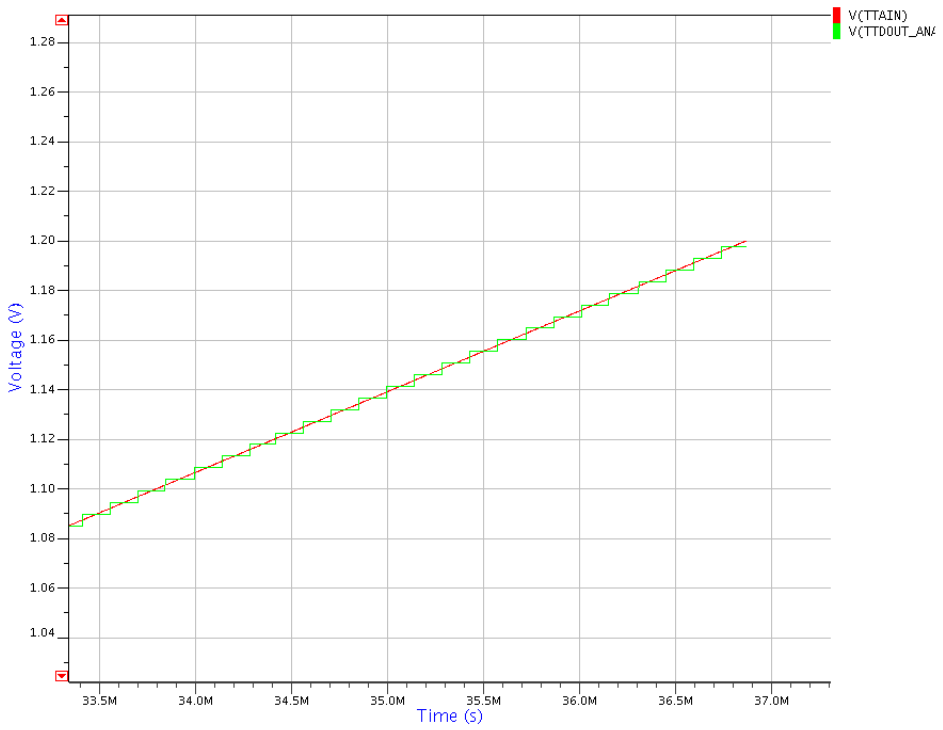
Transient – Full Scale Ramp

Full Scale Slow ramp excitation



(a)

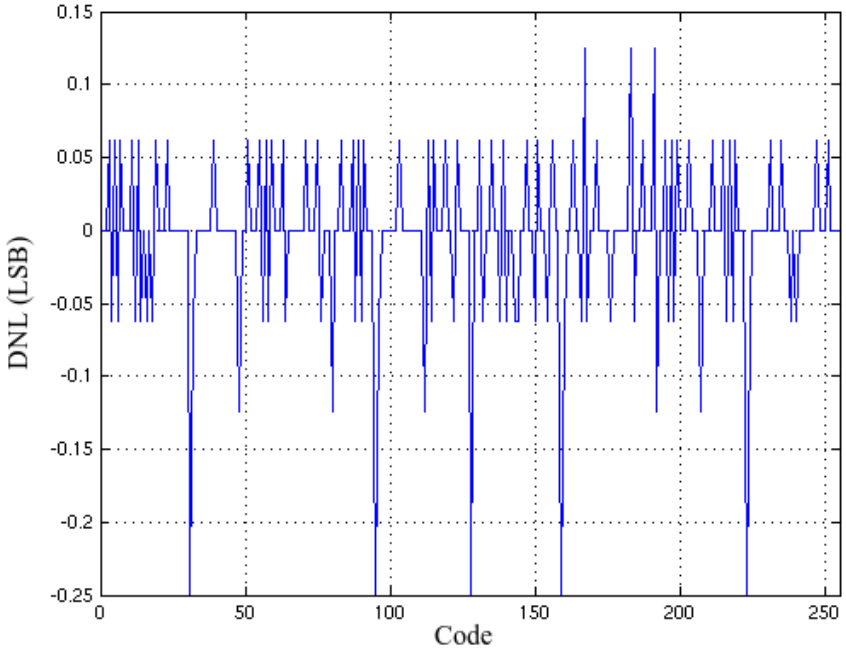
Zoom - in



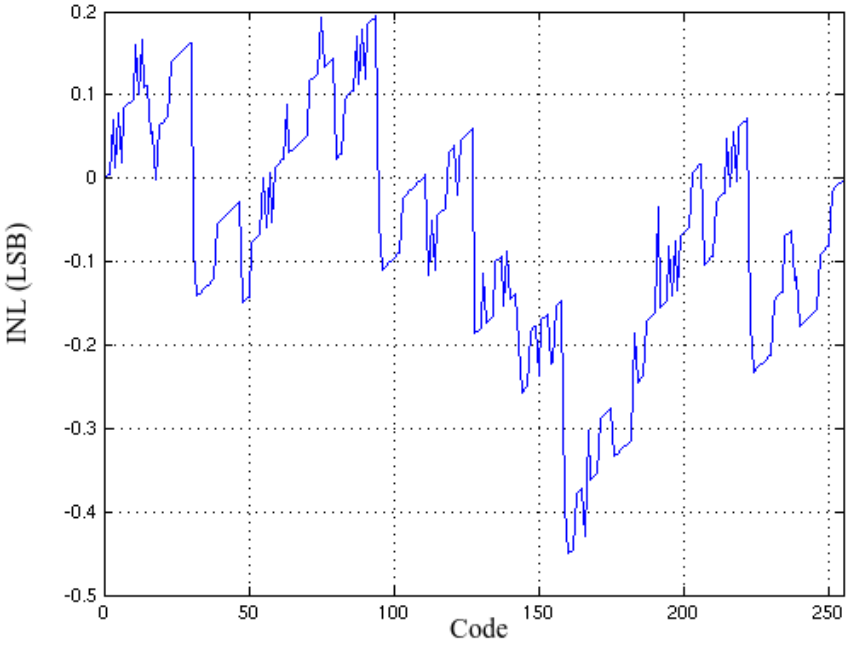
(b)

Static Performance - Transistor Level

Static performance Evaluation in (LSB): DNL and INL [16 sample / bin]



(a)



(b)

Dynamic Performance – Ideal Models

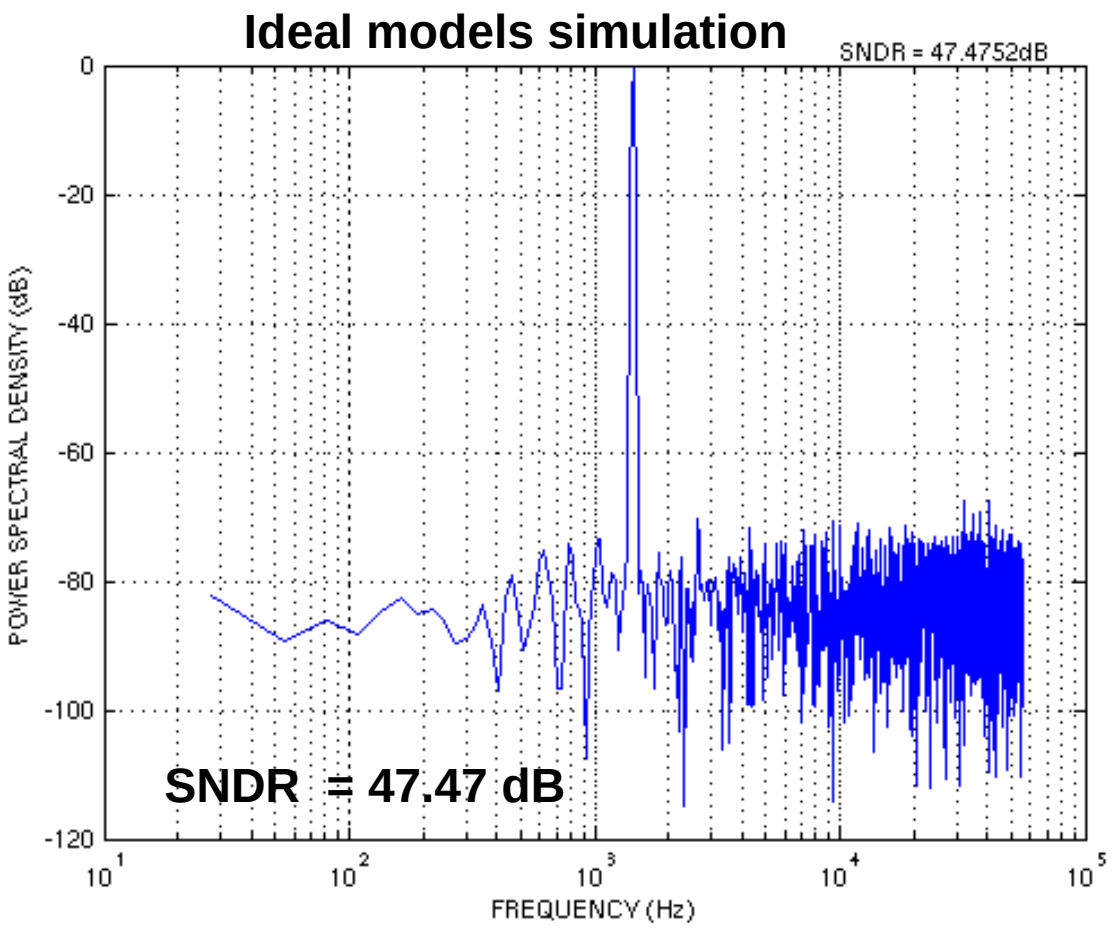
Vdd 1.2V

Fin 1.4KHz

Fclk 1MHz

Vin_{p-p} 1.2V

4096 point FFT



Dynamic Performance – Mixed Models

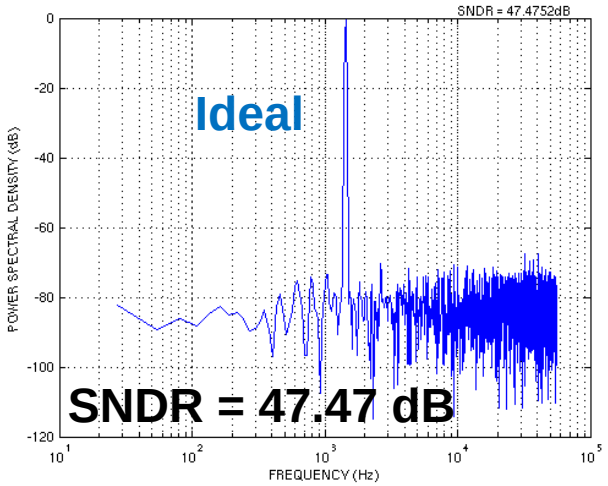
Vdd 1.2V

Fin 1.4KHz

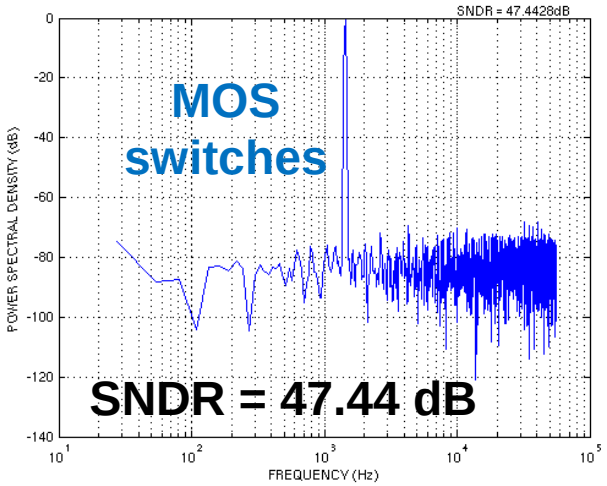
Fclk 1MHz

Vin$_{p-p}$ 1.2V

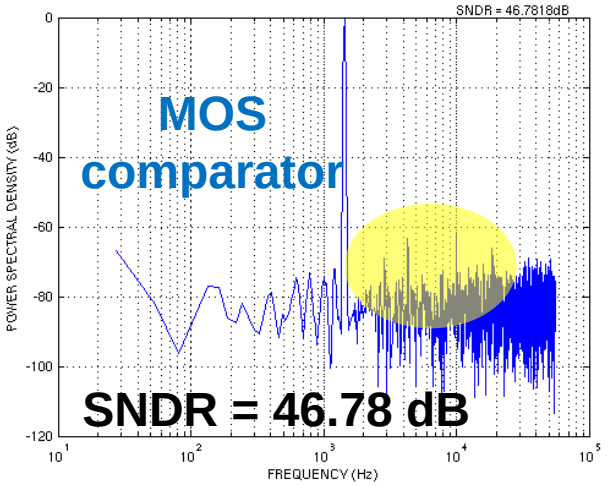
4096 point FFT



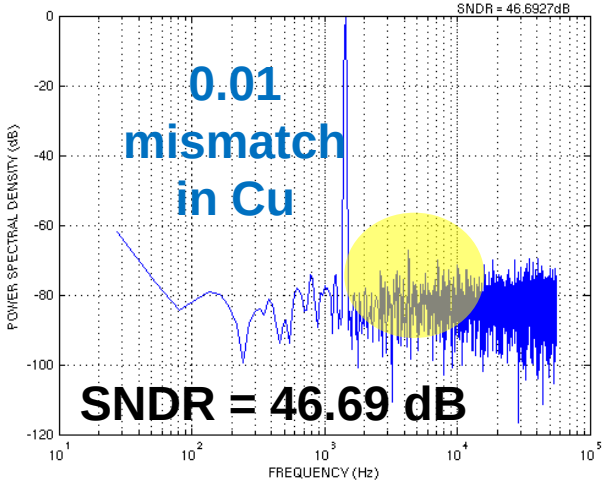
(a)



(b)



(c)



(d)

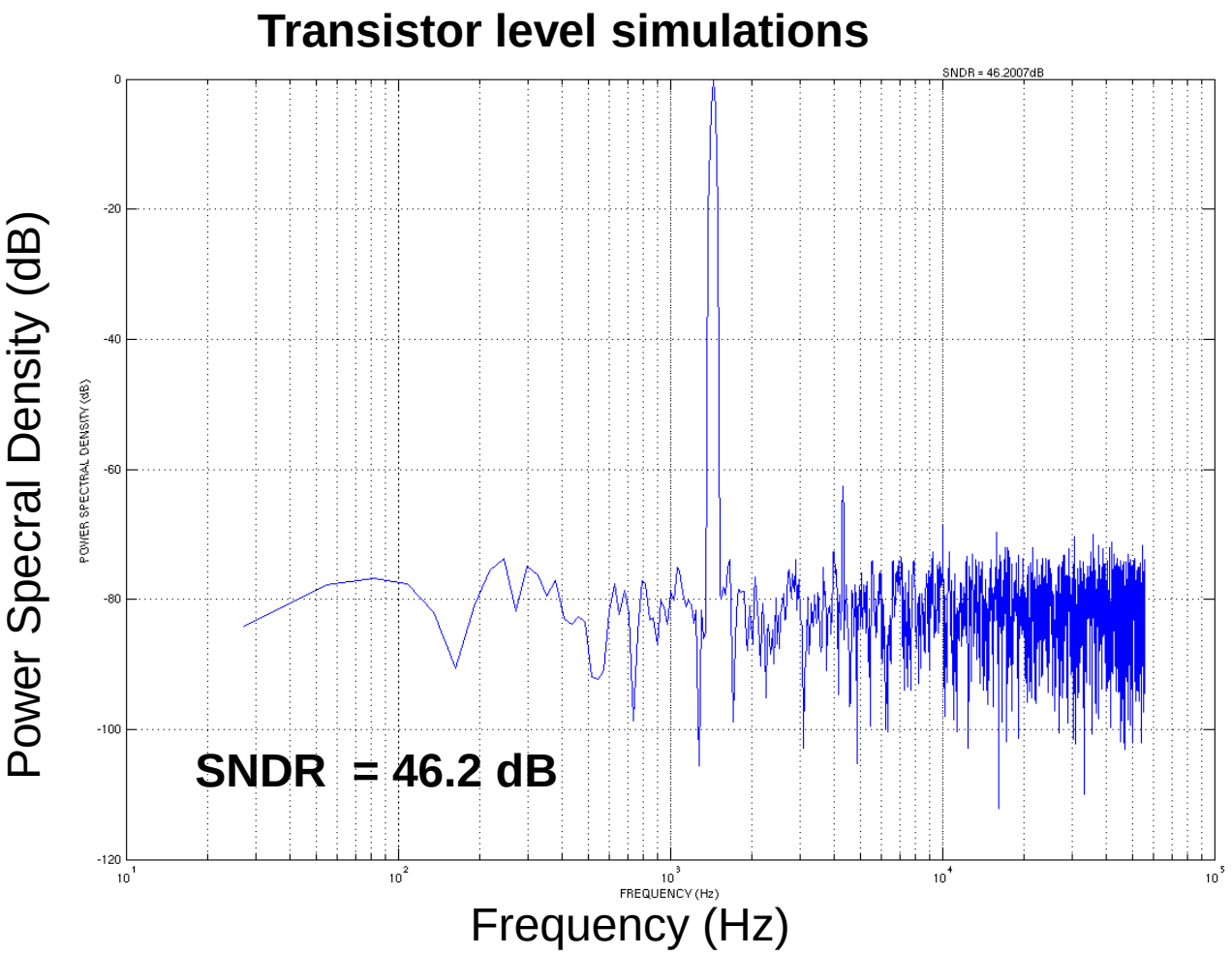
Dynamic Performance – Transistor Level

Vdd 1.2V

Fin 1.4KHz

Fclk 1MHz

1024 point FFT



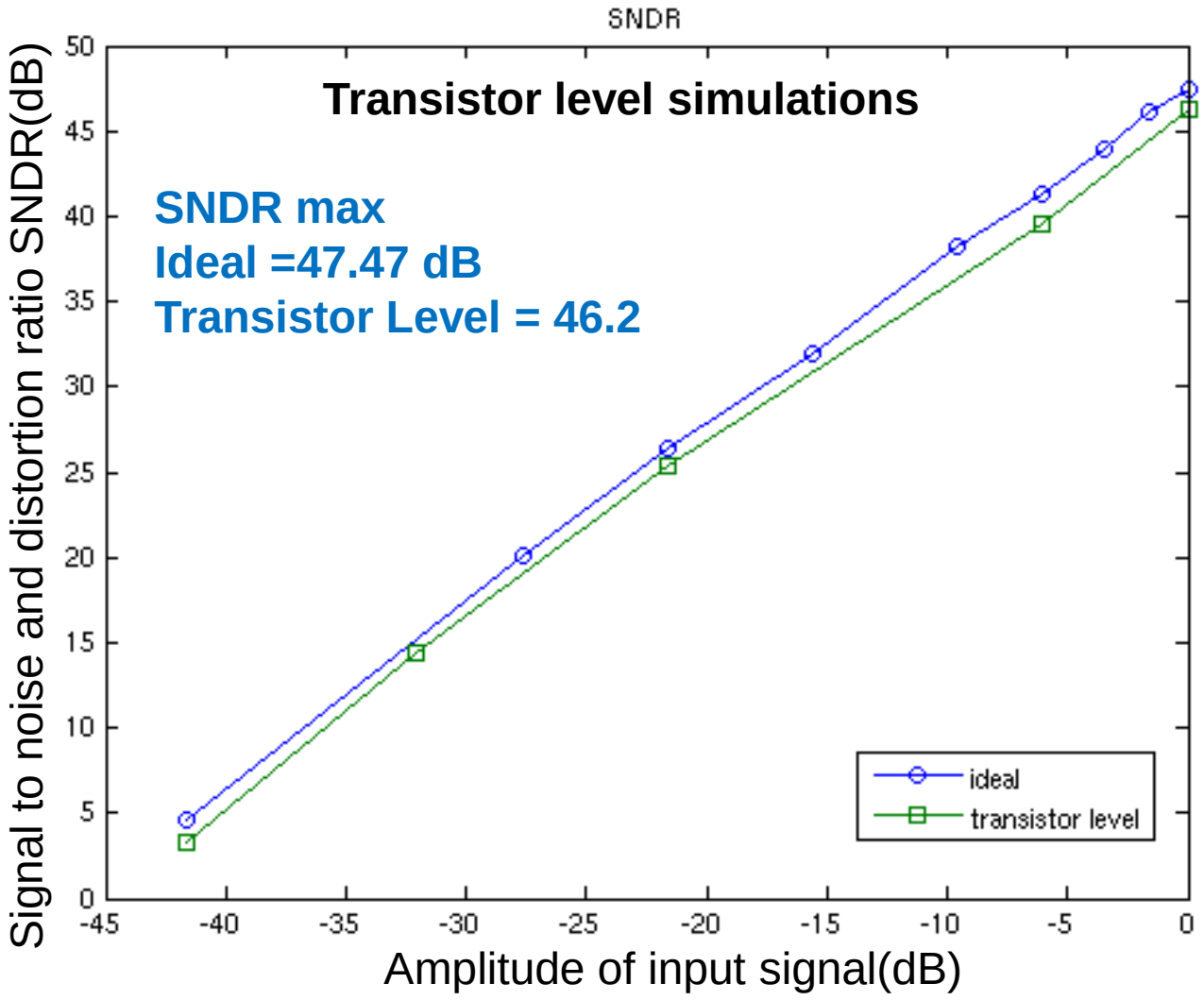
Dynamic Performance

Vdd 1.2V

Fin 1.4KHz

Fclk 1MHz

4096 point FFT



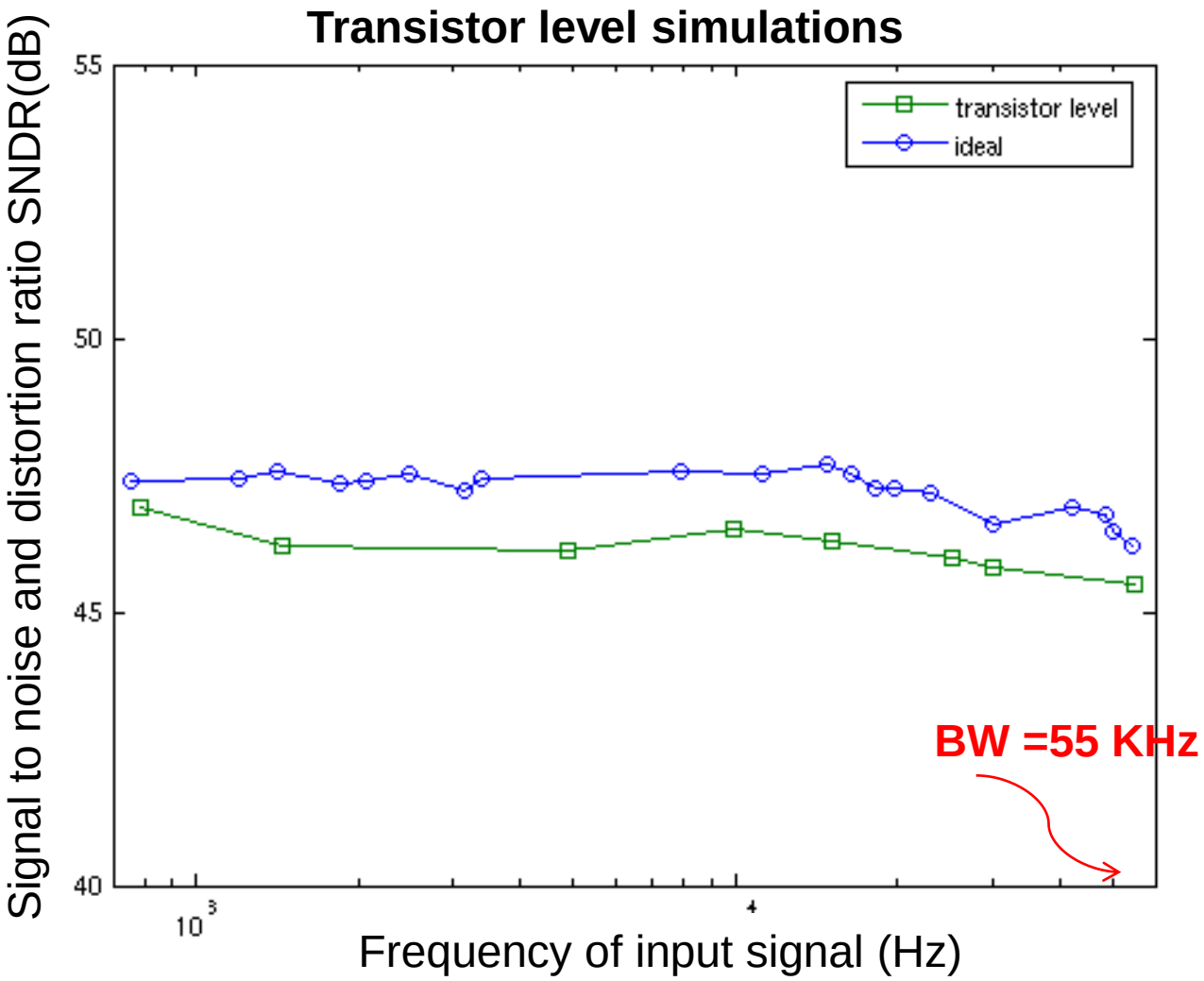
Dynamic Performance

Vdd 1.2V

Fclk 1MHz

Vin_{p-p} 1.2V

4096 point FFT



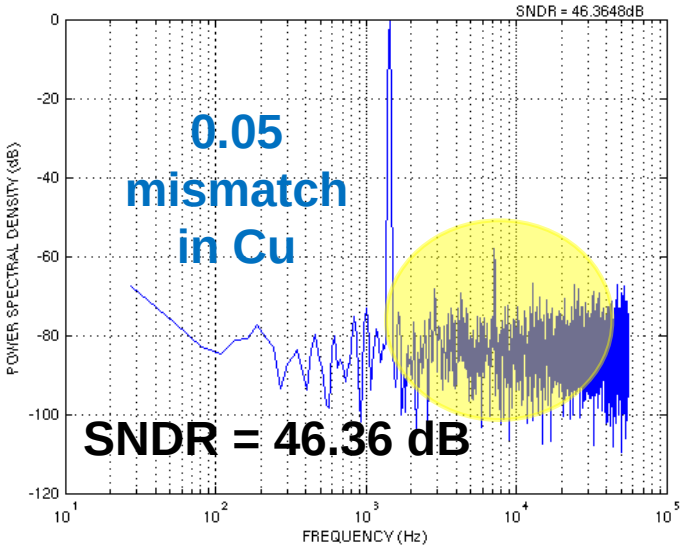
Mismatch analysis

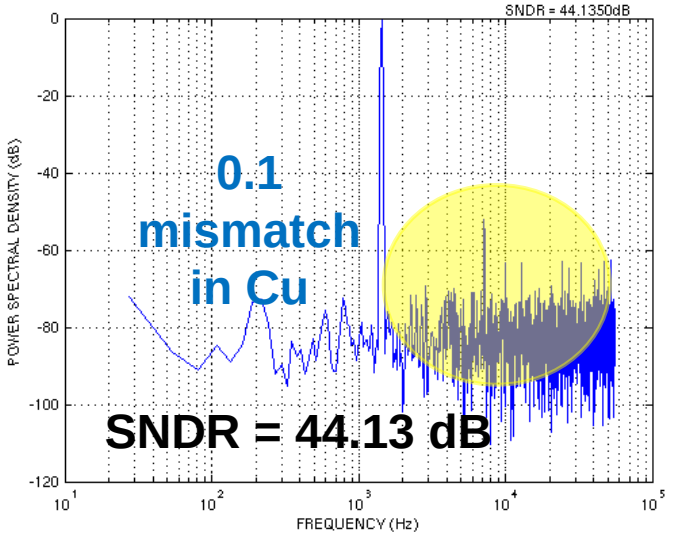
Vdd 1.2V

Fin 1.4KHz

Fclk 1MHz

Vin_{p-p} 1.2V

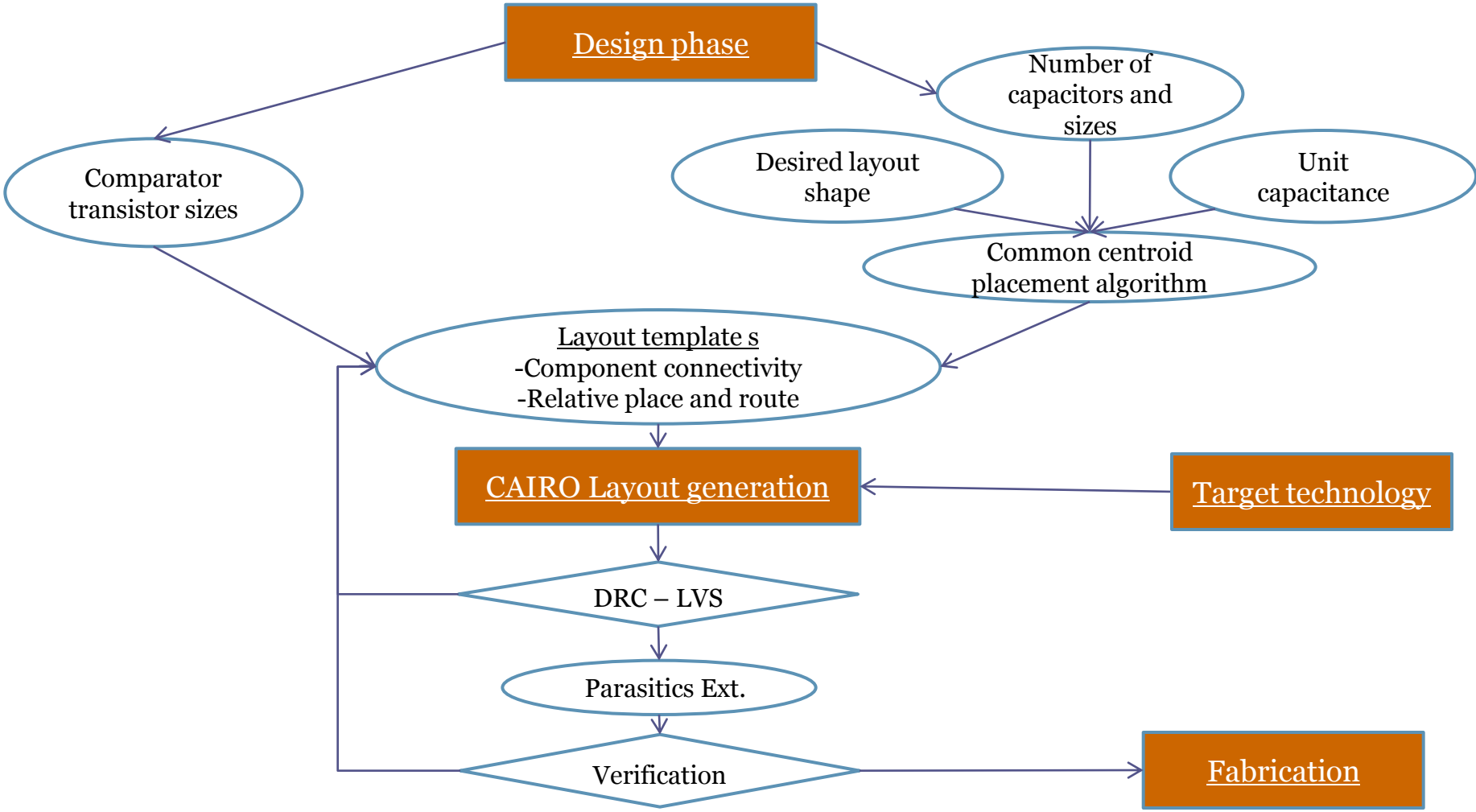




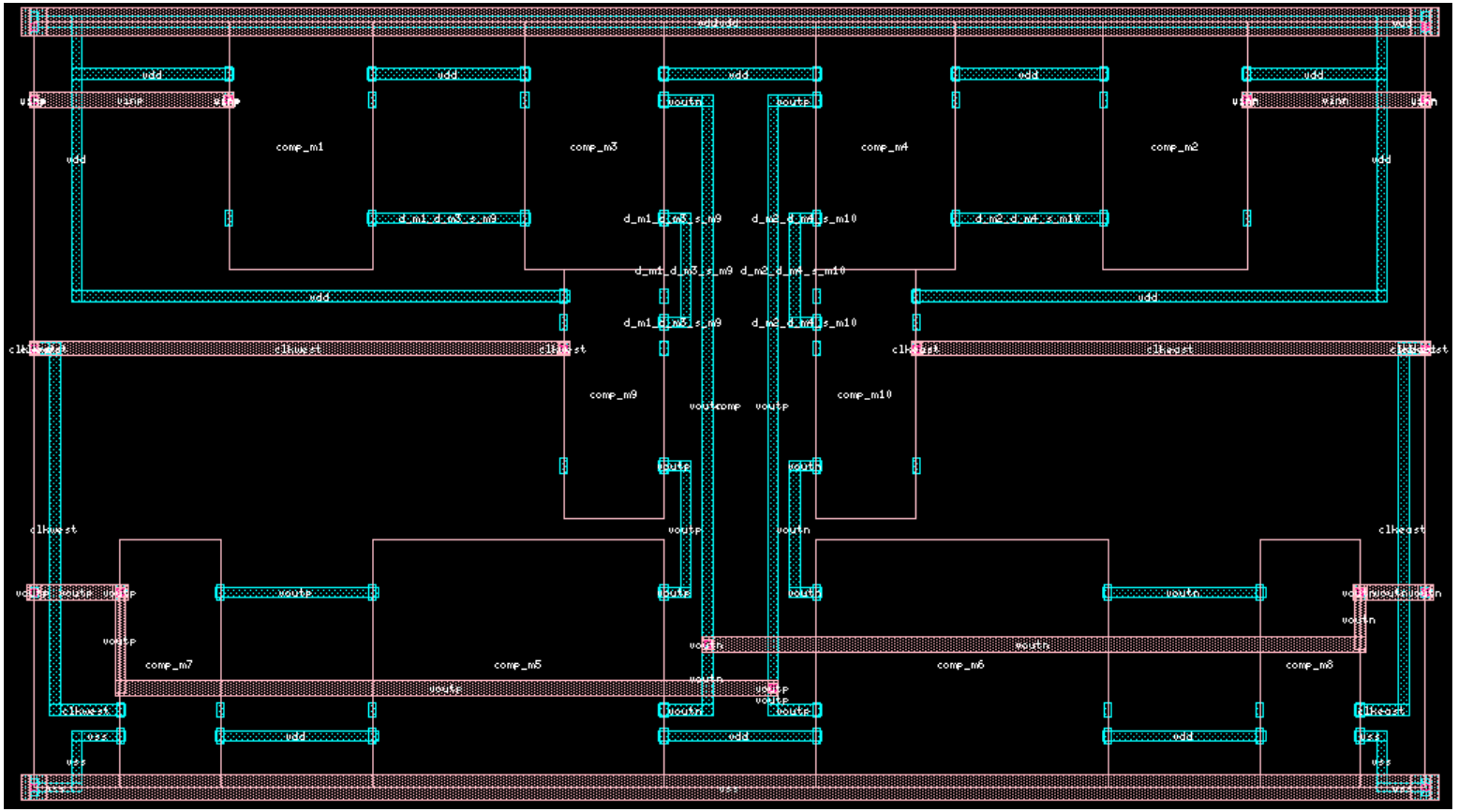
4096 point FFT

C_u	Variance σ					Ideal
	0.01	0.02	0.05	0.1	0.2	
10fF	47.36	46.40	43.22	39.10	35.6	47.44
20fF	47.2	47.09	44.99	42.08	35.77	47.44
30fF	43.89	44.6	40.19	39.02	32.7	47.44

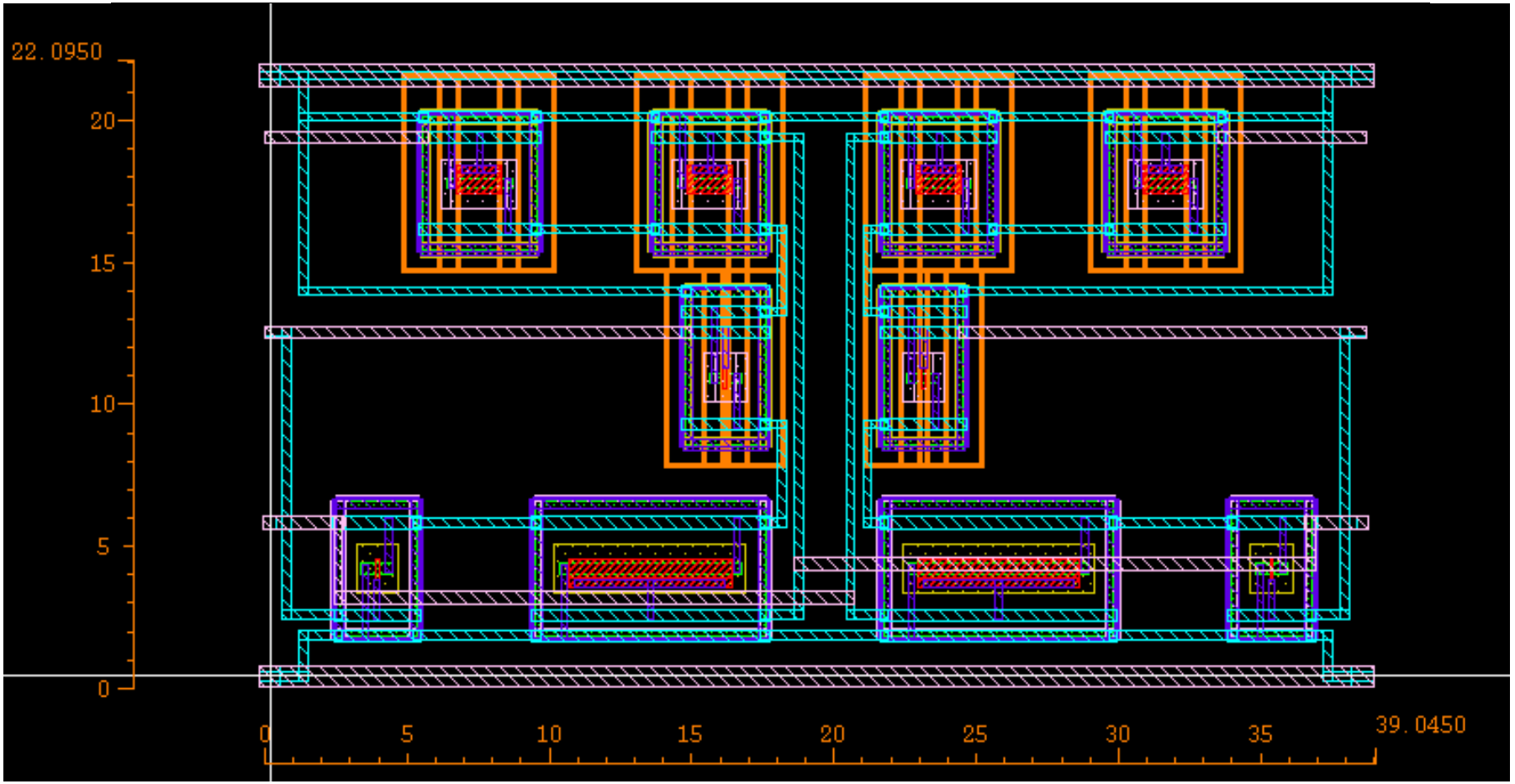
Layout generation for SA-ADC



Layout – Comparator - Floorplan



Layout – Comparator - Generated



Area 22 x 39 μm²

Dummies Removed for Layout verification

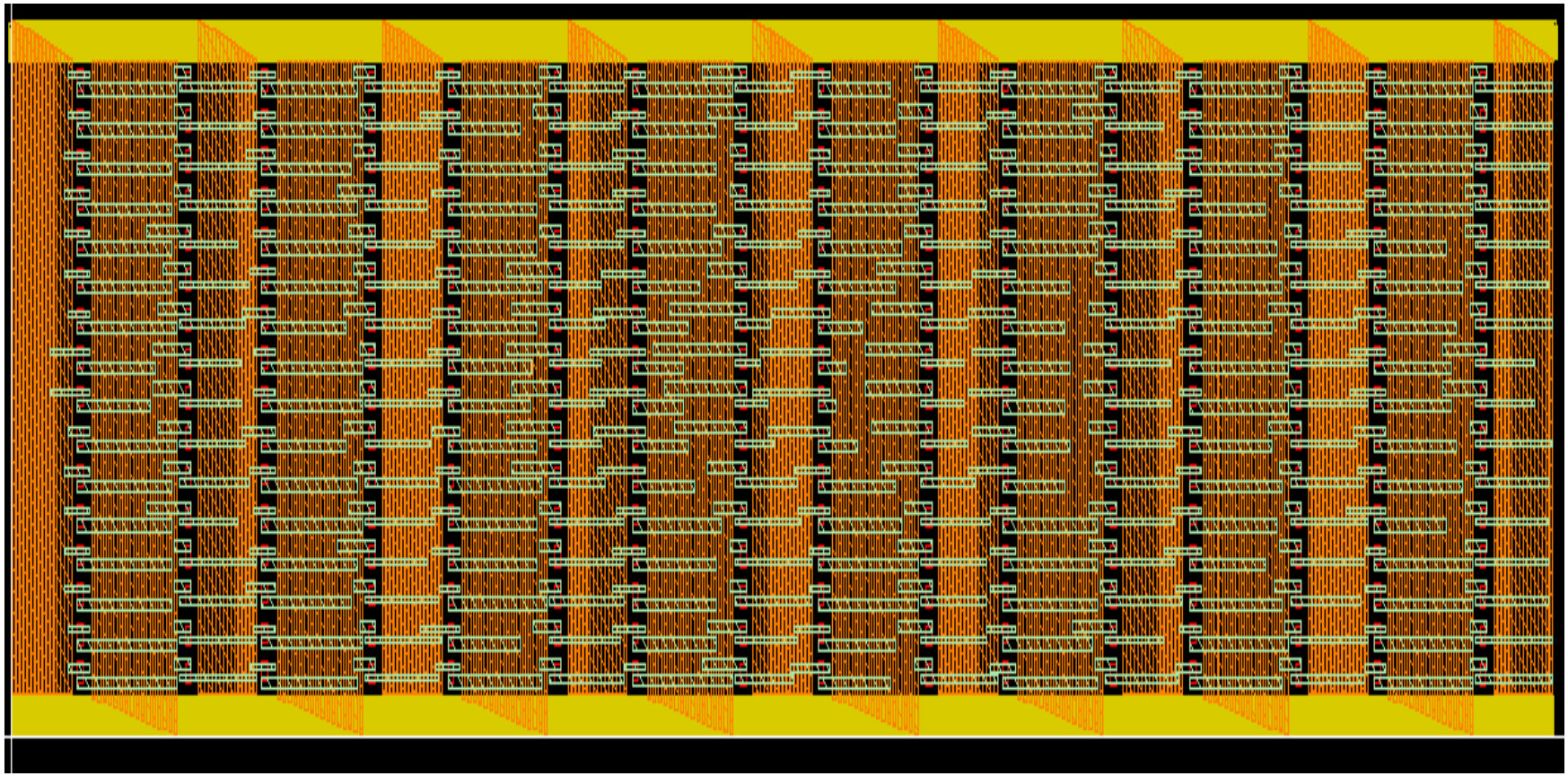
Layout – Differential DACs - Floorplan

Common centroid placement for 16 capacitor

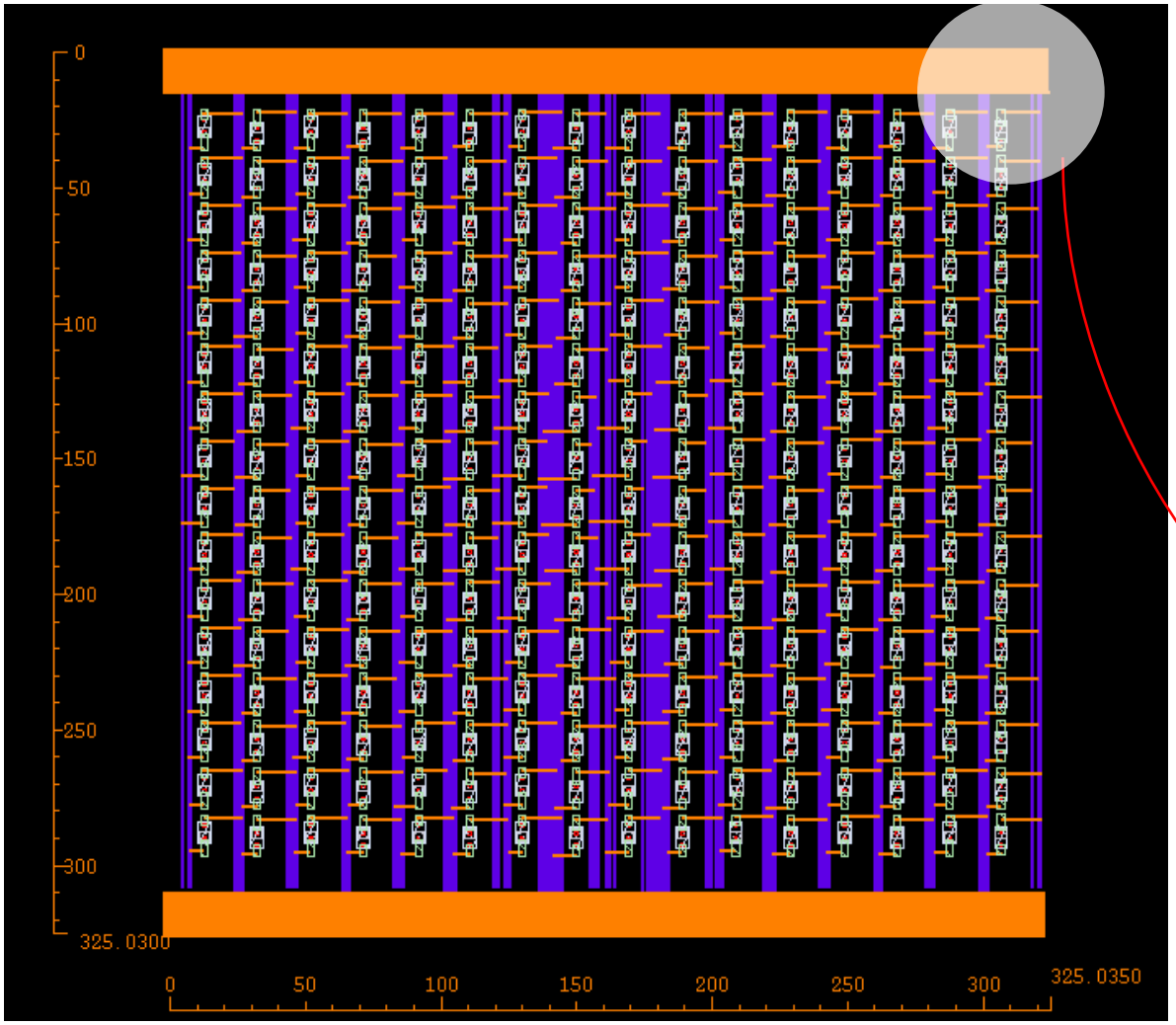
```
how many capacitors? 16
routing? 1
enter values
1 1 1 1 2 2 4 4 8 8 16 16 32 32 64 64
use rectangles?(1=yes)1
enter unit capacitor side length:
1
enter length:
16
sum:256
16  16  15  15  15  15  16  11  11  16  15  15  15  15  16  16
16  16  16  16  11  14  13  12  12  13  14  11  16  16  16  16
15  16  14  15  16  15  13  16  16  13  15  16  15  14  16  15
15  16  15  12  14  15  13  16  16  13  15  14  12  15  16  15
15  11  16  14  14  15  14  13  13  14  15  14  14  16  11  15
15  14  15  15  15  9   10  12  12  9   10  15  15  15  14  15
16  13  13  13  14  10  8   5   6   8   9   14  13  13  13  16
11  12  16  16  13  9   7   2   3   7   10  13  16  16  12  11
11  12  16  16  13  10  7   4   1   7   9   13  16  16  12  11
16  13  13  13  14  9   8   6   5   8   10  14  13  13  13  16
15  14  15  15  15  10  9   12  12  10  9   15  15  15  14  15
15  11  16  14  14  15  14  13  13  14  15  14  14  16  11  15
15  16  15  12  14  15  13  16  16  13  15  14  12  15  16  15
15  16  14  15  16  15  13  16  16  13  15  16  15  14  16  15
16  16  16  16  11  14  13  12  12  13  14  11  16  16  16  16
16  16  15  15  15  15  16  11  11  16  15  15  15  15  16  16
```

Layout – Differential DACs - Generated

Layout 1 - 256 C_u – Placed and Routed – Area 1.26 x 0.26 mm^2 and Huge routing parasitics

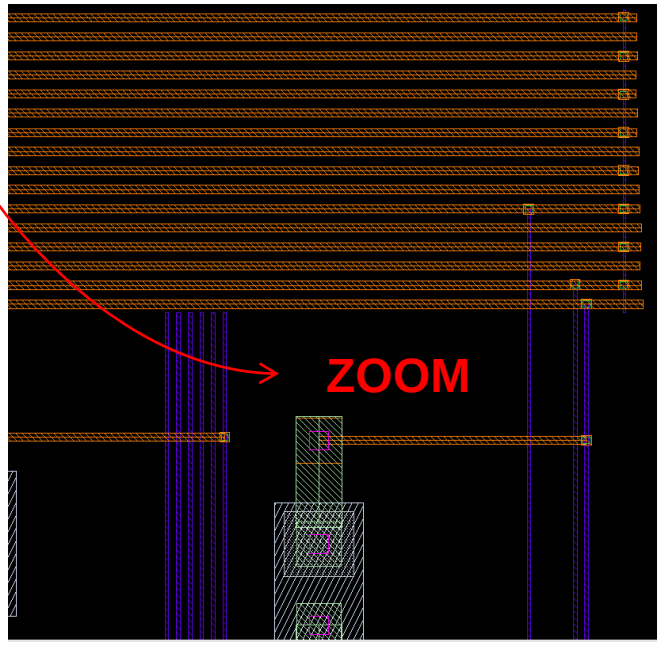


Layout – Differential DACs - Manual



Layout 2 - 256 C_u – Placed and Routed – 2/3 less routing parasitics

Area 0.1056 mm^2



Performance

	[Hongo7]	This work*	[scott03]
Technology	0.18 µm	0.13 µm	0.25 µm
Supply	0.83 V	1.2 V	1.0 V
Input range	Rail to Rail	Rail to Rail	Rail to Rail
Sampling rate	111 KHz	111 KHz	100 KHz
Unit Cap.	24 fF	30fF	12f
Power (Analog)	1.16 µW	0.72µW	2.2 µW
Area	0.062 mm2	0.122 mm2	0.053 mm2
SNDR@BW	47.40 dB	46.2dB	43.8 dB
Architecture	Single Ended	Differential	Single Ended
FOM	65 fJ/bit	64fJ/bit	2163 fJ/bit

Outline

- Background
- Principles of Operation
- System and Circuit Design
- Case Study
  - Simulations
  - Layout Generation
  - Performance Evaluation
- Conclusion
- Perspectives

Summary and Conclusion

- Systematic design methodology for SA-ADC from system to layout.
- General simulation environment
  - Different abstraction levels.
  - Different verification tests.
- Emphasis on analog design automation and reuse
- Optimizing Layout for best component matching
- Verification with case study for WSN specs

Perspectives

- Targeting high frequency specs (>500 Msample/S)
  - Redundant system error correction code [Kuttner02]
  - Digital calibration [Promitzer01]
  - Asynchronous operation [Chen06]
  - Time interleaving [Chen06]
- Full Automation
  - Sizing procedure with layout parasitics awareness
  - Layout generation for the full ADC

Thank You