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A 12-bit, 10 Msps Two Stage SAR-Based Pipeline ADC

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A 12-bit, 10 Msps Two Stage SAR-Based Pipeline ADC

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REPORT

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Dedicated to God and to my family.

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A 12-bit, 10 Msps Two Stage SAR-Based Pipeline ADC

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The market for battery powered communications devices has grown significantly in recent years. These devices require a large number of analog to digital converters (ADCs) to transform wireless and other physical data into the digital signals required for digital signal processing elements and microprocessors. For these applications, power efficiency and accuracy are of the utmost importance. Successive approximation register (SAR) ADCs are frequently used in power constrained applications, but their main limitation is their low sampling rate. In this work, a two stage pipelined ADC is presented that attempts to mitigate some of the sampling rate limitations of a SAR while maintaining its power and resolution advantages. Special techniques are used to reduce the overall sampling capacitance required in both SAR stages and to increase the linearity of the multiplying digital to analog converter (MDAC) output. The SAR sampling network, control logic, and MDAC blocks are completely implemented. Ideal components were used for the clocking, comparators, and switches. At the end of this design, a figure of merit of 51 fJ/conversion-step was achieved.

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Chapter 1

Introduction

Pipeline analog-to-digital converters (ADCs) have become a very popular architecture for high-speed high-resolution circuits required in many applications, including communications circuits. The explosion in recent years of portable, battery-powered, electronics has also driven interest in pipeline ADCs, since pipeline ADCs can provide significant area and power benefits. Generally, pipeline ADCs have employed flash sub-ADCs, since the flash topology is the architecture capable of achieving the highest performance and pipelining this topology results in significant area savings. The downside to this architecture is the latency introduced by each stage in the pipeline, which is not tolerable in some applications. For most communications circuits, however, a small latency is generally tolerable, especially considering that most back-end digital signal processing introduces additional pipelined latencies. In an effort to increase the power efficiency of the pipeline architecture even further, this work used a successive approximation register (SAR) topology instead of the traditional flash topology for the pipeline sub-ADC. SAR ADCs are ideal for battery-powered applications due to their high energy efficiency, but the low sample rates allowed by this topology limits their usage [12]. By pipelining the SAR topology, sampling rates can be increased while maintain-

ing the energy advantages of the SAR topology.

The goal of this work was to produce a 12 bit ADC with a medium sampling rate, f_{samp}, of 10 Msps while reducing the power to the minimum required. The ADC architecture was initially validated using ideal components. Afterwards a transistor-level design of the operational transconductance amplifier (OTA) in order to provide more realistic performance and power consumption data. The OTA design was integrated into the main ADC architecture and final performance metrics were obtained.

This chapter provides an introduction to the concepts discussed in the rest of the report. The first sections of this chapter will provide an overview of ADC terminologies, as well as a discussion of general pipeline ADC and SAR ADC operation. The following sections will be a more in-depth discussion of the benefits of pipelining a SAR topology, as well as a discussion of the advantages of using a SAR topology as the pipeline sub-ADC versus a flash topology. Next will be a discussion of the primary transistor level design methodology for this report. This chapter will conclude with an overview of the organization of the rest of the report.

1.1 ADC Terminology

This section defines terms and performance metrics that will be used throughout the rest of this report. An analog-to-digital converter takes an analog sample as an input, and converts this input to a digital code. Most ADC's use an internal reference voltage for conversions. In the case of the ADC

designed in this Master's Report, the expression for the voltage reference, V_{ref}, is:

$$V_{ref} = \frac{V_{FS}}{2} \tag{1.1}$$

where V_{FS} is the full-scale input voltage range of the ADC. For a standard ADC with a resolution of N bits, the corresponding analog voltage difference between adjacent digital codes is known as the least significant bit (LSB) size. The expression for LSB size, Δ, as a function of V_{FS}, is:

$$\Delta = \frac{V_{FS}}{2^N} \tag{1.2}$$

The transition level is defined as the analog input level at the transition between two digital codes [19]. Assuming that the transition level lies halfway between each digital code, the magnitude of the maximum error of an ideal ADC is:

$$|\epsilon_q| = \frac{\Delta}{2} \tag{1.3}$$

Assuming a full-scale sinusoidal input and a uniform distribution of ϵ_q, the signal-to-quantization-noise ratio of an N bit ADC is [19]:

$$\begin{aligned} SQNR &= \frac{P_{sig}}{P_{qnoise}} \\ &= \frac{\frac{1}{2}\left(\frac{V_{FS}}{2}\right)^2}{\frac{\Delta^2}{12}} = 6.02N + 1.76\text{dB} \end{aligned} \tag{1.4}$$

where P_{sig} is the total signal power and P_{qnoise} is the total quantization noise power. SQNR defines the signal-to-noise ratio (SNR) of an N bit ADC with

zero electronic noise and a perfectly linear transfer function. Since all real electronic circuits generate some electronic noise and have non-linear transfer functions, a better measure of ADC performance is known as the signal-to-noise and distortion ratio (SNDR). The expression for SNDR is:

$$SNDR = \frac{P_{signal}}{P_{noise} + P_{distortion}} \tag{1.5}$$

where P_{noise} is the total noise power including quantization and electronic noise and $P_{distortion}$ is the distortion power. Substituting SNDR for SQNR in Equation 1.4 and solving for N, the effective number of bits (ENOB) of an ADC can be expressed as:

$$ENOB = \frac{SNDR - 1.76}{6.02} \text{ dB} \tag{1.6}$$

When performing design simulations, the quantization noise and distortion are simulated separately from the noise power. For this situation, another useful metric is the signal-to-quantization noise and distortion ratio (SQDR). SQDR can be expressed as:

$$SQDR = \frac{P_{signal}}{P_{qnoise} + P_{distortion}} \tag{1.7}$$

SNDR can be calculated from this metric by adding the simulated noise power into the denominator. In an effort to combine accuracy, speed, and power metrics into a single performance number, an expression for a very commonly used figure of merit (FOM) is:

$$FOM = \frac{P}{F_s \cdot 2^{ENOB}} \left(\frac{\text{J}}{conversion - step} \right) \tag{1.8}$$

where P is the power consumption in watts, F_s is the sampling frequency, and $ENOB$ is the effective number of bits from Equation 1.6.

1.2 Pipeline ADC Basics

This section begins with an introduction to the operation of a simple pipeline ADC. After the introduction, the operation of the Multiplying DAC (MDAC), an important block in pipeline ADC design, is presented in detail. This section concludes with a discussion of redundancy, a commonly used method in pipeline ADC designs for reducing the offset requirements of the sub-ADC comparators.

1.2.1 Pipeline ADC Operation

Figure 1.1 illustrates a general two stage pipelined ADC. The first stage

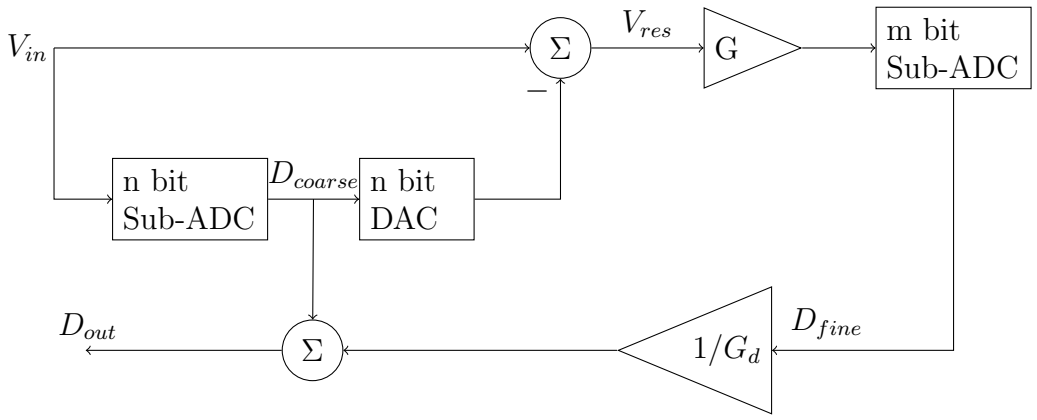

Figure 1.1: Example two-stage pipelined ADC

ADC operates in two phases, a sampling phase and an amplify/hold phase. In the first phase, an input voltage is sampled, generally using a capacitive array. Once the sampling is complete, the first stage moves into the amplify/hold phase. The n bit sub-ADC converts the input voltage into a digital code,

D_{coarse}. An n bit digital- to-analog converter (DAC) then transforms D_{coarse} to an analog voltage. The analog output from the n bit DAC is then subtracted from the input voltage, producing an error residue voltage, V_{res}. The residue voltage is bounded by:

$$-\frac{V_{ref}}{2^n} \leq V_{res} \leq \frac{V_{ref}}{2^n} \tag{1.9}$$

The residue voltage is then amplified with a gain of G. This amplifier is used to reduce the precision requirements of the downstream ADC. The precision requirements on the m bit fine ADC without an amplification stage would be m+n bits. Without amplification, V_{FS} of the second stage is given by Equation 1.9. Using this value in Equation 1.2 gives a second-stage Δ of:

$$\Delta = \frac{V_{FS}}{2^{n+m}} \tag{1.10}$$

which is equivalent to an m+n bit ADC. With an amplification stage gain of $G = 2^B$, Δ becomes:

$$\Delta = \frac{V_{FS}}{2^{n+m-B}} \tag{1.11}$$

which reduces the precision requirement to $m + n - B$ bits. Since, in general, the full-scale voltage of the second stage is equivalent to the full-scale voltage of the first stage, the amplification factor G sets the effective resolution of the input to the second stage. Generally, the subtraction and amplification stages are implemented as a single switched capacitor device, the MDAC. Section 1.2.2 discusses this MDAC operation in more depth. The second stage is sampling the output from the MDAC while the first stage is in its amplify/hold phase. At the end of the second stage sampling phase, the sampled voltage is

quantized by an m bit ADC, producing D_{fine}. D_{fine} is then passed through a digital gain stage with ideal $G_d = G$ and combined with the coarse ADC output to produce the final $(m + B)$ bit digital output, D_{out} [18]. Although this example is only for two stages, this idea could be expanded to any number of arbitrary stages by adding an MDAC with its own amplify/hold phaseto the second stage and replicating more stages. A high resolution ADC can be constructed from a series of low resolution ADCs by partitioning the conversion in this manner. For a pipeline with i stages, a latency of $^{i}/_{2}$ cycles is introduced, but the cycle time is only limited by the longest stage sampling time.

1.2.2 MDAC Operation

Figure 1.2 shows the first stage from Figure 1.1 with an n of one. The sum and gain stages are replaced with an ideal MDAC model. This particular MDAC topology is known as a non-fliparound architecture. A single-ended model is shown for simplicity. At the heart of the MDAC is an operational transconductance amplifier. For the purposes of this example, the OTA gain is assumed to be infinite, so that the voltage difference between the two OTA input terminals is zero. ϕ_1 and ϕ_2 are non-overlapping clock signals. ϕ_1 corresponds to the sample/conversion stage and ϕ_2 corresponds to the amplify/hold stage of the pipeline ADC. C_{s1} and C_{s2} are the sampling capacitors and C_f is the feedback capacitor. For the purposes of this example, these capacitors all have a value of C. When ϕ_1 is active, the input voltage, V_{in}, is sampled onto the sampling capacitors. The expression for the charge at node X at the end

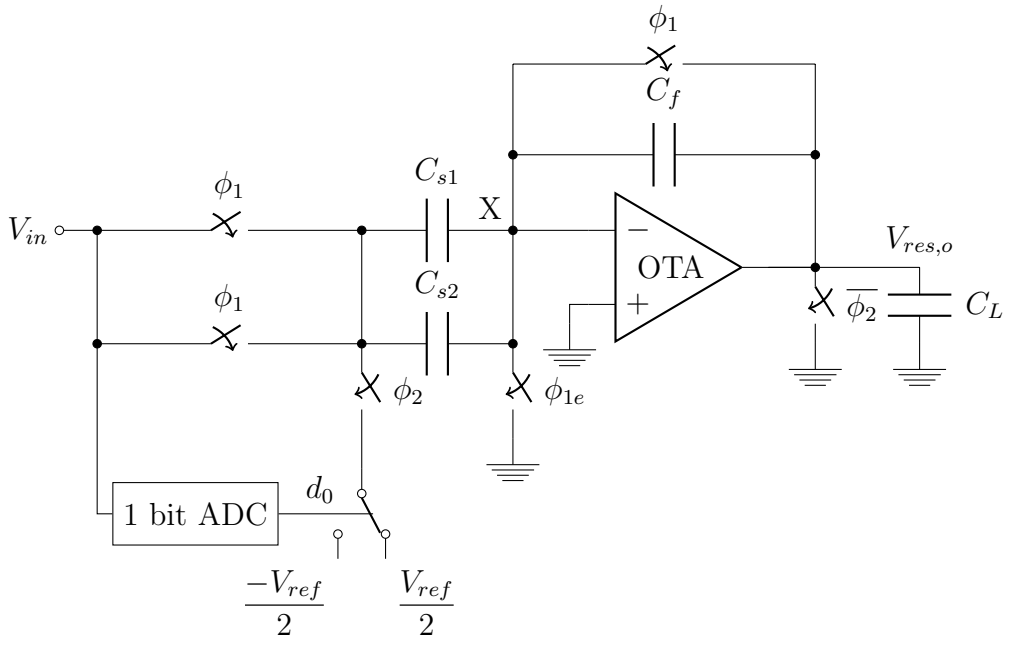

Figure 1.2: Example one bit non-fliparound MDAC

of ϕ_1, Q_{x,ϕ_1} is:

$$Q_{x,\phi_1} = -2CV_{in} \tag{1.12}$$

At the end of ϕ_1, the sub-ADC performs its conversion and connects the bottom plate of C_{s2} to $\pm\frac{V_{ref}}{2}$. When ϕ_2 is active, the charge at node X, Q_{x,ϕ_2} is:

$$Q_{x,\phi_2} = \begin{cases} -CV_{res,o} - CV_{ref} & \text{if } V_{in} > 0 \\ -CV_{res,o} + CV_{ref} & \text{if } V_{in} \leq 0 \end{cases} \tag{1.13}$$

where $V_{res,o}$ is the amplified residue voltage. From charge conservation, Q_{x,ϕ_1} and Q_{x,ϕ_2} must be equal. Setting these quantities equal to each other and

solving for $V_{res,o}$ yields:

$$V_{res,o} = \begin{cases} 2V_{in} - V_{ref} = 2(V_{in} - \frac{V_{ref}}{2}) & \text{if } V_{in} > 0 \\ 2V_{in} + V_{ref} = 2(V_{in} + \frac{V_{ref}}{2}) & \text{if } V_{in} \leq 0 \end{cases} \tag{1.14}$$

Putting Equation 1.14 in terms of G and V_{res} from Figure 1.1, the voltage at the input of the m bit ADC is:

$$V_{res,o} = 2(V_{in} \pm \frac{V_{ref}}{2}) = GV_{res} \tag{1.15}$$

Another commonly used MDAC topology is known as the flip-around topology. Figure 1.3 is the equivalent flip-around topology of Figure 1.2. A

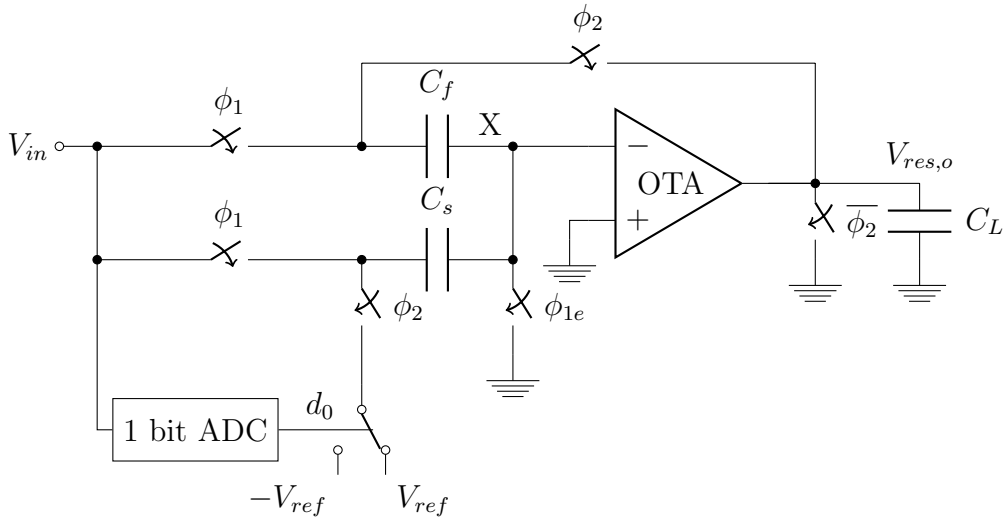

Figure 1.3: Example one bit flip-around MDAC

similar analysis as that for Figure 1.2 shows that Equation 1.14 applies to this topology as well. The advantage to using this topology is the increased feedback factor, β, from 1/3 to 1/2. Increasing the feedback factor in this way increases the speed of the MDAC by 50% [11].

1.2.3 Redundancy

Redundancy is a technique often used in pipeline ADCs to relax comparator offset requirements. To illustrate this, Figure 1.2 will be used. From Equations 1.9 and 1.14, the bound for the amplified residue output is:

$$|V_{res,o}| \leq V_{ref} \tag{1.16}$$

From this equation, it can be seen that $V_{res,o}$ is bound by the full-scale input range of the next stage ADC. Comparator offsets affect the decision levels of the sub-ADC, causing some residue voltages to exceed Equation 1.9. This will then cause $V_{res,o}$ to exceed the input range of the next stage ADC. The use of redundancy increases the resolution in the stage sub-ADC without increasing the interstage MDAC gain. In this case, the effective stage resolution remains the same, but the maximum sub-ADC decision error decreases, thus allowing some additional headroom for comparator offsets. Most pipelined designs opt for either 1 bit or ½ bit redundancy. Adding an additional bit to the stage ADC in Figure 1.2 reduces the maximum input residue voltage by a factor of two, so the bound of $V_{res,o}$ becomes:

$$|V_{res,o}| \leq \frac{V_{ref}}{2} \tag{1.17}$$

With 1 bit redundancy, the MDAC can accommodate comparator offsets of up to ½ LSB without overloading the next stage ADC. Adding 0.5 bit redundancy to Figure 1.2 involves changing the decision level for the ADC from 0 to $\pm\frac{V_{ref}}{4}$. The output from the ADC would switch the bottom plate voltage to $\pm V_{ref}$ or

0. In this example, adding 0.5 bit redundancy requires adding one less decision level than the corresponding 1 bit redundancy. The new equation for $V_{res,o}$ becomes:

$$V_{res,o} = \begin{cases} 2V_{in} - V_{ref} & \text{if } V_{in} > \dfrac{V_{ref}}{4} \\ 2V_{in} & \text{if } -\dfrac{V_{ref}}{4} \leq V_{in} < \dfrac{V_{ref}}{4} \\ 2V_{in} + V_{ref} & \text{if } V_{in} < -\dfrac{V_{ref}}{4} \end{cases} \tag{1.18}$$

Using 0.5 bit redundancy in the circuit in Figure 1.2 allows for offsets of up to 1/4 LSB. The trade-off between using the two topologies lies in the allowable comparator offset versus the additional circuit complexity.

1.3 SAR ADC Basics

This section discusses the basic characteristics of SAR ADCs, beginning with an explanation of SAR ADC operation. Next is a discussion of the major performance metrics for a SAR ADC, and their limiting factors. These metrics include accuracy, speed, and power consumption.

1.3.1 SAR Operation

SAR ADCs use a binary search algorithm to successively approximate the input voltage by comparing the input sampled voltage, V_{in} to a DAC output voltage, V_{DAC}. In many cases, the DAC is implemented using a capacitive charge redistribution method. Figure 1.4 illustrates a two bit capacitive charge redistribution SAR ADC. A single-ended version of this design is shown for simplicity. In Figure 1.4, the capacitor of size $2C$ is known as the most sig-

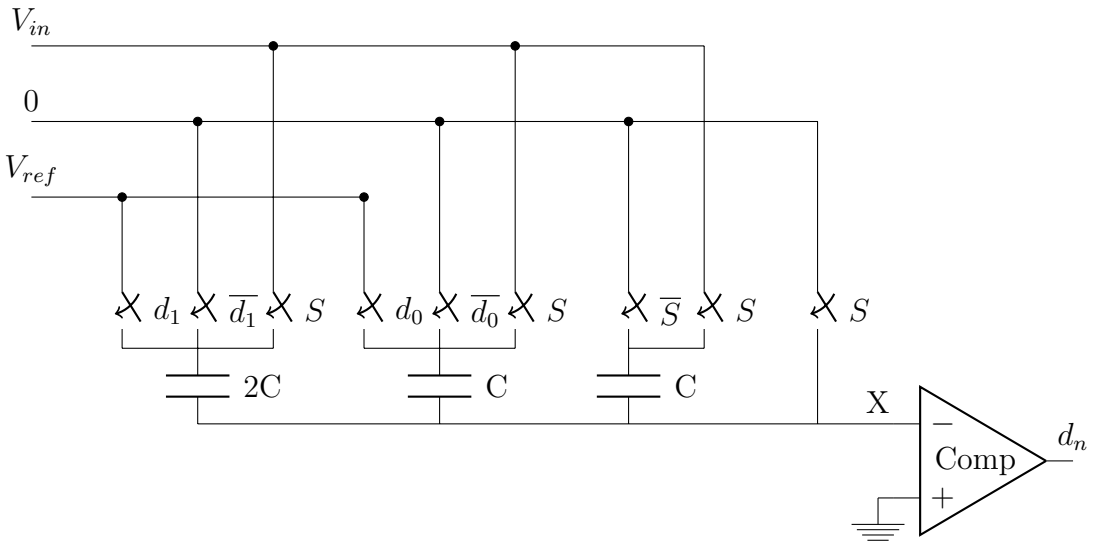

Figure 1.4: Example two bit SAR ADC

nificant bit (MSB) capacitor and the first C is known as the least significant bit (LSB) capacitor. The second capacitor of size C is known as a dummy LSB capacitor. The signals d_1 and d_0 correspond to the digital outputs from the first and second conversion steps, respectively. The digital outputs are obtained from the output of the comparator. From the figure, the total capacitance of this ADC is $4C$. A general expression for the total capacitance of an N bit SAR ADC with a unit capacitance of C is:

$$C_T = 2^N \cdot C \tag{1.19}$$

To perform a conversion, the ADC first samples the input. During this phase, the bottom plates of all capacitors are connected to V_{in} and the top plates are connected to V_{cm}. For simplicity, V_{cm} is set to zero volts. In this configuration,

the charge at node X is:

$$Q_{x,sample} = -V_{in} \cdot 4C \tag{1.20}$$

At the end of the sampling phase, the switch connecting the top plates to V_{cm} opens. The bottom plate of the $2C$ capacitor is connected to V_{ref} and all other capacitors are connected to V_{cm}. At this time, the charge on node X is:

$$Q_{x,d_1} = 4C \cdot V_x - 2C \cdot V_{ref} \tag{1.21}$$

From charge conservation, $Q_{x,sample}$ must be equal to Q_{x,d_1}. Solving for V_x yields a voltage at the positive comparator input of:

$$V_{comp,in} = V_x = -V_{in} + \frac{V_{ref}}{2} \tag{1.22}$$

The expression for the comparator output, c_{out} is:

$$c_{out} = \begin{cases} 0 & \text{if } V_{in} > \dfrac{V_{ref}}{2} \\ 1 & \text{if } V_{in} < \dfrac{V_{ref}}{2} \end{cases} \tag{1.23}$$

The digital output from the first conversion, d_1, is the logical not of c_{out}. Since d_1 controls the input switches on the $2C$ capacitor, at the end of the first conversion phase, the DAC output voltage, $V_{DAC,1}$ will be:

$$V_{DAC,1} = \begin{cases} \dfrac{V_{ref}}{2} & \text{if } d_1 = 1 \\ 0 & \text{if } d_1 = 0 \end{cases} \tag{1.24}$$

Using a similar analysis, the expression for V_x during the second conversion phase is:

$$V_{comp,in} = -V_{in} + V_{DAC,1} + \frac{V_{ref}}{4} \tag{1.25}$$

The expression for the DAC output voltage at the end of the second conversion stage is:

$$V_{DAC,2} = \begin{cases} V_{DAC,1} + \dfrac{V_{ref}}{4} & \text{if } d_1 = 1 \\ V_{DAC,1} & \text{if } d_1 = 0 \end{cases} \tag{1.26}$$

These expressions can be generalized to an N bit SAR ADC. For the n^{th} successive approximation conversion step, the positive input voltage to the comparator is:

$$V_{comp,in} = -V_{in} + V_{DAC,N-(n-1)} + \frac{V_{ref}}{2^n} \tag{1.27}$$

The general expression for the DAC output voltage at the end of the n^{th} conversion step is:

$$V_{DAC,n} = \begin{cases} V_{DAC,n-1} + \dfrac{V_{ref}}{2^n} & \text{if } d_1 = 1 \\ V_{DAC,n-1} & \text{if } d_1 = 0 \end{cases} \tag{1.28}$$

For an N bit ADC, N conversion steps are required to obtain the final digital output. This serialization of the conversion causes the limited sample rates discussed at the beginning of this chapter [12]. In general, the time taken to convert a sample as a function of the maximum single conversion step time, T_{conv} is:

$$T_{samp} = NT_{conv} \tag{1.29}$$

1.3.2 SAR ADC Accuracy

The main factors affecting the accuracy of the SAR ADC are the thermal noise from the capacitive array, the mismatch of the capacitive array, and the comparator accuracy. To achieve a desired resolution of N bits, C must

be sized large enough so that the $^{kT}/_{C}$ thermal noise power is not greater than the quantization noise. From [1], for a given resolution, N, the requirement on the total capacitance to obtain thermal noise power approximately equal to quantization noise power is:

$$C_T > \frac{24 \cdot kT \cdot 2^{2N}}{V_{ref}^2} \tag{1.30}$$

Assuming C is sized appropriately to meet thermal noise requirements, the main limiting factor for the accuracy of this topology becomes the capacitor matching. Appropriately size metal-insulator-metal (MIM) capacitors can achieve mismatch percentages of better than 0.1% [4]. A statistical analysis of the effect of mismatch on differential non-linearity (DNL) and integral non-linearity (INL) of an ADC is the most logical, since mismatches will vary from device to device. The analysis of unit current source mismatch on the DNL and INL of a binary weighted DAC in [15] can also be applied to a SAR ADC, with the unit capacitance in place of the unit current source. Assuming mismatch is a random variable with Gaussian distribution relative matching of a unit capacitance is:

$$\sigma_u = \frac{\sigma}{\mu} = \text{std}\left(\frac{\Delta C}{C}\right) \tag{1.31}$$

where ΔC is the capacitor mismatch and C is the unit capacitor size. The mismatch itself is a function of capacitor size. The relationship between the capacitor size and mismatch is generally provided by the foundry. For a given σ_u, the worst case σ_{DNL} is:

$$\sigma_{DNL} = \sigma_u \sqrt{2^N - 1} \tag{1.32}$$

The worst case σ_{INL} is:

$$\sigma_{INL} = \frac{1}{2}\sigma_u\sqrt{2^N} \tag{1.33}$$

Using these equations along with a maximum DNL and INL specification, the required mismatch percentage can be calculated. From this requirement, the minimum capacitor size to meet this mismatch percentage can be obtained from foundry data.

The final factor determining overall SAR ADC accuracy is the accuracy of the comparator. For accurate operation, the comparator must be able to resolve differences down to Δ. As discussed in Section 1.2.3, the comparator offset must be lower than the maximum allowed for in the chosen redundancy scheme. Additionally, the comparator input-referred offset noise also needs to be less than Δ, so that the comparator noise does not adversely affect decision levels [12].

1.3.3 SAR ADC Conversion Time

Two main factors control the speed of the SAR conversion, the settling time of the DAC and the comparator decision time. In general, the DAC settling time will be set by the settling time of the MSB conversion, since this conversion represents the largest excursion of the DAC output [12]. Comparators are generally designed to operate in two phases. The DAC should settle to its final voltage by the end of the first phase, so the minimum comparator decision time is given by:

$$T_{comp,min} = 2T_{DAC} \tag{1.34}$$

where T_{DAC} is the worst case DAC settling time. Higher ADC resolutions require exponentially larger MSB capacitors, and thus the maximum sampling rate decreases significantly with increased resolution. In addition to the longer settling time due to the larger MSB capacitors, each additional bit of resolution requires an additional conversion step, further limiting the sampling rate. For an N bit SAR ADC, the minimum conversion period is:

$$T_{conv,min} = NT_{comp,min} \tag{1.35}$$

Alternatively, for a given sampling rate, T_{samp}, the worst case comparator decision time is:

$$T_{comp} = \frac{T_{samp}}{2N} \tag{1.36}$$

Where a factor of two assumes that half of the sampling clock period is used for sampling.

1.3.4 SAR ADC Power Consumption

The power consumed by the SAR ADC is related to the power consumed by the comparator and the charging/discharging of the capacitor array. In general, the power of the comparator is insignificant compared to the charging/ discharging power. From [7], to sample a full-scale sine wave at Nyquist frequency with a conversion period T_s, the capacitive array will consume an average of:

$$P_{in} = \frac{C_T V_{ref}^2}{T_s} \tag{1.37}$$

and the reference generator for charge redistribution will consume an average of:

$$P_{in} = \frac{C_T V_{ref}^2}{2T_s} \tag{1.38}$$

From these equations, the exponential growth of power consumption with increasing ADC resolution, N, can be seen.

1.4 Advantages of Pipelining a SAR Topology

Aside from the latency introduced by introducing pipelining to a SAR topology, pipelining a SAR topology offers potentially significant area, power, speed, and accuracy advantages. The area and power advantages relate mainly to the reduction in total capacitance when pipelining the SAR design. Conversion speed is increased due to the reduction in the size of the MSB capacitor, as well as the reduction in conversion steps. Due to the reduction in the stage resolutions of the pipelined SAR, accuracy requirements on each stage can also be reduced.

1.4.1 Power and Area Advantages

The size of the total capacitance is a major contributor to both the size of the SAR design and to the An N bit SAR ADC pipelined by i identical stages has a total capacitance of:

$$C_T = i \cdot 2^{N/i} C \tag{1.39}$$

For sufficiently high N, pipelining can achieve a significant reduction in total capacitance. In reality, C_T will be even lower than this estimate, as C can be reduced in later stages due to the fact that the input referred thermal noise of later stages is reduced by a factor of the interstage gains. Even using this conservative estimate and applying this C_T to Equation 1.37 and Equation 1.38, one can see that for the same conversion period, pipelining can significantly reduce power consumption. The trade-off here is the additional power consumption from the $i-1$ additional interstage amplifiers, which will need to be a consideration during the design of the amplifiers. Similarly, this reduction in C_T should represent a reduction in the total area of the design, assuming that the area from the $i-1$ additional amplifiers and comparators is kept below the C_T area savings. These requirements suggest that N should be high, so that the reduction of capacitance is significant, and i should be kept low, to reduce the additional circuit complexity introduced by pipelining. Another reason to keep i low is the diminishing returns on C_T as i is increased. As an example, a 12 bit ADC will have a C_T of $4096C$. Pipelining with $i = 2$ reduces C_T to $128C$, a reduction by a factor of 32. With $i = 3$, C_T goes down to $48C$, an incremental reduction of less than a factor of 3.

1.4.2 Conversion Time Improvements

As mentioned in section 1.3.3, conversion speed is mainly limited by the settling time of the DAC and the decision time of the comparator. A similar analysis to section 1.4.1 can be applied to the size of the MSB capacitor that

limits the settling time of the DAC. In addition to the reduction in DAC settling time, the number of conversion steps is reduced to $^{N}/_{i}$, which allows for either a reduction of T_{samp} by a factor of i, or the usage of a lower power comparator with longer decision time for an equivalent T_{samp}.

1.4.3 Accuracy Requirement Relaxation

With pipelining, the resolution of each ADC is $^{N}/_{i}$. Using this value in Equation 1.33 and Equation 1.32 shows that the capacitor matching requirements are exponentially reduced with pipelining. This can be very useful to achieve higher resolutions than would be achievable from a given capacitor mismatch. Additionally, using the stage resolution in Equation 1.2, allows for a large reduction in the required accuracy of each stage comparator.

1.5 Pipelined SAR ADC vs. Pipelined Flash ADC

Flash ADCs are indisputably the sub-ADC of choice for pipelined applications requiring very high sampling rates. Flash ADCs are popular for high sampling rate applications because the critical path of a single stage conversion is the sum of the decision time of a comparator and the settling time of the residue input on the MDAC, no matter how many bits are resolved in each pipeline stage. This creates an advantage for the flash topology over the SAR topology, where sampling time is Equation 1.29. For applications with lower sampling rate requirements, however, the usage of a SAR topology as the pipelined sub-ADC has many benefits.

1.5.1 High First Stage Resolution

Obtaining a high first stage resolution is much easier with a SAR ADC than with flash. Since N bit flash ADCs require 2^N comparators, resolutions beyond a few bits incur significant area penalties [12]. In addition, from Equation 1.2, increasing the stage resolution decreases the stage Δ, which translates to stricter offset requirements on the comparators. Implementing a single low offset comparator, as in the case of a SAR sub-ADC, is much less complex than guaranteeing the same offset requirements for the large number of comparators that a high resolution flash ADC would require [10]. Having a high first stage resolution has been shown to be very advantageous in pipelined designs.

1.5.1.1 Effect on Noise Power

In [2], an analysis on the effect of multi-bit stages on thermal noise in pipelined ADCs was performed. This work showed that higher stage resolution decreases the input-referred noise contribution of downstream stages due to the higher gain of the amplifier in the multi-bit stage. Having a high resolution in the first stage thus propagates this advantage to all other stages in the design. The reduced noise power in later stages allows the later stage unit capacitor size to be scaled down, decreasing charging/discharging power in later stages.

1.5.1.2 Effect on Power Consumption

Since the accuracy requirements in the first stages of a pipelined ADC are generally the highest, the power consumption of these stages usually dom-

inates the overall ADC power consumption. In [10], the effect of a high resolution first stage on power consumption is discussed. At the end of the hold phase, the expression for V_{res} including circuit non-idealities is:

$$V_{res} = V_{ideal} + V_{err} \;\; and \;\; V_{err} = (V_{ideal} - V_{initial})e^{-\frac{T\beta G_m}{C_{L,tot}}} \tag{1.40}$$

where β is the feedback factor of the first-stage op-amp, T is the time available for settling, G_m is the amplifier transconductance, and $C_{L,tot}$ is the total output load on the op-amp. Each one bit increase in first-stage resolution decreases β by factor of approximately 2 and decreases $C_{L,tot}$ by a factor of approximately 2, implying that overall V_{err} remains unaffected by an increase in first-bit resolution. Each one bit increase in first-stage resolution also decreases the required resolution of the downstream pipeline stages, however. This reduced resolution of later stages means that a larger V_{err} is tolerable in the first-stage op- amp and that G_m can be decreased to meet the larger V_{err}. Reducing G_m implies reduced op-amp power consumption.

1.5.1.3 Effect on ADC Linearity

The benefits of a high first-stage resolution on the DNL of the ADC are shown in [1]. The expression for DNL due to capacitor mismatch in the first stage of the pipeline is:

$$DNL = \frac{k \cdot 2^{N-l/2}}{\sqrt{C_T}} \tag{1.41}$$

where l is the first stage resolution in bits and k is a mismatch constant. This shows that each additional bit of resolution in the first stage of the pipeline

reduces the DNL due to capacitor mismatch by a factor of $\sqrt{2}$.

1.5.2 Removal of Front-End Sample-and-Hold Amplifier

Another less obvious advantage to using a SAR as the pipelined sub-ADC is the ability to remove the front-end sample-and-hold amplifier (SHA). The SHA can consume about 20% to 30% of the total ADC power and limit the linearity and dynamic range of the ADC [9]. SHAs are generally required in pipelined circuits using flash sub-ADCs due to the different signal paths of the sub-ADC and sampling capacitors in Figure 1.2. In the general case, the sampling time of the sub-ADC is later than that of the sampling capacitors. Without a stable voltage on both inputs, large voltage difference between the MDAC sampled input and the sub-ADC sampled input may be observed. This difference in voltage is known as aperture error and can cause serious signal-to-noise ratio (SNR) degradation at high input frequencies [3].

Both [3] and [20] suggest methods to reduce the aperture error, including matching the time constants of both signal paths and digital error correction. Both of these methods, however, increase design complexity and power consumption. In the case of a SAR sub-ADC, the front-end SHA can be removed without any design penalty. Since both the SAR ADC and the MDAC rely on capacitive arrays, the array can be designed such that the SAR and the MDAC share the same capacitive array. Since both circuits share the same signal path, aperture error is removed without any additional design complexity [10].

1.6 Transistor Level Design Methodology

Generally, hand calculations for the design of analog circuits involve first-order approximations of the relationship between drain current, I_D, and the gate overdrive voltage:

$$V_{ov} = V_{gs} - V_t \tag{1.42}$$

where V_{gs} is the transistor gate-to-source voltage and V_t is the transistor threshold voltage. These approximations generally ignore the effects of small devices on transistor operation. These effects include velocity saturation from the horizontal field and mobility degradation from the vertical field [6]. In older processes with larger channel lengths, ignoring these effects did not adversely affect the accuracy of hand calculations as long as the transistor was operated in the strong inversion region. With increased scaling, however, these first-order models can no longer be used to accurately predict device operation. In an effort to overcome these limitations, the g_m/I_d method was developed [17]. This methodology relies on the ratio of transconductance (g_m) to drain current (I_d) as its main design control.

Most analog devices are characterized by their gain, bandwidth, and power consumption. A large g_m/I_d implies that a large transconductance can be achieved for a small amount of current, so it is also known as the current efficiency. Another useful figure of merit (FOM) is the intrinsic gain of the device, g_m/g_{ds}, where g_{ds} is the output conductance. g_m/g_{ds} usually defines the maximum gain achievable from a given transistor, so a higher g_m/g_{ds} implies

higher gain. The final important metric is the transit frequency, given by:

$$\omega_T = \frac{g_m}{C_{gg}} \tag{1.43}$$

where C_{gg} is the sum of the gate-to-source, gate-to-bulk, and gate-to-drain capacitances. For a given transconductance, a larger transit frequency implies small intrinsic capacitors. Since bandwidth is limited by transconductance and intrinsic capacitor size, knowledge of ω_T gives valuable insight into the bandwidth of the circuit. If one knows the relationship between these three FOMs, a good approximation of overall device performance can be hand calculated.

Due to short channel effects, first order equations for the relationship between the three FOMs are not suitably accurate. To overcome this issue, a simple transistor test-bench can be designed and simulated. This testbench involves characterizing the output of a transistor by sweeping its overdrive voltage. From this testbench, graphs for the relationship between g_m/I_d and g_m/g_{ds}, g_m/I_d and ω_T, and g_m/I_d and transistor size can be obtained for a given channel length [14]. Since this data is obtained from simulations, they are based on models that are much more accurate than first order approximations. Generally, increasing g_m/I_d increases the g_m/g_{ds} and decreases ω_T. From this relationship, the trade-off between increasing gain and increasing bandwidth is shown. The data gathered from these simulations can be used to develop lookup tables in tool such as Matlab or Excel. In the case of this design, lookup tables were created using Matlab.

Using the g_m/I_d methodology along with simulated technology data, a

design can exhibit excellent agreement with simulated data and even a fabricated prototype [17]. For this reason, all transistor level designs for this Master's Report leveraged this design methodology.

1.7 Organization of the Report

The rest of the report will focus on the design details of this ADC. Chapter 2 discusses architectural decisions and improvements that were applied to the general circuits described in Chapter 1. Chapter 3 discusses the full design of the ADC using ideal components. Chapter 4 covers the design and integration of the OTA, as well as final ADC performance numbers with the integrated OTA. Chapter 5 provides closing remarks, as well as a discussion of improvements and possible future work.

Chapter 2

Architectural Features

Using the pipeline and SAR architectures described in Chapter 1, some high-level architectural decisions had to be made, mainly relating to the partitioning of the design. In addition, some enhancements were applied to the basic architectures in order to enhance overall performance. These decisions and enhancements are the subject of this chapter.

2.1 Architectural Decisions

Before any block-level specifications could be created, the partitioning of the pipeline stages had to be decided. First the total number of pipeline stages needed to be decided. Next, the resolutions for each stage needed to be decided. Finally, a suitable redundancy scheme for design had to be chosen.

2.1.1 Number of Pipeline Stages

The discussion in Section 1.4 highlights the diminishing returns of increasing the number of pipeline stages. Beyond two pipeline stages, the effect on power consumption from the reduction in capacitance would likely be outweighed by the power consumption of the additional MDAC OTA. Similarly,

to realize the potential benefits of pipelining on the speed of the ADC, the speed of the comparator must be increased as well. At some point, this will place a prohibitive constraint on the comparator speed. In addition, SAR converters show the most advantage over flash ADC's at higher resolutions. Using more than two pipeline stage for a 12 bit design would require an average stage resolution of 3 or less bits. In addition, from the discussion in Section 1.5.1, a high first stage resolution is desired to achieve maximum benefits. For these reasons, a two stage design was chosen.

2.1.2 Operation Partitioning

After determining the number of stages, each stage's required operations must be partitioned between the two phases of the sampling clock. For the second stage ADC, which must only perform sampling and conversion, partitioning the operations between the two clock phases is straightforward. Due to the latency introduced by the first stage, the sampling will occur in the second clock phase, and the conversion will occur in the first clock phase of the next clock cycle. The first stage ADC must perform three operations: sampling, conversion, and amplification. Assuming that half of a clock phase is allotted for conversion, this means that either the sampling or the conversion time must be halved. To achieve the same sampling resolution in half the time, the input switch resistance must be halved. Similarly, to achieve the same static error from the MDAC in half the time, the MDAC bandwidth must be doubled. Another side effect to sharing a clock phase between con-

version and amplification is that the available sampling time for the second stage would also be halved. In general, reducing switch resistance is simpler to implement than increasing the MDAC bandwidth. In addition, doubling the MDAC bandwidth would likely increase power consumption more than halving the switch resistance. For these reasons, as well as the lack of side effects on the second stage, the sampling and conversion phases were combined in this design.

2.1.3 Stage Resolution

Next, the resolutions for each stage had to be determined. From the above discussion, the conversion time for the first stage will be half that of the second stage. From Equation 1.36, for equivalent comparator specifications in both stages, the ratio of second stage resolution to first stage resolution should be 2:1. In a 12 bit ADC, this would mean a 4 bit first stage and an 8 bit second stage. While one may assume that the eight bit second stage would require a much larger DAC settling time, this would likely not be the case. A first stage resolution of 4 bits would imply a high closed loop gain in the MDAC. The high closed loop MDAC gain means that the input-referred offset noise of the second stage capacitor array is significantly reduced. This reduction in input-referred noise means that the unit capacitor for the second stage ADC could be decreased, and thus the difference between the capacitance of the two stages would likely not be significant. Beyond simply striving for equivalent comparator specifications, the first stage resolution should be as high as possi-

ble in order to achieve all the benefits from Section 1.5.1. A fundamental limit to the benefits of first stage resolution does exist, however. This limit is due to the output parasitics in the MDAC OTA. From Equation 1.40, G_m can be decreased in part because each 1-bit increase in first stage resolution decreases $C_{L,tot}$ by a factor of 2. This decrease in $C_{L,tot}$ no longer applies once the load capacitance becomes dominated by the self-parasitics of the MDAC op-amp. This implies that, for optimized power consumption, the first stage resolution should be increased to the point that output capacitance is dominated by the op-amp parasitics [10]. The issue with using the parasitics of the op-amp as the deciding factor for stage resolution is that without knowledge of stage resolution, the requirements for MDAC bandwidth and loop gain cannot be known. These specifications are strongly linked to parasitic capacitance size, and thus a sort of chicken and egg problem is created. In [10], a 5 bit first stage and a 7 bit second stage were used, so this was used as a starting point. This also seemed like a reasonable partition in terms of comparator specifications. The speed requirement for the second stage comparator is relaxed with this partitioning, but this can also mean that a lower power comparator can theoretically be used for the second stage.

2.1.4 MDAC Redundancy Scheme

Without MDAC redundancy, overloading of the second stage ADC is basically guaranteed. For the purposes of this design, it was decided that 1 bit redundancy was the preferred scheme. First, the high stage resolution

places stricter requirements on the comparator offset, so the additional offset headroom provided by 1-bit redundancy makes comparator implementation simpler. Second, unlike in flash ADCs, the implementation of a half bit of redundancy in SAR ADCs is not very straightforward. For flash ADCs, a half bit of redundancy involves the addition of comparators and the modification of their reference voltages. Implementing half bit redundancy in a SAR ADC would require changing the fundamental binary search algorithm used, which is a much more significant design modification. Implementing an extra bit of redundancy for a SAR, on the other hand, requires the addition of a single capacitor and an increase in comparator speed requirements. For these reasons, 1 bit redundancy was used.

2.2 Architectural Enhancements

Beyond the basic pipeline and SAR architectures discussed in Sections 1.2 and 1.3, respectively, some additional architectural enhancements were used. First, a half-gain MDAC architecture was used. Second, the dummy LSB in the SAR sub-ADCs was exploited to achieve an additional bit of resolution.

2.2.1 Half-Gain MDAC

In [10], an MDAC with a half-gain architecture is used to decrease power consumption. In general MDAC designs with 1 bit redundancy, the closed loop MDAC gain is 2^{N-1}. In half-gain designs, this closed loop gain is reduced to 2^{N-2}. For this design, the closed loop gain is reduced from 32 to

16. Feedback factor in terms of closed loop gain is:

$$\beta = \frac{1}{A_{cl} + 1} \tag{2.1}$$

where A_{cl} is the closed loop gain of the MDAC. From this equation, reducing the MDAC gain by a factor of two increases the feedback factor by approximately a factor of two, from 1/33 to 1/17. From 1.40, for the same V_{err}, this feedback factor reduction implies that op-amp G_m can also be reduced by approximately a factor of two. In addition to reduced power consumption, reducing the feedback factor also decreases DNL due to finite op-amp gain, since

$$|DNL_{max}| \propto \frac{2^{N-M}}{A_{OLDC}\beta} \tag{2.2}$$

where N is the total ADC resolution, M is the number of bits resolved in the first stage, and A_{OLDC} is the open loop op-amp gain [10]. One disadvantage to this design technique is that the usage of a half-gain architecture reduces the available output swing from $\frac{V_{ref}}{2}$ to $\frac{V_{ref}}{4}$. Lowered output swing place stricter requirements on the downstream ADC. To obtain the same resolution as an ADC with a full-gain upstream MDAC, an additional bit of resolution is required. In this design, a reference voltage of $\frac{V_{ref}}{2}$ is used for the second stage pipeline ADC. As long as the second-stage ADC is not thermal noise limited, adding an additional bit of resolution is achievable.

2.2.2 Achieving an Additional Bit of Resolution With the Dummy LSB Capacitor

The dummy LSB capacitor in SAR ADCs can also be used to achieve an extra bit of resolution without increasing the total capacitance. Figure 2.1 expands Figure 1.4 to illustrate this concept. In Figure 2.1, the dummy LSB

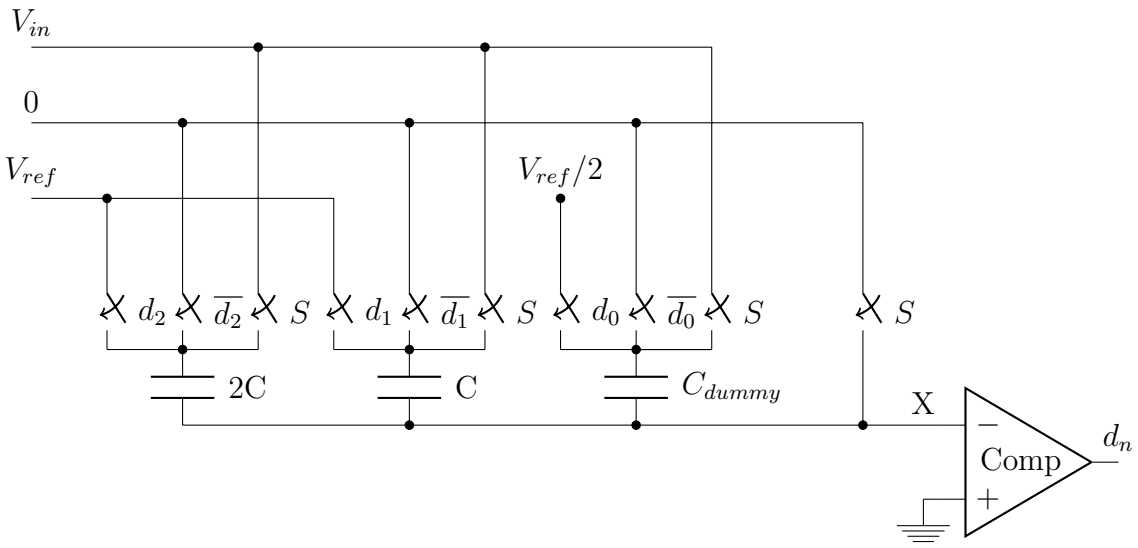

Figure 2.1: Example three bit SAR ADC using the dummy LSB capacitor

capacitor has an additional switch connected to its top plate. This switch is connected to an additional voltage source of value $\frac{V_{ref}}{2}$. Unlike the ADC from Figure 1.4, this ADC has three conversion stages. The charge on node X after the third sampling phase is:

$$Q_{x,d_0} = 4C \cdot V_x - C \cdot \frac{V_{ref}}{2} - 2C \cdot V_{ref} \cdot d_2 - C \cdot V_{ref} \cdot d_1 \tag{2.3}$$

The positive input voltage to the comparator is:

$$V_{comp,in} = -V_{in} + V_{DAC,2} + \frac{V_{ref}}{8} \tag{2.4}$$

where $V_{DAC,2}$ is equivalent to:

$$V_{DAC,2} = \frac{V_{ref} \cdot d_2}{2} + \frac{V_{ref} \cdot d_1}{4} \tag{2.5}$$

From Equation 1.27, this is the expression for $V_{comp,in}$ that one would expect for a standard 3 bit SAR ADC. Thus, without increasing the total capacitance, a two bit SAR ADC has been transformed into a three bit SAR ADC. The disadvantage to this scheme is that an additional reference voltage is required, but the significant reduction in total capacitance allowed by using this architecture in high resolution ADCs should make this trade-off worthwhile. Both the first and second stage SAR ADCs took advantage of this architectural feature. Modifying Equation 1.19, the new expression for the total capacitance of an N bit ADC with a unit capacitance of C is:

$$C_T = 2^{N-1} \cdot C \tag{2.6}$$

Chapter 3

ADC Design Using Ideal Circuit Blocks

After defining all of the architectural features of the design, the next step was to use ideal circuit blocks to simulate the entire ADC design. Designing in this manner gave valuable insights into how different circuit block specifications affected overall ADC performance. This chapter begins with an explanation of the ideal circuit blocks that were used in this design. It follows with a discussion of the design and simulated results from a single-ended version of the ADC. This chapter concludes with a discussion of the design of the fully differential ADC and its simulated performance.

3.1 Ideal Circuit Blocks

A set of ideal circuit blocks were provided by Dr. Nan Sun for this design. These circuit blocks include a single-ended OTA, a differential OTA, a comparator, a switch, a clock generator, and a single-ended to differential signal converter. This section discusses these blocks in more detail, with input/output details as well as settable parameters.

3.1.1 OTA

The OTA model is used in the design of the first-stage MDAC. The single-ended and differential OTA models are essentially the same, the difference between the two being that the differential model has an additional output pin for the negative output voltage. The pins for the OTA models are given in Table 3.1. The differential model has an internal common-mode

Name	Pin Type	Description
Vdd	Supply	DC power supply
Vin	Input	Positive input voltage
Vinb	Input	Negative input voltage
Vcmo	Output	Common-mode output voltage
Vout	Output	Positive output voltage
Voutb	Output	Positive output voltage, differential model only

Table 3.1: OTA Ideal Model Pins

feedback (CMFB) circuit that ensures the common-mode output of the OTA matches the voltage on *Vcmo*. In this design, the power supply is 1.8V.

In addition to the pins, the OTA models also have a number of parameters that govern its behavior. These parameters are given in Table 3.2 The

Parameter	Description
Gain	OTA DC gain
f_T	Transistor transit frequency
g_m/I_d	Current efficiency
g_m	Transistor transconductance
noiseconst	Constant controlling total noise power

Table 3.2: OTA Ideal Model Parameters

device characteristics that are controlled by these parameters are the output voltage, the input capacitance, and the input-referred noise. The *Gain* parameter is the ratio of the output voltage to the input voltage. The input capacitance of the OTA is:

$$C_{in} = \frac{g_m}{2\pi \cdot f_T} \tag{3.1}$$

where g_m and f_T are OTA parameters. This relationship is based on Equation 1.43. An internal current source generates current based on the g_m/I_d and g_m parameters. The input-referred noise of the OTA is:

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{4 \cdot kT \cdot noiseconst}{g_m} \tag{3.2}$$

where *noiseconst* and g_m are OTA parameters.

3.1.2 Comparator

The pins for the ideal comparator model are given in Table 3.3. When

Name	Pin Type	Description
Vin	Input	Positive input voltage
Vinb	Input	Negative input voltage
CLK	Input	Clock signal
d	Output	Digital decision
db	Output	Logical not of db

Table 3.3: Comparator Ideal Model Pins

$CLK = 0$V, the comparator operates in a tracking mode. In this mode, the input voltages are sampled onto capacitors inside the model. When $CLK =$

1.8V, the comparator goes into its decision phase. In the decision phase, the output d is given by:

$$d = \begin{cases} 1 & \text{if } V_{in} > V_{inb} \\ 0 & \text{if } V_{in} < V_{inb} \end{cases} \tag{3.3}$$

3.1.3 Clock Generator

The clock generator is used to generate the non-overlapping clocks for the design. The pins for this block are given in Table 3.4. The parameters

Name	Pin Type	Description
f1	Output	ϕ_1 clock signal
f1e	Output	ϕ_1 clock signal with early falling edge
f2	Output	ϕ_2 clock signal
f2e	Output	ϕ_2 clock signal with early falling edge
f1b	Output	Complementary ϕ_1 clock signal
f1eb	Output	Complementary ϕ_1 clock signal with early falling edge
f2b	Output	Complementary ϕ_2 clock signal
f2eb	Output	Complementary ϕ_2 clock signal with early falling edge

Table 3.4: Ideal Clock Generator Pins

that control the behavior of these outputs are given in Table 3.5.

Parameter	Description
period	Clock period
t_early	Time difference between the falling edge of f1 and f1e
t_edge	The rise and fall times
t_nonoverlap	The non-overlapping time between f1 and f2

Table 3.5: Ideal Clock Generator Parameters

3.1.4 Switch

The switch model has three pins, given in Table 3.6 The switch is open

Name	Pin Type	Description
A	Input/Output	One side of switch
B	Input/Output	One side of switch
ctrl	Input	Control input

Table 3.6: Ideal Switch Pins

when the voltage on the *ctrl* pin is less than 0.9V. When the voltage on *ctrl* is greater than 0.9V, the switch is closed and A is connected to B. The switch has only one parameter, given in Table 3.7.

Parameter	Description
ron	Closed switch resistance

Table 3.7: Ideal Switch Parameters

3.1.5 Single-to-Differential Converter

This block takes in a single-ended signal along with a common-mode voltage and outputs a differential voltage. The pins for the single-to-differential converter are given in Table 3.8 The relationship between the output voltages and the input voltage is:

$$V_{out} = V_{cmi} + \frac{V_{in}}{2} \tag{3.4}$$

$$V_{outb} = V_{cmi} - \frac{V_{in}}{2}$$

Name	Pin Type	Description
Vin	Input	Single-ended input voltage
Vcmi	Input	Common-mode input voltage
Vout	Output	Positive output voltage
Voutb	Output	Negative output voltage

Table 3.8: Ideal Single-Ended-to-Differential Converter Pins

3.2 Calculation of Design Parameters

Before any schematic entry or simulation could be performed, the required design parameters needed to be calculated. These correspond to the parameters of the ideal circuit blocks, as well as the size of the capacitors for both pipeline stages. A Matlab script was used to perform all of the calculations outlined in this section.

3.2.1 Calculation of Capacitor Size

The main factor determining the required capacitor size is thermal noise. As mentioned in Section 1.3.2 most designs try to obtain thermal noise that is on the order of quantization noise. In order to achieve this, the noise power has to be partitioned between all of the noise sources. In the case of this design, the noise sources are the first and second stage capacitive arrays and the OTA. The partitioning chosen for this design was 45% of total noise power allotted to the first stage capacitor array, 45% for the OTA, and 10% for the second stage capacitive array. The reasoning behind allotting such a small percentage to the second stage capacitive array is that the output noise

of the second stage will be divided by the closed loop gain of the MDAC, 16, when calculating input-referred noise. Having such a large closed loop gain should mean that the effect of the second stage thermal noise on overall quantization noise should be very small. For a 12 bit ADC with a full-scale voltage of 2V, the quantization noise power is $141\,\mu V_{rms}$. Using this value, the maximum noise calculations in Table 3.9 can be obtained. While input-referred

Noise Source	Noise Power (nV^2)	RMS Noise Voltage (μV_{rms})
12 bit ADC Quantization Noise	19.9	141
Stage 1 Capacitors	8.94	94.6
OTA	8.94	94.6
Stage 2 Capacitors	1.99	4.46

Table 3.9: Maximum Input Referred Noise

noise is the metric used for calculating SNDR, most measurements obtain the output-referred noise. For this reason, it is also useful to look at the maximum output-referred noise for each of these noise generators. In an effort to balance the total noise contribution with the required power consumption, the maximum output-referred noise for the second stage was scaled by a factor of A_{cl} instead of the typical A_{cl}^2 [15]. The output-referred noise calculations are summarized in Table 3.10.

With the maximum noise power for the capacitive arrays defined, the sizes of the capacitors could be calculated. Figure 3.1 is a simplified model of the MDAC used in this design. In this figure, the capacitive arrays for both stages are lumped into single capacitors, C_{s1} and C_{s2}. An additional feedback

Noise Source	Noise Power (μV^2)	RMS Noise (mV_{rms})
Stage 1 Capacitors	2.29	1.5
OTA	2.29	1.5
Stage 2 Capacitors	0.318	0.1783

Table 3.10: Maximum Output Referred Noise

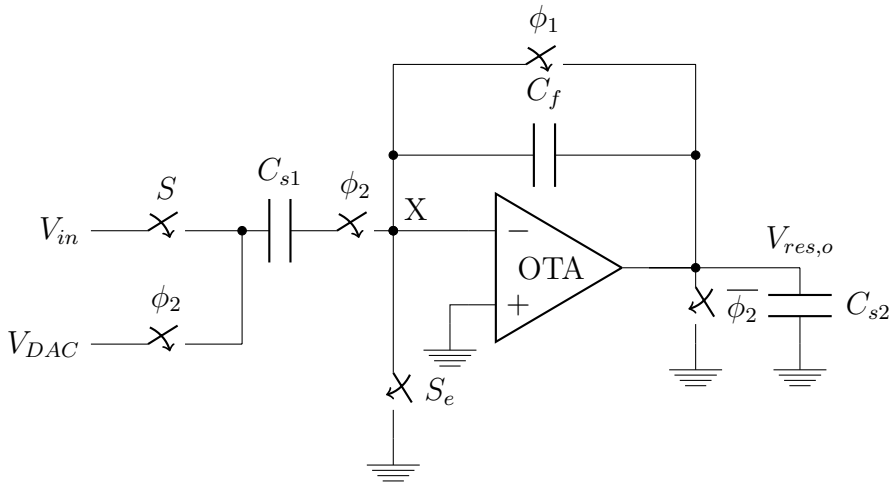

Figure 3.1: Simplified Schematic of MDAC

capacitor, C_f, sets the closed loop gain of the MDAC. The expression for the closed loop gain is:

$$A_{cl} = -\frac{C_{s1}}{C_f} = 16 \tag{3.5}$$

In addition, the SAR control logic, switches, and comparator are abstracted away as a final output voltage, V_{DAC}, that is applied to C_{s1} during ϕ_2. Also, the sampling switches are labeled with S instead of ϕ_1 to signify that ϕ_1 is now split into a sampling and conversion phase. During the sampling phase, the

OTA is no longer connected to the input capacitance, and thus has no effect on the output noise. An equivalent schematic for the MDAC in the sampling phase is given in Figure 3.2. In this configuration, the output-referred noise

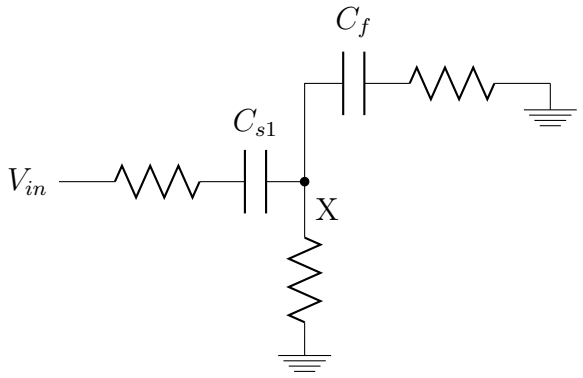

Figure 3.2: Equivalent MDAC Schematic in the Sampling Phase

is [15]:

$$\begin{aligned}
\overline{v_o^2} &= \frac{\overline{q}_x^2}{C_f^2} \\
&= \frac{kT(C_{s1}+C_f)}{C_f^2} \\
&= \frac{kT}{C_f}\left(1+\frac{C_{s1}}{C_f}\right) \\
&= \frac{16kT}{C_{s1}} \cdot (17) \\
&= (0.5) \cdot (2.29\,\mu\mathrm{V}^2)
\end{aligned} \tag{3.6}$$

where the relationship from Equation 3.5 was used to put the equation in terms of C_{s1}. Since this calculation only accounts for the single-ended noise contribution from C_{s1}, the maximum output noise power was multiplied by a

factor of 1/2. Solving Equation 3.6 for C_{s1} yields:

$$C_{s1} = \frac{16kT \cdot 17}{(0.5) \cdot (2.29\,\mu V^2)} \tag{3.7}$$
$$= 976.3\,fF$$

Using Equation 2.6, the stage 1 unit capacitance is:

$$C_{u1} = \frac{C_{s1}}{2^{(6-1)}} \tag{3.8}$$
$$= 30.51\,fF$$

Using the value of C_{s1} in Equation 3.5, the feedback capacitance is:

$$C_f = \frac{976.3\,fF}{16} \tag{3.9}$$
$$= 61.02\,fF$$

The only contribution from the second stage capacitance to the total output-referred noise is kT/C noise. The expression for C_{s2} in terms of maximum output noise power is:

$$C_{s2} = \frac{kT}{\overline{v}^2_{on,max}} \tag{3.10}$$
$$= 129.3\,fF$$

From Equation 2.6, C_{u2} is calculated to be 2.02 fF. Using a unit capacitance of 20.28 fF, the value of C_{s2} is:

$$C_{s2} = 2^{7-1} \cdot (20.28\,fF) \tag{3.11}$$
$$= 1.30\,pF$$

The values for C_{s1}, C_{s2}, and C_f fully specify the capacitances of this design.

With unit capacitance values for both stages calculated, the statistical mismatch could be calculated to ensure that it was within reasonable bounds. Table 3.11 summarizes the statistical effect of mismatch on the DNL and INL of each stage. The mismatch standard deviation is assumed to be 1%. From

Stage	Resolution (bits)	σ_u	σ_{INL} (LSB)	σ_{DNL} (LSB)
1	6	0.01	0.057	0.079
2	7	0.01	0.0035	0.007

Table 3.11: Capacitor Mismatch Effect on ADC INL and DNL

these calculations, it can be seen that the capacitor mismatch has a minimal effect on INL and DNL.

3.2.2 Calculation of OTA Model Parameters

Once noise partitioning and the calculation of the capacitor sizes was performed, all of the OTA model parameters could be calculated. First, the required OTA gain was calculated, followed by the g_m/I_d and the transit frequency. Finally, a calculation of the required OTA bandwidth was performed, which was used to calculate the required OTA transconductance.

The required OTA loop gain is determined by the specified static gain error that is presented to the ADC. The static gain percentage, ϵ_s, in terms of OTA loop gain is [14]:

$$\epsilon_s = \frac{1}{T_0} \tag{3.12}$$

where T_0 is the OTA loop gain. For a single-stage OTA, the relationship between T_0 and the OTA open-loop gain is:

$$\begin{aligned} T_0 &= \beta G_m R_o \\ &= \beta A_{OLDC} \end{aligned} \tag{3.13}$$

where G_m is the transconductance of the OTA, R_o is the OTA output resistance, and A_{OLDC} the OTA open loop gain. The *Gain* OTA parameter is equivalent to A_{OLDC}. For the static error to not have a significant effect on the accuracy of the downstream ADC, the static error was decided to be $1/2$ LSB. To obtain this, the expression for ϵ_s is:

$$\begin{aligned} \epsilon_s &= \frac{\Delta_2}{2 \cdot V_{FS,2}} \\ &= 0.0039 \end{aligned} \tag{3.14}$$

where Δ_2 is the LSB size of the second stage ADC, and $V_{FS,2}$ is the full-scale voltage of the second stage. The full-scale voltage of the second stage is reduced to 1V by the usage of the half-gain MDAC. Using Equations 3.14 and 3.12, the required loop gain is:

$$\begin{aligned} T_0 &= \frac{1}{\epsilon_s} \\ &\approx 256 \\ &\approx 48\,\text{dB} \end{aligned} \tag{3.15}$$

Using Equations 3.13 and 3.15, the required open-loop gain is:

$$\begin{aligned} A_{OLDC} &= \frac{1}{\epsilon_s \cdot \beta} \\ &\approx 4352 \\ &\approx 73\,\text{dB} \end{aligned} \tag{3.16}$$

Interestingly, this value holds for any 12 bit pipelined ADC regardless of its stage resolutions. For each additional bit resolved in the second stage, the feedback factor and the LSB size increases by a factor of approximately two, so the overall open-loop gain requirement remains unchanged. Once the required open-loop gain has been determined, some assumptions had to be made about the implementation of the OTA in order to calculate g_m/g_{ds}, g_m/I_d, and ω_T. The assumption made for this design was that a triple-cascoded amplifier would be used. Cascode topologies are very power efficient due to their load compensation [5]. The load compensation also makes designing a stable amplifier a less challenging task. Finally, for the same g_m/g_{ds}, a cascode provides more gain than a two-stage amplifier. The main limitation of cascode devices is their lower output swing. This design mitigates this issue through the use of the half-gain MDAC. The gain of a triple-cascode is approximately:

$$A_{OLDC} = \frac{1}{2}\left(\frac{g_m}{g_{ds}}\right)^3 \tag{3.17}$$

From Equation 4.4, the required g_m/g_{ds} is calculated to be 20.57. From the g_m/I_d lookup functions mentioned in Section 1.6, the g_m/I_d OTA parameters is 4.0325 and the ω_T OTA parameter is 45.5 GHz. The g_m/I_d specified for this

design was probably too low for a practical design, since g_m/I_d is inversely proportional to the transistor overdrive voltage. Increasing g_m/I_d in the actual implementation would decrease the static error, so the this issue would not constrain the static error. Increasing g_m/I_d does decrease the transit frequency, which means larger parasitic capacitances. Once g_m was calculated, the effect of raising g_m/I_d on parasitic capacitance could be more fully explored.

In order to calculate the required OTA transconductance, the allowable dynamic error must be specified. The dynamic output error is directly tied to the bandwidth of the OTA. For this design, it was desired to settle to within $1/8$ LSB of the second stage in a half clock cycle. The OTA loop crossover frequency in terms of dynamic error is [14]:

$$\begin{aligned} f_c &= \left(\frac{-f_s}{\pi}\right) \ln\left(\epsilon_d \left[1 - \beta \frac{C_f}{C_f + C_{s2}}\right]\right) \\ &= \left(\frac{-10\,\text{MHz}}{\pi}\right) \ln\left(\frac{1}{8 \cdot 2^7}\left[1 - \frac{1}{17} \cdot \frac{61\,\text{fF}}{61\,\text{fF} + 1.3\,\text{fF}}\right]\right) \\ &= 22.1\,\text{MHz} \end{aligned} \tag{3.18}$$

where f_s is the sampling frequency and ϵ_d is the tolerable dynamic error. The loop-crossover frequency is equivalent to the $-3\,\text{dB}$ bandwidth of the closed loop MDAC. The expression in Equation 3.18 purposefully ignores the effects of slewing on settling time. Slewing occurs when the differential output current saturates to to large differential input voltage steps. During slew time, the amplifier output is driven with an approximately constant current bias that is equal to the tail bias. For the amplifier to operate in this condition, the input

differential voltage, V_{id} must be:

$$|V_{id}| > \sqrt{2} \cdot V_{ov} \tag{3.19}$$

where V_{ov} is the overdrive voltage of the input transistor. From long-channel equations, V_{ov} is approximately:

$$V_{ov} \approx \frac{2}{g_m/I_d} \tag{3.20}$$

The maximum differential input voltage step for a design is limited by its closed-loop gain and the absolute value of its maximum differential output voltage. An expression for the maximum V_{id} in terms of these values is:

$$|V_{id,max}| = \frac{|V_{od,max}|}{A_{cl}} \tag{3.21}$$

where $V_{od,max}$ is the maximum differential output voltage and A_{cl} is the closed-loop gain. Combining Equations 3.19, 3.20, and 3.21, solving for g_m/I_d, and plugging in values for this design, the maximum g_m/I_d that can be used without slewing is:

$$\begin{aligned}(g_m/I_d)_{max} &= \frac{2.8 \cdot A_{cl}}{|V_{od,max}|} \\ &= \frac{2.8 \cdot 16}{1} \\ &= 44.8\,\mathrm{V}^{-1}\end{aligned} \tag{3.22}$$

In the weak inversion region, MOSFET operation is very similar to bipolar junction transistor (BJT) operation. The g_m/I_d in weak inversion approximates the g_m/I_d of a BJT with a reduction factor caused by capacitive division

on the base potential of the MOSFET. The expression for g_m/I_d of a BJT is:

$$(g_m/I_d)_{BJT} = \frac{1}{V_T} \tag{3.23}$$

where V_T is the thermal voltage. This corresponds to a g_m/I_d value of approximately $38\,\mathrm{V}^{-1}$ at room temperature. Since g_m/I_d of a MOSFET is always below the g_m/I_d of a BJT, the g_m/I_d value calculated in Equation 3.22 is not achievable. For this reason, slewing was ignored in the derivation of the settling time equation. An alternative expression for the closed loop bandwidth in terms of the OTA transconductance is:

$$f_c = \frac{\beta G_m}{2\pi C_{L,tot}} \tag{3.24}$$

where $C_{L,tot}$ is the total load capacitance of the OTA. In order to calculate G_m from Equation 3.24, the total load capacitance must be known. An approximate expression for the total load capacitance that neglects OTA parasitics is:

$$\begin{aligned} C_{L,tot} &= C_{s2} + (1-\beta)\cdot C_f \\ &= 1.36\,\mathrm{pF} \end{aligned} \tag{3.25}$$

Using the calculated load capacitance in Equation 3.24 and solving for the OTA transconductance yields:

$$\begin{aligned} G_m &= \frac{(2\pi f_c)(C_{L,tot})}{\beta} \\ &= 3.2\,\mathrm{mS} \end{aligned} \tag{3.26}$$

With G_m now calculated, the potential effect of raising g_m/I_d on parasitic capacitance could be examined. Table 3.12 shows the simulated total gate capacitance for a number of g_m/I_d values. For the total gate capacitance to

g_m/I_d	C_{gg} (fF)
10	19
15	32.7
20	75
22	133

Table 3.12: Total Gate Capacitance for Given g_m/I_d

be 10% of the load capacitance, g_m/I_d has to be set to larger than 22. This gives adequate design headroom so that the unrealistic g_m/I_d used for the ideal design was not given further consideration.

The final OTA parameter that needed to be calculated was the *noisec-onst*. The expression for the noise of a basic cascode stage is [14]:

$$\overline{v_o^2} = \frac{1}{\beta}\gamma\left(1 + \frac{g_{m2}}{g_{m1}} \cdot \frac{\omega_c}{\omega_{p2}}\right) \tag{3.27}$$

where g_{m2} is the transconductance of the common-gate transistor, g_{m1} is the transconductance of the common-source transistor, γ is a parameter that is a function of transistor parameters and bias conditions, and ω_{p2} is the non-dominant pole frequency. In order to simplify this expression to a constant, some approximations need to be made. First, the parameter γ is assumed to be 1, which is a reasonable approximation for short channel devices [16]. Next, for optimal settling performance, a phase margin of 75° is assumed. This constraint means that the ratio of ω_{p2} to ω_c is 3:1. Finally g_{m1} and g_{m2}

are assumed to be approximately equal. Using these approximations, dividing both sides of the expressions by the equivalent noise bandwidth, and referring the noise to the input gives the expression:

$$\begin{aligned}\frac{\overline{v_i^2}}{\Delta f} &= kT\frac{\left(\frac{1}{1.57\beta^2}+\frac{1}{4.71\beta^2}\right)\cdot 2\pi}{A_{cl}^2\cdot g_m} \\ &= \frac{6.02kT}{g_m}\end{aligned} \tag{3.28}$$

Another abstraction used in this simplification is that this only includes noise sources from a basic cascode stage, not from a triple-cascode. To allow for some headroom from the additional noise of the additional common-gate transistor, a factor of 1.5 was applied to the input-referred noise. Applying this factor, setting Equations 3.28 and 3.2 equal to each other, and solving for *noiseconst* yields a *noiseconst* value of 2.36. Using the calculated g_m, the total input-referred OTA noise is $20.5\,\mu V_{rms}$. Comparing this value to that from Table 3.9, the calculated value is well below the maximum input-referred noise, so even if these approximations yielded an optimistic approximation, there was plenty of additional noise headroom to compensate.

Table 3.13 summarizes the OTA parameters that were used for the ideal design.

3.2.3 Switch Parameters

The only parameter that needed to be set for the ideal switch was its closed resistance. Generally one should strive for a switch RC that is 10 times

Parameter	Value
Gain	4352
f_T	4.55×10^{10}
g_m/I_d	4.0325
g_m	0.0033
noiseconst	2.36

Table 3.13: Parameter Settings for Ideal OTA Model

or greater than the bandwidth of the OTA. The distributed nature of the switches and capacitors made obtaining a numerical expression for the ideal switch resistance difficult. It was decided to start at a low resistance of $100\,\Omega$ and increase the resistances until it began affecting system performance.

3.2.4 Clock Generators

A number of clock domains were needed for this design. Many of these clocks also had to be gated so that they only operated in one phase of the main clock. The main clock generator was used to generate the ϕ_1 and ϕ_2 signals. Another clock generator was used to generate the sampling clocks. Two additional clock generators were needed to control the SAR clocks. The required period for the SAR clocks was calculated using Equation 1.36. Table 3.14 summarizes all of the clock signals in the design, their frequencies, and the signals that were used to gate the clocks. Figure 3.3 shows a general waveform of a single cycle of the design clocks and how the signals relate to each other.

Clock Signal	Clock Frequency	Description	Gating Signals
ϕ_1	10 MHz	Phase 1 of 10 MHz clock	N/A
ϕ_2	10 MHz	Phase 2 of 10 MHz clock	N/A
S	20 MHz	Sampling clock, used to control sampling switches	ϕ_1
comp1clk	240 MHz	Stage 1 SAR Clock	$\overline{S}, \phi_1$
comp2clk	140 MHz	Stage 2 SAR Clock	ϕ_2

Table 3.14: Design Clocks

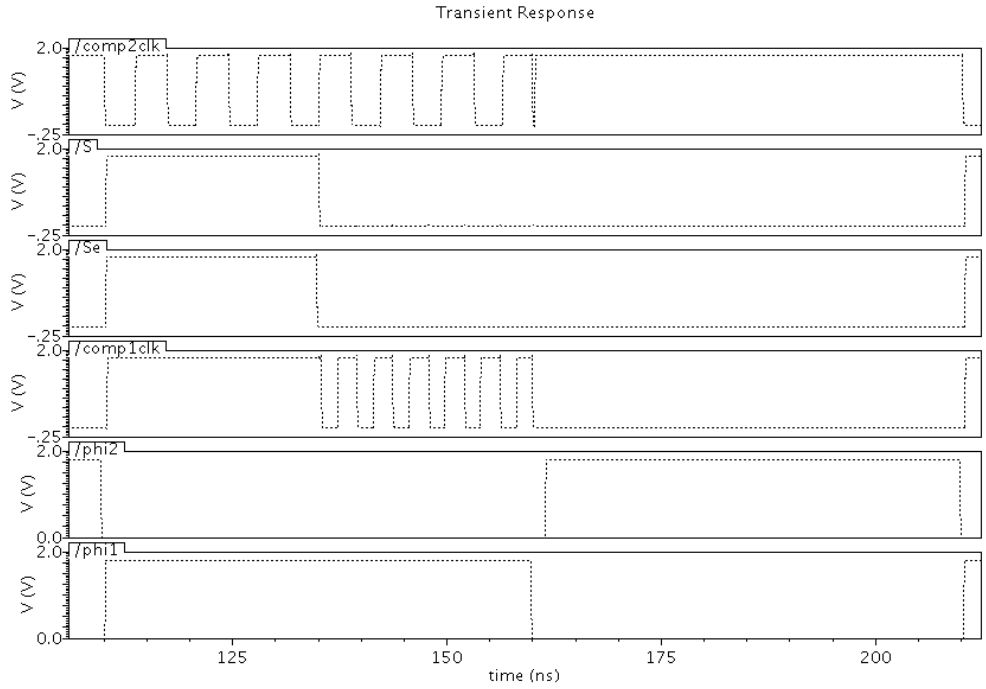

Figure 3.3: Waveform of a Single Cycle of Design Clocks

3.3 Design of Single-Ended ADC

With the calculation of all the general design parameters complete, the design could move into the circuit design and simulation phase. The first design was a single-ended one, as this design was easier to debug. Although all of the previous chapter's calculations assumed a differential design, only a few changes needed to be made to accommodate the single-ended design. First, the full-scale voltage would only be 1 V for the single-ended design. Second, all noise calculations were done assuming differential capacitor arrays, so expected noise contributions had to be halved for the single-ended design. The operation of the first and second stage SAR ADCs follows the explanation in Section 1.3.1, with the operation expanded to six and seven bits, respectively. The first task in the single-ended design was to design the digital SAR control logic. Next, the clocking scheme, capacitor sizes, and digital logic were verified by using ideal component parameters. Once all of the surrounding logic had been verified, the calculated parameters from Section 3.2 were put into the ideal models. With the calculated parameters, transient simulations were run to verify that the MDAC settling met the specifications from Section 3.2.2. Once adherence to the settling specification was verified, a longer simulation was run to obtain device SQDR. Once the 74 dB SQDR was achieved, noise simulations were run to ensure that the total input-referred noise met the design specifications. Once all this was complete, work moved on to the differential design.

3.3.1 Single-Ended SAR Control Logic

The SAR control logic determines the operation of all of the conversion switches in the design. In addition, it uses the comparator output to construct the digital output code of the ADC. All of the digital logic described in this section was designed at the gate level using standard cells. Due to the low speed, in digital terms, of the clocks in this design and the low complexity of the digital logic, minimum sized gates were used throughout the design. Using minimum sized gates decreases the dynamic power consumption of the digital blocks in the design.

The first-stage SAR logic was designed first with the intention of expanding the logic to the second stage. The SAR control logic governs the behavior of the d_i switches in Figure 1.4. The first-stage control logic was implemented as a state machine with the negative edge of the SAR clock controlling state transitions. Table 3.15 summarizes the operation of the SAR state machine. In this table, C corresponds to the comparator output at the end of the previous state, and d_ip corresponds to the d_i signal maintaining its previous state. When the ADC is in the sampling phase, clock signal S is active and all other switches are open. This is accomplished by gating all the d_i and $\overline{d_i}$ switch control inputs with $\overline{S}$. During this phase, the SAR state machine is reset to its initial state. Once the sampling phase ends, the first stage SAR clock, *comp1clk*, falls, the state machine moves into State 1, and the SAR begins its conversion operation. For the state machine to complete all of its operations, seven *comp1clk* falling edges are required. Once the state

State Outputs		Switch Outputs					
Current State	Next State	d_5	d_4	d_3	d_2	d_1	d_0
0	1	0	0	0	0	0	0
1	2	1	0	0	0	0	0
2	3	$\overline{C}$	1	0	0	0	0
3	4	d_{5p}	$\overline{C}$	0	0	0	0
4	5	d_{5p}	d_{4p}	$\overline{C}$	1	0	0
5	6	d_{5p}	d_{4p}	d_{3p}	$\overline{C}$	1	0
6	7	d_{5p}	d_{4p}	d_{3p}	d_{2p}	$\overline{C}$	1
7	0	d_{5p}	d_{4p}	d_{3p}	d_{2p}	d_{1p}	$\overline{C}$

Table 3.15: Stage One SAR Control Logic State Machine

machine reaches State 7, it maintains its state until the next sampling clock rising edge. This state machine must hold its state throughout ϕ_2 so that the residue voltage is properly amplified by the MDAC. Once the sampling clock rising edge occurs, the state machine is reset to State 0, and all of the SAR switches open.

The SAR control logic for the second stage ADC is almost identical to the first stage. An additional state and digital output were added to accommodate the seven bit ADC. In this case, eight falling *comp2clk* edges are required. Also, the second stage state machine is reset by the negative edge of ϕ_2, which corresponds to the sampling phase of the second stage ADC. Other than these differences, the operation of the second stage SAR is identical to that of the first stage.

3.3.2 Test Setups

Before continuing with the discussion on simulating the ADC using ideal component parameters, it is worthwhile to discuss the simulation tests that were used throughout the design of this ADC. When evaluating the performance of the entire pipelined system, four main tests were used for all design iterations. The first was a short transient simulation to ensure that the MDAC output was settling properly and the digital outputs were being set properly. The next test was a longer transient simulation that was used to perform a DFT on the digital output. Once performance in these two simulations met specifications, two different types of noise simulations were run, in order to provide a means of verifying that the noise results were accurate. First, AC noise simulations were run on the ADC in both its sampling and amplification phases. Next, a transient periodic noise simulation was run on the ADC. Once transistor level models for the OTA had been integrated into the full ADC, power consumption simulations were also performed on the design. This section describes in more detail each of these simulations.

3.3.2.1 Transient Settling Test

In this test, a full-scale voltage step was applied to the input of the ADC. The digital output was checked to ensure that the output was the maximum digital code from the ADC. If the digital output was not its maximum, this implied an error with the digital control logic that would be fixed. Next, the output of the MDAC at the end of ϕ_2 was checked to ensure that the MDAC

settling specifications were met. If the circuit was not settling properly, this meant that the *Gain* or g_m OTA model parameters were not large enough and needed to be corrected. In the case of differential designs, a full-scale negative input was also applied. If the digital output code was correct and the MDAC settled within specifications, this test was considered successful.

3.3.2.2 Transient DFT Test

In this test an input sine wave with a frequency of (31/64)×10 MHz was applied to the input of the ADC and the simulation is run for 64 cycles. Once the test is complete, a Matlab script is used to perform a 64-point DFT on the output samples and obtain an SQDR. This input frequency was chosen for a few reasons. First, this frequency is very close to the Nyquist frequency of the ADC, so the ADC is being tested close to its theoretical maximum frequency. Second, when capturing a 64-point DFT, exactly 31 cycles of this input frequency will be sampled. Having an integer number of periods ensures that no spectral leakage occurs in the DFT and therefore no windowing has to be applied to the input samples. Last, the number of cycles and the number of DFT samples is mutually prime in order to obtain random quantization noise. When the mutually prime criteria is not met, the quantization noise is more deterministic and periodic, so the DFT power is spread across fewer bins. If the SQDR meets specification, this test is considered passed. In terms of simulation using ideal components, an ideal SQDR for a 12 bit ADC of 74 dB was expected.

3.3.2.3 AC Noise Analysis

AC Noise analysis computes a static DC operating point, and computes an AC noise output power using this operating point. Since this ADC operates in two phases, the circuit schematics could not be used as designed when performing AC analysis. Two different schematics had to be created for simulation, one that models the device in its sampling phase, and one that models the device in its amplification phase. In the sampling phase a schematic similar to that in Figure 3.2 was used. For the sampling phase AC noise analysis, the first stage capacitive network was fully modeled, not lumped together. Since the second stage capacitive array only contributes kT/C noise, it was modeled as a lumped capacitance. For the amplification phase AC noise analysis, a circuit similar to that of Figure 3.1, with only the ϕ_2 switches closed. The first stage capacitive array was again fully modeled, while the second-stage array was modeled with a lumped capacitance. The sum of the noise power from each of these simulations was the total ADC noise output power. If the output noise power was less than that defined in Table 3.10, this test was considered successful. A failure of this test meant that capacitor sizes likely needed to be enlarged, or OTA noise needed to be decreased by increasing OTA g_m. Another signal that something was wrong with the simulation was if it did not match the next test, the AC periodic noise simulation. In the case that the simulations did not match, an issue with the simulation setup was generally assumed.

3.3.2.4 AC Periodic Noise Analysis

In this test, a periodic steady state (PSS) simulation is combined with a transient periodic noise (PNOISE) simulation to give a calculation of the total noise power. In this case, the circuit simulator tries to solve for the periodic operation of the circuit. Once a periodic steady state solution is achieved, it calculates the noise across the period at a given time point. The point chosen for this simulation was at the end of the amplification phase. This simulation was the most prone to having setup issues due to the large number of required run settings. An excellent overview of using PSS and PNOISE analysis is in [8] and the recommendations from this paper were used in setting up the simulation correctly. Using AC noise simulations, the number of sidebands and maximum AC frequency to use were determined for this design. Table 3.16 summarizes the PNOISE parameters used for all simulations of this design.

Parameter	Value
Beat Frequency	5 MHz
Accuracy	conservative
Maximum Sidebands	400

Table 3.16: PNOISE Simulation Setup

3.3.2.5 Power Consumption Test

Although the power consumption test did not become truly relevant until the OTA had been integrated into the design, it is worthwhile to discuss it in the context of the full ADC design. For this test, the ADC was stimulated

with the same input from the transient DFT test described in Section 3.3.2.2. While the power consumption of the ADC is generally dominated by the static bias current of the OTA, the switching activity on the digital control logic and the sampling capacitors contributes some dynamic power. The amount of switching activity is dependent on the input signal presented to the ADC. In order to obtain an accurate estimation of total current consumption a number of input amplitudes needs to be applied to the ADC. In order to achieve this, a transient test is run with a duration of ten sampling cycles. This corresponds to just under five cycles of the input sinusoid, so a good distribution of input values should be obtained. The average current through the supply voltage is calculated and multiplied by the supply current value in order to obtain the total power consumption.

3.3.3 Simulation Using Ideal OTA Model Parameters

After designing the full single-ended ADC circuit, performance testing could commence. In an effort to separate the verification of the SAR operation from the verification of the pipeline block parameters, ideal OTA model parameters were used in the first design simulations. In this case, ideal OTA parameters refers to using a very large gain and transconductance, so that the error in the MDAC output is negligible. By doing this, any errors in the digital output could only be the result of bugs in SAR sub-ADCs. During this simulation phase, the transient settling and transient DFT tests were used to verify proper operation.

A number of bugs were discovered during this testing phase. A large number of these had to do with errors in the state machine logic that were easily caught during the initial transient settling test. Two bugs relating to the relationship between the clock domains proved to be the most difficult to debug.

First, the time between the last decision of the first-stage SAR ADC and the rising edge of the ϕ_2 clock was not great enough. This meant that the last DAC output voltage from the SAR was not fully settled by the time amplification started, causing errors in the residue voltage that was initially amplified. Two solutions were considered to fix this. First, the *comp1clk* speed could be increased to 280 MHz to allow for an extra clock cycle between the last decision phase and the start of the amplification phase. This option would required a slight redesign of the first stage state machine, as well as an increase in comparator decision time of over 15%. Second, the start of the amplification phase could be delayed slightly to allow adequate time for the last DAC voltage to settle before amplification started. This solution would mean decreasing the overall amplification time slightly, which would require an increase in the OTA transconductance to maintain the same dynamic error. Simulations showed that increasing the time between the last SAR decision and the amplification phase to 1.3 ns allowed the DAC output voltage to fully settle and for the amplified voltage to be within specification for all samples. This caused a decrease in the amplification time from 48.8 ns to 48.5 ns. Recalculating the required OTA bandwidth and transconductance

using Equations 3.26 and 3.18 showed that the transconductance only needed to increase to 3.3 mS to maintain the same dynamic error. Since the required increase in OTA transconductance was minimal, decreasing the amplification time slightly was the chosen solution to this issue.

Next, an issue with the second-stage SAR clocking was found. The time between the last falling edge of the second stage SAR clock and the ϕ_2 signal was causing the state machine to reset before the final bit decision was captured. This caused the least significant bit of the digital output to always be 0. Since the second stage comparator already had a lower speed requirement than that of the first-stage, it was decided to add another clock cycle to the second stage SAR ADC. This caused an increase in *comp2clk* from 140 MHz to 160 MHz. Some changes to the control logic were likely required to implement the differential SAR, so it was decided to fix this issue without raising the clock frequency at that time. Figure 3.4 shows the modifications made to the clocking scheme. Markers *M0* and *M1* in Figure 3.4 show the time difference between the falling edge of *comp1clk* and the rising edge of ϕ_2. Markers *M1* and *M2* show the reduction in amplification time. The waveform for *comp2clk* shows the additional clock cycle that was added.

Once these bugs were fixed, the transient DFT simulation was run on the design. Figure 3.5 shows the final DFT output from this iteration of the design. With an SQDR of 74 dB, this iteration of the design could be considered complete.

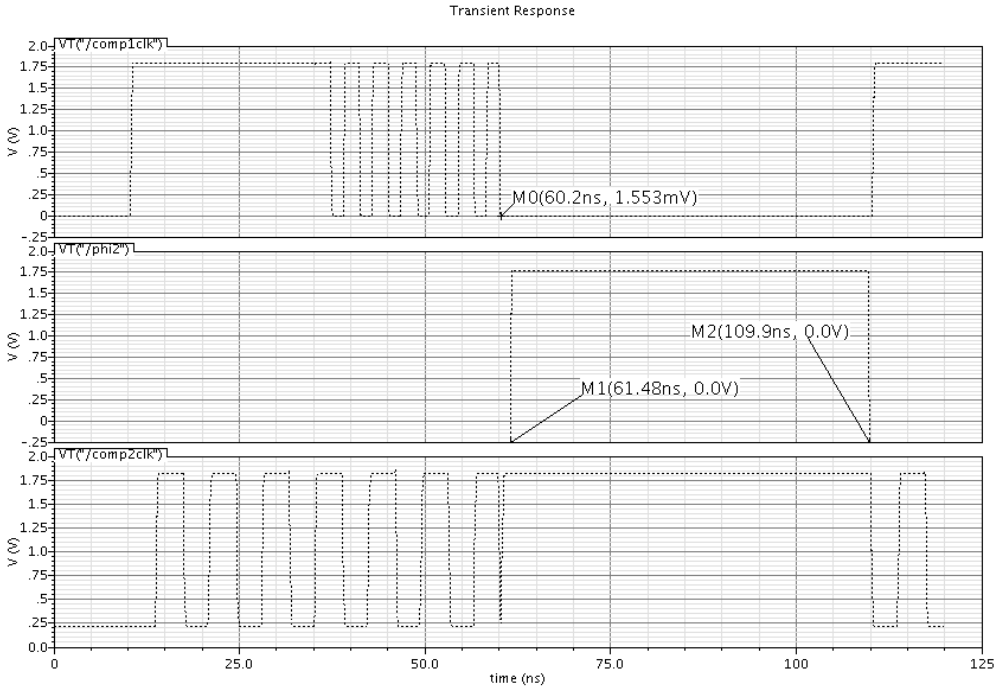

Figure 3.4: Clocking Modifications Made for Ideal Component Parameter Design

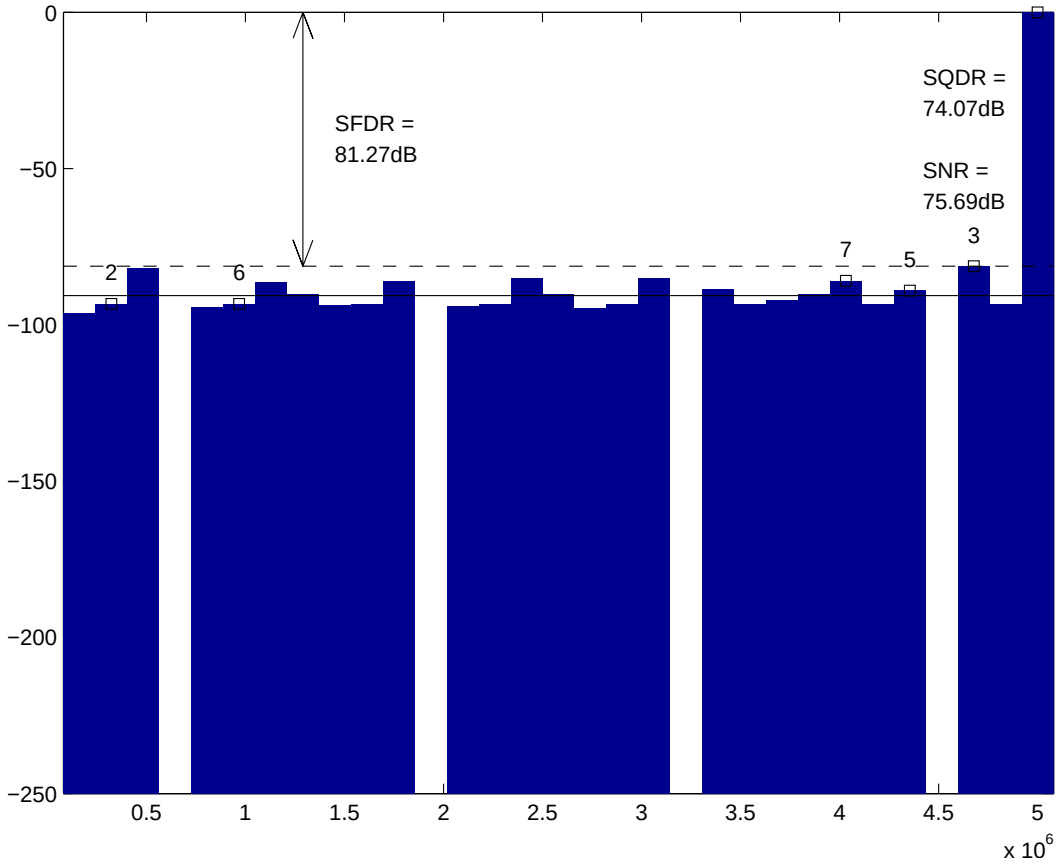

Figure 3.5: Final DFT Output of Single-Ended Model With Ideal OTA Parameters

3.3.4 Simulation with Calculated OTA Model Parameters

Once the ideal SQDR was achieved with ideal OTA model parameters, the calculated model parameters were used and simulations were run again. In this case, the transient settling simulation and transient DFT simulations were run first. After these simulations, the noise simulations were run to verify the noise behavior of the circuit.

The first verification step was running transient simulations. Figure 3.6 shows the output voltage of the MDAC during the amplification stage with full-scale voltage input. At the end of the amplification phase, the MDAC output voltage is 848.5 mV With a full-scale input, the expected MDAC output is:

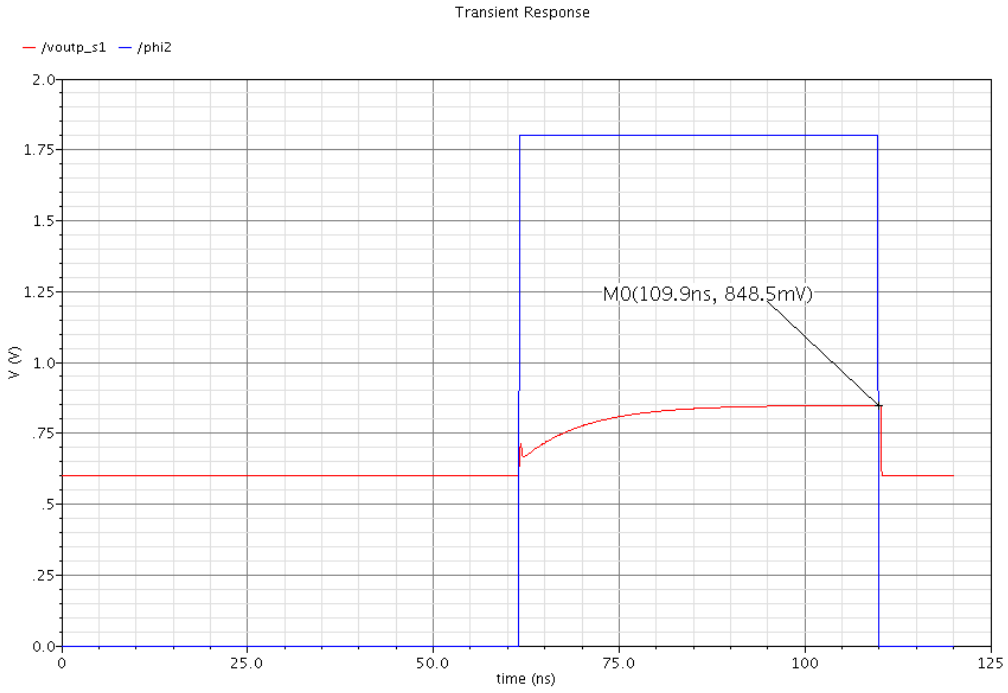

Figure 3.6: Transient Settling of Single-Ended ADC With Ideal Components

$$V_{MDAC} = \frac{V_{ref}}{4} + V_{cm} \tag{3.29}$$

where V_{cm} is the common-mode voltage. In this case, the common-mode voltage is set to 600 mV, the expected output voltage is 850 mV. From Figure 3.6, the settling error is -1.5 mV. The maximum error is the sum of the static and dynamic error specifications, or 2.4 mV. The full-scale input error was within this error envelope, so the testing moved on to transient DFT.

The initial transient DFT simulation yielded an SQDR of 74 dB, which met the required specification. After achieving this metric, the switch resistances were increased in order to reduce the size and power consumption of the switches when implemented as transistors. After running a number of times, a sampling switch resistance of 400 Ω was found to still produce SQDR. All other switch resistances were set to 500 Ω. Figure 3.7 shows the final DFT from these simulation runs.

After obtaining an SQDR of 74 dB from the transient DFT simulation, noise simulations could be run. First the AC sampling and amplification phase noise simulations were run. Figures 3.8 and 3.9 are graphs of the integrated output noise obtained from these simulations. Additionally, an AC noise simulation was run with the OTA noise generator turned off, in order to compare the calculated OTA noise power to that of the simulation. These results are summarized in Table 3.17. The only noise value that significantly diverges from its calculated value is that of the AC hold phase noise, despite the OTA noise being very close to its calculated value. It was first thought that the C_{s2}

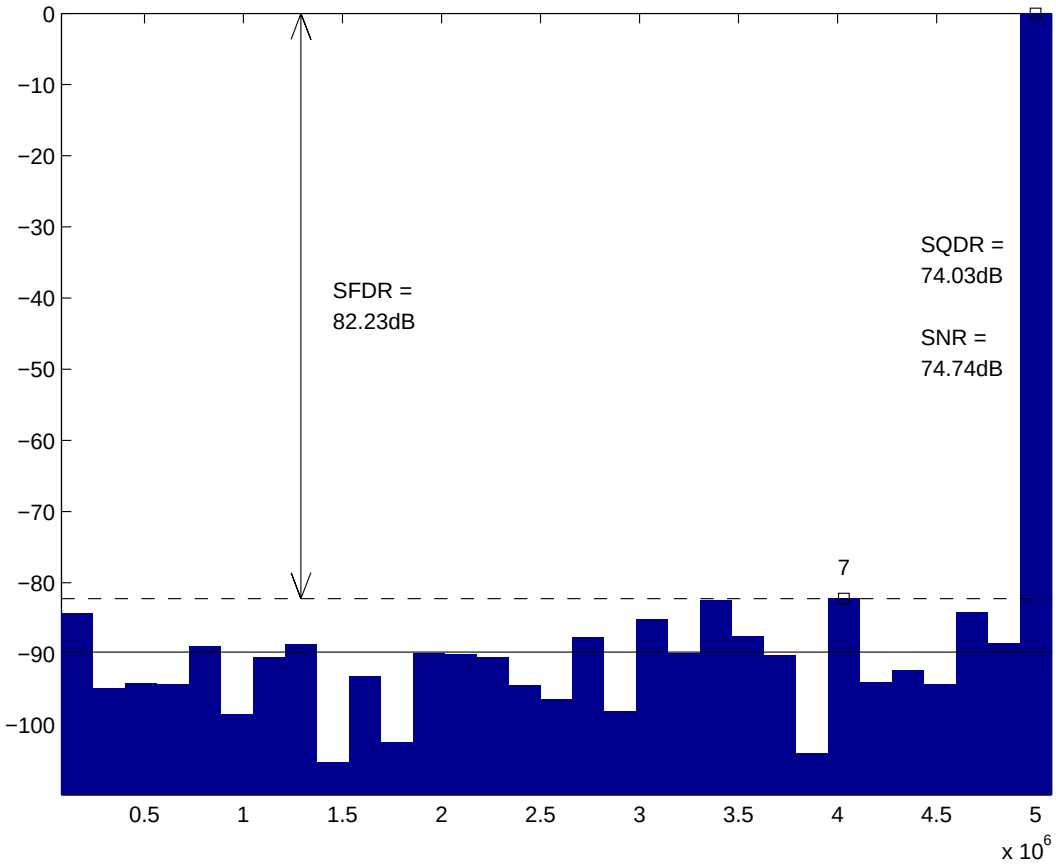

Figure 3.7: DFT of Single-Ended ADC With Calculated Parameters

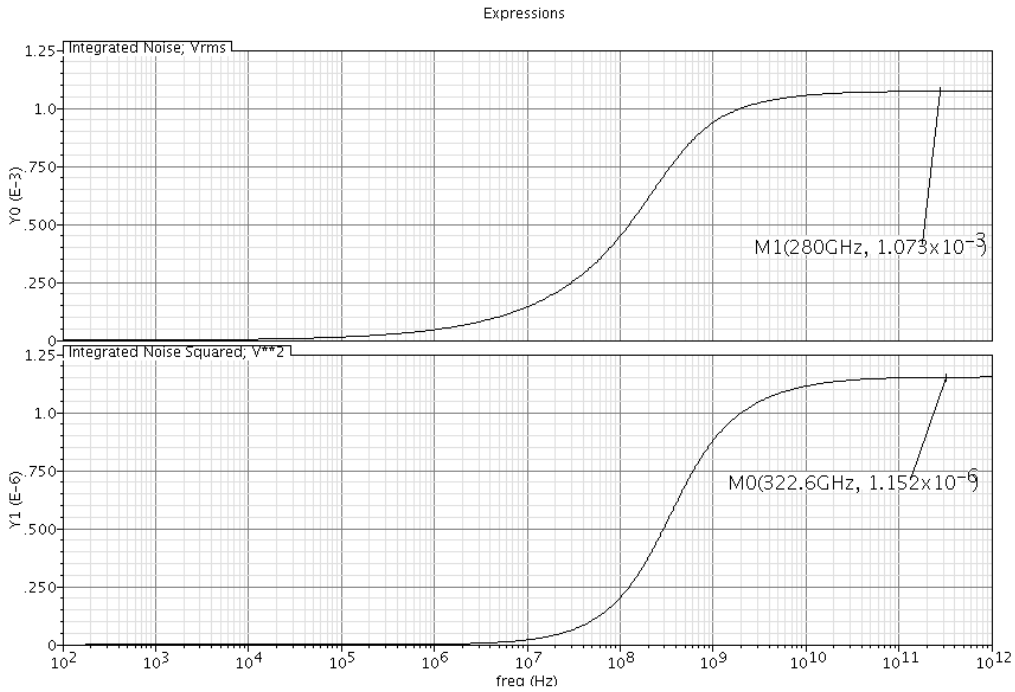

Figure 3.8: AC Noise During Sampling Phase of Single-Ended ADC

Setup	AC Sampling Noise (mV_{rms})	Total AC Hold Noise (mV_{rms})	AC Hold OTA Noise (mV_{rms})	AC Total Noise (mV_{rms})
Simulation	1.07	0.44	0.32	1.16
Calculation	1.07	0.41	0.33	1.10
Design Target	1.07	1.56	1.51	1.89
Error (%)	0.31	7.10	-1.69	5.63
Headroom (%)	-0.48	72.20	78.66	38.89

Table 3.17: Single-Ended AC Output Noise Power Summary

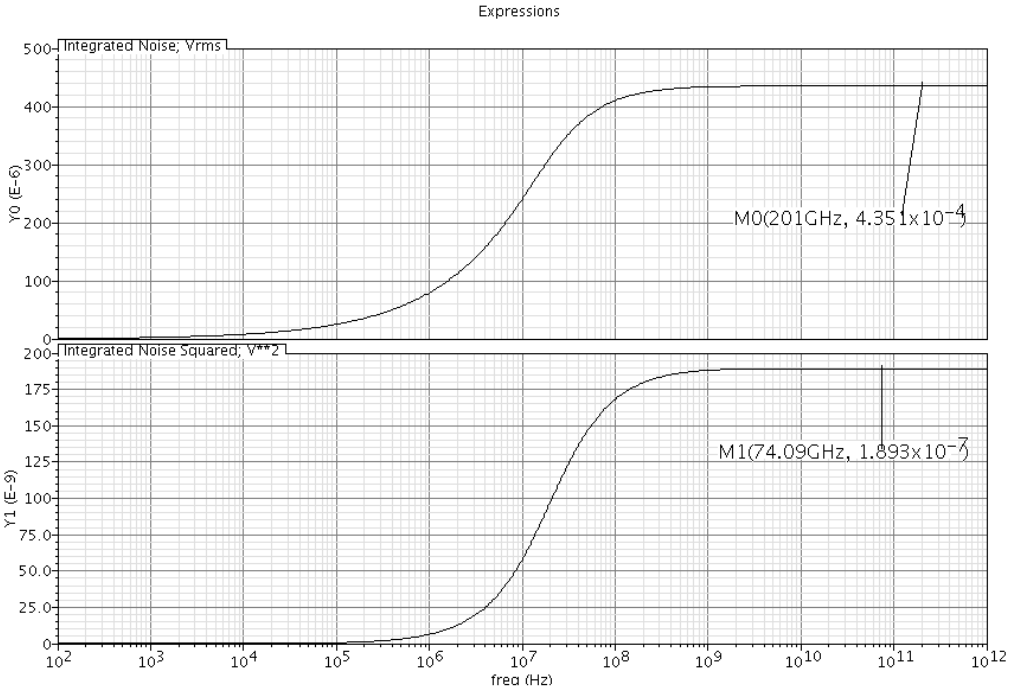

Figure 3.9: AC Noise During Amplification Phase of Single-Ended ADC

noise contribution may not have been calculated correctly. To test this, all noise sources were turned off except for the switch at the output of the stage two capacitive array. The output noise in this case matched the calculated kT/C noise, so this was determined to not be the cause of error. Further simulations revealed that the switch resistances at the input of the MDAC were contributing significant noise, which was not accounted for in the noise calculations. Since both the hold noise power and the total noise power were well within their budgets, the switch resistance was not changed as a result of this finding. While no changes were made, the switch resistance was kept as a knob to tune the total output noise power if, after implementing the transistor level design, total output noise became an issue. Next, a PSS/PNOISE simulation was run to verify the AC noise simulations. Figure 3.10 shows the integrated root-mean-square (RMS) output noise voltage from this simulation. Table 3.18 translates this result into an output noise power and compares it to that from the AC simulations. The PNOISE simulations show good agreement

Setup	Total Noise Power (mV_{rms})	Error vs Calculation (%)	Error vs AC Simulation (%)
PNOISE Simulations	1.22	6.69	5.44

Table 3.18: Single-Ended PNOISE Output Noise Summary

with both the AC Simulations and the calculations. With good agreement between both simulations and the calculations, as well as a total output noise power that was well within budget, the noise simulations were considered a success.

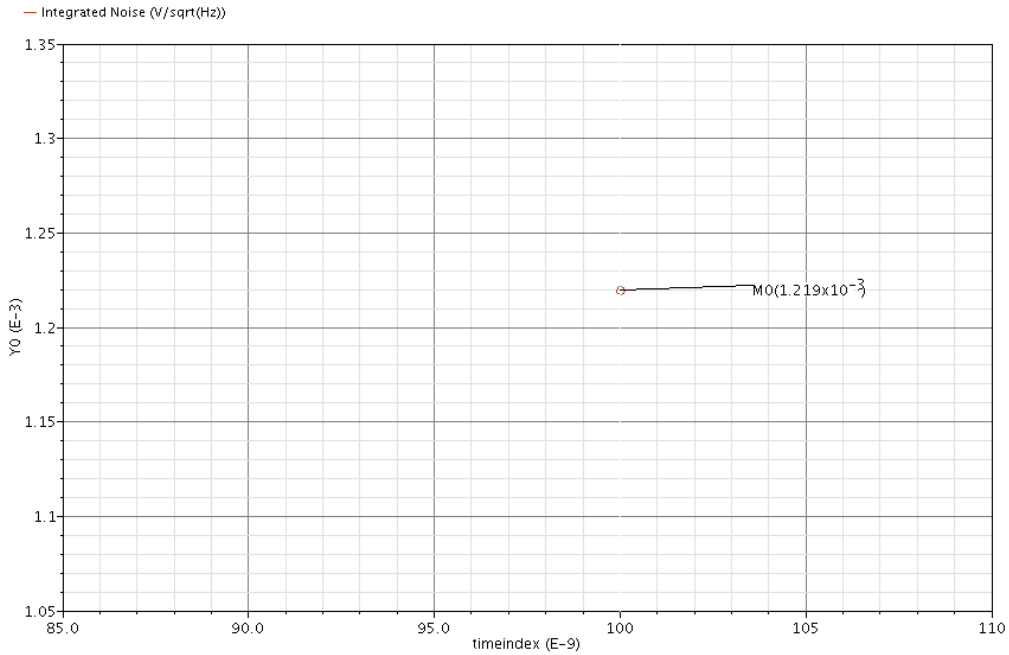

Figure 3.10: Single-Ended PNOISE Simulation Result

With both noise simulations and transient performance simulations complete, a full SNDR of the single-ended system could be calculated. Solving for the distortion and quantization noise power in Equation 1.7 yields:

$$P_{qnoise} + P_{distortion} = \frac{\frac{1}{2}\left(\frac{V_{FS}}{2}\right)^2}{SQDR} = 4.94\,\mathrm{nV}^2 \tag{3.30}$$

Since the PNOISE result gave the highest output noise, that was the value used for the SNDR calculation. Referring the noise power to the input produced a noise power of $5.82\,\mathrm{nV}^2$. Using Equation 1.5, the calculated SNDR was:

$$SNDR_{SE} = 70.7\,\mathrm{dB} \tag{3.31}$$

From Equation 1.6, this translates to an ENOB of 11.4 bits.

3.4 Design of Fully Differential ADC With Ideal Components

Once the single-ended design was complete, it needed to be expanded to a differential design. Expanding to a differential design involved mirroring the sub-ADC capacitor arrays to enable a positive and negative input, as well as using the differential OTA model for the MDAC. In addition, to accommodate the differential design, the SAR control logic had to be slightly redesigned. The parameters for all of the design blocks and all of the capacitor sizes were able to remain the same, however. The differential design followed a similar design cycle as that of the single-ended design.

3.4.1 Expanding the SAR ADCs to Accept Differential Inputs

In order for the SAR ADC to accept a differential signal, the voltage reference had to be split into a positive reference voltage and a negative reference voltage. The relationship between these voltages is:

$$V_{refp} = V_{cm} + \frac{V_{ref}}{2} \tag{3.32}$$

$$V_{refn} = V_{cm} - \frac{V_{ref}}{2} \tag{3.33}$$

Figure 3.11 is an expansion of 2.1 to include differential inputs. While Figure 3.11 still uses the dummy LSB capacitor to achieve an extra bit of resolution, the resolution of the ADC has been lowered to two bits. The switches connecting the bottom plate of the sampling capacitors is now controlled by a new signal, G. At the end of the sampling phase, the G signal is asserted for all bits, and all other switches are open. Using an analysis similar to the analysis from Section 1.3.1, the expression for the comparator output at the end of the first conversion step is:

$$d_n = \begin{cases} 0 & \text{if } V_{inp} > V_{inn} \\ 1 & \text{if } V_{inp} < V_{inn} \end{cases} \tag{3.34}$$

Once again, the digital output of the ADC is the logical not of the comparator output. After the first conversion step, G_1 is deasserted, and the expression for the differential voltage at the comparator inputs is:

$$V_{diff,cin} = \begin{cases} (V_{inp} - V_{inn}) - \frac{V_{ref}}{2} & \text{if } d_1 = 1 \\ (V_{inp} - V_{inn}) + \frac{V_{ref}}{2} & \text{if } d_1 = 0 \end{cases} \tag{3.35}$$

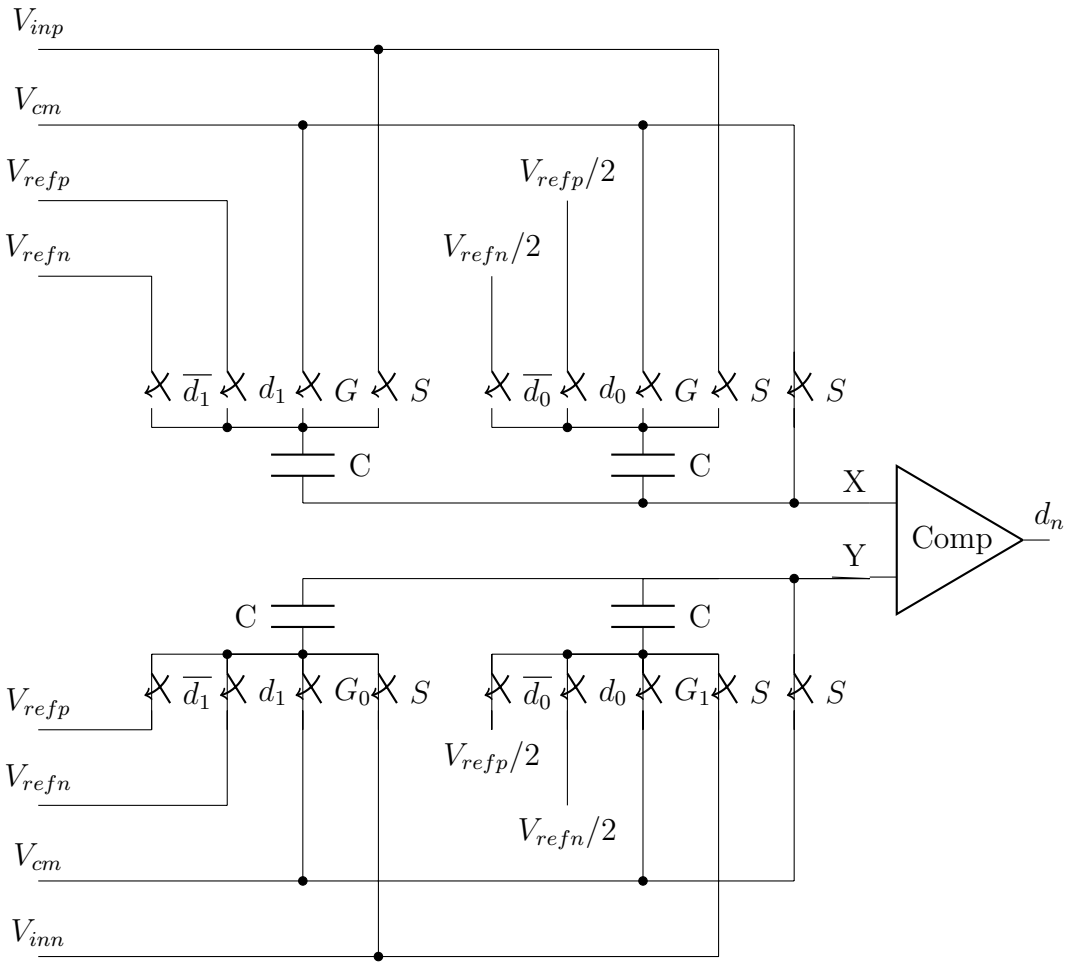

Figure 3.11: Example Two Bit Differential SAR ADC

The expression for the d_0 at the end of the second conversion stage is:

$$d_0 = \begin{cases} 1 & \text{if } V_{inp} - V_{inn} > \dfrac{\pm V_{ref}}{2} \\ 0 & \text{if } V_{inp} - V_{inn} < \dfrac{\pm V_{ref}}{2} \end{cases} \tag{3.36}$$

where V_{ref} is positive if d_1 is 1 and negative if d_1 is 0. Conversion could continue in this manner for an arbitrary number of stages.

3.4.2 Design of Differential Control Logic

The expansion to differential outputs necessitated two major changes in the SAR control logic. First, a new control signal has been added to control the switches connected to the common-mode input. These switches must stay asserted until after the corresponding bit decision stage. Additionally, the first decision stage of the differential ADC requires that only G_i signals be asserted, which is different than that of the single-ended stage. In addition to these required changes, some design issues that were encountered during the single-ended design phase needed to be addressed. The reason the additional clock cycle needed to be added to the second-stage ADC is that the state machine was being asynchronously reset by the rising edge of the sampling clock signal. This asynchronous behavior was removed during the design of the differential control logic. The state machine would now reset itself synchronously, so issues between the clock domains were removed and the second stage sampling clock frequency could be restored to 140 MHz. Also, flip-flops separate from the normal control logic were used to store the digital output codes, allowing for easier sampling of the digital data.

Table 3.19 shows the digital outputs, d_i, in terms of the differential SAR state machine. Table 3.20 shows the common-mode switch control output, G, in terms of the differential SAR state machine. The G_i, d_i, and $\overline{d_i}$, control signals must all be gated by the sampling clock of the sub-ADC, so that only the input sampling switch is closed during the sampling phase. The first and second stage control logic had only two differences. First the the second stage has an extra state to account for the extra conversion step required. Second, the sampling clock and the SAR conversion clocks for the two stages are different, although the internal behavior in response to these clocks is exactly the same. At the first falling edge of the SAR conversion clock, the state machine moves from state 6, or 7, to state 0 and conversion begins. Conversion ends when the state machine reaches state 6, or 7.

Current State	Next State	d_5	d_4	d_3	d_2	d_1	d_0
0	1	0	0	0	0	0	0
1	2	$\overline{C}$	0	0	0	0	0
2	3	d_{5p}	$\overline{C}$	0	0	0	0
3	4	d_{5p}	d_{4p}	$\overline{C}$	0	0	0
4	5	d_{5p}	d_{4p}	d_{3p}	$\overline{C}$	0	0
5	6	d_{5p}	d_{4p}	d_{3p}	d_{2p}	$\overline{C}$	0
6	7	d_{5p}	d_{4p}	d_{3p}	d_{2p}	d_{1p}	$\overline{C}$

Table 3.19: Differential ADC Digital Output State Machine

Current State	Next State	G_5	G_4	G_3	G_2	G_1	G_0
0	1	1	1	1	1	1	1
1	2	0	1	1	1	1	1
2	3	0	0	1	1	1	1
3	4	0	0	0	1	1	1
4	5	0	0	0	0	1	1
5	6	0	0	0	0	0	1
6	7	0	0	0	0	0	0

Table 3.20: Common-Mode Switch Control Output State Machine

3.4.3 Simulation Using Ideal OTA Model Parameters

Similar to the design of the single-ended ADC, ideal OTA model parameters were used in order to verify the SAR operation. This phase was much shorter than in the single-ended case, as almost all of the bugs that were found were in the control logic and fixing them was straightforward. The amplification phase had to be shortened by another 100 ps in order for the last bit decision to fully settle. This slight decrease in the amplification phase did not necessitate any change in the OTA transconductance. By the end of this phase, the SQDR was once again 74 dB.

3.4.4 Simulation with Calculated OTA Model Parameters

After obtaining an ideal SQDR with the ideal OTA model parameters, the design was put through the same battery of tests that the single-ended design was put through. Transient simulations ensured that distortion power did not negatively effect the ADC performance, and then noise simulations were performed to ensure that the output noise was within its budget.

The transient settling simulation was the same as in the single-ended case, except that an input with the maximum negative magnitude and the maximum positive magnitude was used to ensure that the settling was not affected by signal polarity. Figures 3.12 and 3.13 are the graphs of the transient settling with a full-scale positive input and full-scale negative input, respectively. In the case of the positive input, the settling error is $-1.7\,\mathrm{mV}$. In the

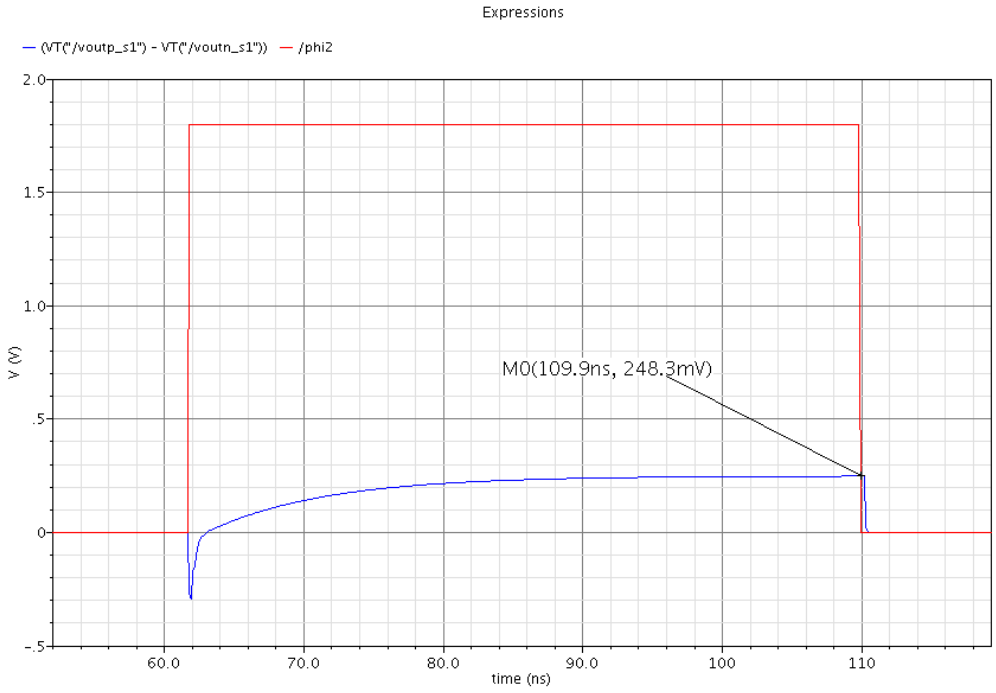

Figure 3.12: Transient Settling of Differential ADC With Ideal Components With Full-Scale Positive Input Voltage

case of the negative input, the transient settling error is $2.7\,\mathrm{mV}$. In both of these cases, the settling error is within the maximum settling error envelope.

After verifying that the MDAC was settling properly, the DFT simula-

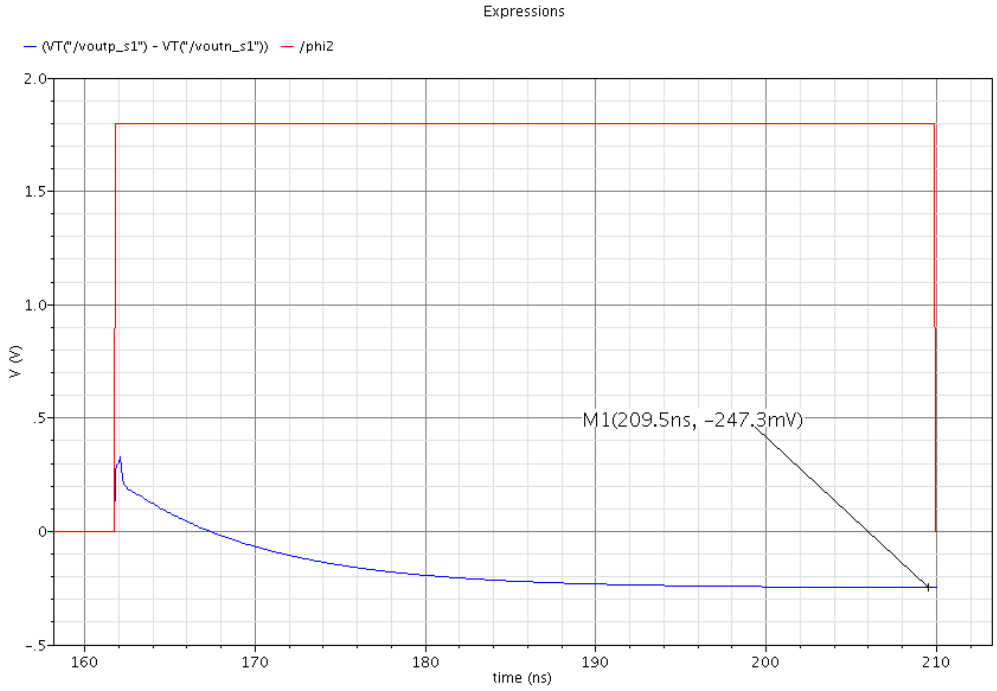

Figure 3.13: Transient Settling of Differential ADC With Ideal Components With Full-Scale Negative Input Voltage

tions were run. These simulations yielded an SQDR of 74 dB on the first run. Some additional runs were performed, however, to try to adjust the size of the sampling switches. In the case of the differential design, all switches were able to be sized with an on resistance of 500 Ω. Figure 3.14 shows the DFT results from the final run of the differential simulation.

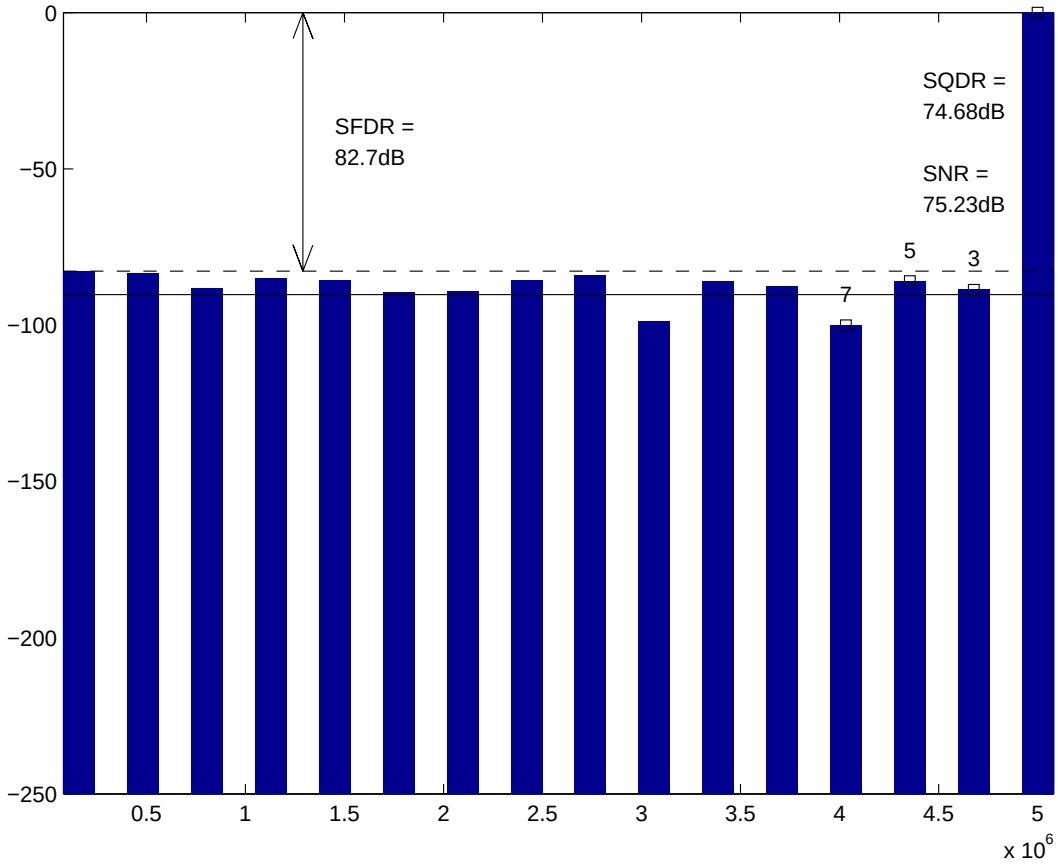

Figure 3.14: DFT of Differential ADC With Calculated Model Parameters

With the transient performance meeting specification, the final step in the verification of the differential design was the noise simulations. Graphs

of the simulation results from the AC noise simulations are given in Figures 3.15 and 3.16. Not surprisingly, the noise contribution from the sampling

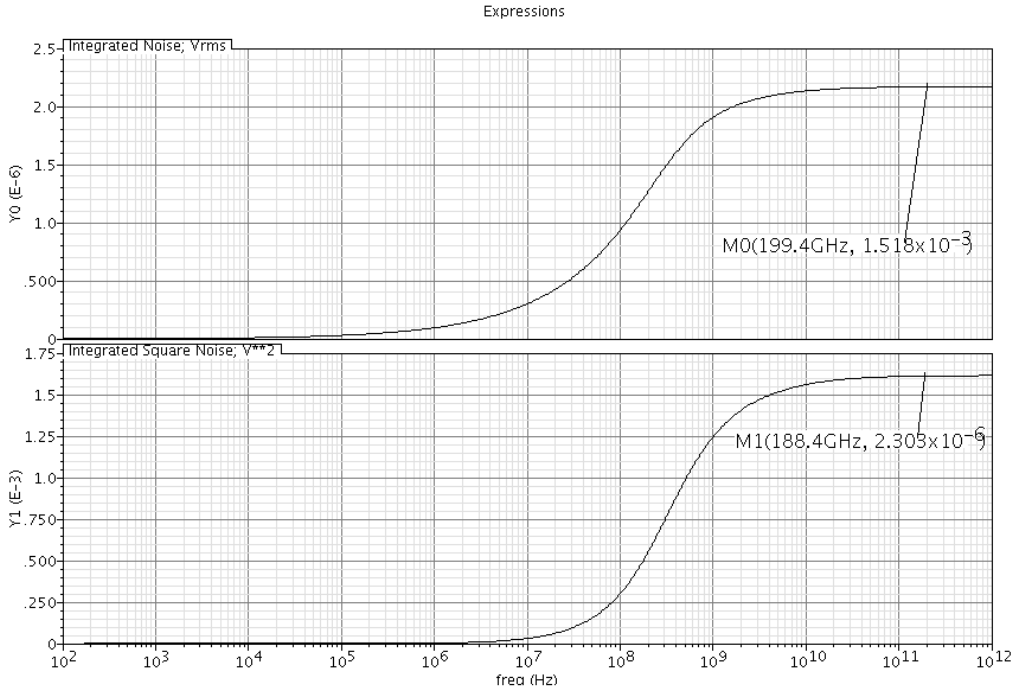

Figure 3.15: AC Noise During Sampling Phase of Differential ADC

phase has roughly doubled. This is due to the doubling of the capacitance from the differential design. The noise in the amplification phase does not exactly double because the OTA noise power is independent of the differential or single-ended implementation. The contribution to amplification phase noise power from the input switches and from the second stage capacitive array does double, however. Table 3.21 summarizes the results from the AC noise simulation. Once again, the hold noise calculations are off due to neglecting the contribution to noise power of the input switches. Despite this limitation,

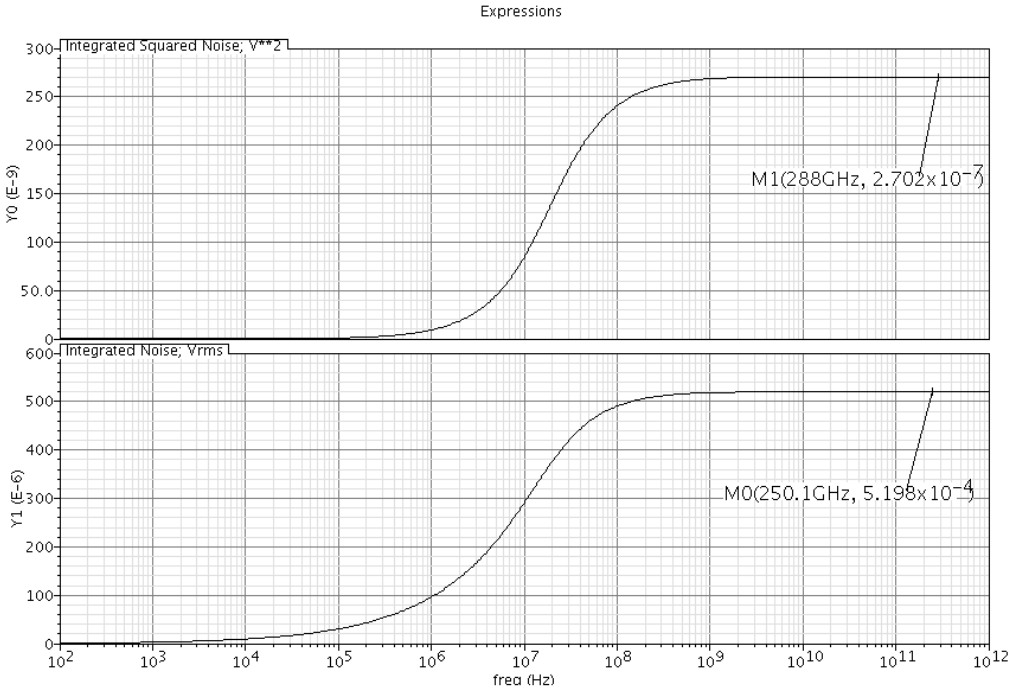

Figure 3.16: AC Noise During Amplification Phase of Differential ADC

Setup	AC Sampling Noise (mV_{rms})	Total AC Hold Noise (mV_{rms})	AC Hold OTA Noise (mV_{rms})	AC Total Noise (mV_{rms})
Simulation	1.52	0.52	0.32	1.60
Calculation	1.51	0.34	0.33	1.55
Design Target	1.51	1.62	1.51	2.21
Error (%)	0.31	53.79	-1.69	3.48
Headroom (%)	-0.26	67.82	78.66	27.55

Table 3.21: Differential AC Output Noise Summary

the noise power is still well within the budget. Figure 3.17 is the result of the PSS/PNOISE simulation with the differential ADC. The results from this

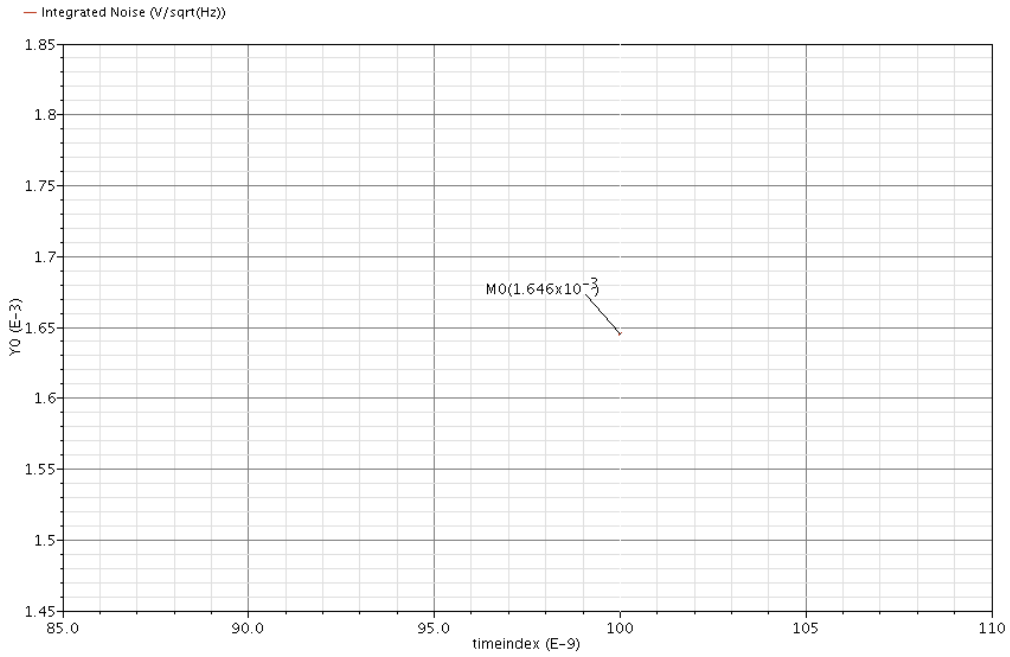

Figure 3.17: Differential PNOISE Simulation Result

simulation are compared with the noise calculations and the results from the AC noise simulation in Table 3.22. The differential PNOISE results agreed

Setup	Total Noise Power (mV_{rms})	Error vs Calculation (%)	Error vs AC Simulation (%)
PNOISE Simulations	1.65	6.21	2.64

Table 3.22: Differential PNOISE Output Noise Summary

closely with the calculated results and the AC noise simulations, so the noise simulations were considered successful.

As in the case of the single-ended design, an equivalent SNDR could now be calculated with the SQDR and noise power. The differential PNOISE noise power was used, as this was the largest simulated noise power. The calculated SNDR for the differential design was:

$$SNDR = 72.6\,\mathrm{dB} \tag{3.37}$$

From Equation 3.37, the ENOB is calculated to be 11.8 bits, which is better than the result from the single-ended design. With the differential ADC design performance meeting specification, the design could move on to the next phase, implementing transistor-level designs for the OTA.

Chapter 4

MDAC Design and Integration

After successfully simulating the design with ideal circuit blocks, the next step was to perform the transistor level design of the MDAC. The MDAC is one of the most important blocks in a pipelined ADC design. The accuracy of the closed-loop gain directly affects the accuracy of the downstream ADC. In addition, the overall power consumption and noise power is generally dominated by the contributions from the MDAC, so careful design of the MDAC is required in order to obtain high accuracy and low power consumption. From Section 1.2.2, the MDAC consists of an OTA along with a capacitive feedback network. Since the feedback network and OTA parameters had already been specified in Section 3.2, the main design task was to meet the required specifications using a transistor level design. This chapter will begin with a discussion of the chosen OTA architecture, as well as the main design knobs used to obtain the required OTA specifications. Next will be a high level overview of the biasing and CMFB networks used to obtain the OTA operating point. Following this is a discussion of the simulation methods used and some design challenges that had to be overcome after initial simulations. This chapter then moves on to a presentation of the simulation results of the OTA. Finally, the performance results of the full ADC with the OTA integrated are

presented and a final FOM of the design is calculated.

4.1 OTA Design

From Section, 3.2.2, in order to achieve the required static and dynamic errors, a loop gain of 48 dB and a loop crossover frequency of 22.1 MHz was required. The main factor driving the choice of OTA topology was the large gain required. The maximum gain in almost all OTA architectures is set by the intrinsic gain, g_m/g_{ds} or $g_m r_o$, of its transistors. In order to achieve an open-loop gain of 73 dB using a topology with a gain of approximately $(g_m r_o)^2$, an intrinsic gain of approximately 36 dB would be required. Assuming minimum channel length devices, intrinsic gains this large would not be achievable. If, however, a topology with a gain of approximately $(g_m r_o)^3$ was used, the required intrinsic gain drops to approximately 16. An intrinsic gain of 16 is attainable using minimum channel length devices, so the investigation was limited to topologies with a gain proportional to $(g_m r_o)^3$. Two topologies that fit this requirement are a triple cascoded topology and a two-stage topology with a cascoded first stage. In general, two stage designs require pole splitting to maintain stability, which causes the dominant pole to shift lower. These concerns are not present with cascoded designs, since the non-dominant pole is generally close to the transit frequency. This means that higher bandwidths are easier to obtain using a single triple cascoded stage. In addition, using a single stage generally consumes less power, since each stage requires its own bias current. The main reason why many designs do not use a

triple cascoded topology is their extremely limited output swing. For a triple cascoded differential topology, the output voltage range is approximately:

$$-(V_{dd} - 7V_{ov}) < V_{out} < (V_{dd} - 7V_{ov}) \tag{4.1}$$

where V_{ov} is the overdrive voltage of the transistors. For many low-voltage processes, this limitation prohibits the usage of this topology.

In this design the usage of the half-gain topology allows for the usage of the triple-cascode topology. The half-gain topology reduces the maximum output swing of the second stage to 1 V, assuming a comparator offset of 1/2 LSB. Using a 1.8 V supply and assuming an overdrive voltage of approximately 200 mV, the maximum output swing would be approximately 1.2 V, which is large enough to meet the needs for this design. This fact, along with the many advantages of using a single stage topology, drove the decision to use this architecture. The other major disadvantage of this architecture is the complex biasing required to maintain proper bias voltages on the five transistors in the stack, but since this would only mean more design effort, this did not affect the choice to use this architecture. Figure 4.1 shows a general triple cascode OTA. In this design, two equally sized tail transistors were used as the current source. The first had a fixed bias set by a current mirror, with value $V_{currmirr}$. The second had a variable bias used to set the output common-mode to its desired voltage. The output voltage from the CMFB network is denoted in this figure as V_{cmc}. The design of the biasing network and the CMFB network is covered in Sections 4.2 and 4.3. The following sections will discuss in more

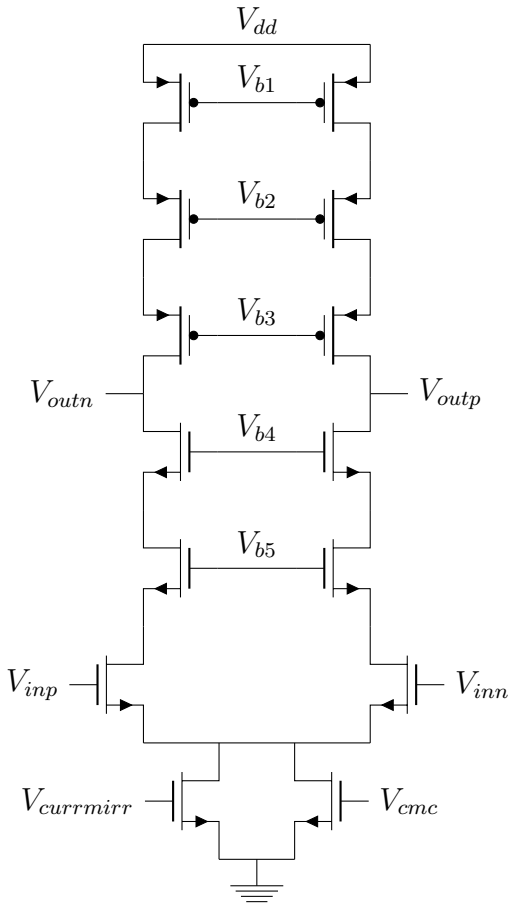

Figure 4.1: Triple Cascode OTA

detail the different performance parameters for the triple cascode topology, as well as their relationship to the main design knob, g_m/I_d.

4.1.1 Primary OTA Performance Goals

The three critical OTA design parameters were the loop gain, loop crossover frequency, and output noise power. If these specifications were not met, the ADC would not perform within its accuracy specifications.

4.1.1.1 OTA Loop Gain

From Equation 3.13, the factors controlling the loop gain of the OTA are the open-loop gain of the OTA and the OTA feedback factor. This section will derive expressions for each of these parameters in terms of device characteristics, and discuss their dependence on g_m/I_d.

The open-loop gain of the OTA is approximately equal to the product of its effective transconductance, G_m, and its output resistance, R_{out}. For the triple-cascode topology, the signal path consists of a common source transistor followed by two common gate transistors. Since the current gain of the common gate transistors is approximately one, the effective transconductance of this configuration is:

$$G_m = g_{m,CS} \tag{4.2}$$

where $g_{m,CS}$ is the transconductance of the common source transistor. Assuming that the g_m of all transistors is equal, a PMOS output resistance of r_{op}, and an NMOS output resistance of r_{on}, the approximate output resistance of

this configuration is:

$$R_{out} \approx (g_m^2 r_{on}^3)||(g_m^2 r_{op}^3) \tag{4.3}$$

The expression for the open-loop gain of this configuration is:

$$A_{OLDC} = G_m R_{out} \approx \frac{(g_m r_o)^3}{2} \tag{4.4}$$

where this expression assumes that the output resistance of the PMOS and NMOS transistors is approximately equal. From this equation, it can be seen that maximizing g_m/g_{ds} will also maximize the open-loop gain of the amplifier. Since g_{ds} is directly proportional to I_d, a larger g_m/I_d implies a higher g_m/g_{ds}, which means a larger gain.

Up until this point, a simplified model for the feedback factor has been used. This model only accounted for the effect of the MDAC feedback capacitor and first stage sampling capacitors on the feedback factor. A more accurate model incorporating the effect of the amplifier input capacitance, C_{in} is:

$$\beta = \frac{C_f}{C_f + C_{s1} + C_{in}} \tag{4.5}$$

The input capacitance of the amplifier is a function of the parasitic capacitance from the input NMOS transistor. An approximate expression for the input capacitance in terms of the input NMOS device parasitics is:

$$C_{in} = C_{gs} + 2C_{gd} \tag{4.6}$$

where C_{gs} is the gate to source capacitance and C_{gd} is the gate to drain capacitance. The factor of two applied to C_{gd} comes from the application of the

Miller approximation to a cascoded common source stage. From Equations 4.5 and 4.6, larger device parasitics will degrade the feedback factor. From Section 1.6, a larger g_m/I_d generally means larger device parasitics. From this the tradeoff between increased open-loop gain and decreased feedback factor can be seen. This tradeoff becomes even more important when the OTA loop crossover frequency.

4.1.1.2 OTA Loop Crossover Frequency

From Equation 3.24, the OTA loop crossover frequency is dependent upon the feedback factor, the OTA transconductance, and the total load capacitance. Up to this point, Equation 3.25 has been used when estimating the load capacitance. A more accurate equation for load capacitance that accounts for the parasitic capacitances from the PMOS and NMOS transistors connected to the output node is:

$$C_{l,tot} = C_{s2} + (1-\beta)\cdot C_f + C_{db,p} + C_{gd,p} + C_{db,n} + C_{gd,n} \tag{4.7}$$

where $C_{db,p}$ and $C_{db,n}$ are the drain to bulk capacitances for the PMOS and NMOS respectively, and $C_{gd,p}$ and $C_{gd,n}$ are the gate to drain capacitances for the PMOS and NMOS respectively. Here, again, larger g_m/I_d will cause larger device parasitics, which will limit the loop crossover frequency of the OTA. In order to achieve both the gain and crossover frequency goals, g_m/I_d of the load transistors must be carefully chosen to balance the tradeoffs between these two metrics. A degree of freedom is offered by the dependence of loop crossover

frequency on G_m, but care must be taken when using this knob as increased G_m also means increased power consumption.

4.1.1.3 OTA Noise

From Equation 3.27, the main factors in OTA output noise are the ratio of common gate transconductance to common source transconductance, and the ratio of the loop crossover frequency to the non-dominant pole frequency. Decreasing the common gate to common source transconductance ration implies using a small g_m, and thus a small g_m/I_d, in the common gate transistors. Due to headroom issues, this ratio had to be kept around 1, so it was decided that the transconductance ratio would not be a knob used to decrease the OTA output noise. Fortunately, more latitude was available in the ratio of the loop crossover frequency to non-dominant pole frequency. In addition to the dominant pole at the output node, there are two additional nodes on the signal path that contribute non-dominant poles. Assuming that all transistors on the signal path are sized equally, the capacitance at each node, C_x, will be:

$$C_x = C_{gd,n} + C_{gs,n} + C_{sb,n} + C_{db,n} \tag{4.8}$$

where $C_{sb,n}$ is the source to bulk capacitance of the NMOS transistor. The resistance, R_x at each of these nodes is essentially the input resistance of a common gate transistor, which is:

$$R_x = \frac{1}{g_m} \tag{4.9}$$

Using the expressions from Equations 4.8 and 4.9, the non-dominant pole frequencies, $\omega_{p2,3}$ are:

$$\omega_{p2,3} = \frac{g_m}{C_x} \tag{4.10}$$

The ratio between the loop crossover frequency and the non-dominant pole frequencies essentially simplifies to the ratio between the load capacitance and the non-dominant node capacitances. From the data in Table 3.12, even for very large g_m/I_d values the total gate capacitance only approaches 10% of the load capacitance. From this observation, the expected ratio between loop crossover frequency and non-dominant pole frequency could be expected to be much larger than the 3:1 ratio assumed in Section 3.2. Even if the expression from Equation 3.28 underestimated the actual design noise power, the expectation was that the noise power should not exceed the specified limits. For this reason, noise power was not given much consideration in the overall amplifier design. If necessary, the common gate transistors' g_m and ω_T could be tweaked once other design specifications were met, but the assumption that this likely would not be an issue was made.

4.1.2 Secondary Design Goals

Beyond the specifications required to meet the stated ADC performance specifications, some additional design parameters were accounted for in the design phase. Maximizing the output swing would allow for larger first-stage comparator offsets without compromising the accuracy of the ADC. Obtaining a phase margin larger than the minimum required 45° provides better

settling performance. Finally, the power consumption of the OTA is typically the dominant contributor to pipelined ADC power consumption, so reducing power consumption as much as possible was crucial to obtaining maximum ADC power effficiency. This section will provide an overview of the design parameters affecting these secondary design goals.

4.1.2.1 Output Swing

Output swing can be a fairly ambiguous term, for the purposes of this design the output swing is defined as the output voltage points where the open-loop gain degrades 30% from its peak value. In order for the ADC to meet its accuracy specifications, the absolute minimum output swing is 0.5 V. Having an output swing of only 0.5 V, however, constrains the maximum comparator offset to zero. In real comparator implementations, this constraint would be unrealistic. In order for the design to be able to take full advantage of the 1-bit redundancy, allowing for a maximum comparator offset of ½ LSB, the output swing of the OTA must be 1 V. Anything between these two values will constrain the comparator offset to below the value allowed for by the redundancy scheme. Using Equations 4.1 and 3.20 with a targeted output swing of 1 V and assuming that the g_m/I_d of all transistors is the same, the minimum g_m/I_d is:

$$(g_m/I_d)_{min} = \frac{28}{2 \cdot V_{dd} - 1} \tag{4.11}$$
$$= 10.8$$

In order to ensure maximum allowable comparator offset, the g_m/I_d was maintained above this value.

4.1.2.2 Phase Margin

The same concerns from Section 4.1.1.3 apply to phase margin, since the ratio between the loop crossover frequency and the non-dominant pole frequencies determine the phase margin. From the analysis in the OTA noise section, phase margin was expected to be well above the 3:1 value needed to obtain the desired settling behavior, so this design criteria was largely ignored in the design phase. In the case of loop gain simulations that showed instability, the size of the common-gate transistors could be reduced in order to reduce capacitance at the non-output nodes.

4.1.2.3 Power Consumption

The OTA power consumption is dependent on the supply voltage and the bias current. Assuming a fixed supply voltage of 1.8 V, minimizing bias current is the only knob to reduce power consumption. Required bias current is a function of both the g_m/I_d and the g_m of the design. Larger g_m/I_d means that for a given transconductance, the bias current will be lower. Larger g_m/I_d also implies a lowered ω_T, however, which implies a larger required transconductance in order to meet bandwidth requirements. Some design iteration is generally required to find the optimal combination of g_m/I_d and g_m to minimize power consumption.

4.1.3 Initial Design Parameters

After analyzing all the design goals and their various tradeoffs, an initial design could be specified. A Matlab script was created in order to calculate the bias current and transistor widths required to meet the OTA specifications. The only constraint given to this script was the design g_m/I_d. In this way, various g_m/I_d values could be specified and its effect on different transistor parameters could be observed. A limitation of this script was that it assumed the g_m/I_d of all design transistors was the same, but for the purposes of a first pass design this limitation was deemed acceptable. The purpose of this design script was a) to obtain a solution that was close to optimal, and b) to use the knowledge gained from the analysis of the design to make small manual changes to the transistor parameters, and then re-simulate. After some experimentation, a g_m/I_d of 15 was settled upon for the transistors. A summary of the major design parameters, along with some estimated performance parameters, is given in Table 4.1. With these base design specifications, the only tasks left before running simulations were designing the bias network and the CMFB network.

4.2 Bias Network Design

A carefully designed bias network was crucial to ensure maximum output swing and acceptable common-mode rejection. In order to maximize output swing, the bias network had to ensure that the bias voltage on each of the non-input transistors would produce a V_{DS} that was on the edge of saturation.

Parameter	Value
g_m/I_d	$15\,\mathrm{V}^{-1}$
V_{ov}	$0.13\,\mathrm{V}$
g_m	$3.41\,\mathrm{mS}$
I_{total}	$454\,\mu\mathrm{A}$
W_{PMOS}	$124\,\mu\mathrm{m}$
W_{NMOS}	$24.2\,\mu\mathrm{m}$
$(g_m/g_{ds})_{PMOS}$	42.2
$(g_m/g_{ds})_{NMOS}$	37.9
$f_{t,PMOS}$	$5.73\,\mathrm{GHz}$
$f_{t,NMOS}$	$16.2\,\mathrm{GHz}$
A_{oldc}	$90\,\mathrm{dB}$
Loop gain	$65\,\mathrm{dB}$
f_c	$23\,\mathrm{MHz}$
Phase Margin	89.9°

Table 4.1: Initial OTA Design Parameters

A poorly designed bias network could obtain the required performance specifications while significantly degrading the output swing of the OTA. In order to maximize common-mode rejection, the tail current mirror had to be designed properly. This section discusses the design of both the non-input transistor bias and the tail current mirror.

4.2.1 Biasing Cascoded Transistors

Special design techniques are required to ensure that the bias voltages of the transistors produce a V_{DS} on the edge of saturation. Figure 4.2 illustrates how the biasing network can ensure that the V_{DS} of each transistor in the cascode stack is on the edge of saturation. For the purposes of this example,

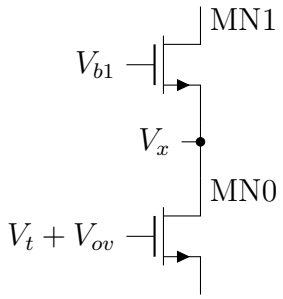

Figure 4.2: Simplified Cascode Stack

the desired overdrive voltage on both MN0 and MN1 is assumed to be equal to V_{ov}. The minimum voltage at V_x for MN0 to remain in saturation is:

$$V_{x,min} = V_{ov} \tag{4.12}$$

In order for the overdrive voltage of transistor MN1 to be V_{ov}, V_x must be:

$$V_x = V_{b1} - V_{ov} \tag{4.13}$$

In order to bias MN1 to the desired overdrive voltage, while also maintaining the minimum voltage at V_x, V_{b1} must be:

$$V_{b1,min} = V_t + 2V_{ov} \tag{4.14}$$

Any value of V_{b1} larger than this will result in a non-optimal output swing. A similar analysis could be performed on a three transistor stack to show that the optimal bias voltage for the third transistor is $V_t + 3V_{ov}$. A number of circuit implementations that meet the requirements of Equation 4.14 are covered in [6]. From these, an implementation using a diode-connected transistor in series with a triode transistor was chosen. Figure 4.3 illustrates this configuration.

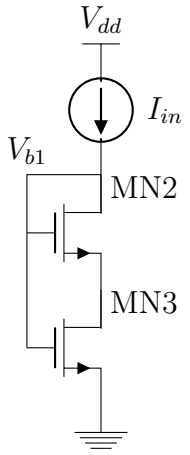

Figure 4.3: High Swing Bias Configuration

MN2 operates in the saturation region and MN3 operates in the triode region. From the figure, the value of V_{b1} is equal to the gate to source voltage of MN3. The current through both MN2 and MN3 is equal to I_{in}, so the expression for the current in terms of the transistor parameters for MN2 and MN3 is:

$$\frac{k'}{2}\left(\frac{W}{L}\right)_2 (V_{gs2} - V_t)^2 = \frac{k'}{2}\left(\frac{W}{L}\right)_3 \left(2(V_{gs3} - V_t)V_{ds3} - V_{ds3}^2\right) \tag{4.15}$$

In order to satisfy Equation 4.14, the drain to source voltage of MN3 must be:

$$V_{ds3} = V_{ov} \tag{4.16}$$

when

$$V_{gs2} = V_t + V_{ov} \tag{4.17}$$

If these conditions holsd true, the expression for V_{b1} will be:

$$\begin{aligned} V_{b1} &= V_{gs3} \\ &= V_{gs2} + V_{ds3} \\ &= V_t + 2V_{ov} \end{aligned} \tag{4.18}$$

This expression matches that from Equation 4.14. Using Equations 4.15, 4.16, 4.17, and 4.18, and solving for the relationships between the aspect ratios of MN2 and MN3:

$$\left(\frac{W}{L}\right)_3 = \frac{1}{3}\left(\frac{W}{L}\right)_2 \tag{4.19}$$

Using the biasing circuit from Figure 4.3 the full triple-cascoded biasing circuit could be designed. For the third transistor in the cascode stack, a gate voltage of $V_t + 3V_{ov}$ is desired. Following a similar analysis as in the derivation for the second transistor biasing, the ratio of MN2 to MN3 aspect ratio is 8:1. An important note is that in order to increase the bias voltage, the ratio of MN2 to MN3 aspect ratio must be increased. These results were used to design the full bias circuit shown in Figure 4.4. V_{b4} and V_{b5} correspond to the bias voltage connections in Figure 4.1. The addition of MN3 is necessary in order to maintain the same V_{ds} values for MN5 and the second cascode transistor in the triple cascode topology. Maintaining equal V_{ds} values for these transistors removes systematic gain error of the current mirror [6]. A very similar topology was used to bias the PMOS transistors, with an additional transistor stack to bias the PMOS transistor closest to the power supply.

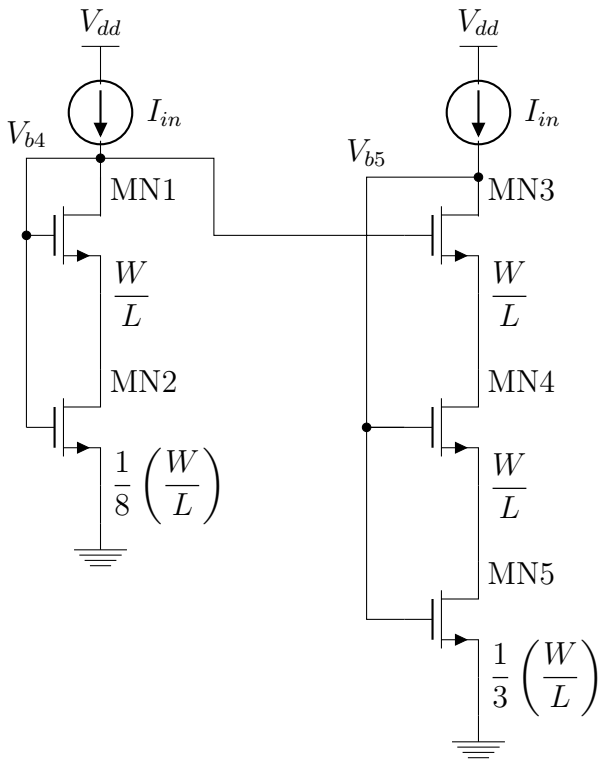

Figure 4.4: Full Cascode Bias Circuit

4.2.2 Tail Current Source Design

Designing a tail current source with high output resistance is important in obtaining high common-mode rejection for the OTA. In an effort to maximize the output resistance, many designs use a cascoded current mirror rather than a simple single transistor mirror. However this option did not seem feasible for this design due to the already limited output swing caused by the triple cascode topology. In an effort to increase the output resistance, a non-minimum channel length of 360 nm was used for the tail transistor. In addition, the g_m/I_d was kept high in order to both maintain a large output resistance and to minimize the effect on output swing from the tail transistor.

4.3 Common-Mode Feedback Design

For differential designs, the operating output voltage is very sensitive to small changes in device characteristics [14]. Small changes in the bias voltage can cause very large changes in the operating output voltage. In order to control these variations, common-mode feedback is employed. Common-mode feedback applies a variable amount of bias current in order to correct for excursions from the ideal output common-mode voltage. In order to achieve this, circuits are required to sense the common-mode voltage, to compare this sensed voltage to the desired common-mode voltage, and to apply a variable amount of current based on the difference between actual output common-mode and desired commmon-mode. For the purposes of initial design simulations, an ideal CMFB network was used to ensure that the base OTA design worked by

itself. In later design stages, a real CMFB implementation was implemented and tested. The following sections discusses both the ideal and real CMFB implementations.

4.3.1 Ideal CMFB

Figure 4.5 illustrates the schematic for the ideal CMFB network. V_{op}

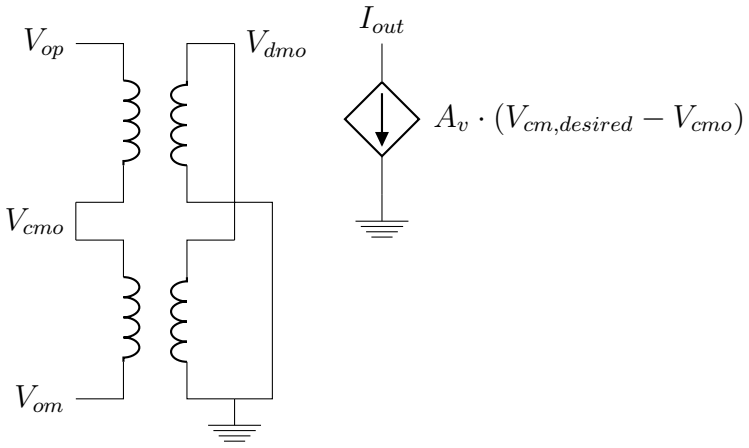

Figure 4.5: Ideal CMFB

and V_{om} are the positive and negative output voltages, respectively. An ideal balun is used as the sensing element to separate the common-mode, V_{cmo}, and differential-mode, V_{dmo}, voltages from the output signal. The transistor with variable bias in Figure 4.1 is replaced with the voltage controlled current source in Figure 4.5. This current source performs both the comparison as well as current application functions described earlier. When the gain of the controlled source, A_v, is set to be very large, the output common-mode voltage will be very close to the desired common-mode voltage, which is the desired

operation of the CMFB network.

4.3.2 Real CMFB Design

After performing simulation with the ideal CMFB and ensuring that all of the desired OTA specifications were met, a real CMFB implementation had to be designed. The simplest method to sense the output common-mode voltage is to use a resistive divider. The issue with using resistors on the output is that they have to be very large to not destroy the differential gain of the amplifier. This issue can be overcome by buffering the output with source followers, but this causes headroom issues. A simpler solution to the sensing problem is to use purely capacitive sensing. Once the sensing implementation had been decided on, the next step was to decide on the implementation of the comparison and variable current output functions. Many solutions use a similar idea as that used in the ideal CMFB case, by using a voltage controlled current source with high transconductance and applying the output current to the tail of the OTA. This function can be implemented using standard differential transsistor amplification techniques, since MOSFETs in saturation act as voltage controlled current sources. The downside to applying this strategy is the additional bias current required to implement an additional differential amplifier. This additional bias current can be a large percentage of the current used to bias the main OTA circuit.

Alternative implementations were investigated since power efficiency was a primary goal in this design. Since this OTA is only required to be

active during the second clock phase, a passive CMFB implementation could be used [14]. This implementation still requires additional bias current, but in general the additional current is smaller than in other implementations. Figure 4.6 shows a general model for the passive CMFB network. In the ϕ_1

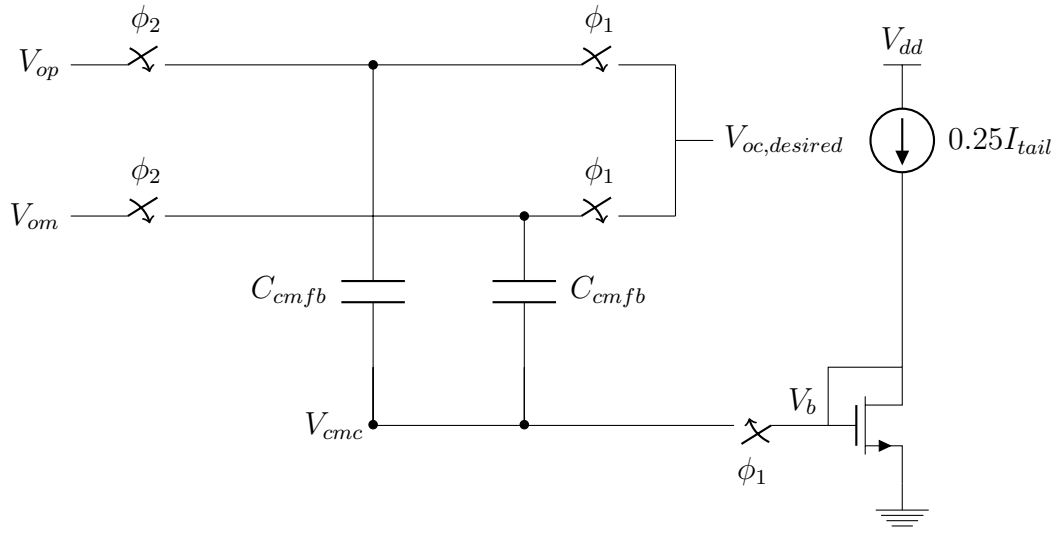

Figure 4.6: Real CMFB Implementation

clock phase, the voltage across the feedback capacitors, V_{Ccmfb} is charged to:

$$V_{Ccmfb} = V_{oc,desired} - V_b \tag{4.20}$$

This charging phase is the reason why the OTA cannot be active during ϕ_1. Once the OTA enters its active phase, ϕ_2, the feedback network will be activated. In this configuration, if the output common-mode is larger than the desired output common-mode, V_{cmc} will become larger than V_b, which will cause more current to flow through the transistor tail. This additional current will cause the common mode output decrease. The opposite effect occurs if the

output common-mode is smaller than the desired output common-mode. The transistor that sets V_b is sized to be half of the tail transistor that it controls in order to allow for the bias current to be $1/4$ of the total bias current. An optimization applied to this design was the removal of the additional bias current and bias transistor. Since an appropriate V_b was already being generated from the tail current mirror, the output bias voltage from the current mirror could be applied to the CMFB as well. This removed the need for any additional bias current to be applied to the CMFB network.

Another design consideration is the sizing of the feedback capacitors. These must be sized large enough so that the bandwidth of the common-mode feedback is not so large as to cause instability, but also not too large that the feedback network cannot respond quickly enough to changes in the output common-mode. A good rule of thumb is to make the common-mode feedback bandwidth about 30% of the differential bandwidth. Assuming that the circuit has approximately 10 time constants to settle, this allows 3 time constants for the CMFB voltage to settle, which can remove approximately 95% of common-mode disturbance [14].

4.4 OTA Test Setup

In order to ensure that the OTA met its specifications, a number of different simulations had to be run. This section gives a brief overview of the different test setups used to obtain different device parameters. Once all of these simulations produced adequate results, the same simulation as outlined

in Section 3.3.2 were run on the entire ADC with the real OTA model instead of the ideal one.

4.4.1 Loop Gain, Loop Crossover Frequency, Phase Margin, and Power Consumption Simulation

A typical method for simulating the loop gain and loop crossover frequency is simulating the OTA in its open loop configuration. The requirements for the open-loop gain can be derived from the loop gain requirements, as done in Equation 3.16. Similarly, the desired open-loop unity gain frequency can be estimated by dividing the desired loop crossover frequency by the feedback factor, β. The limitation of simulating with this technique is that it does not take into account the effect of the feedback network on the OTA performance. The feedback capacitor adds additional capacitance at the load, which means open-loop simulations will overestimate the true loop crossover frequency. The additional capacitance can be calculated accurately and added to the load capacitance, so this is not typically an issue in open loop simulations. An issue that is not as easily solved is the degradation of the feedback factor due to the input capacitance of the OTA. Open loop simulations cannot account for this effect, which means that both the loop gain and loop crossover frequency will be overestimated.

Fortunately, the simulator used in this design offered a method for simulating the performance of the OTA with the feedback network implemented. In order to perform this simulation a special probe was placed in

order to break the feedback loop. A special simulation, called an *stb* simulation was performed, which can give information on both the common-mode and differential-mode loop gain and loop crossover frequencies. In addition, this simulation provides the phase margin for the circuit. As a side effect of this simulation, if an operating point is saved, the power consumption of the OTA can also be measured. Unfortunately, the version of the tool used for this design did not have a periodic version of the *stb* analysis available, so these simulations could only be performed on the OTA with ideal CMFB network. Transient simulation were used to validate the settling behavior of the OTA with real CMFB as well as the settling of the output common-mode voltage.

4.4.2 Output Swing Simulation

In order to simulate the output swing, a DC simulation was performed. In this case, the open-loop configuration was used for the OTA. Input DC values were applied that would cause the output voltage to vary across the entire desired differential output swing. The negative and positive output voltages which caused a 30% decrease in the open-loop gain were recorded, and the difference between these two values were considered to be the output swing.

4.4.3 OTA Noise

Before performing the noise simulations on the entire design, the noise contribution from just the OTA was simulated. A similar setup as that in

Section 4.4.1 was used, where the OTA was placed in its final feedback configuration, and the output AC noise was simulated. This setup is very similar to that of the AC hold noise simulation described in Section 3.3.2.3, except that the switches were not included in this setup. As long as the OTA noise was within the maximum value allowed for in Table 3.10, it was very likely that the overall ADC would meet its noise specifications.

4.5 OTA Design Challenges

After calculating initial design parameters that were expected to meet the specifications, designing the bias network and the CMFB network, and determining the necessary simulations to checkout the design, initial simulations could be run. A number of issues were found in the initial simulations that had to be corrected before obtaining an acceptable result. This section will outline some of the challenges that were encountered and the methods used to overcome them in order to obtain an acceptable design.

The initial loop gain simulation produced a gain significantly below that estimated by the g_m/I_d models. After some investigation, it was discovered that the values for g_m/g_{ds} and ω_T that were estimated by the original g_m/I_d simulations were much higher than the measured results from the simulation. This inaccuracy was due to the dependence of these design parameters on the transistor V_{ds}. When creating the device models, the simulations were performed using a constant V_{ds} of 900 mV, with the assumption that the design parameters would not change very much with variation in V_{ds}. While this

holds true across a wide V_{ds} range, this independence no longer holds with very small values of V_{ds}, which was the case with the biasing for this design. After coming to this realization, some additional characterization simulations were performed on the simple NMOS testbench to determine the minimum V_{ds} required to obtain a ω_T and g_m/g_{ds} close to that estimated from the models. Figure 4.7 shows the dependence on V_{ds} of g_m/g_{ds} and Figure 4.8 shows the dependence on V_{ds} of ω_T. From these graphs, it was decided that the

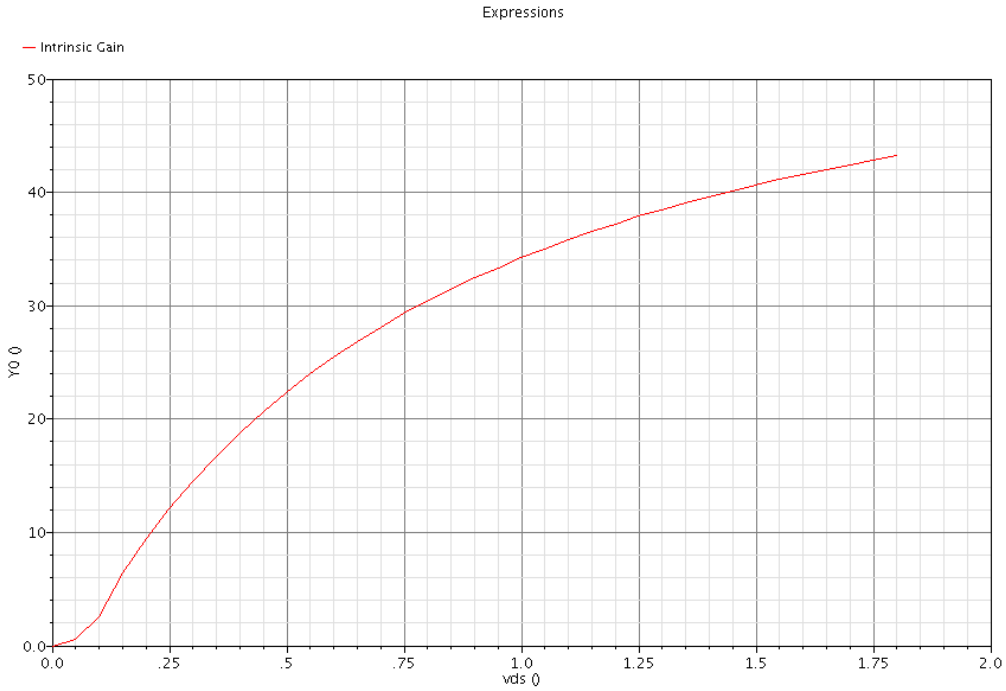

Figure 4.7: g_m/g_{ds} Dependence on V_{ds}

minimum V_{ds} required to obtain results close to the estimated results, while mainataining a reasonable output swing, was 200 mV. In order to achieve this larger transistor drain to source voltage, the method used in Section 4.2.1 was

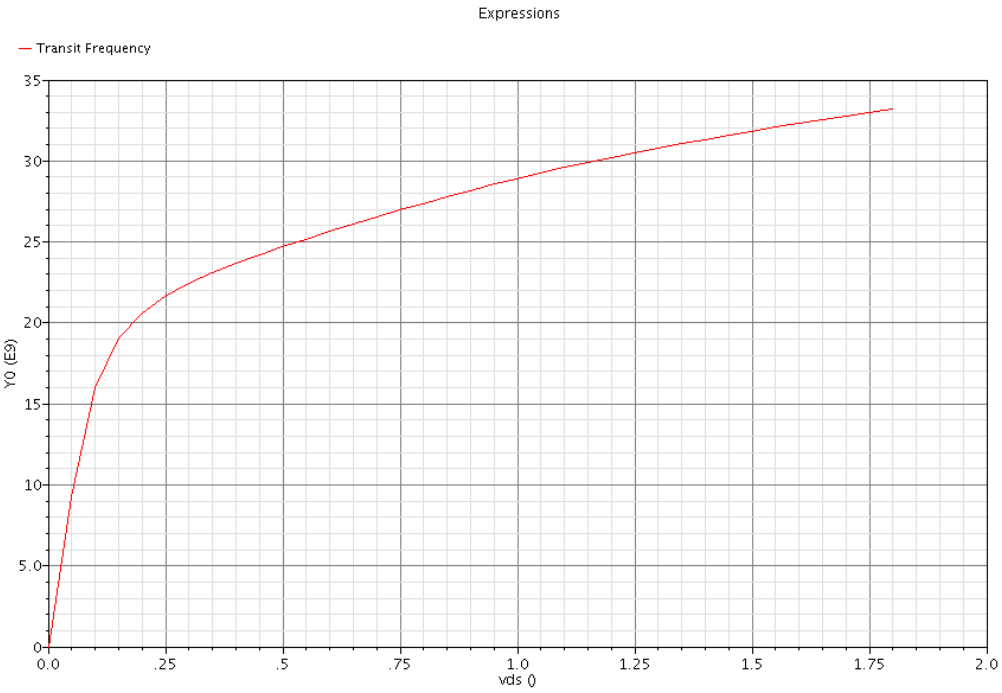

Figure 4.8: ω_T Dependence on V_{ds}

used, to decrease the aspect ratio of the triode transistor. Once all of the transistor V_{ds} voltages were raised to this value, the design parameters began to more closely resemble the calculated models.

Although increasing the V_{ds} on the transistors did increase the gain significantly, this change was not enough for the design to meet the loop gain requirements. In order to increase the gain, the g_m/I_d of the transistors was increased to 20. After making this change, the loop gain specification was met, but the loop crossover frequency was only about 16 MHz, well below the specified requirements. From Equation 4.7, the crossover frequency is only dependent on the parasitics at the load node. In examining the capacitances at the load, it was noticed that the load capacitance contribution from the PMOS was much larger than that from the NMOS. Based on this observation, the width of the load PMOS was reduced in an effort to decrease the load capacitance. A reduction in transistor width while maintaining the same bias current results in a decrease in the transistor g_m/I_d . In the case of the PMOS load, a reduction in g_m/I_d to $15\,\mathrm{V}^{-1}$ was observed. While this modification did increase the crossover frequency of the OTA, it was still not high enough to meet specifications. Further reductions in the load g_m/I_d had little effect on the crossover frequency and caused sharp drops in gain, so the g_m/I_d was not modified any further. In order to meet the required crossover frequency, the g_m of all transistors was increased to 4.8 mS. After this modification, the loop crossover frequency met specification. In retrospect, a much better knob to use would have been the g_m/I_d of the input NMOS transistor. Although

the parasitics from the load transistors do reduce the crossover frequency, they are still a small percentage of the second stage sampling capacitance, which dominates the load capacitance. The size of the feedback capacitor is on the same order as the input parasitics, so changes in the input parasitics can have a much larger effect on the feedback factor of the OTA. Unfortunately, this realization was not made until after the design had already been checked out. This optimization will be assessed in future modifications to the OTA.

After overcoming these two major design challenges, the OTA was meeting the loop gain and loop crossover frequency specifications. Further simulations showed that the noise specification was also being met, so the rest of the simulations described in Section 4.4 were performed in order to fully characterize the OTA. The following section will present the results from all of these simulations.

4.6 OTA Simulation Results

This section summarizes the simulation results from the OTA tests described in 4.4. These results include those from the *stb* analysis, the DC output swing analysis, the AC noise simulation, and the transient simulation used to verify the CMFB network operation. This section will conclude with an overview of device parameters and performance results.

4.6.1 STB Results

The *stb* analysis allowed for loop gain and phase measurements while taking into account the effect of the feedback network on the OTA. Figure 4.9 shows the results from this analysis. From this graph, the final loop gain is

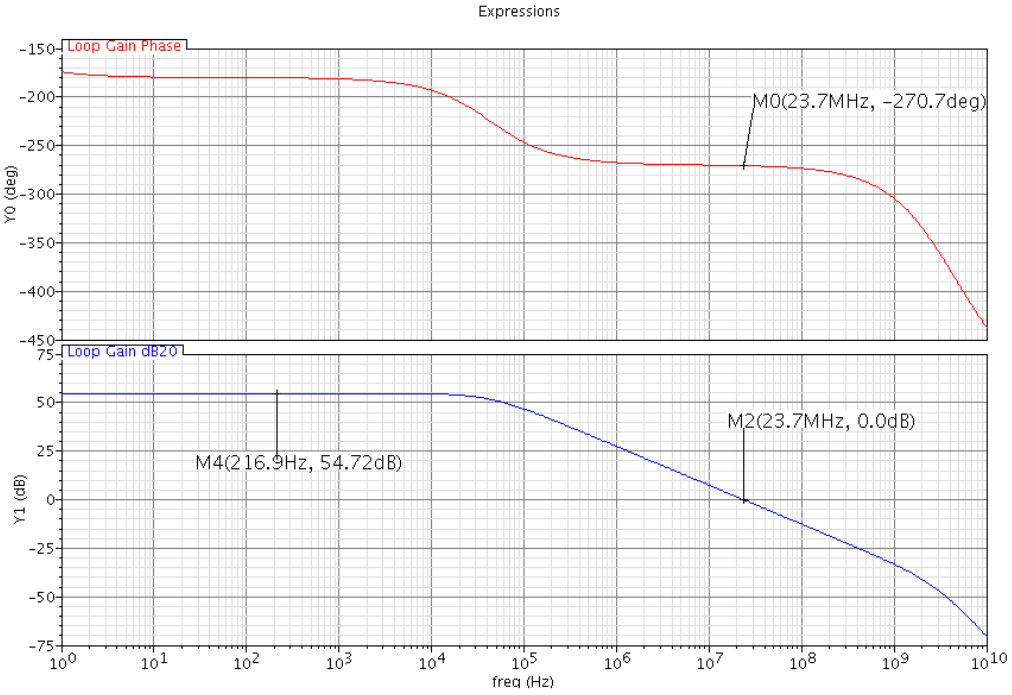

Figure 4.9: STB Analysis Results

54.7 dB and the loop crossover frequency is 23.7 MHz. In addition, the phase margin is 89.3°. All of these values are above their specified values.

4.6.2 Output Swing

Figure 4.10 shows the results from the output swing simulations. The peak open-loop gain is 4590. A reduction of 30% of this value is a gain of 3213.

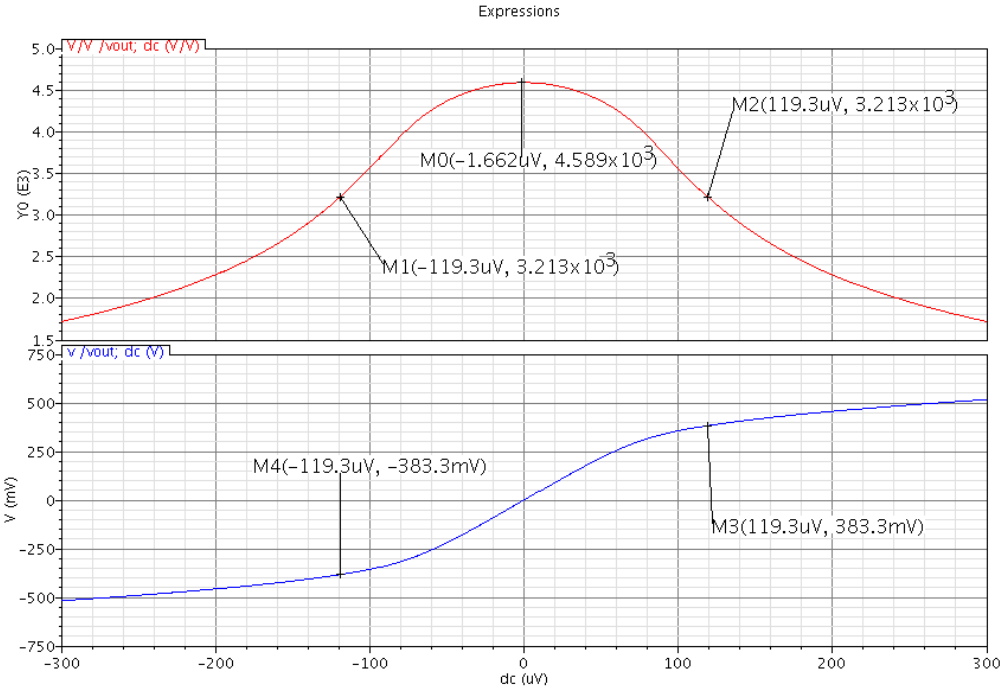

Figure 4.10: DC Output Swing Results

The output voltage values at which the gain reaches 3213 are −383.3 mV and 383.3 mV. This results in a total output swing of 766.6 mV. This value is below the targeted output swing of 1 V. An output swing of this value allows for approximately 1/4 LSB of comparator offset. It was decided that with careful comparator design this tighter constraint could be met, so the output swing was deemed acceptable.

4.6.3 OTA Noise

Figure 4.11 shows the results from the OTA AC noise simulations. The

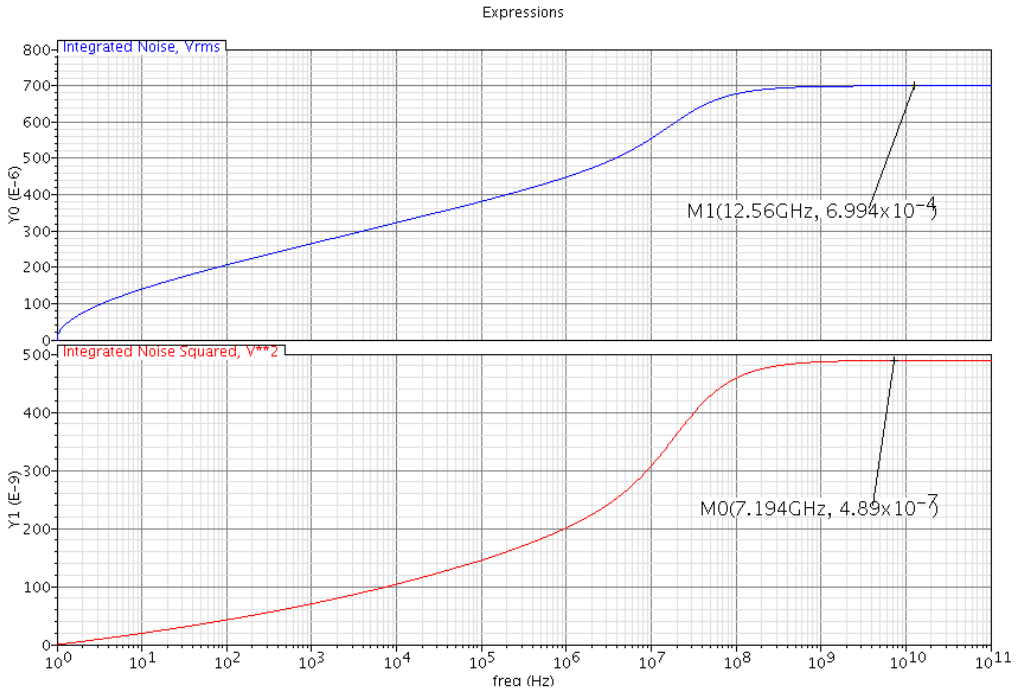

Figure 4.11: AC Noise Results

measured OTA output noise of 699 μV_{rms} is still well below the maximum

$1.5\,\mathrm{mV_{rms}}$ allowed for in Table 3.10. This value is, however, well above the expected value calculated from 3.27. This is likely because the additional common-gate transistor causes much larger noise voltage on the output than allowed for by this equation. A better estimate would include the effects of the additional cascode stage and the additional gain it contributes to the common-source noise contribution. This calculation was not updated since the output noise was well within its limits.

4.6.4 Real CMFB Transient Simulation

In order to validate the operation of the passive CMFB network, a transiet simulation was performed. This transient simulation applied a sinusoidal input to the OTA and the output common-mode voltage was observed. Figure 4.12 shows the output common-mode voltage measurements. The deviations from the desired common-mode voltage observed occur during the ϕ_1 clock phase and are the reason the OTA can only be active in the ϕ_2 phase. While the OTA is in its active phase, the output common-mode agrees well with the desired common-mode voltage of 1 V.

4.6.5 Summary of OTA Simulation Results

The measurements presented here show that the OTA achieved the performance desired for the ADC to achieve its performance specifications. Table 4.2 summarizes the important design parameters, as well as the simulation results. Note that an additional transistor parameters had to be added to rep-

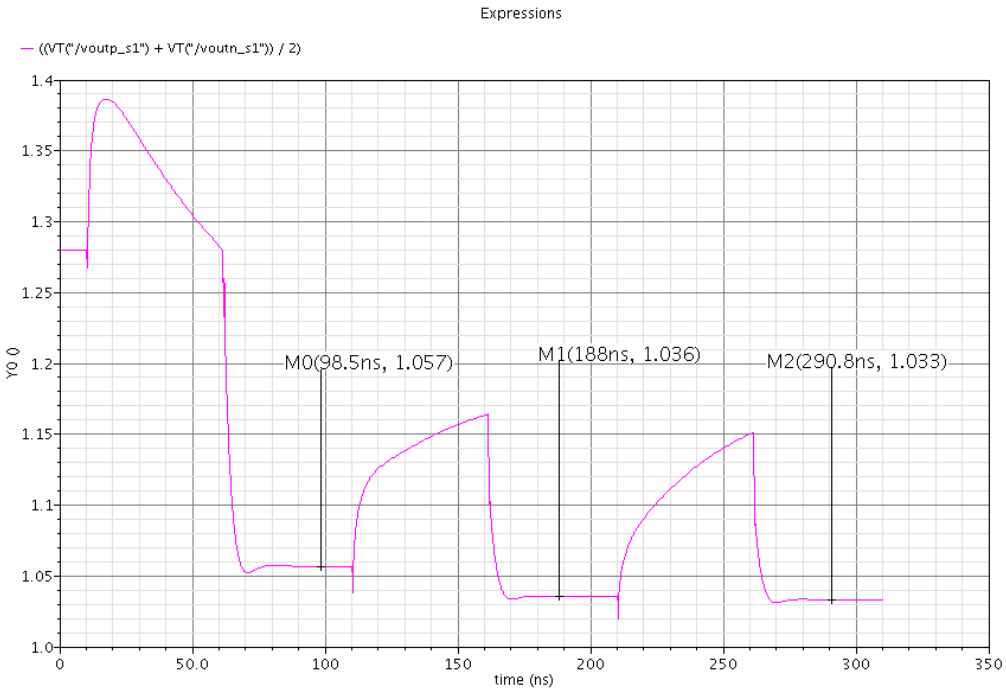

Figure 4.12: Output Common-Mode Voltage Transient Simulation Results

resent the PMOS load with different g_m/I_d. Note also that I_{total} is the total current used by the OTA, including additional current for the biasing circuits.

Parameter	Value
g_m/I_d	$20\,\mathrm{V}^{-1}$
$(g_m/I_d)_{PMOS,load}$	$15\,\mathrm{V}^{-1}$
g_m	4.8 mS
I_d	694 µA
W_{PMOS}	280.7 µm
$W_{PMOS,load}$	81.5 µm
W_{NMOS}	92.5 µm
Loop gain	54.7 dB
f_c	23.7 MHz
Phase Margin	89.3°
Power	1.25 mW
Noise	$699\,\mu\mathrm{V}_{\mathrm{rms}}$

Table 4.2: Final OTA Design Parameters and Results

4.7 ADC Simulation Results With Integrated OTA

Once the OTA performance was deemed acceptable, the next step was to perform the simulations outlined in Section 3.3.2 on the differential ADC design with the transistor-level OTA model in place of the ideal OTA model. This section provides a summary of these results.

The first check for the ADC was a transient settling test. Since the performance of the OTA directly impacts the settling performance of the output to the second stage, ensuring that this test met its requirements was a very

important step in verifying the OTA integration. Figures 4.13 and 4.14 show the results from the transient simulation. In the case of the positive input,

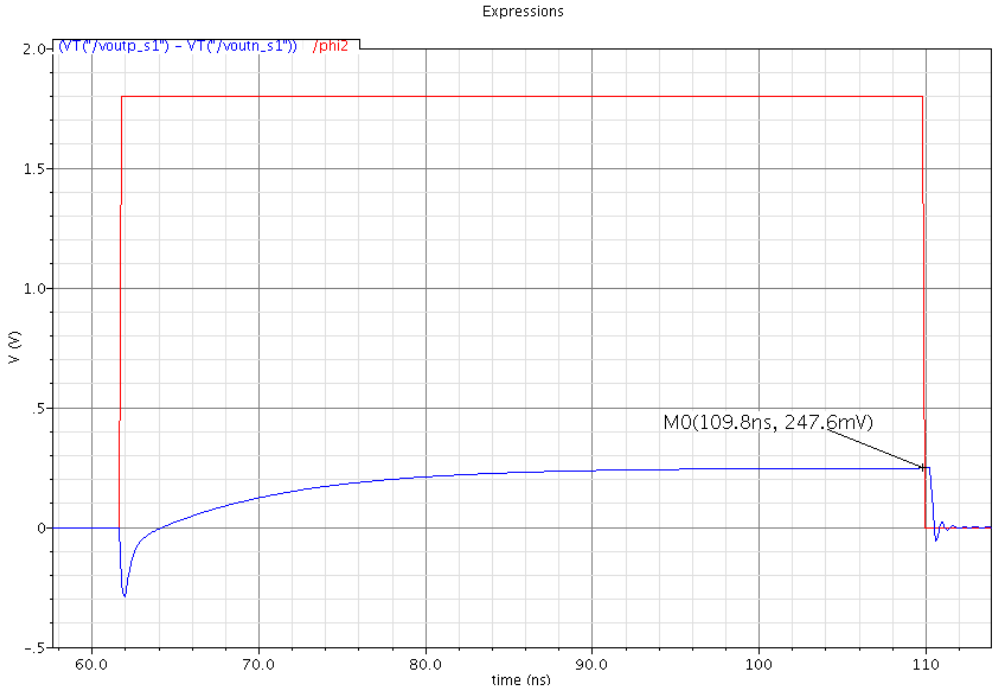

Figure 4.13: Transient Settling of ADC With Real OTA Design With Full-Scale Positive Input Voltage

the settling error is $-2.4\,\text{mV}$. In the case of the negative input, the transient settling error is $2.9\,\text{mV}$. In both of these cases, the settling error is within the maximum settling error envelope.

Next, the full DFT simulation could be performed to measure the SQDR of the ADC. Figure 4.15 shows the results from this simulation. The obtained SQDR was $73.4\,\text{dB}$, a slight degradation from the ideal simulations. This degradation is expected, however, since simulations involving real tran-

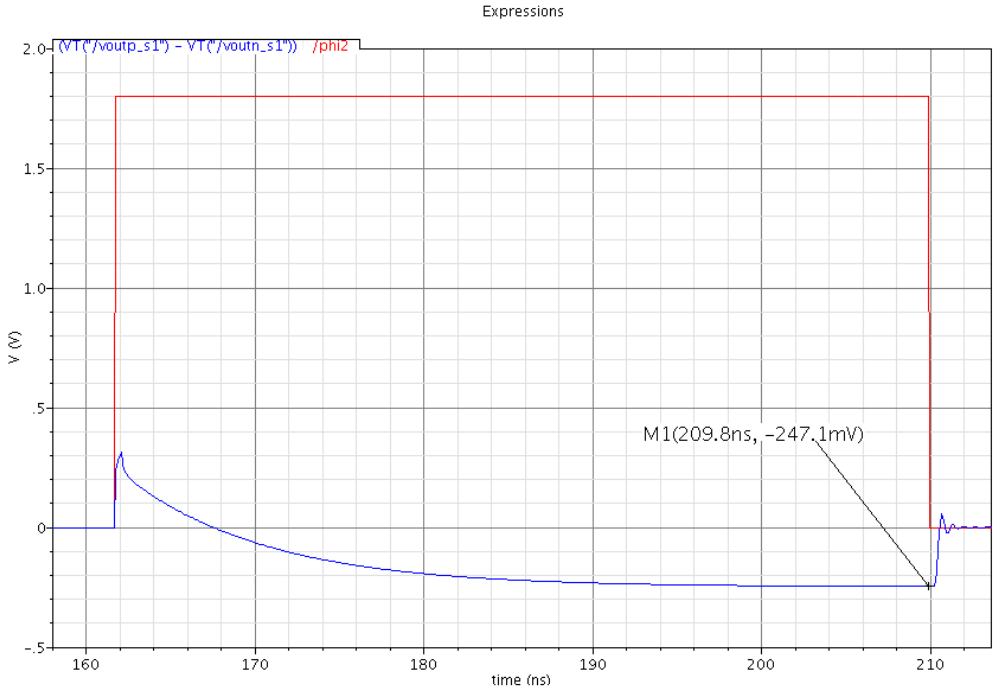

Figure 4.14: Transient Settling of ADC With Real OTA Design With Full-Scale Negative Input Voltage

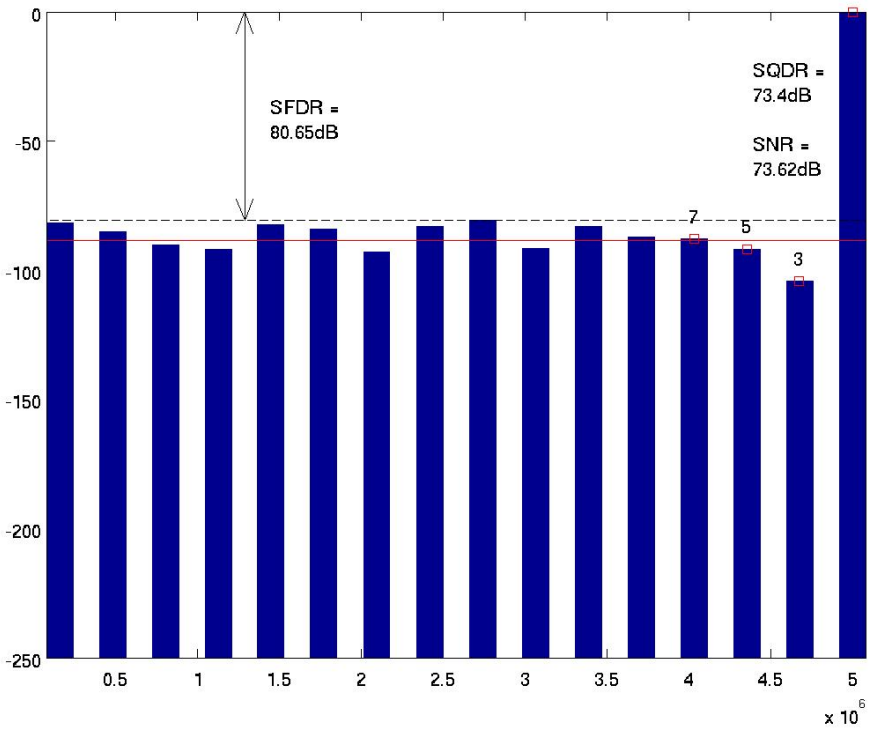

Figure 4.15: DFT of ADC With Real OTA Design

sistors will have additional non-linearities that are not present in the ideal model. In addition, the SQDR is still very close to the ideal 12-bit SQDR, so this result was considered acceptable.

After performing the SQDR simulations, the noise performance of the entire ADC could be simulated. Only the AC noise in the hold phase and the PNOISE simulations needed to be rerun. Since the OTA is not active in the sampling phase, the OTA does not contribute to the output noise in that phase. Figure 4.16 is a graph of the simulated ADC noise in the hold phase. The total output noise during the hold phase is $723\,\mu V_{rms}$, which is in

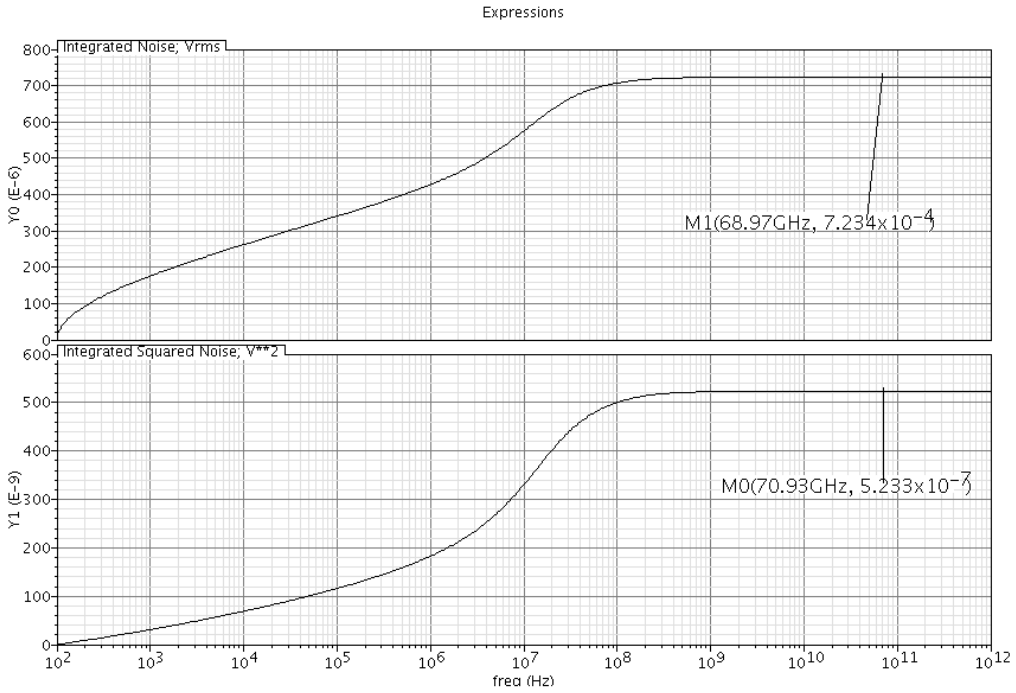

Figure 4.16: AC Noise During Hold Phase of ADC With Real OTA

good agreement with the simulations performed only on the OTA model. The

additional output noise is likely contributed from the switches. Once again, the output noise in the hold phase is well within budget. Table 4.3 summarizes the results from the AC noise simulation.

Setup	AC Sampling Noise (mV_{rms})	Total AC Hold Noise (mV_{rms})	AC Total Noise (mV_{rms})
Simulation	1.52	0.72	1.68
Calculation	1.51	0.34	1.55
Design Target	1.51	1.52	2.15
Error (%)	0.22	114.19	8.36
Headroom (%)	-0.22	52.52	21.75

Table 4.3: AC Noise Summary With Real OTA

After obtaining AC noise simulations that were within budget, the PNOISE simulation was run to ensure good agreement between AC noise and PNOISE simulations. The graph from the PNOISE simulation is shown in Figure 4.17 While the PNOISE results are higher than that obtained from the AC noise simulations, the results are still within 20% of each other. This level of agreement was considered acceptable for the noise simulations. Table 4.4 compares the results of the PNOISE simulation with the calculated values as well as the obtained AC noise measurements.

Differential Noise			
Setup	Total Noise Power (mV_{rms})	Error vs Calculation (%)	Error vs AC Simulation (%)
PNOISE Simulations	1.84	18.75	9.58

Table 4.4: ADC With Real OTA PNOISE Output Noise Summary

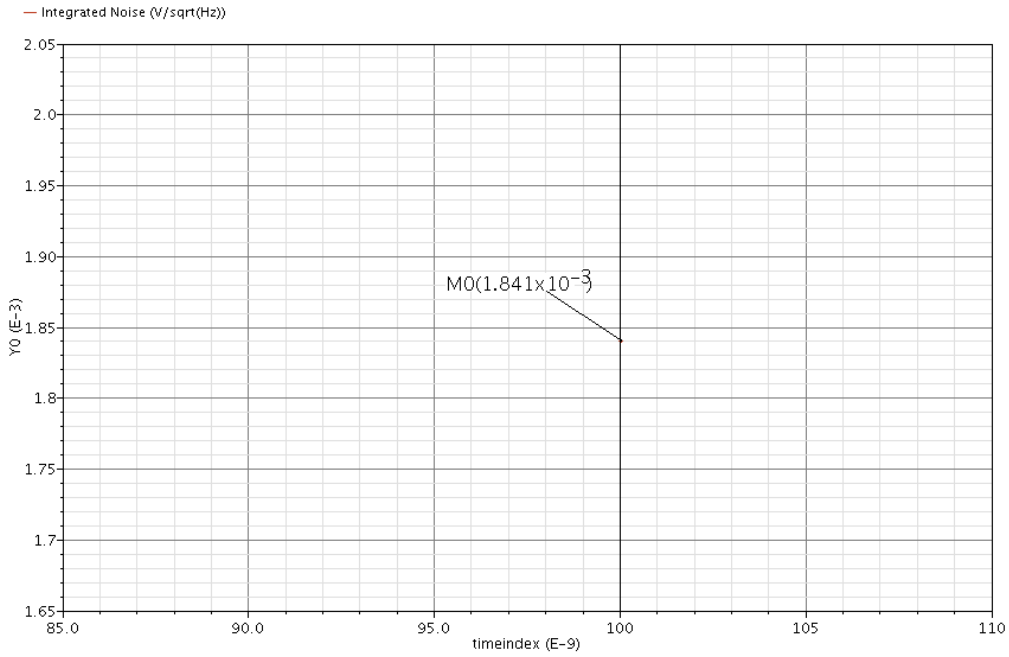

Figure 4.17: PNOISE Simulation Results of ADC With Real OTA

After obtaining acceptable results frm the noise simulation, the power consumption of the design could be simulated. Table 4.5 summarizes the simulated average total current consumption and the contribution to the total from different circuit blocks. From this average current, the average power

Circuit Block	Current (µA)	Percent of Total
OTA	694 µA	80.98
Digital logic and SAR capacitors	163 µA	19.02
Total	857 µA	

Table 4.5: ADC Power Consumption Summary

consumption was calculated to be 1.54 mW.

As in the case of previous simulations, the results from the SQDR and noise simulations could be combined to obtain an SNDR and ENOB. Additionally, the ENOB, sampling frequency, and power consumption numbers could be combined to obtain the final FOM of the design. Since the PNOISE simulation produced the highest output noise, its value was used for the SNDR calculation. The SNDR calculated using these parameters was:

$$SNDR = 71.4\,\text{dB} \tag{4.21}$$

From Equation 3.37, the ENOB is calculated to be 11.56 bits, which is still very close to an ideal 12-bit ADC performance. Using Equation 1.8, the FOM for this design was calculated to be:

$$FOM = \frac{1.54\,\text{mW}}{10\,\text{MHz} \cdot 2^{11.56}} \tag{4.22}$$

$$= 51\frac{\text{fJ}}{\text{conv-step}} \tag{4.23}$$

This number compares favorably with that obtained in other SAR-based pipeline designs [13].

Chapter 5

Conclusion

This chapter summarizes the results and discusses future work for this design.

5.1 Discussion

This work presented the initial design stages of a SAR-based pipeline ADC. With ever increasing focus on portable applications, power efficiency in ADCs will only become more important in the future. SAR ADCs are well known to be power efficient for applications requiring low sampling rates and medium to high resolutions. Applying the principles of pipelined ADCs to a SAR topology can increase the SAR application space to medium speed applications while still maintaining the power efficiency and high accuracy of the SAR topology. This design used a half-gain MDAC topology in order to reduce the required output swing and to increase overall ADC linearity. The half-gain topology alowed for the use of a triple-cascode OTA, which ended up being a low current solution. A novel scheme to obtain an additional bit of accuracy without increasing capacitance by utilizing the dummy LSB capacitor was also implemented. Although ideal clocks, comparators, and switches were

used the OTA performance generally dominates the power and SNDR figures. The total figure of merit obtained from this design show that this topology has a lot of promise for power constrained designs.

5.2 Future Work

While this design covers the majority of the implementation of the ADC, there is still much to be done to ensure that this design would perform adequately when taped out. Some additional architectural modifications could reduce the load capacitance of the design signficantly. In addition, there are circuit level optimizations that could be performed on both the OTA and the digital control logic. Finally, some additional blocks need to be designed and additional simulations need to be performed.

An extension of the implementation scheme in 2.2.2 could be used to obtain an additional bit of accuracy, or alternatively to halve the load capacitance in the second stage. Additionally, the differential scheme produces an additional bit of resolution that is currently not being utilized. This could lead to a factor of four reduction in load capacitance from the second stage capacitors. This could result in reduced power consumption or an increased sampling rate. These facts, along with realistic data on the parasitics from the OTA, suggest some re-architecting of the design could be done. The resolution of the two stages can be adjusted in order to achieve the best balance between sampling rate, power consumption, and total resolution. Furthermore, one large issue with the OTA design is that it will not scale well to future lower

voltage processes. A reevaluation of the OTA topology used would like be a worthwhile exercise as well. Performing these architectural modifications could greatly improve the total performance of the design.

One disadvantage to the usage of the implementation scheme in 2.2.2 is the additional reference voltages required to obtain the additional bit of accuracy from the dummy LSB capacitor. The voltages used in this report were ideal, so the additional reference voltages did not affect the overall power consumption of the design. This would not be true in a real design, however. Designing additional voltage references that are at least 12-bit accurate is a non-trivial task and the implementation may end up consuming too much power to be beneficial for the design. An alternative scheme that introduces some imbalance in the SAR common-mode voltage can be used to obtain the additional bit without introducing more reference voltages. This scheme could only be implemented in the second stage of the pipeline, because introducing this imbalance could cause inaccuracies in the residue voltage. This is not a severe disadvantage, however, since the second stage sampling capacitance has a larger effect on the OTA power consumption than the first stage capacitance. Adding an additional bit to the first stage through traditional means would mean an increase in total area, but since the unit capacitance of the first stage is not at its minimum this increase could be mitigated slightly. This is a limitation that could likely be overcome.

In addition to the architectural modifications the OTA and digital control logic performance could likely be improved at the circuit level. The OTA

performance could likely be improved by reducing the input capacitance to the amplifier. Another area worth taking a second look at is the digital control logic. Although the OTA dominates total power consumption, the switching of the SAR capacitors and the digital control logic contribute about 20% of the power. The digital logic was designed at the gate level using standard cells. It may be worthwhile to transform this design into register-transfer level (RTL) code, such as Verilog. Once this transformation is complete, a synthesis tool could be used to try to reduce the power consumption of the digital control logic even further.

After completing this front-end work, the clocking network, comparators, and switches will need to be designed. Simulations will need to be run on all these blocks both individually and integrated into the ADC to ensure that the ADC will meet its performance requirements across all process corners. Once all this work is done, a layout and parasitic extraction can be performed. With this data, additional simulations and design adjustments can be performed in order to obtain a high level of confidence that a manufactured design will meet its specifications. Finally, the design will need to be manufactured and tested. Depending on the results from this testing, additional debugging and design adjustments may be necessary to achieve the desired performance. In the ideal case, first silicon would yield the desired results, but if this is not the case another manufacturing run could be performed with an additional round of testing to follow. If all goes well in this second stage, working silicon could be demonstrated.

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