

Archlab 实验报告

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I. Part A

1. sum_list

完整汇编代码如下。

```
1  /* sum_list func */
2
3      .pos 0
4  init:
5      irmovl Stack, %esp      # init stack
6      irmovl Stack, %ebp
7      call Main
8      halt
9
10
11      .align 4                # example variable
12  ele1:
13      .long 0x00a
14      .long ele2
15  ele2:
16      .long 0x0b0
17      .long ele3
18  ele3:
19      .long 0xc00
20      .long 0
21
22
23  Main:
24      pushl %ebp
25      rrmovl %esp,%ebp
26      irmovl ele1, %edx      # %edx: head
27      pushl %edx             # set argument of sum_list
28      call sum_list         # sum_list();
29      rrmovl %ebp,%esp
30      popl %ebp
31      ret
32
33
34  sum_list:
35      pushl %ebp             # set stack
36      rrmovl %esp, %ebp
37      irmovl $0, %eax        # int val = 0; // %eax: val
38      mrmovl 8(%ebp), %ecx    # %ecx: ls
39      jmp loop_start
40
41  loop_start:                # while
42      mrmovl (%ecx), %edx     # %edx: ls->val
43      addl %edx, %eax         # val += ls->val;
44
```

```

45         mrmovl 4(%ecx), %ecx      # ls = ls->next; %edx: ls->next
46         andl %ecx, %ecx          # if ls == 0
47         je loop_end
48         jmp loop_start
49
50     loop_end:                    # restore stack
51         rrmovl %ebp, %esp
52         popl %ebp
53         ret                      # return val; // %eax
54
55
56     .pos 0x100
57     Stack:
58

```

程序运行结果如下，函数返回了 `0xcba`，即链表中所有元素的和。

```

thu@ubuntu:~/Documents/CSAPP/archlab-handout/sim/misc$ ./yis ./part_a/sum.yo
Stopped in 37 steps at PC = 0x11.  Status 'HLT', CC Z=1 S=0 O=0
Changes to registers:
%eax:  0x00000000      0x00000cba
%edx:  0x00000000      0x00000c00
%esp:  0x00000000      0x00000100
%ebp:  0x00000000      0x00000100

Changes to memory:
0x00ec: 0x00000000      0x000000f8
0x00f0: 0x00000000      0x0000003d
0x00f4: 0x00000000      0x00000014
0x00f8: 0x00000000      0x00000100
0x00fc: 0x00000000      0x00000011

```

2. rsum_list

其余代码与 `sum_list` 相同，`rsum_list` 部分代码如下。

```

1     /* rsum_list func */
2
3     rsum_list:
4         pushl %ebp
5         rrmovl %esp, %ebp
6         mrmovl 8(%ebp), %ecx      # %ecx: ls
7
8         andl %ecx, %ecx          # if (!ls)
9         je final
10
11        mrmovl (%ecx), %edx       # %edx: ls->val (*)
12        pushl %edx               # save now value
13
14        mrmovl 4(%ecx), %edx      # %edx: ls->next
15        pushl %edx               # set ls->next to be argument of next call
16        call rsum_list           # after call, %eax: rest = rsum_list(ls->next);
17        popl %edx
18        popl %edx                # %edx: val = ls->val saved in (*)
19        addl %edx, %eax          # %eax: val + rest, rtn value
20        jmp end
21

```

```

22     final:
23         irmovl $0, %eax    # %eax: 0, the rtn value
24         jmp end
25
26     end:
27         rrmovl %ebp, %esp
28         popl %ebp
29         ret                # return val; // or return 0, %eax

```

程序运行结果如下，函数也成功返回了 `0xcba`。

```

● thu@ubuntu:~/Documents/CSAPP/archlab-handout/sim/misc$ ./yis ./part_a/rsum.yo
Stopped in 73 steps at PC = 0x11.  Status 'HLT', CC Z=0 S=0 O=0
Changes to registers:
%eax: 0x00000000    0x00000cba
%edx: 0x00000000    0x0000000a
%esp: 0x00000000    0x00000100
%ebp: 0x00000000    0x00000100

Changes to memory:
0x00bc: 0x00000000    0x000000cc
0x00c0: 0x00000000    0x00000068
0x00c8: 0x00000000    0x00000c00
0x00cc: 0x00000000    0x000000dc
0x00d0: 0x00000000    0x00000068
0x00d4: 0x00000000    0x00000024
0x00d8: 0x00000000    0x000000b0
0x00dc: 0x00000000    0x000000ec
0x00e0: 0x00000000    0x00000068
0x00e4: 0x00000000    0x0000001c
0x00e8: 0x00000000    0x0000000a
0x00ec: 0x00000000    0x000000f8
0x00f0: 0x00000000    0x0000003d
0x00f4: 0x00000000    0x00000014
0x00f8: 0x00000000    0x00000100
0x00fc: 0x00000000    0x00000011

```

3. copy_block

完整汇编代码如下。

```

1  /* copy_block func */
2
3      .pos 0
4  init:
5      irmovl Stack, %esp
6      irmovl Stack, %ebp
7      call Main
8      halt
9
10
11     .align 4        # example variable
12     # Source block
13     src:
14         .long 0x00a
15         .long 0x0b0
16         .long 0xc00
17     # Destination block
18     dest:

```

```

19     .long 0x111
20     .long 0x222
21     .long 0x333
22
23
24 Main:
25     pushl %ebp
26     rrmovl %esp,%ebp
27
28     irmovl $3, %eax      # third argument: len = 3
29     pushl %eax
30     irmovl dest, %eax    # second argument: dest
31     pushl %eax
32     irmovl src, %eax     # first argument: src
33     pushl %eax
34
35     call copy_block
36     rrmovl %ebp,%esp
37     popl %ebp
38     ret
39
40
41 copy_block:
42     pushl %ebp
43     rrmovl %esp, %ebp
44     mrmovl 8(%ebp), %esi  # %esi: src
45     mrmovl 12(%ebp), %edi # %edi: dest
46     mrmovl 16(%ebp), %ecx # ecx: cnt
47     irmovl $0, %eax      # int result = 0; // %eax: result
48     loop:
49         mrmovl (%esi), %edx # %edx: value = *src;
50         rmmovl %edx, (%edi) # *dest = value;
51         xorl %edx, %eax    # result = result xor val;
52
53         irmovl $4, %edx
54         addl %edx, %esi    # src++;
55         addl %edx, %edi    # dest++;
56
57         irmovl $1, %edx
58         subl %edx, %ecx    # len--;
59         andl %ecx, %ecx    # if (len != 0)
60         jne loop
61     end:
62     rrmovl %ebp, %esp
63     popl %ebp
64     ret                  # return result; // %eax
65
66
67     .pos 0x100
68 Stack:
69

```

程序运行结果如下，程序返回了 `0xcba` 的结果，且 `dest` 所在的内存 `0x20 - 0x28` 中的值被 `dest` 覆盖。

```

lru@ubuntu:~/Documents/CSAPP/archlab-handout/sim/misc$ ./yis ./part_a/copy.yo
Stopped in 55 steps at PC = 0x11.  Status 'HLT', CC Z=1 S=0 O=0
Changes to registers:
%eax: 0x00000000 0x00000cba
%edx: 0x00000000 0x00000001
%esp: 0x00000000 0x00000100
%ebp: 0x00000000 0x00000100
%esi: 0x00000000 0x00000020
%edi: 0x00000000 0x0000002c

Changes to memory:
0x0020: 0x00000111 0x0000000a
0x0024: 0x00000222 0x000000b0
0x0028: 0x00000333 0x00000c00
0x00e4: 0x00000000 0x000000f8
0x00e8: 0x00000000 0x0000004d
0x00ec: 0x00000000 0x00000014
0x00f0: 0x00000000 0x00000020
0x00f4: 0x00000000 0x00000003
0x00f8: 0x00000000 0x00000100
0x00fc: 0x00000000 0x00000011

```

II. Part B

IADDL 指令将一个立即数的值加到一个寄存器上，并根据结果设置条件码。

ILEAVE 指令将栈恢复到上一个状态，相当于 **RRMOVL %ebp, %esp** 和 **IPOPL %ebp** 两条指令合并的效果。考察实际发生的变化，**%ebp** 指向的地址更新为其当前所指向的值，**%esp** 指向的地址为更新 **%esp** 当前所指向的地址+4。为了保持设计的一致性，译码阶段将 **%ebp** 同时存进 **valA** 与 **valB** 中。

1. SEQ

IADDL 指令与 **ILEAVE** 指令在 **SEQ** 实现中不同阶段的计算如表所示。

Stage	IADDL V, rB	ILEAVE
Fetch	$\text{icode:ifun} \leftarrow M_1[\text{PC}]$ $\text{rA:rB} \leftarrow M_1[\text{PC}+1]$ $\text{valC} \leftarrow M_4[\text{PC}+2]$ $\text{valP} \leftarrow \text{PC}+6$	$\text{icode:ifun} \leftarrow M_1[\text{PC}]$ $\text{valP} \leftarrow \text{PC} + 1$
Decode	$\text{valB} \leftarrow R[\text{rB}]$	$\text{valA} \leftarrow R[\text{\%ebp}]$ $\text{valB} \leftarrow R[\text{\%ebp}]$
Execute	$\text{valE} \leftarrow \text{valC} + \text{valB}$ Set CC	$\text{valE} \leftarrow 4 + \text{valB}$
Memory		$\text{valM} \leftarrow M_4[\text{valA}]$
Write Back	$R[\text{rB}] \leftarrow \text{valE}$	$R[\text{\$esp}] \leftarrow \text{valE}$ $R[\text{\$ebp}] \leftarrow \text{valM}$
Update PC	$\text{PC} \leftarrow \text{valP}$	$\text{PC} \leftarrow \text{valP}$

在 HCL 代码中，直接根据表中不同阶段内容补全语句即可。

(1) Fetch

添加两个指令有效并指定 `IADDL` 需要寄存器和立即数。

```
1  bool instr_valid = icode in
2      { INOP, IHALT, IRRMOVL, IIRMOVL, IRMMOVL, IMRMOVL,
3          IOPL, IJXX, ICALL, IRET, IPUSHL, IPOPL, IADDL, ILEAVE };
4
5  # Does fetched instruction require a regid byte?
6  bool need_regids =
7      icode in { IRRMOVL, IOPL, IPUSHL, IPOPL,
8          IIRMOVL, IRMMOVL, IMRMOVL, IADDL };
9
10 # Does fetched instruction require a constant word?
11 bool need_valC =
12     icode in { IIRMOVL, IRMMOVL, IMRMOVL, IJXX, ICALL, IADDL };
```

(2) Decode

为 `IADDL` 指定寄存器 `rB` 为 `srcB` 与 `dstE`，为 `ILEAVE` 指定寄存器 `%esp` 为 `srcA`、`srcB` 与 `dstE`，`%ebp` 为 `dstM`。

```
1  ## What register should be used as the A source?
2  int srcA = [
3      icode in { IRRMOVL, IRMMOVL, IOPL, IPUSHL } : rA;
4      icode in { IPOPL, IRET } : RESP;
5      icode in { ILEAVE } : REBP;
6      1 : RNONE; # Don't need register
7  ];
8
9  ## What register should be used as the B source?
10 int srcB = [
11     icode in { IOPL, IRMMOVL, IMRMOVL, IADDL } : rB;
12     icode in { IPUSHL, IPOPL, ICALL, IRET } : RESP;
13     icode in { ILEAVE } : REBP;
14     1 : RNONE; # Don't need register
15 ];
16
17 ## What register should be used as the E destination?
18 int dstE = [
19     icode in { IRRMOVL } && Cnd : rB;
20     icode in { IIRMOVL, IOPL, IADDL } : rB;
21     icode in { IPUSHL, IPOPL, ICALL, IRET, ILEAVE } : RESP;
22     1 : RNONE; # Don't write any register
23 ];
24
25 ## What register should be used as the M destination?
26 int dstM = [
27     icode in { IMRMOVL, IPOPL } : rA;
28     icode in { ILEAVE } : REBP;
29     1 : RNONE; # Don't write any register
30 ];
```

(3) Execute

IADDL 计算 `valC+valB` 并设置条件码, ILEAVE 计算 `4+valB`。

```
1  ## Select input A to ALU
2  int aluA = [
3      icode in { IRRMOVL, IOPL } : valA;
4      icode in { IIRMOVL, IRMMOVL, IMRMOVL, IIADDL } : valC;
5      icode in { ICALL, IPUSHL } : -4;
6      icode in { IRET, IPOPL, ILEAVE } : 4;
7
8      # Other instructions don't need ALU
9  ];
10
11 ## Select input B to ALU
12 int aluB = [
13     icode in { IRMMOVL, IMRMOVL, IOPL, ICALL,
14               IPUSHL, IRET, IPOPL, IIADDL, ILEAVE } : valB;
15     icode in { IRRMOVL, IIRMOVL } : 0;
16     # Other instructions don't need ALU
17 ];
18
19 ## Set the ALU function
20 int alufun = [
21     icode == IOPL : ifun;
22     icode in { IIADDL, ILEAVE } : ALUADD;
23     1 : ALUADD;
24 ];
25
26 ## Should the condition codes be updated?
27 bool set_cc = icode in { IOPL, IIADDL };
```

(4) Memory

设置 ILEAVE 读取内存, 地址为 `valA`。

```
1  ## Set read control signal
2  bool mem_read = icode in { IMRMOVL, IPOPL, IRET, ILEAVE };
3
4  ## Set write control signal
5  bool mem_write = icode in { IRMMOVL, IPUSHL, ICALL };
6
7  ## Select memory address
8  int mem_addr = [
9      icode in { IRMMOVL, IPUSHL, ICALL, IMRMOVL } : valE;
10     icode in { IPOPL, IRET, ILEAVE } : valA;
11     # Other instructions don't need address
12 ];
```

2. PIPE

IADDL 指令与 ILEAVE 指令在 PIPE 中实现与 SEQ 大致类似, 区别如下。最大的区别是需要对 ILEAVE 指令处理冲突问题, 见最后一部分。

(1) Fetch

添加两个指令有效并指定 `IADDL` 需要寄存器和立即数。只需将 `icode` 更为 `f_icode`。

```
1  bool instr_valid = f_icode in
2      { INOP, IHALT, IRRMOVL, IIRMOVL, IRMMOVL, IMRMOVL,
3          IOPL, IJXX, ICALL, IRET, IPUSHL, IPOPL, IIADDL, ILEAVE };
4  bool need_regids =
5      f_icode in { IRRMOVL, IOPL, IPUSHL, IPOPL,
6                  IIRMOVL, IRMMOVL, IMRMOVL, IIADDL };
7
8  # Does fetched instruction require a constant word?
9  bool need_valC =
10     f_icode in { IIRMOVL, IRMMOVL, IMRMOVL, IJXX, ICALL, IIADDL };
```

(2) Decode

为 `IADDL` 指定寄存器 `rB` 为 `srcB` 与 `dstE`，为 `ILEAVE` 指定寄存器 `%esp` 为 `srcA`、`srcB` 与 `dstE`，`%ebp` 为 `dstM`。只需将 `srcA`、`srcB`、`dstE`、`dstM` 都加上前缀 `d_`，`icode` 加上前缀 `D_`。

```
1  ## What register should be used as the A source?
2  int d_srcA = [
3      D_icode in { IRRMOVL, IRMMOVL, IOPL, IPUSHL } : D_rA;
4      D_icode in { IPOPL, IRET } : RESP;
5      D_icode == ILEAVE : REBP;
6      1 : RNONE; # Don't need register
7  ];
8
9  ## What register should be used as the B source?
10 int d_srcB = [
11     D_icode in { IOPL, IRMMOVL, IMRMOVL, IIADDL } : D_rB;
12     D_icode in { IPUSHL, IPOPL, ICALL, IRET } : RESP;
13     D_icode == ILEAVE : REBP;
14     1 : RNONE; # Don't need register
15 ];
16
17 ## What register should be used as the E destination?
18 int d_dstE = [
19     D_icode in { IRRMOVL, IIRMOVL, IOPL, IIADDL } : D_rB;
20     D_icode in { IPUSHL, IPOPL, ICALL, IRET, ILEAVE } : RESP;
21     1 : RNONE; # Don't write any register
22 ];
23
24 ## What register should be used as the M destination?
25 int d_dstM = [
26     D_icode in { IMRMOVL, IPOPL } : D_rA;
27     D_icode == ILEAVE : REBP;
28     1 : RNONE; # Don't write any register
29 ];
```

(3) Execute

`IADDL` 计算 `valC+valB` 并设置条件码，`ILEAVE` 计算 `4+valB`。除了加上前缀外，设置条件码的条件有所变化，但只需将 `E_icode == IOPL` 改为 `E_icode in { IOPL, IIADDL }` 即可。

```
1  ## Select input A to ALU
2  int aluA = [
```



```

3     E_icode in { IRRMOVL, IOPL } : E_valA;
4     E_icode in { IIRMOVL, IRMMOVL, IMRMOVL, IIADDL } : E_valC;
5     E_icode in { ICALL, IPUSHL } : -4;
6     E_icode in { IRET, IPOPL, ILEAVE } : 4;
7     # Other instructions don't need ALU
8 ];
9
10 ## Select input B to ALU
11 int aluB = [
12     E_icode in { IRMMOVL, IMRMOVL, IOPL, ICALL,
13                 IPUSHL, IRET, IPOPL, IIADDL, ILEAVE } : E_valB;
14     E_icode in { IRRMOVL, IIRMOVL } : 0;
15     # Other instructions don't need ALU
16 ];
17
18 ## Set the ALU function
19 int alufun = [
20     E_icode == IOPL : E_ifun;
21     E_icode in { IIADDL, ILEAVE } : ALUADD;
22     1 : ALUADD;
23 ];
24
25 ## Should the condition codes be updated?
26 bool set_cc = E_icode in { IOPL, IIADDL } &&
27     # State changes only during normal operation
28     !m_stat in { SADR, SINS, SHLT } && !W_stat in { SADR, SINS, SHLT };

```

(4) Memory

设置 `ILEAVE` 读取内存，地址为 `valA`。只需更改前缀。

```

1     ## Select memory address
2     int mem_addr = [
3         M_icode in { IRMMOVL, IPUSHL, ICALL, IMRMOVL } : M_valE;
4         M_icode in { IPOPL, IRET, ILEAVE } : M_valA;
5         # Other instructions don't need address
6     ];
7
8     ## Set read control signal
9     bool mem_read = M_icode in { IMRMOVL, IPOPL, IRET, ILEAVE };
10
11     ## Set write control signal
12     bool mem_write = M_icode in { IRMMOVL, IPUSHL, ICALL };

```

(5) Pipeline Register Control

处理冒险情况。`ILEAVE` 本质上执行了一个 `IPOPL` 指令，会出现加载使用冒险，导致后续代码若试图调用 `%ebp` 的值会得到错误结果。在代码中包含 `IPOPL` 处类似地补充 `ILEAVE`，使程序在必要时等待访存阶段结束即可。

```

1     # Should I stall or inject a bubble into Pipeline Register F?
2     # At most one of these can be true.
3     bool F_bubble = 0;
4     bool F_stall =
5         # Conditions for a load/use hazard
6         E_icode in { IMRMOVL, IPOPL, ILEAVE } &&

```

```

7      E_dstM in { d_srcA, d_srcB } ||
8      # Stalling at fetch while ret passes through pipeline
9      IRET in { D_icode, E_icode, M_icode };
10
11     # Should I stall or inject a bubble into Pipeline Register D?
12     # At most one of these can be true.
13     bool D_stall =
14         # Conditions for a load/use hazard
15         E_icode in { IMRMOVL, IPOPL, ILEAVE } &&
16         E_dstM in { d_srcA, d_srcB };
17
18     bool D_bubble =
19         # Mispredicted branch
20         (E_icode == IJXX && !e_Cnd) ||
21         # Stalling at fetch while ret passes through pipeline
22         # but not condition for a load/use hazard
23         !(E_icode in { IMRMOVL, IPOPL, ILEAVE } && E_dstM in { d_srcA, d_srcB }) &&
24         IRET in { D_icode, E_icode, M_icode };
25
26     # Should I stall or inject a bubble into Pipeline Register E?
27     # At most one of these can be true.
28     bool E_stall = 0;
29     bool E_bubble =
30         # Mispredicted branch
31         (E_icode == IJXX && !e_Cnd) ||
32         # Conditions for a load/use hazard
33         E_icode in { IMRMOVL, IPOPL, ILEAVE } &&
34         E_dstM in { d_srcA, d_srcB };

```