Ziyi Huang
EE 371 HW3
April 30, 2019

1. P1

   Design decisions

   - count to 31 and stay there in the cycling mode
   - always start from 0 in cycling mode

   Testbenches

   - read without write in cycling mode
   - write while reading in cycling mode to show the synchronicity
   - verify the write and read at any address in normla mode. The testbench provides the read addresses.

   Simulations

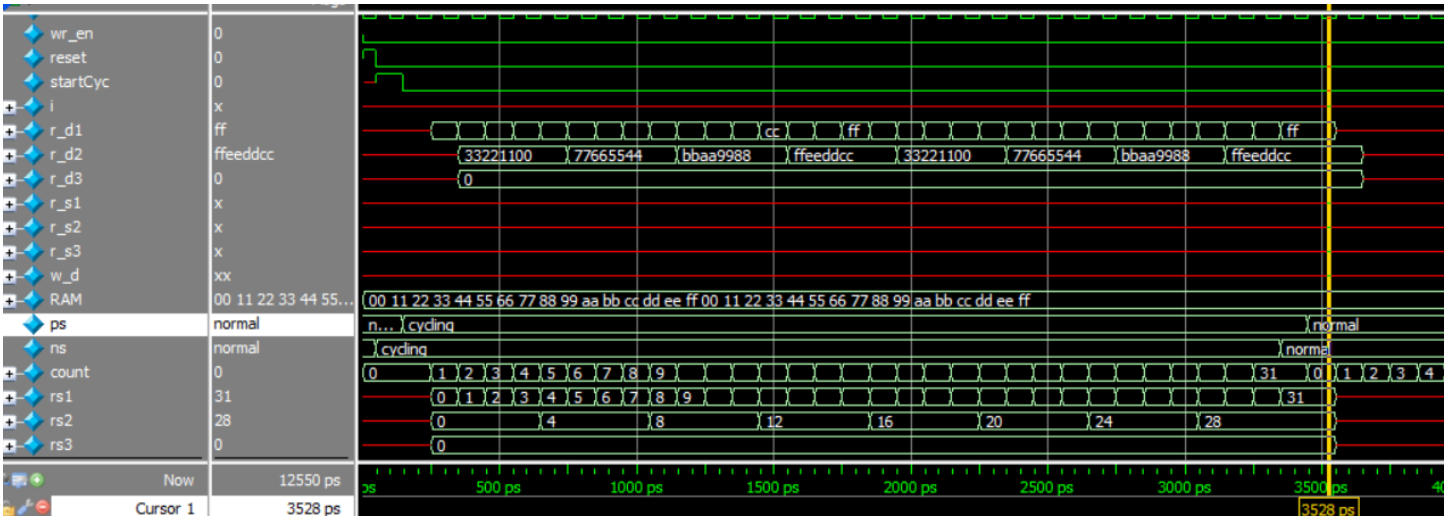

Figure 1: Test Case 1

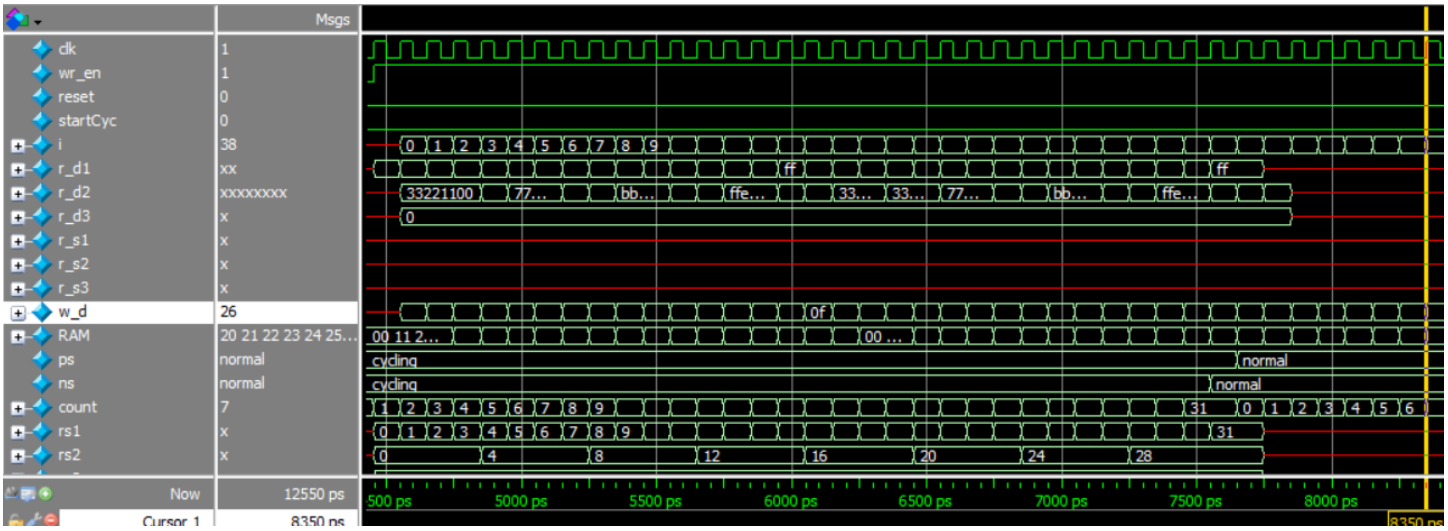

Figure 2: Test Case 2

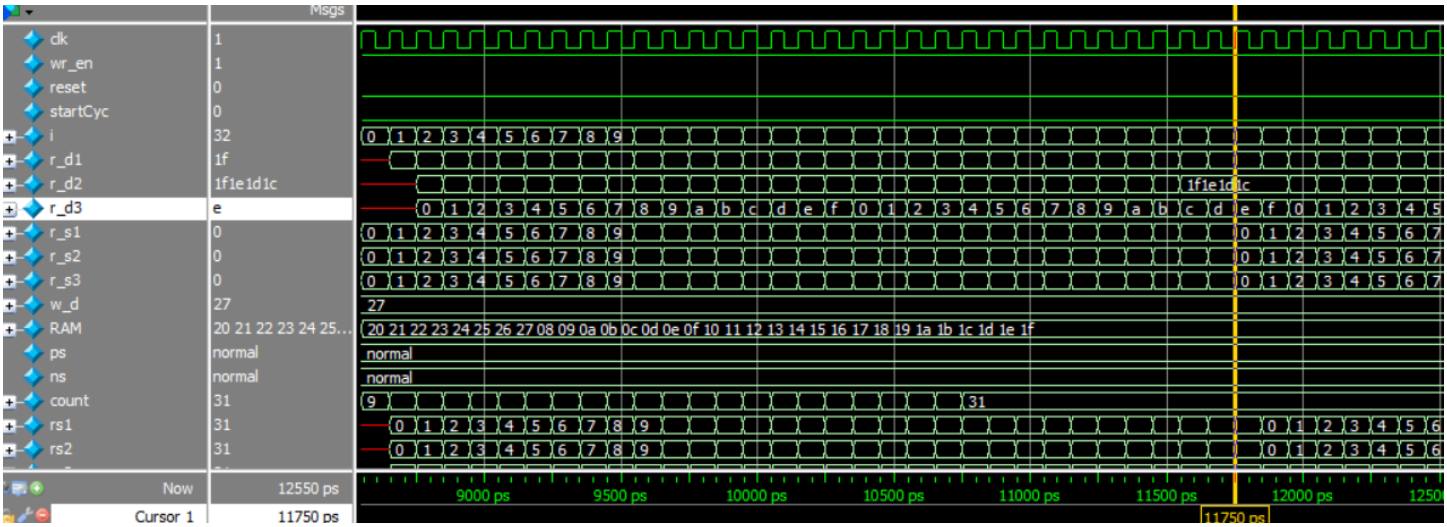

Figure 3: Test Case 3

2. P2
   Modifications

   - changed w_{data} to double the size of r_{data}
   - changed the w_{succ} to increment by 2 every time

   Made sure it is able to write at any good address but stops when full; make sure it's able to read at any address till it's empty; make sure it writes before reads.

   Simulations

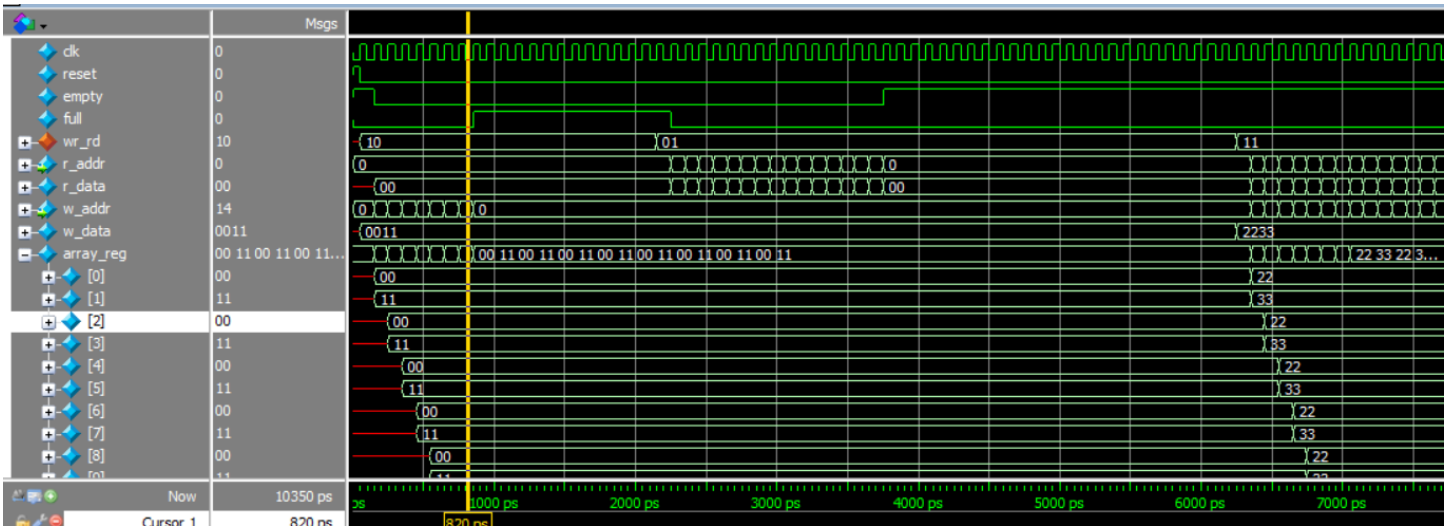

Figure 4: Keeps writing the FIFO till it's full

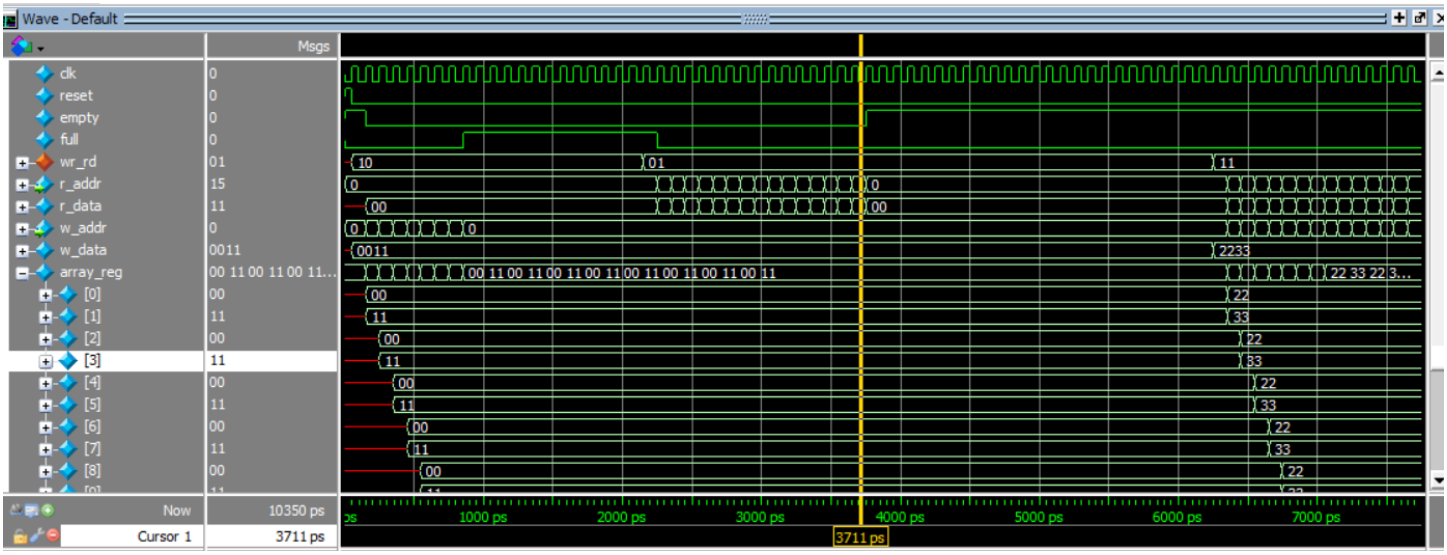

Figure 5: Keeps reading the FIFO till it's empty

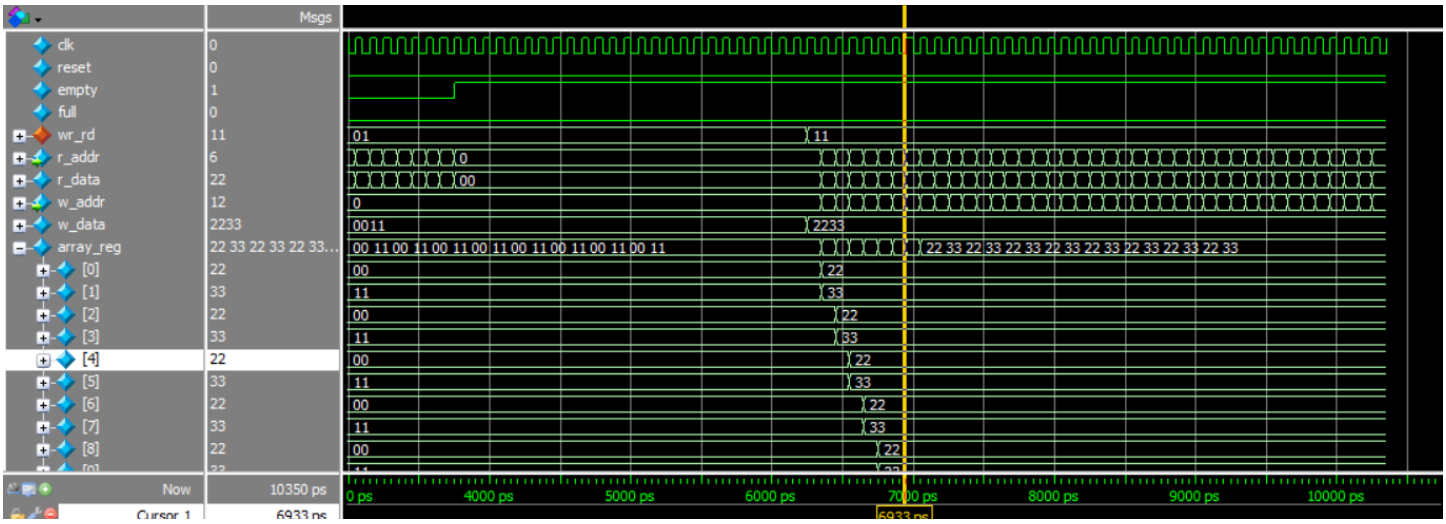

Figure 6: Write and read at the same time

3. P3

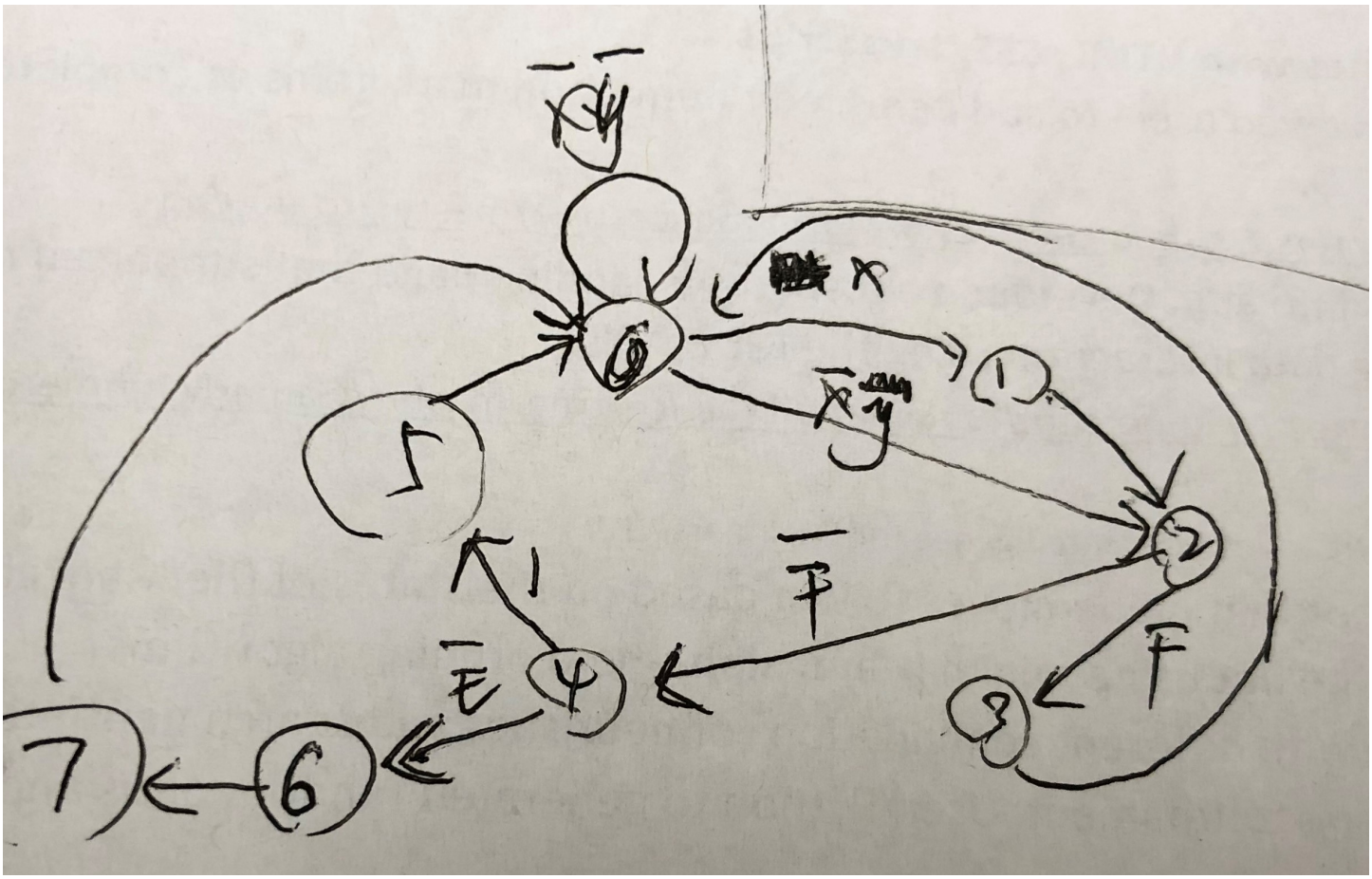

Figure 7: The ASM chart

4. Comments
   I like this homwork. I spent around 3 hours doing it. The major difficulty lies in organizing the logic. It's kind of challenging and intellectually stimulating.