EE/CSE 371 Digital Design

HW4

Algorithmic State Machines with Datapath

1. Draw the ASMD charts for the following state transitions:
   a. If x=1, control goes from state S1 to state S_2; if x=0, generate a conditional operation R<=R+2 and go from S1 to S2.
   b. If x=1, control goes from S1 to S2 and then to S_3; if x=0, control goes from S1 to S3.
   c. Start from state S_1; then if xy=11, xy=11, go to S_2; if xy=01 go to S_3; and if xy=10, go to S_1; otherwise, go to S3.

2. Construct a block diagram and an ASMD chart for a digital system that counts the number of people in a room. The one door through which people enter the room has a photocell that changes a signal *x* from 1 to 0 while the light is interrupted. They leave the room from a second door with a similar photocell that changes a signal *y* from 1 to 0 while the light is interrupted. The datapath circuit consists of an up–down counter with a display that shows how many people are in the room. Each person should be counted once.

3. The purpose of this exercise is to take a legacy code that may not be functioning correctly and fix it. You are provided with Verilog files that implement the divider that was discussed in lectures and you need to convert the code into SystemVerilog and simulate it in ModelSim. The purpose is not to create a new implementation for the divider but to work with what is provided, test it, and make it work as it is supposed to be. Your understanding of the divider's datapath and control path should help in figuring out the faults in the program (if any). Provide screen shots of the simulation before and after your modification to the program and attach the SystemVerilog files with your submission.

Deliverables:

- Solution to the hw problems in a word or pdf file.
- SystemVerilog files for any code written.
- A commentary section with feedback on the hw highlighting the level of difficulty and the time spent to solve it.