1-Tbyte/s 1-Gbit DRAM Architecture Using 3-D Interconnect for High-Throughput Computing

Tomonori Sekiguchi, *Member, IEEE*, Kazuo Ono, Akira Kotabe, and Yoshimitsu Yanagawa

***Abstract*—Aiming to resolve memory bottlenecks in multi-core system, novel 1-Tbyte/s 1-Gbit DRAM architecture based on a multi-core configuration and 3-D interconnects was developed. The DRAM stacked on a multi-core CPU has 512-bit I/Os with through-silicon-via (TSV) distributed in 16 memory cores. Five-stage pipelined architecture in the compact DRAM core was developed to reduce the operation cycle of the data-bus to 2 ns. A low-noise early-bar-write scheme for an 8-ns cycle array operation and 16-Gbit/s I/O circuits on TSV were also developed. The proposed DRAM architecture greatly improves power efficiency. TSV scheme reduces the parasitic capacitance of the interconnects between the DRAM and CPU, and multi-core architecture reduces the length of the data bus on the DRAM. A 1-Gbit DRAM was designed based on the 45-nm stand-alone DRAM process. Chip size is 51.6 mm^2 assuming 4F^2 memory cells, and the density is about 5 times higher than that of embedded DRAM. Circuit simulations confirmed the 2-ns operation of the data bus, 8-ns operation of the memory array, and 16-Gbit/s operation of I/O circuits. Power consumption is 19.5 W, providing power efficiency of 51.3 Gbyte/s/W, which is an order of magnitude higher than that of conventional DRAMs.**

***Index Terms*—DRAM, multi-core, pipeline, TSV, 3D interconnect.**

I. Introduction

THE clock frequency of typical single-core CPU for desktop computing almost saturated at the beginning of the 2000s. At that time, with the introduction of multi-core CPUs, data throughput started to increase again, as shown in Fig. 1. Data throughput of DRAM module has been increased by doubling the number of pre-fetch bits in a DRAM chip and adding a memory-bus channel. From now onwards, the required data rate for DRAM will increase proportionally with the increasing number of cores integrated on a CPU. It will become harder for conventional general-purpose DRAM to keep up with the data-rate requirement due to the ever increasing power consumption.

The relationships between power consumption and data rate of various DRAMs are plotted in Fig. 2. GDDR4 DRAM achieves 200 Gbyte/s by using parallel operation of 16 chips.

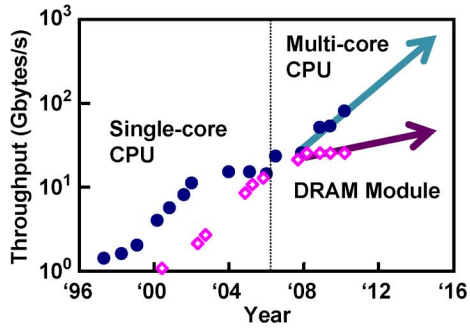


Fig. 1. Gap between CPU's and DRAM Module's data throughput.

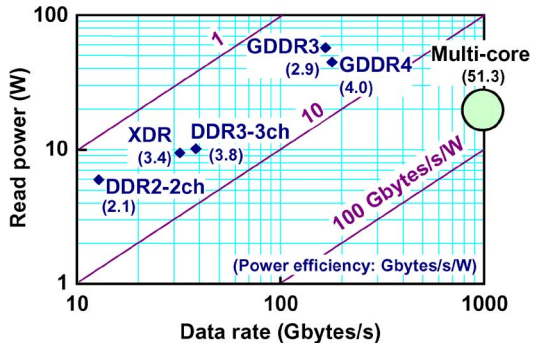


Fig. 2. Power efficiency comparison between multi-core DRAM and conventional DRAMs.

However, its power consumption is very large, namely, 50 W in total. If the power efficiency defined by the data rate per unit power consumption is assumed to be constant, a 1-Tbyte/s memory system based on GDDR4 would require a power supply of over 250 W. A memory with such a huge power consumption would be unacceptable because the increasing power consumption of IT systems has recently become problematic from the environmental viewpoint. A new DRAM architecture for increasing power efficiency by an order of magnitude is therefore necessary to realize future 1-Tbyte data-rate memory systems.

Recently, 3-D integration of chips, such as a stacked DRAM on a CPU based on micro-bump technology [1], multiple stacked DRAMs based on through-silicon-via (TSV) technology [2], a stack composed of an SRAM on a CPU based on TSV [3], a stacked reconfigurable SRAM on a SoC based on micro-bump technology [4], has been developed. This 3-D integration technology increases the number of I/O pins between chips drastically because they can be placed anywhere on the chips. It also reduces the parasitic capacitance of the interconnection between chips. These two factors enable faster data rate

Manuscript received August 09, 2010; revised November 12, 2010; accepted December 21, 2010. Date of publication March 03, 2011; date of current version March 25, 2011. This paper was approved by Guest Editor Makoto Nagata.

T. Sekiguchi is with Hitachi Europe Ltd. European Research and Development Centre, Maidenhead, Berkshire SL6 8YA, U.K. (e-mail: tomonori.sekiguchi@hitachi-eu.com).

K. Ono, A. Kotabe, and Y. Yanagawa are with Hitachi, Ltd., Central Research Laboratory, Measurement Systems Research Department, Kokubunji, Tokyo 185-8601, Japan.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2011.2109630

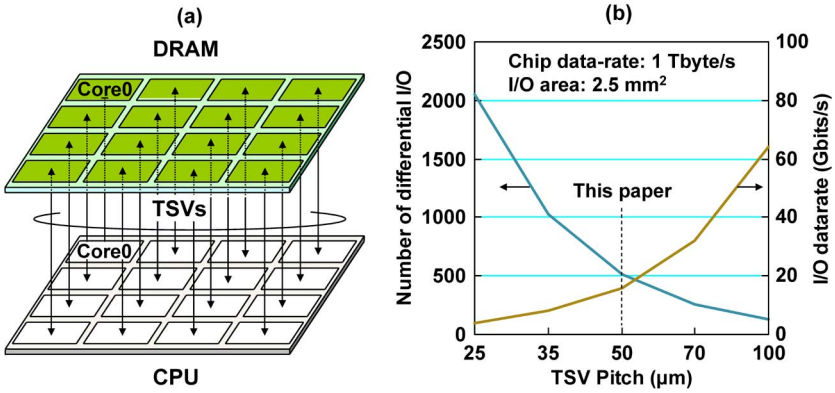


Fig. 3. Concept of multi-core DRAM that features core-to-core connection with TSVs.

and lower-power chip-to-chip communication compared with conventional 2-D interconnection. However using SRAM cell, density of the memory cell, which is reported as 3.0 Mbits/mm^2 even in 40 nm technology [5], is smaller compared with that of the embedded DRAM, which is reported as 4.2 Mbits/mm^2 in 45 nm technology [6], and impact on the memory capacity of 3-D integration is not significant.

In the present study, a new multi-core DRAM architecture stacked on a CPU using TSV—which supports high data rate (1 Tbyte/s) and high capacity (1 Gbit)—is proposed [7]. A 45-nm stand-alone DRAM technology enables to integrate 1 Gbit of memory cells in 51.6 mm^2 of chip size. Its density is 19.8 Mbits/mm^2, about 5 times higher than embedded DRAM. The fast array cycle of 8 ns is achieved even in stand-alone DRAM technology by reducing array size and introducing early-write scheme, which is conventionally used in embedded DRAM [8]. A new low-noise early-write scheme suitable for open bit-line array is proposed.

This paper is organized as follows. First, the new DRAM architecture for multi-core systems is introduced, and the novel concept of core-to-core connection between DRAM and a CPU is described in Section II. Three circuit techniques for achieving 1-Tbyte/s date rate are described in Section III. These are micro-pipelined DRAM core, a new memory array write scheme called "early bar write", and a 16-Gbits/s input-output circuit. Finally, some results of circuit simulation of the designed DRAM are described.

II. Concept of Multi-Core DRAM

A conceptual image of a 3D-integrated multi-core DRAM and CPU system is shown in Fig. 3(a). The DRAM chip is divided into 16 cores, and each DRAM core is connected to a CPU core by a group of TSVs. This system has three advantages. First, each pair of cores (i.e., a CPU core and a DRAM core) can be operated independently by using dedicated TSVs. In conventional multi-core systems, a DRAM is shared by several CPU cores because the number of I/O pins is limited. This sharing often causes access conflict when several CPU cores issue memory-access commands concurrently. Thanks to the use of TSV technology, each CPU core can have a dedicated DRAM core, which can be independently accessed, because the number of I/O pins is increased and the pins can be placed anywhere on the chip. This memory architecture widely increases the flexibility of memory system design.

The second advantage is an ultra-high-speed interface. Small TSVs are used to integrate thousands of I/O pins on a chip, and interconnect parasitics between stacked chips is greatly reduced. These features make a 1-Tbyte/s interface between chips possible. Fig. 3(b) shows the condition that must be met to achieve 1-Tbyte/s throughput in multi-core DRAM. It is assumed that the I/O area occupies 5% of the chip area of 50 mm^2. As TSV pitch is reduced, the number of I/Os on the chip is increased, and I/O data rate can thus be reduced. In this study, under the assumption that the TSV pitch is 50 μm, a DRAM chip has 512 differential I/Os operating at 16 Gbits/s. The third advantage is reduction of power consumption. TSVs shorten interconnect length between the CPU and DRAM chip. Moreover, since the DRAM chip is divided into multi cores, the data bus on the DRAM chip also becomes short. Shorter interconnect length reduces power consumption of off-chip, and the shorter data bus reduces that of on-chip data communication.

The multi-core DRAM can be used as main-memory for a system with limited memory capacity such as graphics card. It also can be used as L2 cache with conventional DRAM based main-memory in a system with high memory capacity such as server. Moreover it is reported that stacked DRAM extends the capacity of the SRAM based L2 cache [9]. Proposed multi-core DRAM can also be applied to this architecture. Here the system performance improvement is estimated assuming that the multi-core DRAM is applied to L2 cache.

In conventional memory systems, as shown in Fig. 4(a), the low data-rate of the main-memory DRAM and a small L2 cache restrict system performance. The L2 caches for each CPU core are separated for simplicity, although it is shared in some case. For example, current CPUs have a cache with a capacity of 64 Mbits, and DDR3 DRAM modules on three channels have a data rate of 40 Gbytes/s. As the throughput of the CPU increases, miss rate of each L2 cache also increases. This miss-rate increase severely degrades the performance of the system because the CPU is delayed by the large latency of the main-memory DRAM.

In contrast, with our multi-core DRAM cache, as shown in Fig. 4(b), main-memory DRAM latency will be concealed

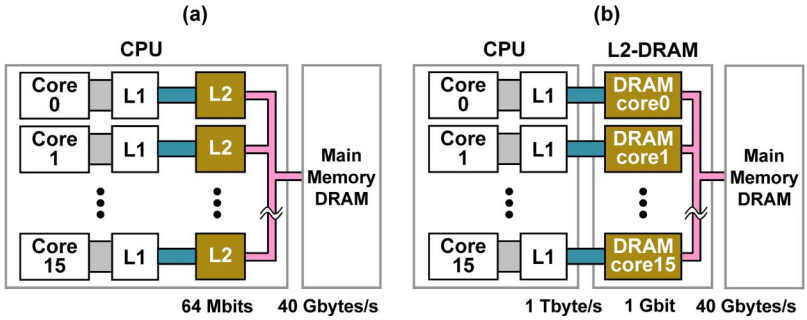


Fig. 4. Bottleneck between multi-core CPU and DRAM: (a) conventional memory system and (b) proposed memory system with multi-core DRAM.

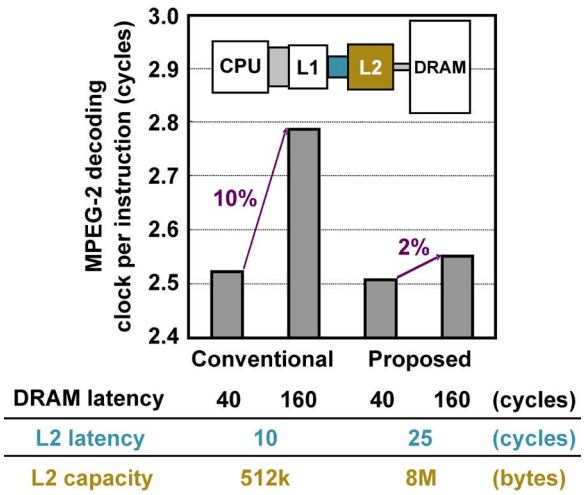


Fig. 5. Performance improvement of multi-core high-density cache memory system.

TABLE I
DRAM ARCHITECTURES

	DDR3 DRAM	Multi-core DRAM (Proposed)
Architecture	CA, Array 47.5-ns cycle, DBUS, I/O x16	Core 0, CA, Array 8-ns cycle, DBUS, I/O x32, Core 1 ... Core 15
DBUS cycle	5 ns	2 ns
DBUS length	~ 5 mm	~ 1.3 mm
Granularity	128 bits @ 3.2 Gbytes/s 40 kbits @ 1 Tbyte/s	1 kbit @ 1 Tbyte/s

thanks to the large (i.e., 1-Gbit) memory capacity and high throughput (i.e., 1 Tbyte/s) between the CPU and L2-DRAM. Such high throughput is realized by a direct connection between the L1 cache and the L2-DRAM core through a TSV. Large capacity is attained by using $4F^2$ DRAM cells [10] with a stand-alone DRAM process.

The performance of the multi-core DRAM cache on a multi-core CPU system was estimated and compared with that of a conventional memory system as shown in Fig. 5. A single-core computation was simulated by dividing L1 and L2 capacity between 16 cores. Contention for memory access by multi-cores was not considered, for simplicity. However, it was reported that with the help of operating system, access from each core can be controlled mainly to correspond L2 cache [9].

In a conventional system, L2 cache is assumed to have low latency of 10 and small capacity of 512 kbytes, which are features of an on-chip SRAM. On the other hand, L2 cache of the proposed system is assumed to have medium latency of 25 and larger capacity of 8 Mbytes, which are features of the proposed multi-core DRAM. The graph compares the two systems evaluated in terms of clock-per-instruction value for MPEG-2 decoding operation of HD quality video. For each system, two cases, namely, the best and worst DRAM latency (i.e., 40 cycles and 160 cycles in the CPU clock, respectively) were simulated. L2 miss rate of the conventional system is 14%, but that of the proposed system is reduced to 2% due to the large L2 capacity. Performance degradation from best-case to worst-case DRAM latency is high, namely, 10%, in the case of the conventional system. In contrast, in the case of the proposed system, it is reduced to only 2%. That means the performance of the proposed system is not susceptible to latency change of main-memory DRAM caused by contention of multi-cores. These results verify that the multi-core system with a large L2 cache improves system performance.

III. 1-TBYTE/S DRAM CIRCUIT TECHNIQUES

A. *Five-Stage Micro-Pipelined DRAM Core*

So far, synchronous DRAM has increased data rates by doubling the number of pre-fetch bits. In the case of DDR3 as shown in Table I, the DBUS, which connects the memory array and I/O circuit, consists of 128-bit wide data lines for 16-bit I/O circuits with 8-bit pre-fetch. The DBUS width determines the granularity of the chip, which is the minimum data size that can be accessed independently. In the case that the DBUS is operated in 5-ns cycles, data rate of the chip is 3.2 Gbyte/s. In a conventional DDR3 architecture, it is difficult to reduce the cycle time of the DBUS drastically because the length of the DBUS is long (namely, about 5 mm in typical case) and because the improvement in MOS transistor performance on the DRAM is moderate.

To realize a throughput of 1 Tbyte/s by a pre-fetch strategy keeping DBUS cycle as 5 ns, the number of pre-fetch bits must be increased by a factor of 320, resulting in a granularity as large as 40 kbits. Because of such a huge granularity and long

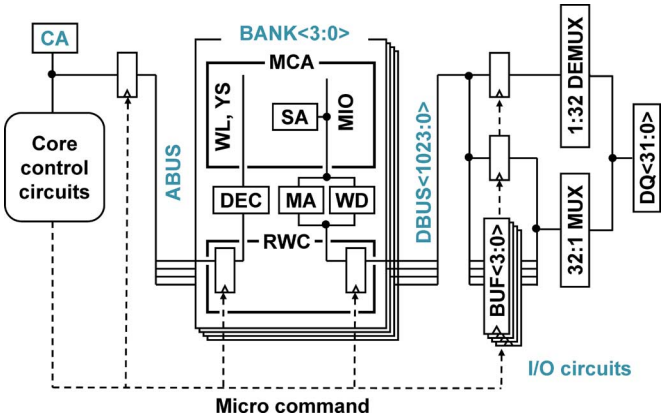


Fig. 6. Five-stage-pipelined DRAM core.

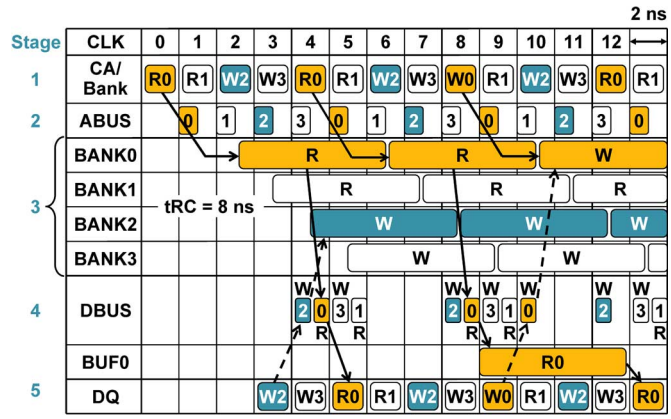


Fig. 7. Four-bank interleaved pipeline operation.

data bus, the power consumption of the bus is expected to be huge. Moreover, owing to a slow array cycle of 47.5 ns, which is a typical value in data-sheet of DDR3 products, the page-miss penalty will become too large to allow the DDR3 architecture to be applied for cache memory.

To eliminate these disadvantages regarding the DDR3 architecture, a novel multi-core DRAM architecture (as shown in the Table I) is proposed. In this architecture, a DRAM chip is separated into 16 cores. Each core has a DBUS with 1024 lines, and its length is reduced to 1.3 mm. Circuit simulation described later confirms that the DBUS operates at 2-ns cycle.

A memory array based on the novel multi-core DRAM architecture can be operated in an 8-ns cycle as also confirmed in circuit simulation. The proposed DRAM can achieve 1-Tbyte/s throughput by increasing the number of pre-fetch bits by a factor of eight only. That is to say, granularity is only increased to 1024 bits by the 16-core architecture and 2-ns-cycle DBUS. As a result, it is confirmed in the circuit simulation that DBUS power consumption is reduced to 28%. High-speed array operation enables fast random access suitable for cache memory.

The proposed micro-pipelined architecture is shown in Fig. 6. Pipeline registers divide the core into five stages: command/address input buffer (CA), address bus (ABUS), memory bank (BANK), data bus (DBUS), and input-output (I/O) circuits. The I/O circuits consist of 32 data input/output buffers (DQ), 32:1 multiplexers (MUX) and 1:32 de-multiplexers (DEMUX) for each DQ, and delayed buffers (BUF) for each bank. DBUS and DQ are bidirectionally used for read and write data transmission. Each BANK operates at an 8-ns cycle in an interleaved manner, whereas CA, ABUS, and DBUS operate in a 2-ns cycle. Controlled by a group of 32 equally separated phase clocks, DQ transmits and receives the data in a 62.5-ps cycle, as described in a later section. Each pipeline register is controlled by micro commands generated by a core-control circuit.

The timing sequence for four-bank interleaved pipeline operation is shown in Fig. 7. Access to each BANK uses CA, ABUS, and DQ in order. Read and write latencies are set to 5 and 1, respectively. Accordingly, at the DQ and array activation stages, the same time-slot can be assigned for read and write operations. A gapless operation sequence in the case of a concurrent read and write operations for different banks is depicted as *BANK0-Read (R0)* issued at CA in CLK cycle 0 and *BANK2-Write (W2)* issued in cycle 2. The DBUS cycle is separated into two slots in the time domain. The first slot is assigned to write data, and the second is assigned to read data. As a result, read data from BANK0 and write data to BANK2 can pass each other on the DBUS in cycle 4 without collision.

A gapless-operation sequence in the case of successive read and write operations for the same bank is depicted as *BANK0-Read (R0)* issued at CA in cycle 4 and *BANK0-Write (W0)* issued in cycle 8 (see Fig. 7). In the conventional architecture, output data for the read command will conflict with input data for the write command at the DQ stage. A "*no operation*" (*NOP*) at cycle 8 results in a data bubble at DQ. To avoid this bubble and to achieve gapless read and write operations, a delay buffer (shown as BUF0) retains the read data temporarily. Write data is accepted prior to output of read data. The read data in BUF0 is output after another read command is accepted. In the case shown here, *BANK0-read (R0)* input at cycle 12 produces a read-data output at cycle 13.

Floor plans of the data-bus and micro-command wiring from the pipeline control circuits are shown in Fig. 8. The 1024-bit wide data bus vertically connects the read/write circuits (RWCs) in the banks and the data latches (DLs) in the I/O circuits used commonly for read and write. Read/write circuits and data-latch circuits are shown schematically in Fig. 9. In the Read/Write circuits, the read-data from the memory array kept in the main-amplifier (MA) is latched and transmitted on DBUS by $\mathrm{RCK}\langle \mathrm{n} \rangle$ for each bank. The write data on the DBUS are received by the flip-flop according to $\mathrm{WCK}\langle \mathrm{n} \rangle$ and transferred to the write driver (WD) in the banks. In this architecture, data on DBUS0 to DBUS15 are transmitted or received on a DQ synchronized to the first half clock phase, Φ_0 to Φ_{15}, and data on DBUS16 to DBUS31 are transmitted or received on the same DQ synchronized to the second half clock phase, Φ_{16} to Φ_{31}. Data latch DLD is connected to DBUS0-15, and DLU is connected to DBUS16-31. In both circuits, data on the data bus are received by RCKO in a latch or a flip-flop connected to the input of the multiplexer (MUX), TD0-31. The data are received by a delayed buffer according to ICK and transmitted from it by OCK. During the write operation, data in the flip-flop connected to

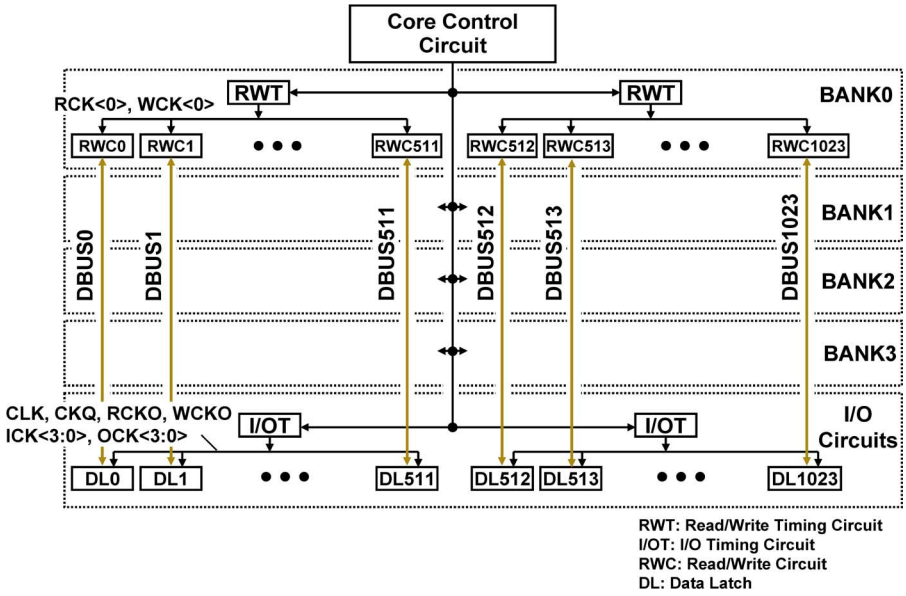


Fig. 8. Databus and micro-command wiring floor plan.

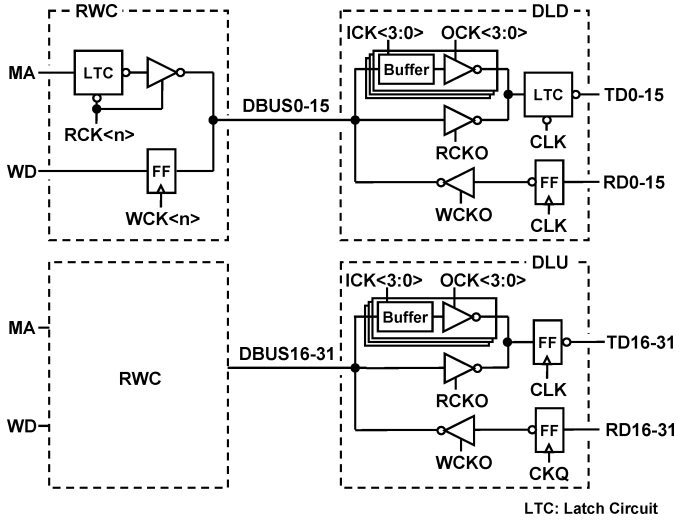


Fig. 9. Read/write circuits and data-latch circuits.

the output of the de-multiplexer (DEMUX), RD0-31, are transferred on DBUS by WCKO.

Fig. 10(a) shows the read timing diagram of the data bus. $\mathrm{RCK}\langle \mathrm{n} \rangle$ is activated in the second half of the clock cycle, and the data are transmitted on DBUS. In the I/O circuit, RCKO is activated at the same time. At the DLD, a latch is connected to the input of the multiplexer TD0 to TD15. The data at the input is valid delayed by the bus-delay after the CLK falls to "L". The timing margin of the multiplexer is kept long enough to accommodate the first clock phase, Φ_0. In the case that the write-data was transmitted on the bus while the CLK was "H", TD0 to TD15 are overwritten by the previous write-data and invalid soon after the CLK falls to "L". However, such invalid data are not generated in the continuous-read case because the previous read-data are left on the bus. At the DLU, a flip-flop is connected to the input of multiplexer TD16 to TD31. The data is received when the CLK rises to "H". The timing margin is also kept long enough to accommodate clock phase Φ_{16}. Because TD0 to TD31 are output according to the timing of $\Phi_0 - \Phi_{31}$, they have different setup time. In the case that the write command is received by the pipeline control circuit of the same bank right after the read command, ICK is activated instead of RCKO; as a result, the data on the DBUS is received by the delayed buffer. In the case that the read command is received while the delayed buffer has read data, OCK is activated instead of RCKO to transfer the data in the delayed buffer to a latch or a flip-flop.

Fig. 10(b) shows write timing diagram of the data bus. As a result of the de-multiplexing delay, the outputs of the de-multiplexer, RD0 to RD31, are delayed from each input clock from Φ_0 to Φ_{31}. In the DLD, the first half of the data on RD0 to RD15 is received by flip-flops according to CLK. The second half of the data on RD16 to RD31 are received by flip-flops according to delayed clock CKQ generated by DLL. Data in the flip-flops are transmitted on the DBUS only in the first half of the cycle according to WCKO, which synchronously rises with CKQ. In BANK-n, write data is received according to $\mathrm{WCK}\langle \mathrm{n} \rangle$, and write operation is started.

B. Early-Bar-Write Scheme for 8-ns Cycle DRAM Memory Array

To reduce cycle time of DRAM-array operation, it is critical to reduce write time because the full bit-line voltage (V_{DL}) must be written into a storage capacitor through a minimum-sized MOS transistor in a memory cell during the write cycle. For that purpose, an early write scheme (EW) is often used [8]. However, the EW scheme causes a coupling noise problem. When a target bit-line pair, $\mathrm{B_{LW}}$ and $/\mathrm{BL_W}$ in Fig. 11(a) are written to V_{DL} and V_{SS}, respectively, by activating a column select line (YS), the voltage swing of $\mathrm{BL_W}$ causes a coupling noise on the adjacent bit lines, $\mathrm{BL_R}$, before sensing as shown in Fig. 11(b). This noise reduces the signal on $\mathrm{BL_R}$ during restore operation for an adjacent storage-node, $\mathrm{SN_R}$ and makes array operation unstable. In a folded bit-line array, the coupling noise is canceled

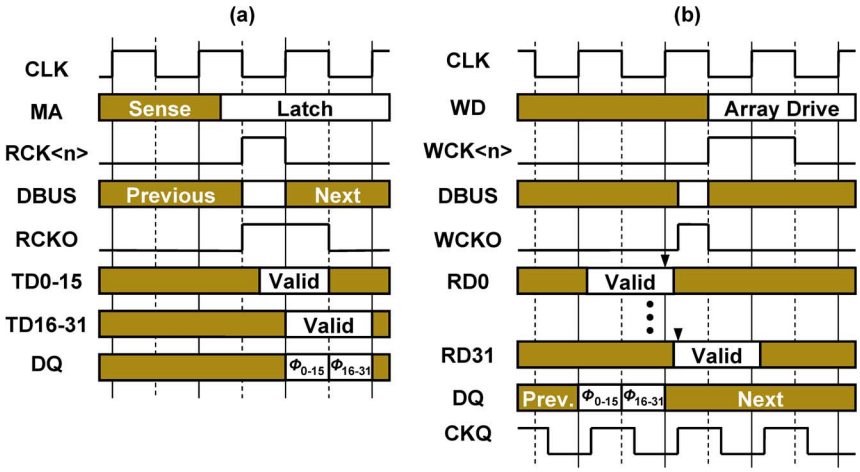


Fig. 10. Data-bus timing diagram: (a) read sequence and (b) write sequence.

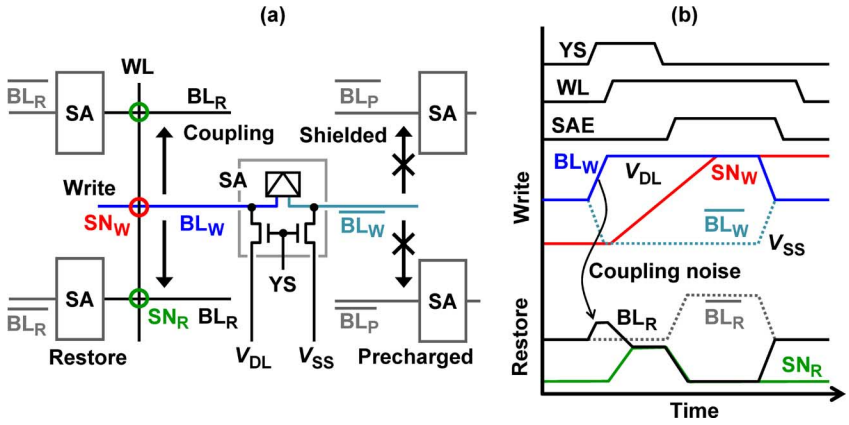


Fig. 11. Conventional early-write scheme: (a) memory array circuits and (b) waveform.

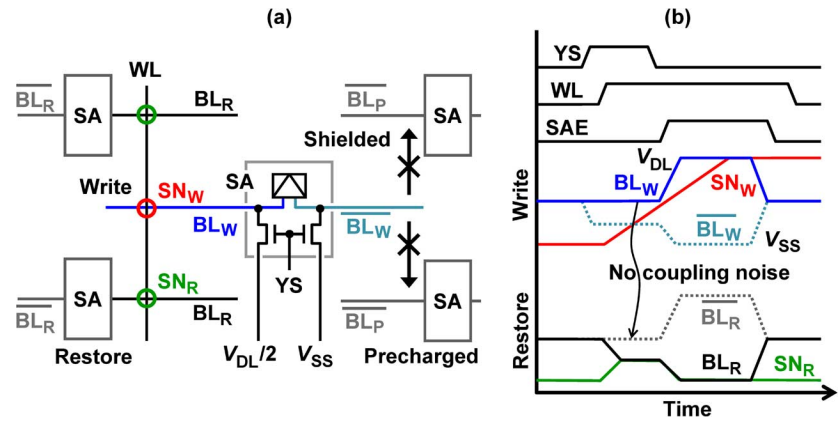


Fig. 12. Proposed early-bar-write scheme: (a) memory array circuits and (b) waveform.

by bit-line twisting. However, in a $4F^2$ open bit-line array, $\mathrm{BL_W}$ and its compliment $/\mathrm{BL_W}$ are located on opposite sides of SA, as shown in the figure, so bit-line twist cannot be applied.

To solve this coupling-noise issue in regard to an open bit-line array, an early-bar-write (EBW) scheme was devised (Fig. 12). In this scheme, as in the EW scheme, YS is activated before a word line, WL; however, the data is written only on $/\mathrm{BL_W}$ while $\mathrm{BL_W}$ is held at half V_{DL}. That causes no coupling noise on adjacent bit line $\mathrm{BL_R}$ before sense-amplifier-enable signal (SAE). The voltage swing of $/\mathrm{BL_W}$ does not affect operation of adjacent cells because adjacent $/\mathrm{BL_P}$'s are pre-charged and the coupling noise is shielded in open bit-line arrays with alternately placed SAs. In the final stage of the array operation, $\mathrm{BL_W}$ swings after activation of SAE. Data on $\mathrm{BL_W}$ are written into $\mathrm{SN_W}$ of the selected cell at the same time as the restore operation in $\mathrm{SN_R}$ of adjacent cells. Moreover, the pre-sensing of adjacent SAs through a common source node is avoided by limiting the amplitude on the written bit line to about 50% by means of sharing the charge between the I/O line and the bit line. The high-voltage level is further limited by the small conductance of nMOS column switch.

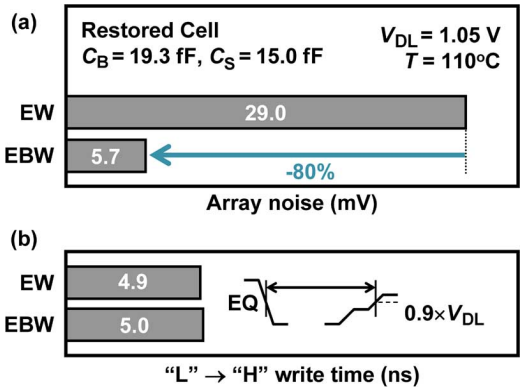


Fig. 13. (a) Memory-array noise and (b) write time in conventional early write and proposed early bar write.

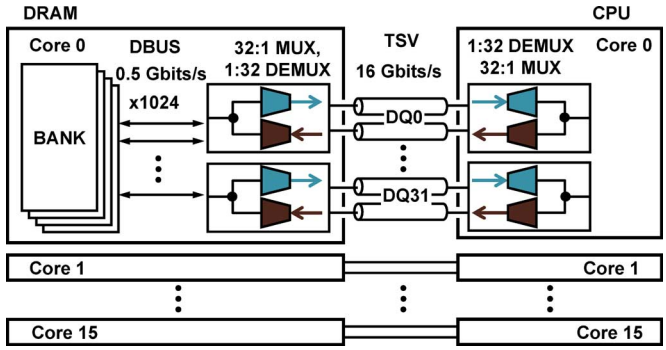


Fig. 14. Structure of 1-Tbyte/s I/O circuit.

With attention paid to the restored cell adjacent to the written cell, memory-array noises during EW and EBW operations were calculated. An open bit-line memory-array model with the parasitic capacitance and resistance in a memory-cell structure of 45-nm process has been created based on the analytical scheme reported before [11]. The model assumes a hierarchical bit-line architecture using $4F^2$ cell, and the lengths of the global bit line and local bit line are 256 cells and 64 cells, respectively. Short bit-line length causes small bit-line capacitance $C_{\rm B}$ (including the capacitance of the sense amplifier) of 19.3 fF. Cell capacitance $C_{\rm S}$ is assumed to be 15.0 fF. The bit-line amplitude $V_{\rm DL}$, the peripheral circuit voltage $V_{\rm DD}$, temperature are assumed to be 1.05 V, 1.35 V, and 110°C, respectively. The write and restoring operations are repeatedly simulated for both operations by reducing the initial storage-node voltage at $\rm SN_R$. Array noise is calculated as the critical signal voltage necessary on $\rm BL_R$ for successful sensing in the coupling-noise worst data-pattern. The proposed EBW scheme reduces array noise from 29.0 to 5.7 mV as shown in Fig. 13(a). Write time is defined as duration from the termination of sense-amplifier equalization to the time when $0.9 \times V_{\rm DL}$ is written to the originally "L" store cell. Fig. 13(b) shows the EBW scheme has no considerable degradation of write time in comparison with the EW scheme. Moreover, the EBW does not have an area penalty concerning the sense amplifier because it uses no additional MOS transistors.

C. Bidirectional and Differential Input and Output Circuits With TSVs

Fig. 14 shows the structure of a 1-Tbyte/s I/O circuit. The I/O circuits consist of 32-to-1 multiplexers (MUX), 1-to-32 de-multiplexers (DEMUX), and TSVs. A DBUS with 1024 lines is connected to 32 MUXs and four banks. A MUX connects one pair of TSVs and 32 lines of DBUS. 32 pairs of TSVs connect a DRAM core and a CPU core. A bidirectional and differential DQ is realized by using a pair of TSVs. Operation of 1024-bits DBUS at 0.5 Gbits/s by 16 cores results in 1-Tbyte/s throughput per chip. For data transfer of 32 bits in each 2-ns clock cycle, the DQ must support throughput of 16-Gbits/s per TSV.

The transmitter is divided into two stages, and consists of two 16-to-1 MUXs, a 2-to-1 MUX, and a delay-locked loop (DLL), as shown in Fig. 15(a). These circuits, in which a unit interval (UI) is 62.5 ps, convert 32-bit parallel data with a speed of 0.5 Gbits/s into differential serial data with speed of 16 Gbits/s. $\rm CKT\langle 15{:}0\rangle$ is a group of 2-ns-cycle-clock signals with positive period of 2UI and 16 equally separated phases. $\rm CKM\langle 1{:}0\rangle$ is a pair of complimentary clock signals which have a cycle of 4UI and transition timing shifted by 1UI from that of $\rm CKT\langle 15{:}0\rangle$. $\rm CKT\langle 15{:}0\rangle$ activates the former 16-to-1 MUX, and $\rm CKM\langle 1{:}0\rangle$ activates the latter 2-to-1 MUX. Through TSV, TD0 to TD31 are transmitted in phases Φ_0 to Φ_{31}. This circuit technique allows pulse widths of 2-UI in $\rm CKT\langle 15{:}0\rangle$ and $\rm CKM\langle 1{:}0\rangle$ and, thus, results in stable operation of the transmitter.

IO pins are assumed to be TSVs made of copper arranged at 50-μm pitch. Diameter and length of a TSV and thickness of dielectric are shown schematically in Fig. 16(a). An equivalent circuit of a pair of TSVs is shown in Fig. 16(b). The circuit model parameters (including resistance, self-inductance, capacitance to substrate, coupling capacitance, and mutual inductance) were calculated in accordance with [12].

IV. 45-nm 1-Gbit DRAM Chip Design

A floor plan of a 45-nm 1-Gbit DRAM chip based on the proposed circuit techniques is shown in Fig. 17. The chip is divided into 16 DRAM cores. Each DRAM core consists of four memory banks. TSVs are employed for command/address, data, and power supply. The memory cell array (MCA) consists of small 64-kbit sub-arrays with $4F^2$ cells and hierarchical bit-line architecture. These small sub-arrays decrease bit-line capacitance and thus enable high-speed array operation. To utilize the open bit-line array, a half of the bit-lines in the sub-arrays at bank-edges are not used and precharged to half $V_{\rm DL}$ [13].

The chip size is estimated to be 51.6 $\rm mm^2$. Area-occupancy ratio of each circuit component is shown in Fig. 18. The ratio for the memory cell array is 16.5%, which is lower than that of the stand-alone DRAM. Using short bit-line length for high-speed memory-array operation increases the area of the array peripheral circuits including a local bit-line switch and sense amplifier. The multi-core architecture also has an area overhead due to plural I/O circuits, including TSV and multiplexer, and core control circuits. However, utilizing $4F^2$ stand-alone DRAM cell, a cache memory with about 5 times higher density than embedded DRAM can be achieved.

Simulated waveforms with parasitic components based on the floor plan in Fig. 17 represent a throughput of 1 Tbyte/s

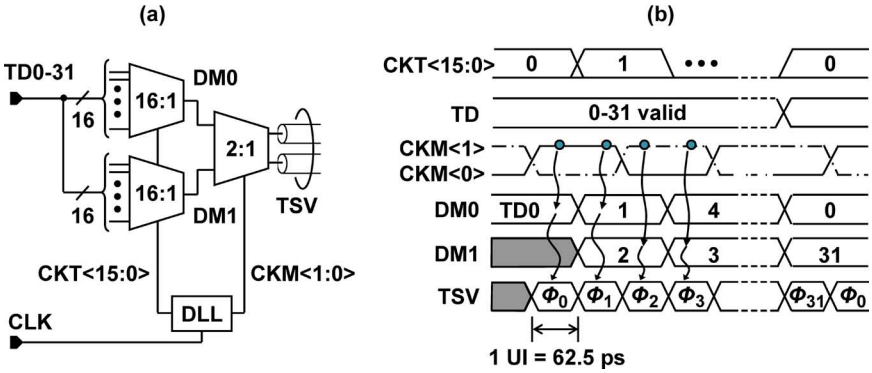


Fig. 15. Transmitter architecture: (a) schematic and (b) timing diagram.

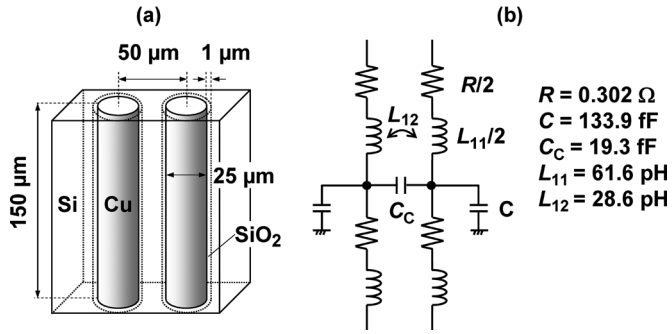


Fig. 16. Differential TSV I/O: (a) structure and (b) equivalent circuits.

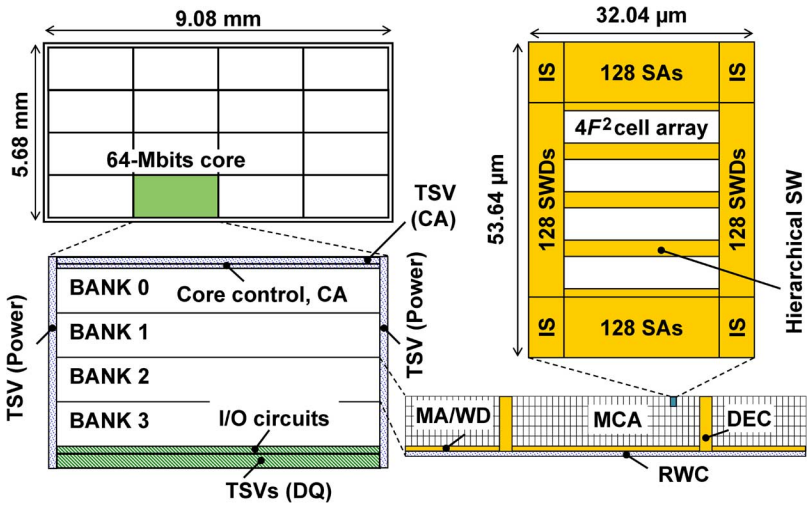


Fig. 17. Floor plan of 45-nm 1-Gbit chip.

under the condition of $V_{\mathrm{DD}} = 1.35$ V, $V_{\mathrm{DL}} = 1.05$ V, and $T = 110°\mathrm{C}$ as shown in Fig. 19. In BANK3, using an early-bar-write scheme realizes successful 8-ns-cycle write and read operations. In the DBUS, gapless operation of *BANK3-read* and *BANK2-write* was simulated in cycles 6 and 7. The mean power consumption is estimated to be 19.5 W per chip, as shown in Fig. 20. I/O circuit consumes 40%, and core-control circuits, CA, and RWC with DBUS consume 48% of the total power of the chip. The proposed multi-core DRAM achieves power efficiency of 51.3 Gbytes/s/W, which is improved by an order of the magnitude compared with that of conventional DRAMs as shown in Fig. 2.

V. Summary

A novel 3D-integrated multi-core DRAM architecture on a multi-core CPU chip based on TSV technology and core-to-core direct connection were proposed. A 1-Tbyte/s 1-Gbit DRAM architecture with power consumption of 19.5 W was demonstrated by a chip-level circuit simulation assuming a $4F^2$ stand-alone DRAM cell. This performance was achieved by three circuit techniques, namely, a five-stage pipelined core for 2-ns cycle bus; an early-bar-write scheme for 8-ns cell array cycle; and a two-stage multiplexer circuit for data rate of 16 Gbits/s per differential TSV pair. Designed chip size is 51.6 mm^2 assuming

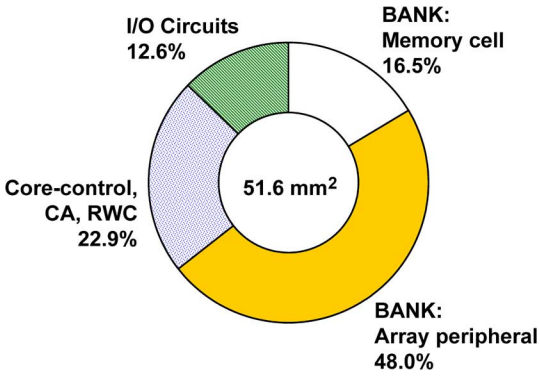


Fig. 18. Area-occupancy ratio of each circuit component (calculated based on 45-nm stand-alone DRAM technology).

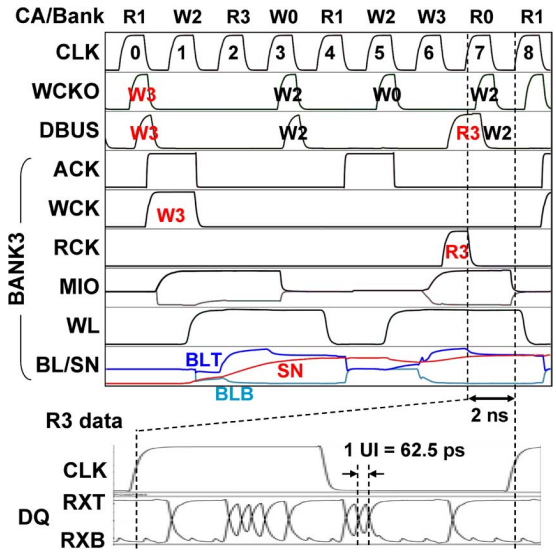


Fig. 19. Simulated waveform of DRAM core ($V_{\mathrm{DD}} = 1.35$ V, $V_{\mathrm{DL}} = 1.05$ V, $T = 110°$C).

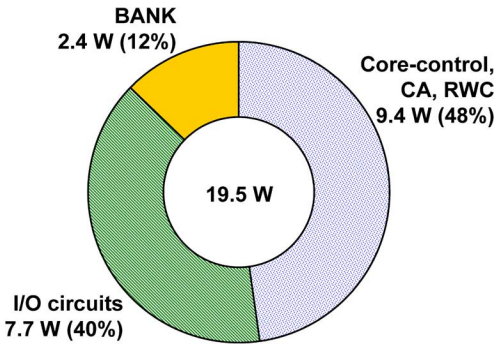


Fig. 20. Power consumption of chip ($V_{\mathrm{DD}} = 1.35$ V, $V_{\mathrm{DL}} = 1.05$ V, $T = 110°$C).

45 nm process, and the density is about 5 times higher than embedded DRAM. The proposed DRAM achieves power efficiency of 51.3 Gbytes/s/W, which is improved by an order of magnitude compared with that of conventional DRAMs.

ACKNOWLEDGMENT

The authors would like to thank N. Irie, H. Mizuno, K. Osada, M. Saen, and S. Miura for the discussion on 3-D integrated system, S. Akiyama and R. Takemura for the discussion of DRAM architectures, and K. Uchiyama, T. Kodama, J. Miyakoshi, A. Tomoda, and K. Ito for the comment on multi-core CPU system.

REFERENCES

[1] T. Ezaki, K. Kondo, H. Ozaki, N. Sasaki, H. Yonemura, M. Kitano, S. Tanaka, and T. Hirayama, "A 160 Gb/s interface design configuration for multichip LSI," in *IEEE ISSCC Dig. Tech. Papers*, 2004, pp. 140–141.

[2] M. Kawano, S. Uchiyama, Y. Egawa, N. Takahashi, Y. Kurita, K. Soejima, M. Komuro, S. Matsui, K. Shibata, J. Yamada, M. Ishino, H. Ikeda, Y. Saeki, O. Kato, H. Kikuchi, and T. Mitsuhashi, "A 3-D packaging technology for 4 Gbit stacked DRAM with 3 Gbps data transfer," in *IEDM Dig. Tech. Papers*, 2006, pp. 581–584.

[3] S. Borkar, "3D integration for energy efficient system design," in *Symp. VLSI Technology Dig. Tech. Papers*, 2009, pp. 58–59.

[4] H. Saito, M. Nakajima, T. Okamoto, Y. Yamada, A. Ohuchi, N. Iguchi, T. Sakamoto, K. Yamaguchi, and M. Mizuno, "A chip-stacked memory for on-chip SRAM-rich SoCs and processors," in *IEEE ISSCC Dig. Tech. Papers*, 2009, pp. 60–61.

[5] K. Takeda, T. Saito, S. Asayama, Y. Aimoto, H. Kobatake, S. Ito, T. Takahashi, K. Takeuchi, M. Nomura, and Y. Hayashi, "Multi-step word-line control technology in hierarchical cell architecture for scaled-down high-density SRAMs," in *Symp. VLSI Circuits Dig. Tech. Papers*, 2010, pp. 101–102.

[6] J. Barth, D. Plass, E. Nelson, C. Hwang, G. Fredeman, M. Sperling, A. Mathews, W. Reohr, K. Nair, and N. Cao, "A 45 nm SOI embedded DRAM macro for POWER7 32 MB on-chip L3 cache," in *IEEE ISSCC Dig. Tech. Papers*, 2010, pp. 342–343.

[7] K. Ono, A. Kotabe, Y. Yanagawa, and T. Sekiguchi, "1-Tbyte/s 1-Gbit DRAM architecture with micro-pipelined 16-DRAM cores, 8-ns cycle array and 16-Gbit/s 3-D interconnect for high throughput computing," in *Symp. VLSI Circuits Dig. Tech. Papers*, 2010, pp. 187–188.

[8] J. Barth, D. Anand, S. Burns, J. Dreibelbis, J. Fifield, K. Gorman, M. Nelms, E. Nelson, A. Paparelli, G. Pomichter, D. Pontius, and S. Sliva, "A 500-MHz multi-banked compilable DRAM macro with direct write and programmable pipelining," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 213–222, Jan. 2005.

[9] N. Madan, Z. Li, N. Muralimanohar, A. Udipi, R. Balasubramonian, R. Iyer, S. Makineni, and D. Newell, "Optimizing communication and capacity in a 3-D stacked reconfigurable cache hierarchy," in *Symp. IEEE High Performance Computer Architecture (HPCA)*, 2009, pp. 262–274.

[10] K. Song, J. Kim, H. Kim, H. Chung, H. Kim, K. Kim, H. Park, H. Kang, S. Kim, N. Tak, D. Park, W. Kim, Y. Lee, Y. Oh, G. Jin, J. Yoo, K. Oh, C. Kim, and W. Lee, "A 31 ns random cycle VCAT-based $4F^2$ DRAM with enhanced cell efficiency," in *Symp. VLSI Technology Dig. Tech. Papers*, 2009, pp. 132–133.

[11] T. Sekiguchi, K. Itoh, T. Takahashi, M. Sugaya, H. Fujisawa, M. Nakamura, K. Kajigaya, and K. Kimura, "A low-impedance open bit-line array for multi-gigabit DRAM," *IEEE J. Solid-State Circuits*, vol. 37, no. 4, pp. 487–498, Apr. 2002.

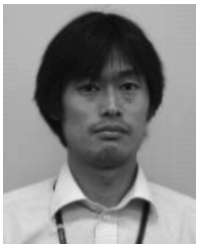
[12] I. Savidis and E. Friedman, "Closed-form expressions of 3-D via resistance, inductance, and capacitance," *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 1873–1881, Sep. 2009.

[13] M. Inoue, T. Yamada, H. Kotani, H. Yamauchi, A. Fujiwara, J. Matsushima, H. Akamatsu, M. Fukumoto, M. Kubota, I. Nakao, N. Aoi, G. Fuse, S. Ogawa, S. Odanaka, A. Ueno, and H. Yamamoto, "A 16-Mbit DRAM with a relaxed sense-amplifier-pitch open-bit-line architecture," *IEEE J. Solid-State Circuits*, vol. SC-23, no. 5, pp. 1104–1112, Oct. 1988.

Tomonori Sekiguchi (M'93) received the B.S. degree in physical electronics and the M.S. degree in electrical and electronic engineering, both from the Tokyo Institute of Technology, Tokyo, Japan, in 1991 and 1993, respectively.

He joined the Central Research Laboratory of Hitachi Ltd., Tokyo, in 1993. Since then, he was engaged in the research of DRAMs. He was a visiting researcher at the Integrated Systems Laboratory, Swiss Federal Institute of Technology Zürich (ETH), from 2002 to 2003. He has been temporally transferred to European R&D Centre of Hitachi Europe Ltd., Maidenhead, U.K., from 2010.

Mr. Sekiguchi is a member of the Institute of Electronics, Information and Communication Engineers of Japan. He served as a member of the program committee of the Symposium on VLSI Circuits from 2006 to 2010.



Kazuo Ono was born in Shizuoka, Japan, in 1978. He received the B.E., M.E., and D.E. degrees from the University of Tokyo, Tokyo, Japan, in 2001, 2003, and 2006, respectively.

In 2006, he joined Hitachi Ltd. Central Research Laboratory, Tokyo, where he has been engaged in the research and development of emerging memory technology.

Dr. Ono won the Young Researcher Award of the SSDM 2009.

Akira Kotabe received the B.E. and M.E. degrees from the Department of Information and System Engineering, Chuo University, Tokyo, Japan, in 1999 and 2001, respectively.

In 2001, he joined the Central Research Laboratory, Hitachi, Ltd., Tokyo, Japan, where he has been engaged in the research and development of low-power circuits for high-density MOS memories.

Mr. Kotabe is a member of the Institute of Electronics Information and Communication Engineers of Japan.

Yoshimitsu Yanagawa received the B.S., M.S., and Ph.D. degrees in electronic engineering from The University of Tokyo, Tokyo, Japan, in 2003, 2005, and 2008, respectively.

In 2008, he joined the Central Research Laboratory, Hitachi, Ltd., Tokyo, Japan, where he has been engaged in the research and development of low-noise circuits for high-density commodity DRAMs.

Dr. Yanagawa is a member of the Institute of Electronics Information and Communication Engineers of Japan.