Aror University of Art, Architecture, Design & Heritage Sukkur.

BS (AI & MMG)
Fall-2025
Digital Logic Design Lab

Course Title: Digital Logic Design
Course Code: CSC214
Credit Hours: (2 Hours)
Course Instructor: Muzaffar Hussain
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Description:

- Digital Logic Design (DLD) is a branch of electronics that deals with the study and design of digital circuits—systems that use signals having only two states: 0 (Low / OFF), 1 (High / ON).
- It provides the foundation of modern computers, microprocessors, and digital systems. In this subject, we learn how basic electronic components, like logic gates, can be combined to perform logical decisions, arithmetic operations, data storage, and communication tasks.

Aims and Objectives:

- Analyze basic logic gates, Boolean algebra, and simplification techniques.
- Design combinational logic circuits such as adders, subtractors, multiplexers, demultiplexers, encoders, and decoders. .
- Construct sequential circuits such as latches, flip-flops, counters, and registers.
- Implement digital circuits using Karnaugh maps (K-maps) and other minimization techniques. Relate the use of digital logic to real-life applications in computer systems, communication, and AI.
- Utilize simulation tools and laboratory experiments to validate theoretical concepts in a practical setting.

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Week	Topic	Completion
1	To verify the truth tables of NOT, AND, and OR gates using ICs.	**10.00%**
2—3	To implement and verify Boolean expressions using logic gates.	**20.00%**
4	To design and verify Half Adder and Full Adder circuits.	**30.00%**
5 — 6	To simplify Boolean functions using K-maps and implement the simplified circuit.	**40.00%**
7	To implement a seven-segment display decoder using K-map simplification	**50.00%**
8	To implement and verify the truth tables of the Decoder and Encoder.	**60.00%**
	MID TERM	
9	To design and verify a 4-bit comparator circuit	**70.00%**
10 — 11	To design and verify Multiplexer (MUX) and Demultiplexer (DEMUX).	**80.00%**
12 — 13	To design and verify SR, JK, D, and T Flip-Flops.	**90.00%**
14	To design and verify 4-bit bidirectional shift register.	**100.00%**

15 / 16	To perform an Open-ended Lab	
FINAL TERM		