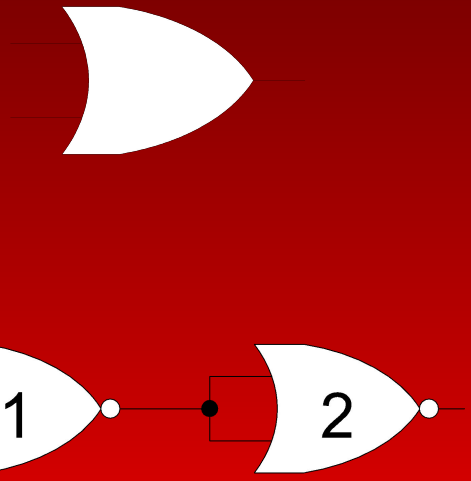
Digital Logic & Design

Dr. Waseem Ikram

Lecture 06

NOR Universal Gate

Input		Output
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1



NOR Universal Gate

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0	0	0
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1	0	0
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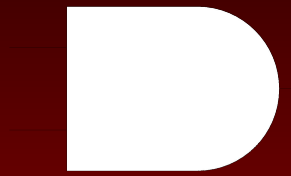
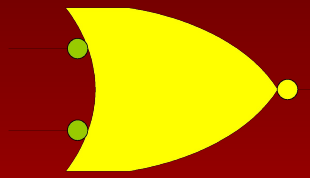
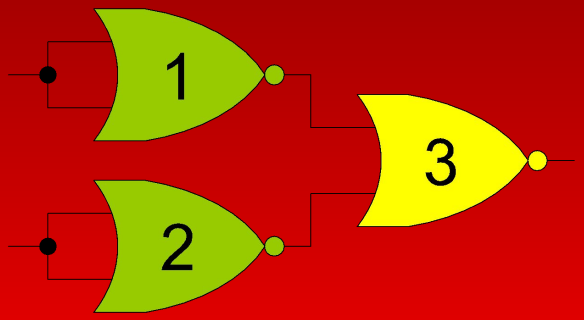
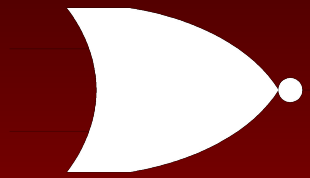
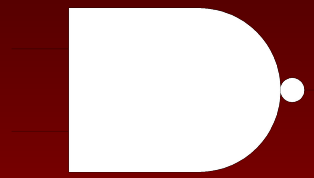


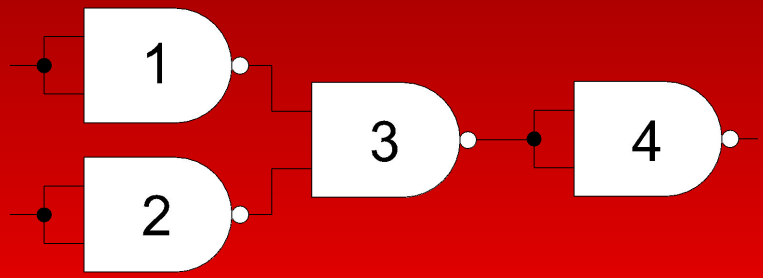


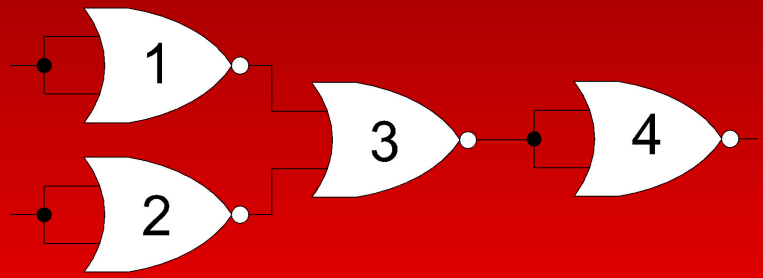


NAND-NOR Universal Gate



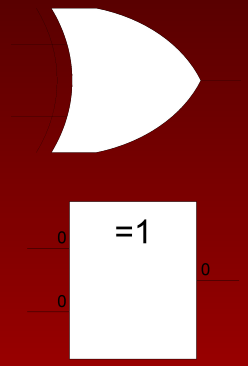






XOR Gate

- 1 output
- 2 inputs
- Multiple inputs

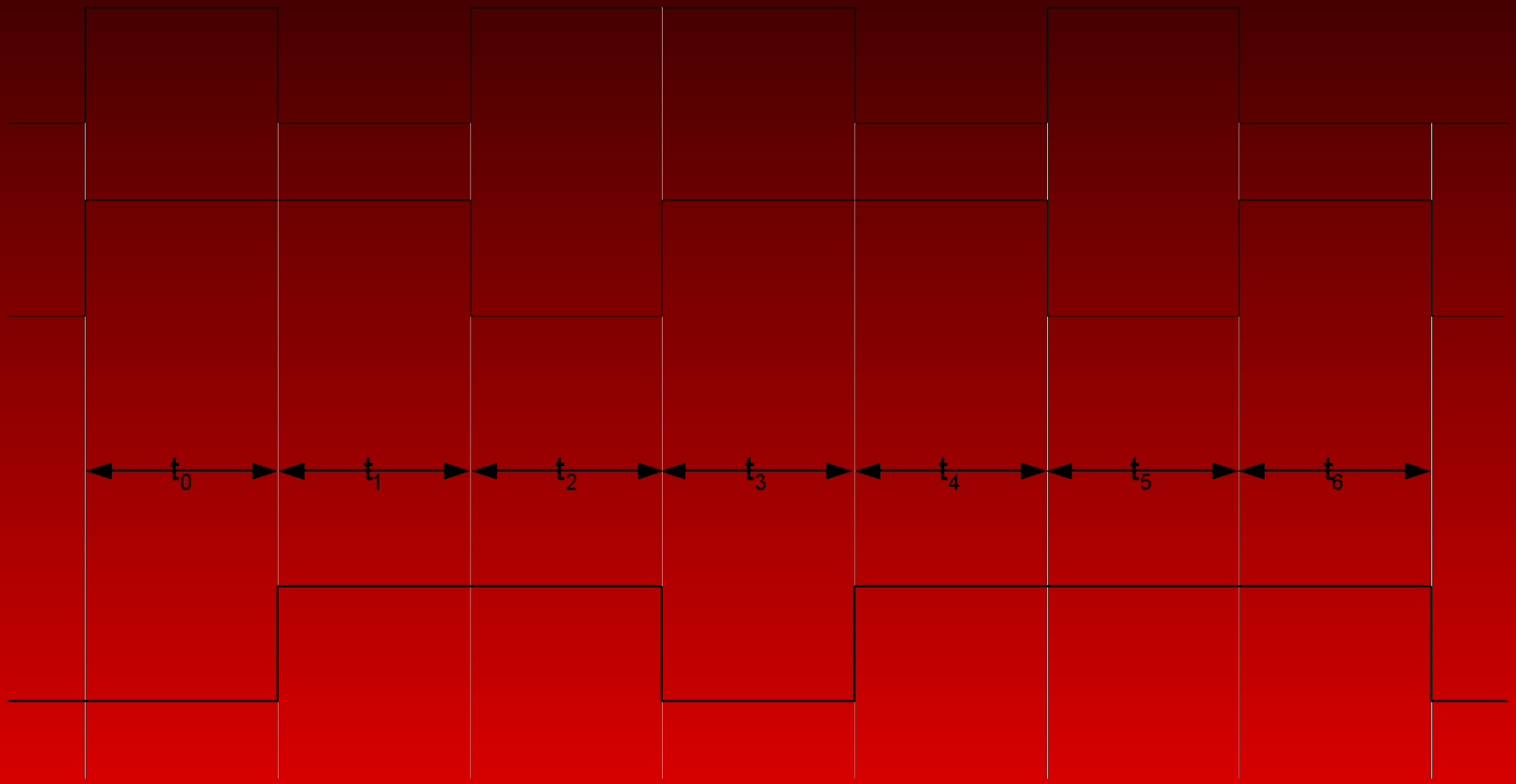


XOR Gate function

Input		Output
A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

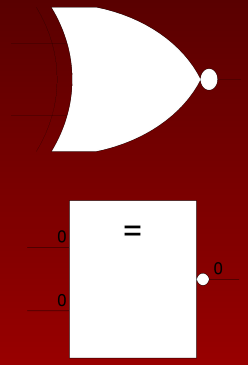
$$F = A \oplus B$$

XOR Gate Timing Diagram



XNOR Gate

- 1 output
- 2 inputs
- Multiple inputs



XNOR Gate function

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1	0	0
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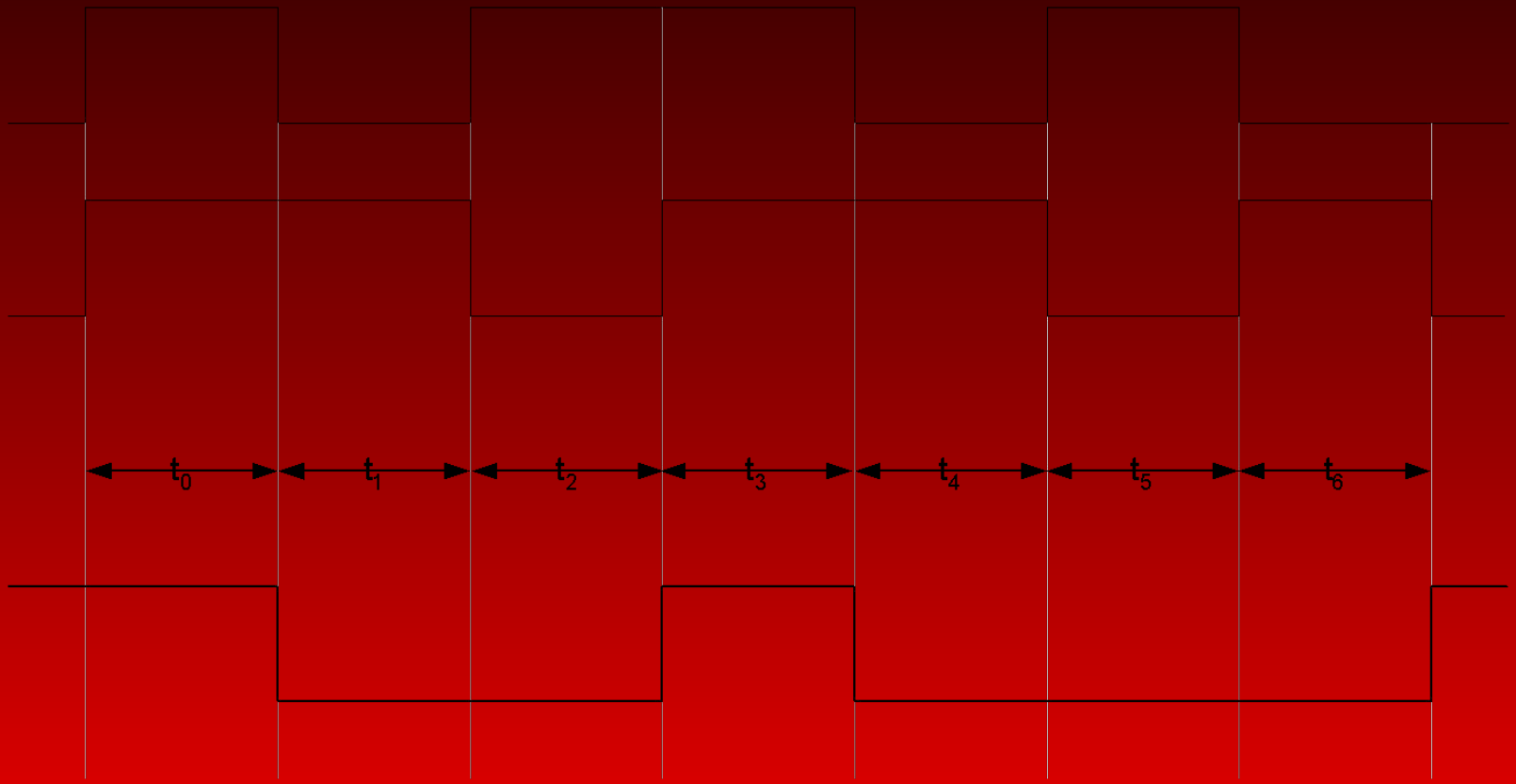
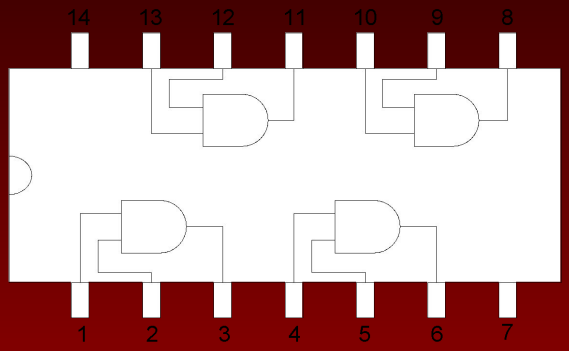
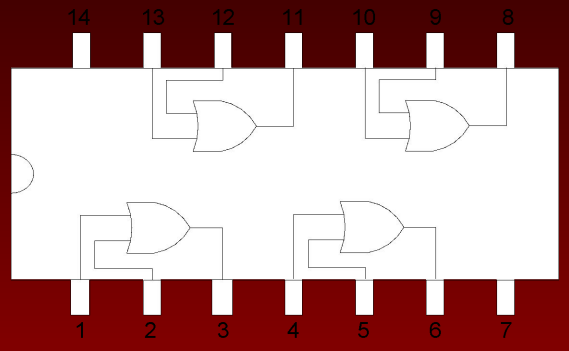
XNOR Gate Timing Diagram



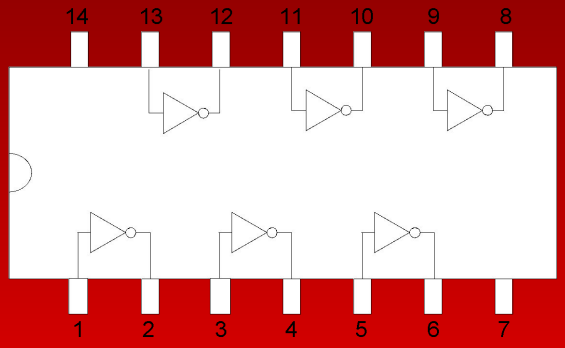
Logic Gate Integrated Circuits



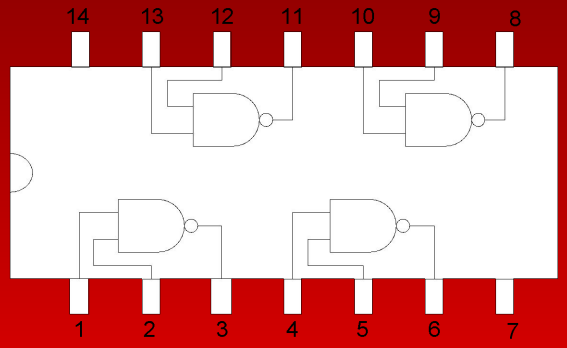
7408
Four 2-Input AND Gate



7432
Four 2-Input OR Gate

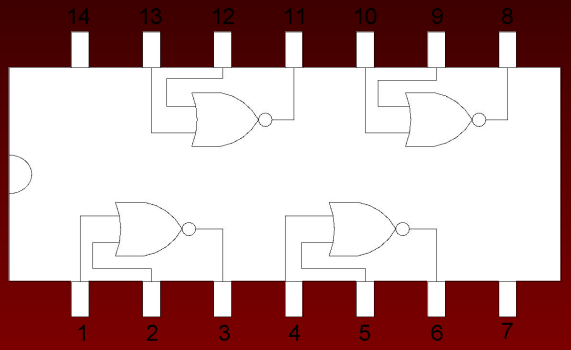


7404
Hex Inverters

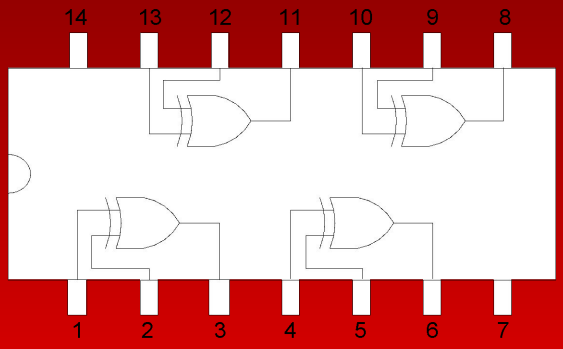


7400
Four 2-Input NAND Gate

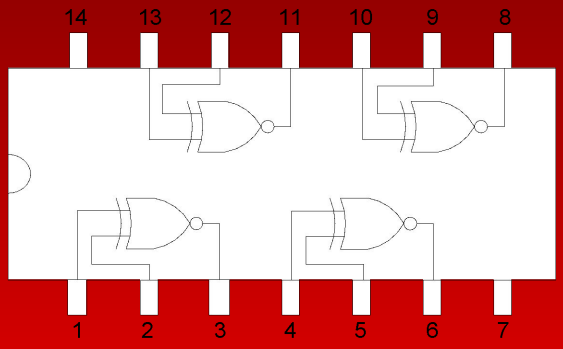
Logic Gate Integrated Circuits



7402
Four 2-Input NOR Gate



7486
Four 2-Input XOR Gate



74266
Four 2-Input XNOR Gate