

Lec 21 and 22 : Latches

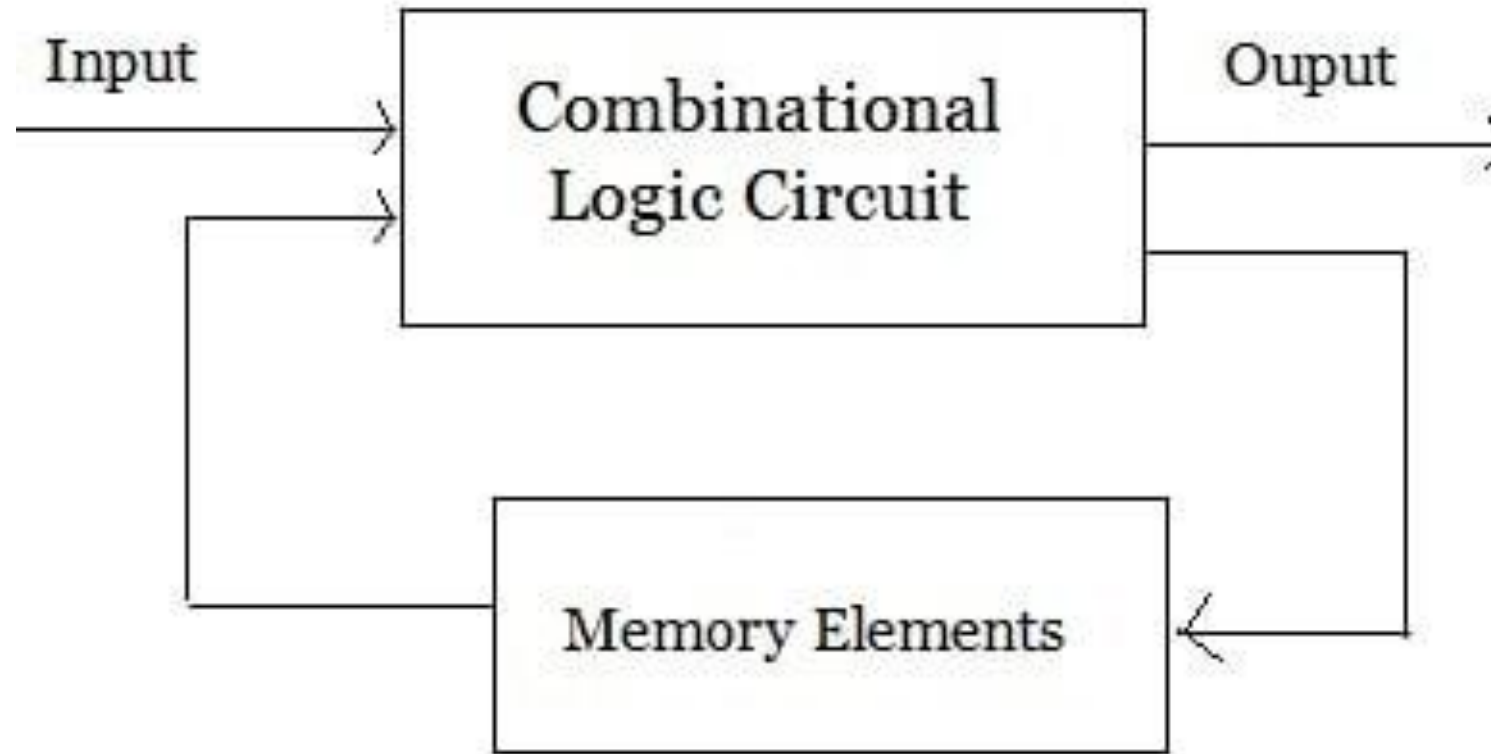
Abdul Ghafoor

Outline

After completing this section, you should be able to

- Explain the operation of a basic S-R latch
- Explain the operation of a gated S-R latch
- Explain the operation of a gated D latch
- Implement an S-R or D latch with logic gates
- Describe the 74HC279A latches

Sequential Circuit



Latches

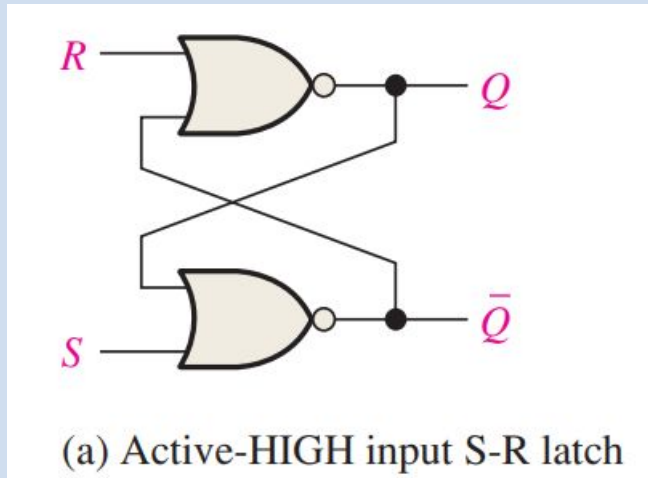
The latch is a type of temporary storage device that has two stable states (bistable).

Types of latches

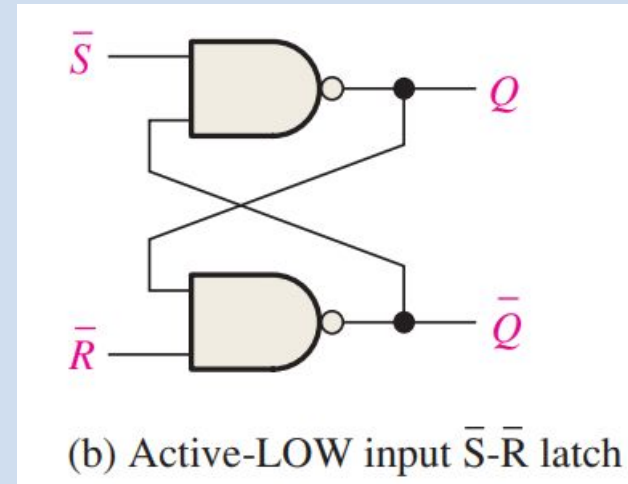
1. S-R Latch
2. D-Latch

The S-R (SET-RESET) Latch

An active-HIGH input S-R (SET-RESET) latch is formed with two cross-coupled NOR gates



an active-LOW input S-R latch is formed with two cross-coupled NAND gates



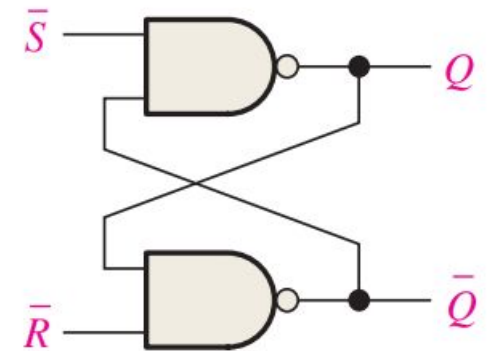
Notice that the output of each gate is connected to an input of the opposite gate. This produces the regenerative feedback that is characteristic of all latches and flip-flops.

The S-R (SET-RESET) Latch

- To explain the operation of the latch, we will use the NAND gate S@R latch

Truth table for an active-LOW input \bar{S} - \bar{R} latch.

Inputs		Outputs		Comments
\bar{S}	\bar{R}	Q	\bar{Q}	
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition



(b) Active-LOW input \bar{S} - \bar{R} latch

The S-R (SET-RESET) Latch : Example

If the \bar{S} and \bar{R} waveforms in Figure 7-5(a) are applied to the inputs of the latch in Figure 7-4(b), determine the waveform that will be observed on the Q output. Assume that Q is initially LOW.

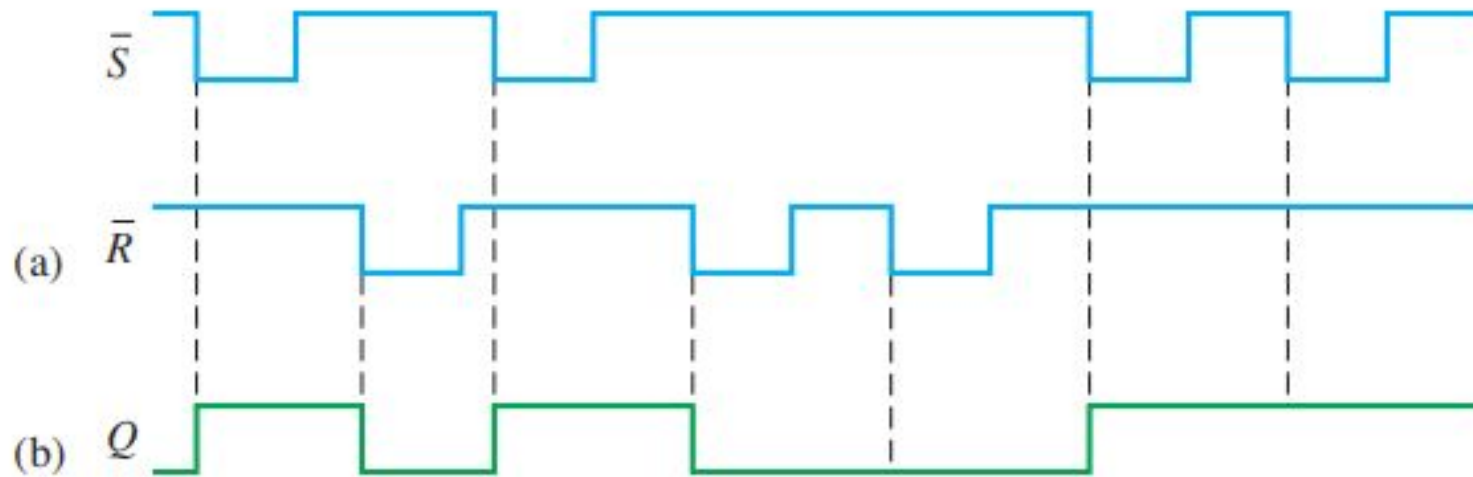
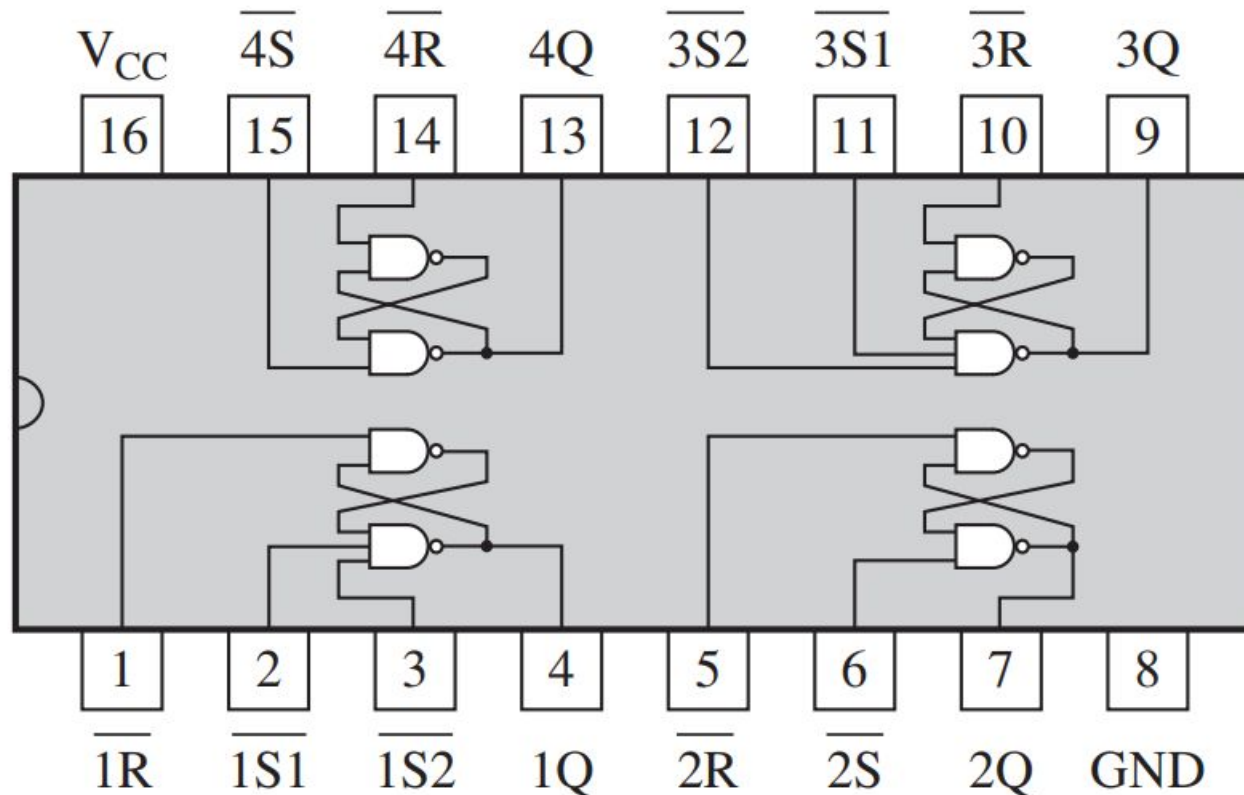


FIGURE 7-5

The S-R (SET-RESET) Latch

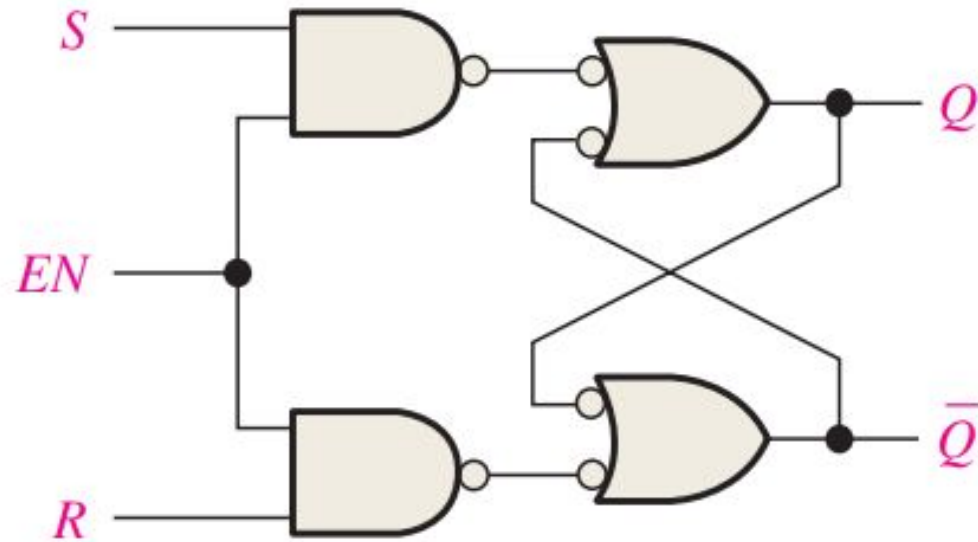
- The 74HC279A quad S-R latch (Logic diagram)



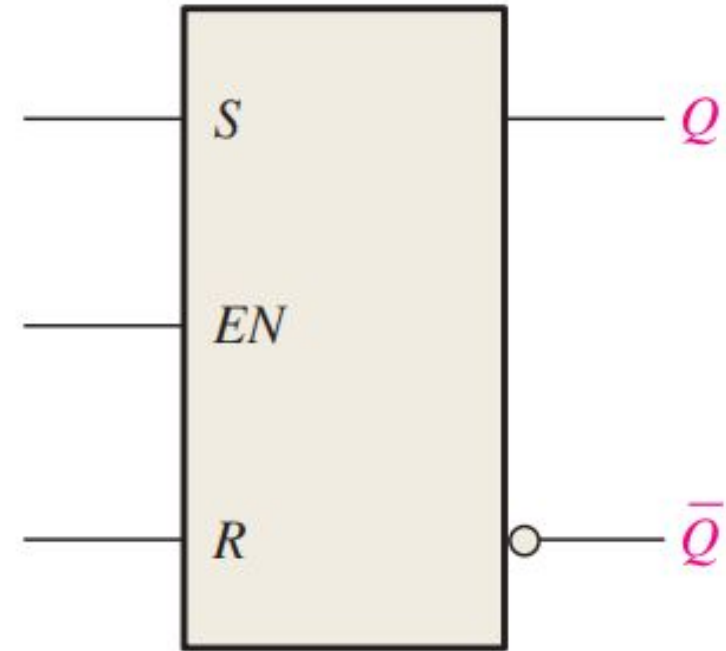
The Gated S-R Latch

- A gated latch has an additional input called the enable input (EN or G).
- The enable input controls whether the latch responds to changes in the S and R inputs.
- When the enable input is HIGH, the latch is enabled, meaning it can respond to changes in the S and R inputs.
- When the enable input is LOW, the latch is disabled, meaning it ignores changes in the S and R inputs, and its output remains unchanged.

The Gated S-R Latch



(a) Logic diagram



(b) Logic symbol

The Gated S-R Latch (Example)

Determine the Q output waveform if the inputs shown in Figure 7–9(a) are applied to a gated S-R latch that is initially RESET.

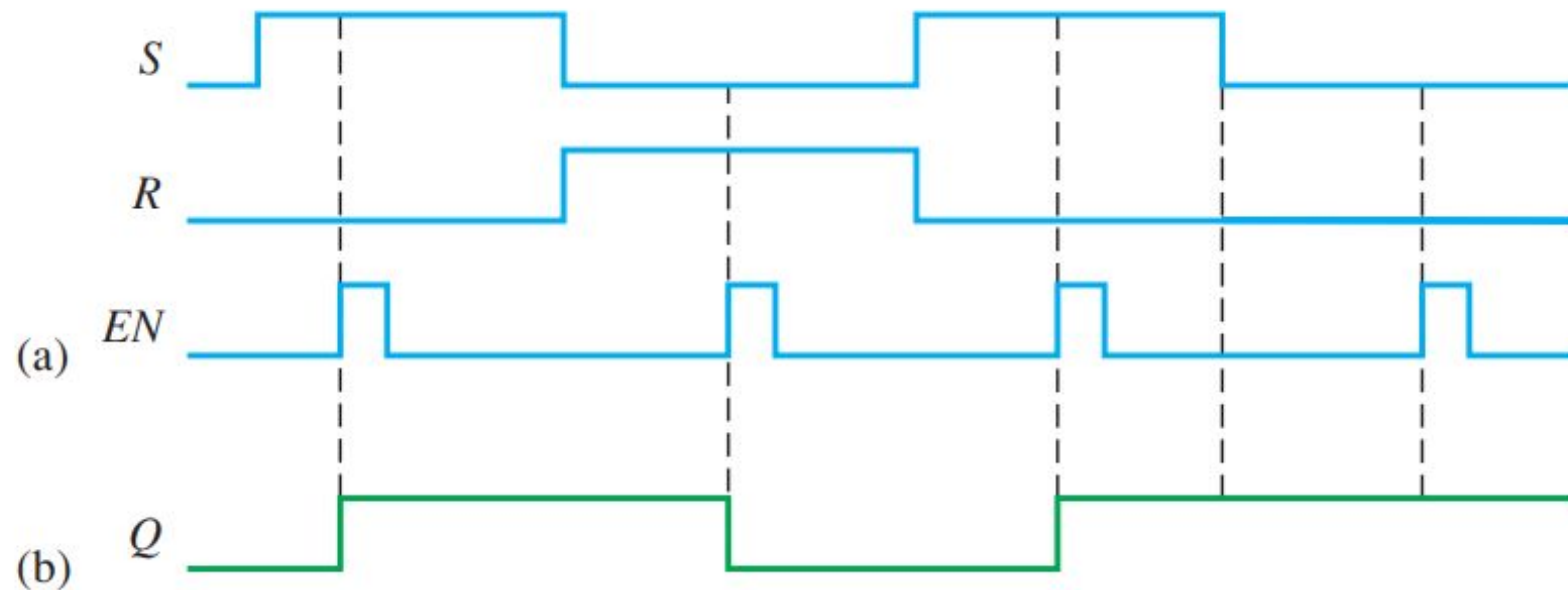


FIGURE 7–9

The Gated D Latch

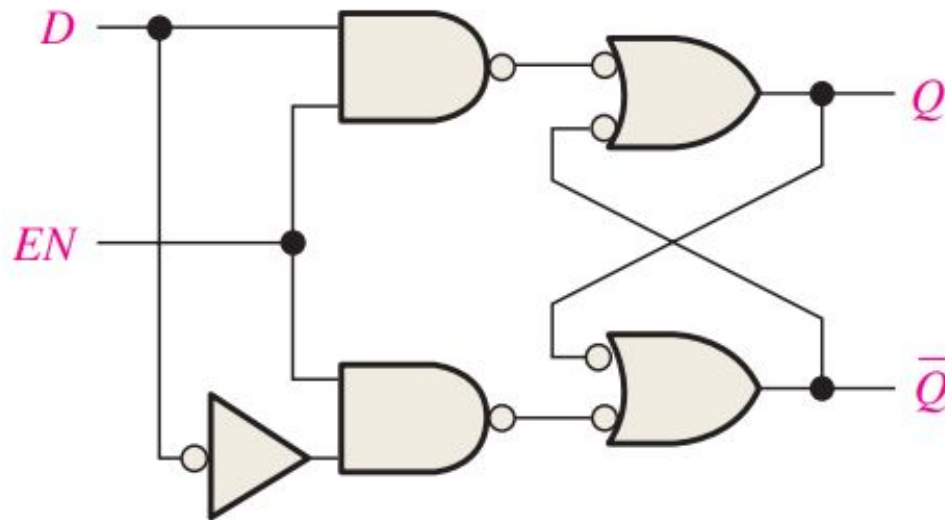
- A D latch is a type of gated latch that has only one input in addition to the enable input (EN or G).
- This input is called the D (data) input.
- Unlike an S-R latch, which has separate set and reset inputs, a D latch uses the D input to control its behavior.

The Gated D Latch (**Operation**)

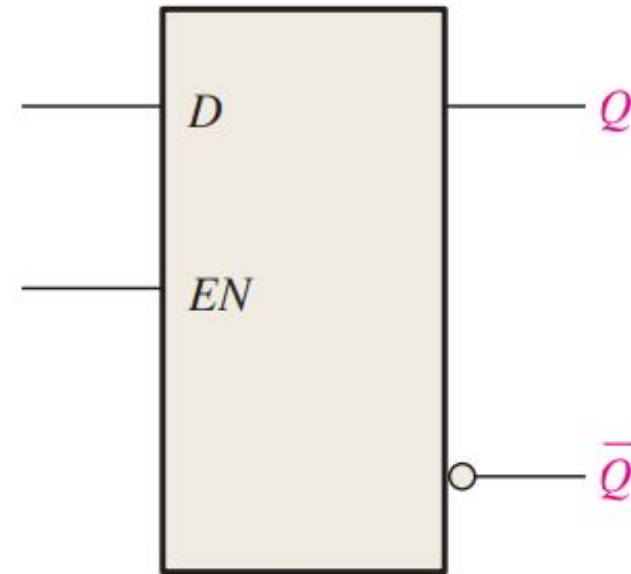
- When the D input is HIGH and the enable input (EN) is HIGH, the latch will set. This means that the output (Q) will become HIGH.
- When the D input is LOW and the enable input (EN) is HIGH, the latch will reset. This means that the output (Q) will become LOW.
- In other words, the output Q follows the input D when the enable input (EN) is HIGH.
- When the enable input (EN) is LOW, the latch is disabled, and it holds its previous state regardless of the input D.

The Gated D Latch

Inputs		Outputs		Comments
D	EN	Q	\bar{Q}	
0	1	0	1	RESET
1	1	1	0	SET
X	0	Q_0	\bar{Q}_0	No change



(a) Logic diagram



(b) Logic symbol

Quiz

1. List three types of latches.
2. Develop the truth table for the active-Low input S-R latch.
3. What is the Q output of a D latch when $EN = 1$ and $D = 1$?