Digital Logic & Design

Mr. Abdul Ghafoor

Lecture 05

Recap

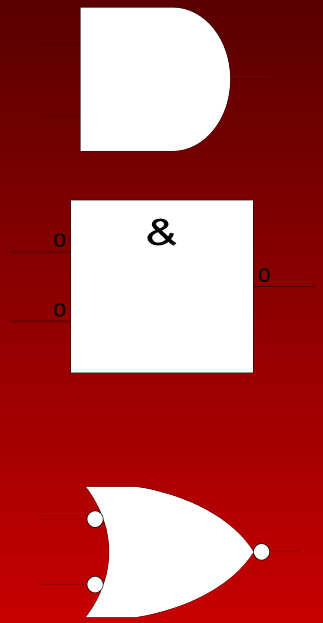
- Number System
- Alternate Representations
  - BCD Code
  - Gray Code
- Alphanumeric Code (ASCII)
- Error Detection using Parity Bit

Logic Gates

- Basic Building Blocks
- Logic Gate Symbol
- Unique function
- Truth or Function Table
- Function Expression
- Timing Diagram

AND Gate

- 1 output
- 2 inputs
- 3 inputs
- 4 inputs
- Multiple inputs



AND Gate function

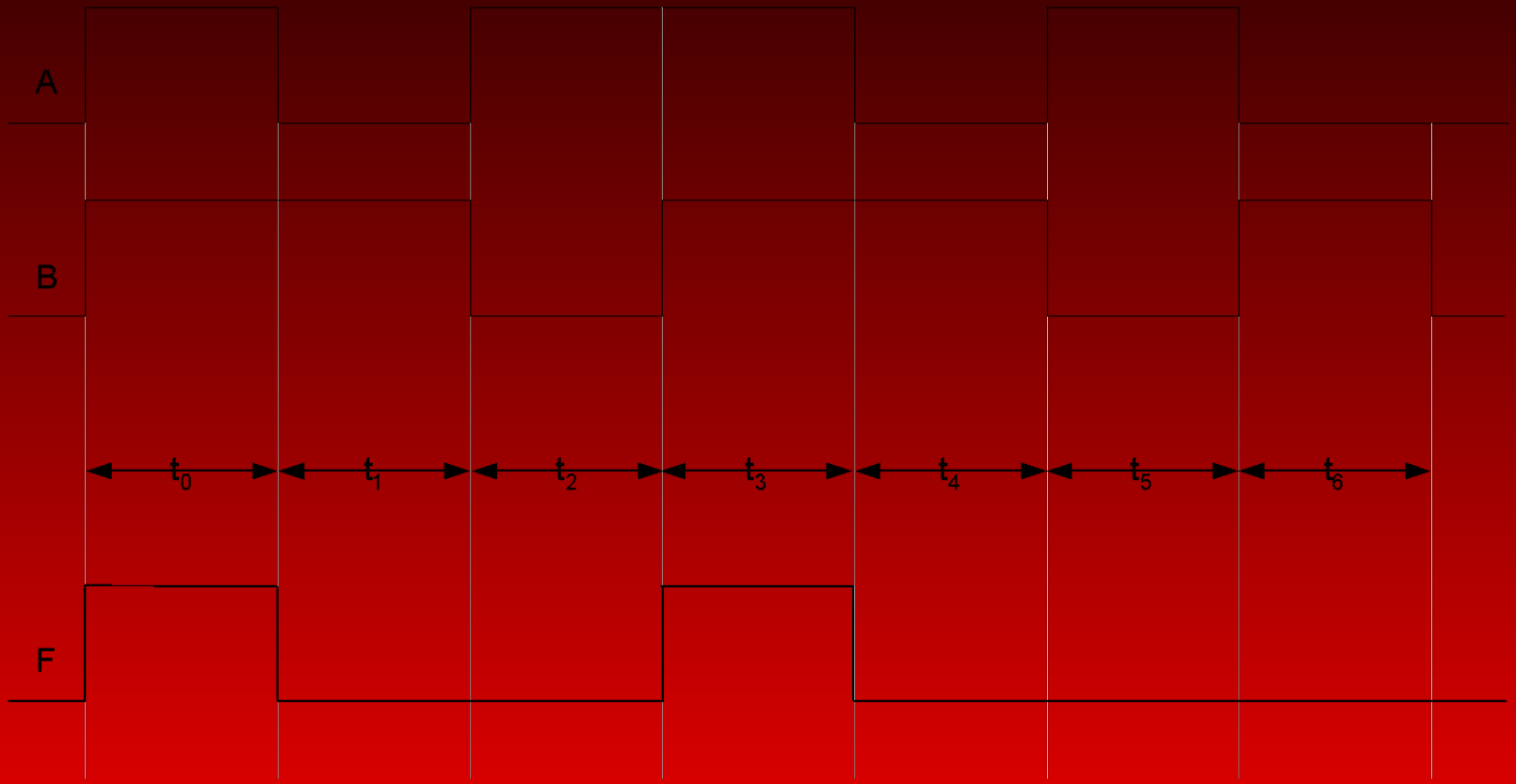
- Logical Multiplication function

Input		Output
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

$$F = A \bullet$$

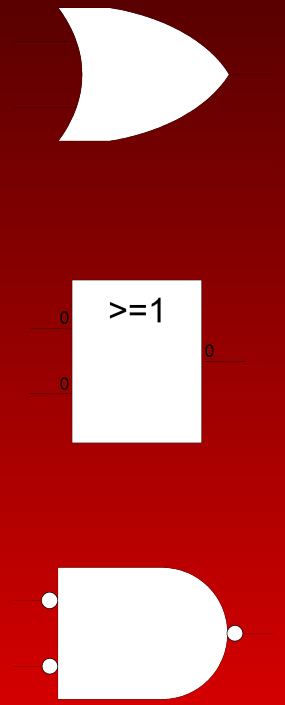
$$F = A \bullet B \bullet C \bullet \ldots$$

AND Gate Timing Diagram



OR Gate

- 1 output
- 2 inputs
- 3 inputs
- 4 inputs
- Multiple inputs



OR Gate function

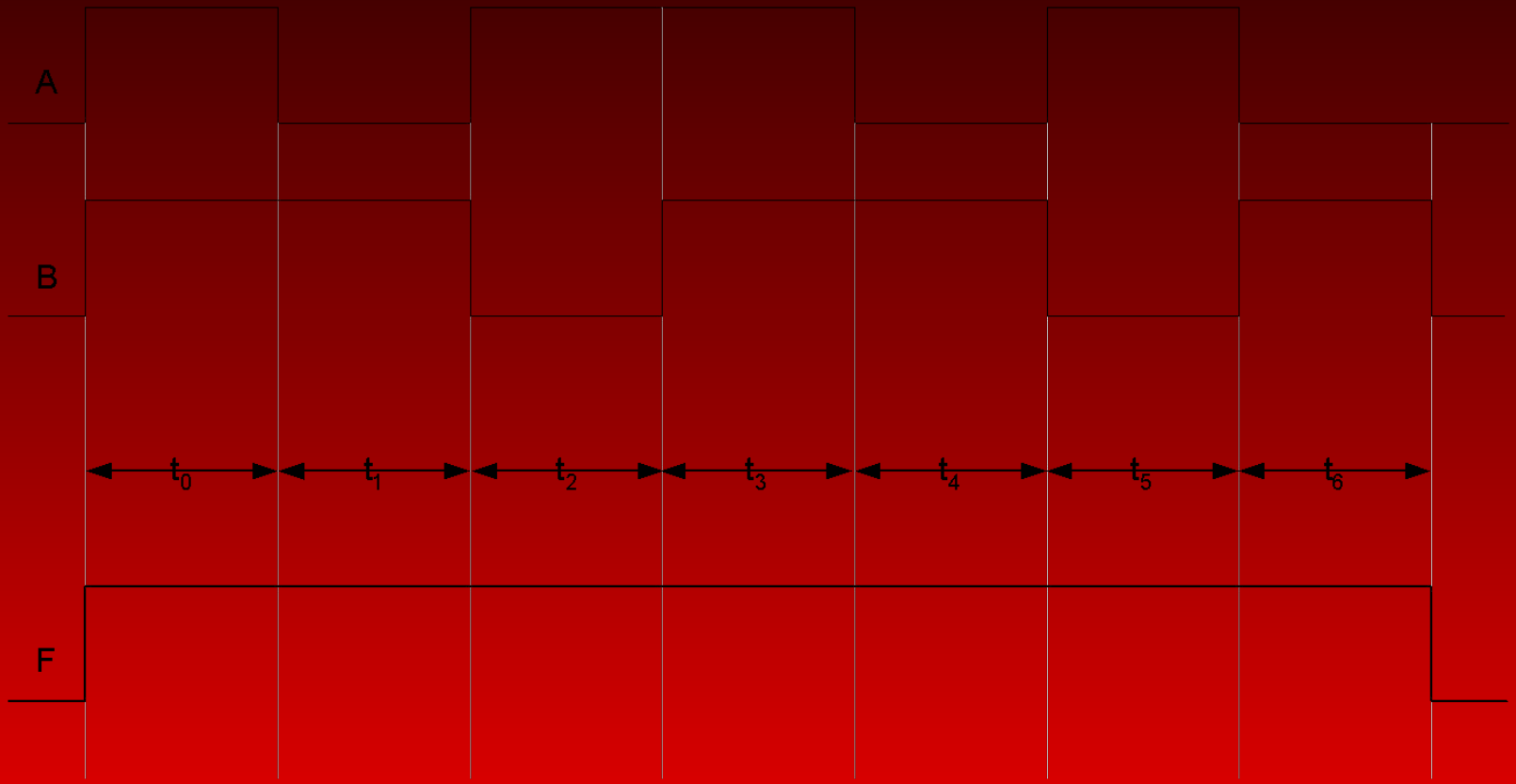
- Boolean Add function

Input		Output
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

$$F = A +$$

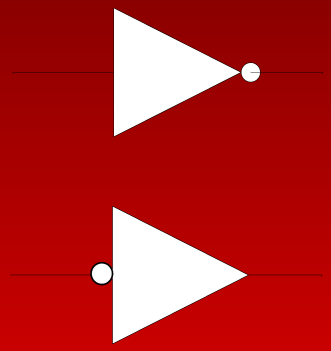
$$F = A + B + C + ..$$

OR Gate Timing Diagram



NOT Gate

- 1 input
- 1 output



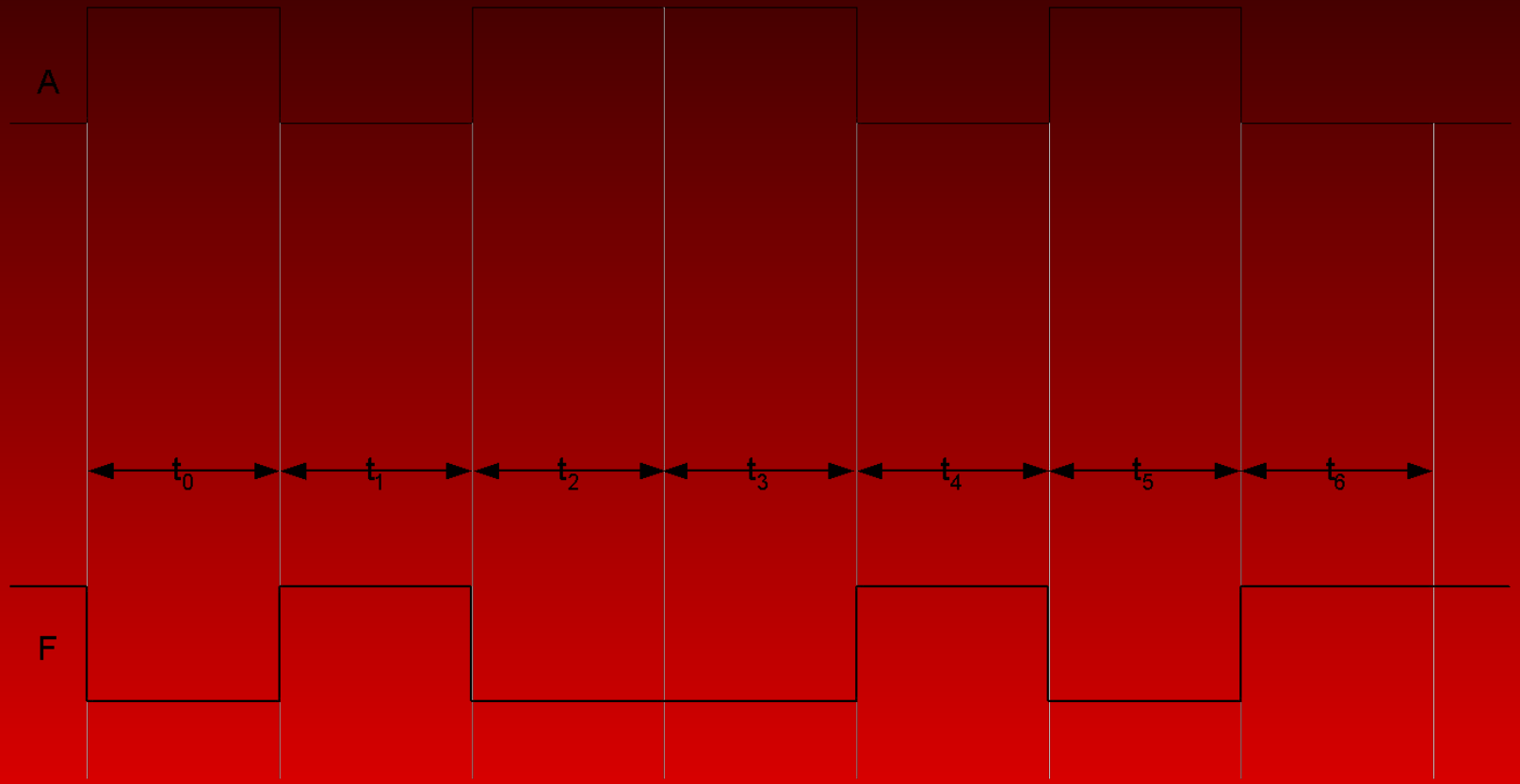
NOT Gate function

- Invert function

Input	Output
A	F
0	1
1	0

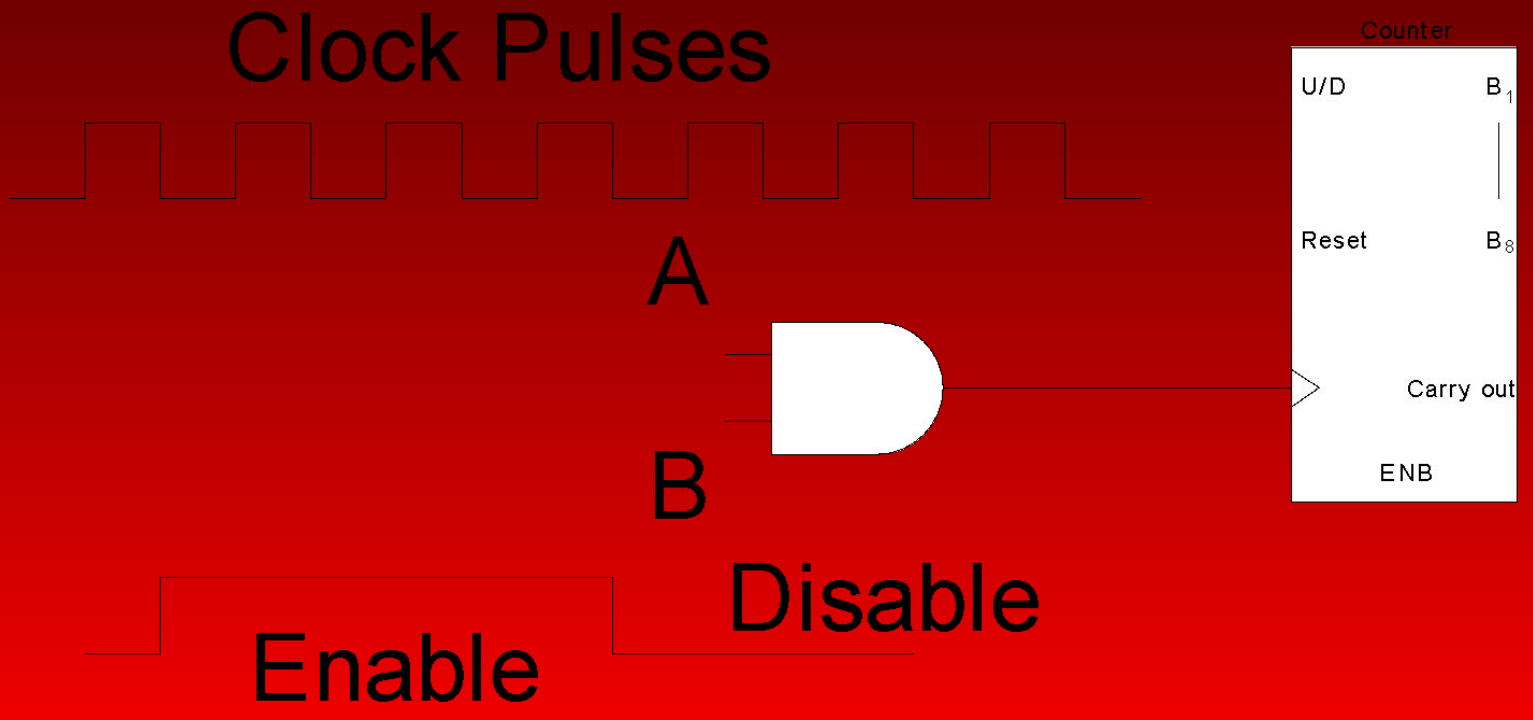
$F = \bar{A}$

NOT Gate Timing Diagram



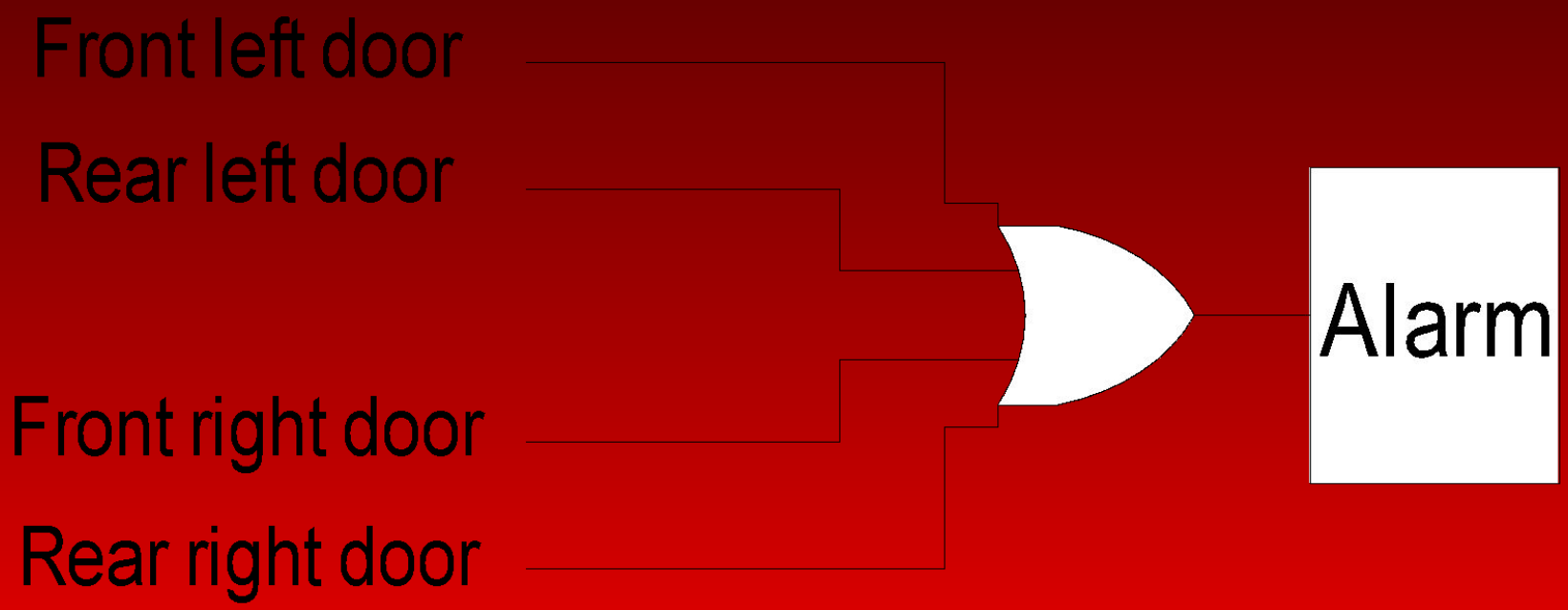
AND Gate Applications

- Enable/Disable Device
  - Counter counts when it receives pulses



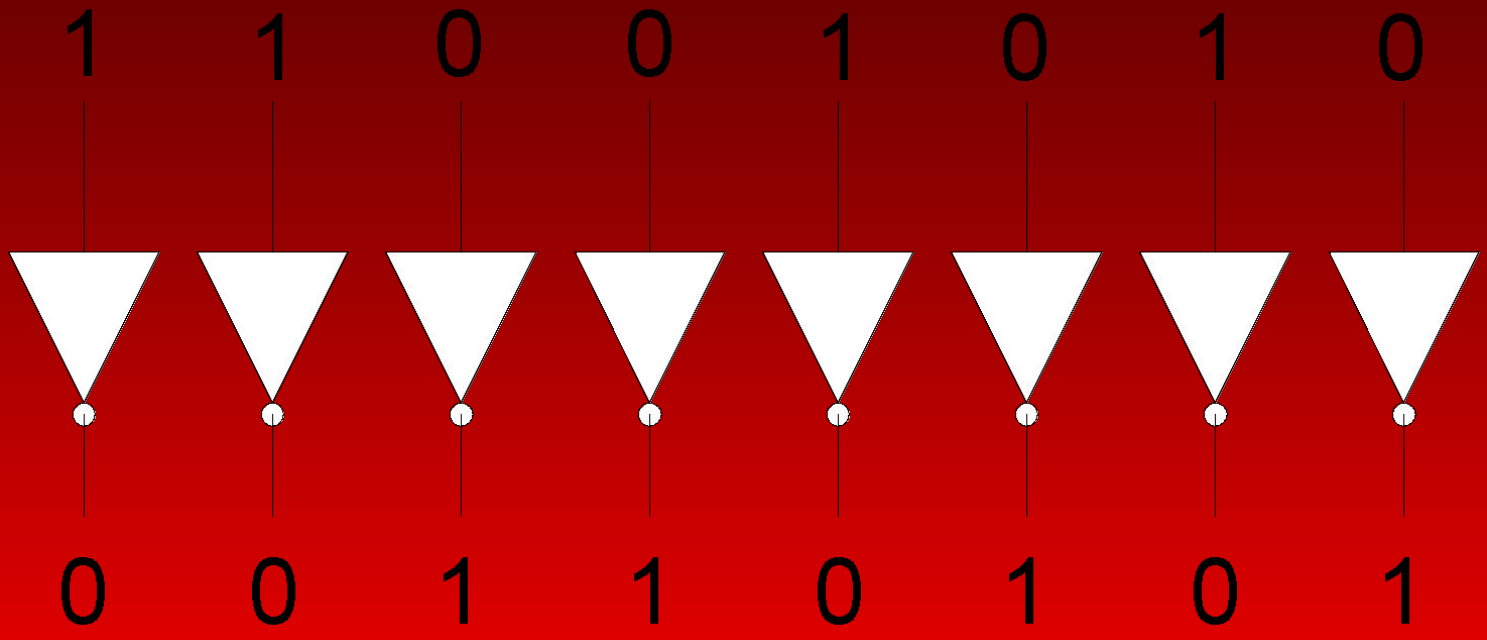
OR Gate Applications

- Car door open alarm



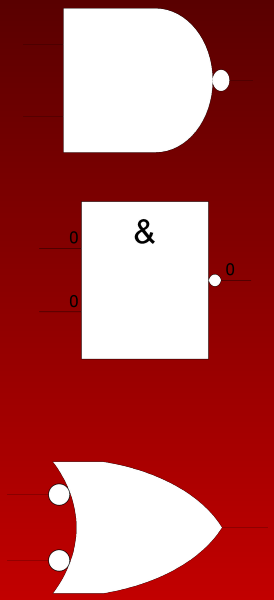
NOT Gate Applications

- 1’s Complement



NAND Gate

- 1 output
- 2 inputs
- 3 inputs
- 4 inputs
- Multiple inputs



NAND Gate function

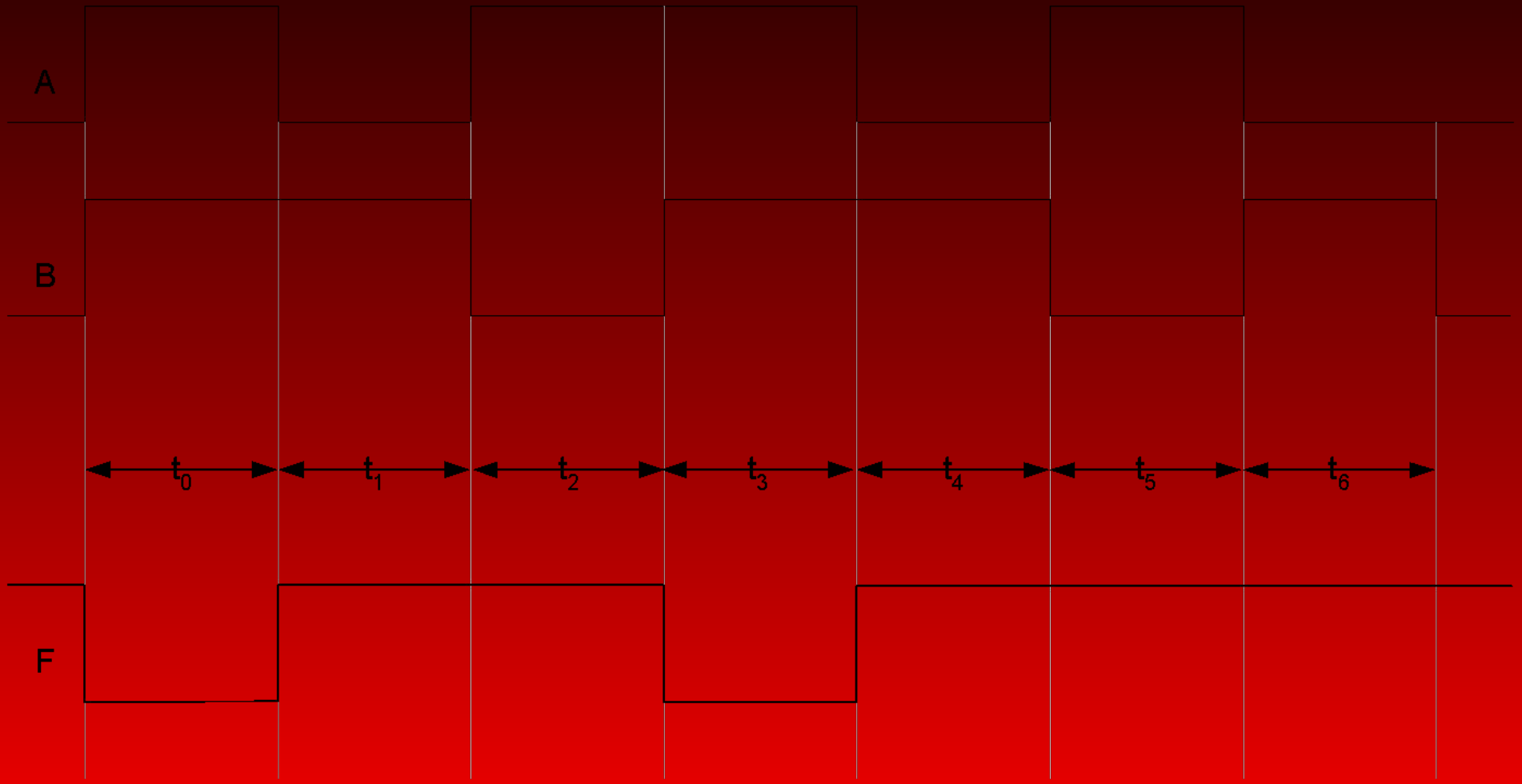
- NOT-AND function

Input		Output
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

$$F = \overline{A \cdot}$$

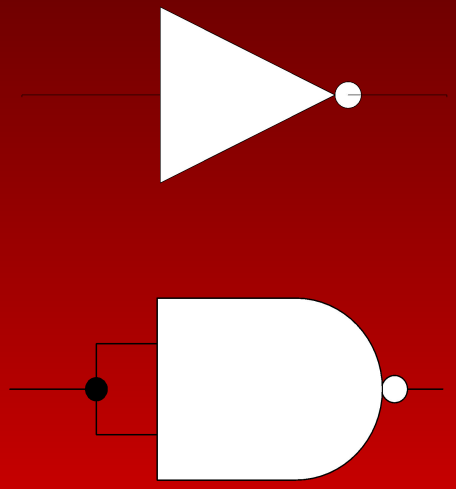
$$F = \overline{A \cdot B \cdot C \cdot}$$

NAND Gate Timing Diagram



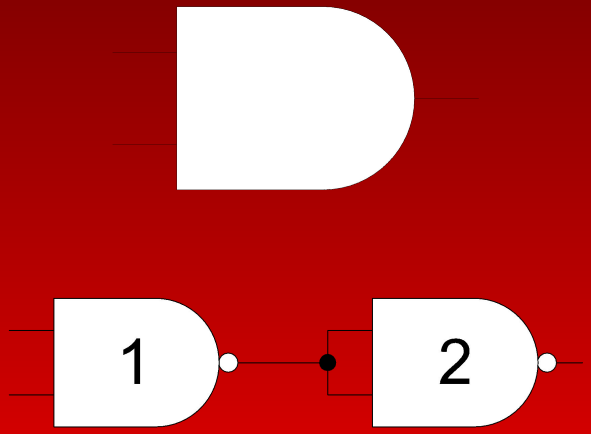
NAND Universal Gate

Input		Output
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0



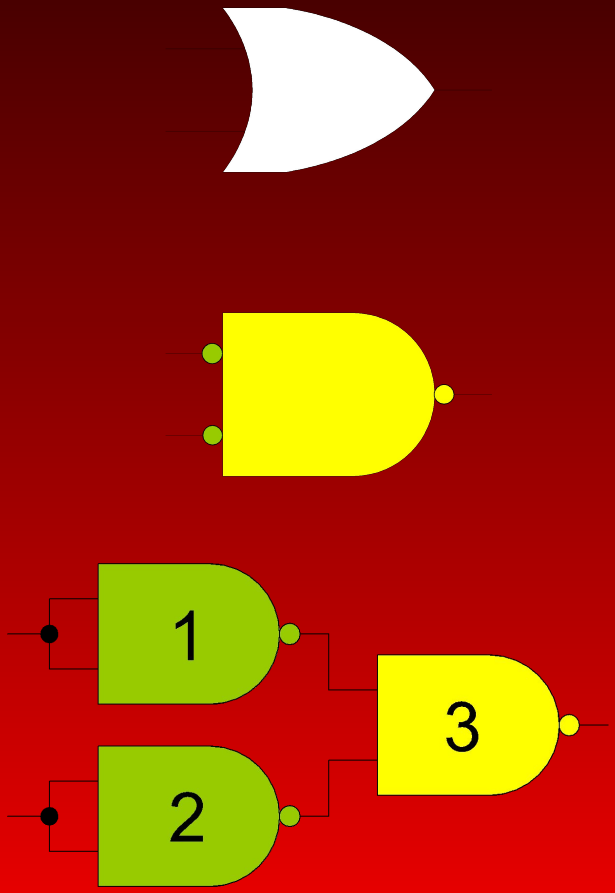
NAND Universal Gate

Input		Output	Output
A	B	F1	F
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1



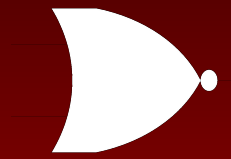
NAND Universal Gate

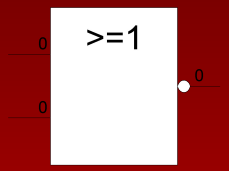
Input		Output
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

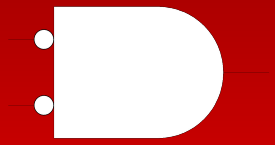


NOR Gate

- 1 output
- 2 inputs
- 3 inputs
- 4 inputs
- Multiple inputs







NOR Gate function

- NOT-OR function

Input		Output
A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

$$F = \overline{A + B + C + \cdots}$$

NOR Gate Timing Diagram