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DIGITAL ELECTRONICS TRAINER

IT-300 Digital Logic Training System is a comprehensive and self-contained system suitable for anyone engaged in digital logic experiments. All necessary equipments for digital logic experiments such as power supply, signal generator, switches and displays are installed on the main unit. Bread Board section allows students to connect many types of experiments in the field of digital logic. It is a time and cost saving device for both students and researchers interested in developing and testing circuit prototypes.

Specifications

DC Power Supply

Voltage Range: +5V, +15V and -15V

With output overload protection

Clock Generator

Frequency: up to 65Hz

Ranges: X1 and X10

Logic Switches

8-bit switch with complimentary outputs

Debounce Switches

Set of independent control output

Each set with Q, Q' output, pulse width > 5ms

Each set of switch with DEBOUNCE circuit

Display

State Monitor

8 independent LEDs to indicate high and low logic state.

Input Impedance: < 100 K ohm

7-segment Display

Pair of independent 7-segment LED display

With BCD, 7-segment decoder/driver and DP input

Input with 8-4-2-1 code

Testing Devices

Logic Probe

“Lo”, “Hi” and “Pulse” LED display low and high state respectively

Potentiometers

Three carbon track variable resistances

Value: 5K, 10K and 100K

EXPERIMENT 1 AND GATE OPERATION

Objective

To check the operation of AND gate according to the AND's truth table, using the IC 74LS08.

Equipment

Component

1. 74LS08 x 1

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezers
6. Pair of Pliers

Diagram



Fig. 2.1

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS08 on the trainer's breadboard.
4. Wire the circuit according to the diagram in figure 2.1 by consulting AND gate IC's data sheet in fig. 2.2.
5. Use any of the two logic switches from S0 to S7 for inputs A and B respectively.
6. For output indication use any of the LED's from (L0 – L7)
7. Supply the +5V and GND to the pins 14 and 7 of the IC.
8. Test all the possible combination of inputs and verify the output according to the truth table of AND gate.
9. Fill the truth table given below according to the results.

Table1. Truth Table for AND Gate

Inputs		Output
A	B	AND
0	0	
0	1	
1	0	
1	1	

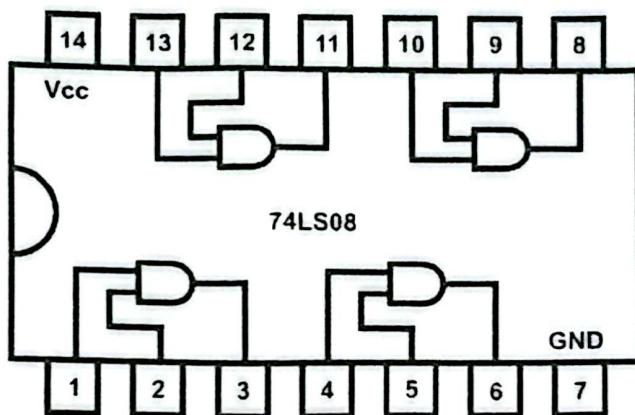


Fig. 2.2

In case of trouble

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using truth table.

EXPERIMENT 2

OR GATE OPERATION

Objective

To check the operation of OR gate according to the OR's truth table, using the IC 74LS32

Equipment

Component

1. 74LS32 x 1

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezers
6. Pair of Pliers

Diagram

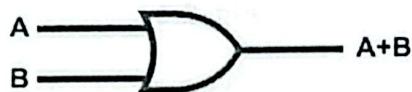


Fig. 3.1

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS32 on the trainer's breadboard.
4. Wire the circuit according to the diagram in figure 3.1 by consulting OR gate IC's data sheet in fig 3.2.
5. Use any of the two logic switches from S0 to S7 for inputs to OR gate.
6. For output indication use any of the LED's from (L0 – L7)
7. Supply the VCC= +5V and GND to the pins 14 and 7 of the IC.
8. Test all the possible combination of inputs and verify the output according to the truth table of OR gate.
9. Fill the truth table given below according to the results.

Table1. Truth Table for OR Gate

Inputs		Output
A	B	OR
0	0	
0	1	
1	0	
1	1	

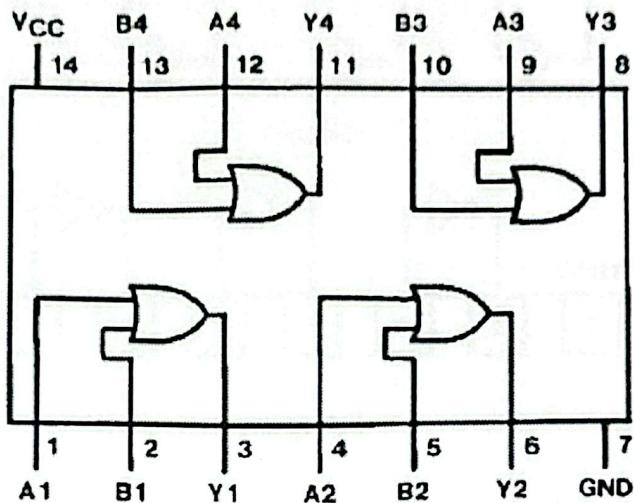


Fig. 3.2

In case of trouble

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using truth table.

EXPERIMENT 3

NOT GATE OPERATION

Objective

To check the operation of NOT gate according to the NOT's truth table, using the IC 74LS04

Equipment

Component

1. 74LS04 x 1

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezes
6. Pair of Pliers

Diagram

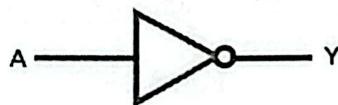


Fig. 4.1

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS04 on the trainer's breadboard.
4. Wire the circuit according to the diagram in figure 4.1 by consulting NOT gate IC's data sheet in fig 4.2.
5. Use any of the two logic switches from S0 to S7 for inputs A.
6. For output Y use any of the LED's from (L0 – L7)
7. Supply the VCC= +5V and GND to the pins 14 and 7 of the IC.
8. Test all the possible combination of inputs and verify the output according to the truth table of NOT gate.
9. Fill the truth table I according to the results.

Table1. Truth Table for NOT Gate

Inputs	Output
A	NOT
0	
1	

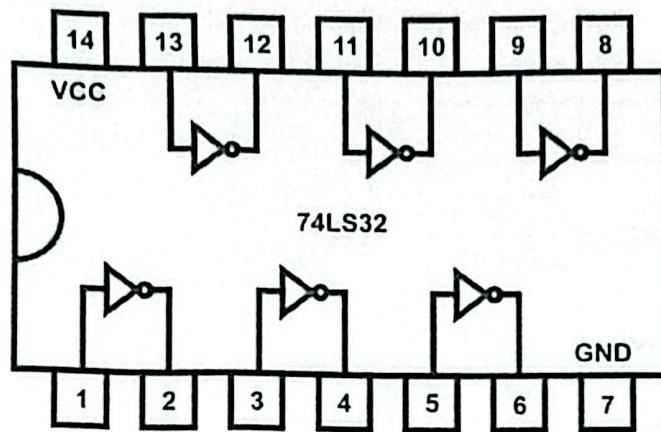


Fig. 4.2

In case of trouble

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using truth table.

EXPERIMENT 4

NAND GATE OPERATION

Objective

To check the operation of NAND gate according to the NAND's truth table, using the IC 74LS00

Equipment

Component

1. 74LS00 x 1

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezes
6. Pair of Pliers

Diagram



Fig. 5.1

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS00 on the trainer's breadboard.
4. Wire the circuit according to the diagram in figure 5.1 by consulting OR gate IC's data sheet in fig 5.2.
5. Use any of the two logic switches from S0 to S7 for inputs to NAND gate IC's.
6. For output indication use any of the LED's from (L0 – L7)
7. Supply the VCC= +5V and GND to the pins 14 and 7 of the IC.
8. Test all the possible combination of inputs and verify the output according to the truth table of NAND gate.
9. Fill the truth table given below according to the results.

Table1. Truth Table for NAND Gate

Inputs		Output
A	B	NAND
0	0	
0	1	
1	0	
1	1	

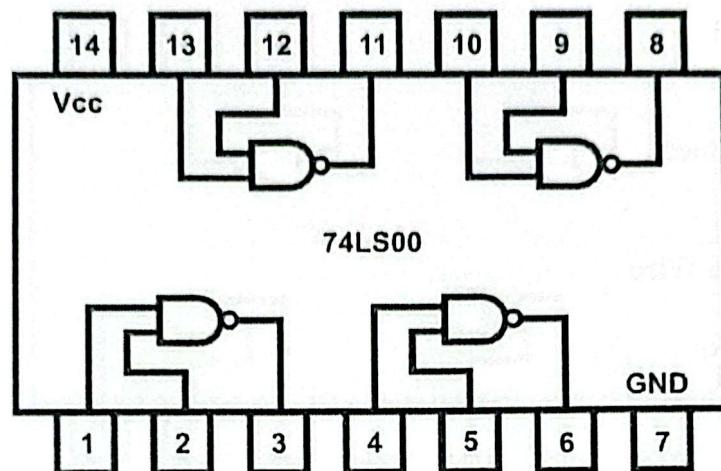


Fig. 5.2

In case of trouble

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using truth table.

EXPERIMENT 5

NOR GATE OPERATION

Objective

To check the operation of NOR gate according to the NOR's truth table, using the IC 74LS02.

Equipment

Component

1. 74LS02 x 1

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezers
6. Pair of Pliers

Diagram

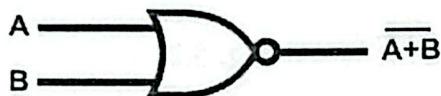


Fig. 6.1

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS02 on the trainer's breadboard.
4. Wire the circuit according to the diagram in figure 6.1 by consulting NOR gate IC's data sheet in fig 6.2.
5. Use any of the two logic switches from S0 to S7 for inputs to NOR gate ICs.
6. For output indication use any of the LED's from (L0 – L7)
7. Supply the VCC= +5V and GND to the pins 14 and 7 of the IC.
8. Test all the possible combination of inputs and verify the output according to the truth table of NOR gate.
9. Fill the truth table given below according to the results.

Table1. Truth Table for NOR Gate

Inputs		Output
A	B	NOR
0	0	
0	1	
1	0	
1	1	

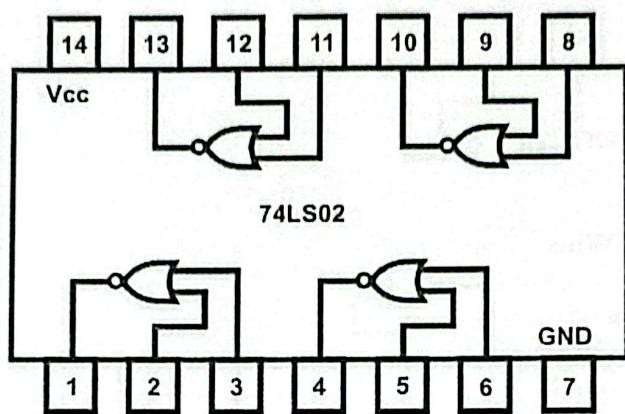


Fig. 6.2

In case of trouble

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using truth table.

EXPERIMENT 6

XOR GATE OPERATION

Objective

To check the operation of XOR gate according to the XOR's truth table, using the IC 74LS86

Equipment

Component

1. 74LS86 x 1

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezers
6. Pair of Pliers

Diagram



Fig. 7.1

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS86 on the trainer's breadboard.
4. Wire the circuit according to the diagram in figure 7.1 by consulting XOR gate IC's data sheet in fig 7.2.
5. Use any of the two logic switches from S0 to S7 for inputs to XOR gate IC's.
6. For output indication use any of the LED's from (L0 – L7)
7. Supply the VCC= +5V and GND to the pins 14 and 7 of the IC.
8. Test all the possible combination of inputs and verify the output according to the truth table of XOR gate.
9. Fill the truth table given below according to the results.

Table1. Truth Table for XOR Gate

Inputs		Output
A	B	XOR
0	0	
0	1	
1	0	
1	1	

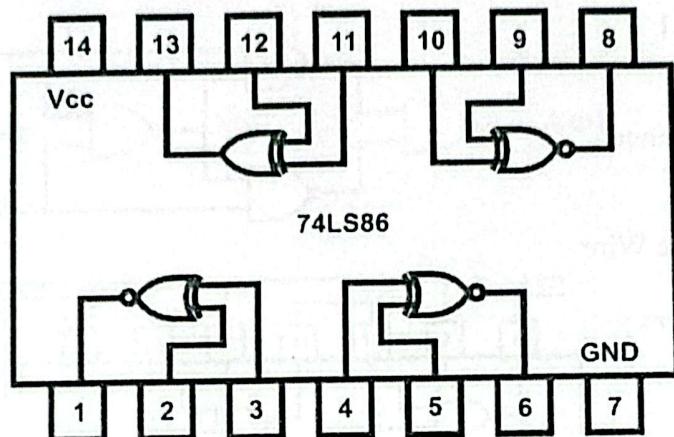


Fig. 7.2

In case of trouble

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using truth table.

EXPERIMENT 7

CONSTRUCTION OF XOR GATE FROM NAND GATES

Objective

To check the operation of XOR gate according to the NAND's truth table, using the IC 74LS00

Equipment

Component

1. 74LS00 x 1

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezers
6. Pair of Pliers

Diagram

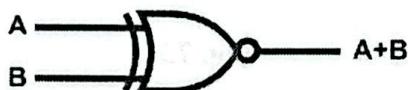


Fig. 8.1

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS00 on the trainer's breadboard.
4. Wire the circuit according to the diagram in figure 8.1 by consulting OR gate IC's data sheet in fig 8.2.
5. Use any of the two logic switches from S0 to S7 for inputs A and B respectively.
6. For output indication use any of the LED's from (L0 – L7)
7. Supply the VCC= +5V and GND to the pins 14 and 7 of the IC.
8. Test all the possible combination of inputs and verify the output according to the truth table of XOR gate.
9. Fill the truth table given below according to the results.

EXPERIMENT 7

CONSTRUCTION OF XOR GATE FROM NAND GATES

Objective

To check the operation of XOR gate according to the NAND's truth table, using the IC 74LS00

Equipment

Component

1. 74LS00 x 1

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezers
6. Pair of Pliers

Diagram

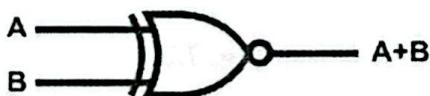


Fig. 8.1

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS00 on the trainer's breadboard.
4. Wire the circuit according to the diagram in figure 8.1 by consulting OR gate IC's data sheet in fig 8.2.
5. Use any of the two logic switches from S0 to S7 for inputs A and B respectively.
6. For output indication use any of the LED's from (L0 – L7)
7. Supply the VCC= +5V and GND to the pins 14 and 7 of the IC.
8. Test all the possible combination of inputs and verify the output according to the truth table of XOR gate.
9. Fill the truth table given below according to the results.

Table1. Truth Table for OR Gate

Inputs		Output
A	B	OR
0	0	
0	1	
1	0	
1	1	

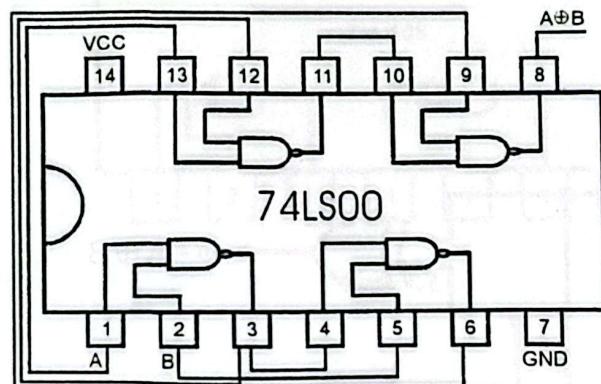
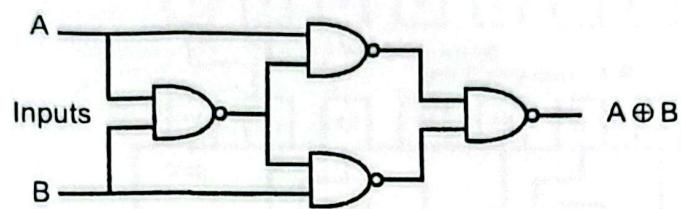


Fig. 8.2 - 8.3

In case of trouble

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using truth table.

EXPERIMENT 8

HALF ADDER OPERATION

Objective

To design half adder circuit using XOR and AND gates.

Equipment

Component

1. 74LS86 x 1
2. 74LX08 x 1

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezers
6. Pair of Pliers

Diagram

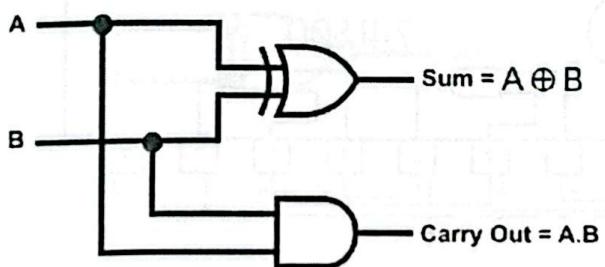


Fig. 9.1

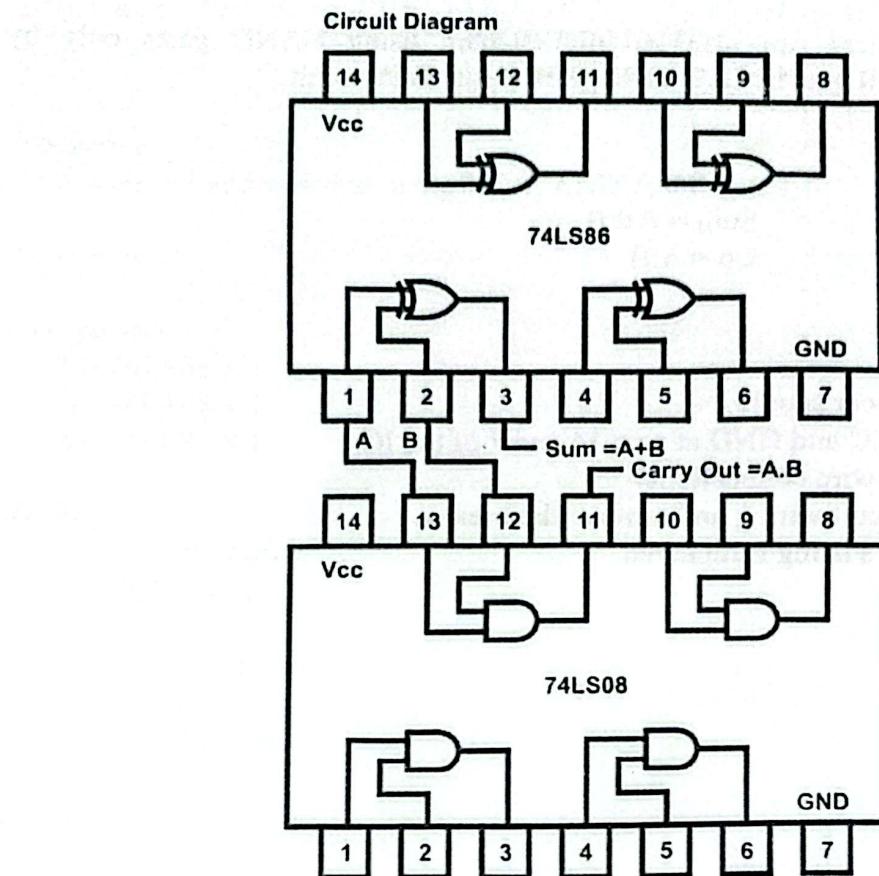


Fig. 9.2

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS08 & IC 74LS86 on trainer's breadboard.
4. Wire the circuit according to the diagram in figure 9.2.
5. Use any of the two logic switches from S0 to S7 for inputs A and B.
6. For output sum, use LED's L0 and for output Carry, use LED L1.
7. Supply the VCC= +5V and GND to the pins 14 and 7 of the ICs.
8. Test all the possible combination of inputs and verify the output according to the truth table half adder.
9. Fill the truth table given below according to the results.

Table1. Truth Table for OR Gate

Inputs		Output	
A	B	Sum	Carry out
0	0		
0	1		
1	0		
1	1		

10. This experiment can also be implemented using NAND gates only by replacing XOR gate by its NAND gates equivalent circuit.

Results

Logic Functions:

$$\text{Sum} = A \oplus B$$

$$\text{Co} = A \cdot B$$

In case of trouble

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC's using truth table.

EXPERIMENT 9

FULL ADDER OPERATION

Objective

To design full adder circuit using XOR, AND & OR gates.

Equipment

Component

1. 74LS86 x 1
2. 74LS08 x 1
3. 74LS32 x 1

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezers
6. Pair of Pliers

Diagram

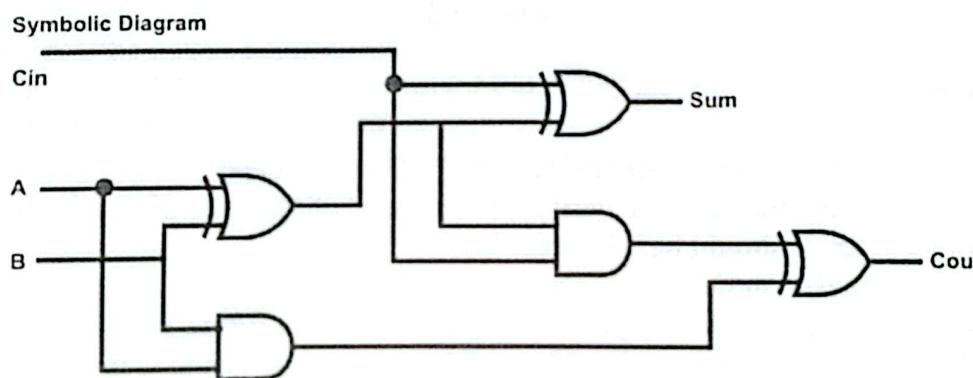


Fig. 10.1

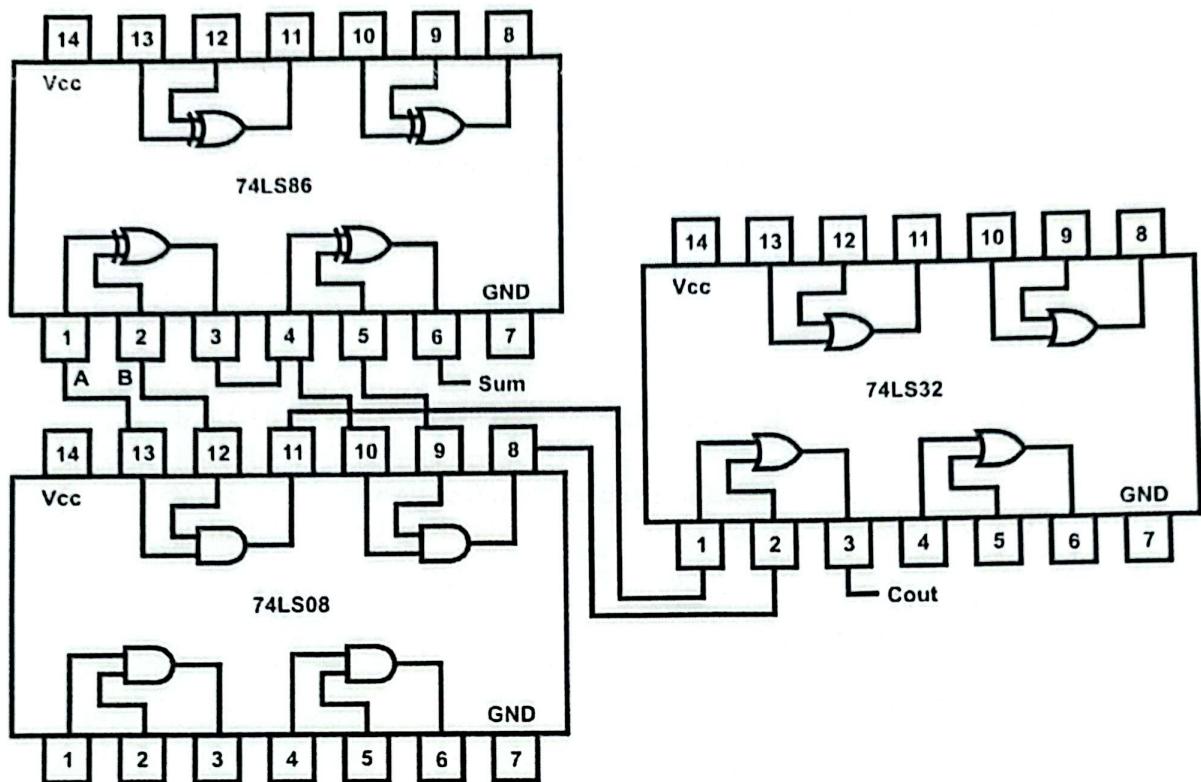


Fig. 10.2

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the ICs on the breadboard.
4. Wire the circuit according to the diagram shown in figure 10.2.
5. Use logic switches from S2, S3 and S4 for inputs A, B and C in respectively.
6. For output sum, use LED L0 and for output carry, used LED L1.
7. Supply the VCC= +5V and GND to the pins 14 and 7 of the ICs.
8. Test all the possible combination of inputs and verify the output according to the truth table of full adder.
9. Fill the truth table given below according to the results.

Table1. Truth Table for Full Adder

Inputs			Output	
A	B	Cin	S	Cout
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

10. You can also implement this experiment using NAND gates only by replacing XOR by its NAND gates equivalent circuit.

Results

Logic Function:

$$\begin{aligned} \text{Sum} &= A \oplus B \oplus \text{Cin} \\ \text{C out} &= ((A \oplus B) \cdot \text{Cin}) \oplus (A \cdot B) \end{aligned}$$

In case of trouble

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using truth table.

EXPERIMENT 10

HALF SUBTRACTOR OPERATION

Objective

To design half subtractor circuit using XOR, AND and NOT gates.

Equipment

Component

1. 74LS86 x 1
2. 74LS08 x 1
3. 74LS04 x 1

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezers
6. Pair of Pliers

Diagram

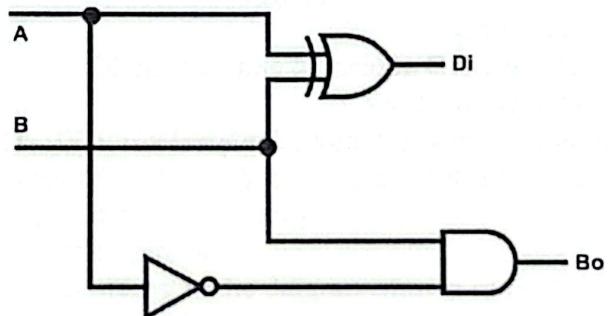


Fig. 11.1

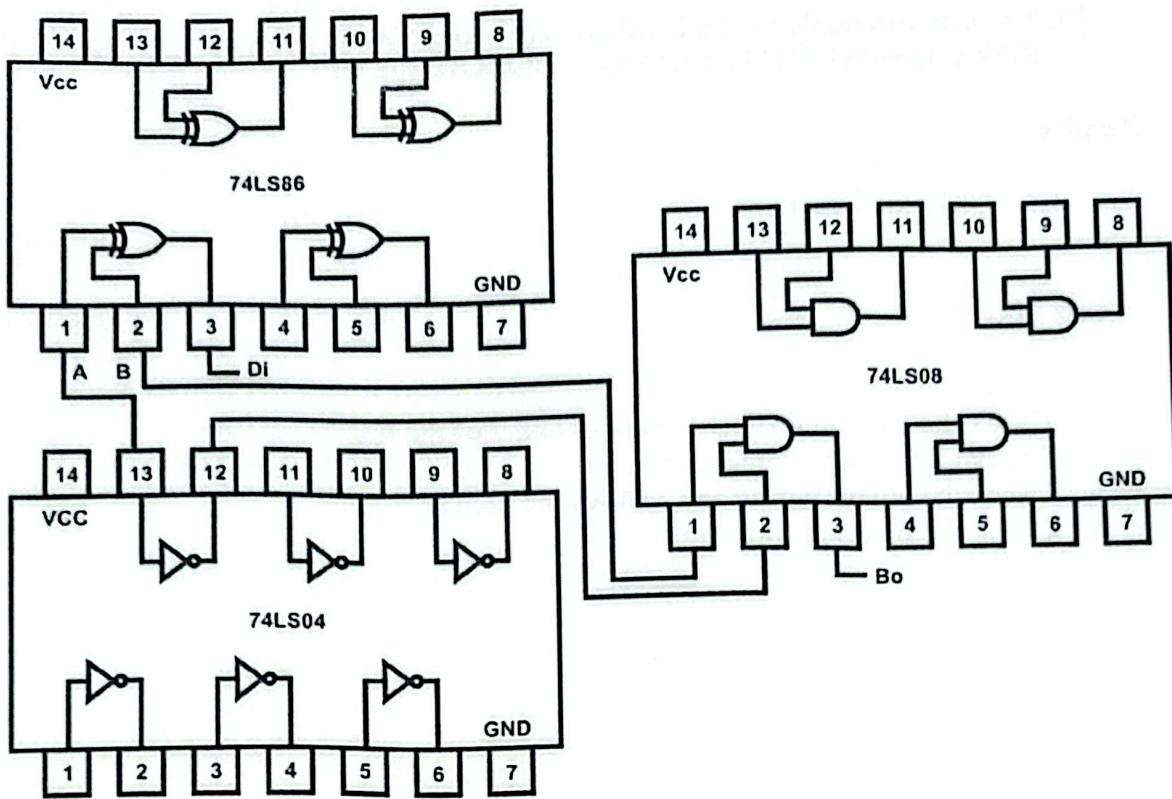


Fig. 11.2

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS08, 74LS86 and 74LS04 on the trainer's breadboard.
4. Wire the circuit according to the diagram in figure 11.2.
5. Use any of the two logic switches from S0 to S7 for inputs A and B.
6. For output difference, use LED's from L0 and for output borrow, use LED L1.
7. Supply the VCC= +5V and GND to the pins 14 and 7 of the ICs.
8. Test all the possible combination of inputs and verify the output according to the truth table of half subtractor.
9. Fill the truth table given below according to the results.

Table1. Truth Table for Half Subtractor

Inputs		Output	
A	B	Bo	Di
0	0		
0	1		
1	0		
1	1		

10. You can also implement this experiment using NAND gates only by replacing XOR gate with its NAND gates equivalent-circuit.

Results

Logic Functions:	$D_i = A \oplus B$
	$B_o = A' \cdot B$

In case of trouble

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using truth table.

EXPERIMENT 11

FULL SUBTRACTOR OPERATION

Objective

To design full subtractor circuit using XOR, AND, NOT and OR gates.

Equipment

Component

1. 74LS86 x 1
2. 74LS08 x 1
3. 74LS04 x 1
4. 74LS32 x 1

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezers
6. Pair of Pliers

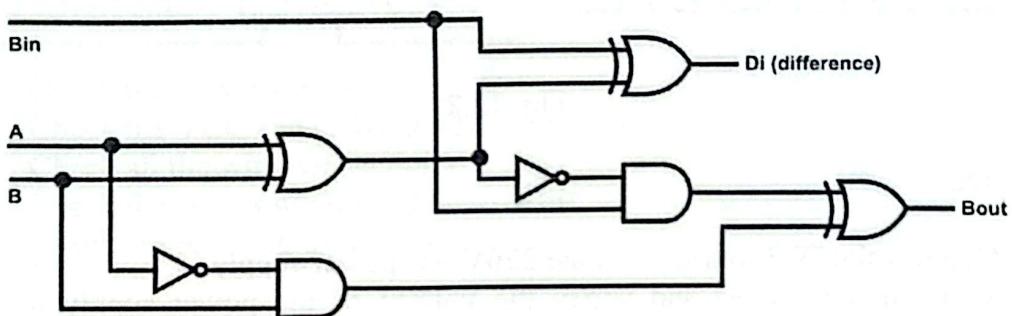


Fig. 12.1

Full Subtractor using logic gates

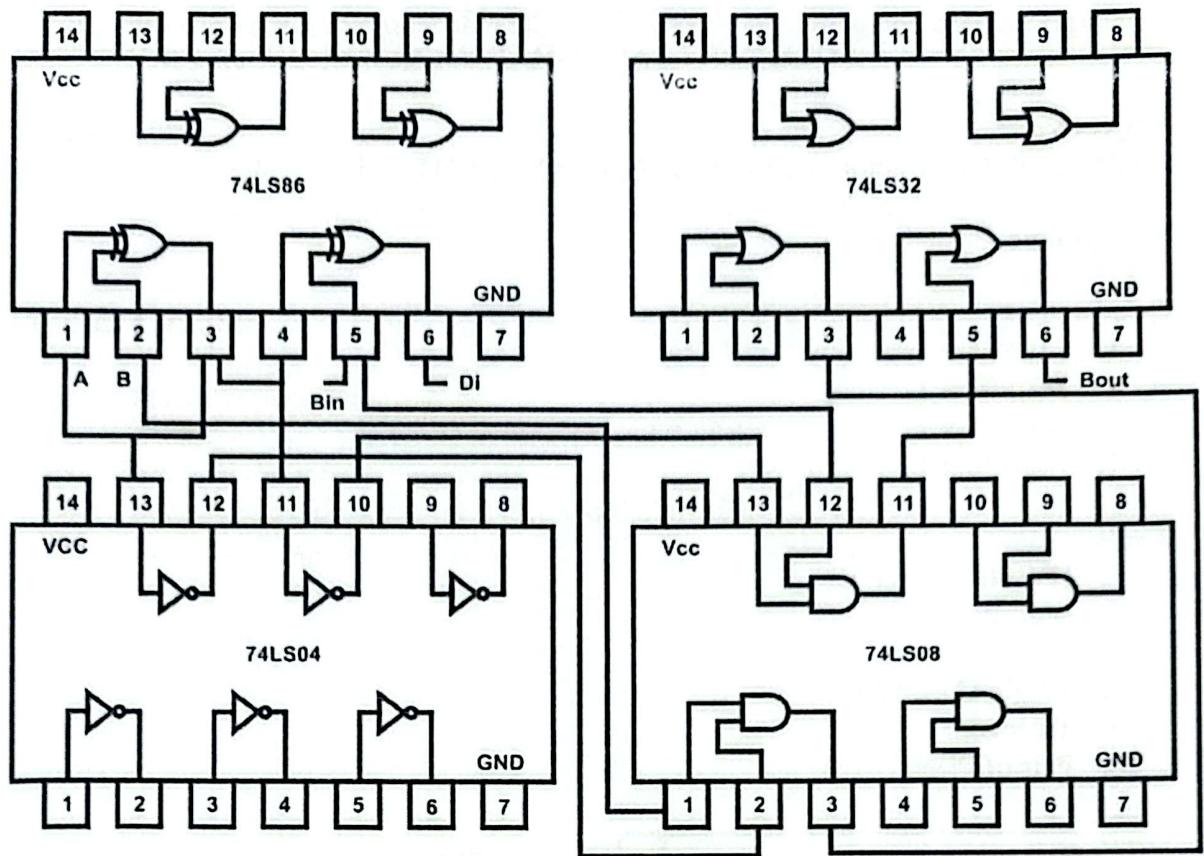


Fig. 12.2

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC's 74LS86, 74LS32, 74LS08 and 74LS04 on the trainer's breadboard.
4. Wire the circuit according to the diagram in figure 12.2.
5. Use logic switches S2, S3, and S4 for inputs A, B and Bin respectively.
6. For output Di use LED L0 and for output bout use LED L1.
7. Supply the VCC= +5V and GND to the pins 14 and 7 of the ICs.
8. Test all the possible combination of inputs and verify the output according to the truth table of half subtractor.
9. Fill the truth table given below according to the results.

Table1. Truth Table for Full Subtractor

Inputs			Output	
A	B	Bin	Bo	Di
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

10. You can also implement this experiment using NAND gates only by replacing XOR by its NAND gates equivalent circuit.

Results

Logic Functions:

$Di = (A \oplus B) \oplus Bin$
$Bout = (Bin.(A \oplus B))' \oplus (A'.B)$

In case of trouble

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using truth table.

EXPERIMENT 12

7-SEGMENT DISPLAY OPERATION

Objective

To check the operation of common anode 7-segment display.

Equipment

Component

1. 7-segment display (common anode) x 1.
2. 180 ohms resistances x 8.

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezers
6. Pair of Pliers

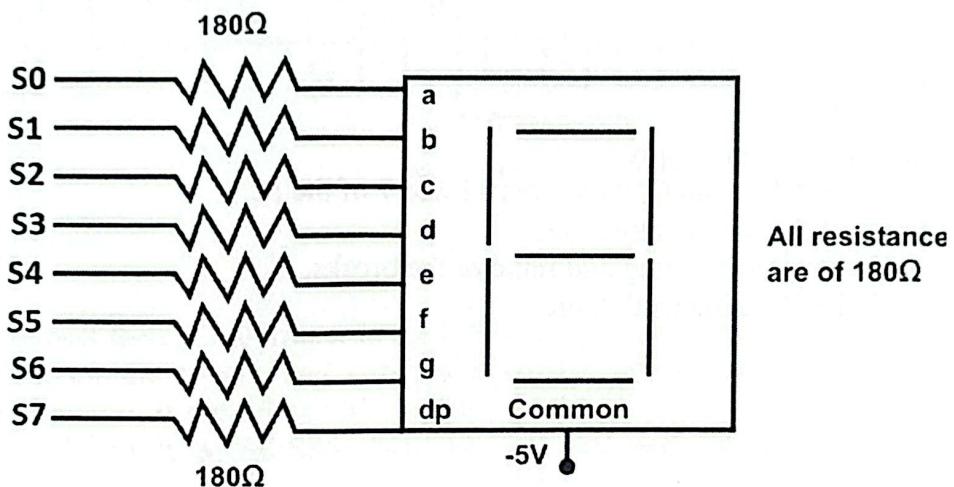


Fig. 12.1

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the 7-segment display on trainer's breadboard.
4. Wire the circuit according to the diagram shown above by consulting data sheet of Common Anode display in fig 13.2.
5. Use logic switches S0 through S7 for inputs a through g and dp respectively.
6. Connect the common pin of 7-segment display to +5V.
7. Test all the possible combination of inputs as shown in table-1 and see the results.
8. Fill the truth table given below according to the results.

Table1. Truth Table for 7-Segment Display

S2	S3	S4	S5	S6	S7	S8	S9	dp	Digit Displayed
A	B	c	d	e	f	g			
0	0	0	0	0	0	1		0	
1	0	0	1	1	1	1		0	
0	0	1	0	0	1	0		0	
0	0	0	0	1	1	0		0	
1	0	0	1	1	0	0		0	
0	1	0	0	1	0	0		0	
1	1	0	0	0	0	0		0	
0	0	0	1	1	1	1		0	
0	0	0	0	0	0	0		0	
0	0	0	1	1	0	0		0	

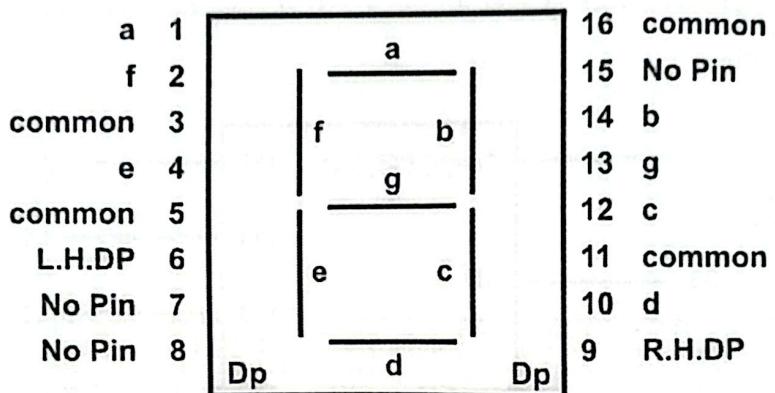


Fig. 13.2

Results

0-9 digits will be displayed with dp ON.

In case of trouble

1. Check the power supply.
2. Check +5V to common pin of 7-segment display.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the individual segments of 7-segment display by consulting its data sheet.

EXPERIMENT 13

DECODER OPERATION

Objective

To check the operation of 2 to 4 line decoder using the IC 74LS139

Equipment

Component

1. 74LS139 x 1

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezer
6. Pair of Pliers

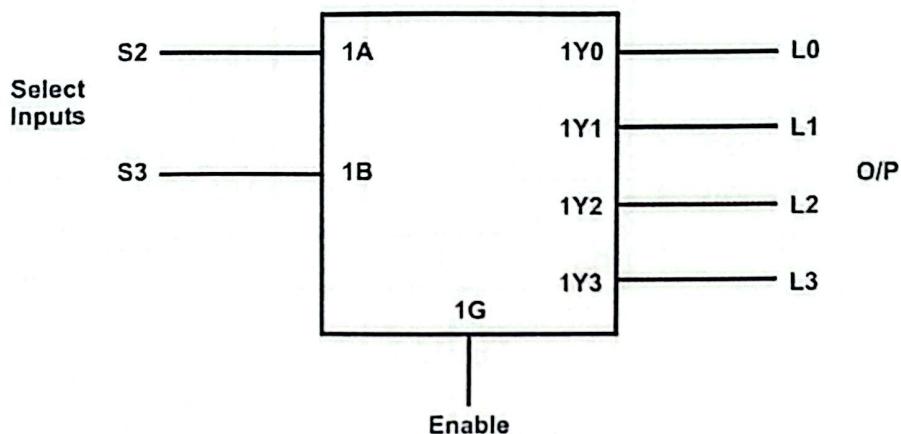


Fig. 14.1

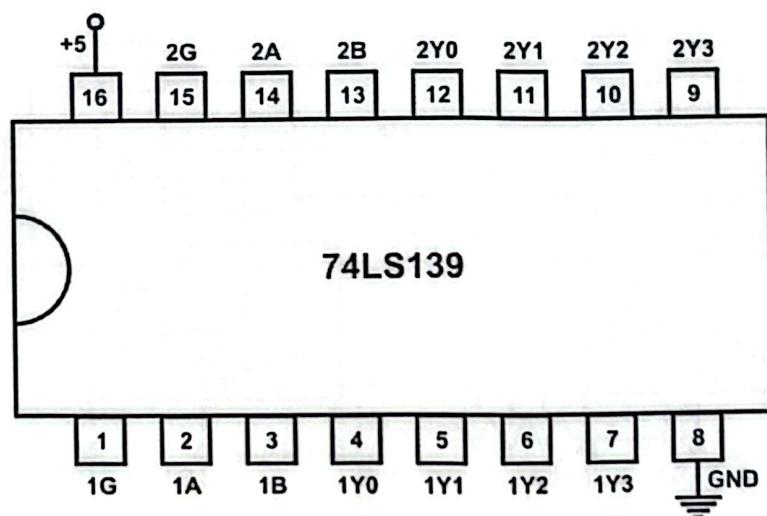
Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS139 on trainer's breadboard.
4. IC 74LS139 is a dual 2 to 4 line decoders / demultiplexers. Wire one of such decoder according to the diagram in fig. 14.1 by consulting data sheet of the IC.
5. Use logic switches S2 and S3 for decoder inputs 1A and 1B respectively.
6. Connect outputs 1Y0, 1Y1, 1Y2 and 1Y3 to LED's L0, L0, L1, L2 and L3 respectively.
7. Supply the VCC= +5V and GND to the pins 16 and 8 of the IC.
8. Test all the possible combination of inputs and verify the output according to the truth table of 74LS139.
9. Fill the truth table given below according to the results.

Table1. Truth Table for 2 to 4 lines Decoder

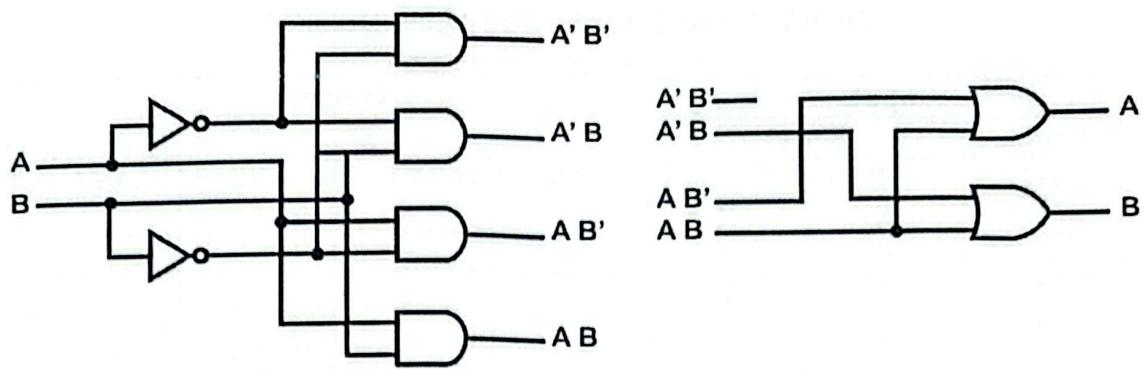
Inputs			Output			
Enable	Select		1Y0	1Y1	1Y2	1Y3
1G	1B	1A				
1	X	X				
0	0	0				
0	0	1				
0	1	0				
0	1	1				

Dual 2-Line to 4-Line Decoders

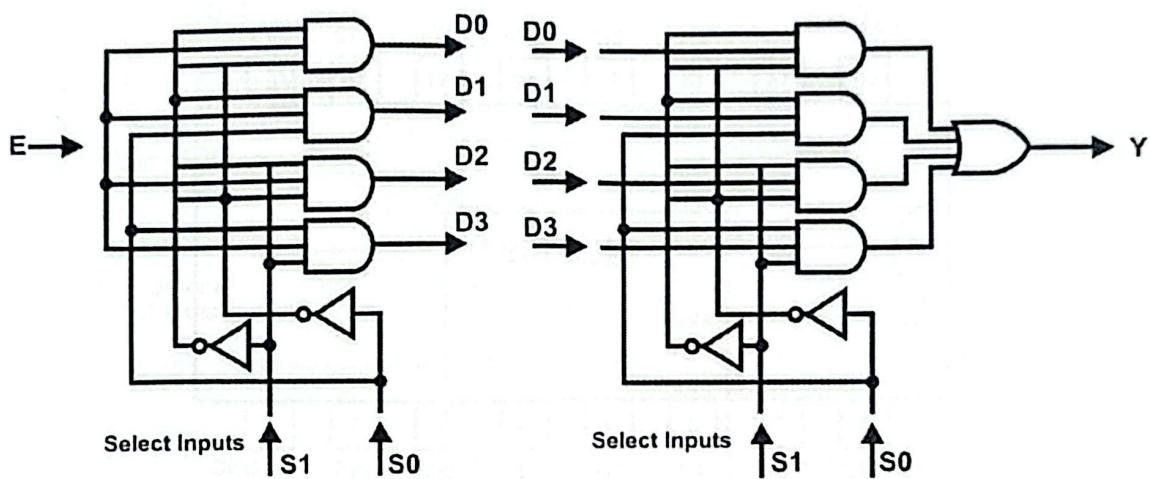


In case of trouble

1. Check the power supply.
2. Check the VCC and GND at pins 16 and 8 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using truth table.



Binary Encoder and Decoder Circuits



AND gate realization of Multiplexer and Demultiplexer

EXPERIMENT 14

BCD TO 7-SEGMENT DISPLAY

Objective

To check the operation of common anode BCD to 7-segment decoder using IC 74LS47.

Equipment

Component

1. 7-segment display (common anode) x 1.
2. $180\Omega \times 8$
3. IC 74LS47

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezer
6. Pair of Pliers

Diagram

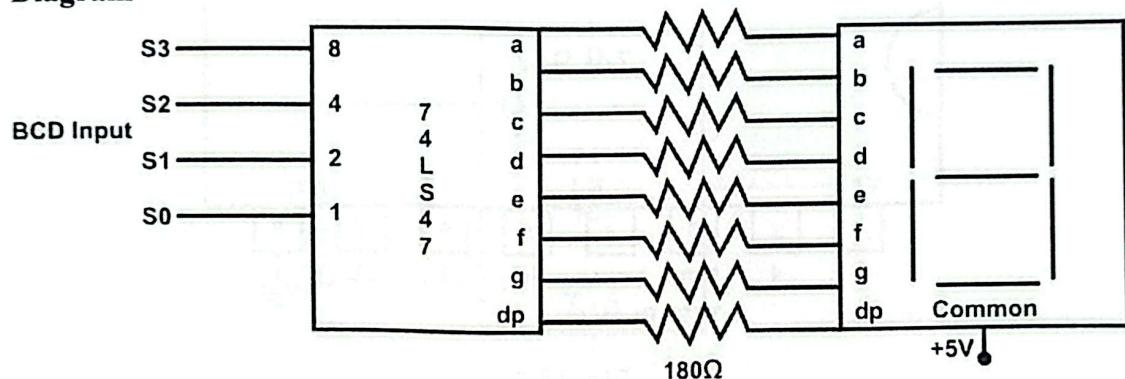


Fig. 15.1

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install 7-segment display and IC 74LS47 on trainer's breadboard.
4. Wire the circuit according to the diagram shown above.
5. Use logic switches S0 through S3 for BCD inputs (1,2,4 and 8) to decoder.
6. Supply the VCC= +5V and GND to the pins 16 and 8 of the IC.
7. Connect the common pin of 7-segment display to +5V.
8. Enter BCD numbers from 0-9 using logic switches and see the result on to the display.
9. Fill the truth table given below according to the results.

Table1. Truth Table for BCD to 7-segment decoder

S3	S2	S1	S0	Display Decimal Digit
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	

BCD to 7-Segment Decoder - Driver

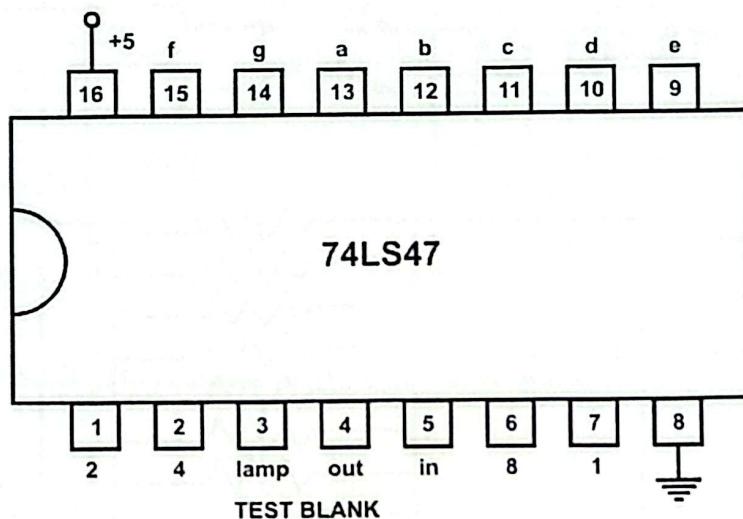


Fig. 15.2

Results

0-9 digits will be displayed in sequence.

In case of trouble

1. Check the power supply.
2. Check the +5V to common pin of 7-segment display.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the individual segments of 7-segment display by consulting its data sheet.

EXPERIMENT 15

MULTIPLEXER OPERATION

Objective

To check the operation of 1 of 2 data selector / multiplexer using the IC 74LS157.

Equipment

Component

1. 74LS157 x 1

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezer
6. Pair of Pliers

Diagram

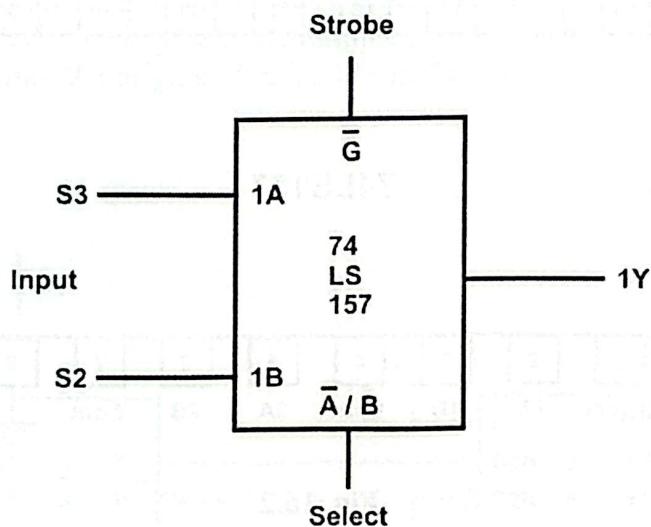


Fig. 16.1

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS157 on trainer's breadboard.
4. IC 74LS157 is a quadruple 1 of 2 data selectors / multiplexers. Use one out of 4 such MUX and wire the circuit according to the diagram.
5. Use logic switches S3 for 1A and switch S2 for 1B respectively.
6. Connect output 1Y to LED L0.
7. Supply the VCC= +5V and GND to the pins 16 and 8 of the IC.

- Test all the possible combinations of inputs and verify the output according to the truth table of 74LS157.
- Fill the truth table given below according to the results.

Table1. Truth Table for 1 of 2 data multiplexer

Inputs			Output		
Strobe G	Select A / B	Date	1A	1B	1Y
1	X	X		X	
0	0	0		X	
0	0	1		X	
0	1	X		0	
0	1	X		1	

- You will see that when select input is 0, then input A will be selected if select input is 1 then input B will be selected as output.

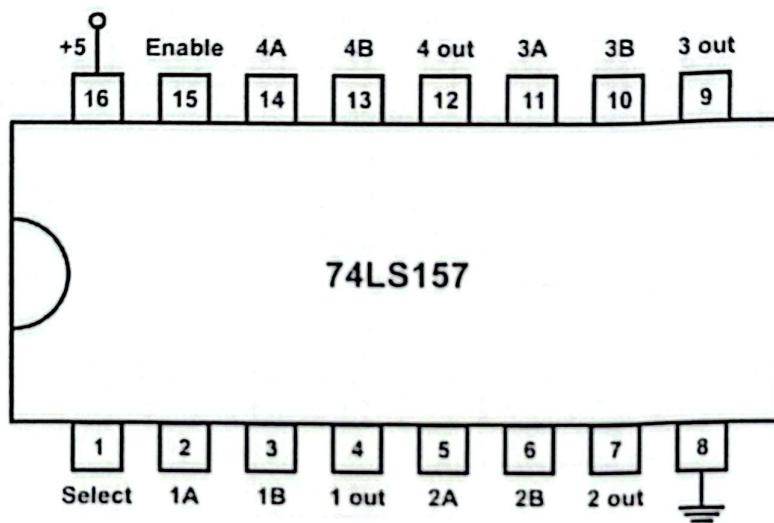


Fig. 16.2

In case of trouble

- Check the power supply.
- Check the VCC and BND at pins 16 and 8 of the IC.
- Check all the wire connections.
- Check the circuit wiring and remove the breaks.
- Check the IC using its truth table.

EXPERIMENT 16

USING MULTIPLEXER AND DEMULTIPLEXER / DECODER

Objective

To employ a 74LS151 as a multiplexer and a 74LS138 as a demultiplexer in a single-line digital communications circuit.

Theory of Operation

As shown in figure 17.1, the 74LS151 functions as a 1-of-8 multiplexer. The 3-bit select code will command which of the data inputs will be steered to the Y output. This same 3-bit code will be applied to the select inputs of the 74LS138 demultiplexer. Instead of running eight separate data lines, this circuit employs one multiplexed data line and three lines of select code. This saves a total of four lines.

The select code of the desired data line (0 through 7) is applied to select inputs of both ICs as shown in figure 17-1. If the selected data is low, the Y output of 74LS151 will go low. This low is applied to the G2A enable input of 74LS138 which will enable the IC and the output that corresponds to the select code will go low and match the original data from 74LS151. If the selected data is high, the Y output of multiplexer will go high. When this high is applied to the active-low enable input of 74LS138, IC will become disabled. All outputs of demultiplexers will go high. The selected output will be high, matching the original data sent from 74LS151.

Equipment

Component

1. 74LS151 x 1
2. 74LS138 x 1

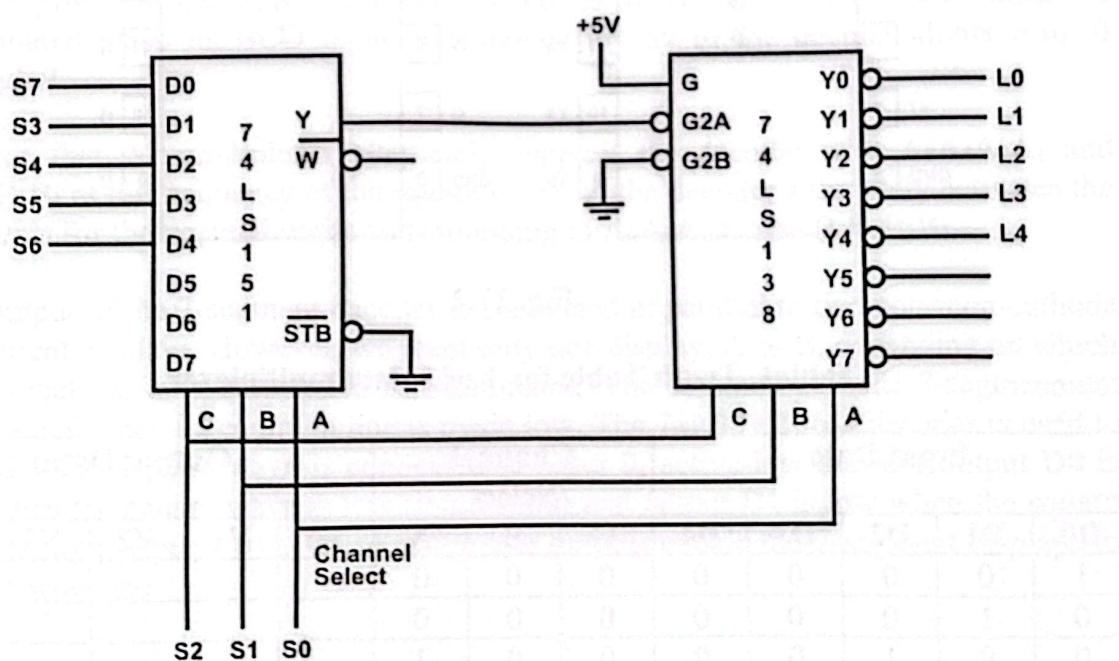


Fig. 17.1

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the ICs 74LS151 and 74LS138 on trainer's breadboard.
4. Wire the circuit according to the diagram in figure 17-1 by consulting data sheets in figure 17.2.
5. Maximum 8 switches are available on the trainer so for inputs D0 through D4 use logic switches S3 through S7 and for select lines A, B and C use switches S0, S1 and S2 respectively.
6. Connect outputs Y0 through Y4 of 74LS138 to LED's L0 through L4 respectively.
7. Supply the VCC= +5V and GND to the pins 16 and 8 of the ICs.
8. Apply the select code of the desired data line (0 through 4).
9. Observe the corresponding output match the original data.
10. Test all the select inputs (0 through 4) and verify the output matches the corresponding input.
11. Fill the table-1 according to the results.

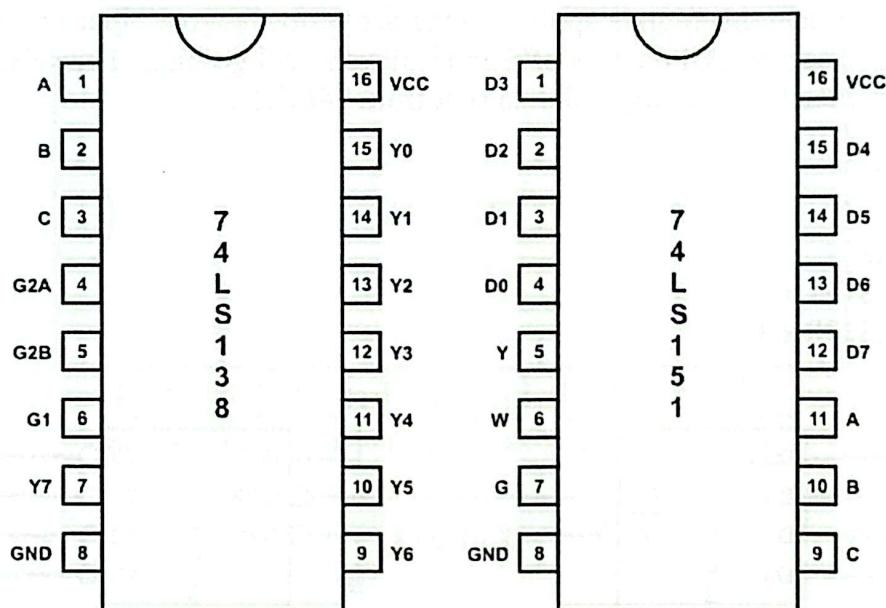


Fig. 17.2

Table1. Truth Table for 1 of 2 data multiplexer

Input Data					Channel Select			Output Data				
D0	D1	D2	D3	D4	C	B	A	Y0	Y1	Y2	Y3	Y4
1	0	0	0	0	0	0	0					
0	1	0	0	0	0	0	0					
0	0	1	0	0	0	0	0					
0	0	0	1	0	0	0	1					
0	0	0	0	1	1	1	0					

PROJECT 1

MULTIPLEXING 7-SEGMENT DISPLAYS

Theory of Operation

Optical output displays, such as 7-segment displays, typically consume considerable power. In applications where power consumption is a major concern, such as pocket calculator, and where several displays must be illuminated simultaneously, multiplexers are used to reduce power consumption.

Instead of illuminating all displays simultaneously, a multiplexer selects each display in turn. If the rate at which the displays are illuminated is great enough (usually around 30 times per second), the human eye will not be able to detect any flicker, and it will appear that all displays are illuminated simultaneously. The power consumption will be no greater than if a single display were illuminated continuously.

Figure 1(a) shows how a 74LS157 multiplexer can be used to multiplex two 7-segment displays. The 74LS157 contains four 1-to-2 multiplexers, all of which have the same data-select input. See selected, when so is 1, all four D1 inputs are selected. Thus the output of the circuit is four parallel bits that have been selected from either the four D0 outputs or from the four D1 inputs, as shown in part (b) of the figure, the two 8-4-2-1 BCD numbers whose values are to be displayed, $A = A_8A_4A_2A_1$ and $B = B_8B_4B_2B_1$, are connected to the data inputs of the multiplexer.

The A bits are connected to the D0 inputs and B bits are connected to the D1 inputs. A square wave drives the data-select input. When the square wave is low, the D0 inputs are selected, so the A bits are routed to the output. When the square wave is high, the D1 inputs are selected and the B bits are routed to the output. The parallel output of the multiplexer is connected to the input of a 7449 BCD-to-7-segment-display decoder. Recall from the BCD-to-7-segment decoder experiment that this device provides the seven outputs needed to drive the segment that must be illuminated when its BCD input corresponds to any of the decimal digits from 0 through 9.

We see that the multiplexer alternately supplies the decoder with $A_8A_4A_2A_1$ and $B_8B_4B_2B_1$ at the frequency of the square wave, so the decoder alternately activates the segments for the decimal digits corresponding to $A_8A_4A_2A_1$ and $B_8B_4B_2B_1$.

The output of the 7-segment decoder is connected in parallel to two common-cathode 7-segment displays. However, we want only one display, A or B, depending on which BCD input has been selected to be illuminated. The common-cathode 7-segment is activated when its common line is made low. The 74LS39 2-to-4 decoder is used to logical 0 and square wave is connected to input 0, active-low decoder output D0 is low when the square wave is low (input = 00) and output D1 is low when the square wave is high (input = 01). These active-low outputs enable the 7-segment displays in proper sequence.

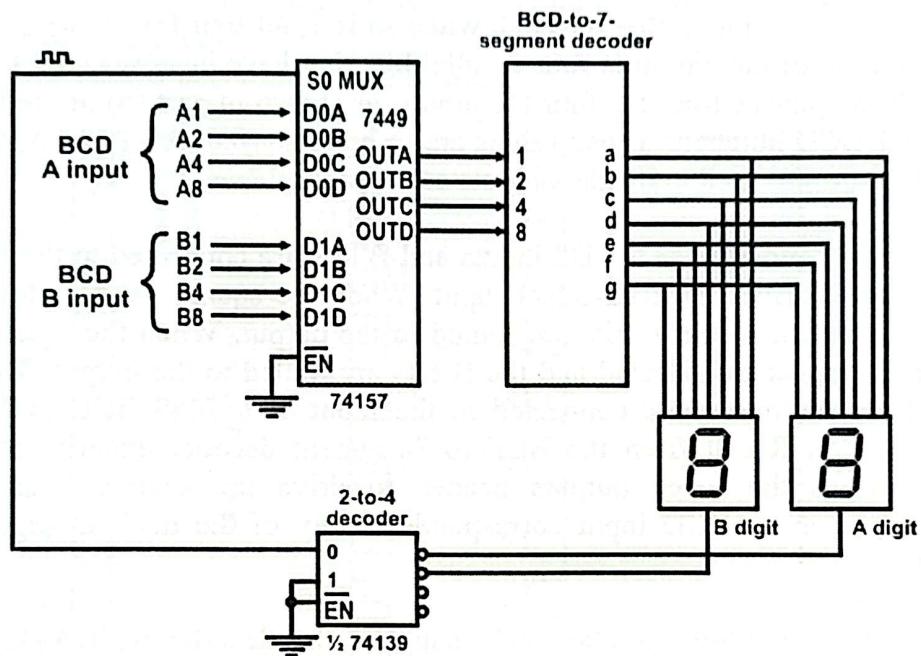
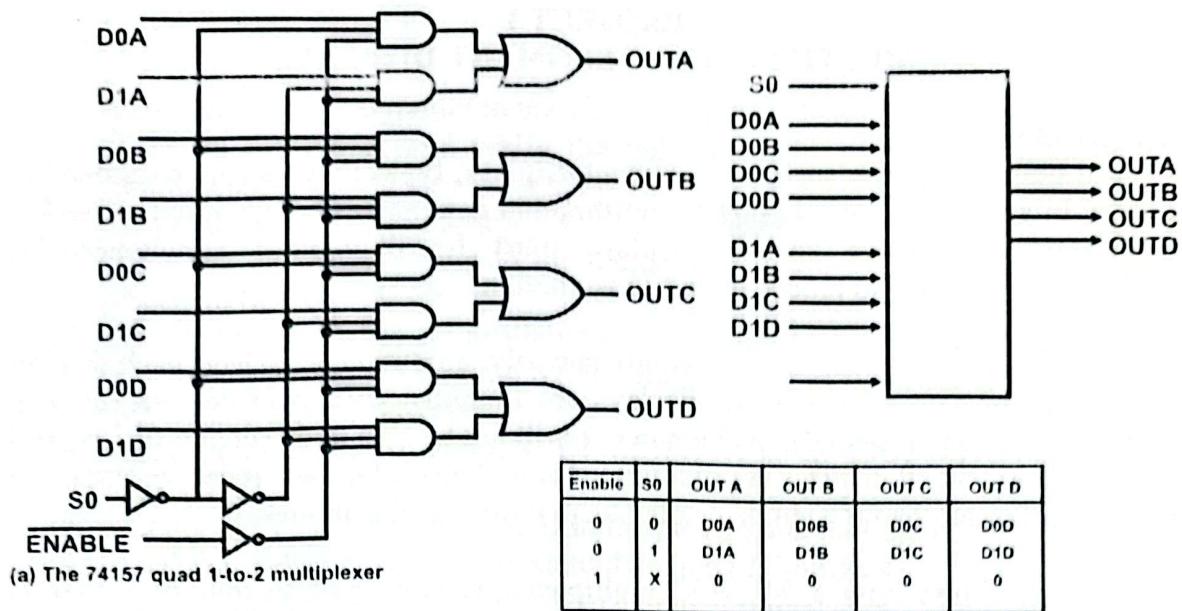


Fig. 1

Components

1. 74LS157 X 1
2. 74LS139 X 1
3. Common-Cathode Display x 2
4. 74LS49 X 2 : BCD-to-7-segment decoder

Tool

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezer

6. Pair of Pliers

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC's 74LS157, 74LS49, 74LS139 and displays on trainer's breadboard.
4. Wire the circuit according to the diagram in Figure 1.
5. For BCD input A, use logic switches S0 through S3 and for BCD input B, use logic switches S4 through S7.
6. Connect outputs of the multiplexer to the BCD input of the 7-segment decoder as shown in Figure 1.
7. Connect data select line (So) of multiplexer to the timer/clock output (CLK).
8. Supply the VCC= +5V and GND to all the ICs.
9. Test all the possible combination of BCD inputs A and B and verify the digits displayed at displays A & B are according to the BCD inputs A and B.
10. Observe how 7-segment display is enabled in proper sequence.

In case of trouble

1. Check the power supply.
2. Check the VCC and BND at pins 16 and 8 of the ICs.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.

EXPERIMENT 17

COMPARATOR OPERATION

Objective

To check the operation of 4-bit Magnitude Comparator using the IC 74LS85.

Comparators

A comparator is a logic circuit used to compare the magnitude of two binary numbers. It may simply provide an output that is active (goes High) when the two numbers are equal, or it may additionally provide outputs that signify which of the number is larger when equality does not hold. 74LS85 is a 4-bit magnitude comparator. Figure 18.1 shows this IC, which accepts two four-bit words at its inputs and produces one of three outputs, A>B, A=B, and A<B. Depending upon the status of the four-bit words at the inputs, the appropriate one of these outputs will be high and the other two will be low. $A_0A_1A_2A_3$ and $B_0B_1B_2B_3$ are two 4-bit numbers. Note from the Figure 18.2a that pins 4,5 and 6 are designated (A>B)in, (A=B)in are used for cascading.

Equipment

Component

1. 74LS85 x 1

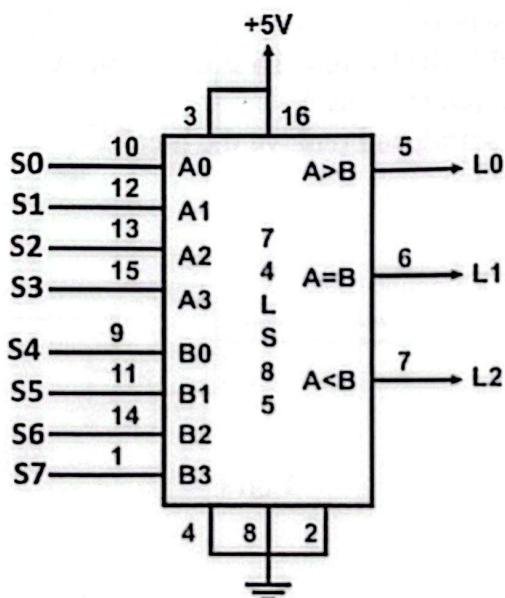
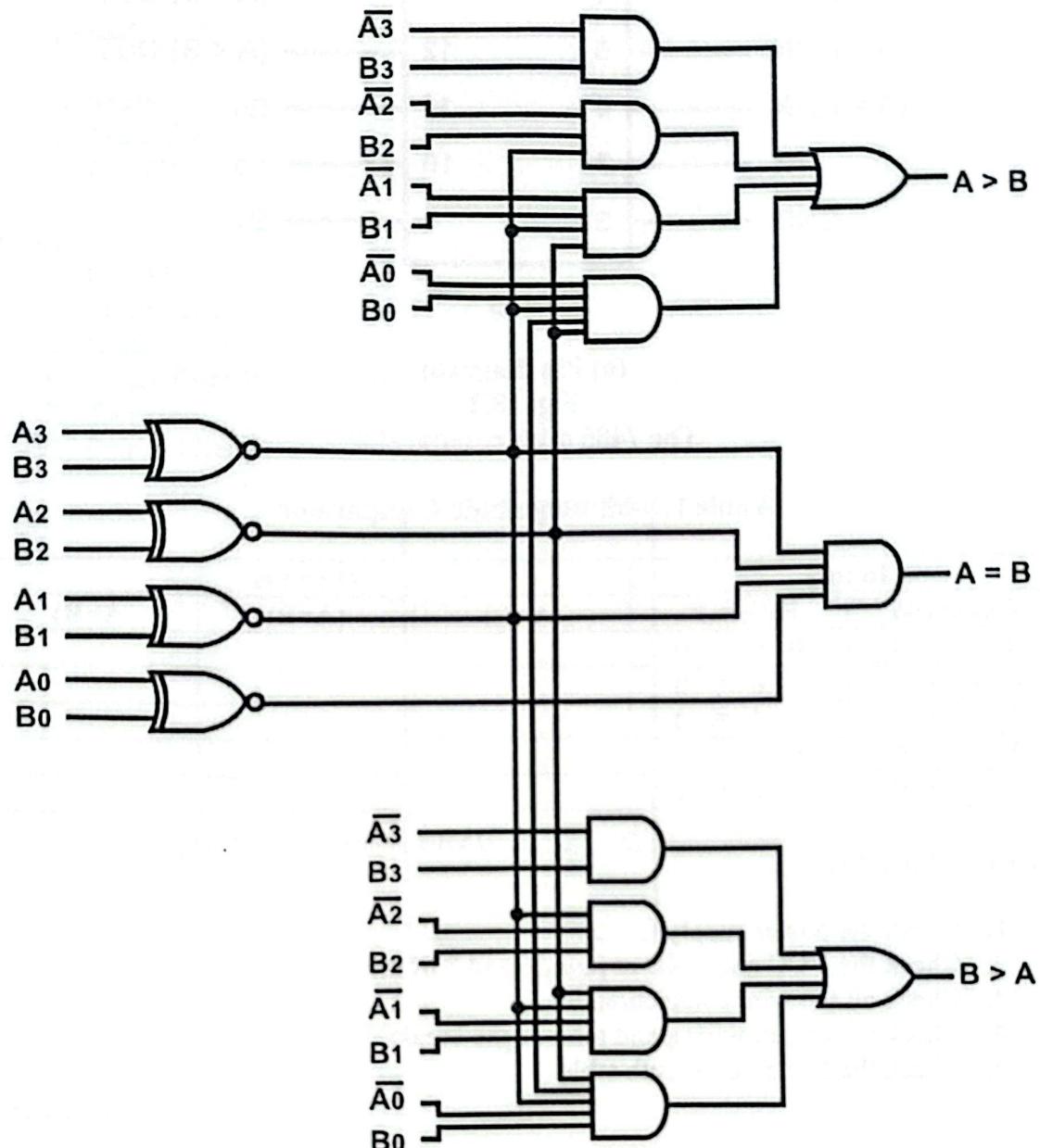


Fig. 18.1

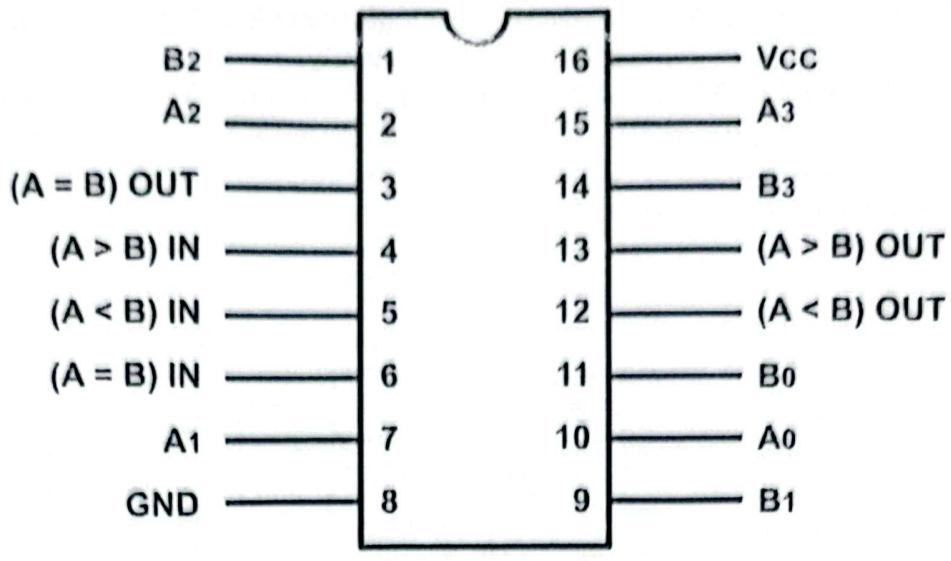
Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS85 on trainer's breadboard.
4. Wire the circuit by consulting the diagram in Figure 18.2.

- Supply the VCC = +5V and BND to the pins 16 and 8 of the IC.
- For binary input A ($A_3A_2A_1A_0$) use logic switches S5S4S3S2 and for B ($B_3B_2B_1B_0$) use switches S9S8S7S6 respectively.
- Use LED's L0, L1 and L2 for outputs ($A < B$) out ($A = B$) out and ($A > B$) respectively.
- For different settings of A and B, observe the outputs.
- Fill in the table 1 according to the results.



A 4-bit magnitude comparator used to determine which of inputs $A = A_3A_2A_1A_0$ and $B=B_3B_2B_1B_0$ is larger or if they are equal.



7485

(a) Pin diagram

Fig. 18.2

The 7485 4-bit comparator

Table 1. 4-bit magnitude Comparator

Inputs		Outputs		
$A_3 A_2 A_1 A_0$	$B_3 B_2 B_1 B_0$	$(A < B)$	$(A = B)$	$A > B$
0 0 1 0	0 0 0 0			
0 1 0 0	1 0 0 0			
1 1 0 0	1 1 0 0			
1 1 0 0	0 0 1 1			
1 0 0 0	1 0 0 1			

In case of trouble

1. Check the power supply.
2. Check the VCC and BND at pins 16 and 8 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using its truth table.

EXPERIMENT 18

D LATCH AND FLIP FLOP OPERATION

Objective

The experiment is to use the D latch and flip flop according to its truth table and to learn how it works by using IC 74LS75 Quad D Latch and 74LS74 Dual D Edge Triggered Flip-Flops.

Equipment

Components

1. 74LS75 x 1
2. 74LS74 x 1

Tools

1. IT-300
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezer
6. Pair of Pliers

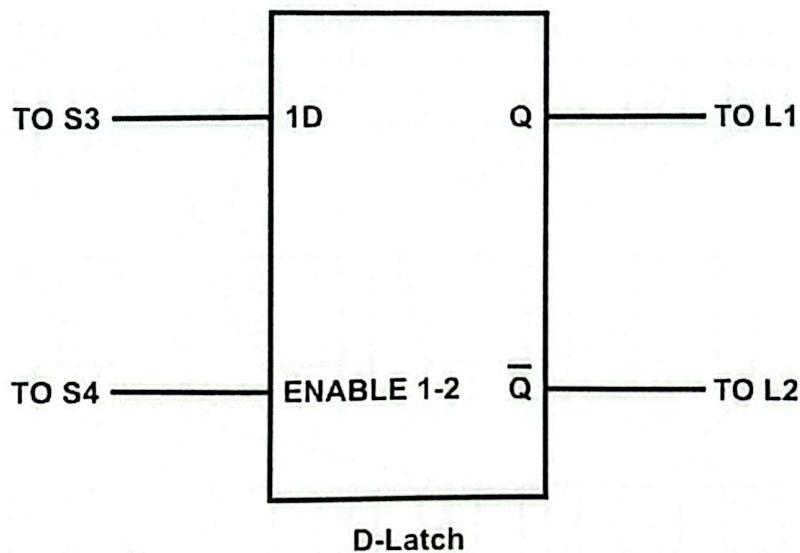


Fig. 19.1

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS75 on trainer's breadboard.
4. Wire the circuit according to the diagram in Figure 19.1 by consulting IC's data sheet in Figure 19.2.
5. Supply the VCC = +5V and GND to the pins 5 and 12 of the IC.
6. Connect Enable 1-2 to switch S4.

7. Change the setting of switch S3 and make switch S4 (Enable) High.
8. Observe the output is latched. That is, the output retains the data that was present at the input when the enable is made high.
9. Also observe that when Enable is high output is continually updated. The output follows any change in input when Enable is high. Thus this latch has an enable that requires a High level.
10. Fill the truth table given below according to the results.

Table 1 Truth Table for D Latch

Enable	Input	Output
E1-2	D	Q
0	1	
0	0	
1	1	
1	0	

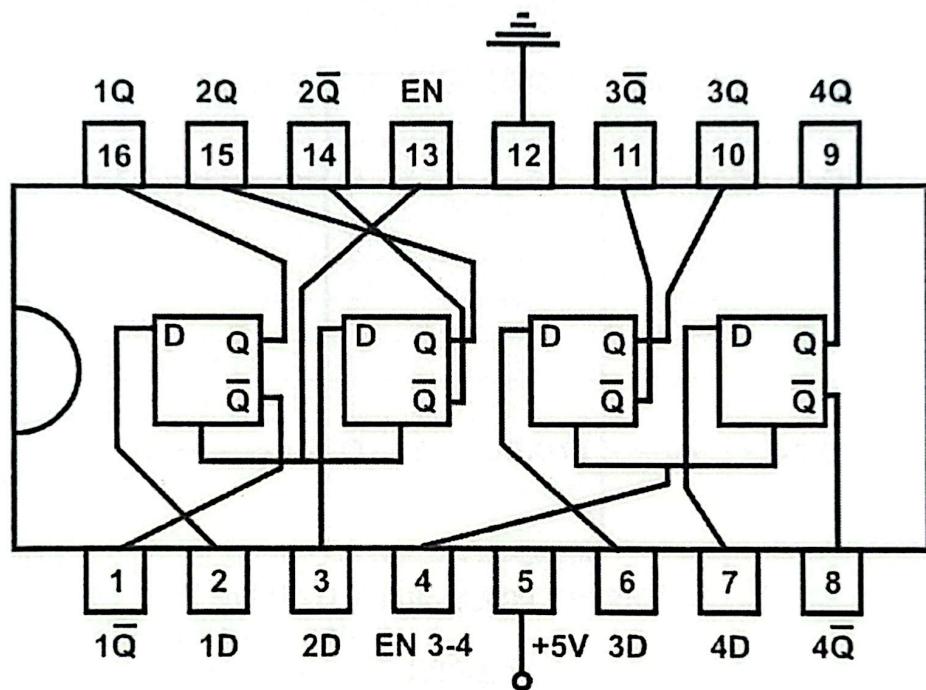
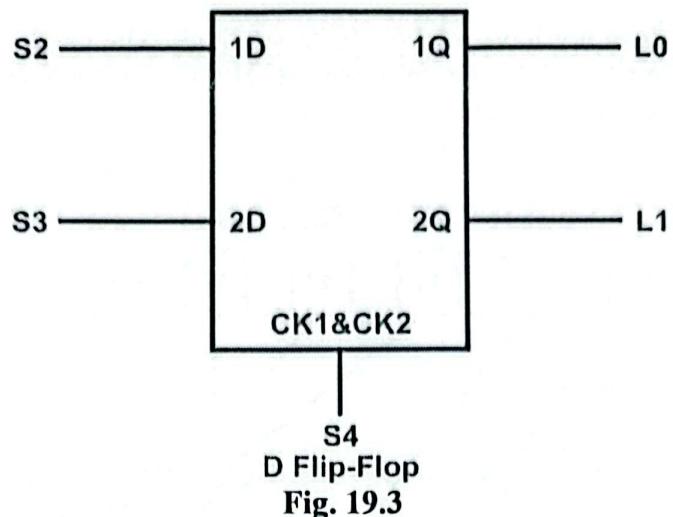


Fig. 19.2

74LS75 Quad D Latch



Procedure

1. Install the IC 74LS74 on the trainer's breadboard.
 2. Connect switches S2 and S3 to inputs ID and 2D respectively.
 3. Connect LED's L0 and L1 to outputs 1Q and 2Q respectively.
 4. Connect S4 to CK1 and CK2 pins of the IC.
 5. Recognize that S4 controls the clock for the flip-flops. We will determine what is required on the clock to allow data to transfer. There are four possibilities:
 - Low level
 - High level
 - Positive Edge (Low to high change)
 - Negative edge (High to Low change)
 6. Set switches S2 and S3 to High and S4 to low. Now move S4 to High and back Low again. Both LED's L0 and L1 should read 1: do they? -----
 7. Set S2 to low. The L0 display should indicate 1. Does it? What is the L1 LED indicating? -----
 8. Now move S4 to high. Do the L0 LED updated to new information? -----
 9. Move S2 to high and S3 to low position. Do the LED's L0 and L1 update to the new data?-----
 10. Move S4 to low. Any change in the LED's?-----
 11. Now move S4 to high. Any change now?-----
 12. Therefore, what is required to the output?-----
 - (1) Low Level
 - (2) High level
 - (3) Positive edge
 - (4) Negative edge
 13. We should have seen that the D flip-flop would not transfer data if the clock is held Low or held high.

14. That is, it does not have a level sensitive clock. The clock responds only to a positive transition (change from low to High). The output follows the input when the transition occurs.

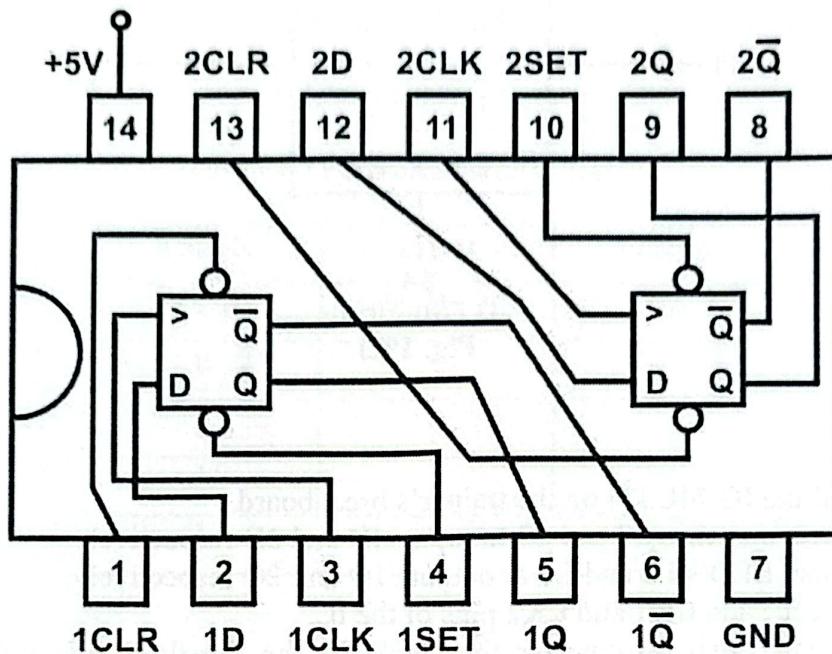


Fig. 19.4
74LS74 Dual D Edge Triggered Flip-Flops

In case of trouble

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using its truth table.

EXPERIMENT 19

LATCHING BCD DATA FOR DISPLAYING ON 7-SEGMENT DISPLAY

Objective

The experiment is to learn how a D latches can be used to latch BCD data using IC 74LS75 Quad D Latch, IC 74LS47 7-segment Decoder/Driver and common anode 7-segment display.

Equipment

Components

1. 74LS75 x 1
2. 74LS47 x 1
3. Common anode display

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezer
6. Pair of Pliers

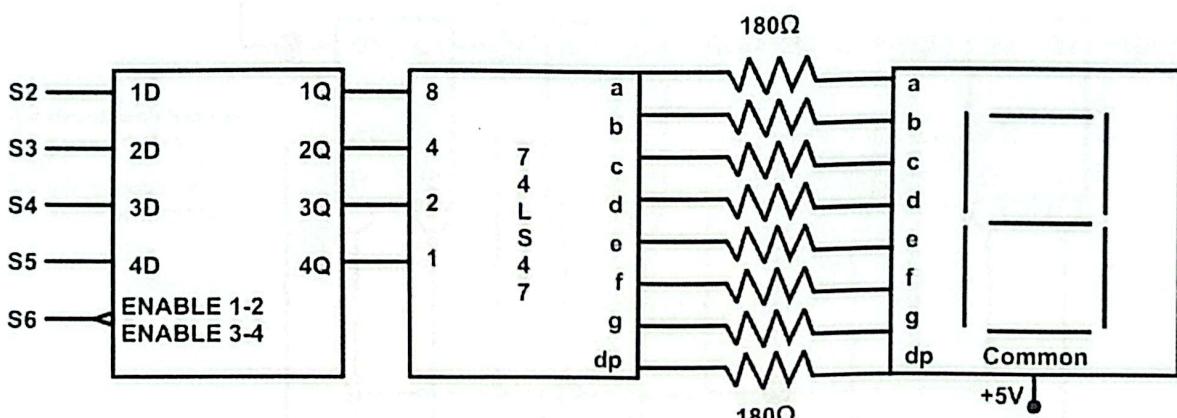


Fig. 20.1

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS75 on trainer's breadboard.
4. Supply the VCC = +5v and GND to the pins 5 to 12 of the IC.
5. Wire the circuit according to the diagram using IC's data sheet.
6. Use logic switches S2 through S5 for inputs 1D through 4D.
7. Connect the enable signals coming out of each flip-flop (Enable 1-2 and Enable 3-4) to S6. Connect the outputs 1Q through 4Q 7Q LS 54 to BCD input 8421 of 7447 respected available on SBB-63.

8. Input different BCD words using switches S2 through S5 and then set S6 to High.
9. Observe that the output is latched and corresponding digit is displayed on 7-segment display. That is, the output retains the data that was present when the enable is high.
10. Also observe that when Enable is high, the output follows any change in input.

In case of trouble

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the ICs.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using its truth table.

EXPERIMENT 20

RECALCULATING DATA

Objective

The experiment is to examine the concept of shifting data around in a circular shift register. By presetting the flip-flop any desired output pattern can be generated.

Equipment

Components

1. 74LS47 x 1

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezers
6. Pair of Pliers

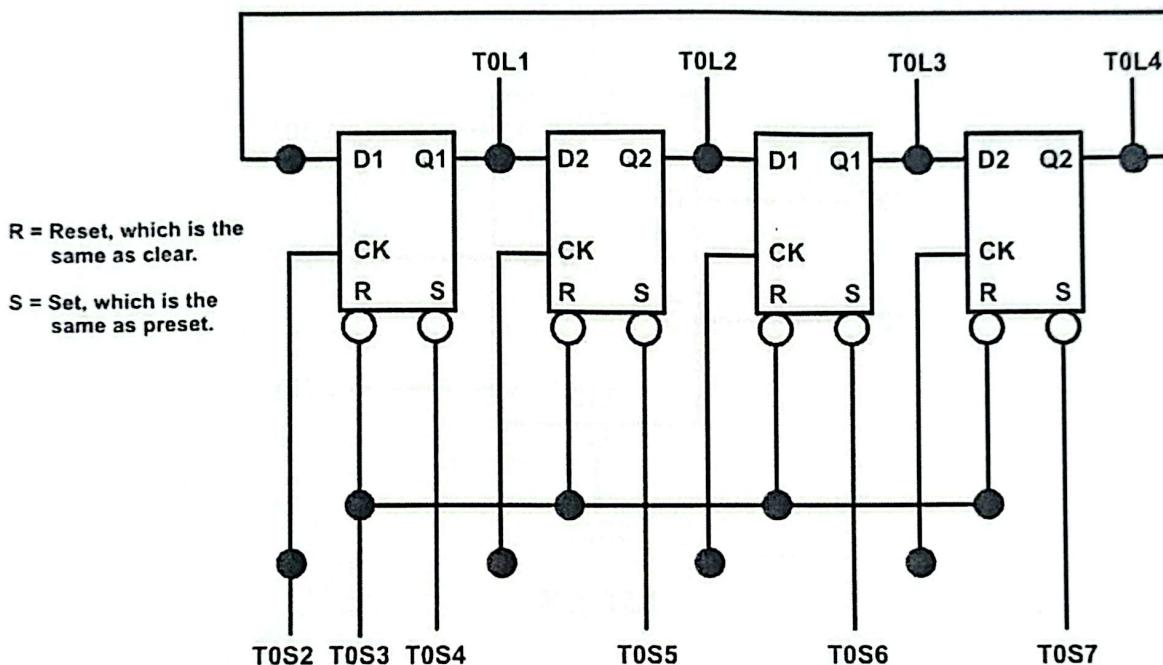


Fig. 21.1

Procedure

1. Install the Two 74LS74 ICs on the trainer's breadboard.
2. Wire the circuit according to the diagram in figure in 21.1.
3. Set S2 to Low. Set S4, S5, S6 and S7 to High.
4. Set S3 to Low and then back to high. This resets all flip-flops. All four LED's should be OFF.
5. Move S4 to Low and then back high. This has set (preset) the first flip-flop; its Q output should be high and L1 should be lit.

6. Now cycle the data through the ring of flip-flops by supplying a clock signal. Move S2 to High and then back Low again. Note that the High has moved to L2.
7. Again cycle S2 High and then Low. The data again should have shifted one position.
8. Continue to cycle S2, observing that four clock are needed to get the data completely around the loop.

In case of trouble

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the ICs.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using its truth table.

EXPERIMENT 21

J-K FLIP FLOP OPERATION

Objective

The experiment is to use the J-K flip-flop according to its truth table and to learn how it works by using IC 74LS76 Dual J-K Flip-Flops.

Equipment

Components

1. 74LS76 x 1

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezer
6. Pair of Pliers

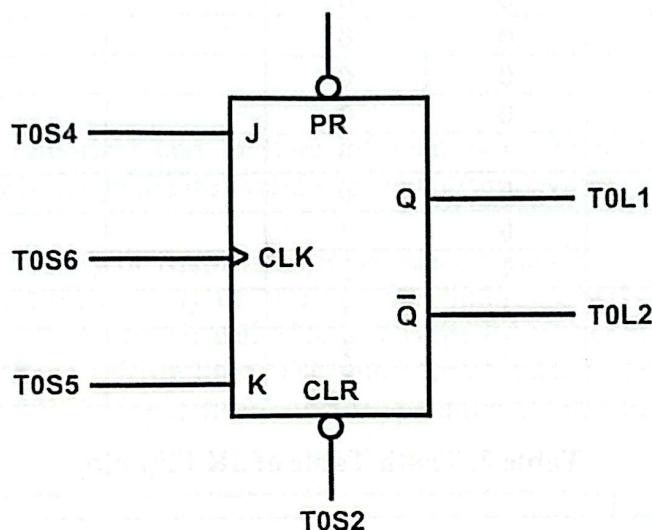


Fig. 22.1

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS76 on trainer's breadboard.
4. Wire the circuit according to the diagram using IC's data sheet.
5. Supply the VCC = +5V and GND to the pins 14 and 7 of the IC.
6. Set the switches as shown in table – 1 and record the indications of L1 and L2.
7. Analyze your result to determine some conclusions about the JK.
8. When Clear and Preset is both High, does the output respond to the J, K and clock inputs?-----

9. When Clear is Low, does Q get held Low or High? -----
10. When preset is Low, does Q get held Low or High? -----
11. With Highs on Preset, clear, J and K what happens to the output with each successive clock pulse?
12. Test all possible combinations of inputs, verify the output and fill the Table 2.

Table 1

Inputs					Outputs		CLR = Clear which is the same as reset
S2=CLR	S3=PRE	S4=J	S5=K	S6=CLK	L1=Q	L2=Q'	
1	1	1	0	0-1-0	1	0	1 RESPOND TO J & k
1	1	0	0		1	0	
1	1	0	1		0	1	
1	1	0	0				
1	1	1	0				
1	1	0	1				
1	1	1	0				
0	1	1	0				
0	1	0	0				
0	1	0	0				
1	0	0	0				2 HELD IN CLEAR
1	0	1	0				
1	0	0	0				
1	0	0	1				
1	1	1	1				3 HELD IN PRESET
1	1	1	1				
1	1	1	1				
1	1	1	1				
4	TOGGLE						

Table 2. Truth Table of JK Flip Flop

Mode	Inputs		Outputs			Effect on Q
	J	K	Q	Q'		
Hold	0	0				
Reset	0	1				
Set	1	0				
Toggle	1	1				

In case of trouble

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the ICs.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using its truth table.

EXPERIMENT 22 RANDOM ACCESS MEMORIES

Objective

To check the Read / Write operation of a RAM.

Equipment

Components

1. 74LS47 x 1
2. 74LS93 x 1
3. 74LS170 x 1

Tools

1. IT-300 Trainer
2. Multimeter
3. Cutter
4. Single Core Wire
5. Tweezers
6. Pair of Pliers

Theory

A memory is an important part to store information. Computer memories include tapes, punched cards, magnetic disks and semiconductor devices.

Random Access Memory or RAM is a semiconductor memory wherein any location is accessible to retrieve (read) or store (write) information regard to any other location. In a Figure 16.1 a basic cell of Read / Write RAM which consist select, data input, output and Read / Write lines. The select input enables the cell for writing or reading. The Read / Write input determine the operation on the selected cell.

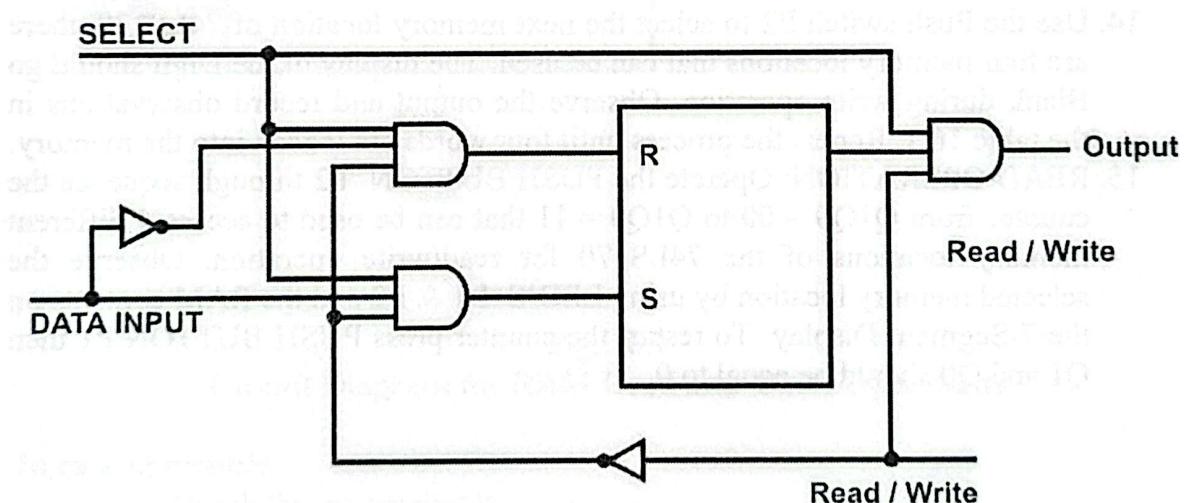


Fig. 16.1
A RAM CELL

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. WRITE OPERATION: Install the 4 x 4 RAM chip 74LS170 and the binary counter 74LS93 on the trainer's breadboard.
4. Wire the circuit as shown in the Figure 16.2.
5. Use logic switches S5 to S2 for data inputs A to D.
6. To read and write enable inputs, i.e., pin # 11 and # 12(74LS170), use logic switches S0 and S1 respectively.
7. Use LED L2 and L1 for outputs Q1 and Q0 of the counter.
8. The outputs of the Binary Counter 7493 that are Q1 and Q0 which are connected to the read / write select inputs of the RAM.
9. Set logic switches S0 (read operation) & S1 (write operation) to low state.
10. Now set the memory address using P2.
11. Set logic switches S2 to S5 to any state that you want to store in desired memory address.
12. Set S1 to high state and press P2 (selection of memory address) to move next memory location and read the binary word from memory address.
13. Observe the output and record your observation in table 16.1.

Table 16.1

Address		Binary Word Loaded				Output Display
Q1	Q0	S5	S4	S3	S2	
0	0					
0	1					
1	0					
1	1					

14. Use the Push switch P2 to select the next memory location of 74LS170, there are four memory locations that can be used. The display of the Digit should go Blank during write operation. Observe the output and record observations in the table 16.1. Repeat the process until four words are loaded into the memory.
15. READ OPERATION: Operate the PUSH BUTTON P2 through sequence the counter from Q1Q0 = 00 to Q1Q0 = 11 that can be used to access 4 different memory locations of the 74LS170 for read/write operation. Observe the selected memory location by using LED'S L1 & L2 and the RAM contents on the 7-Segment Display. To restart the counter press PUSH BUTTON P1 then Q1 and Q0 should be equal to 0 .

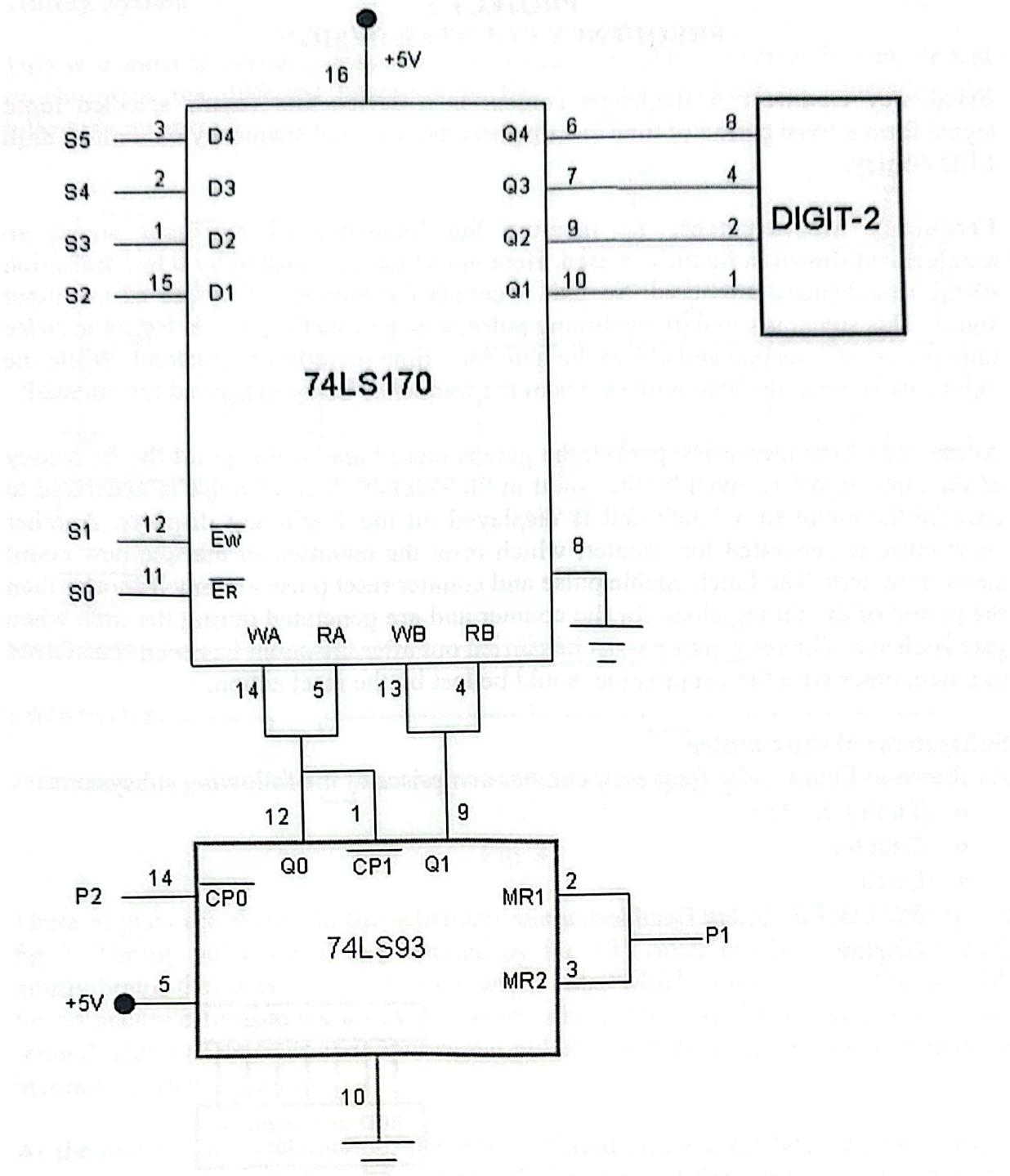


Fig. 16.2
Circuit Diagram for RAM Read and Write Operations

In case of trouble

1. Check the power supply.
2. Check the V_{CC} and GND of the ICs.
3. Check the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using its truth table.

PROJECT 2

FREQUENCY COUNTER DESIGN

Frequency Counter: A frequency counter is a device that counts selected input signal form a fixed period of time and displays the resultant frequency on a multi digit LED display.

Frequency Measurement: To measure the frequency of an input signal an arrangement shown in figure 1 is used. Here the counter is clocked by 0 to 1 transition of the signal being measured. So that it counts the number of cycles of the input signal. This signal is gated by the timing pulse, which turns the gate on for an accurate time period of 1 second and closes the gate for a time period of 0.2 second. While the input gate is open, the incoming cycles of the frequency being measured are counted.

At the end of the measuring period, the gate is closed and at this point the frequency of the input signal is given by the count in the counter. A short pulse is generated to transfer the count to a Latch and is displayed on the 7-segment displays. Another short pulse is generated for counter, which reset the counters so that the new count starts from zero. The Latch enable pulse and counter reset pulse are much shorter than the period of the timing clock for the counter and are generated during the time when gate is closed. The reset action must be carried out after the count has been transferred to Latch, other wise the count value would be lost by the reset action.

Subsystems of the counter

As shown in figure 1, the frequency counter comprises of the following subsystems.

- Timing System
- Counter
- Latch
- BCD to 7-Segment Decoder/Driver
- Display

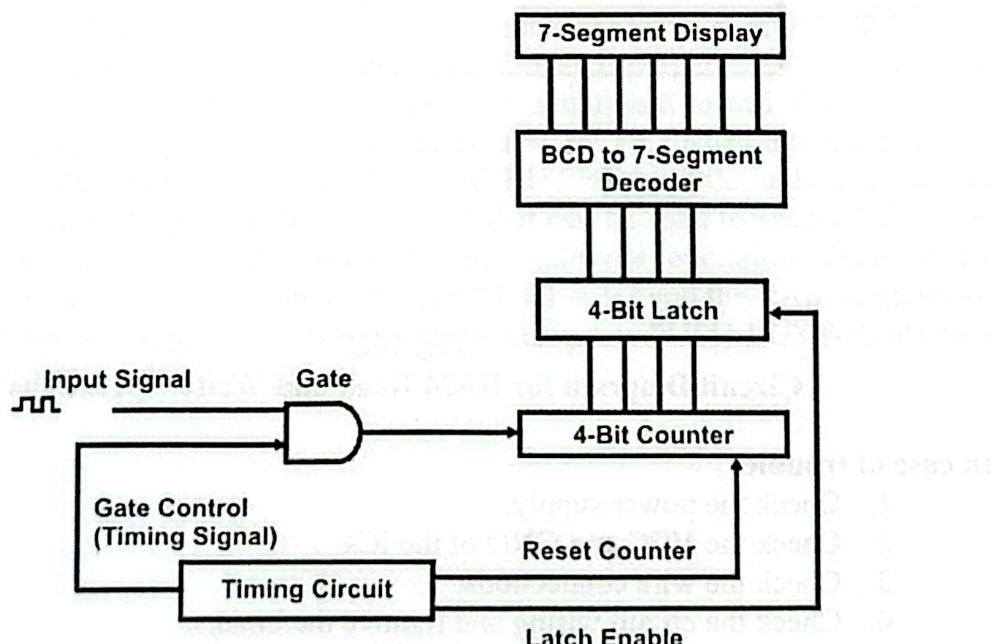


Fig. 1

Timing System

This is a most important subsystem in a frequency counter system. It controls and synchronizes the different operation of the frequency counter by generating the following pulses:

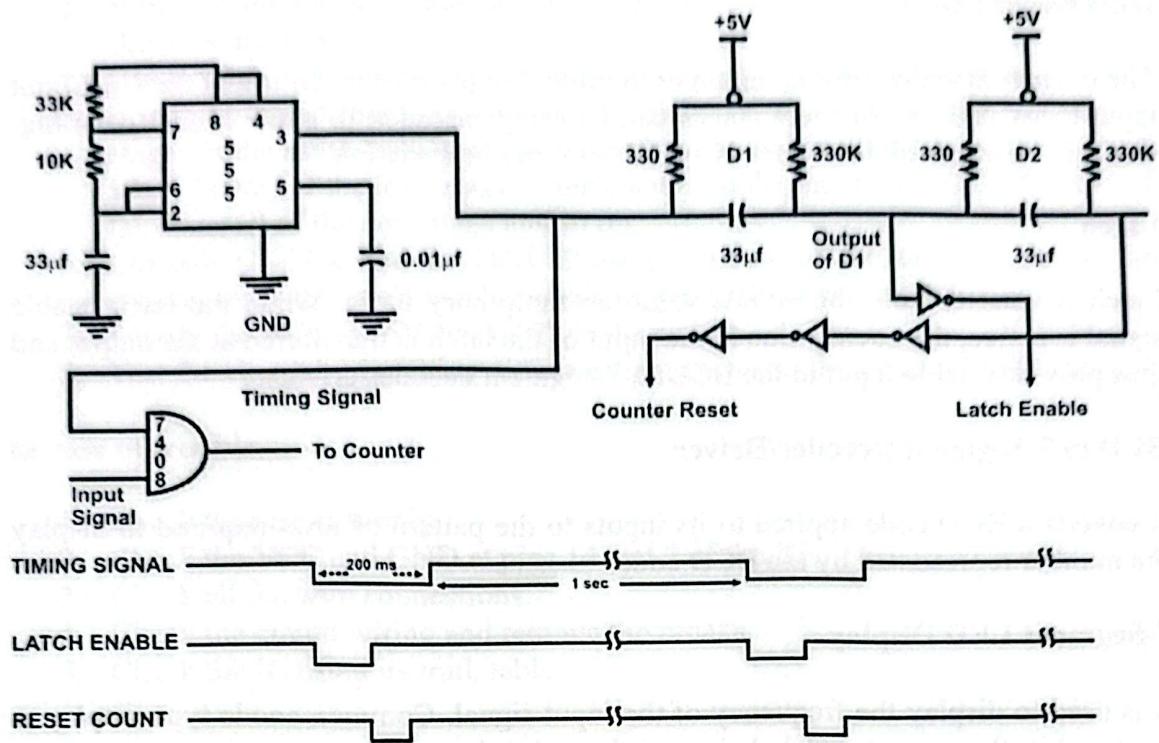


Fig. 2

These signals are shown in the schematic diagram along with the timing diagram in fig 2. Timing pulse signal is generated by the 555 timer configured as an astable multivibrator that puts out a fixed time width pulse which is used to turn the gate ON for an accurate time period of 1 second and closes the gate for a time period of 0.2 second. During ON time, the input signal pulses clock the counter, which counts the incoming signal frequency.

At the end of this (ON) period, the gate is closed and a short latch enable pulse is generated to transfer the count to a latch. Falling edge of the timing pulse is detected by the differentiator D1 and it produces a negative-going pulse of 2ms duration. This pulse is passed through an inverter to get a well-shaped pulse of 2ms duration to enable the latch. Another differentiator D2 is used to detect the falling edge of the signal at the output of the D1. It generates the negative-going pulse (counter reset signal) of 2 ms, which is then passed through three inverters to get an appropriate delay. This signal is used to reset the counter to zero.

Counter

4-bit synchronous decade counter (74192) is used which divide the input frequency by 10 and can count in either direction. Viewed from another perspective, it can be thought of as counting the input pulses and signaling (via a single output pulse) when it has reached 10.

The counter advances one count on each ground to positive transition of the Up-Count input clock and two or more stages can be carry cascaded to allow higher counting. Consult the attached data sheet of 74192 for more information.

Latch

Latch is used to hold the counts value on temporary basis. When the latch enable signal is active, the count value at the input of the latch is transferred at the output and thus provides stable input to the BCD to 7-segment decoder/drivers.

BCD to 7-Segment Decoder/Driver

It converts a BCD code applied to its inputs to the pattern of lows required to display the number represented by the BCD code.

7-Segment LED Display

It is used to display the frequency of the input signal. Common anode type display is used and its 8-segments is labeled as 'a' through 'g'.

Frequency Counter

Objective

To design a frequency measuring circuit to count from 0-999Hz.

Components and Tools

- 74192 x 3 Decade UP/DOWN Counter
- 7408 Quad 2-input AND Gate
- 74175 x 3 Quad D +ve Edge-Clocked Latch
- 555 Timer
- 7447 x 3 BCD to 7-segment Decoder/Driver
- Common Anode LED Display x 3
- Resistances: 180 x 24 , 330 x 2 , 3.3K x 3 , 33K, 10K
- Capacitors: 33uFx3, 0.01uF
- IT-300 Trainer

Procedure

1. Connect the IT-300 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of power supply using multimeter, it should be +5V exactly.
3. Wire the circuit according to the diagram in fig. 3 by consulting the data sheets of the ICs.
4. Use BCD to 7-Segment decoder/driver provided on the IT-300 trainer.
5. It is to be noted that only one stage is shown here, construct the rest of two stages in the same fashion and cascade them by connecting the carry out (pin# 12 of 74192) of the least stage of the counter to the input UP COUNT (pin#5 of the counter) of the next stage and so on.
6. Connect CLEAR and LATCH ENABLE inputs of the three stages to the counter reset and latch enable signals respectively as shown in figure 3.
7. Supply the VCC = +5V and GND to the circuit.
8. Test the circuit by inputting different frequencies in the range of 0-999Hz.

In case of trouble

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the ICs.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using its truth table.