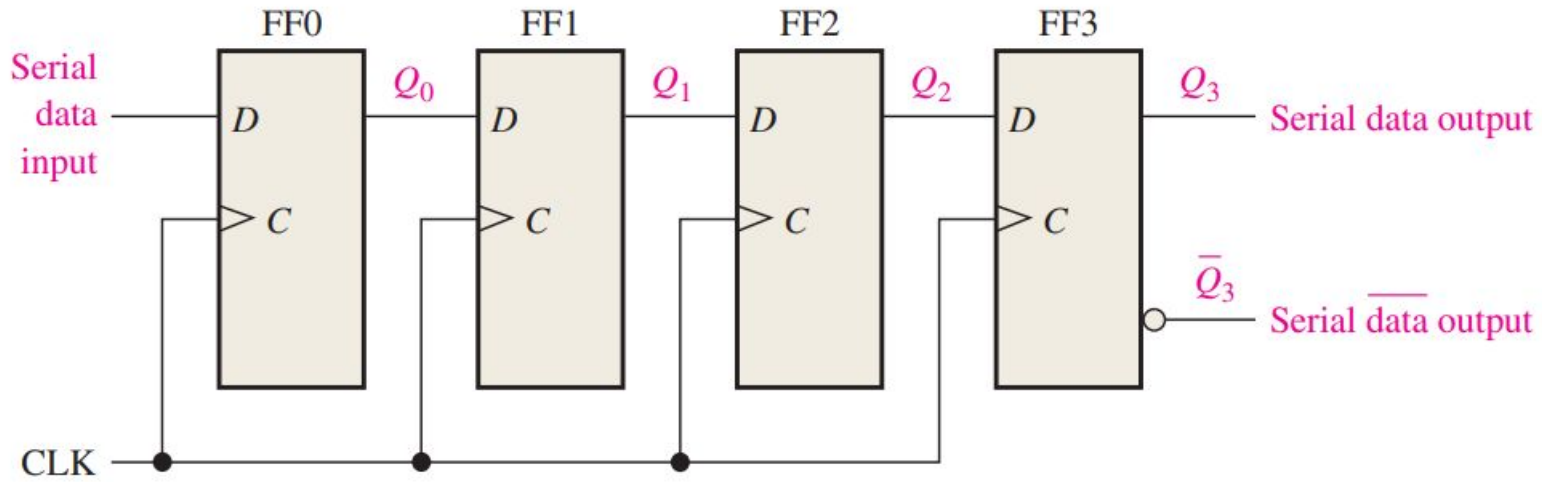
Shift Registers

Abdul Ghafoor

Shift Register

- Shift registers consist of arrangements of flip-flops and are important in applications involving the storage and transfer of data in a digital system.



Principal functions are performed by a Shift Register

- A register is a digital circuit with two basic functions: data storage and data movement.
- The storage capability of a register makes it an important type of memory device.
- The storage capacity of a register is the total number of bits (1s and 0s) of digital data it can retain.
- Each stage (flip-flop) in a shift register represents one bit of storage capacity; therefore, the number of stages in a register determines its storage capacity.

Principal functions are performed by a Shift Register

- The shift capability of a register permits the movement of data from stage to stage within the register

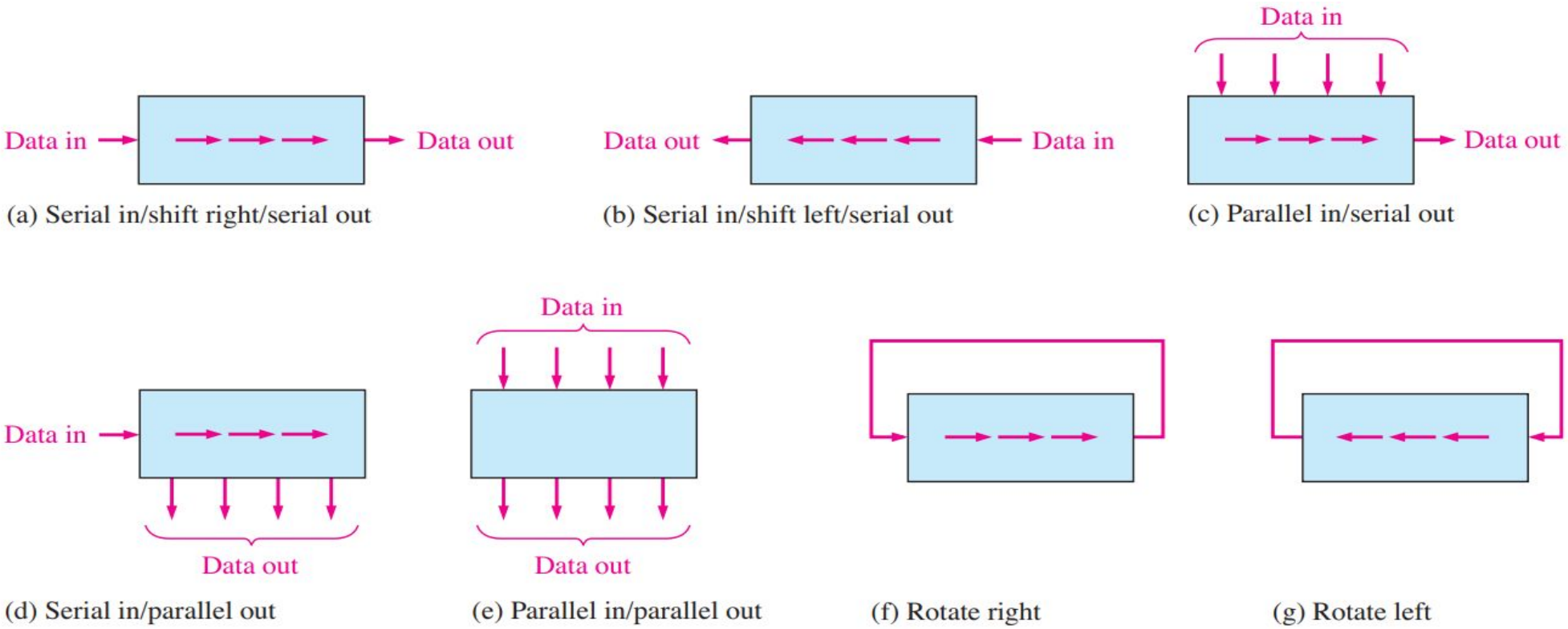


FIGURE 8–2 Basic data movement in shift registers. (Four bits are used for illustration. The bits move in the direction of the arrows.)

Types of Shift Register Data I/Os

1. Serial in/serial out
2. Serial in/parallel out
3. Parallel in/serial out
4. Parallel in/parallel out

Serial In/Serial Out Shift Registers

- The serial in/serial out shift register accepts data serially—that is, one bit at a time on a single line. It produces the stored information on its output also in serial form.

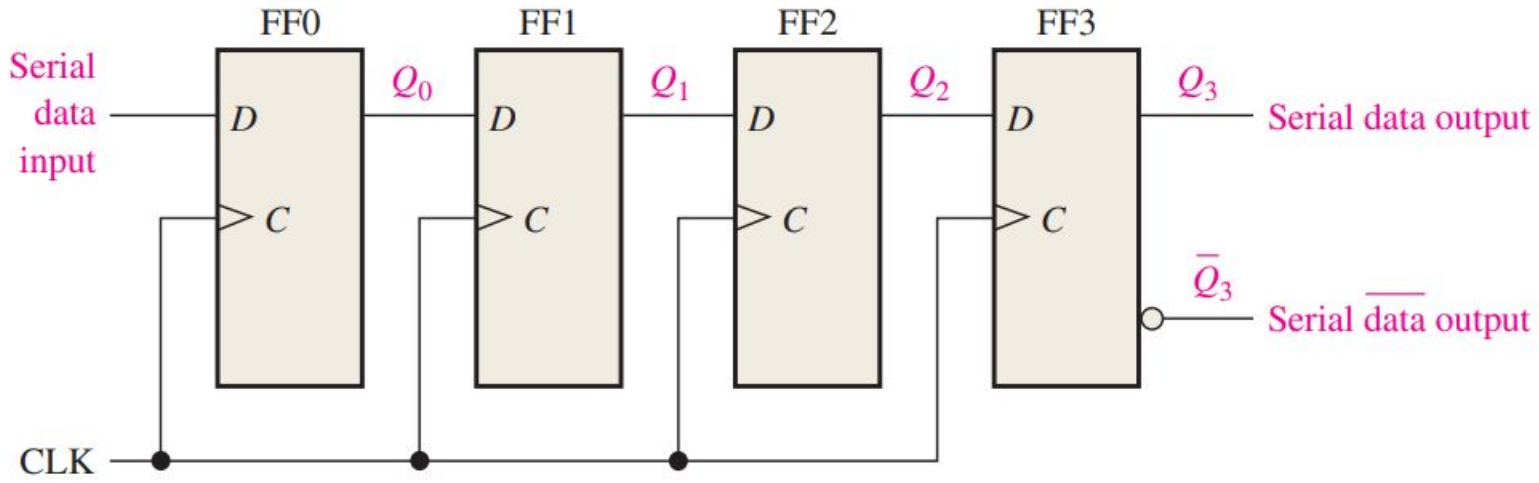


FIGURE 8–3 Serial in/serial out shift register.

Serial In/Serial Out Shift Registers

- Table below shows the entry of the four bits 1010 into the register in Figure illustrated in previous slide. The register is initially clear.

CLK	FF0 (Q_0)	FF1 (Q_1)	FF2 (Q_2)	FF3 (Q_3)
Initial	0	0	0	0
1	**0**	0	0	0
2	**1**	**0**	0	0
3	**0**	**1**	**0**	0
4	**1**	**0**	**1**	**0**

Serial In/Serial Out Shift Registers

Shifting a 4-bit code out of the shift register in Figure 8–3. Data bits are indicated by a beige screen.

CLK	FF0 (Q_0)	FF1 (Q_1)	FF2 (Q_2)	FF3 (Q_3)
Initial	**1**	**0**	**1**	**0**
5	0	**1**	**0**	**1**
6	0	0	**1**	**0**
7	0	0	0	**1**
8	0	0	0	0

Serial In/Parallel Out Shift Registers

- Data bits are entered serially (least-significant bit first) into a serial in/parallel out shift register in the same manner as in serial in/serial out registers.
- The difference is the way in which the data bits are taken out of the register; in the parallel output register, the output of each stage is available.
- Once the data are stored, each bit appears on its respective output line, and all bits are available simultaneously, rather than on a bit-by-bit basis as with the serial output.

Serial In/Parallel Out Shift Registers

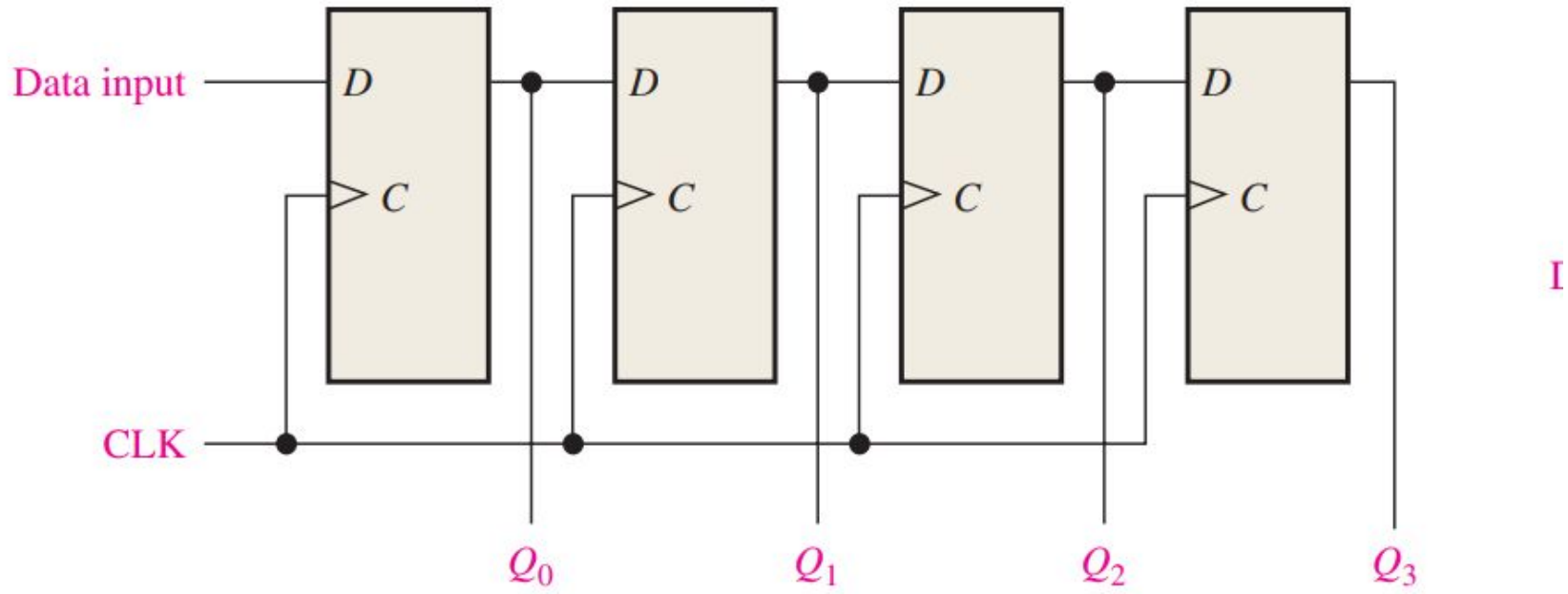
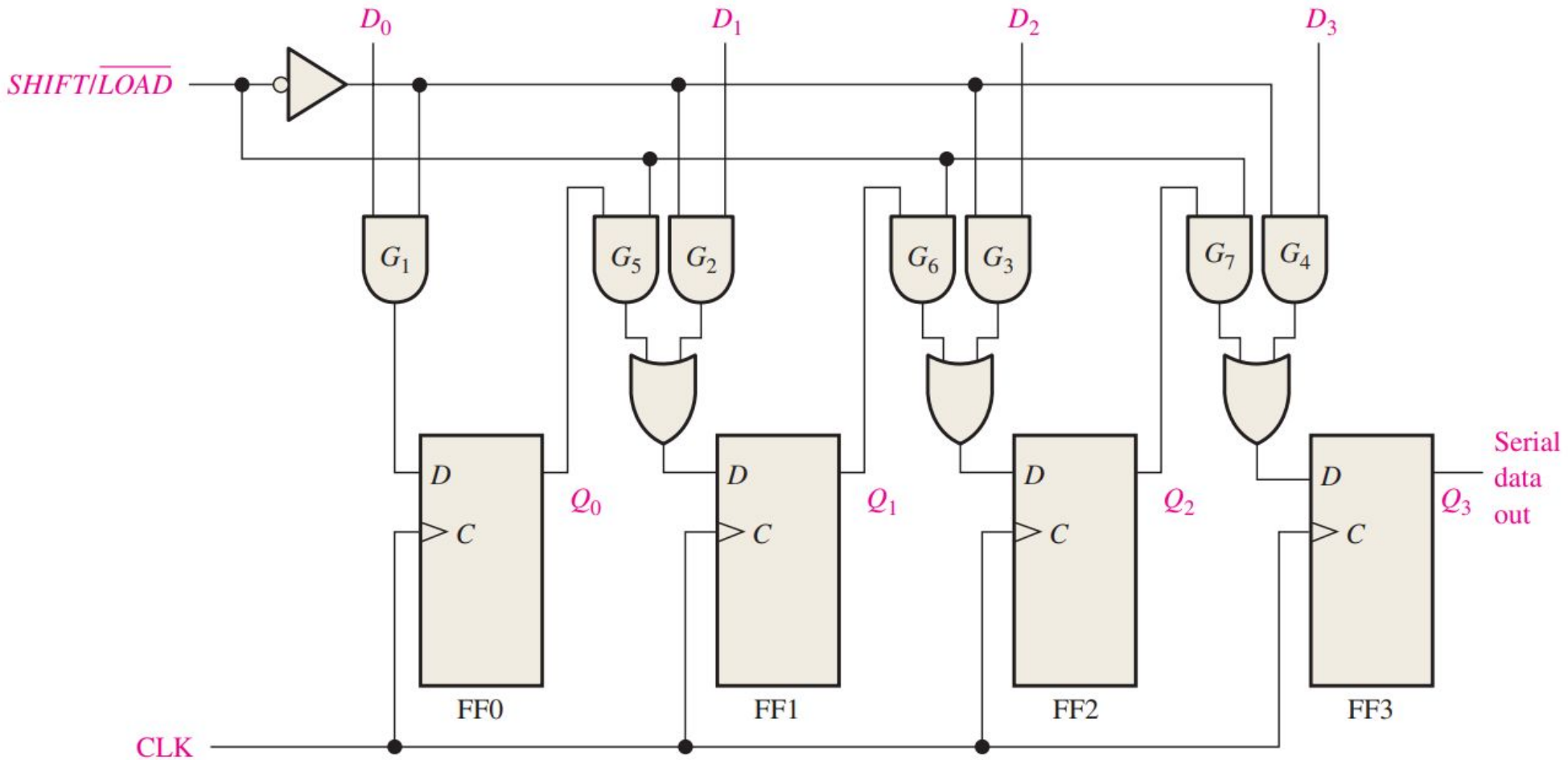


FIGURE 8–6 A serial in/parallel out shift register

Parallel In/Serial Out Shift Registers

- For a register with parallel data inputs, the bits are entered simultaneously into their respective stages on parallel lines rather than on a bit-by-bit basis on one line as with serial data inputs.
- The serial output is the same as in serial in/serial out shift registers, once the data are completely stored in the register

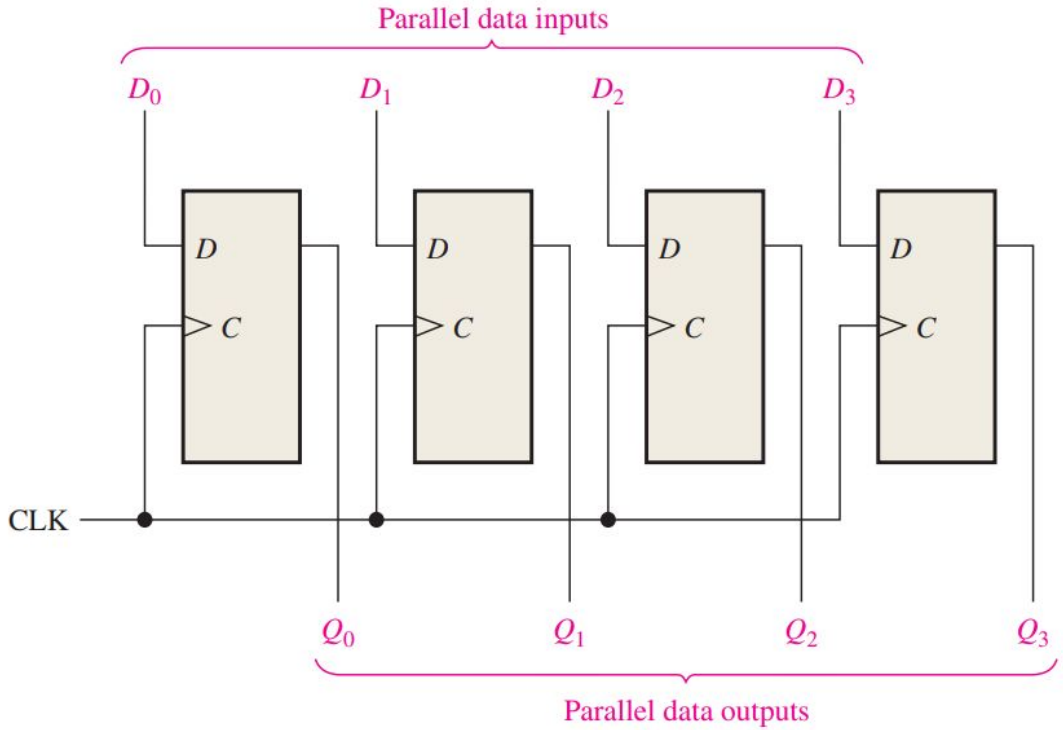
Parallel In/Serial Out Shift Registers



(a) Logic diagram

Parallel In/Parallel Out Shift Registers

- PIPO shift registers have multiple data lines for input and output, allowing entire data (i.e., multiple bits) to be loaded in or read out simultaneously. Unlike serial shift registers, where data bits are entered or exited one at a time.



Bidirectional Shift Register

- A bidirectional shift register is one in which the data can be shifted either left or right.
- It can be implemented by using gating logic that enables the transfer of a data bit from one stage to the next stage to the right or to the left, depending on the level of a control line.

Bidirectional Shift Register