|  |  |
| --- | --- |
| **Formula** | **Explanation** |
| Diode types | **Types of Diodes & Their Basic Uses**   | **Diode Type** | **Basic Use / Application** | | --- | --- | | 1. PN Junction Diode | Basic rectification (AC to DC), switching | | 2. Zener Diode | Voltage regulation, voltage clamping | | 3. Schottky Diode | High-speed switching, low voltage drops (used in SMPS, RF) | | 4. Light Emitting Diode (LED) | Light emission in displays, indicators | | 5. Photodiode | Converts light to current (used in sensors, solar cells) | | 6. Tunnel Diode | Very fast switching; works in negative resistance region (microwave, oscillator) | | 7. Varactor (Vari cap) Diode | Acts as a voltage-controlled capacitor in RF tuning circuits | | 8. Laser Diode | High-intensity light in fibre optics, laser pointers | | 9. Avalanche Diode | Used for protection, operates in avalanche breakdown | | 10. PIN Diode | RF switch and attenuators (low noise, high freq.) | | **11. Flyback (Freewheeling) Diode** | Protects switching devices from voltage spikes in inductive loads (e.g., across relays, motors) |   Example of diode names and properties      VI characteristics of a PN junction diode (in forward bias (acting as conductor) and in reverse bias(acting as insulator)) |
| Reverse saturation current | In diode/PN junction diode (both are same) – when we connect it in reverse bias a small amount of current flows through it due to travelling of minority carriers (electrons in P region and holes in N region) – that is called reverse saturation current    Here when due to reverse voltage (minority carriers travels to their respective regions generating flow of electron / holes (current)  (they are now in the range of nA)  Reverse saturation current ( Temp)  As the temp rises the increases [ every 10 rise in temp leads to doubling in value |
| Avalanche breakdown and Zener breakdown effect | Due to application of large reverse voltage breakdown of diode occurs (it then starts conducting in the reverse bias as well) – this is called avalanche effect  **Zener Effect**: Think of the depletion layer as a **very thin wall**. When reverse voltage is applied, **quantum tunnelling** allows electrons to **"go through"** this thin barrier. Happens at **low voltages**.  **Avalanche Effect**: Here, the wall is **thicker**. Electrons **gain enough energy** from the high reverse voltage to **slam into atoms**, knocking more electrons loose — like an **avalanche** of charge carriers.  Temp effect on Zener and avalanche effect  Breakdown volt < 4v : Zener effect is dominant (negative temp Coeff = as the temp increases the breakdown volt will also reduce)  Breakdown volt > 6v : Avalanche effect is dominant (positive temp Coeff = as the temp increases the breakdown volt will also increase) |
| Zener diode | Zener diode is heavily doped in both P and N region compared to normal PN junction diode …that’s why their regions are mentioned as P+ and N+    VI characteristics of Zener diode    Zener diode comes from 2v to 200v (normal diodes have breakdown volt >20v)    Zener diodes allow max of current and min of current(also known as knee current) (hence it is always suggested to use a resistor(to limit current) in series with Zener to avoid Zener being damaged)    and ( it says Zener is operating properly in the breakdown region)  Note : After breakdown current changes (from to ) but voltage remain the same (hence Zener diodes can be use to clamp voltages (or u can say they can be used as voltage regulators)    From VI characteristics of Zener diode, we can see that the voltage after break down is not constant (so to avoid that and make it const we add series resistor to it which is called as Zener resistor |
| How to check weather Zener diode will work as a regulator or not?? | Consider this ckt –  = Source voltage  = Series resistance  = Load resistance (across which we need const voltage)  **Step 1 : consider Thevenin theory (nothing is present between this 2 points)**    Using volt divider logic  🡨 this should be greater than breakdown volt of zener ( )  This means over no zener connection -- appears at divisor point between and  **Step 2 : consider zener connected now**    Point A  Point B  Now as we know zener allows max - breakdown voltage to appear across it (that’s why we use it as volt regulator) (so or ) Will appear across point A and B – and same across (as they are In parallel)    Thus, current across load = = =  Thus, source current / main current = =  Thus, current in zener diode branch = (using Kirchoff’s current law (KCL))  Thus, power dissipation across zener = =  **Example :**    Here,  zener max allowed current = 50 mA  **Calculations :**  (which is greater than breakdown volt of zener …so no worries -this zener will work like regulator)  = = 0.01A = 10mA  = = 0.032A = 32mA  Thus ,  Thus ,  Here things to note :  (max zener current)  (breakdown volt of zener)  Makes it work as regulator (if any violation would be there , this wouldn’t have worked as volt regulator)  **CASE 1 : CALCULATING MAX AND MIN such that zener works as regulator (and being known and fixed)**    Now considering and as const and as variable (so we can identify max and min resistor for zener to work as volt  regulator)  :   * Find * Identify (max zener current) from data sheet * Calculate * Calculate   **CASE 2 : CALCULATING MAX AND MIN such that zener works as regulator (and being known and fixed)**      :   * Find * Find ( = max current allowed through zener)   **CASE 3 : CALCULATING MAX AND MIN such that zener works as regulator (and being known and fixed)**     * Find * Find ( = max current allowed through zener)   NOTE : this all calculations are ideal (we have not considered (series resistance of zener) and also have consider (min zener  Current) = 0 (which Have some non-zero value) |
| Schottky diode | Schottky diode has forward volt of 0.3 to 0.5v (other PN junction diode has forward voltage of 0.6-0.7)  VI characteristics comparison of Schottky diode and PN junction diode    **Normal pn junction diode doesn’t work as expected as higher freq**  Ex.   1. At lower freq (normal PN junction diode)      1. At high freq (normal PN junction diode)     Because **reverse recovery time** of normal PN junction diode is large (that means it will also conduct in reverse bias for some time)  **Schottky diode at high freq**    Because **reverse recovery time** of Schottky diode is very small. Hence, they are fast responsive and can be used in high freq applications    Reverse breakdown is also lower compared to PN junction diode  Reverse leakage current of Schottky diode is higher compare to PN junction diode  **Limitation of schottky diode:**   * Reverse leakage current of Schottky diode is higher compare to PN junction diode * Reverse breakdown is also lower compared to PN junction diode * Operating temp range of schottky diode is also less   **Construction**     * Metal – semiconductor junction is formed * Both n type material and metal have electrons as their carrier * The major energy is carried by n type material electrons ( thus schottky diode is also called as hot carrier diode) * It is a unipolar device as only electrons constituent/causes the flow (no minority carriers )   **Reverser recovery time**    Here we can see when the polarity of voltage changes or u can say the diode become reverse biased – ideally it should stop conducting current right away – however as shown in image it keeps on conducting (in reverse bias) till seconds and then current decreases in time to become 0  = storage time = time required by carriers on minority side to go to majority side  = transition time    Due to this reverse recovery time the current does not become 0 instantaneously  **This affects PN junction diode only as they contain minority charge carriers (however schottky diode does not contain it/may contain in very few amount - so it does not have any reverse recovery time or negligible reverse recovery time)** |
| LED | Light emitting diode (releases photons (of different wavelength – thus different colours)    Wavelength of various types of signal |
| Photodiode | A photodiode is a semiconductor device that absorbs light energy to generate electric current.  It is also sometimes referred to as **photo-detector , photo-sensor** or **light-detector**  Photo diodes are specially design to operate in reverse bias condition    In photodiode when light falls on it 🡪 along with the **reverse saturation current (in the range of uA) [Dark current]** + **photo current** is also generated  **VI characteristics of photodiode**    Here P1, P2 , P3 and P4 are light intensity (so as the light intensity increases the photo current also increases leading to increase in total current(photo current + dark current)  The wavelength of incident light should be in range 400 to 1100nm  Responsivity ( R ) = ( = photo current(A) , P = Incident light power(watt)    Silicon , GaAs(gallium arsenide) works in visible region (their responsivity various over wavelength from 400nm to 1100nm)  InGaAs , Germanium works In the Infrared region  PIN photo diodes : Ptype – Intrinsic – N type (has bigger depletion region and when light strikes-more electron moves – so more photo current)    3db frequency is the freq where signal power becomes half  Rise time mainly depends on the RC characteristics of photo diode – R = equivalent Resistance of photo diode and load resistance --- C = equivalent capacitance of photodiode  Large area photodiodes are slower compared to small area photodiodes |
| Varactor Diode (Varicap Diode) | **Purpose:**  Used as a **voltage-controlled capacitor** in RF/microwave circuits, especially for **tuning**.  **Construction & Working:**   * Built like a normal **PN junction diode** but **always operated in reverse bias**. * In reverse bias, the **depletion region acts like a dielectric** → diode behaves like a **capacitor**. * **As reverse voltage increases → depletion width increases → capacitance decreases**.   **Key Point:**   * It’s not used to conduct current — it's used for its **capacitance**, which changes with voltage.   **Applications:**   * **Tuneable RF circuits** (e.g. radios, TVs) * **Voltage-controlled oscillators** (VCOs) * Phase-locked loops (PLLs)  1. Tuneable RF circuits   In tuning we use LC circuit (tuneable freq is achieved by setting it as resonance freq) (ex. radios- we switch to 93.5 FM)  In a traditional LC circuit:   * Frequency f = * Here to tune it at various freq we need changing capacitance (thus we use varactor diode – which acts as a capacitor – by controlling reverse voltage – in order controlling its reverse depletion region – and thus capacitance) * If you **change the capacitance C**, the frequency changes.   👉 So instead of using a **physical variable capacitor** (which is bulky), we use a **varactor diode**:   * Apply different **reverse voltages** → diode's **capacitance changes** → resonance frequency shifts.   **Example: Radio Tuning**   * Old radios used **mechanical tuning knobs** to adjust actual capacitors. * Modern RF circuits use **varactor diodes**:   + A **control voltage** varies the diode's capacitance.   + This shifts the tuned frequency of the LC tank → you “tune” the radio to your desired station electronically.  1. Voltage controlled Oscillator (VCO)   **What it does:**  A VCO is a circuit that **generates an oscillating signal (waveform)** — and the **frequency of that signal depends on an input voltage**.  **Role of Varactor:**   * The VCO often uses an **LC tank circuit**. * The **C part is a varactor diode**. * As you apply different **control voltages**, the varactor's capacitance changes → so the **oscillation frequency changes**.   📌 **Think of it as a frequency generator where voltage = tuning knob.**   1. Phase locked loop(PLL)   **What it does:**  A PLL is a control system that:   * **Generates**, **tracks**, and **locks** a signal’s phase and frequency. * It keeps an output signal **in sync with a reference signal**.   **Main Blocks of PLL**  [Reference Clock] ─► [Phase Detector] ─► [Low Pass Filter] ─► [VCO with Varactor] ─► [Output]  ▲ │  └──────────────[Divider (optional)]◄─────────┘  **✅ What Each Block Does:**   1. **Reference Clock** – A fixed, stable frequency input (e.g., crystal oscillator) 2. **Phase Detector** – Compares the **phase** (and freq) of reference vs. VCO output → Generates a **voltage** representing the phase error 3. **Low-Pass Filter** – Smooths out this error signal → Resulting in a **clean DC control voltage** 4. **VCO (Voltage-Controlled Oscillator)** – Here’s where the **Varactor Diode** is used!   **🌟 How Varactor is Used in PLL:**   * In the **VCO**, we have an **LC tank** (oscillating at some frequency). * Replace the **capacitor** with a **Varactor Diode**. * The **control voltage from the low-pass filter** is applied **across the varactor**. * This voltage changes the **capacitance** → changing the **oscillation frequency** of the LC tank. * So now, the VCO’s frequency **automatically adjusts** to **reduce the phase difference** with the reference signal.   👉 The **PLL “locks”** when VCO frequency = Reference frequency and both are in phase.   You can **synthesize different frequencies** from a single reference.   PLLs **filter out jitter** and **clean up signals**.   They’re **adaptive** — can auto-correct small drifts in output frequency.  **📌 Real-World Applications of PLL (with Varactor inside VCO):**   * **Clock generation** in CPUs (e.g., 2 GHz clock from 50 MHz reference) * **FM demodulators** * **Wireless communication** (syncing transmitter and receiver) * **Synthesizers in radios**   **🔧 Clock Generation in Microcontrollers (Using PLL)**  **🪨 Step 1: Crystal Oscillator as Reference**   * A microcontroller typically has a **crystal oscillator** (like 8 MHz or 16 MHz). * Crystals are **highly stable** but not very high frequency.   👉 This crystal becomes the **reference clock** for everything else.  **🔁 Step 2: Feed to PLL**   * The **crystal signal** is fed into a **PLL (Phase-Locked Loop)**. * The PLL’s **VCO** (which contains a **Varactor Diode**) can now generate much **higher frequencies** — say, 48 MHz or 72 MHz — by **multiplying** the base frequency.   **⚙️ Step 3: Use Dividers/Mux for System & Peripheral Clocks**   * The high-frequency clock from the PLL is:   + **Divided down** for subsystems like UART, SPI, ADC   + **Given to CPU core** for executing instructions   + Sent to **timers**, **memory buses**, and **communication blocks**   **📲 Example (like STM32 microcontrollers):**   | **Clock Source** | **Purpose** | | --- | --- | | Crystal Oscillator (e.g., 8 MHz) | Stable reference clock | | PLL (VCO + Varactor) | Generates higher clock (e.g., 72 MHz) | | Clock Divider/Mux | Selects & adjusts clocks for peripherals | |
| Tunnel Diode | **🔍 What Is It?**  A **Tunnel Diode** is a **highly doped PN junction diode** that exhibits **negative resistance** in a part of its operation. It uses a quantum phenomenon called **tunnelling** — that’s where the name comes from!  A Tunnel Diode is a highly doped PN junction diode that allows quantum tunnelling. It exhibits a unique **negative resistance region** in its V-I curve, where increasing voltage causes decreasing current. This property enables it to be used in **high-speed oscillators, amplifiers, and microwave circuits**. It’s much faster than standard diodes but more complex to use in modern digital designs.  [negative resistance : as per ohm’s law V I --- but when they are inversely proportional (that is called negative resistance)]  **⚙️ How It’s Built:**   * **P and N regions are extremely heavily doped** (about 1000 times more than a normal diode). * This makes the **depletion layer extremely thin** — in nanometres. * Because of this, electrons can **quantum tunnel** through the barrier even at very low forward voltages.   📌 *Tunnelling:* Electrons pass through the energy barrier **without climbing over it** — like magic, but real and based on quantum mechanics!      **V- I graph**    Here at Vp and Ip = voltage peak and current Peak  Here at Vv and Iv = valley voltage and valley current  Here after peak point the current starts decreasing until Valley voltage(Vv) (that is called negative resistance region  Advantages   * + High speed operation   + Low cost   + Low noise   + Low power dissipation   **🎯 Why is This Useful?**  **✅ Negative Resistance = High-Speed Switching**  This weird region allows:   * **Oscillators** at microwave frequencies * **Ultra-fast switching** circuits * Amplifiers with special feedback designs   Tunnel diodes can respond in **picoseconds** — way faster than regular diodes.  **🧠 Applications:**   | **Application** | **Why Tunnel Diode Is Used** | | --- | --- | | **Microwave Oscillators** | Stable high-frequency oscillation | | **High-speed logic** (historical) | Used before BJTs and FETs matured | | **Low-power amplifiers** | Useful in radio & satellite equipment | | **Memory cells** (some designs) | Used for bistable operation | | **Quantum computing** (research phase) | For tunnelling-based logic concepts | |
| Application 1 of diodes : Half wave rectifier | Conversion from AC to DC is called as rectification. Who can do this are called rectifiers  Rectifiers   * 1. Half wave rectifier   2. Full wave rectifier   Here we will learn half wave rectifier  AC signal is converted into pulsating DC      Circuit      (note : here we have considered diode ideal – in reality (due to reverse recovery time in reverse bias – it conducts and waveform would not be like this ++ also diode has some forward voltage as well )    So as shown here peak voltage will be Vm-0.7(for PN junction diode) and will also start conducting after forward drop of 0.7v  **Halfwave rectifier with filter**      here = RC should be much higher than T(time period of waveform) (thus before its discharging to 36.8% (takes period ) of its full charging – the next signal arrives and its starts charging again  here t1 = charging period and t2 = discharging period  Efficiency of rectifier = 40.6%  **half wave rectifier parameters** |
| Application 2 of diodes : Full wave rectifier | Full wave rectifier circuits are made using two methods   * 1. Centre tapped transformers   2. Diode-bridge circuit  1. Centre tapped transformer     **Working in the positive half of sine wave**    **Working in the negative half of sine wave**    **Total op waveform for full sine wave**    Notes :   * Here u can see for negative half and positive half of waveform is generating waveform on positive side only (here the output waveform repeats its pattern every T/2 sec (sine waveform repeats its waveform every T sec) * Thus, op freq becomes 2x that of input freq * Also, avg. voltage can be given by =       Actual op Waveform   1. Diode bridge circuit rectifier     **Working in the positive half of sine wave**    **Working in the negative half of sine wave**    **Total op waveform for full sine wave**    Notes :   * Here u can see for negative a positive half of waveform generating waveform on positive side only (here the output waveform repeats its pattern every T/2 sec (sine waveform repeats its waveform every T sec) * Thus, op freq becomes 2x that of input freq * Also, avg. voltage can be given by =     here = RC should be much higher than T(time period of waveform) (thus before its discharging to 36.8% of its full charging – the next signal arrives and its starts charging again  here t1 = charging period and t2 = discharging period  Efficiency of rectifier = 81.2% |
| Clipper circuit | **These circuits are used in 🡪 overvoltage protection 🡪 waveform shaping**  Simplest form of **clipper circuit** is **halfwave rectifier**  Based on **which part is being clipped** they are classified into two parts   * + - Positive clipper ckt     - Negative clipper ckt   Based on the position of the diode it is classified into further two parts   * Series clipper ckt * Parallel clipper ckt      * **PARALLEL CLIPPER CKT / SHUNT CLIPPER CKT (without Bias)**  |  |  | | --- | --- | | Positive clipper ckt    Here   * + in positive half – diode is forward biased and acts as a short ckt letting the signal pass – Vout = 0 (ideally) otherwise 0.7v drop appears   + in negative half – diode is reverse biased and acts as open ckt letting full voltage appear at vout = Vin | Negative clipper ckt    Here   * + in positive half – diode is reverse biased and acts as an open ckt letting full vin appear at Vout = Vin   + in negative half – diode is forward biased and acts as short ckt letting signal pass and no voltage appears at Vout = 0 (ideally) (otherwise 0.7v drop occurs) |  * **PARALLEL CLIPPER CKT (with Bias)**  |  |  | | --- | --- | | Positive clipper with positive Vr    Note :   * Here opposition of diode to Vin is till 0.7v – i.e. – till 0.7(Vf) volt diode acts as open ckt (doesn’t allow current to pass) and after 0.7( (it allows full current to pass) * Here opposition of DC battery is till Vr volt – i.e. – till Vr volt battery acts as open ckt (doesn’t allow current to pass) and after Vr volt( (it allows full current to pass) * **So, the total opposition is of (0.7 + Vr) volt** * **For positive half of the waveform**   + When Vin < (0.7 + Vr) = the branch acts as full opposition = open ckt full Vin appears at Vout **[Vout = Vin]**   + When Vin > = (0.7 + Vr) = the branch acts as 0 opposition = short ckt – shunting the signal to gnd (nothing appears at Vout) **[Vout = 0]** * **For negative half of the waveform**   + When Vin becomes negative (i.e. its polarity changes = diode becomes reverse biased for entire signal = open ckt = full volt appears at output **[Vout = Vin]** | Positive clipper with negative Vr    Note:   * Assuming Vr = 2v * Here opposition = 0.7 + (-2) = -1.3v * Vin >= (-1.3v) will be shunted * Vin < (-1.3) will appear at op   Ex. let’s say Vin = 3v AC (XYZ Hz)   * So Vm = 3v and -Vm = -3v * So, -3 , -2.4 , -1.8 , -1.4 which is all < (-1.3v) thus it will allow it to pass (will appear at Vout) * And -1.3,-1.1, -0.8 , 0 , 0.5,0.9,1.3 which is all >= (-1.3) -which will get shunted (so won’t be appearing Vout) (only -1.3v will appear at op )   In a nutshell   * Vin >= -1.3v -- Vout = -1.3 * Vin < -1.3 – Vout = Vin | | Negative clipper with positive Vr    Ex. let’s say Vin = 3v AC (XYZ Hz) and Vr = 2v   * Opposition = -0.7 + 2v = 1.3v * Now when signal is positive (diode is reverse biased) – hence is open ckt – full signal appears (but after 1.3v) * Now when signal is negative (diode is forward bias output gets shunted to gnd) – nothing appears as op   In a nutshell   * If Vin >= 1.3v -- Vout = Vin * If Vin < 1.3v -- Vout = 1.3v | negative clipper with negative Vr    Ex. let’s say Vin = 3v AC (XYZ Hz) and Vr = 2v   * Opposition = -0.7 + -2v = -2.7v * Now when signal is positive (diode is reverse biased) – hence is open ckt – full signal appears (but above -2.7v) * Now when signal is negative (diode is forward bias output gets shunted to gnd) – nothing appears as op   In a nutshell   * If Vin >= -2.7v -- Vout = Vin * If Vin < -2.7v -- Vout = -2.7v | | Parallel positive and negative clipper ckt with bias | |  * **SERIES CLIPPER CIRCUIT**  |  |  | | --- | --- | | Series Positive clipper ckt     * + For positive half : diode is reverse biased hence acts as an open ckt – nothing appears at Vout   + For negative half : diode is forward biased hence acts as short ckt – Vin appears at Vout | Series negative clipper ckt     * + For positive half : diode is forward biased hence acts as a short ckt – Vin appears at Vout   + For negative half : diode is reverse biased hence acts as an open ckt – nothing appears at Vout |  * **SERIES CLIPPER CIRCUIT (with Bias)**  |  |  | | --- | --- | | Series Positive clipper ckt with positive Vr    **During the positive half cycle :**  terminal A is positive and terminal B is negative. That means the positive terminal is connected to n-side and the negative terminal is connected to p-side. As we already know that if the positive terminal is connected to n-side and the negative terminal is connected to p-side then the [diode](https://www.physics-and-radio-electronics.com/electronic-devices-and-circuits/rectifier/clippercircuit-seriesclippersandshuntclippers.html) is said to be reverse biased. Therefore, the diode is reverse biased by the input supply voltage Vi.  However, we are supplying the voltage from another source called [battery](http://www.physics-and-radio-electronics.com/blog/battery-battery-works/). As shown in the figure, the positive terminal of the battery is connected to p-side and the negative terminal of the battery is connected to n-side of the diode. Therefore, the diode is forward biased by the battery voltage VB.  That means the diode is reverse biased by the input supply voltage (Vi) and forward biased by the battery voltage (VB).  Initially, the input supply voltage Vi is less than the battery voltage VB (Vi < VB). So the battery voltage dominates the input supply voltage. Hence, the diode is forward biased by the battery voltage and allows electric current through it. As a result, the signal appears at the output.  When the input supply voltage Vi becomes greater than the battery voltage VB, the diode D is reverse biased. So no current flows through the diode. As a result, input signal does not appear at the output.  Thus, the clipping (removal of a signal) takes place during the positive half cycle only when the input supply voltage becomes greater than the battery voltage.  **During negative half cycle:**  During the negative half cycle, terminal A is negative and terminal B is positive. That means the diode D is forward biased due to the input supply voltage. Furthermore, the battery is also connected in such a way that the positive terminal is connected to p-side and the negative terminal is connected to n-side. So the diode is forward biased by both battery voltage VB and input supply voltage Vi.  That means, during the negative half cycle, it doesn’t matter whether the input supply voltage is greater or less than the battery voltage, the diode always remains forward biased. So the complete negative half cycle appears at the output.  Thus, the series positive clipper with positive bias removes a small portion of positive half cycles. | Series Positive clipper ckt with negative Vr    **During positive half cycle:**  During the positive half cycle, the diode D is reverse biased by both input supply voltage Vi and battery voltage VB. So no signal appears at the output during the positive half cycle. Therefore, the complete positive half cycle is removed.  **During negative half cycle:**  During the negative half cycle, the diode is forward biased by the input supply voltage Vi and reverse biased by the battery voltage VB. However, initially, the battery voltage VB dominates the input supply voltage Vi. So the diode remains to be reverse biased until the Vi becomes greater than VB. When the input supply voltage Vi becomes greater than the battery voltage VB, the diode is forward biased by the input supply voltage Vi. So the signal appears at the output. | | Series Negative clipper ckt with positive Vr    **During positive half cycle:**  During the positive half cycle, terminal A is positive and terminal B is negative. That means the positive terminal A is connected to p-side and the negative terminal B is connected to n-side. As we already know that if the positive terminal is connected to p-side and the negative terminal is connected to n-side then the diode is said to be forward biased. However, we are also supplying the voltage from another source called battery. As shown in the figure, the positive terminal of the battery is connected to n-side and the negative terminal of the battery is connected to p-side of the diode.  That means the diode is forward biased by input supply voltage Vi and reverse biased by battery voltage VB. Initially, the battery voltage is greater than the input supply voltage. Hence, the diode is reverse biased and does not allow electric current. Therefore, no signal appears at the output.  When the input supply voltage Vi becomes greater than the battery voltage VB, the diode is forward biased and allows electric current. As a result, the signal appears at the output.  **During negative half cycle:**  During the negative half cycle, the diode D is reverse biased by the input supply voltage Vi and forward biased by the battery voltage VB. Initially, the input supply voltage Viis less than the battery voltage VB. So the [diode](https://www.physics-and-radio-electronics.com/electronic-devices-and-circuits/rectifier/clippercircuit-seriesclippersandshuntclippers.html) is forward biased by the battery voltage VB. As a result, the signal appears at the output.  When the input supply voltage Vi becomes greater than the battery voltage VB, the diode will become reverse biased. As a result, no signal appears at the output. | Series Negative clipper ckt with negative Vr    **During positive half cycle:**  During the positive half cycle, the diode D is forward biased by both input supply voltage Vi and the battery voltage VB. So it doesn’t matter whether the input supply voltage is greater or less than battery voltage VB, the diode always remains forward biased. Therefore, during the positive half cycle, the signal appears at the output.  **During negative half cycle:**  During the negative half cycle, the diode D is reverse biased by the input supply voltage Vi and forward biased by the battery voltage VB. Initially, the input supply voltage Viis less than the battery voltage VB. So the [diode](https://www.physics-and-radio-electronics.com/electronic-devices-and-circuits/rectifier/clippercircuit-seriesclippersandshuntclippers.html) is forward biased by the battery voltage VB. As a result, the signal appears at the output.  When the input supply voltage Vi becomes greater than the battery voltage VB, the diode will become reverse biased. As a result, no signal appears at the output. |   **Zener Clipper ckt**    For positive half of waveform :   * D2 is forward bias (providing 0.7v opposition) * D1 is reverse biased (till V1 volt it doesn’t conduct – hence it acts as open ckt – allowing Vin to appear at Vout) * When Vin > V1 – D1 starts to conduct in breakdown region and v1 appears across Vout (any voltage > Vzener 🡪 it allows only zener volt to pass (remember it acts as voltage regulator)   For negative half of waveform :   * D1 is forward bias – allows conduction after 0.7v * D2 is reverse biased (till V2 volt it doesn’t conduct – hence it acts as open ckt – allowing Vin to appear at Vout) * When Vin > V2 – D2 starts to conduct in breakdown region and v2 appears across Vout (any voltage > Vzener 🡪 it allows only zener volt to pass (remember it acts as voltage regulator) |
| Clamper Circuit | 1. Positive Clamper circuit (shift the waveform to positive side)      1. Negative clamper circuit (shifts the waveform to negative side)      |  | | --- | | **Positive clamper circuit**      **Process of how it gets shifted**   * (assuming we have just started powering the device – this is the first sine wave) In the positive half of the cycle – diode is reverse biased (acts as a open ckt) and entire positive cycle appears – at op (as marked yellow on waveform)      * Then in the negative half (from volt 0 to -Vm) -polarity reverses – diode becomes forward biased (acts as a short circuit)- capacitor has no path to spend its power on – so it charges (output at Vout = 0)     Point AS  Point BS   * The voltage that appears at point A – B is Vin + Vm * During the second half of negative half : Now (Vin + Vm) makes the diode reverse bias (even if the sine wave is increasing(actually decreasing in value ex. -3,-2,-1,0) in the negative part (thus forcefully making diode work in reverse bias (as a open ckt)      * Thus, now when Vout = Vin + Vm (however when Vin = -Vm ::: Vout = -Vm + Vm = 0 ) and then as the waveform (ie. Vin increasing from -Vm to 0 (Vout goes from 0 to Vm)      * Now during the next positive half cycle (the diode will be reverse biased as Voltage across diode will be Vin + Vm)      * During the second negative half cycle (the diode will still remain reverse biased – so we will get this type of waveform)      * So, in the steady state condition output will look like this     Example – tested | | **Negative clamper circuit**    Every function same as above (understand positive first – negative functions the same way)      However here we going to learn it by using a **rectangular wave as input**   * During the positive half of the cycle diode will be forward biased – and will act as a short circuit – thus in this cycle capacitor will get charged till Vm volt (so the output Vout = 0 – as shown by yellow line on waveform) | |
|  |  |
|  | * In the negative half of the cycle : diode will get reverse biased due to Vin being -Vm and cap voltage is also Vm – thus appearing voltage at diode will be -Vm + -Vm = -2Vm      * During the next positive cycle : the cap will have less value compared to Vin – due to expenditure on RL – so now due to Vin = Vm – the diode will be forward biased and will act as short circuit     **The steady state waveform**     |  |  | | --- | --- | | **Negative Clamper ckt with +ve bias**     * **During Positive half cycle** : Diode is forward biased (acts as a short circuit)      * The capacitor starts charging via the shown path (the voltage across cap can be given as Vc = Vm – V (using KVL) * Vout = V * **During the negative half cycle :** diode is reverse biased (acts as an open ckt) (Vout = -2vm + V)        * **Steady state output**     **(without biasing voltage – output would be varying between 0v to -2Vm volt) – due to positive V bias (output has been shifted from V to -2Vm + V volt))**  **(basically -ve clamper shift the entire signal to negative (0 to (-XYZ)) - and bias shifts it positive or negative depending on the bias type  let suppose we have a signal of -10 to 10v (sine wave) if we provide it to**   * + **Negative clamper with positive bias of 3 v (the negative clamper would shift it to 0 to -20 and positive bias would make it positive , thus making signal from 3 to -17v**   + **Negative clamper with negative bias of -3v (the negative clamper would shift it to 0 to -20 and -3 bias would further shift it -3 to -23v** | **Positive clamper with +ve bias :**  **Ex. 10 to -10 v signal after positive clamper be 0 to 20 and with bias of +3v it would become 3 to 23**  **Positive clamper with -ve bias :**  **Ex. 10 to -10v signal after positive clamper be 0 to 20 and with bias of -3v it would become -3 to 17v** | |
| Reverse polarity Protection | **💡 Purpose:**  Protects your circuit if **power supply terminals are accidentally reversed** (e.g., battery connected backward).  **✅ Simple Diode-Based Protection:**   * Place a **diode in series** with the positive supply line:   + If polarity is correct → diode conducts   + If reversed → diode blocks = ✅ circuit safe   + ⚠️ Downside: **Voltage drop (0.7V)** and power loss   **✅ Better Method: Diode across power input (shunt + fuse)**   * Place **diode in reverse bias across V+ and GND**, and add a fuse in series * If polarity reverses → diode conducts heavily (short) → **fuse blows**, disconnecting circuit * ⚠️ Diode must handle surge current until fuse blows |
| Logic level shifting | **💡 Purpose:**  Interfacing between components with **different logic voltages** (e.g., 5V → 3.3V microcontroller)  **✅ Diode Clamp Method:**   * Use a **Zener diode** (e.g., 3.3V Zener) between signal line and GND * When input exceeds 3.3V:   + Zener conducts, **clamps voltage at 3.3V**   + Prevents damage to low-voltage device   💬 You can also combine with a **series resistor** to limit current going into the Zener |
| Freewheeling diode in Inductive load | **💡 Purpose:**  **Used with inductive loads (relays, motors, solenoids) to suppress voltage spikes when switching OFF**  **✅ Why needed?**   * **When current through an inductor is suddenly interrupted, the collapsing magnetic field causes a high voltage spike (V = –Ldi/dt)** * **This can damage switching transistors or ICs**   **✅ Solution:**   * **Connect a diode across the inductor in reverse bias (called a flyback diode or freewheeling diode)** * **When switch opens, diode provides a path for inductor current to circulate safely** * **Protects the circuit** |
| Diodes in CMOS Processes (Parasitic & Body Diodes) | **✅ What is a Parasitic Diode?**  In **CMOS technology**, every **MOSFET** (both NMOS and PMOS) is fabricated in **semiconductor layers**, and this structure **automatically forms unintended diodes** between junctions.  These are called **parasitic diodes**, and they are always present — you can’t remove them.  **✅ Body Diode (Key Example)**  Let’s take an **NMOS** transistor:  Drain (n+)  |  ---  | | <- Parasitic diode (Drain to Body)  ---  |  Substrate (p-type)  |  GND  The **n+ Drain and p-type substrate** form a **PN junction diode** — this is the **body diode**, and it's **reverse biased** during normal operation.  **For PMOS:**   * The **p+ source/drain** sits in **n-well** → again forms **body diode** with the n-well * The n-well is usually tied to **VDD**   **💡 What happens if the body diode conducts?**   * If **drain goes below GND (NMOS)** or above VDD (PMOS), the **parasitic diode conducts** * That can cause:   + **Leakage**   + **Latch-up**   + **Unintended current paths**   **🛑 Why It’s Important in VLSI:**   1. **ESD Sensitivity** – these diodes are **used in ESD clamps**, but can also be **triggered unintentionally** 2. **Signal Integrity Issues** – if a signal goes below GND or above VDD, it can **forward-bias** these diodes 3. **Latch-up Risk** – parasitic structures like **PNPN** (thyristors) can trigger a **latch-up event**, where current flows uncontrollably   **🧠 Real-World Tip:**  In layout:   * **Tie the body/bulk appropriately**:   + NMOS body → GND   + PMOS body → VDD * Prevent **voltage swings** on pins that might forward-bias parasitics |
| **ESD Protection Diodes in ICs** | **✅ What is ESD?**  **ESD (Electrostatic Discharge)** is a **sudden high-voltage surge** caused by static electricity — like when you touch a chip after rubbing your socks on carpet.   * Can be **a few thousand volts**! * Happens in **nanoseconds** * Can **instantly destroy ICs** — especially modern low-voltage CMOS devices   **🔥 Why ESD is Dangerous in CMOS:**   * CMOS gates are made from **ultra-thin oxides** → they break down easily * Even **>100V spike** can punch through gate oxide * You’ll never even see it happen — but the IC dies   **✅ How ICs Defend: ESD Protection Diodes**  **Inside most modern ICs:**  Every **input/output (I/O) pin** has **two clamping diodes**:  VDD  |  ↑  [Diode]  ↑  Input Pin —────┼────—> To Internal Logic  ↓  [Diode]  ↓  GND  **🛡️ How it works:**   * If voltage on pin goes **above VDD** → **upper diode conducts** → current goes to **VDD rail** * If voltage on pin goes **below GND** → **lower diode conducts** → current goes to **GND rail**   💥 So the diodes **clamp the voltage to within VDD and GND ± 0.7V** (typical forward drop)  **✅ Other ESD Protection Structures:**  In real VLSI, you may also see:   | **Structure** | **Purpose** | | --- | --- | | **Diode clamps** | Simple and fast | | **Snapback devices** | Used for large current clamping | | **Thyristor-based clamps (TSCRs)** | Stronger protection for power pins | | **Resistors + diodes** | Current limiting before ESD diodes |   **📘 Where you'll see this in practice:**   * MCU datasheets often say:   “All I/O pins are protected against ESD to ±6kV (IEC 61000-4-2)”   * That's because of these **internal ESD diodes** |
| **Guard Rings & Substrate Isolation** | **✅ Why do we need them?**  In CMOS chips, **many transistors share the same silicon substrate**.   * This means **parasitic paths** (like unwanted diodes or BJTs) can form between transistors * These hidden paths can lead to:   + **Leakage**   + **Noise coupling**   + Even **latch-up** — a dangerous short between VDD and GND!   That’s where **guard rings** and **isolation** come in.  **🔹 1. What is a Guard Ring?**  A **guard ring** is:  A ring of doped silicon (like P+ or N+) connected to a **fixed potential (GND or VDD)** that surrounds sensitive devices.  **🔸 Purpose of Guard Ring:**   | **✅ Function** | **Explanation** | | --- | --- | | **Absorbs leakage current** | Prevents stray carriers (holes/electrons) from reaching other transistors | | **Breaks latch-up paths** | Shunts current from parasitic BJTs or diodes | | **Noise shielding** | Prevents analog noise or switching noise from crossing into other blocks |   **📘 Example:**  Imagine a **PMOS transistor** inside an **N-well**, and there's a lot of switching NMOS around.   * You add a **P+ guard ring connected to GND** around NMOS blocks * You add an **N+ guard ring connected to VDD** around PMOS blocks   These rings:   * **Sink minority carriers** * **Trap injected noise** * **Prevent latch-up**   **🔹 2. What is Substrate Isolation?**  This is the **technique of keeping transistor regions electrically separated**, so that:   * One transistor’s body doesn’t interfere with another * Especially critical in **analog ICs**, **mixed-signal**, or **high-voltage domains**   **Types:**   | **Type** | **Description** | | --- | --- | | **P-substrate isolation** | NMOS transistors are in shared P-substrate | | **N-well isolation** | PMOS transistors are in isolated N-wells | | **Triple-well / Deep N-well** | Fully isolate analog or high-voltage blocks | | **SOI (Silicon on Insulator)** | Advanced tech – transistors on oxide layer – no latch-up! |   **🧠 Fun Fact:**  Latch-up is caused by:  A **parasitic PNPN structure (like an SCR)** forming between adjacent NMOS and PMOS — it becomes a short circuit!  Guard rings and isolation **break that loop.** |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |