|  |  |
| --- | --- |
| Formula | Explanation |
| C = | C = capacitance  Q = charge  V = voltage |
| Energy stored in capacitor | E = |
| C = | A = Area of the plates  Ɛ = permittivity of dielectric ( Ɛ = \* )   * = Absolute permittivity * = relative permittivity (or dielectric constant of the material)   d = distance between the plates / thickness of the plates |
| Leakage current (as a spec in capacitor) or insulation resistance (also sometimes called as parallel resistance) | In some specs of capacitor where leakage current in µA to mA range it is labelled as leakage current and in some capacitor, where is low it is labelled as insulation resistance (results in Giga-mega range) |
| ESR (equivalent series resistance )  ESL (equivalent series Inductance) | Whenever we mention use of capacitor (we consider its nominal value -however in actual scenario it contains some series resistance and series inductance and some parallel insulation resistance)  ESR = it’s a small **resistance present *inside* the capacitor** due to its leads, plates, and electrolyte  ESL = **ESL** stands for **Equivalent Series Inductance**, and it represents the **tiny inductance** present **inside** a real-world capacitor.    Capacitor behaviour is freq dependent  At low frequency – (0 Hz = DC) and freq < f resonant 🡪 capacitor’s capacitance is only responsible as impedance  At f= fresonant – ESR dominates (capacitor impedance = ESR (capacitance and parasitic inductance cancels out each other)  And at high freq (f>fresonant) – ESL dominates (capacitor impedance = ESR + ESL)    In nutshell: (Capacitor behaviour is frequency-dependent )   * At **low frequencies** (including DC = 0 Hz): The **capacitive reactance dominates (Xc)** — the capacitor behaves like a capacitor. * At the **resonant frequency**: The effects of capacitance and ESL **cancel each other**: (so we’re left with ESR only) (The total impedance is **at its minimum**, equal to **just ESR)** * At **frequencies above resonance**: **ESL dominates** — the capacitor starts acting like an **inductor**.   Capacitor behaviour = frequency driven ✅ Low freq → Capacitance dominates 🡪 capacitor actually behaves like capacitor ✅ f = Resonant freq → ESR dominates (minimum impedance) ✅ High freq → ESL dominates → cap behaves inductive  Sometimes manufacturers mention **dissipation factor** instead of ESR   |  | | --- | | **Real Word capacitor Application Example** | | **1. Power Supply Filtering (Decoupling Capacitors)**  **Used in:** Microcontrollers, CPUs, FPGAs, VLSI cores  **🔧 The Problem:**   * Digital ICs switch ON/OFF **millions of times per second**. * This causes **fast current spikes** on the power line → creates **voltage noise/ripple**.   **⚡ What You Need:**   * A capacitor that **quickly supplies or absorbs charge** during those spikes. * **Low ESR** → so it doesn’t waste energy or drop voltage * **Low ESL** → so it can respond to **very fast changes (MHz–GHz)**   **💡 Real-World Fix:**   * Place a **ceramic SMD capacitor (e.g., 0.1µF)** **very close to IC pin** * It has **very low ESR + ESL** → perfect for **high-frequency decoupling** | | **🛠️ 2. Analog Filters (RC Filters)**  **Used in:** Audio circuits, sensor signal processing, anti-aliasing  **🔧 The Problem:**   * You want to **pass low-frequency signals** and **block noise** * You design an **RC low-pass filter**   **⚡ Why ESR/ESL matter:**   * If ESR is too high → the filter is **less sharp** * If ESL is high → the filter **fails at higher frequencies**, or lets **spikes through**   **💡 Example:**  A bad-quality capacitor in an audio filter might allow **high-pitched noise** or **hum** to pass through. | | **📡 3. RF Circuits / High-Speed Communication**  **Used in:** WiFi, Bluetooth, RF amplifiers, Ethernet  **🔧 The Problem:**   * Signals in these circuits are in the **MHz to GHz range** * Any capacitor with **ESL** acts like an **antenna or inductor**   **⚡ Why ESL is dangerous:**   * At high freq, ESL causes the cap to **stop acting like a cap** * It **reflects signals** or **distorts waveform**   **💡 Fix:**   * Use **special low-inductance ceramic caps** * Keep capacitor **physically very close** to the signal line * Use **multiple caps (0.1µF, 0.01µF, etc.)** in parallel → better across frequency range | | 🔋 4. Bulk Power Storage / Battery Backup  Used in: Routers, clocks, EEPROM hold-up  🔧 The Problem:   * You need to store charge for longer durations (slow discharge)   ⚡ Why Rp (leakage) matters:   * If Rp is low, the capacitor leaks slowly and drains faster * Your backup time becomes shorter   💡 Solution:   * Use capacitors with high Rp (low leakage) * Tantalum or electrolytic caps are common here | | 💣 5. Switching Regulators (SMPS)  Used in: Laptop chargers, phone chargers, motor drives  ⚡ Problem:   * These circuits switch power at high speed (50kHz to 1MHz) * Capacitor must filter output cleanly, else it causes ripple, heat, noise   🔧 Why ESR matters:   * If ESR is high, ripple increases and components heat up * You may even get oscillation in the circuit   💡 Solution:   * Use Low ESR electrolytic capacitors or polymer caps * ESR is often mentioned clearly in datasheets for SMPS designs | |
| Dissipation factor ( DF) | The DF of a capacitor is the measure of the energy lost as heat during its operation (it should be as low as possible)  DF =  🡪 = [ f = frequency in Hz , c = capacitance in farad ] |
| Volumetric Efficiency (VE) | It tells you **how much capacitance** (in µF) a capacitor can provide **per unit volume** (in cm³ or mm³).    🧠 Why It Matters:  In modern electronics:   * Space is precious (think smartphones, wearables, VLSI chips) * So, designers want maximum capacitance in minimum space * Hence, high volumetric efficiency = better design choice!   🔎 Example:  Let’s say you have:   * A ceramic capacitor: 1 µF in a 1 mm³ package → VE = 1 µF/mm³ * An electrolytic capacitor: 10 µF but takes 20 mm³ → VE = 0.5 µF/mm³   Even though electrolytic has more capacitance, ceramic is more efficient per volume. |
| Capacitors in parallel and in series | (in parallel) – capacitor in parallel increases capacitance (think of it as capacitor plate size increases and dielectric thickness is same)  (in series) – capacitor in series decreases capacitance below the lowest capacitance in series (think of it as capacitor in series increases the dielectric material)  [the below given example is for dc ]  Note :     * + Parallel capacitor stores same charge   + Ex. C1 = 10uf , C2 = 220uf , C3 = 100uf ctot = 330uf = 0.00033F   + Total charge (Q) = tot capacitance \* volt = 0.00033 \* 9v = 0.00297 coulombs   + Charge across capacitors Q1 + Q2 + Q3 = Q (here charge is diff for diff capacitors)   + Capacitor in series stores charge differently   + Ex. C1 = 10uf , C2 = 220uf ctot = 1 / (1/c1 + 1/c2) = 9.56uf (less than the lowest capacitor(c1))   + Ex. C1 = 10uf , C2 = 220uf , C3 = 100uF ctot = 1 / (1/c1 + 1/c2 + 1/c3) = 8.73uf (less than the lowest capacitor(c1))   + Total charge (Q) = tot capacitance \* volt = 0.0000873 \* 9v = 0.0000785 coulombs   + Charge across capacitor c1 = Q , c2 =Q and c3 =Q (as the current is same in series so does the charge across capacitor      * + Hence max voltage v1 in capacitor c1 🡪 Q/C = 0.0000785/0.00001 = 7.857 v   + Hence max voltage v2 in capacitor c2 🡪 Q/C = 0.0000785/0.00022 = 0.357 v   + Hence max voltage v3 in capacitor c3 🡪 Q/C = 0.0000785/0.0001 = 0.786 v   + Here v1 + v2 + v3 = V = 9v = total volt of battery |
| Capacitor charging time | Here 5 sections = 5 time constant (τ) is needed to achieve 99.3% of the volt applied  Time constant (τ) = resistance (ohm) \* capacity(farad) = 10000 \* 0.0001 = 1  Hence time taken for this capacitor to charge upto 99.3% is 5\* 1 sec = 5 sec  So  After 1st time constant 🡪 voltage reaches 63.2%  After 2nd time constant 🡪 voltage reaches 86.5%  After 3rd time constant 🡪 voltage reaches 95.0%  After 4th time constant 🡪 voltage reaches 98.2%  After 5th time constant 🡪 voltage reaches 99.3%  Note : as the voltage in capacitor increases the current decreases (as the capacitor blocks DC after being fully charges. So while charging it reduces the current flow by accumulating the charge) |
| Capacitor dis-charging time |  |
| Capacitor , inductor and resistor behaviour with AC | * DC current/voltage is constant * AC current/voltage is sinusoidal (alternating with time) * Thus in DC there being no phase difference between current and voltage (think of it as there is no physical lag – ex voltage changes suddenly-current will change suddenly and vice versa) * In AC –   + Resistor – does not do anything with current or voltage that makes them lag or lead each other   + **Capacitor opposes changes in voltage** — when voltage tries to change suddenly, the capacitor charges/discharges to **smooth it out**, causing **voltage to lag behind current**. Hence, **current leads voltage by 90°**, which means a **−90° phase angle**.   + **Inductor opposes changes in current** — when current tries to change suddenly, the inductor develops a voltage that **resists** that change. As a result, **current lags voltage by 90°**, giving a **+90° phase angle**. |
| Capacitor power in AC circuits | * In DC voltage and current has no phase angle between them * In AC voltage and current are sinusoidal * Power here in terms of AC has two components (Active power (that is been consumed or used) + reactive power (that is been consumed but released also (so net power is 0)) (ex. capacitor saves energy in form of charge and then releases it when needed –thus net power is 0) * S = P(active power) + Q(reactive power) = S=P+jQ (jQ is imaginary 🡪 as it gets consumed and released so net power is 0)   **Real (Active) Power, P**   * Power that actually does useful work * Converts into heat, light, motion, etc. * Unit: **Watt (W)** * Formula:   P = VI cos Ø  **Reactive Power, Q**   * Power that is stored and returned to the source * No actual energy is consumed permanently * Unit: **VAR (Volt-Amp Reactive)** * Formula:   Q = VI sin Ø   * For **resistor** S = P + Q = VI cos(0) + VI sin(0) = VI (1) + VI (0) = VI [only real part exists for resistor] * For **Capacitor** S = P + Q = VI cos(-90) + VI sin(-90) = VI (0) + VI (-1) = -VI [only imag part exists for capacitor as it consumes and releases power so net power is 0] * For **inductor** S = P + Q = VI cos(90) + VI sin(90) = VI (0) + VI (1) = VI [only imag part exists for inductor as it consumes and releases power so net power is 0]   So, for capacitor S = P + Q = VI cos(-90) + VI sin(-90) = VI (0) + VI (-1) = -VI |
| Lag / Lead in phase | Note : lag and lead only exist in AC as due to existence of components like capacitor and inductor (bottom line -- due to their reactances)   * In capacitor current leads voltage by 90 degrees (-90degree phase shift) * In inductor voltage leads current by 90 degrees (+90degree phase shift)   But what is exactly lag and lead  For a sine wave:   * One full cycle = 360° * 90° = 1/4 cycle   So, if you're at 50 Hz:   * One cycle time period T = = = 0.002 sec = 20 ms * 90° lag 🡪 20 ms = 5 ms delay caused by reactances * Voltage hits its peak **5 milliseconds** after current does (in a capacitor at 50 Hz -due to component). * Voltage hits its peak **5 milliseconds** before current does (in an Inductor at 50 Hz -due to component). |
| Reactance | **Reactance** is the **opposition** a component offers to **AC current**, due to its ability to **store and release energy**.  **Think of it like:**   * Resistance opposes current **in general** (DC or AC) * Reactance opposes current **only when current is changing** (i.e., in AC)   Reactance is similar to resistance, but:   * **It doesn't consume energy** (no power loss) * **It stores and releases energy** (in electric or magnetic field) * It is measured in **ohms (Ω)** — same unit as resistance!   Capacitor resonant freq  **There are Two Types of Reactance:**  **1. Capacitive Reactance (Xc)**   * Opposes **low-frequency AC signals** more * Formula:   + f = frequency in Hz   + C = capacitance in farads * At **low frequency** → is high (blocks AC) * At **high frequency** → ​ is low (allows AC)   **2. Inductive Reactance ()**   * Opposes **high-frequency AC signals** more * Formula:   + f = frequency in Hz   + L = inductance in henrys * At **low frequency** → is low (allows AC) * At **high frequency** → ​ is high (blocks AC)   **⚙️ Total Opposition in AC = Impedance**  Reactance combines with resistance to form **impedance**:  Z = R + j X   * Z = impedance (total opposition to AC) * X=​− * j = imaginary unit (shows phase shift) |
| Resonant Frequency | The **resonant frequency** is the frequency at which a circuit containing a **capacitor (C)** and an **inductor (L)** naturally oscillates.  At this frequency: ​=  As a result:   * Their **reactances cancel each other out** * The **total reactance becomes zero** * The circuit behaves like it has **only resistance** * The **impedance is minimum** (in series) or **maximum** (in parallel)   For a standard **LC circuit** (without resistance):   * = **resonant frequency** (Hz) * = inductance (henry, H) * = capacitance (farad, F)   **▶ In a Series LC Circuit:**   * ​= ​ → net reactance = 0 * Impedance is **minimum** * Acts like a **short circuit** for AC at that frequency * Allows **maximum current** to flow * Used in **tuned amplifiers, bandpass filters, antenna matching**   **▶ In a Parallel LC Circuit:**   * ​= ​ → they create a very high impedance * Total current drawn from the source is **minimum** * Circuit acts like an **open circuit** to AC at that frequency * Used in **oscillators, band-stop filters, tank circuits** |
| Series LC and parallel LC | For AC, remember:   * **Capacitive Reactance:** * Decreases with frequency * **Inductive Reactance:** * Increases with frequency   **Resonance Condition**  At resonance: ​= => net reactance=​- ​=0  **1️⃣ Series LC Circuit at Resonance**  **Circuit:**  AC Source → L → C → back to source  **What happens:**   * L and C are **in series** * At resonance: ​= => net reactance=​- ​=0 * So total **reactance = 0**, and if resistor is negligible, * Z = R + j (​- ) = 0   **Minimum impedance!** → Circuit behaves like a **short circuit** → AC current **flows freely** → Voltage across L and C may be large, but overall source sees **low opposition**  **Used in:**   * Band-pass filters * Tuned amplifiers * Signal selection   2️⃣ **Parallel LC Circuit at Resonance**  **Circuit:** |----- L -----|  AC Source | | back to source  |----- C ---- |  **What happens:**   * Each branch **has current**, but:   + Inductor current **lags**   + Capacitor current **leads** * At resonance: ​= => equal and opposite * So, **currents in L and C cancel each other out** * → This means **almost no net current** is drawn from the source → From the source's point of view: **circuit looks open** → Hence, **impedance is very high**   **Used in:**   * Oscillators (tank circuits) * Band-stop filters * Frequency-selective circuits   **Summary Table**   | **Type** | **Resonance Behaviour** | **Impedance at Resonance** | **Current Drawn** | | --- | --- | --- | --- | | **Series LC** | Reactances cancel | **Minimum (Z → 0)** | **Maximum** | | **Parallel LC** | Currents cancel | **Maximum (Z → ∞)** | **Minimum** | |
| Low pass filter | Low pass filter   * Active lpf : made using active components such as transistor or op-amp * Passive lpf : made using passive components (inductor , capacitor , resistor)   3 types of passive LPF  🡪 RC Low pass filter  🡪 RL low pass filter  🡪 RLC low pass filter   |  |  | | --- | --- | | **RC low pass filter** | **RL low pass filter** | | Herereactance **: =**   * At low freq = (acts as open ckt)(so we get vin at vout) * At high freq = (acts as short ckt) (shunts the signal to gnd) | Herereactance **: =**   * At low freq ( 🡪 0 ) (acts as short ckt)(so we get vin at vout) * At high freq ( 🡪 ) (acts as open ckt) (so no current flows and no voltage occurs) |  |  |  |  | | --- | --- | --- | | Ideal Low pass filter response graph    Actual low pass filter response graph    At lower freq 🡪 it provides 0 attenuation  As the freq increases it gradually increases attenuation    After cutoff freq (output will attenuate at the rate of -20dB  Cut off freq formula for RC lpf 🡪 for RL lpf 🡪  Output waveform will lag from the input phase by  That is identified by below given equation   |  |  | | --- | --- | | **For RC low pass filter**  Cut off freq formula for RC lpf 🡪  =   * freq = 0 (DC) 🡪 (op waveform Insync with input) * freq = (cutoff freq) 🡪 (op waveform lags by 45 degrees from input waveform) * freq = 🡪 (op waveform lags by 90 degrees from input waveform)   Hence in short, the output waveform (for input of Vin and f freq 🡪 is and f freq with phase lag  e.g. in input = 10v 2khz ac signal 🡪 output will be  **,** freq is same and phase shift of ~51 **🡪 output waveform will have 6.22v of amplitude and freq will be same but will have phase lag of ~51** | **For RL low pass filter**  Cut off freq formula for RC lpf 🡪  =   * freq = 0 (DC) 🡪 (op waveform Insync with input) * freq = (cutoff freq) 🡪 (op waveform lags by 45 degrees from input waveform) * freq = 🡪 (op waveform lags by 90 degrees from input waveform) | | |
| High pass filter | High pass filter   * Active hpf : made using active components such as transistor or op-amp * Passive hpf : made using passive components (inductor , capacitor , resistor)   3 types of passive hpf  🡪 RC high pass filter  🡪 RL high pass filter  🡪 RLC high pass filter   |  |  | | --- | --- | | **RC high pass filter** | **RL high pass filter** | | Herereactance **: =**   * At low freq = (acts as open ckt)(so current doesn’t flow and no op appears) * At high freq = (acts as short ckt) (current flows , op appears across resistor) | Herereactance **: =**   * At low freq ( 🡪 0 ) (acts as short ckt)(so we get vin at vout) * At high freq ( 🡪 ) (acts as open ckt) (so no current flows and no voltage occurs) |  |  |  |  | | --- | --- | --- | | Ideal High pass filter response graph    Actual low pass filter response graph    At lower freq 🡪 it provides increasing attenuation  As the freq increases it gradually increases attenuation    Before cutoff freq output will attenuate at the rate 20db/decade  Cut off freq formula for RC hpf 🡪 for RL hpf 🡪  Output waveform will lag from the input phase by  That is identified by below given equation   |  |  | | --- | --- | | **For RC low pass filter**  Cut off freq formula for RC lpf 🡪  =   * freq = 0 (DC) 🡪 (op waveform leads by 90 degrees with input) * freq = (cutoff freq) 🡪 (op waveform leads by 45 degrees from input waveform) * freq = 🡪 (op waveform in sync with input waveform) | **For RL low pass filter**  Cut off freq formula for RC lpf 🡪  =   * freq = 0 (DC) 🡪 (op waveform Insync with input) * freq = (cutoff freq) 🡪 (op waveform leads by 45 degrees from input waveform) * freq = 🡪 (op waveform leads by 90 degrees from input waveform) | | |
| RC delay ckts  \*( One of capacitor application to delay voltage ) | It’s a circuit where **a resistor and capacitor** work together to **delay a voltage change** — typically when power is first applied or a switch is flipped.   * When a **step voltage** (like 0 → 5 V) is applied at **Vin**, the capacitor **charges slowly**, not instantly. * **Vout is taken across the capacitor**, so you get a **rising voltage** with a delay. * The voltage across the capacitor follows an **exponential charging curve**.  | **Time** | **Vout (approx.)** | | --- | --- | | 0 | 0 V | | 1τ = RC | 63% of 5 V = 3.15 V | | 2τ | 86% of 5 V | | 3τ | 95% of 5 V | | 5τ | ~100% of 5 V |   This gradual increase **creates a time delay** before Vout reaches a certain logic threshold.  **🛠️ Real-Life Example: Power-On Reset Delay**   * Some ICs or microcontrollers need time to stabilize after power is turned on. * You connect an RC delay at their **reset pin**. * Until Vout reaches a certain voltage, the IC stays in reset. * After the **delay**, Vout crosses threshold, and the IC starts running. |
| RC LPF as Integrator | It is basically LPF circuit (but in specific case it works are Integrator)   * When Time period of input signal (T = ) is less than =RC 🡪 i.e. When **T <<** or **T << RC**…LPF works as an Integrator   (time period of waveform should be very lower than the RC(or tau))  Square wave 🡪 triangular wave |
| RC differentiator ckt | It is basically **hpf**  circuit (but in specific case it works are differentiator)  When Time period of input signal (T = ) is greater than =RC 🡪 i.e. When T >> or T >> RC…HPF works as a differentiator  (waveform’s time period should be very higher than the RC(or tau))  (tau=RC is very less means 🡪 capacitor takes very less time to charge(charging time = 5\*) and discharge      Here in RC HPF – output is taken across resistor   * When a square wave is applied   - rising Edge 🡪 at sudden input volt appears at the output ..however after sometime capacitor starts charging…making vout fall from level to 0v level  - const voltage 🡪 output is blocked due to capacitor being fully charged… volt is 0 at output  - falling edge 🡪at falling edge , capacitor encounters sudden drop in volt -so it tries to keep volt as it is and drains making vout appear high and then lessened as capacitor drained ) (As a result, it **discharges rapidly**, producing a **negative spike** at the output (opposite polarity)) |
| Band Pass filter | Series LC parallel LC  LC circuit as band pass filter    Band pass filter working concept   * At low freq is lower ( effective impedance = capacitive impedance * At high freq is lower ( effective impedance = Inductive impedance * At certain freq (f resonance) - (so they cancel out each other – and effective impedance is very low)   Resonance freq :  **Series LC (as band-pass):**   * At resonant freq →  → Total impedance = **minimum (near zero)** → **Signal passes through** = ✅ **Band Pass behaviour**   **Parallel LC (as band-pass):**   * At resonant freq →  → Total **admittance (1/Z)** is max → **Impedance is maximum** = acts like an **open circuit** → **Used in parallel with a resistor** → maximum **voltage across the LC** → **Resonance appears at output across LC tank**   So, it **passes signal** only if you take the output across LC or across a load connected in parallel.   | **Type** | **Resonance Effect** | **Signal Behaviour** | | --- | --- | --- | | **Series LC** | Acts like a **short** (min impedance) | Signal **passes through** | | **Parallel LC** | Acts like an **open** (max impedance) | Signal appears **across LC** | |
| Parasitic capacitance | **Unwanted capacitance** due to layout, materials, and device physics:   * **Gate Capacitance (Cg)**: Between MOSFET gate & channel (controls switching delay). * **Interconnect Capacitance (Ci)**: Between adjacent wires (can cause **crosstalk** and **delays**).   Unwanted capacitance – Cg + Ci + Cf(fanout gate capacitance)  **Effect**: → Slows down signal transitions due to added **RC delay (Capacitance charging/discharging causes delay)**  → Makes layout-sensitive → more critical in advanced nodes. |
| RC delay (gate delay) | * Every MOS gate behaves like an RC circuit:   + R = Resistance of NMOS/PMOS channel   + C = Load capacitance (parasitic + fanout gates) * Gate Delay ∝ RC → time to charge/discharge output node * Important for timing closure, affects clock frequency |
| **Capacitors in ADCs, DACs & Sample-and-Hold Circuits** | * Sample-and-hold (used in ADCs): → Capacitor samples input voltage and holds it steady while conversion happens. * Used to:   + Maintain voltage level during conversion window.   + Reduce signal fluctuation and improve ADC accuracy. |
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