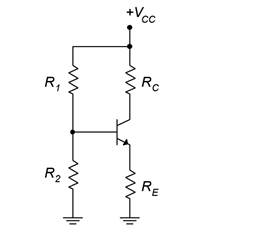
**DC analysis**

1. First step is to find DC biasing for Q point(point where it sits perfect in active region that no clipping or attenuation to signal occurs – not close to saturation or cutoff) perfectly in active region
2. Setup should be like this

* Base – Emitter junction forward bias (base being at greater volt than Emitter)
* Base – collector junction reverse bias (collector being at greater volt than base)

Example :



**E**

**C**

**B**

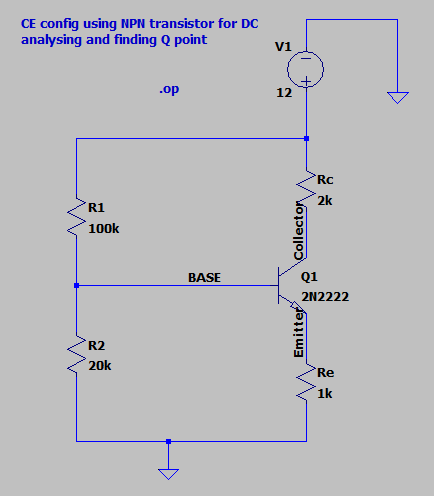
|  |  |
| --- | --- |
| (source volt) | 12v |
| R1 | 100k ohm |
| R2 | 20k |
| Rc | 2k |
| Re | 1k |
| BJT   * Vbe = 0.7v * Vce(saturation) = 0.2 * = (at config 🡪 = 1.0 mAdc, = 10 Vdc) = 50 | 2N2222 (NPN) |

Now let’s calculate various parameters:

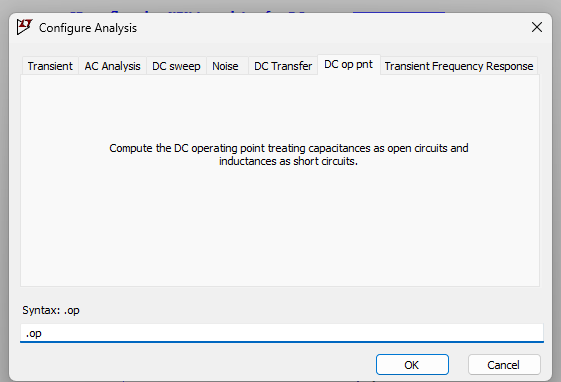
* Here volt divider has been used (to make this independent of Beta()(or ) )
* = = 12 \* 2v
* = - = 2 – 0.7 1.3
* = = 0.0093 1.3mA
* = 1.3mA
* = = 12v – 1.3mA\*2k = 12 – 2.6 = 9.4v
* = - = 8.1v
* Q point () = (1.3mA , 8.1v)
* Here = 50 (as per the datasheet)
* = = 0.026 mA = 26uA

1. Now let’s stimulate it in LTspice and check whether we receive same para values

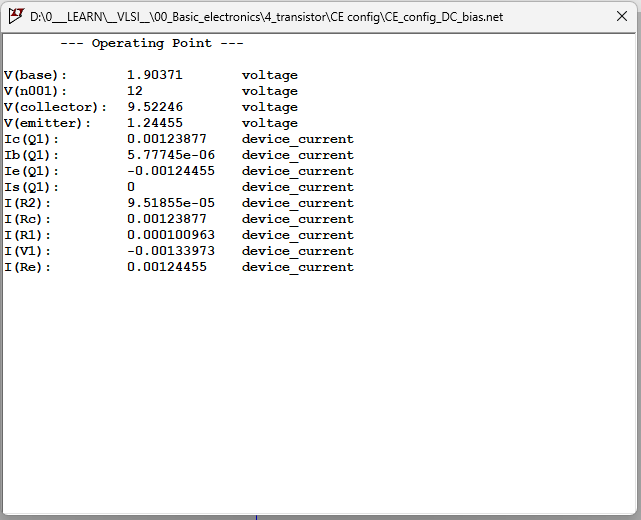
* Open LTspice
* Develop below mentioned ckt



* Set the config analysis (.op)



* Now run simulation (Alt + R) – you will see a window opening



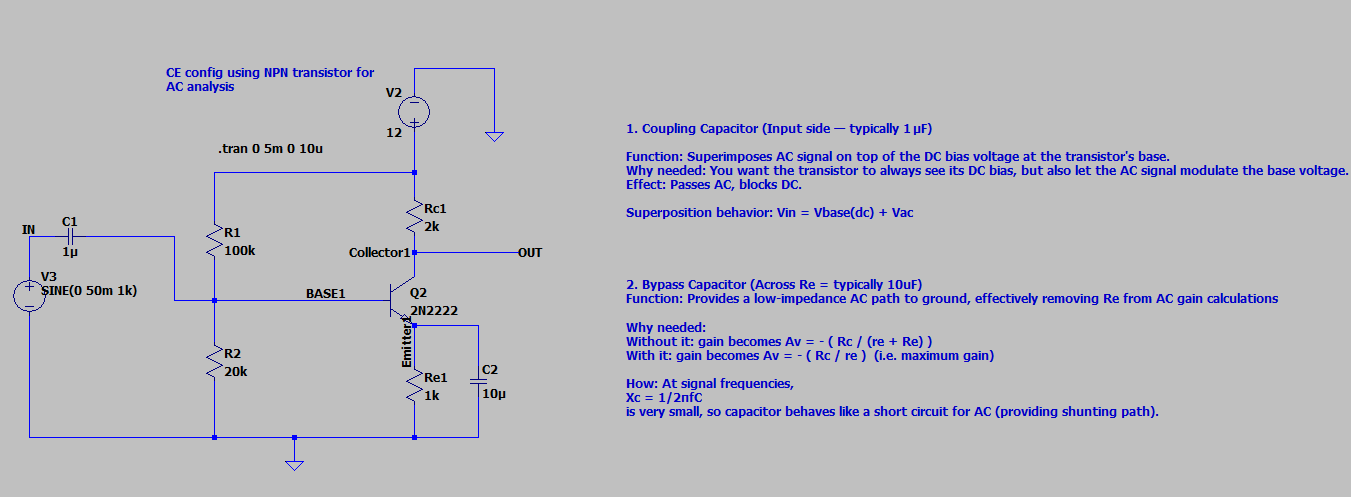
* Let’s compare it

|  |  |  |
| --- | --- | --- |
| **parameter** | **LT spice op** | **Manual calculation op** |
|  | 1.90371 | 2 |
|  | 12v | 12v |
|  | 9.522 | 9.4 |
|  | 1.244 | 1.3 |
|  | 0.00123 = 1.23mA | 1.3mA |
|  | 5.77uA | 26uA |
|  | 0.00124 = 1.24mA | 1.3mA |
| = - | 8.28 | 8.1 |

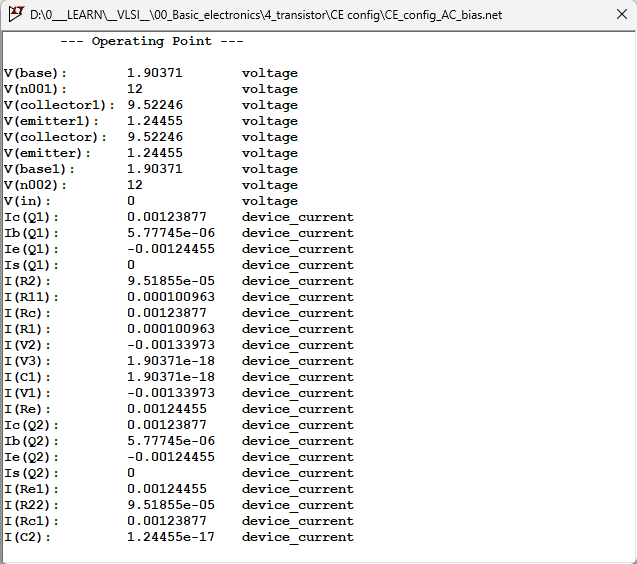
* Now Q point () = (1.23mA , 8.27v)

**AC analysis of CE config**

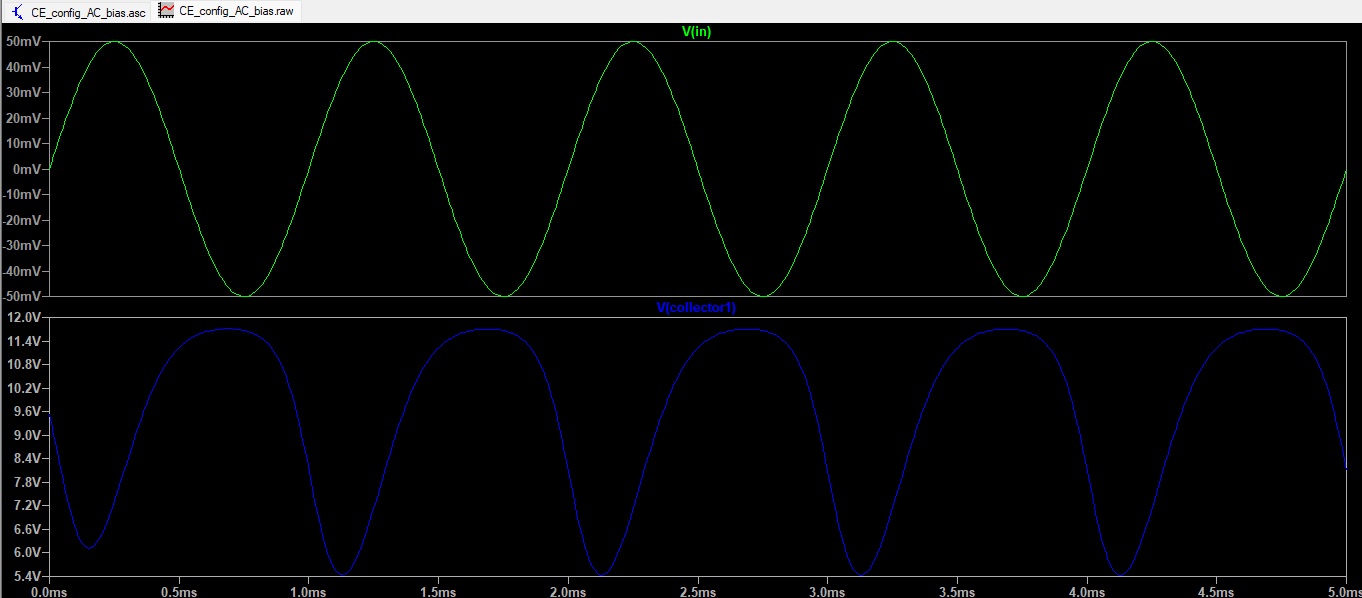
1. Now let’s see how it can amplify signals (a CE config provides high current gain and moderate volt gain)



1. Connect it like this (input signal = 50mV , 1KHz) (transient = 5ms , max time step = 10 us)
2. Here the DC operating point result (compare DC biasing data and data once we apply AC ) (both are same – that means Q point remained same)



1. Resultant waveform (showing amplification )



[Note : here you can see the input is swinging across 0mV (because our observation point on ckt is before capacitor – i.e. AC input signal is yet to be superimposed on DC bias – if you observe the waveform after capacitor, you can see it swinging across 2v as (the DC bias at base is 2v)]

Superimposed signal :

Example :

* DC bias = 2v
* AC signal = sine wave (50mV , 1KHz) , peak-to-peak = 100mV

2 + 0.050 \* sin (2\*1000\*t)

|  |  |
| --- | --- |
| **Time** | **Calculation** |
| t =0 ms (start of sine wave) | sin(2π⋅1000⋅0.0005)=sin(π)=0  V(0 ms)= 2 + 0 = 2v |
| t = 0.25ms (quarter of cycle) | sin(2π⋅1000⋅0.00025)=sin(π/2)=1  V(0.25ms)= 2 + 0.050 \* 1 = 2.050v |
| T = 0.5 ms (half cycle) | sin(2π⋅1000⋅0.0005)=sin(π)=0  V(0.5 ms)= 2 + 0 = 2v |
| T = 0.75ms (three- quarter of cycle) | sin(2π⋅1000⋅0.00075)=sin(3π/2)=−1  V(0.75 ms)= 2 + 0.050 \* -1 = 1.95 v |
| T = 1ms (full cycle) | sin(2π⋅1000⋅0.001)=sin(2π)=0  V(1ms)= 2 + 0 = 2v |

1. Here let’s analyse output

* Input signal = Vin = 50 to -50mV (peak-to-peak = 100mV)
* Output signal = Vout = 11.70 to 5.45 (peak-to-peak = 6.25V)
* **Analysis 1 : Inversion Check:**
  + When input is +ve (rising) 🡪 output falls
  + When input is -ve (falling) 🡪 output rises
  + This is signature of a common Emitter Amplifier
* **Analysis 2 : Voltage gain:**
  + Av = = = 62.5
  + Voltage gain = -62.5 (negative sign indicates phase shift of 180 degree)
* Your **transistor is correctly biased in active region**
* The **bypass capacitor is working**, because gain is high
* The **circuit is amplifying AC as expected**, with proper **input/output coupling**

1. Why this output swinged across midpoint = 8.5 and not someplace else??

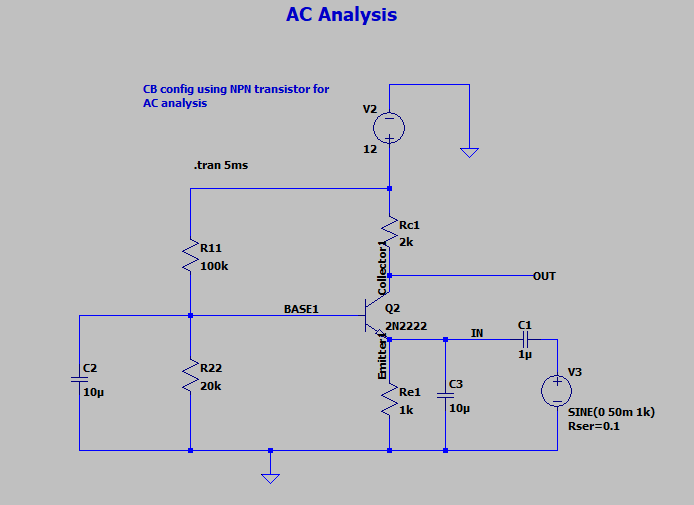
* Vin
  + Lowest point : -50mV
  + Mid-point : 0mv
  + Max point : 50mV
* Vout
  + Lowest point : 5.45 V
  + Mid-point : 8.5 V
  + Max point : 11.70 V
* Because the output swings around the DC Q point ( )
* In CE amplifier Vout = =( \* )
* You set the **DC bias** so that the transistor is in the **active region**
* The **DC operating point (Q-point)** is chosen roughly midway between Vcc and ground to allow **maximum symmetric swing**
* On top of this DC voltage, the **AC amplified signal is superimposed**
* In our case
  + Vce = 8.28 (as per the LTspice operating point)
  + Av = 62.5
  + Vin = 50mV
  + Vout = \* = 8.28 62.5 \* 0.05 = 8.28 3.125 [ 11.40v to 5.15v]

**AC analysis of CB config**

1. Now let’s see how it can amplify signals (a CB config provides high voltage gain and ~ 1 current gain)
2. Do below mentioned connection in LTspice (DC biasing condition remains the same)

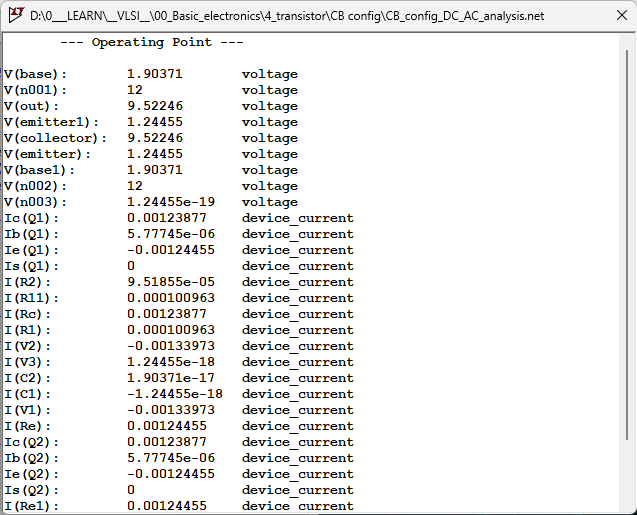
|  |  |  |
| --- | --- | --- |
| **parameter** | **LT spice op** | **Manual calculation op** |
|  | 1.90371 | 2 |
|  | 12v | 12v |
|  | 9.522 | 9.4 |
|  | 1.244 | 1.3 |
|  | 0.00123 = 1.23mA | 1.3mA |
|  | 5.77uA | 26uA |
|  | 0.00124 = 1.24mA | 1.3mA |
| = - | 7.6 | 7.4 |

* Now Q point () = (1.23mA , 7.6v)

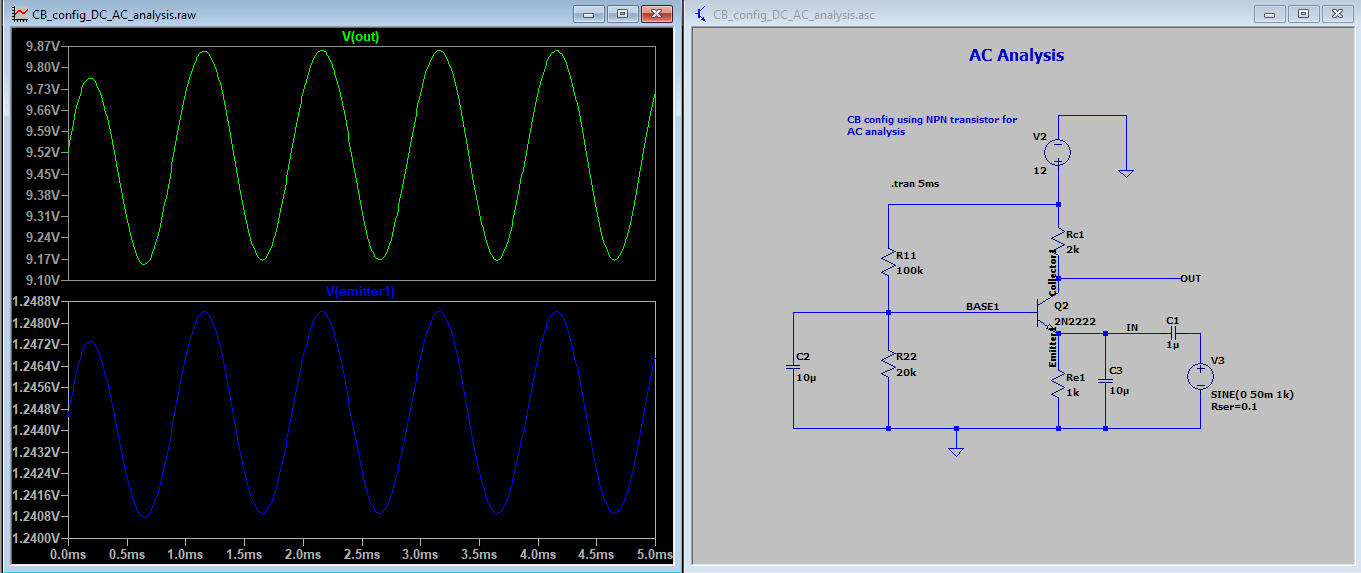


* Here
  + 1uf capacitor at input(at emitter) is for superimposing AC signal over DC signal (DC bias volt) (this is called coupling capacitor)
  + 10uf capacitor across Re is to bypass AC signal to gnd(shunt them) to increase the voltage gain (refer page 25 of 01\_transistor\_basics.docx file to know more)
  + 10uF across R22 is to bypass AC signal to gnd(shunt them) to increase the voltage gain (refer page 25 of 01\_transistor\_basics.docx file to know more)

1. Here the DC operating point result (compare DC biasing data and data once we apply AC ) (both are same – that means Q point remained same)



1. Here , resultant waveform



1. Lets analyse the output

* Input signal = Vin = 50 to -50mV (peak-to-peak = 100mV)
* Output signal = Vout = 9.8562 to 9.1673 (peak-to-peak = 0.688v)
* **Analysis 1 : Voltage gain:**
  + Av = = = 6.89
  + Voltage gain = 6.89
* Your **transistor is correctly biased in active region**
* The **bypass capacitor is working**, because gain is high
* The **circuit is amplifying AC as expected**, with proper **input/output coupling**

1. Why this output swinged across midpoint = 9.5 and not someplace else??

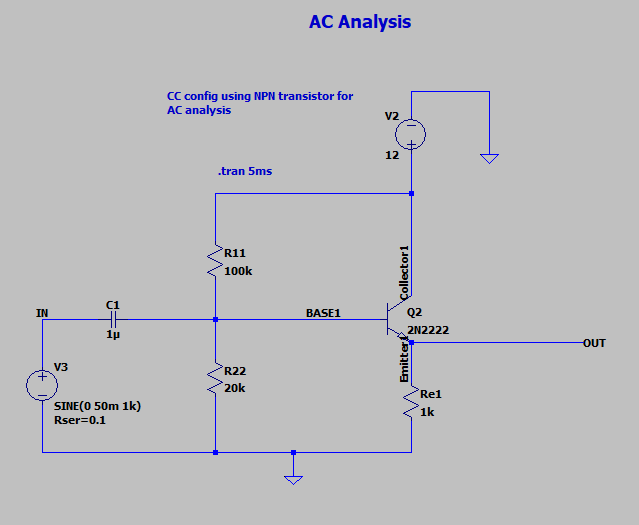
* Vin
  + Lowest point : -50mV
  + Mid-point : 0mv
  + Max point : 50mV
* Vout
  + Lowest point : 9.1673 V
  + Mid-point : 9.5 V
  + Max point : 9.8562 V
* Because we took output at collector and reference Is considered as Gnd (not base) (thus it is superimposed op across Vc = 9.522)
* But in actual it should be measured between C and B terminal (hence 9.5 – 2v = 7.5 v)
* the output swings around the DC Q point ( )
* In CB amplifier Vout = =( \* )
* You set the **DC bias** so that the transistor is in the **active region**
* The **DC operating point (Q-point)** is chosen roughly midway between Vcc and ground to allow **maximum symmetric swing**
* On top of this DC voltage, the **AC amplified signal is superimposed**
* In our case
  + Vcb = 7.6 (as per the LTspice operating point)
  + Av = 6.89
  + Vin = 50mV
  + Vout = \* = 7.6 6.89 \* 0.05 [ 7.1673v to 7.8562v]

**AC analysis of CC config**

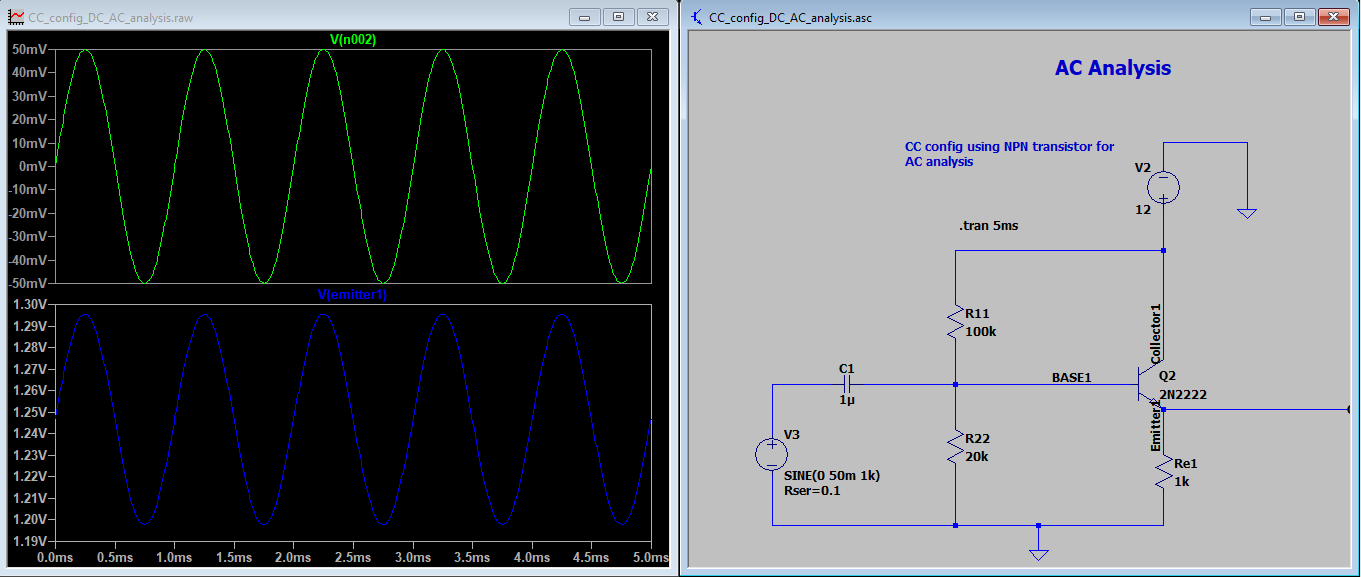
1. Do below mentioned connection in LTspice (DC biasing condition remains the same)

|  |  |  |
| --- | --- | --- |
| **parameter** | **LT spice op** | **Manual calculation op** |
|  | 1.90371 | 2 |
|  | 12v | 12v |
|  | 12v | 12v |
|  | 1.244 | 1.3 |
|  | 0.00123 = 1.23mA | 1.3mA |
|  | 5.77uA | 26uA |
|  | 0.00124 = 1.24mA | 1.3mA |
| = - | 10.756 | 10.7 |

* Now Q point () = (1.24mA , 10.756v)



* Here if we plot volt – it will almost be same (



* Here the output swing is of 98mV which is same as input (…showing that in CC config volt gain is 1
* Current gain ( = = 218) [ basically for 2N2222 current gain ranges from 100-300)
* The output swings between 1.1977 to 1.2954 ( 97 mV) (the swing is centred around 1.24655 (which is the emitter volt- DC bias) (on which AC output is superimposed)