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| **From where did u learn** | **What u learned + explanation** |
| General | |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | Active components | **Definition:** Active components are those that can control current and require an external power source to operate.   * **What they do:** * Amplify signals * Switch currents * Control flow of electricity in a circuit   **🔌 They need power to work.**   |  |  | | --- | --- | | **Component** | **What it does** | | Transistor | Amplifies or switches signals | | Diode | Allows current in one direction | | Op-Amp | Amplifies voltage difference | | IC | Performs complex logic, computation | | MOSFET | Controlled switching and regulation | | | Passive components | **Definition:** Passive components cannot amplify or generate energy. They respond to signals but don’t power the circuit themselves.  **What they do:**   * Resist, store, or filter energy * Cannot add energy to the circuit   **They do not need power to work.**   |  |  | | --- | --- | | **Component** | **What it does** | | Resistor | Limits or drops voltage/current | | Capacitor | Stores and releases energy as charge | | Inductor | Stores energy in a magnetic field | | Transformer | Transfers energy using magnetic coupling (still passive) | | |
| Resistor – video – pull up and pull down | |  |  | | --- | --- | |  | The current(I) any element/component draws when input (I) is a logic level high(H)(i.e. 1)  🡪 I = current  🡪 I = input , H = high | |  | The min voltage level at input from which element/component will start detecting it as logic level high   |  |  |  |  | | --- | --- | --- | --- | | Logic Family | Supply Volt ( ) | Logic Low ( | Logic High ( | | TTL (5v) | 5 | 0 – 0.8v | 2 – 5v | | CMOS (5v) | 5 | 0 – 1.5v | 3.5 – 5v | | CMOS (3.3v) | 3.3 | 0 – ~1v | ~2.3 – 3.3v | | CMOS (1.8v) | 1.8 | 0 – ~0.45v | ~1.35 – 1.8v | | |  | The current(I) any element/component draws when input (I) is a logic level low(L)(i.e. 0)  🡪 I = current  🡪 I = input , L = low | |  | It tells you how much current an output pin can safely sink (pull into itself) when it is outputting a logic LOW (0).   * When a digital output pin is at logic LOW (e.g., 0V), it may have to **absorb (sink) current** from other connected devices (like LEDs, inputs of other ICs, pull-up resistors, etc.). * defines the max safe limit of that sink current.   Ex.  Suppose a microcontroller or logic gate output is connected to an LED with a series resistor.   * When output = **LOW** (0V), current flows from Vcc → resistor → LED → **into the output pin** * This is **sink current** * If current = 5 mA, and **= 8 mA**, it's **safe** * If current > 8 mA, the IC may get damaged or not output a solid LOW | |  | It tells you how much current an output pin can source (push out) when it is outputting a logic HIGH (1).  When a digital output is **HIGH** (e.g., 5V or 3.3V), it might have to **deliver current to a connected load** — like:   * Another IC input * A pull-down resistor * Or even an LED (if you're sourcing current) * tells how much current the IC can safely push out without the voltage dropping or damaging the IC. | | Fan- out | Fan-out = The maximum number of input gates that a single output can drive reliably. (in short - It tells you how many **inputs** (like logic gates, IC pins) you can connect to **one output pin** without causing problems.)  Ex.  You have one output pin on a microcontroller (like an STM32, Arduino, or 8051), and you want to connect it to multiple other inputs — maybe to ICs, logic gates, or digital sensor pins.  How many such devices can you connect to that one pin? → **That's where fan-out comes in.**   * Microcontroller output HIGH drive - = 6mA * Input is CMOS gate and its Input high current - = 1µA   Fan-out = 6 mA / 1 µA = 6000 gates  (That means you could (in theory) connect that one pin to **up to 6000 CMOS inputs**!)  **⚠️ But in real-world design, you never go near the max — here's why:**   * **Wires/traces have capacitance**, which causes **delays and ringing** * More connected devices → **more capacitance** → **slower transitions** * At high speeds, **even a few gates** can load the output   So, **engineers limit fan-out** to 10–20 **for safety and signal quality**, even when current permits more. | | Fan-in | Fan-in = How many inputs a digital circuit (or pin) accepts.  Ex.   * A **2-input AND gate** have **fan-in = 2** * A **4-input NOR gate** have **fan-in = 4** * A **NOT gate (inverter)** has **fan-in = 1** * A **GPIO pin** (e.g., PA0 on STM32) configured as **input (fan-in = 1) – can read one input only** | |  | The **maximum voltage** that an output pin will show when it is supposed to be at **logic LOW (0)**, while also **sinking current** up to its limit.  If a microcontroller or logic IC is outputting a LOW (0), tells you:   * How "LOW" that LOW can actually be under load (not ideally 0V, but close to it)   **Example (TTL Logic like 74LS):**   |  |  | | --- | --- | | **Spec** | **Value** | |  | Max 0.4 V (at = 8 mA) | | |  | If an output pin is at **or above** it’s considered a **valid logic 1**. | |  | The **maximum voltage** that an Input pin will consider as logic low (ex. below – it considers as logic 0 – above – it considered as undefined |   RECAP   |  |  | | --- | --- | | **Symbol** | **Meaning** | |  | Max voltage considered input LOW | |  | Min voltage considered input HIGH | |  | Max output voltage for LOW | |  | Min output voltage for HIGH |  |  |  |  | | --- | --- | --- | | **Symbol** | **Meaning** | **Current direction** | |  | Input current at **logic LOW** (input pin) | Flows **into** the pin | |  | Input current at **logic HIGH** (input pin) | Flows **into** the pin | |  | Output **sink** current at **logic LOW** (output pin) | Flows **into** the pin | |  | Output **source** current at **logic HIGH** (output pin) | Flows **out of** the pin | |
| Impedance matching | **🧠 What is Impedance Matching?**  Impedance matching means ensuring that the **output impedance of one stage** is appropriately matched to the **input impedance of the next stage** to achieve **maximum power transfer** or **signal integrity** — depending on the context.  **📌 1. Low-to-Low or High-to-High**  **🔧 Use Case:** For **power transfer**, especially in high-frequency or transmission line systems (e.g., RF, transmission cables)   | **Goal:** | **Maximum Power Transfer (or prevent reflection)** | | --- | --- | | Example: | RF systems, antenna design, transmission lines, RS-485 long lines | | Matching Needed: | Output Impedance = Input Impedance | | Result: | Minimal reflection, clean waveform |   ✅ **Why?** To **maximize energy flow** and **minimize signal reflection** on high-frequency or long-distance lines  **📌 2. Low-to-High**  **🔧 Use Case:** For **signal systems**, like analog/digital sensors, op-amps, or logic circuits   | **Goal:** | **Signal Preservation (no loading)** | | --- | --- | | Example: | MCU GPIO → ADC, op-amp out → filter in, stage 1 → stage 2 in multi-stage filters | | Output Impedance: | **Low** | | Input Impedance: | **High** | | Result: | Voltage signal is preserved (no voltage drop), no loading effect |   ✅ **Why?** To ensure the signal is **read correctly**, **not dropped or distorted**, and that the **source is not overloaded**  **📌 3. High-to-Low**  ❌ Generally **not desired** — this causes:   * Signal **attenuation** * Voltage **drop** * Potential **distortion or current overdraw**   **💬 Final Crux:**   | **Type** | **Use When** | **Goal** | | --- | --- | --- | | **Low-to-Low / High-to-High** | Power, RF, long cables | Max power transfer, prevent reflection | | **Low-to-High** | Signal transmission | Preserve signal integrity | | **High-to-Low** | ❌ Avoid | Causes voltage drop, signal loss |   **⚡ Impedance Matching – Summary with Real-World Examples**  **🧠 What is Impedance Matching?**  Matching the **output impedance** of one circuit stage to the **input impedance** of the next stage — depending on whether your goal is:   * **Maximum power transfer** (in transmission lines, RF, etc.) * **Signal integrity** (in analog/digital systems)   **📌 1. Low Output Impedance → High Input Impedance**  ✅ **BEST for signal transfer** 🔧 **No matching required — desirable for voltage signals**   | **📍Use Case** | **Analog and digital signal interfacing** | | --- | --- | | ✅ Goal | Signal voltage is preserved | | ✅ Result | Minimal signal loading | | 🛠️ Example 1 | Microcontroller GPIO (low Zo) → ADC input (high Zin) | | 🛠️ Example 2 | Op-amp output → Filter input | | 🛠️ Example 3 | First filter stage → Second stage with high Zin |   **📌 2. Low-to-Low or High-to-High**  ✅ **Required for transmission lines or RF systems** 🔧 **Impedance matching done to prevent reflection / power loss**   | **📍Use Case** | **Long cable, RF, high-speed digital** | | --- | --- | | ✅ Goal | Maximum power transfer / prevent reflection | | ✅ Result | Signal integrity and minimal ringing | | 🛠️ Example 1 | RS-485 line: MAX485 driver (Zo ~ 120 Ω) → Termination resistor (120 Ω) at receiver | | 🛠️ Example 2 | RF circuit: 50 Ω source → 50 Ω coax cable → 50 Ω antenna | | 🛠️ Example 3 | High-speed SPI/MIPI lines in VLSI → matched trace + termination |   **📌 3. High Output Impedance → Low Input Impedance**  ❌ **Undesirable for signal transfer**   | **📍Use Case** | **Signal misdesign** | | --- | --- | | 🚫 Goal | Not preferred — causes loading | | ⚠️ Result | Voltage drop, signal distortion, high current draw | | ⚠️ Example | Sensor with high output impedance connected directly to a low-Z ADC or GPIO pin | | ⚠️ Example | Weak op-amp driving a heavy capacitive load without buffer |   ✅ Fix: Use a **buffer** (e.g., op-amp voltage follower or common collector stage) for impedance bridging  **🧭 Quick Crux Table:**   | **Case** | **Use For** | **Goal** | **Examples** | | --- | --- | --- | --- | | **Low → High** | Signal transfer | Preserve voltage | MCU → ADC, Op-amp → Filter | | **Matched** (Low↔Low or High↔High) | Transmission line | Prevent reflections | RS-485, RF, SPI | | **High → Low** | Avoid | Prevent signal loss | Sensor → ADC (without buffer) | |
| A signal reflection occurs / a path can be considered as transmission line (basically when it becomes as transmission line)-we need to match the impedance | **Example : SPI on ribbon cable**    **Note : signal velocity is velocity of signal in FR-4 pcb material**          **REAL WORLD EXAMPLE (PLC’s 4-20 mA requires impedance matching at somewhere)** |
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