

# Digital Logic



II

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# DESCRIPTION SHEET

## DIGITAL LOGIC

### Chapter-1 : Number Systems and Binary Codes

- Radix based number system : Standard number systems
- Conversion:
  - Decimal number to radix  $r$  number
  - Radix  $r_1$  number to radix  $r_2$  number
  - $(r-1)$ 's and  $r$ 's complement
- Signed binary numbers:
  - Signed magnitude notation
  - Signed 1's complement notation
  - Signed 2's complement notation
- BCD codes: Weighted and non-weighted codes, self complementary codes, reflective codes

### Chapter-2 : Boolean Algebra, Logic Gates and K-Maps

- Boolean Algebra:
  - Boolean operators – Basic and derived
  - Logic gates
  - Boolean algebra properties
  - Sum of product and Product of sum forms
  - Minterms and Maxterms
  - Variables and Literals
  - Universal logic gate
  - Properties of EX-OR and EX-NOR
  - Simplification of Boolean expression and functions using properties
- K-Map:
  - Definition of irredundant and minimal expression
  - Necessity of K-map
  - K-map on 2, 3 and 4 variables

- Definition of implicant, prime implicant and essential prime implicant
- Don't care combinations
- Minimal SOP and POS expressions using K-map
- Five variable K-map

### Chapter-3 : Combinational Logic Circuits

- Code Converters:
  - BCD to Excess-3
  - Excess-3 to BCD
  - Binary to Gray code
  - Gray to binary code
  - 5 - 4 - 2 - 1 BCD to natural BCD
- Arithmetic Circuits:
  - Half-adder, Full-adder, Half subtractor, Full subtractor
  - Binary adder
    - ⇒ Serial adder
    - ⇒ Ripple carry adder
    - ⇒ Carry look ahead adder
  - Binary subtractor:
    - ⇒ Advantages of 2's complement subtractor
    - ⇒ 4-bit binary adder/subtractor
- BCD to Excess-3/Excess-3 to BCD converter circuit using binary adder
- BCD adder and subtractor
- Binary comparator circuit
- Multiplexer:
  - MUX circuit with logic gates
  - Active low and Active high enable

- Applications of MUX's
- Analysis of MUX circuits
- Realising larger size MUX using smaller size MUX's
- Decoder/DE-MUX:
  - Decoder/De-mux circuits with logic gates
  - Active low and active high outputs
  - Application of Decoder/De-MUX
  - Analysis of Decoder circuits
  - Realising larger size decoder using smaller size decoders
- Encoder and priority Encoders
  - Applications of encoders

## **Chapter-4 : Sequential Circuits**

- Flip-Flops:
  - Binary latch
  - S-R and J-K flip-flop circuits with NAND gates
  - Truth table, characteristic equation and excitation table
  - Clear and Preset inputs
  - Race around condition and its solution
  - Master slave J-K flip-flop circuit using NAND gates
- D and T flip-flops
- General procedure for converting one flip-flop to another flip-flop
- Registers:
  - SISO, SIPO, PISO and PIPO and universal shift registers
  - Timing diagrams
  - Application of shift registers
- Asynchronous counter:
  - Difference between asynchronous and ripple counter
  - Implementation of ripple up counter and down counter
  - Designing of MOD-N ripple counter using clear and present terminals.
  - Timing diagrams
  - Analysis of ripple counters
- Synchronous counter:
  - Design:
    - ⇒ Straight sequence
    - ⇒ Random sequence
  - State diagrams
  - Timing diagrams
  - Analysis of synchronous counters



## 1

# Number Systems and Binary Codes



## Multiple Choice Questions

- Q.1** What are the values of  $R_1$  and  $R_2$  respectively, in the expression  $(235)_{R_1} = (565)_{10} = (1065)_{R_2}$ ?  
 (a) 8, 16      (b) 16, 8  
 (c) 6, 16      (d) 12, 8  
 [ESE-2004 (EE)]
- Q.2**  $(2)_3 + (3)_4 = (?)_5$   
 (a) 4      (b) 11  
 (c) None of these      (d) Not possible
- Q.3** Convert the octal number 127543 into the hexadecimal form.  
 (a) AF63      (b) AF53  
 (c) AFD3      (d) BCD3
- Q.4** If  $(11xy)_8 = (12C9)_{16}$  then the values x and y are  
 (a) 3 and 1      (b) 5 and 7  
 (c) 7 and 5      (d) 1 and 5  
 [ESE-2012]
- Q.5** If  $(2.3)_{\text{base } 4} + (1.2)_{\text{base } 4} = (y)_{\text{base } 4}$ ; what is the value of y?  
 (a) 10.1      (b) 10.01  
 (c) 10.2      (d) 1.02  
 [ESE-2005]
- Q.6** How many 1's are present in the binary representation of  
 $(4 \times 4096) + (9 \times 256) + (7 \times 16) + 5?$   
 (a) 8      (b) 9  
 (c) 10      (d) 11  
 [ESE-2004]

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- Q.7** The binary equivalent of hexadecimal number 4F2D.  
 (a) 0101 1111 0010 1100  
 (b) 0100 1111 0010 1100  
 (c) 0100 1110 0010 1101  
 (d) 0100 1111 0010 1101  
 [ESE-2002]
- Q.8** In signed magnitude representation, the binary equivalent of 22.5625 is (the bit before comma represents the sign)  
 (a) 0, 10110.1011      (b) 0, 10110.1001  
 (c) 1, 10101.1001      (d) 1, 10110.1001  
 [ESE-2002]
- Q.9** The 2's complement representation of -17 is  
 (a) 101110      (b) 101111  
 (c) 111110      (d) 110001  
 [GATE-2001]
- Q.10** The 2's complement representation  $(-539)_{10}$  in hexadecimal is  
 (a) ABE      (b) DBC  
 (c) DE5      (d) 9E7  
 [GATE-2001]
- Q.11** F's complement of  $(2BFD)_{\text{hex}}$  is  
 (a) E304      (b) D403  
 (c) D402      (d) C403  
 [ESE-2001]
- Q.12**  $(FE35)_{16} \text{XOR} (CB15)_{16}$  is equal to  
 (a)  $(3320)_{16}$       (b)  $(FF35)_{16}$   
 (c)  $(FF50)_{16}$       (d)  $(3520)_{16}$   
 [ESE-2000]
- Q.13** 11001, 1001 and 111001 correspond to the 2's complement representation of which one of the following sets of number?  
 (a) 25, 9 and 57 respectively  
 (b) -6, -6 and -6 respectively  
 (c) -7, -7 and -7 respectively  
 (d) -25, -9 and -57 respectively  
 [GATE-2004]

**Q.14** Which of the following represents ' $E3_{16}$ '?

- (a)  $(1CE)_{16} + (A2)_{16}$
- (b)  $(1BC)_{16} - (DE)_{16}$
- (c)  $(2BC)_{16} - (1DE)_{16}$
- (d)  $(200)_{16} - (11D)_{16}$

[ESE-2002]

**Q.15** Which of the following subtraction operations result in  $F_{16}$ ?

1.  $(BA)_{16} - (AB)_{16}$
2.  $(BC)_{16} - (CB)_{16}$
3.  $(CB)_{16} - (BC)_{16}$

Select the correct answer using the code given below:

- (a) Only 1 and 2
- (b) Only 1 and 3
- (c) Only 2 and 3
- (d) 1, 2 and 3

[ESE-2006]

**Q.16** Which of the following statement is incorrect for the range of  $n$  bits binary numbers

- (a) Range of unsigned numbers is 0 to  $(2^n - 1)$
- (b) Range of signed magnitude number is  $-(2^{n-1} - 1)$  to  $(2^{n-1} - 1)$
- (c) Range of signed 1's compliment numbers is  $-(2^{n-1} + 1)$  to  $(2^{n-1})$
- (d) Range of signed 2's compliment numbers is  $-(2^{n-1})$  to  $(2^{n-1} - 1)$

**Q.17** A number in 4-bit 2's complement representation is  $X_3 X_2 X_1 X_0$ . This number when stored using 8-bits will be

- (a) 0000  $X_3 X_2 X_1 X_0$
- (b) 1111  $X_3 X_2 X_1 X_0$
- (c)  $X_3 X_3 X_3 X_3 X_2 X_1 X_0$
- (d) 1  $X_3 X_3 X_3 X_3 X_2 X_1 X_0$

[GATE-1999]

**Q.18** Two 4-bit 2's complement numbers 1011 and 0110 are added. The result expressed in 4-bit 2's complement notation is

- (a) 0001
- (b) 0010
- (c) 1101
- (d) Cannot be expressed in 4-bit 2's complement

[GATE-IN:2003]

**Q.19** The BCD code for a decimal number  $(874)_{10}$  is

- (a)  $(100001110100)_{BCD}$
- (b)  $(010001111000)_{BCD}$
- (c)  $(100001000111)_{BCD}$
- (d)  $(011110000100)_{BCD}$

[ESE-2012]

**Q.20** What is the Gray code word for the binary 101011?

- (a) 101011
- (b) 110101
- (c) 011111
- (d) 111110

[ESE-2006]

**Q.21** Which one of the following is the correct sequence of the numbers represented in the series given below?

- (2)<sub>3</sub>, (10)<sub>4</sub>, (11)<sub>5</sub>, (14)<sub>6</sub>, (22)<sub>7</sub>,.....
- (a) 2, 3, 4, 5, 6,.....
- (b) 2, 4, 6, 8, 10,.....
- (c) 2, 4, 6, 10, 12,.....
- (d) 2, 4, 6, 10, 16,.....

[IES-2007]

**Q.22** Which of the following weighted code will give 9's complement by changing (complementing) each individual bit?

- (a) Excess-3
- (b) 5421
- (c) 2421
- (d) Both (a) and (c)

**Q.23**  $(212220221.1222212)_3 = (?)_9$

- (a) 25827.5872
- (b) 58827.5866
- (c) 58817.5876
- (d) 25827.5876

2

6

3

9

### Numerical Answer Type Questions

**Q.24** The decimal equivalent of binary number 10110.11 is \_\_\_\_\_.

**Q.25**  $(-64)_{10} + (80)_{16} = (?)_{10}$

[ESE-2007]

**Q.26** A number is expressed in binary two's complement as 10011. Its decimal equivalent value is \_\_\_\_\_.

[ESE-2002]

**Q.27**  $(X)_8$  is expressed in gray code as  $(11110)_2$ . The value of  $X$  is \_\_\_\_\_.

Q.28 The 16-bit 2's complement representation of an integer is 1111 1111 1111 0101; its decimal representation is \_\_\_\_\_.

[GATE-2016]

Q.29 Given  $(135)_{\text{base } x} + (144)_{\text{base } x} = (323)_{\text{base } x}$   
The value of base  $x$  is \_\_\_\_\_.

[ESE-2005]

Q.30 The base (or radix) of the number system such that the following equation holds is \_\_\_\_\_.

$$\frac{312}{20} = 13.1$$

[GATE-2014]

Q.31 2's complement representation of a 16-bit number (one sign bit and 15 magnitude bits) is FFFF. Its magnitude in decimal representation is \_\_\_\_\_.

[GATE-1993]

Q.32 The minimum decimal equivalent of the number 11C.0 is \_\_\_\_\_.

[ESE-2000]

Q.33 The decimal equivalent of hexadecimal number of 2A0F is \_\_\_\_\_.

[ESE-2002(EE)]

Q.34 In a particular number system having base  $B$ .

$$(\sqrt{41})_B = 5_{10}. \text{ The value of 'B' is _____.}$$

Q.35 Consider a system which has two eight bit inputs  $D_1 = 01010101$ ,  $D_2 = 00000000$ , the system produces eight bit output that is bit wise XOR of the inputs. The eight bit output of the system is input to the Gray Code Converter, the decimal equivalent of the output from Gray Code Converter is \_\_\_\_\_.



### Multiple Select Questions

Q.36 In a 6 bit register

- (a) Smallest decimal number possible to represent is -32 in 1's complement representation.

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- (b) Highest decimal number possible to represent is +31 in 1's complement representation.
- (c) Smallest decimal number possible to represent is -32 in 2's complement representation.
- (d) Highest decimal number possible to represent is +32 in 2's complement representation.

Q.37 Decimal number - 8 can be represented

- (a) 1000 in sign 2's complement notation.
- (b) 11000 in sign 1's complement notation.
- (c) 11000 in sign 2's complement notation.
- (d) 11000 in sign magnitude notation.

Q.38 Gray code is

- (a) Unit distance code.
- (b) Self complementary code.
- (c) Used in BCD arithmetic circuits.
- (d) Reflective code.

Q.39 The arithmetic operation  $\frac{(41)_b}{(3)_b} = (13)_b$  is correct

- (a) if  $b$  is 11
- (b) if  $b$  is 17
- (c) if  $b$  is 5
- (d) if  $b$  is 8



### Try Yourself

T1. Twos complement format of + 127 is

- (a) 01111111
- (b) 10000000
- (c) 01101101
- (d) 10010010

[Ans: (a)]

T2. An equivalent 2's complement representation of the 2's complement number 1101 is

- (a) 110100
- (b) 001101
- (c) 110111
- (d) 111101

[GATE-1998, Ans: (d)]

T3. Find the value of  $x$ .

$$(135)_x + (144)_8 = (214)_{x+2}$$

[Ans:  $x = 7$ ]

T4. Consider the addition of numbers with different bases



## 2

# Boolean Algebra, Logic Gates and K-Maps

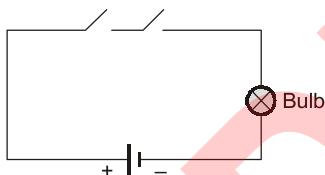


## Multiple Choice Questions

- Q.1** The precedence order while solving Boolean expression is

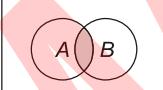
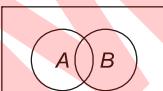
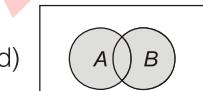
- (a) ( ) < OR < AND < NOT
- (b) ( ) > NOT > AND > OR
- (c) ( ) < NOT < AND < OR
- (d) ( ) < AND > NOT > OR

- Q.2** What logic gate is represented by the circuit shown below?



- (a) AND
- (b) NAND
- (c) NOR
- (d) EQUIVALENCE

- Q.3** The expression  $A + \bar{A}B$  is represented by

- (a) 
- (b) 
- (c) 
- (d) 

- Q.4** If  $X = 1$  in the logic equation

$$[X + Z\{\bar{Y} + (\bar{Z} + X\bar{Y})\}] \{ \bar{X} + \bar{Z}(X + Y) \} = 1 \text{ then}$$

- (a)  $Y = Z$
- (b)  $Y = \bar{Z}$
- (c)  $Z = 0$
- (d)  $Z = 1$

[GATE-2009]

- Q.5** The Boolean expression

$$ABCD + A\bar{B}CD + ABC\bar{D} + A\bar{B}C\bar{D}$$

is equivalent to

- (a)  $A$
- (b)  $AC$
- (c)  $ABC$
- (d)  $1$

[ESE-2008]

- Q.6** If  $x$  and  $y$  are Boolean variables, which one of the following is the equivalent of  $x \oplus y \oplus xy$ ?

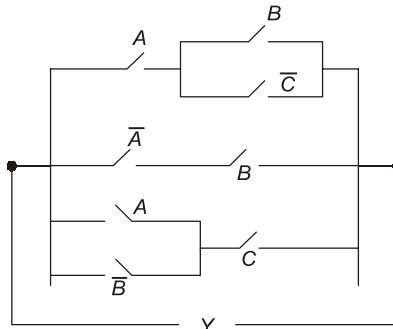
- (a)  $x + \bar{y}$
- (b)  $x + y$
- (c)  $0$
- (d)  $1$

[ESE-2004 (EE)]

- Q.7** The Boolean expression  $\bar{Y}\bar{Z} + \bar{X}\bar{Y} + \bar{X}\bar{Z}$  is logically equivalent to

- (a)  $YZ + \bar{X}$
- (b)  $X\bar{Y}\bar{Z} + \bar{X}\bar{Y}\bar{Z} + \bar{X}Y\bar{Z} + \bar{X}\bar{Y}Z$
- (c)  $XYZ + \bar{X}\bar{Y}\bar{Z}$
- (d)  $XY + YZ + XZ$

- Q.8** Minimized expression for  $Y$  is



- (a)  $A + B + C$
- (b)  $A + BC$
- (c)  $A + \bar{B}C$
- (d)  $\bar{A} + \bar{B} + \bar{C}$

- Q.9** If the output of a logic gate is '1' when all its inputs are at logic '0', the gate is either  
 (a) A NAND or A NOR  
 (b) An AND or an EX-NOR  
 (c) An OR or an NAND  
 (d) An EX-OR or an EX-NOR

[ESE-2014]

- Q.10** Consider the statement below:

1. If the output waveform from an OR gate is the same as the waveform at one of its inputs, the other input is being held permanently LOW.
2. If the output waveform from an OR gate is always HIGH, one of its input is being held permanently HIGH.

The statement/statements, which is/or always true

- (a) Both 1 and 2    (b) Only 1  
 (c) Only 2            (d) None of these

- Q.11** The function

$$f = (A\bar{B}\bar{C} + \bar{A}B\bar{C} + ABC + \bar{A}\bar{B}C) \oplus A \text{ can be}$$

written as:

- (a)  $B \oplus C$     (b)  $A \oplus B \oplus A$   
 (c)  $A$             (d) None of these

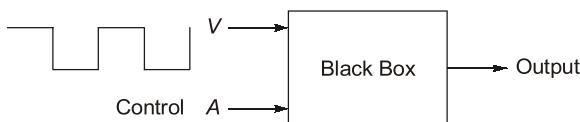
**Q.12**  $[(A + A\bar{B})(A + \bar{A}B)] + [(CD + \bar{C}\bar{D}) + (C \oplus D)] =$

- (a)  $B$     (b)  $A$   
 (c)  $0$     (d)  $1$

- Q.13** If a variable is having Ex-OR operation itself 'n' number of times, then the result is

- (a) Complement of variable if 'n' is even.
- (b) Uncomplement of variable if 'n' is even.
- (c) Complement of the variable if 'n' is odd.
- (d) Uncomplement of the variable if 'n' is odd.

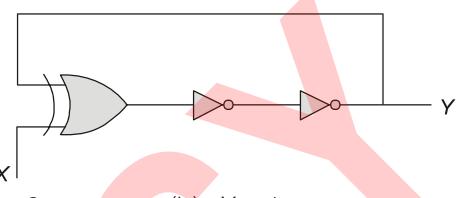
- Q.14** Black box inverts the phase of input  $V$  when control 'A' is 1 and lets it pass through uninverted when control 'A' is 0 then circuit is



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- (a) XNOR gate    (b) XOR gate  
 (c) NAND gate    (d) NOR gate

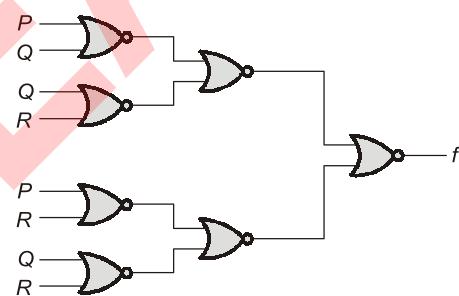
- Q.15** All the logic gates in the circuit shown below have finite propagation delay. The circuit can be used as a clock generator, if



- (a)  $X = 0$     (b)  $X = 1$   
 (c)  $X = 0 \text{ or } 1$     (d)  $X = Y$

[GATE-IN : 2006]

- Q.16** What is the boolean expression for the output of the combinational logic circuit of NOR gates given below?



- (a)  $\overline{Q+R}$     (b)  $\overline{P+Q}$   
 (c)  $\overline{P+R}$     (d)  $\overline{P+Q+R}$

[GATE-2010]

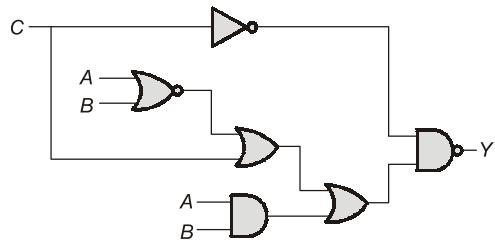
- Q.17 Statement (I):** XOR gate is not a universal gate.

- Statement (II):** It is not possible to realize any Boolean function using XOR gates only.

- (a) Both Statement (I) and Statement (II) are individually true and Statement (II) is the correct explanation of Statement (I).
- (b) Both Statement (I) and Statement (II) are individually true but Statement (II) is not the correct explanation of Statement (I).
- (c) Statement (I) is true but Statement (II) is false.
- (d) Statement (I) is false but Statement (II) is true.

[ESE-2012]

**Q.18** In the circuit shown in the figure, if  $C = 0$ , the expression for  $Y$  is

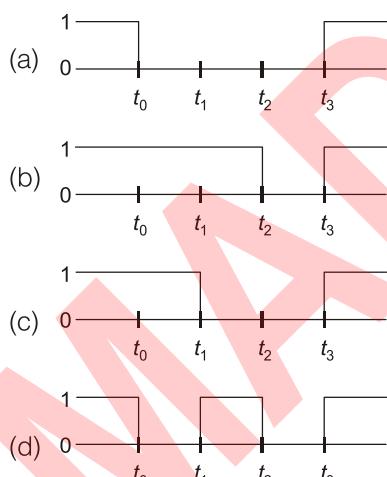
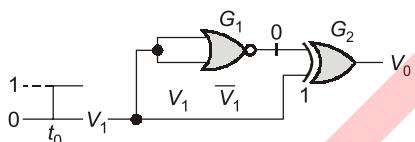


- (a)  $Y = A\bar{B} + \bar{A}B$       (b)  $Y = A + B$   
 (c)  $Y = \bar{A} + \bar{B}$       (d)  $Y = AB$

[GATE-2014]

**Q.19** The gates  $G_1$  and  $G_2$  in the figure have propagation delays of 10 nsec and 20 nsec respectively. If the input  $V_i$  makes an abrupt change from logic 0 to 1 at time  $t = t_0$ , then the output waveform  $V_o$  is

$$(t_1 = t_0 + 10 \text{ ns}, t_2 = t_0 + 20 \text{ ns}, t_3 = t_0 + 30 \text{ ns})$$



[GATE-2002]

**Q.20** The Boolean expression  $AC + B\bar{C}$  is equivalent to

- (a)  $\bar{A}C + B\bar{C} + AC$   
 (b)  $\bar{B}C + AC + B\bar{C} + \bar{A}CB$

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- (c)  $AC + B\bar{C} + \bar{B}C + ABC$   
 (d)  $ABC + \bar{A}\bar{B}\bar{C} + AB\bar{C} + A\bar{B}C$

[GATE-EC : 2004]

**Q.21** The switching expression corresponding to  $f(A, B, C, D) = \Sigma(1, 4, 5, 9, 11, 12)$  is

- (a)  $BC'D' + A'C'D + AB'D$   
 (b)  $ABC' + ACD + B'C'D$   
 (c)  $ACD' + A'B'C + AC'D'$   
 (d)  $A'BD + ACD' + BCD'$

[ISRO-2009]

**Q.22** What is the minimized logic expression corresponding to the given Karnaugh Map?

$wx$	$yz$	00	01	11	10
00			1		
01	1	1	1		
11		1	1	1	
10		1			

- (a)  $xz$   
(b)  $\bar{w}x\bar{y} + \bar{w}yz + w\bar{y}z + wxy$   
(c)  $\bar{w}x\bar{y} + \bar{w}yz + w\bar{y}\bar{z} + wx\bar{y}$   
(d)  $xz + \bar{w}wz + \bar{w}x\bar{v} + wxv + \bar{w}z$

[ESE-2005]

**Q.23** The function  $f(A, B, C, D) = \Sigma(5, 7, 9, 11, 13, 15)$  is independent of variable(s)



[DRDO-2009]

**Q.24** An odd function involving three Boolean variables is

- (a)  $\Sigma(1, 3, 5, 7)$       (b)  $\Sigma(0, 2, 4, 6)$   
(c)  $\Sigma(1, 2, 4, 7)$       (d)  $\Sigma(0, 3, 5, 6)$

[DRDO-2009]

**Q.25** The min term of  $f(P, Q, R) = PQ + QR' + PR'$  is

- (a)  $m_2 + m_4 + m_6 + m_7$   
 (b)  $m_0 + m_1 + m_3 + m_5$   
 (c)  $m_0 + m_1 + m_6 + m_7$   
 (d)  $m_2 + m_3 + m_4 + m_5$

[GATE-2010]

**Q.26** The Boolean functions can be expressed in canonical SOP (sum of products) and POS (product of sums) form. For the functions,  $Y = A + \bar{B}C$ , which are such two forms

- (a)  $Y = \Sigma(1, 2, 6, 7)$  and  $Y = \Pi(0, 2, 4)$
  - (b)  $Y = \Sigma(1, 4, 5, 6, 7)$  and  $Y = \Pi(0, 2, 3)$
  - (c)  $Y = \Sigma(1, 2, 5, 6, 7)$  and  $Y = \Pi(0, 1, 3)$
  - (d)  $Y = \Sigma(1, 2, 4, 5, 6, 7)$  and  $Y = \Pi(0, 2, 3, 4)$
- [GATE-2008]

**Q.27** The SOP (sum of products) form of a Boolean function is  $\Sigma(0, 1, 3, 7, 11)$ , where inputs are  $A, B, C, D$  ( $A$  is MSB, and  $D$  is LSB). The equivalent minimized expression of the function is

- (a)  $(\bar{B} + C)(\bar{A} + C)(\bar{A} + \bar{B})(\bar{C} + D)$
- (b)  $(\bar{B} + C)(\bar{A} + C)(\bar{A} + \bar{C})(\bar{C} + D)$
- (c)  $(\bar{B} + C)(\bar{A} + C)(\bar{A} + \bar{C})(\bar{C} + \bar{D})$
- (d)  $(\bar{B} + C)(A + \bar{B})(\bar{A} + \bar{B})(\bar{C} + D)$

[GATE-2014]

**Q.28** What is the minimum number of NAND gates required to implement  $A + A\bar{B} + \bar{B}C(A + \bar{C})$ ?

- (a) 0
- (b) 2
- (c) 4
- (d) 6

[GATE-2004]

#### Linked Answer Questions (29 and 30):

The following Karnaugh map represents a function  $F$ .

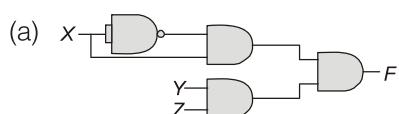
	Y\Z	00	01	11	10
0	1	1	1	0	
1	0	0	1	0	

**Q.29** A minimized form of the function  $F$

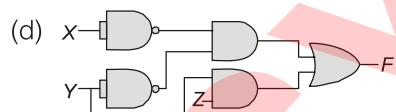
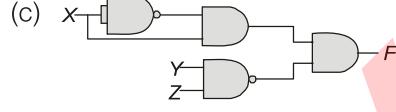
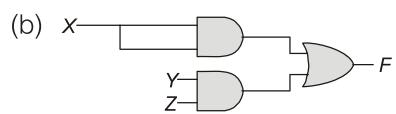
- (a)  $F = \bar{X}Y + YZ$
- (b)  $F = \bar{X} \cdot \bar{Y} + YZ$
- (c)  $F = \bar{X}Y + Y\bar{Z}$
- (d)  $F = \bar{X}Y + \bar{Y}Z$

[GATE-2010]

**Q.30** Which of the following circuits is a realization of the above function  $F$ ?



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[GATE-2010]

**Q.31** Which are the essential prime implicants of the following Boolean function?

- $$f(a, b, c) = a'c + ac' + b'c:$$
- (a)  $a'c$  and  $ac'$
  - (b)  $a'c$  and  $b'c$
  - (c)  $a'$  only
  - (d)  $a'$  and  $bc'$

[GATE-2004]

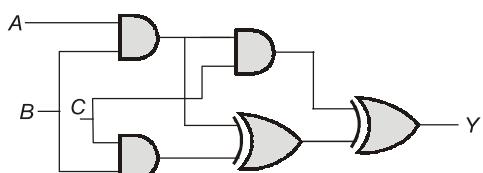
**Q.32** Consider the Boolean function:

$$F(w, x, y, z) = wy + xy + \bar{w}xyz + \bar{w}\bar{x}y + xz + \bar{x}\bar{y}\bar{z}.$$

Which one of the following is the complete set of essential prime implicants?

- (a)  $w, y, xz, \bar{x}\bar{z}$
- (b)  $w, y, xz$
- (c)  $y, \bar{x}\bar{y}\bar{z}$
- (d)  $y, xz, \bar{x}\bar{z}$

**Q.33** The output of the combinational circuit given below is



- (a)  $A + B + C$
- (b)  $A(B + C)$
- (c)  $B(C + A)$
- (d)  $C(A + B)$

[GATE-2016]

**Q.34** The minimum number of 2-input NAND gates required to implement a 2-input XOR gate is

- (a) 4
- (b) 5
- (c) 6
- (d) 7

[GATE-2016]

- Q.35** Consider the Boolean operator # with the following properties:

$x \# 0 = x$ ,  $x \# 1 = \bar{x}$ ,  $x \# x = 0$  and  $x \# \bar{x} = 1$ .

Then  $x \# y$  is equivalent to

- (a)  $x\bar{y} + \bar{x}y$       (b)  $\bar{x}\bar{y} + \bar{x}y$   
 (c)  $\bar{x}y + xy$       (d)  $xy + \bar{x}\bar{y}$

[GATE-2016]

- Q.36** The minimized function  $f$  obtained from the K-map given below is

		BC		A'
		DE		
1				1
			1	
			1	
1				1

		BC		A
		DE		
1				1
				1
1				1

- (a)  $C'E' + A'BCE + BCD'E$   
 (b)  $B'C'E' + A'BCE + ABCD'E + BC'E$   
 (c)  $C'E' + A'BCD + BCDE$   
 (d)  $B'C'E + A'BCE + ABCD'E + BC'E$

[DRDO-2008]

2  
3  
6  
9

### Numerical Answer Type Questions

- Q.37** Consider the logical functions given below:

$$f_1(A, B, C) = \Sigma(2, 3, 4)$$

$$f_2(A, B, C) = \pi(0, 1, 3, 6, 7)$$



If  $f$  is logic zero, then maximum number of possible minterms in function  $f_3$  are \_\_\_\_\_.

- Q.38** Minimum number of 2 input NAND gates required to implement the logic function  $F = A + B + C + D$  are \_\_\_\_\_.

- Q.39** The minimum number of 2 input NOR gates required to realize the Boolean function  $f(A, B, C) = A\bar{B}C$ .

- Q.40** Consider the function:

$$f = \bar{A}(\bar{B}C + BCD) + \bar{B}\bar{D}(A + C) + \bar{A}\bar{B}\bar{C}$$

$$d = \bar{A}B(C\bar{D} + \bar{C}D) + ACD$$

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Where ' $f$ ' represents Boolean function and ' $d$ ' represents don't care condition.

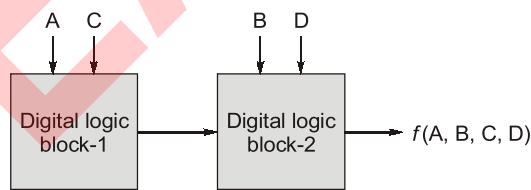
Then simplified Boolean expression ' $f$ ' is reduced to \_\_\_\_\_ literals.

- Q.41** The number of prime-implicants for the given function  $f(A, B, C) = \Sigma_m(0, 2, 5, 6, 7)$  is \_\_\_\_\_.

- Q.42** The number of essential prime-implicants in the given function  $f(w, x, y, z) = \Sigma_m(0, 2, 6, 7, 8, 9, 13, 15)$  is \_\_\_\_\_.

- Q.43** A cyclic prime implicant Boolean function is having how many minimal forms?

- Q.44** The function  $f(A, B, C, D) = \Sigma_m(3, 4, 5, 7, 9, 13, 14, 15)$  is realised with following digital logic block circuit. Each digital logic block is implemented with minimum number of 2 input NAND gates. The number of NAND gates required are \_\_\_\_\_.



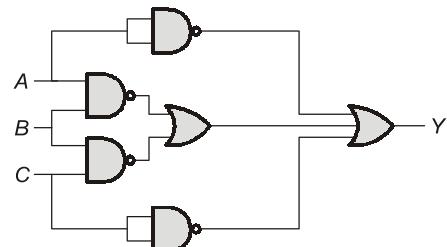
### Multiple Select Questions

- Q.45** Consider:

$Y = A \oplus \bar{A} \oplus \bar{A} \oplus A \oplus A \oplus \bar{A} \oplus \bar{A} \oplus \bar{A} \oplus A$  the  $Y$  is equivalent to:

- (a) 1 OR A      (b) A EX OR 0  
 (c) 1 NOR A      (d) A AND A

- Q.46** For the logic circuit shown in figure below, the output 'Y' is equal to



- (a)  $\overline{AB} + \overline{BC} + \overline{B} + \overline{C}$       (b)  $\overline{AB} + \overline{BC}$   
 (c)  $\overline{A} + \overline{B} + \overline{C}$       (d)  $\overline{A} + B + C$

**Q.47**  $f(X, Y, Z) = \Sigma m(1, 2, 4, 7)$  is possible to realize using

- (a) 2 input NOR gates minimum 8.  
 (b) 2 input NAND gates minimum 7.  
 (c) 2 input NOR gates minimum 7.  
 (d) 2 input NAND gates minimum 8.

**Q.48**  $f(w, \boxtimes, y, z) = \Sigma m(0, 1, 5, 11, 12, 13, 15)$  is having  
 (a) 4 essential prime implicants.  
 (b) 2 minimum forms.  
 (c) 3 essential prime implicants.  
 (d) 3 minimal forms.

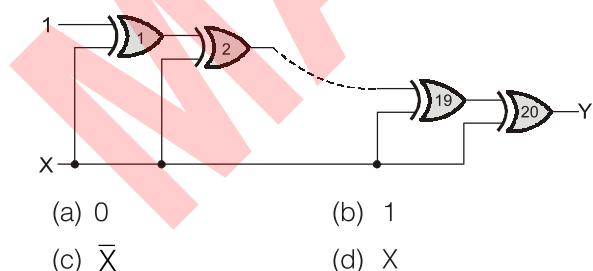
**Q.49** If  $f_1(a, b, c) = \Sigma m(0, 1, 4, 5) + d(2, 7)$  and  $f_2(a, b, c) = \Sigma m(1, 2, 5, 6) + d(4)$ , then  $f_1 \cdot f_2$  is having  
 (a) 4 combinations as max terms.  
 (b) Unique minimal form.  
 (c) 3 combinations as don't cares.  
 (d) 2 combinations as don't cares.

**Q.50**  $f(a, b, c) = \Sigma m(0, 1, 3, 5)$  is  
 (a) A self dual function.  
 (b) Having unique minimal form.  
 (c) Having 3 essential prime implicants.  
 (d) A neutral function.



### Try Yourself

**T1.** If input to digital circuit consisting of a cascade of 20 EXOR gates is 'X' then output 'Y' is:



[Ans: (b)]

**T2.** Define the connective \* for the Boolean variables X and Y as  $X * Y = XY + X'Y'$ . Let  $Z = X * Y$ . Consider the following expressions P, Q and R.

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$$P : X = Y * Z$$

$$Q : Y = X * Z$$

$$R : X * Y * Z = 1$$

Which of the following is TRUE?

- (a) Only P and Q are valid  
 (b) Only Q and R are valid  
 (c) Only P and R are valid  
 (d) All P, Q, R are valid

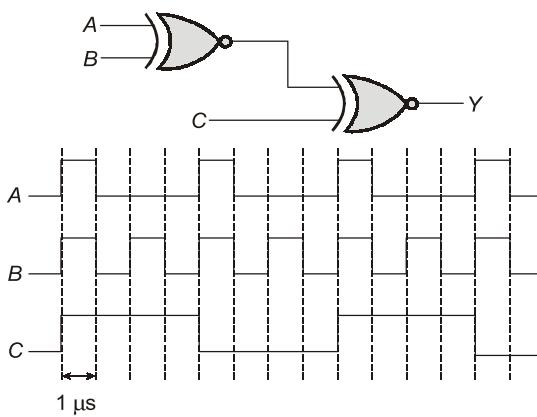
[GATE-2007, Ans: (d)]

**T3.** Which one of the following figures represents the coincidence logic?

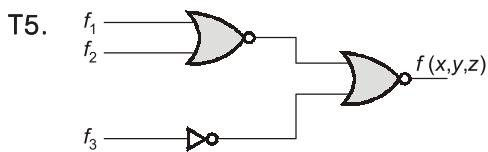
- (a)
- (b)
- (c)
- (d)

[ESE-2000, Ans: (a)]

**T4.** If the waveforms A, B, C shown in figure below are applied to the Ex-NOR gates. Find the frequency of output.



[Ans: 125 kHz]



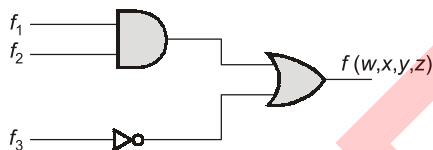
If  $f_1(x, y, z) = \sum m(0, 1, 3, 5)$ ,  
 $f_2(x, y, z) = \sum m(4, 5)$  and  
 $f(x, y, z) = \sum m(1, 4, 5)$

Then  $f_3(x, y, z)$  is \_\_\_\_\_

- (a)  $\sum m(1, 4, 5)$
- (b)  $\Pi M(1, 4, 5)$
- (c)  $\Sigma m(1, 4, 5) + d(2, 6, 7)$
- (d)  $\Pi M(1, 4, 5).d(2, 6, 7)$

[Ans: (c)]

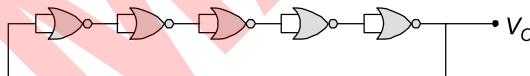
- T6. Determine the function  $f_3$  if  $f_1 = w\bar{x}z + y\bar{z} + x\bar{z}$  and the overall transmission function of the given logic circuit is to be  $f(w, x, y, z) = \sum m(1, 3, 5, 6, 9, 12, 13)$



- (a)  $f_3 = \sum m(0, 2, 4, 7, 8, 10, 11, 14, 15)$
- (b)  $f_3 = \sum m(6, 9, 12)$
- (c)  $f_3 = \sum m(0, 2, 4, 7, 8, 10, 11, 14, 15) + d(6, 9, 12)$
- (d)  $f_3 = \sum m(6, 9, 12) + d(0, 2, 4, 7, 8, 10, 11, 14, 15)$

[Ans: (c)]

- T7. The average propagation delay of each NOR gate shown below is 10 ns. The frequency of the output signal  $V_O$  is \_\_\_\_\_ MHz.



[Ans: 10]

- T8. A Boolean function  $f$  of two variables  $x$  and  $y$  is defined as follows:

$$f(0, 0) = f(0, 1) = f(1, 1) = 1; f(1, 0) = 0$$

Assuming complements of  $x$  and  $y$  are not available, a minimum cost solution for realizing

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fusing only 2-input NOR gates and 2-input OR gates (each having unit cost) would have a total cost of

- (a) 1 unit
- (b) 4 unit
- (c) 3 unit
- (d) 2 unit

[GATE-2004, Ans: (d)]

- T9. A  $T$  gate is having the output  $T(A, B) = \bar{A}\bar{B}$ . Which of the following is/are have about  $T$  gate.

- (a)  $\{T\}$  is functionally complete
- (b)  $\{T, 1\}$  is functionally complete
- (c)  $\{T, 0\}$  is functionally complete
- (d) Both (a) and (b)

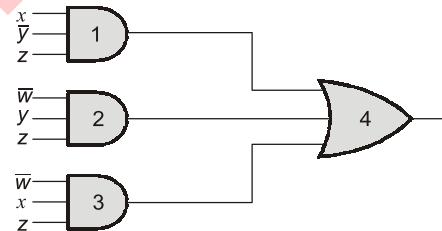
[Ans: (b)]

- T10. The simplification of Boolean expressions.

- $$a + \bar{a}b + \bar{a}\bar{b}c + \dots$$
- (a)  $a + \bar{b} + \bar{c} + \dots$
  - (b)  $\bar{a} + b + \bar{c} + \dots$
  - (c)  $a + b + \bar{c} + \dots$
  - (d)  $a + b + c + \dots$

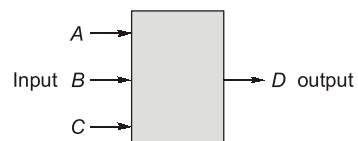
[Ans: (d)]

- T11. The following labelled 1, 2, 3 and 4 in the network shown in the figure is redundant \_\_\_\_\_.



[ESE-1999, Ans: (3)]

- T12. For the box shown the output  $D$  is true if and only if a majority of the inputs are true.



The Boolean function for the output is

- (a)  $D = ABC + \bar{A}BC + A\bar{B}C$
- (b)  $D = ABC + \bar{A}BC + A\bar{B}C + AB\bar{C}$
- (c)  $D = \bar{A}\bar{B}\bar{C} + AB + AC + BC$
- (d)  $D = \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + \bar{A}B\bar{C} + ABC$

[ESE-2013, Ans: (b)]

- T13.** What is the Boolean expression for the truth table shown below?

A	0	0	0	0	1	1	1	1
B	0	0	1	1	0	0	1	1
C	0	1	0	1	0	1	0	1
f	0	0	0	1	0	0	1	0

- (a)  $B(A + C)(\bar{A} + \bar{C})$
- (b)  $B(A + \bar{C})(\bar{A} + C)$
- (c)  $\bar{B}(A + C)(\bar{A} + C)$
- (d)  $\bar{B}(A + C)(\bar{A} + \bar{C})$

[GATE-2006, Ans: (a)]

- T14.** A bank has 3 locks with 1 key for each lock. Each key is owned by a different person. In order to open the vault atleast two people must insert their keys into the assigned locks. All the keys are not inserted at the same time. If the system is to be designed with only two input NAND gates, then find the number of NAND gates required.

[Ans: 6]

- T15.** A logic circuit implements the following Boolean function:

$$F(A, B, C, D) = \bar{A}\bar{C} + A\bar{C}D$$

It is found that in the circuit the input combination  $A = C$  can never occur. Find a simpler expression for  $F$ .

[ESE-2014, Ans:  $C + D$  or  $A' + D$ ]

- T16.** The standard sum of products of the function  $f = A + B'C$  is expressed as:

- (a)  $\Sigma m(1, 4, 5, 6, 7) + d(2, 3)$
- (b)  $\Sigma m(1, 4, 5, 6, 7)$
- (c)  $\Sigma m(0, 2, 3) + d(1, 4, 5, 6, 7)$
- (d)  $\Pi M(1, 4, 5, 6, 7)$

[DRDO-2008, Ans: (b)]

- T17.** The black box in the below figure consists of a minimum complexity circuit that uses only AND, OR and NOT gates. The function  $f(x, y, z) = 1$  whenever  $x, y$  are different and 0 otherwise. In

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addition the 3 inputs  $x, y, z$  are never all the same value. Which one of the following equations leads to the correct design for the minimum complexity circuit?



- (a)  $x'y + xy'$
- (b)  $x + y'z$
- (c)  $x'y'z' + xy'z$
- (d)  $xy + y'z + z'$

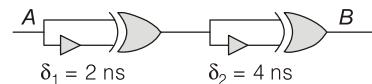
[GATE-2007, Ans: (a)]

- T18.** Let,  $x_1 \oplus x_2 \oplus x_3 \oplus x_4 = 0$  where  $x_1, x_2, x_3, x_4$  are Boolean variables, and  $\oplus$  is the XOR operator. Which one of the following must always be TRUE?

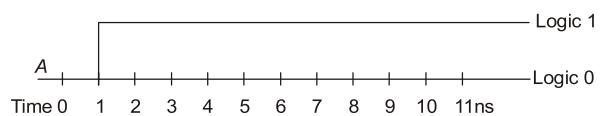
- (a)  $x_1 x_2 x_3 x_4 = 0$
- (b)  $x_1 x_3 + x_2 = 0$
- (c)  $\bar{x}_1 \oplus \bar{x}_3 = \bar{x}_2 \oplus \bar{x}_4$
- (d)  $x_1 + x_2 + x_3 + x_4 = 0$

[GATE-2016, Ans: (c)]

- T19.** Consider the following circuit composed of XOR gates and non-inverting buffers.



The non-inverting buffers have delays  $\delta_1 = 2$  ns and  $\delta_2 = 4$  ns as shown in the figure. Both XOR gates and all wires have zero delay. Assume that all gate inputs, outputs and wires are stable at logic level 0 at time 0. If the following waveform is applied at input A, how many transition(s) (change of logic levels) occur(s) at B during the interval from 0 to 10 ns



- (a) 1
- (b) 2
- (c) 3
- (d) 4

[GATE-2003, Ans: (d)]

- T20. A Boolean function  $f(A, B, C, D)$  is given in the map shown below. Identify how many minimum number of 2 input NAND gates required to realize the function?

		A,C	00	01	10	11	
		B,D	00	1	1	1	1
		01	1	1	1	1	
		10		1		1	
		11		1		1	

[Ans: (2)]

- T21. Following is the K-map of a Boolean function of five variables  $P, Q, R, S$  and  $X$ . The minimum sum-of-product (SOP) expression for the function is

		PQ	00	01	11	10		PQ	00	01	11	10	
		RS	00	0	0	0		RS	00	0	1	1	0
		01	1	0	0	1		01	0	0	0	0	0
		11	1	0	0	1		11	0	0	0	0	0
		10	0	0	0	0		10	0	1	1	0	

$X = 0$

$X = 1$

- (a)  $\bar{P}\bar{Q}S\bar{X} + P\bar{Q}S\bar{X} + Q\bar{R}\bar{S}X + QR\bar{S}X$
- (b)  $\bar{Q}S\bar{X} + Q\bar{S}X$
- (c)  $\bar{Q}SX + Q\bar{S}X$
- (d)  $\bar{Q}S + Q\bar{S}$

[GATE-2016, Ans: (b)]



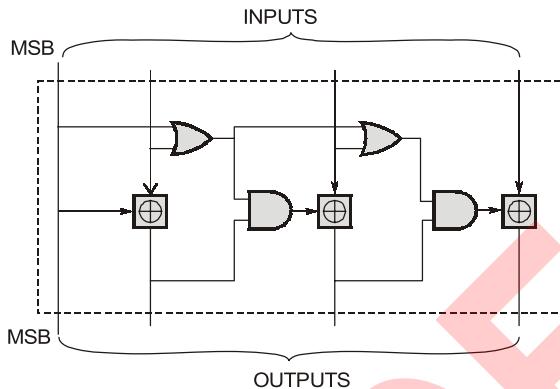
## 3

## Combinational Logic Circuits



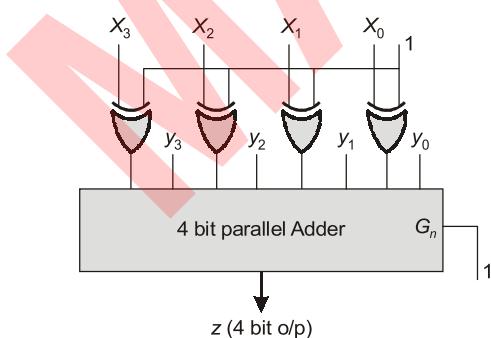
## Multiple Choice Questions

**Q.1** The circuit shown in the figure converts



- (a) BCD to binary code
- (b) Binary to excess - 3 code
- (c) Excess - 3 to Gray code
- (d) Gray to Binary code

**Q.2** Identify the correct statement with respect to following circuit? Numbers are represented in signed magnitude format.



- (a) It outputs  $x + y$
- (b) It outputs  $y - x$
- (c) It outputs  $x + 1$
- (d) It outputs  $y + 1$

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**Q.3**  $x$  and  $y$  are two  $n$ -bit numbers. These numbers are added by a  $n$ -bit carry-lookahead adder, which uses  $k$  logic-levels. If the average gate delay of carry-lookahead adder is  $d$  then what will be the maximum delay of carry-lookahead adder circuit?

- (a)  $n^2$
- (b)  $kd$
- (c)  $nkd$
- (d)  $nd$

**Q.4** In a look-ahead carry generator, the carry generate function  $G_i$  and the carry propagate function  $P_i$  for inputs,  $A_i$  and  $B_i$  are given by

$$P_i = A_i \oplus B_i \text{ and } G_i = A_i B_i$$

The expressions for the sum bit  $S_i$  and carry bit  $C_{i+1}$  of the look-ahead carry adder are given by  $S_i = P_i \oplus C_i$  and  $C_{i+1} = G_i + P_i C_i$ , where  $C_0$  is the input carry.

Consider a two-level logic implementation of the look-ahead carry generator. Assume that all  $P_i$  and  $G_i$  are available for the carry generator circuit and that the AND and OR gates can have any number of inputs. The number of AND gates and OR gates needed to implement the look-ahead carry generator for a 4-bit adder with  $S_3$ ,  $S_2$ ,  $S_1$ ,  $S_0$  and  $C_4$  as its outputs are respectively

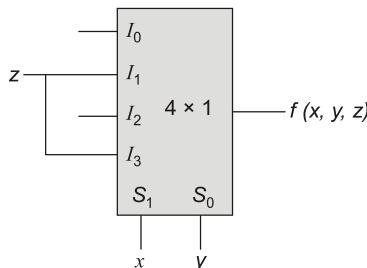
- (a) 6, 3
- (b) 10, 4
- (c) 6, 4
- (d) 10, 5

**Q.5** Consider two 4-bit numbers  $A = A_3 A_2 A_1 A_0$  and  $B = B_3 B_2 B_1 B_0$  and the expression  $x_i = A_i B_i + \overline{A_i} \overline{B_i}$  for  $i = 0, 1, 2, 3$ . The expression  $A_3 \overline{B_3} + x_3 A_2 \overline{B_2} + x_3 x_2 A_1 \overline{B_1} + x_3 x_2 x_1 A_0 \overline{B_0}$  evaluates to 1 if

- (a)  $A = B$   
 (b)  $A \neq B$   
 (c)  $A > B$   
 (d)  $A < B$

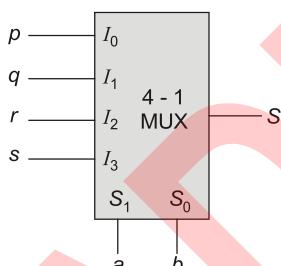
[DRDO-2009]

Q.6 Consider the following circuit:

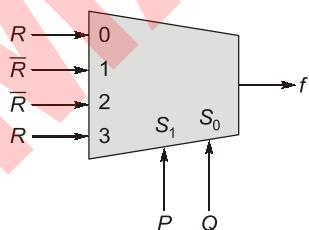


If  $f(x, y, z)$  is  $\Sigma(0, 3, 5, 7)$  then what will be the value of at  $I_0$  and  $I_2$  (respectively)?

- (a)  $\bar{z}, z$   
 (b)  $\bar{z}, \bar{z}$   
 (c)  $z, z$   
 (d)  $z, \bar{z}$
- Q.7 Consider the function  $F(a, b, c) = \bar{b}\bar{c} + bc + \bar{a}$ . If you implement  $F$  by means of 4-to-1 multiplexer then what will be the values of  $p, q, r, s$ , in the following figure.



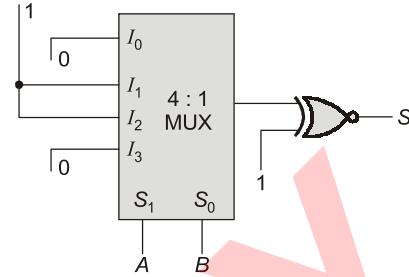
- (a)  $\bar{c}, c, 1, c$   
 (b)  $c, \bar{c}, c, 0$   
 (c)  $1, 0, c, \bar{c}$   
 (d)  $c, \bar{c}, 1, \bar{c}$

Q.8 The Boolean expression for the output  $f$  of the multiplexer shown below is

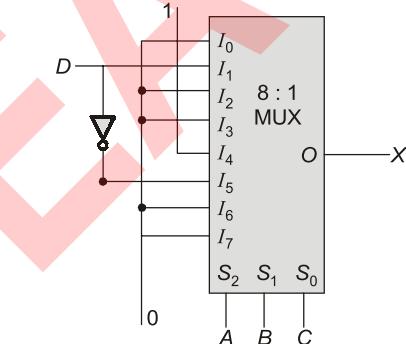
- (a)  $\overline{P \oplus Q \oplus R}$   
 (b)  $P \oplus Q \oplus R$   
 (c)  $P + Q + R$   
 (d)  $\overline{P + Q + R}$

[GATE-2010]

Q.9 The circuit shown below does not represent



- (a)  $S(A, B) = \Sigma(1, 2)$   
 (b) EXOR gate with  $A$  and  $B$  as inputs  
 (c)  $S(A, B) = \Pi(0, 3)$   
 (d) Equality function

Q.10 The circuit below represents function  $X(A, B, C, D)$  as:

- (a)  $\Sigma(3, 8, 9, 10)$   
 (b)  $\Sigma(3, 8, 10, 14)$   
 (c)  $\Pi(0, 1, 2, 4, 5, 6, 7, 11, 12, 13, 15)$   
 (d)  $\Pi(0, 1, 2, 4, 5, 6, 7, 10, 12, 13, 15)$

Q.11 Consider the multiplexer with  $X$  and  $Y$  as data inputs and  $Z$  as control input.  $Z = 0$  selects input  $X$  and  $Z = 1$  selects input  $Y$ . What are the connections required to realize the 2-variable Boolean function  $f = T + R$ , without using any additional hardware?

- (a)  $R$  to  $X$ ,  $1$  to  $Y$ ,  $T$  to  $Z$   
 (b)  $T$  to  $X$ ,  $R$  to  $Y$ ,  $T$  to  $Z$   
 (c)  $T$  to  $X$ ,  $R$  to  $Y$ ,  $0$  to  $Z$   
 (d)  $R$  to  $X$ ,  $0$  to  $Y$ ,  $T$  to  $Z$

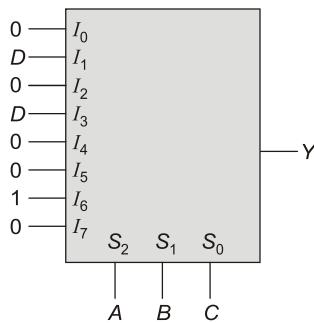
[ESE-2009]

Q.12 Suppose only one multiplexer and one inverter are allowed to be used to implement any Boolean function of  $n$  variables. What is the minimum size of the multiplexer needed?

- (a)  $2^n$  line to 1 line
- (b)  $2^{n+1}$  line to 1 line
- (c)  $2^{n-1}$  line to 1 line
- (d)  $2^{n-2}$  line to 1 line

[GATE-2007]

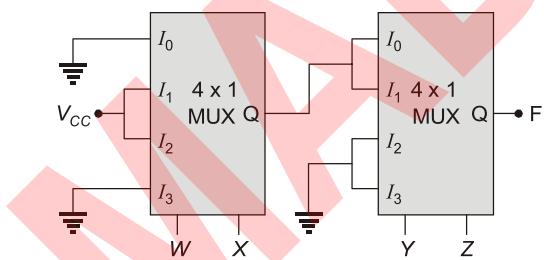
**Q.13** An 8-to-1 multiplexer is used to implement a logical function  $Y$  as shown in the figure. The output



- (a)  $Y = A\bar{B}C + A\bar{C}D$
- (b)  $Y = \bar{A}BC + A\bar{B}D$
- (c)  $Y = ABC\bar{C} + \bar{A}CD$
- (d)  $Y = \bar{A}\bar{B}D + A\bar{B}C$

[GATE-2014]

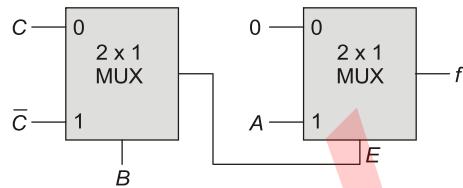
**Q.14** In the circuit shown,  $W$  and  $Y$  are MSBs of the control inputs. The output is given by



- (a)  $F = W\bar{X} + \bar{W}X + \bar{Y}\bar{Z}$
- (b)  $F = W\bar{X} + \bar{W}X + \bar{Y}Z$
- (c)  $F = W\bar{X}\bar{Y} + \bar{W}X\bar{Y}$
- (d)  $F = (\bar{W} + \bar{X})\bar{Y}\bar{Z}$

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**Q.15** The Boolean function ' $f$ ' implemented as shown in the figure using two input multiplexers is

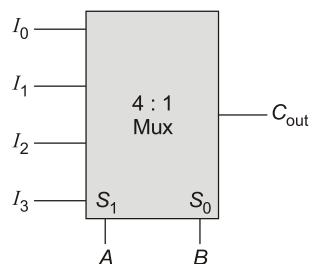


- (a)  $A\bar{B}C + A\bar{C}\bar{D}$
- (b)  $ABC + A\bar{B}\bar{C}$
- (c)  $\bar{A}BC + A\bar{B}\bar{C}$
- (d)  $\bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}$

**Q.16** The minimum number of  $2 \times 1$  multiplexers required to implement a half adder circuit are [when only basic inputs are available, compliments are not available].

- (a) 4
- (b) 2
- (c) 3
- (d) 5

**Q.17** A 4:1 multiplexer is to be used for generating the output carry of a full adder.  $A$  and  $B$  are the bits to be added while  $C_{in}$  is the input carry and  $C_{out}$  is the output carry.  $A$  and  $B$  are to be used as the select bits with  $A$  being the most significant select bit.

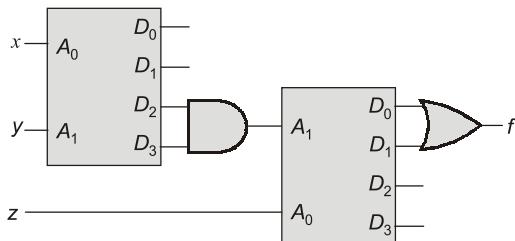


Which one of the following statements correctly describes the choice of signals to be connected to the inputs  $I_0$ ,  $I_1$ ,  $I_2$  and  $I_3$  so that the output is  $C_{out}$ ?

- (a)  $I_0 = 0$ ,  $I_1 = C_{in}$ ,  $I_2 = C_{in}$  and  $I_3 = 1$
- (b)  $I_0 = 1$ ,  $I_1 = C_{in}$ ,  $I_2 = C_{in}$  and  $I_3 = 1$
- (c)  $I_0 = C_{in}$ ,  $I_1 = 0$ ,  $I_2 = 1$  and  $I_3 = C_{in}$
- (d)  $I_0 = 0$ ,  $I_1 = C_{in}$ ,  $I_2 = 1$  and  $I_3 = C_{in}$

[GATE-2016]

**Q.18** A logic circuit consist of two  $2 \times 4$  decoders as shown in the figure. The output of decoder are as follow:

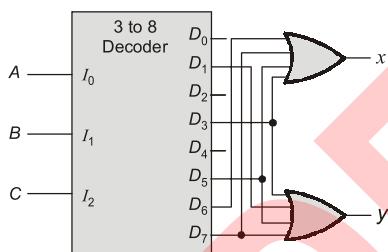


- $$\begin{aligned}D_0 &= 1 \text{ when } A_0 = 0, A_1 = 0 \\D_1 &= 1 \text{ when } A_0 = 1, A_1 = 0 \\D_2 &= 1 \text{ when } A_0 = 0, A_1 = 1 \\D_3 &= 1 \text{ when } A_0 = 1, A_1 = 1\end{aligned}$$

The value of  $f(x, y, z)$  is



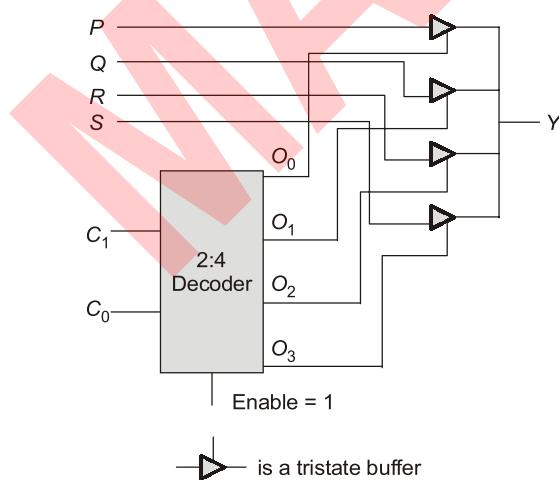
**Q.19** The building block shown in figure is a active high output decoder



The output  $X$  is

- (a)  $AB + BC + CA$       (b)  $A + B + C$   
 (c)  $ABC$       (d) None of these

**Q.20** The functionality implemented by the circuit below is

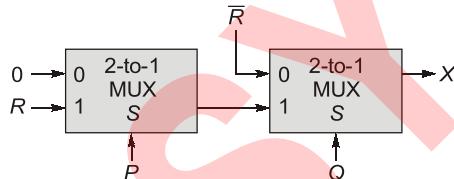


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- (a) 2-to-1 multiplexer
  - (b) 4-to-1 multiplexer
  - (c) 7-to-1 multiplexer
  - (d) 6-to-1 multiplexer

[GATE-2016]

**Q.21** Consider the two cascaded 2-to-1 multiplexers as shown in the figure.



The minimal sum of products form of the output  $X$  is

- (a)  $\bar{P}\bar{Q} + PQR$       (b)  $\bar{P}Q + QR$   
 (c)  $PQ + \bar{P}\bar{Q}\bar{R}$       (d)  $\bar{Q}\bar{R} + PQR$

[GATE-2016]

**Q.22** Who two 8-bit numbers  $A_7 \dots A_0$  and  $B_7 \dots B_0$  in 2's complement representation (with  $A_0$  and  $B_0$  as the least significant bits) are added using a **ripple-carry adder**, the sum bits obtained are  $S_7 \dots S_0$  and the carry bits are  $C_7 \dots C_0$ . An overflow is said to have occurred if

- (a) The carry bit  $C_7$  is 1
  - (b) All the carry bits ( $C_7 \dots C_0$ ) are 1
  - (c)  $(A_7 \cdot B_7 \cdot \bar{S}_7 + \bar{A}_7 \cdot \bar{B}_7 \cdot S_7)$  is 1
  - (d)  $(A_0 \cdot B_0 \cdot \bar{S}_0 + \bar{A}_0 \cdot \bar{B}_0 \cdot S_0)$  is 1

[GATE-2017]



## **Numerical Answer Type Questions**

**Q.23** A one bit full adder takes 75 nsec to produce sum and 50 nsec to produce carry. A 4 bit parallel adder is designed using this type of full adder. The maximum rate of additions per second can be provided by 4 bit parallel adder is  $A \times 10^6$  additions/sec. The value of A is \_\_\_\_\_.

**Q.24** A person wants to design a  $4 \times 1$  multiplexer using only NAND gates. If NAND gates with any number of inputs are available, then total number of NAND gates required are \_\_\_\_\_.

**Q.25** The number of 2-to-4-line decodes with enable input are needed to construct a 4-to-16-line decoder are \_\_\_\_\_. [DRDO-2009]

**Q.26** Minimum number of  $2 \times 1$  multiplexers required to realize the following function is \_\_\_\_\_.  
 $f(A, B, C) = \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}$

(Assume that inputs are available only in true form and Boolean constants 1 and 0 are available.)

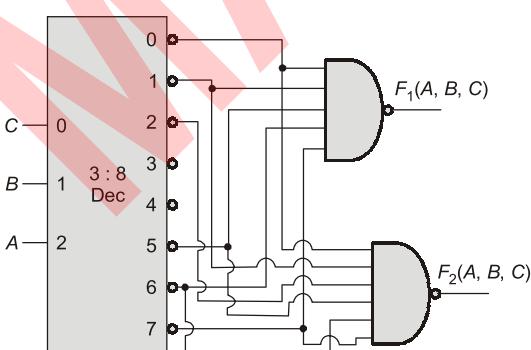


### Multiple Select Questions

**Q.27** A full adder circuit can be implemented using  
 (a)  $4 \times 1$  MUX – 2 No.  
 (b)  $4 \times 1$  MUX – 2 No and NOT gate 1 No.  
 (c)  $8 \times 1$  MUX – 2 No.  
 (d)  $3 \times 8$  Decoder – 1 No.

**Q.28** To design binary subtractor circuit,  
 (a) 1's complement procedure is better, because it uses less hardware.  
 (b) 2's complement procedure is better, because it uses less hardware.  
 (c) Binary '0' is having unique representation in sign 1's complement notation.  
 (d) Binary '0' is having unique representation in sign 2's complement notation.

**Q.29** The function  $F_1$  and  $F_2$ , which are realised by the given circuit are



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- (a)  $F_1 = \bar{A}\bar{B} + AB + AC$
- (b)  $F_1 = \bar{A}\bar{B} + \bar{B}C + AB$
- (c)  $F_2 = \bar{A}\bar{B} + AC + B\bar{C}$
- (d)  $F_2 = \bar{A}\bar{C} + \bar{B}C + AB$

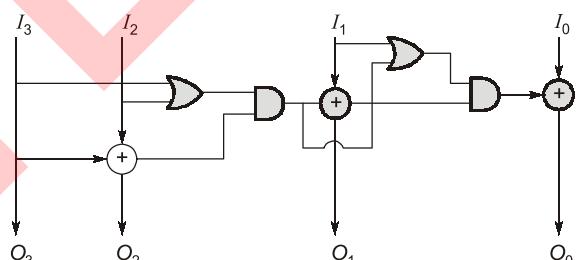
**Q.30** Identify the correct statement(s):

- (a) A multiplexer can be used to convert serial data to parallel form.
- (b) A multiplexer can realize a Boolean function, without using any logic gate.
- (c) A de-multiplexer can be used to convert parallel data to serial form.
- (d) A de-multiplexer can realize a Boolean function, without using any logic gate.



### Try Yourself

**T1.** The circuit shown below converts. (here  $\oplus$  is XOR)



- (a) Binary to gray (b) Binary to Excess 3
- (c) Excess 3 to gray (d) Gray to binary

**[Ans: (d)]**

**T2.** A 1 bit full adder takes 20 ns to generate carry-out bit and 40 ns for the sum bit. What is the maximum rate of addition per second, when four 1 bit full adder are cascade?

**[ESE-2005, Ans:  $10^7$ ]**

**T3.** Given two 3-bit numbers  $a_2a_1a_0$  and  $b_2b_1b_0$  and c the carry in, the function that represents the carry generate function when these two numbers are added is

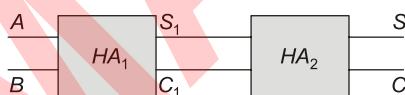
- (a)  $a_2b_2 + a_2a_1b_1 + a_2a_1a_0b_0 + a_2a_0b_1b_0 + a_1b_2b_1 + a_1a_0b_2b_0 + a_0b_2b_1b_0$

- (b)  $a_2b_2 + a_2b_1b_0 + a_2a_1b_1b_0 + a_1a_0b_2b_1 + a_1a_0b_2 + a_1a_0b_2b_0 + a_2a_0b_1b_0$   
 (c)  $a_2 + b_2 + (a_2 \oplus b_2) [a_1 + b_1 + (a_1 \oplus b_1) (a_0 + b_0)]$   
 (d)  $a_2b_2 + \bar{a}_2a_1b_1 + \overline{a_2a_1}a_0b_0 + \bar{a}_2a_0\bar{b}_1b_0 + a_1\bar{b}_2b_1 + \bar{a}_1a_0\bar{b}_2b_0 + a_0\overline{b_2b_1}b_0$
- [GATE-2006, Ans: (a)]

- T4. A 4-bit carry lookahead adder, which adds two 4-bit numbers, is designed using AND, OR, NOT, NAND, NOR gates only. Assuming that all the inputs are available in both complemented and uncomplemented forms and the delay of each gate is 1 time unit, what is the overall propagation delay of the adder? Assume that the carry network has been implemented using two-level AND-OR logic.
- (a) 4 time units    (b) 6 times units  
 (c) 10 times units    (d) 12 times units
- [GATE-2004, Ans: (a)]

- T5. Consider an eight bit ripple-carry adder for computing the sum of  $A$  and  $B$ , where  $A$  and  $B$  are integers represented in 2's complement form. If the decimal value of  $A$  is one, the decimal value of  $B$  that leads to the longest latency for the sum to stabilize is \_\_\_\_\_.
- [Gate-2016, Ans: (-1)]

- T6. Two Half Adders are connected in cascade as shown in figure below. The output "S" and "C" are



- (a)  $S = A \oplus B, C = AB$   
 (b)  $S = A \odot B, C = 0$   
 (c)  $S = A + B, C = 0$   
 (d)  $S = AB, C = 0$

[Ans: (c)]

- T7. A 4 bit binary adder is adding two  $BCD$  numbers and producing the sum output  $S_3S_2S_1S_0$  along with the carry output  $C_0$ . It is required to design

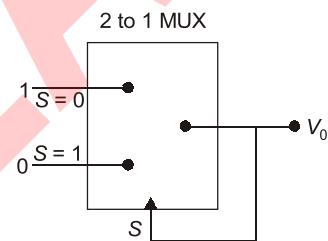
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a checking circuit such that the checking circuit output must be zero, whenever the binary adder output is invalid  $BCD$ , the boolean expression of checking circuit is

- (a)  $\bar{C}_0\bar{S}_3 + \bar{C}_0\bar{S}_2\bar{S}_1$   
 (b)  $C_0 + S_3S_2 + S_2S_1$   
 (c)  $(\bar{C}_0 + \bar{S}_3) \cdot (\bar{C}_0 + \bar{S}_2 + \bar{S}_1)$   
 (d) None of the above

[Ans: (a)]

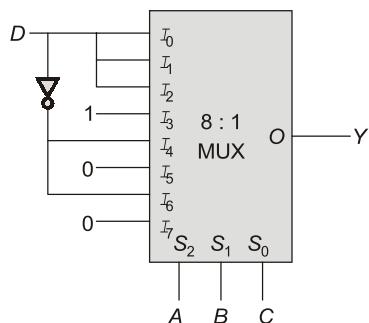
- T8. A 2-to-1 digital multiplexer having a switching delay of  $1 \mu s$  is connected as shown in the figure. The output of the multiplexer is tied to its own select input  $S$ . The input which gets selected when  $S = 0$  is tied to 1 and the input that gets selected when  $S = 1$  is tied to 0. The output  $V_0$  will be



- (a) 0  
 (b) 1  
 (c) Pulse train of frequency 0.5 MHz  
 (d) Pulse train of frequency 1.0 MHz

[Ans: (c)]

- T9. For the given multiplexer,  $Y$  is equal to



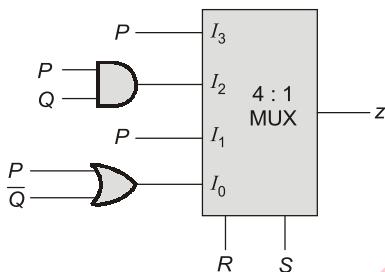
- (a)  $A\bar{C}\bar{D} + \bar{A}BC + \bar{A}\bar{D}$   
 (b)  $A\bar{B}\bar{C} + A\bar{C}\bar{D} + \bar{A}\bar{D}$   
 (c)  $\bar{A}\bar{B}\bar{C} + AC\bar{D} + \bar{A}\bar{D}$   
 (d)  $A\bar{C}\bar{D} + \bar{A}\bar{B}D + A\bar{D}$

[Ans: (a)]

- T10.** Without any additional circuitry, an 8 : 1 MUX can be used to obtain
- Some but not all Boolean functions of 3 variables
  - All functions of 3 variables but none of 4 variables
  - All functions of 3 variables and some but not all of 4 variables
  - All functions of 4 variables

[GATE-EC : 2003, Ans: (c)]

- T11.** For the circuit shown in the following figure,  $I_0 - I_3$  are inputs to the 4 : 1 multiplexer. R(MSB) and S are control bits.

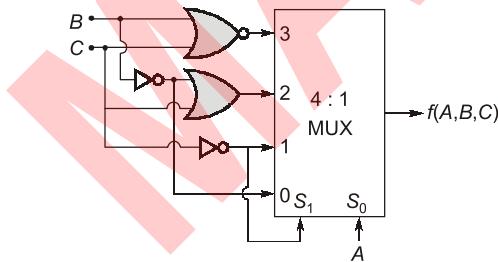


The output  $Z$  can be represented by

- $PQ + P\bar{Q}S + \bar{Q}RS$
- $P\bar{Q} + P\bar{Q}\bar{R} + \bar{P}\bar{Q}\bar{S}$
- $P\bar{Q}\bar{R} + \bar{P}QR + PQRS + \bar{Q}RS$
- $PQ\bar{R} + PQRS + P\bar{Q}\bar{R}S + \bar{Q}\bar{R}\bar{S}$

[GATE-2008, Ans: (a)]

- T12.** The Boolean function  $f(A, B, C)$  realised by the given 4 : 1 MUX, is



- $f(A, B, C) = AB + BC$
- $f(A, B, C) = \bar{A}\bar{B} + BC$
- $f(A, B, C) = AB + \bar{B}\bar{C}$
- $f(A, B, C) = \bar{A}\bar{B} + \bar{B}\bar{C}$

[Ans: (d)]

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**Statement for Linked Answer Question (T13 and T14):**

Two products are sold from a vending machine, which has two push buttons  $P_1$  and  $P_2$ . When a button is pressed, the price of the corresponding product is displayed in a 7-segment display.

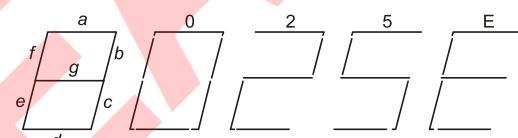
If no buttons are pressed, '0' is displayed, signifying 'Rs. 0'

If only  $P_1$  is pressed, '2' is displayed, signifying 'Rs.2'

If only  $P_2$  is pressed, '5' is displayed, signifying 'Rs.5'

If both  $P_1$  and  $P_2$  are pressed, 'E' is displayed, signifying 'Error'

The names of the segments in the 7-segment display, and the glow of the display for '0', '2', '5' and 'E' are shown below.



Consider:

- push button pressed/not pressed in equivalent to logic 1/0 respectively,
- a segment glowing/not glowing in the display is equivalent to logic 1/0 respectively

- T13.** If segments  $a$  to  $g$  are considered as functions of  $P_1$  and  $P_2$ , then which of the following is correct?

- $g = \bar{P}_1 + P_2, d = c + e$
- $g = P_1 + P_2, d = c + e$
- $g = \bar{P}_1 + P_2, e = b + c$
- $g = P_1 + P_2, e = b + c$

[Ans: (b)]

- T14.** What are the minimum numbers of NOT gates and 2-input OR gates required to design the logic of the driver for this 7-segment display?

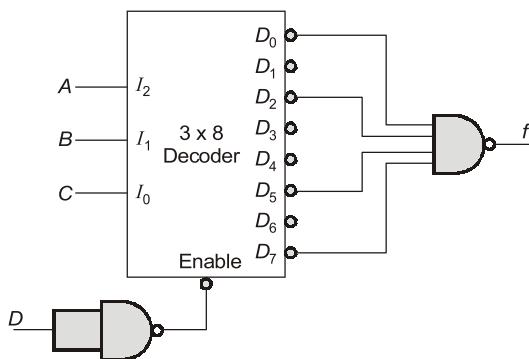
- 3 NOT and 4 OR
- 2 NOT and 4 OR
- 1 NOT and 3 OR
- 2 NOT and 3 OR

[Ans: (d)]

- T15. The number of 3-to-8 line decoders with an enable input are needed to construct a 6-to-64 line decoder without using any other logic gates are \_\_\_\_\_.

[Ans: (9)]

- T16. The logic function  $f(A, B, C, D)$  implemented by the circuit shown below is

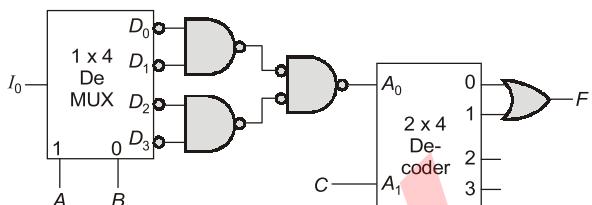


- (a)  $\bar{D}(A \oplus C)$   
 (b)  $D(A \odot C)$   
 (c)  $\bar{D}(A \oplus B)$   
 (d)  $D(A \odot B)$

[Ans: (b)]

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- T17. Consider the logic circuit given below:



The minimized expression for  $F$  is

- (a)  $\bar{C}$   
 (b)  $I_0$   
 (c)  $C$   
 (d)  $\bar{I}_0$

[Ans: (a)]

■ ■ ■ ■

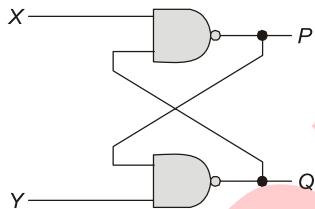
## 4

## Sequential Circuits



## Multiple Choice Questions

- Q.1** The following binary values were applied to the  $X$  and  $Y$  inputs of the NAND latch shown in the figure in the sequence indicated below:  
 $X = 0, Y = 1; X = 0, Y = 0; X = 1, Y = 1.$   
The corresponding stable  $P, Q$  outputs will be

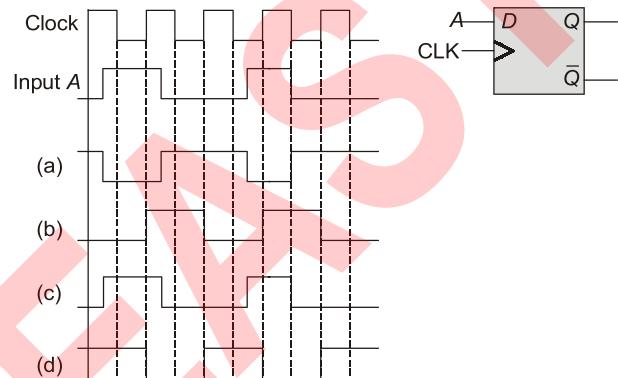


- (a)  $P = 1, Q = 0; P = 1, Q = 0; P = 1, Q = 0$  or  
 $P = 0, Q = 1$
  - (b)  $P = 1, Q = 0; P = 0, Q = 1$  or  $P = 0, Q = 1;$   
 $P = 0, Q = 1$
  - (c)  $P = 1, Q = 0; P = 1, Q = 1; P = 1, Q = 0$  or  
 $P = 0, Q = 1$
  - (d)  $P = 1, Q = 0; P = 1, Q = 1; P = 1, Q = 1$
- [GATE-2007]

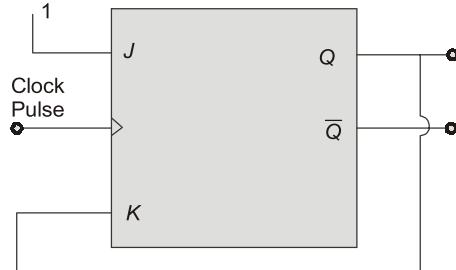
- Q.2** The output  $Q_n$  of a J-K flip-flop is zero. It changes to 1 when a clock pulse is applied. The input  $J_n$  a  $K_n$  are respectively ( $X$  represents don't care condition):
- |               |               |
|---------------|---------------|
| (a) 1 and $X$ | (b) 0 and $X$ |
| (c) $X$ and 0 | (d) $X$ and 1 |
- [ESE-2013]

- Q.3** The input  $A$  and clock applied to the  $D$  flip-flop are shown in figure below. The output  $Q$  is,

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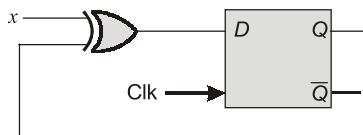


- Q.4** In figure, assume that initially  $Q = 1$ . With clock pulses being given, the subsequent states of  $Q$  will be



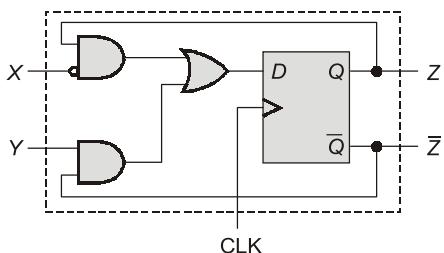
- (a) 1, 0, 1, 0, 1, 0, 1
- (b) 0, 0, 1, 0, 0, 1, 0....
- (c) 1, 1, 0, 1, 1, 0, 1
- (d) 0, 1, 0, 1, 0, 1, 0....

- Q.5** The circuit acts as



- (a) D-Flip Flop
- (b) T-Flip Flop
- (c) Both A and B
- (d) None

- Q.6** A sequential circuit using  $D$  flip-flop and logic gates is shown in figure where  $X$  and  $Y$  are the inputs and  $Z$  is the output. The circuit is



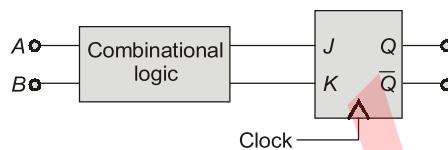
- (a) S-R FF with inputs  $X = R$  and  $Y = S$   
 (b) S-R FF with inputs  $X = S$  and  $Y = R$   
 (c) J-K FF with inputs  $X = J$  and  $Y = K$   
 (d) J-K FF with inputs  $X = K$  and  $Y = J$
- Q.7** The circuit realization of the combination logic block shown in figure to obtain the following truth table will be,

A	B	$Q_{n+1}$
0	0	$\bar{Q}_n$
0	1	1
1	0	$Q_n$
1	1	0



- (a)  $A \rightarrow \text{NOR gate} \rightarrow J$   
 (b)  $B \rightarrow \text{NOR gate} \rightarrow K$   
 (c)  $B \rightarrow \text{NOR gate} \rightarrow J$   
 (d)  $B \rightarrow \text{NOR gate} \rightarrow K$

- Q.8** To realize the given truth table from the circuit shown in the figure, the input to  $J$  in terms of  $A$  and  $B$  would have to be



Truth Table

A	B	$Q_{n+1}$
0	0	$Q_n$
0	1	1
1	0	$Q_n$
1	1	0

- (a)  $\bar{A}$       (b)  $B$   
 (c)  $\bar{AB}$       (d)  $\bar{A}\bar{B}$

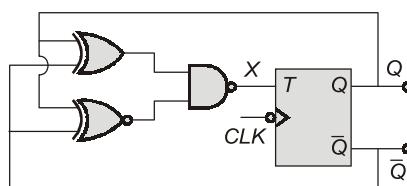
- Q.9** X-Y flip flop, whose Characteristic Table is given below is to be implement using a J-K flip flop

X	Y	$Q_{n+1}$
0	0	1
0	1	$\bar{Q}_n$
1	0	$Q_n$
1	1	0

This can be done by making

- (a)  $J = \bar{Y}, K = X$       (b)  $J = \bar{X}, K = Y$   
 (c)  $J = Y, K = \bar{X}$       (d)  $J = X, K = \bar{Y}$

- Q.10** The clock frequency applied to the digital circuit shown in figure below is 1 kHz. If the initial state of the output  $Q$  of the flip-flop is '0', then the frequency of the output waveform  $Q$  in kHz is



- (a) 0.25      (b) 0.5  
 (c) 1      (d) 2

[GATE-2013]

**Q.11** Match List-I with List-II and select the correct answer using the codes given below the lists:

**List-I**

- A. Shift register
- B. Counter
- C. Decoder

**List-II**

1. Frequency division
2. Addressing in memory chips
3. Serial to parallel data conversion

**Codes:**

A	B	C
(a) 3	2	1
(b) 1	2	2
(c) 2	1	3
(d) 3	1	2

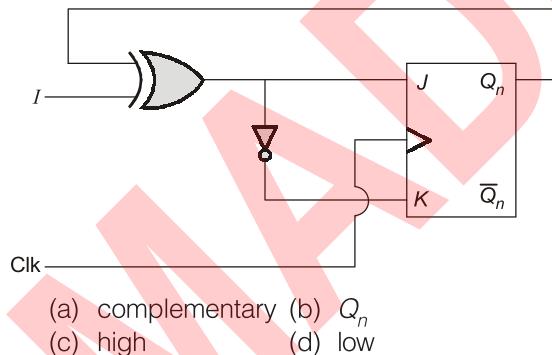
[EC : GATE-2004]

**Q.12** Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature?

- (a) Asynchronous operation
- (b) Low input voltage
- (c) Gate impedance
- (d) Cross coupling

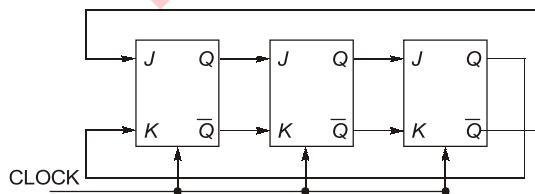
[ESE-2013]

**Q.13** If  $I$  is set high in circuit given below then  $Q_{n+1}$  is



- (a) complementary
- (b)  $Q_n$
- (c) high
- (d) low

**Q.14** For the initial state of 000, the function performed by the arrangement of the J-K flip flops in the figure

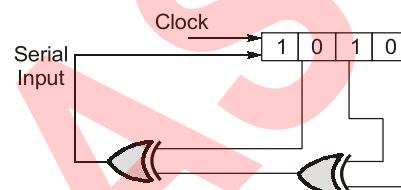


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- (a) Shift Register
- (b) Mod-3 counter
- (c) Mod-6 counter
- (d) Mod-2 counter

[EC : GATE-1993]

**Q.15** The shift register shown in the given figure is initially loaded with the bit pattern 1010. Subsequently the shift register is clocked, and with each clock pulse the pattern gets shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (msb). After how many clock pulses will the content of the shift register become 1010 again?



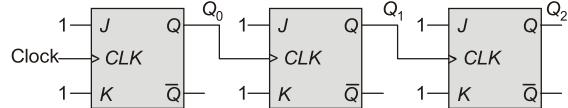
- (a) 4
- (b) 5
- (c) 6
- (d) 7

**Q.16** The number of unused states in a 4-bit Johnson counter is

- (a) 2
- (b) 4
- (c) 8
- (d) 12

[ESE-2003]

**Q.17** The figure below shows a 3-bit ripple counter, with  $Q_2$  as the MSB. The flip-flops are rising-edge triggered. The counting direction is

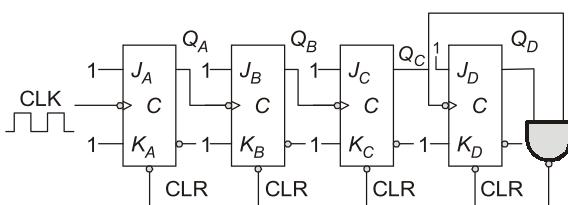


- (a) always down
- (b) always up
- (c) up or down depending on the initial state of  $Q_0$  only
- (d) up or down depending on the initial states of  $Q_2$ ,  $Q_1$  and  $Q_0$

[GATE-IN: 2009]

**Common Data for Questions (18 and 19):**

A counter is shown below:



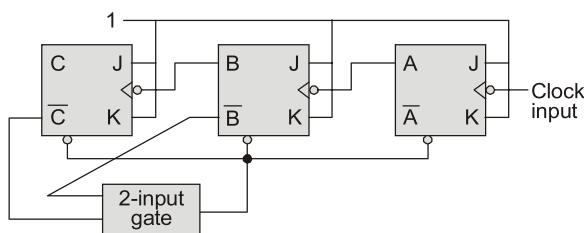
**Q.18** The counter shown is

- (a) Mod-12
- (b) Mod-9
- (c) Mod-14
- (d) None of these

**Q.19** Frequency of output  $Q_D$  for 1 MHz clock is

- (a) 63.3 kHz
- (b) 83.3 kHz
- (c) 73.3 kHz
- (d) None of these

**Q.20** In the modulo-6 ripple counter shown in the figure, the output of the 2-input gate is used to clear the J-K flip-flops.

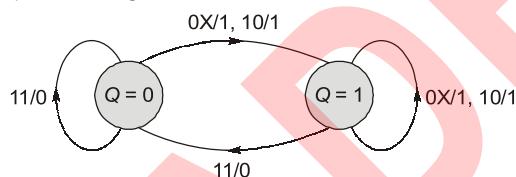


The 2-input gate is

- (a) a NAND gate
- (b) a NOR gate
- (c) an OR gate
- (d) an AND gate

[GATE-2004]

**Q.21** A state diagram of a logic which exhibits a delay in the output is shown in the figure, where X is the do not care condition, and Q is the output representing the state.

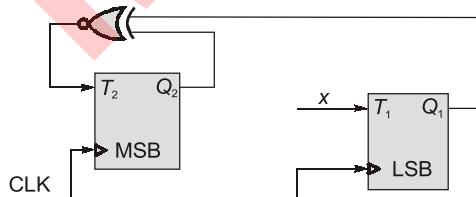


The logic gate represented by the state diagram is

- (a) XOR
- (b) OR
- (c) AND
- (d) NAND

[GATE-2014]

**Q.22** Consider the partial implementation of a 2-bit counter using T flip-flops following the sequence 0-2-3-1-0, as shown below



To complete the circuit, the input X should be

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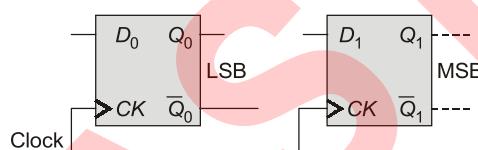
- (a)  $Q_2'$
- (b)  $Q_2 + Q_1$
- (c)  $(Q_1 \oplus Q_2)'$
- (d)  $Q_1 \oplus Q_2$

[GATE-2004]

**Q.23** Two D-flip flops, as shown below are to be connected as a synchronous counter that goes through the following  $Q_1 Q_0$  sequence

$$00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00 \dots$$

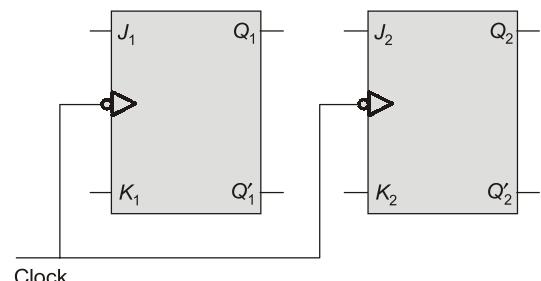
The inputs  $D_0$  and  $D_1$  respectively should be connected as



- (a)  $\overline{Q_1} \overline{Q_0}$  and  $Q_1 Q_0$
- (b)  $\overline{Q_0}$  and  $Q_1$
- (c)  $\overline{Q_1} Q_0$  and  $\overline{Q_1} Q_0$
- (d)  $\overline{Q_1}$  and  $Q_0$

[EC : GATE-2006]

**Q.24** A synchronous counter using two J-K flip-flops that goes through the sequence of states:  $Q_1 Q_2 = 00 \rightarrow 10 \rightarrow 01 \rightarrow 11 \rightarrow 00 \dots$  is required. To achieve this, the inputs to the flip flops are:



- (a)  $J_1 = Q_2, K_1 = 0; J_2 = Q'_1, K_2 = Q_1$
- (b)  $J_1 = 1, K_1 = 1; J_2 = Q_1, K_2 = Q_1$
- (c)  $J_1 = Q_2, K_1 = Q'_2; J_2 = 1, K_2 = 1$
- (d)  $J_1 = Q'_2, K_1 = Q_2, J_2 = Q_1, K_2 = Q'_1$

[GATE-2016]

**Q.25** The next state table of a 2-bit saturating up-counter is given below.

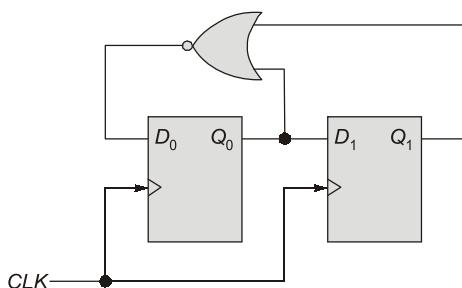
$Q_1$	$Q_0$	$Q_1^+$	$Q_0^+$
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

The counter is built as a synchronous sequential circuit using T flip-flops. The expressions for  $T_1$  and  $T_0$  are

- (a)  $T_1 = Q_1 Q_0$ ,  $T_0 = \bar{Q}_1 \bar{Q}_0$
- (b)  $T_1 = \bar{Q}_1 Q_0$ ,  $T_0 = \bar{Q}_1 + \bar{Q}_0$
- (c)  $T_1 = Q_1 + Q_0$ ,  $T_0 = \bar{Q}_1 + \bar{Q}_0$
- (d)  $T_1 = \bar{Q}_1 Q_0$ ,  $T_0 = Q_1 + Q_0$

[GATE-2017]

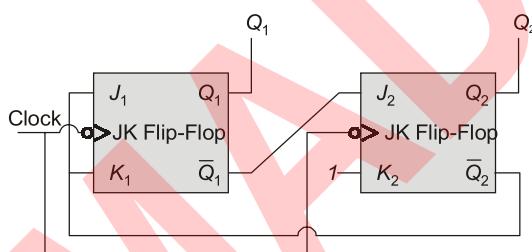
**Q.26** For the circuit shown, the counter state ( $Q_1 Q_0$ ) follows the sequence



- (a) 00, 01, 10, 11, 00 ...
- (b) 00, 01, 10, 00, 01 ...
- (c) 00, 01, 11, 00, 01 ...
- (d) 00, 10, 11, 00, 10 ...

[GATE-2007]

**Q.27** What are the counting states ( $Q_1, Q_2$ ) for the counter shown in the figure below?



- (a) 01, 10, 11, 00, 01... (b) 11, 10, 00, 11, 10...
- (c) 00, 11, 01, 10, 00... (d) 01, 10, 00, 01, 10...

[EC GATE-2009]

**Q.28** The output of Moore sequential machine is a function of

- (a) all present states of machine
- (b) all inputs
- (c) all combination of inputs and present state
- (d) few combination of inputs and present state

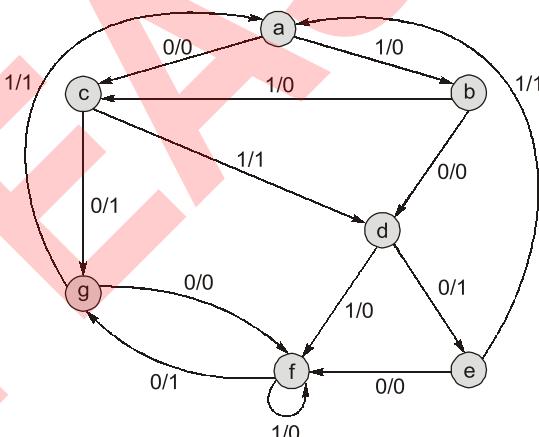
**Q.29**

Synchronous counters eliminate the delay problems encountered with asynchronous (ripple) counter because the

- (a) input clock pulses are applied only to the first and the last stages
- (b) input clock pulses are applied only to the last stage
- (c) input clock pulses are not used to activate any of the counter stages
- (d) input clock pulses are applied simultaneously

[ESE-2013]

**Q.30** Following state diagram shows clocked sequential circuit:



How many minimum number of states the sequential circuit has?

- (a) 6
- (b) 7
- (c) 5
- (d) 4

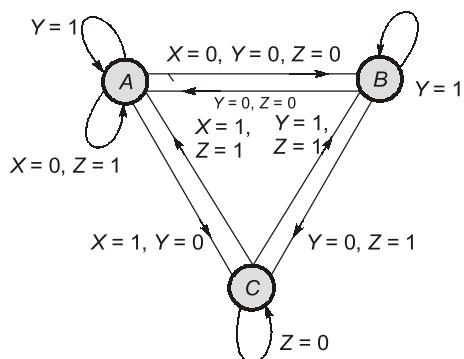
**Q.31** A 4 bit ripple counter and a 4 bit synchronous counter are made using flip flops having a propagation delay of 10 ns each. If the worst case delay in the ripple counter and the synchronous counter be R and S respectively, then

- (a)  $R = 10 \text{ ns}$ ,  $S = 40 \text{ ns}$
- (b)  $R = 40 \text{ ns}$ ,  $S = 10 \text{ ns}$
- (c)  $R = 10 \text{ ns}$ ,  $S = 30 \text{ ns}$
- (d)  $R = 30 \text{ ns}$ ,  $S = 10 \text{ ns}$

[GATE-2003]

**Q.32** The state transition diagram for a finite state machine with states  $A$ ,  $B$  and  $C$ , and binary inputs  $X$ ,  $Y$  and  $Z$ , is shown in the figure.

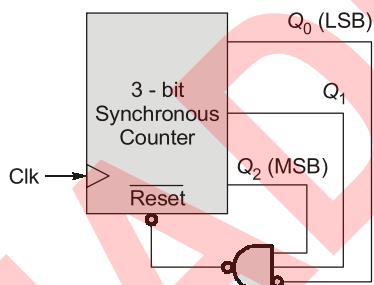
Which one of the following statements is correct?



- (a) Transitions from State A are ambiguously defined.
- (b) Transitions from State B are ambiguously defined.
- (c) Transitions from State C are ambiguously defined.
- (d) All of the state transitions are defined unambiguously.

[GATE-2016]

**Q.33** For the circuit shown in the figure, the delay of the bubbled NAND gate is 2 ns and that of the counter is assumed to be zero.



If the clock (Clk) frequency is 1 GHz, then the counter behaves as a

- (a) mod-5 counter (b) mod-6 counter
- (c) mod-7 counter (d) mod-8 counter

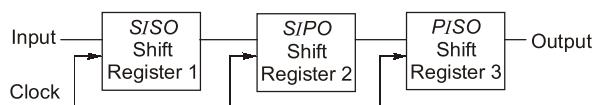
[GATE-2016]

2  
3  
6  
9

### Numerical Answer Type Questions

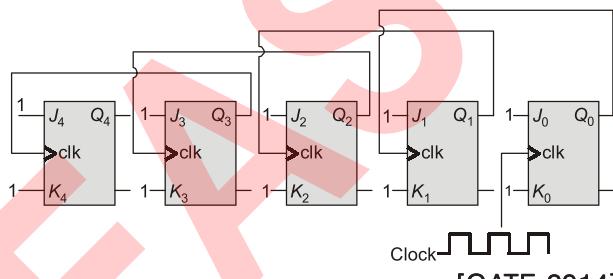
**Q.34** Three 4 bit shift registers are connected in cascade as shown in figure below. Each register is applied with a common clock pulse.

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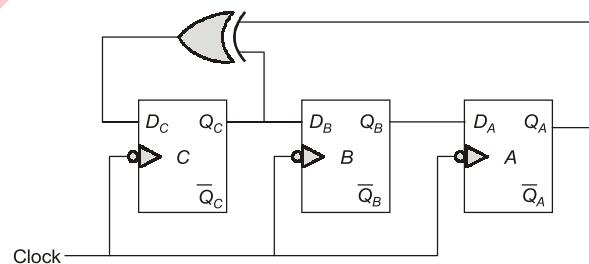
A 4 bit data 1011 is applied to the shift register 1. The minimum number of clock pulses required to get same input data at the output are \_\_\_\_\_.

**Q.35** Five JK flip-flops are cascaded to form the circuit shown in Figure. Clock pulses at a frequency of 1 MHz are applied as shown. The frequency (in kHz) of the waveform at  $Q_3$  is \_\_\_\_\_.



[GATE-2014]

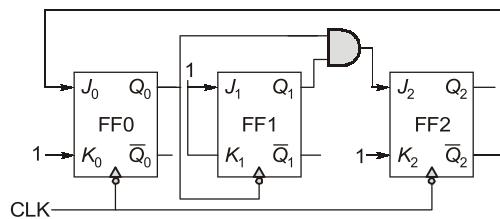
**Q.36** A digital circuit is designed with three D-flip flops and an Ex-OR gate as shown in below figure. If the initial value of  $Q_A Q_B Q_C$  was 110 then the minimum number of clock pulses required to get  $Q_A Q_B Q_C$  as 011 is \_\_\_\_\_.



**Q.37** A certain J-K FF has  $t_{pd}$  12 ns. The largest MOD counter that can be constructed from such FF's and still operate up to 10 MHz is \_\_\_\_\_.

[ISRO]

**Q.38** A counter circuit is shown in below figure:



If the propagation delay of flip-flops and AND gate are 2 ns and 1 ns respectively, what is the maximum clock rate possible to apply so that counter will operate satisfactorily in MHz?

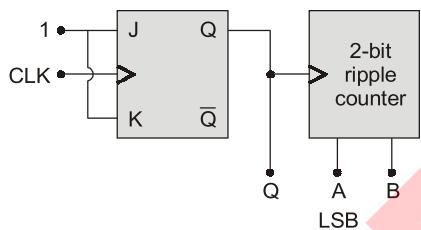
**Common Data for Questions (39 and 40):**

A Mealy system produces a 1 output if the input has been 0 for at least two consecutive clocks followed immediately by two or more consecutive 1's.

**Q.39** The minimum number of states for this system is \_\_\_\_\_.

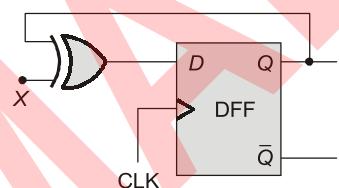
**Q.40** The flip-flops required to implement this system are \_\_\_\_\_.

**Q.41** In figure shown in below Q = A = B = 0. After 3 clock pulses Q, A and B are respectively



## Multiple Select Questions

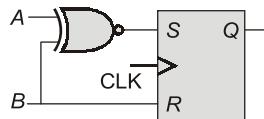
**Q.42** The given logic circuit is



- (a) A T-flip flop if  $X = T$
  - (b) Dividing the input clock frequency by 2 if  $X = 0$ .
  - (c) Dividing the input clock frequency by 2 if  $X = 1$ .
  - (d) Having characteristic equation as  $X \oplus Q_n$ .

**Q.43** An AB flip-flop is constructed from an SR flip-flop as shown in figure. The expression for next state  $Q^+$  is

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- (a)  $\bar{A}\bar{B} + A\bar{Q}$       (b)  $\bar{A}\bar{B} + \bar{B}Q$   
 (c)  $A \oplus B$       (d)  $A \odot B$

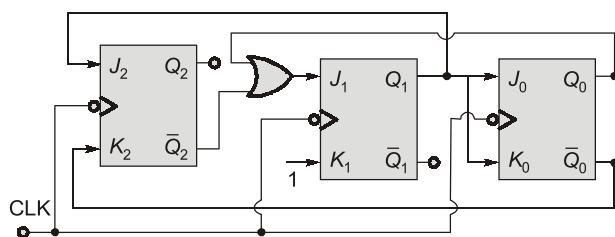
**Q.44** A shift register can be used

- (a) As serial to parallel data converter.
  - (b) As parallel to serial data converter.
  - (c) As a ring counter if  $Q_0$  is connected as serial input.
  - (d) As a Johnson counter if  $\bar{Q}_0$  is connected as serial input.

**Q.45** In a ripple counter

- (a) If D flip-flops are used, all flip flops D input must be connected to 1,
  - (b) If J-K flip-flops are used, all flip-flops J input must be connected to 0 and K input must be connected to 1.
  - (c) If T flip-flops are used, all flip-flops T input must be connected to 1.
  - (d) If J-K flip-flops are used, all flip-flop J and K inputs must be connected to 1.

**Q.46** In the given counter circuit each flip-flop is having propagation delay of 4 nano sec and OR gate is having propagation delay of 1 nano sec



- (a) The counter switching sequence is  

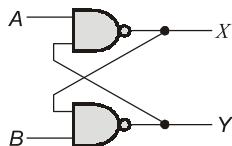
  - (b) The counter switching sequence is  

  - (c) The maximum clock frequency possible to apply to the counter is 250 MHz.
  - (d) The maximum clock frequency possible to apply to the counter is 200 MHz.



## Try Yourself

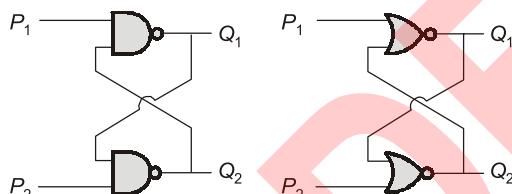
- T1.** In figure initially  $A = 1$  and  $B = 1$ , the input  $B$  is now replaced by a sequence  $1\ 0\ 1\ 0\ 1\ 0\dots$  the outputs  $X$  and  $Y$  will be



- (a) Fixed at 0 and 1 respectively
- (b) Fixed at 1 and 0, respectively
- (c)  $X = 1\ 0\ 1\ 0\dots$  while  $Y = 1\ 0\ 1\ 0\dots$
- (d)  $X = 1\ 0\ 1\ 0\dots$  while  $Y = 0\ 1\ 0\ 1\dots$

[Ans: (a)]

- T2.** Refer to the NAND and NOR latches shown in the figure. The inputs ( $P_1, P_2$ ) for both the latches are first made (0, 1) and then after a few seconds, made (1, 1). The corresponding stable outputs ( $Q_1, Q_2$ ) are



- (a) NAND: first (0, 1) then (0, 1) NOR: first (1, 0) then (0, 0)
- (b) NAND: first (1, 0) then (1, 0) NOR: first (1, 0) then (0, 0)
- (c) NAND: first (1, 0) then (1, 1) NOR: first (0, 1) then (0, 1)
- (d) NAND: first (1, 0) then (1, 0) NOR: first (0, 1) then (0, 0)

[EC : GATE-2009, Ans: (b)]

- T3.** A new flip-flop is having behaviour as described below. It has two inputs  $X$  and  $Y$  and when both inputs are same and they are 1,1, the flip-flop is going to set else flip-flop resets. If both inputs are different and they are 0, 1, flip-flop complements itself otherwise it is going to retain the last state. Which of the following expression

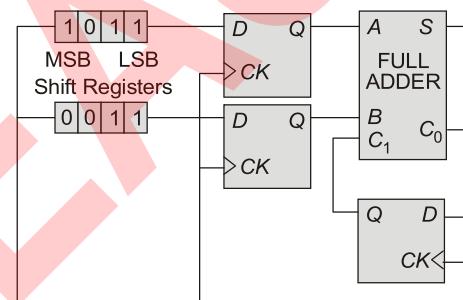
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is the characteristic expression for the new flip flop?

- (a)  $XQ + Y\bar{Q}$
- (b)  $X\bar{Q} + YQ$
- (c)  $X\bar{Q} + Y\bar{Q}$
- (d) None of these

[Ans: (a)]

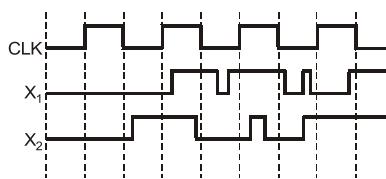
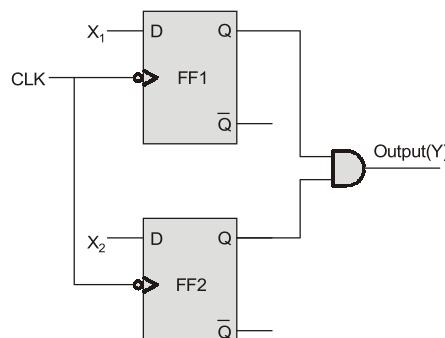
- T4.** For the circuit shown in the figure below, two 4-bit parallel-in-serial-out shift registers loaded with the data shown are used to feed the data to a full adder. Initially, all the flip-flops are in the clear state. After applying two clock pulses, the outputs of the full adder should be



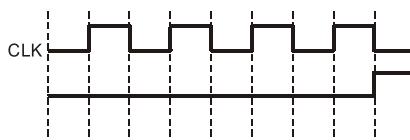
- (a)  $S = 0 \quad C_0 = 1$
- (b)  $S = 0 \quad C_0 = 0$
- (c)  $S = 1 \quad C_0 = 1$
- (d)  $S = 1 \quad C_0 = 0$

[EC GATE-2006, Ans. (c)]

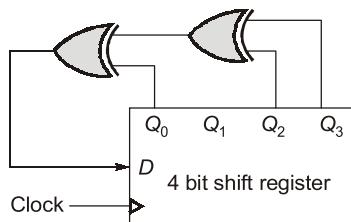
- T5.** Consider the flip-flop circuit diagram shown below. Draw output waveform for the circuit.



[Ans.]



- T6. A 4 bit right shift, shift register is shifting the data to the right for every clock pulse. The serial input  $D$  is derived by using Ex-OR gates as shown in the figure. After three clock pulses the content in the shift register is to be 1010 at  $Q_0 Q_1 Q_2 Q_3$ , what will be the initial content of the register.

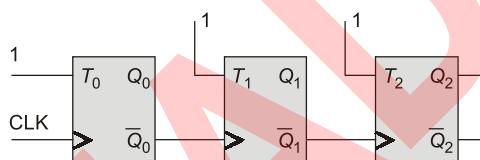


- (a) 1100      (b) 1010  
(c) 0011      (d) 0101

[Ans: (c)]

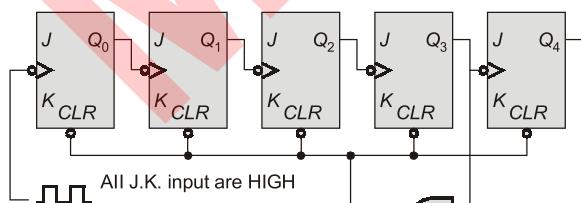
- T7. The given figure shows a ripple counter using positive edge triggered flip-flops.

If the present state of the counter is  $Q_2 Q_1 Q_0 = 011$ , then its next state ( $Q_2 Q_1 Q_0$ ) will be \_\_\_\_\_.



[GATE-2005, Ans: (100)]

- T8. The mod-number of the asynchronous counter shown in figure



- (a) 24      (b) 48  
(c) 25      (d) 36

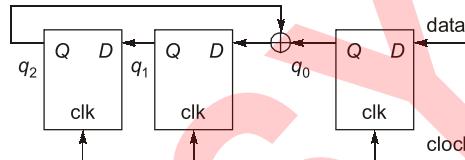
[Ans: (a)]

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- T9. Consider a mod-1000 ripple up counter. The duty cycle for its MSB is \_\_\_\_\_ %.

[Ans: (48.8)]

- T10. Consider the circuit in the diagram. The  $\oplus$  operator represents Ex-OR. The D flip-flops are initialized to zeroes (cleared).



The following data : 100110000 is supplied to the "data" terminal in nine clock cycles. After that the values of  $q_2 q_1 q_0$  are

- (a) 000      (b) 001  
(c) 010      (d) 101

[GATE-2006, Ans: (c)]

- T11. How many pulses are needed to change the contents of a 8-bit up-counter from 10101100 to 00100111 (right most bit is the LSB)?

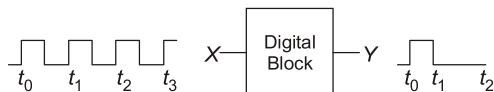
[IT GATE-2005, Ans: (123)]

- T12. If a counter having 10 FF's is initially at 0, what count will it hold after 2060 pulses?

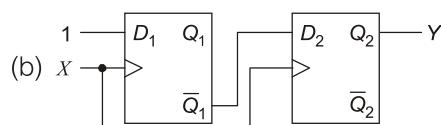
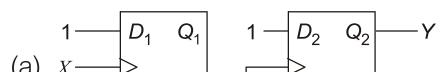
- (a) 000 000 1100      (b) 000 001 1100  
(c) 000 001 1000      (d) 000 000 1110

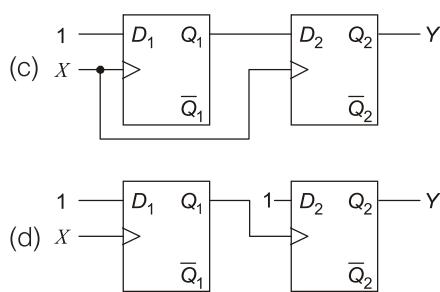
[Ans: (a)]

- T13. The digital block in figure realized using two positive edge triggered D flip-flop. Assume that for  $t < t_0$ ,  $Q_1 = Q_2 = 0$ .



The circuit in the digital block is given by





[Ans: (b)]

- T14.** Consider the following state transition table with two state variables  $A$  and  $B$  and the input variable  $x$  and the output variable  $y$

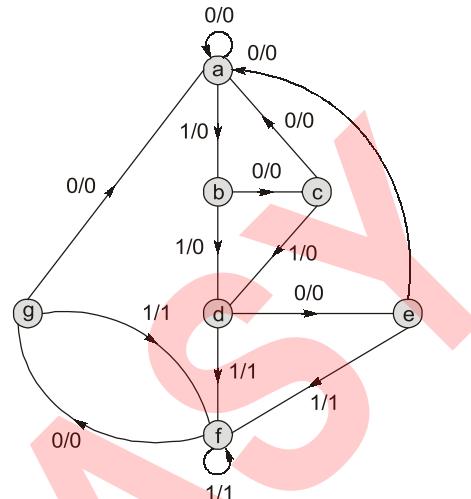
Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1

If the initial state is  $A = 0$  and  $B = 0$ , what is the minimum length of an input string which will take the machine to the state  $A = 1$  and  $B = 1$  with output  $y = 1$ ?



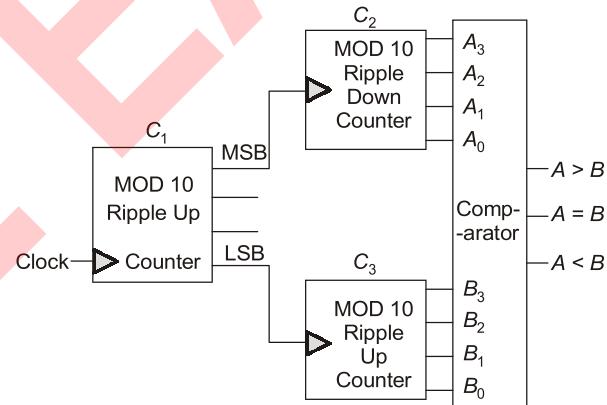
[DRDO-2009, Ans: (b)]

T15. Reduce the following state diagram and also write the reduced state table.



[Ans: (5)]

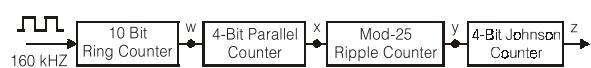
- T16.** Consider the circuit given below:



MSB and LSB of MOD 10 ripple up counter acts as clock to 4 bit ripple down and up counter respectively. Initially all the counter were cleared and output of comparator was  $A = B$ . The clock pulse is applied. Find the minimum number of clock pulses required to make  $A = B$  again.

[Ans: 17]

- T17.** The frequency of the pulse at z in the network shown in figure is      Hz



[Ans: (5)]

