

Compal Confidential Schematic Document

Intel Braswell M
LA-E372P
Kefka and Sabin

2016-07-28 Rev: 0.2

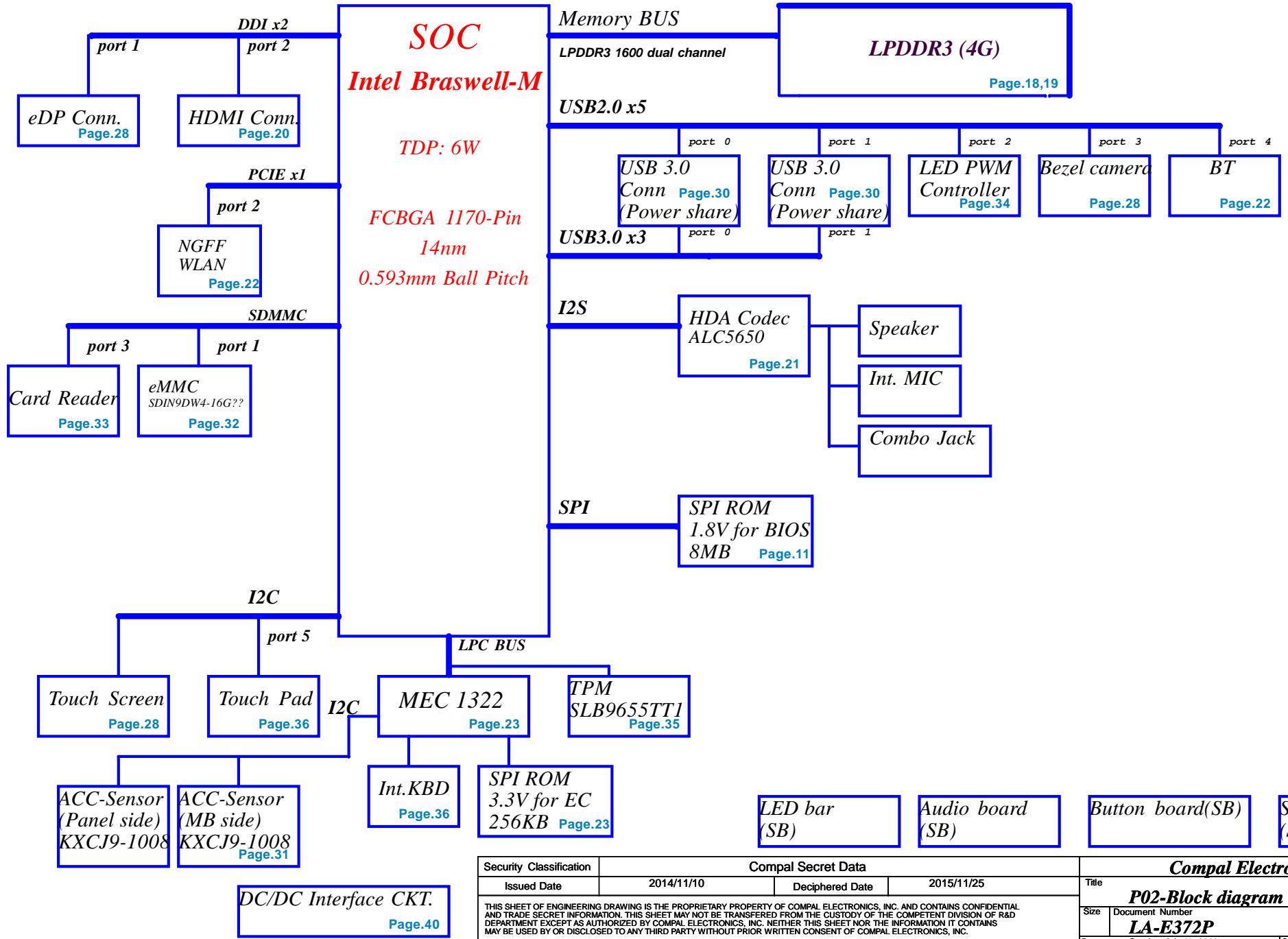
ZZZ1 PCB.CAV01@

PCB 1X2 LA-E372P REV0 M/B CHROME 4
DA6001OL000
Vinafix.com

ZZZ1 PCB.CAV11@

PCB 1X2 LA-E372P REV0 M/B CHROME 2
DA6001OL100

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Issued Date	2014/11/10	Deciphered Date	2015/11/25	P01-Cover Page
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Size	Document Number		Rev	0.2
Custom	LA-E372P		Date	Friday, July 29, 2016
			Sheet	1 of 47



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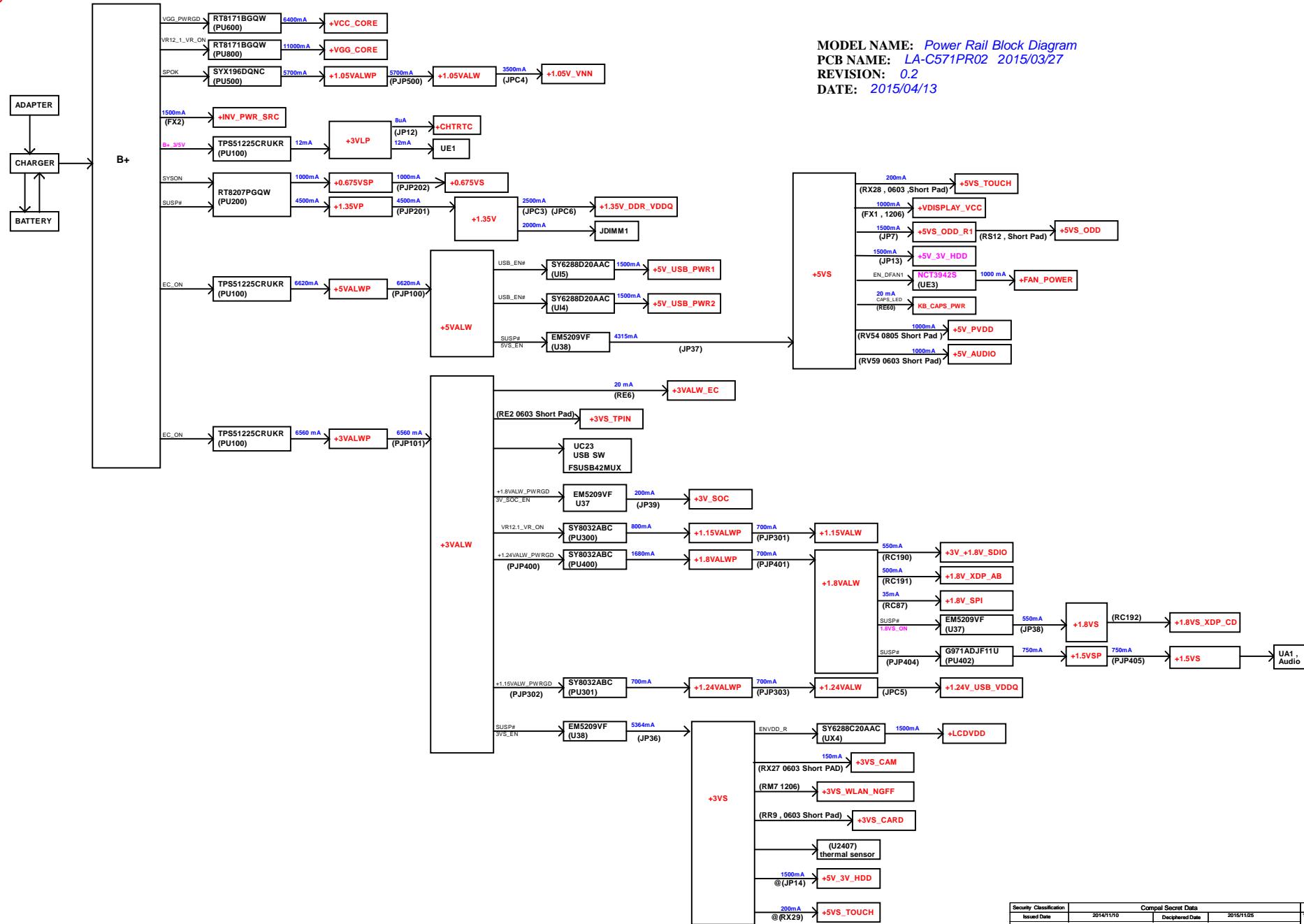
Compal Electronics, Inc.

P02-Block diagram

Number
E332D

Re
d

TBD



MODEL NAME: Power Rail Block Diagram
PCB NAME: LA-C571PR02 2015/03/27
REVISION: 0.2
DATE: 2015/04/13

Security Classification	Compaq Secret Data			Compaq Electronics, Inc.	
Issued Date	2014/11/10	Declassified Date	2015/11/25	Title	P03-DB block diagram
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Spec	Document Number	Rev			
	E-LA-372P	0.2			
Date	Wednesday, July 27, 2016	Sheet	3	of	47

Voltage Rails *TBD*

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.05VALW	+1.05v Always power rail	ON	ON	ON
+1.24VALW	+1.24v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+3V_SOC	+3V_SOC Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+VCC_CORE	Core voltage for SOC	ON	OFF	OFF
+VGG_CORE	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.15VALW	+1.15VALW system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

43 level BOM table *TBD*

43 Level	Description	BOM Structure
4319Y031L01	MB AC571 AAL14 BSW U PEN HDMI	EMI@/ESD@/XDP@/LPC33@/PCB@/ODD@/SOC@/601@/N601@/PARADE@
4319Y031L02	MB AC571 AAL14 BSW U CEL HDMI	EMI@/ESD@/XDP@/LPC33@/PCB@/ODD@/SOC1@/601@/N601@/PARADE@

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Board ID / SKU ID Table for AD channel *TBD*

Board ID / CRC ID Table

Vcc	3.3V +/- 1%	Ra	100K +/- 1%				
Board ID	Rb	VAD_BID_min	VAD_BID_TYP	VAD_BID_max	EC	AD3	
0	0	0.000V	0.000V	0.300V	0x00	- 0x0B	
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C	- 0x1C	
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D	- 0x26	
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27	- 0x30	
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31	- 0x3B	
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C	- 0x46	
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47	- 0x54	
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55	- 0x64	
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65	- 0x76	
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77	- 0x87	
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88	- 0x96	
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97	- 0xA3	
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4	- 0xAD	
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAB	- 0xB7	
14	270K +/- 1%	2.395V	2.408V	2.421V	0xBB	- 0xC0	
15	330K +/- 1%	2.521V	2.533V	2.544V	0xCC1	- 0xC9	
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA	- 0xD3	
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4	- 0xDC	
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD	- 0xE6	
19	NC	3.000V	3.300V	3.300V	0xE7	- 0xFF	

BOARD ID Table

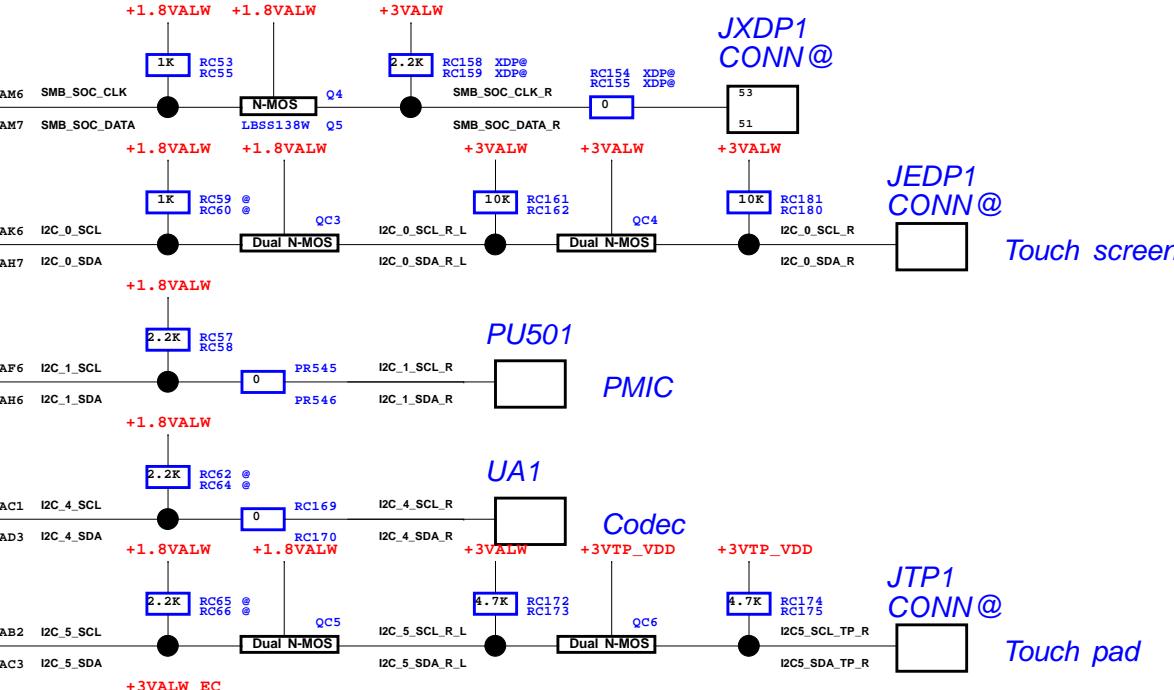
TBD

TBD BOM Option Table

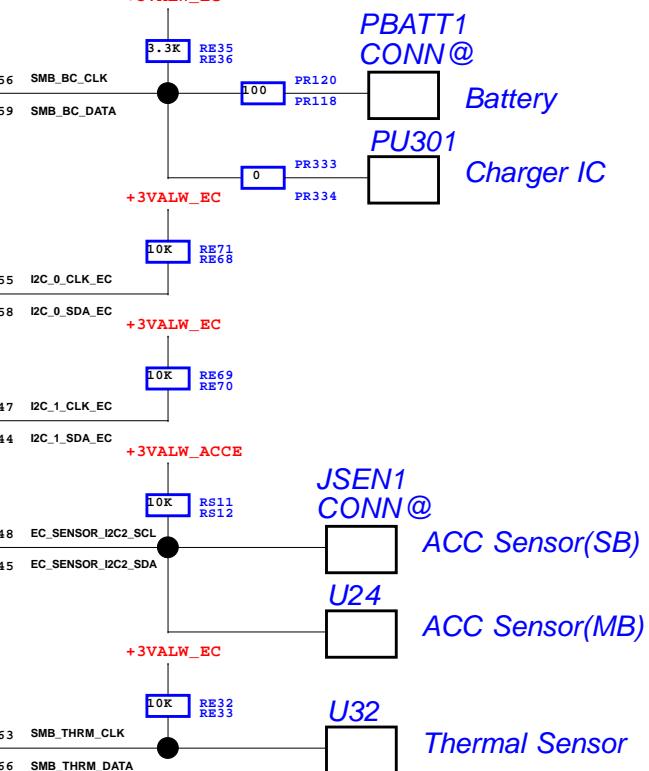
Item	BOM Structure
Unpop	@
Connector	CONN@
XDP (Debug Port)	XDP@
EMC requirement	EMI@
EMC requirement unpop	NEMI@
LPC18	LPC18@
LPC33	LPC33@
Rvs. RF requirement	RF@
ESD requirement	ESD@
XDP (Debug Port) unpop	NXDP@
ESD requirement unpop	NESD@
For JUMP	JP@
For PCB	PCB@
For CPU	SOC@ SOC1@
SATA re-Driver	601@
Test Point	TP@

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SOC
BSW



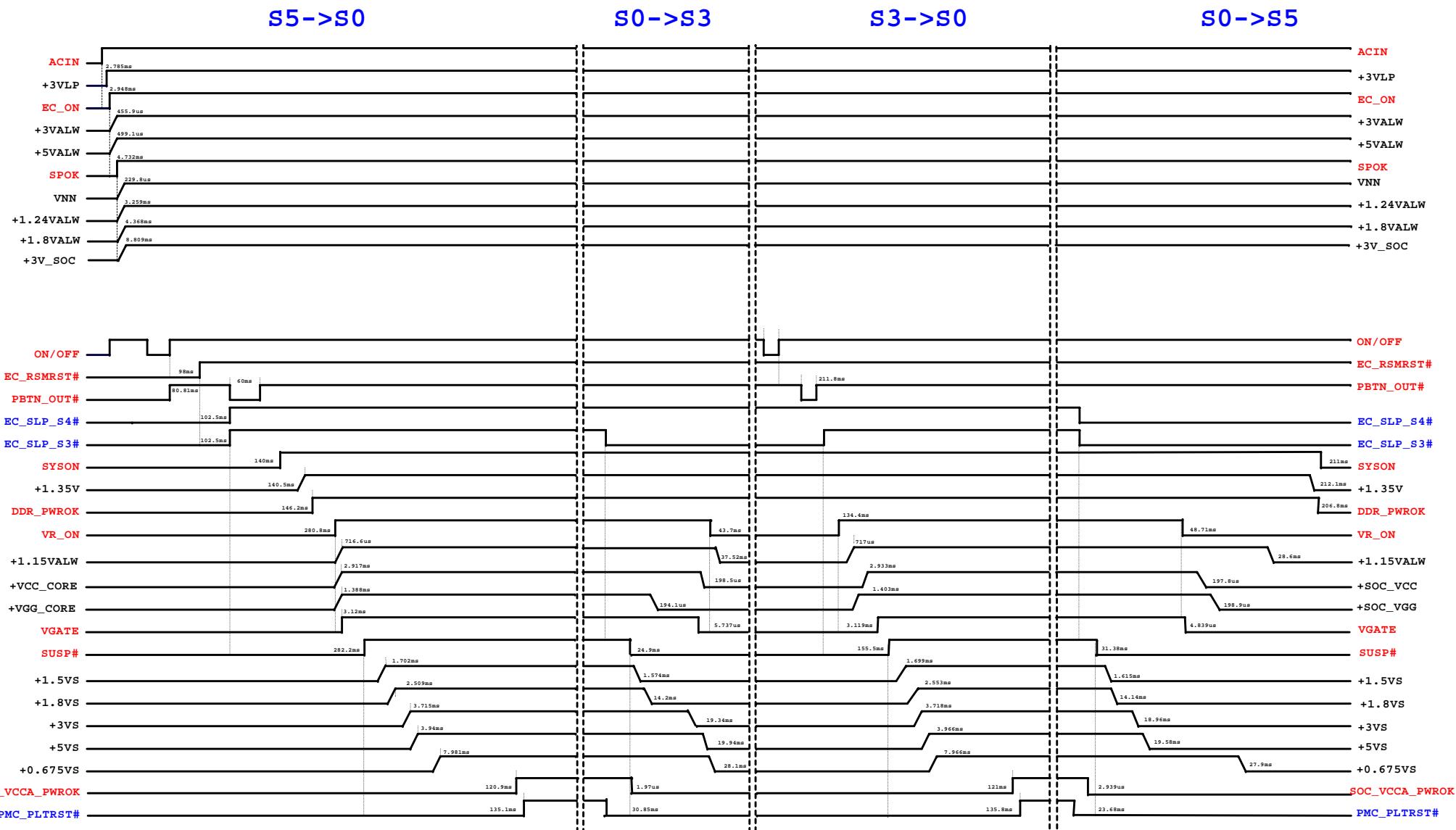
KBC
MEC1322



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MODEL NAME: *SMbus Block Diagram*
PCB NAME: *LA-E372 PR02 2016/06/20*
REVISION: *0.2*
DATE: *2016/06/20*

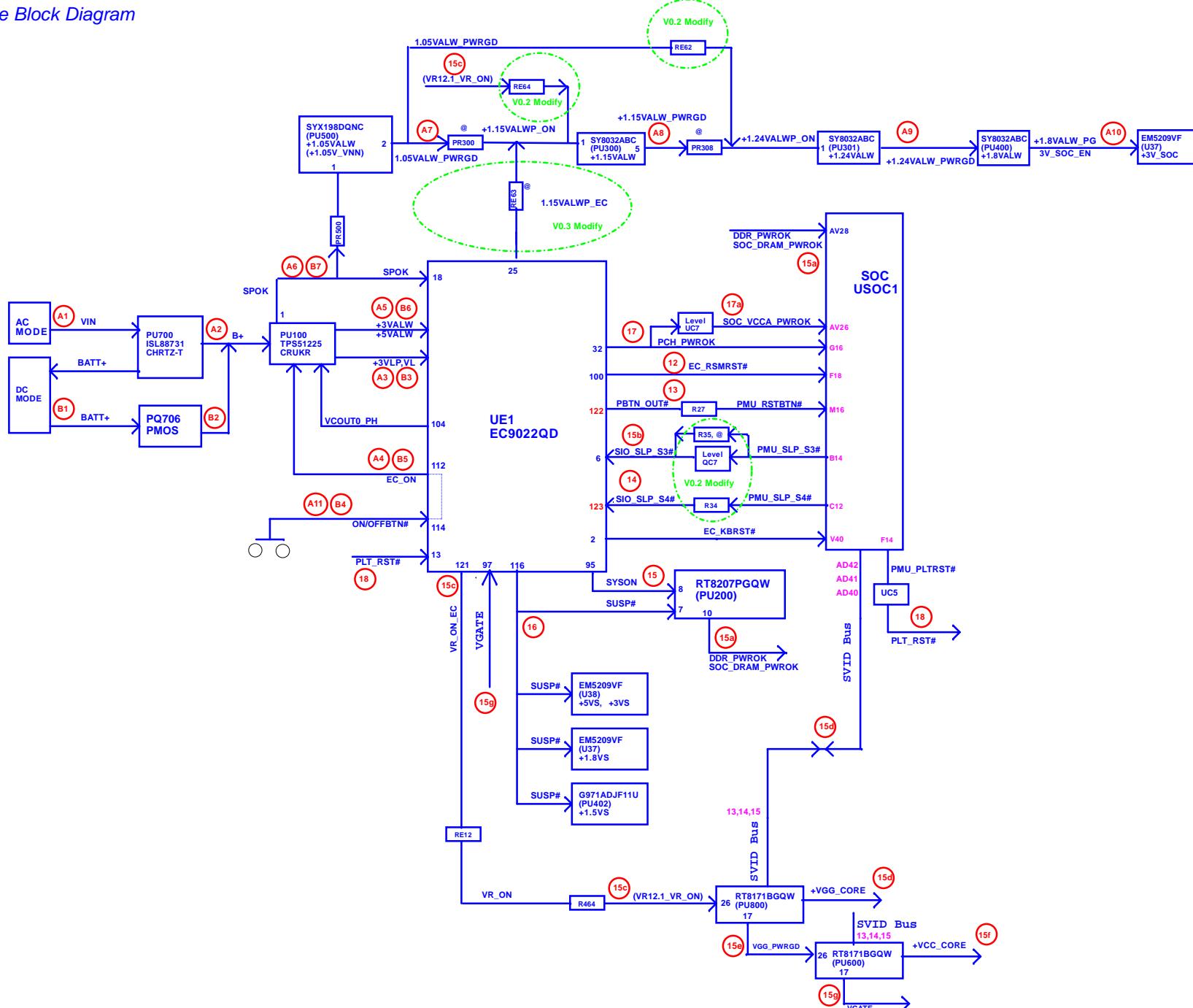
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Issued Date	2014/11/10	Deciphered Date	2015/11/25		P05-SMBus block diagram	
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					LA-E372P	0.
Date:	Sunday, July 17, 2016	Sheet	5	of	47	



MODEL NAME: *Power Sequence Block Diagram*

PCB NAME: ?

REVISION RATE 8



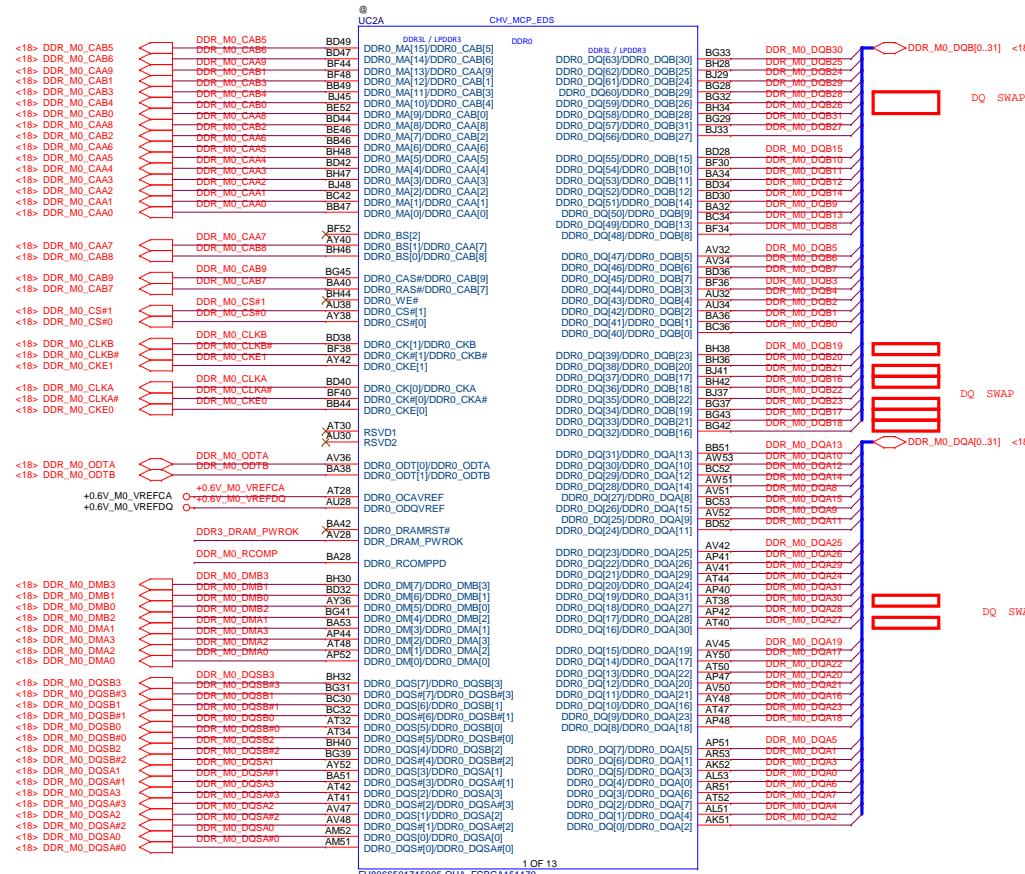
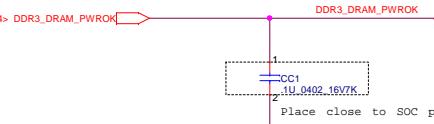
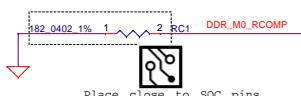
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Size	Document Number	Rev			
Custom	LA-E372P	0.2			
Date:	Sunday, July 17, 2016	Sheet	7	of	47

Main Func = CPU

Modify : LPDDR3 RAM



S IC FH8066501715929 SR2KN D1 1.6G FCBGA151170 A31!
Part Number = SA0009U1L

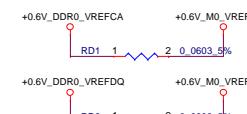


1 OF 13

FH8066501715905_QHA_FCBGA151170

LPDDR3 Bit and Byte Lane Swapping Guidelines

- Data strobe (DQS) swapping and data mask swapping are not allowed. For all Byte lanes, DM[n] must be mapped together with corresponding RD Byte[n] and DQS/DQS#[n].
- Byte lane swapping for LPDDR3 within same DRAM is allowed, **except the lowest two bytes in each DRAM (DQ7:0, DQ15:8)**. Remaining byte lanes can be swapped within the same DRAM. If swapping is used, DQ signals within a channel must match its associated DQS/DQS# and DM signals.
- Data bit swapping within a byte lane in the same channel is allowed, **except in the lowest two bytes in each DRAM**.

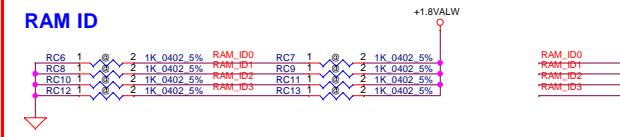
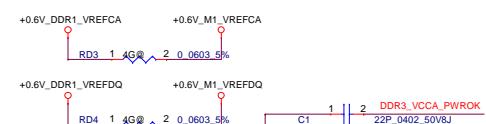


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Issued Date	Deciphered Date				Title	P08-BSW(1/8) DDR3L-CH0
2014/11/10	2015/11/25				Size	Document Number LA-E372P
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Date: Sunday, July 17, 2016 Sheet 8 of 47

Main Func = CPU



HYNIX 4G

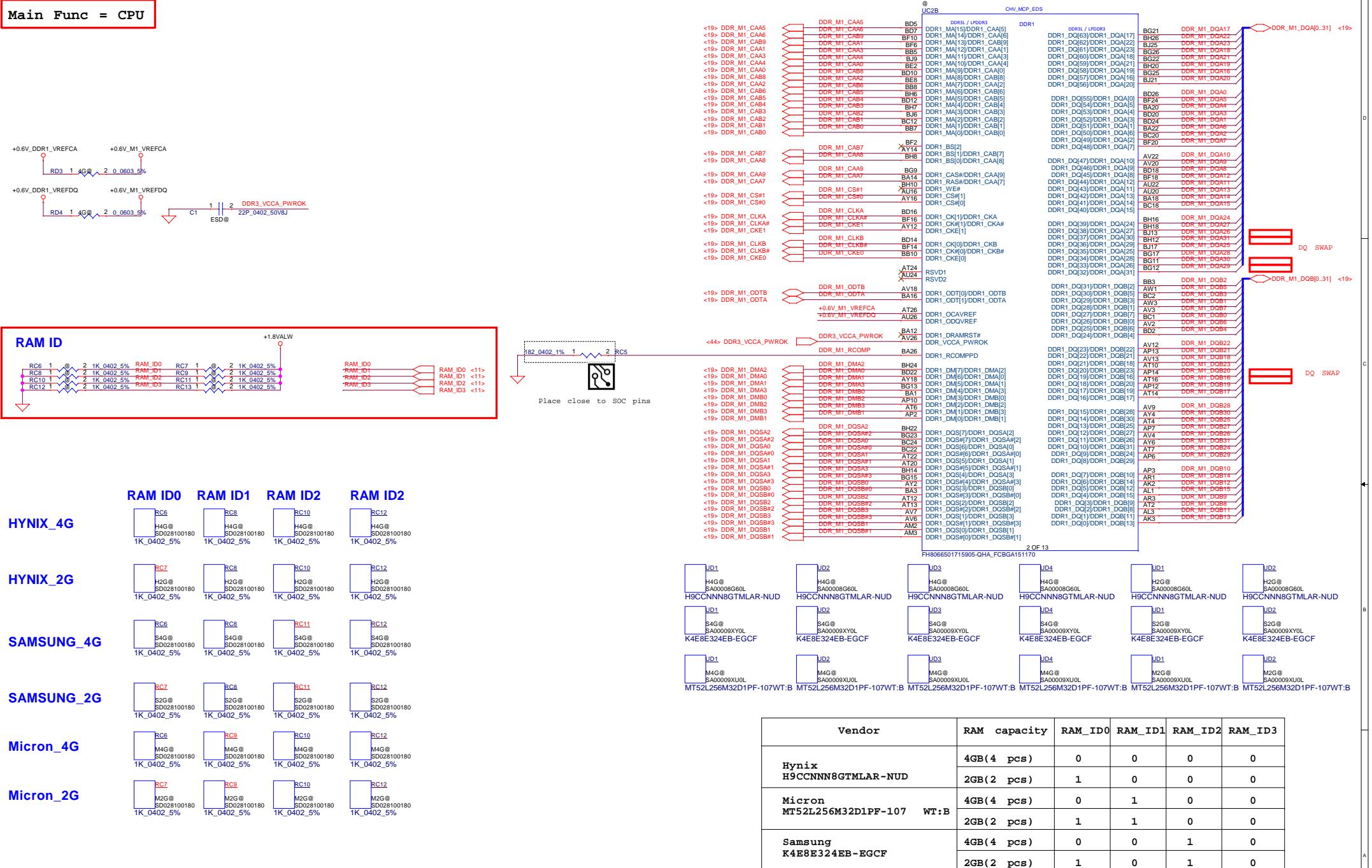
HYNIX 2G

SAMSUNG

SAMSUNG

Micron_4

Micron_2



Main Func = CPU

**Modify : DDI/XDP/SDMMC net name
link XDP/SDMMC**

Display mapping	
DDI0	NC
DDI1	eDP
DDI2	HDMI

SD mapping
SDMMC1 eMMC
SDMMC2 NC
SDMMC3 SD Card

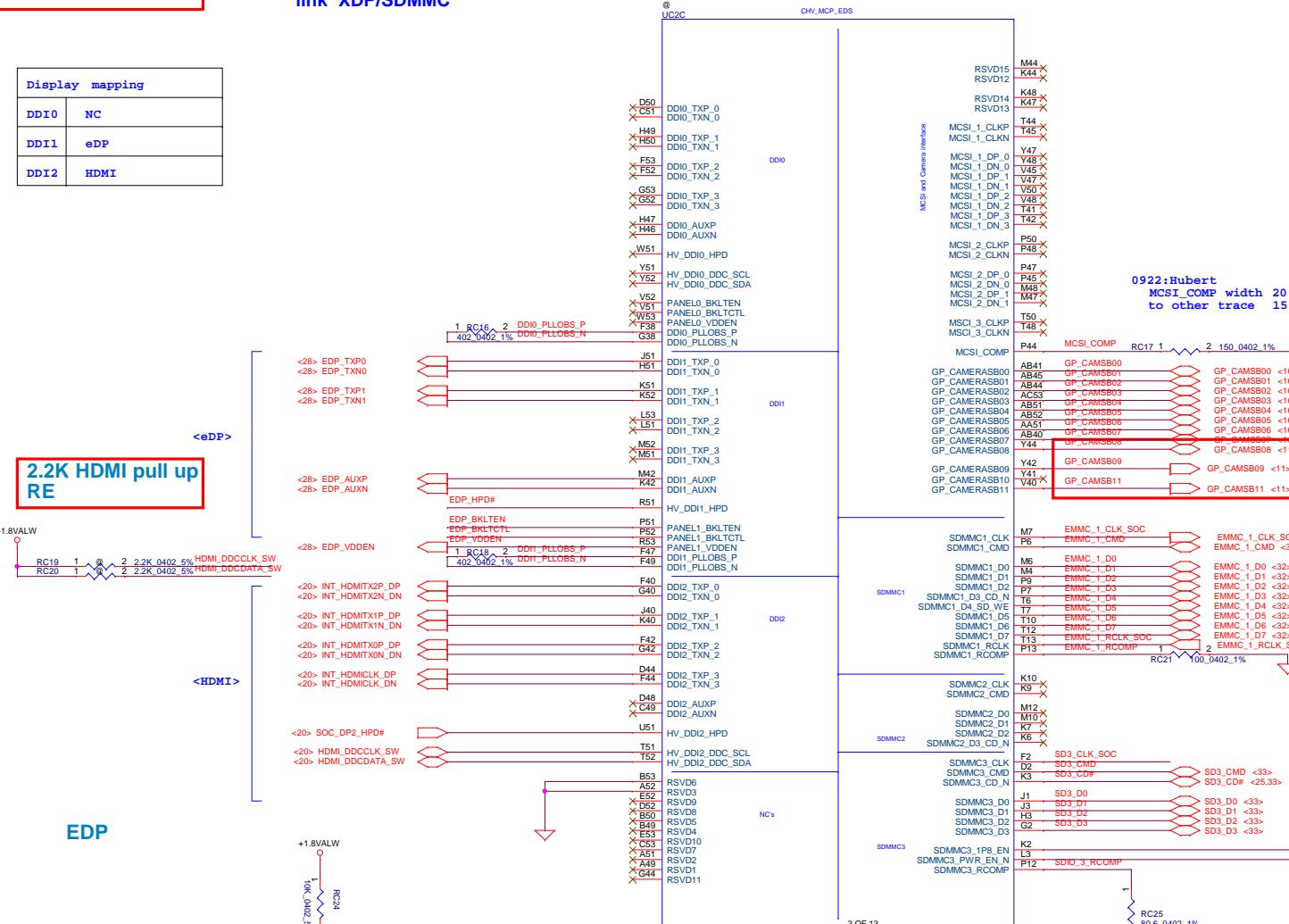
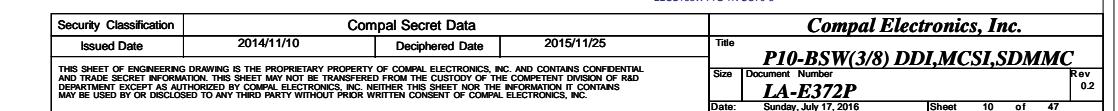


Table 24-2. Digital Display Interface Supported

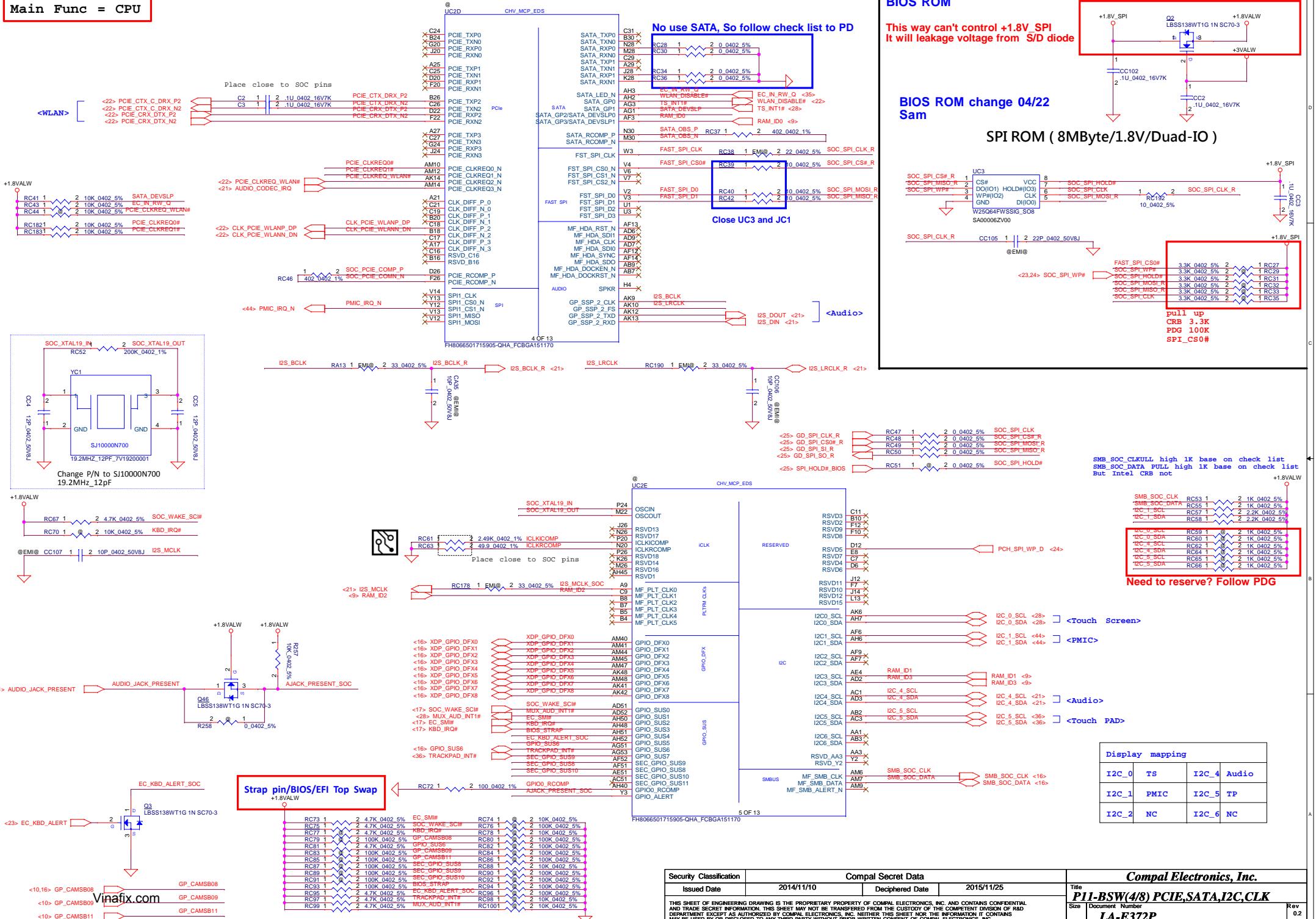
Port	Supported
DDI0	HDMI, DP, or eDP*
DDI1	HDMI, DP, or eDP*
DDI2	HDMI or DP

*Connection to two HDMI displays can be supported simultaneously. It is recommended to have the HDMI on

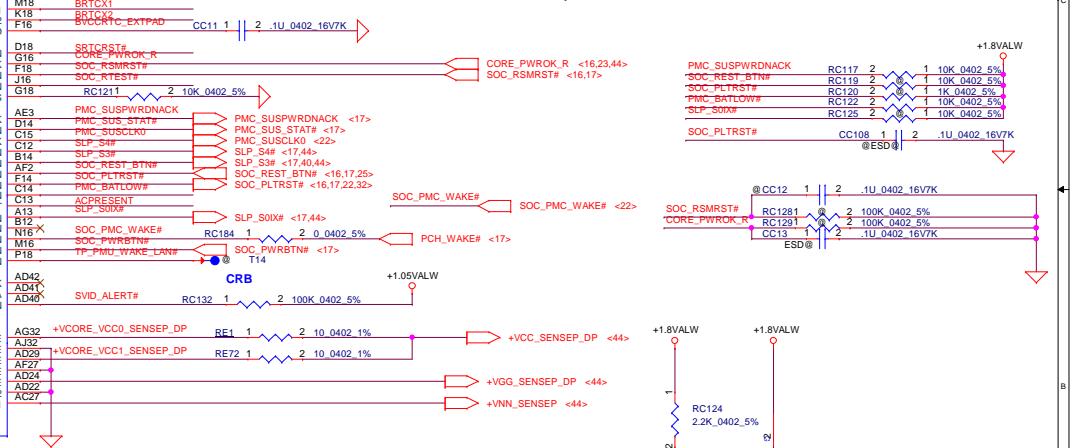
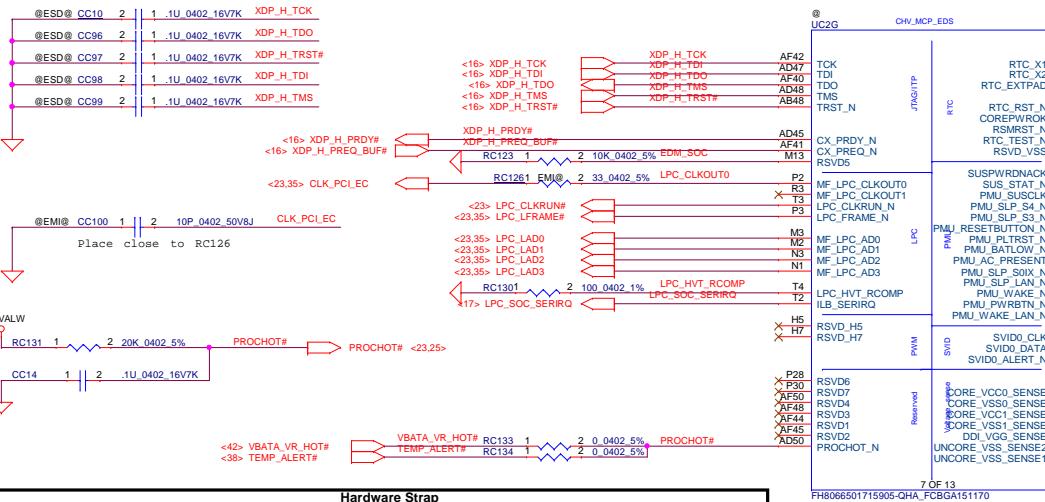
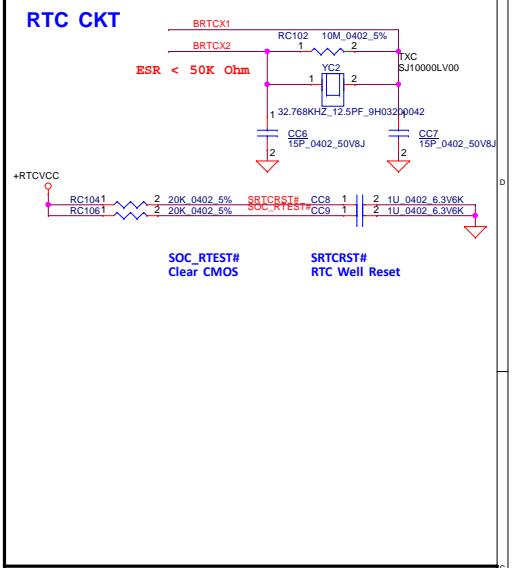
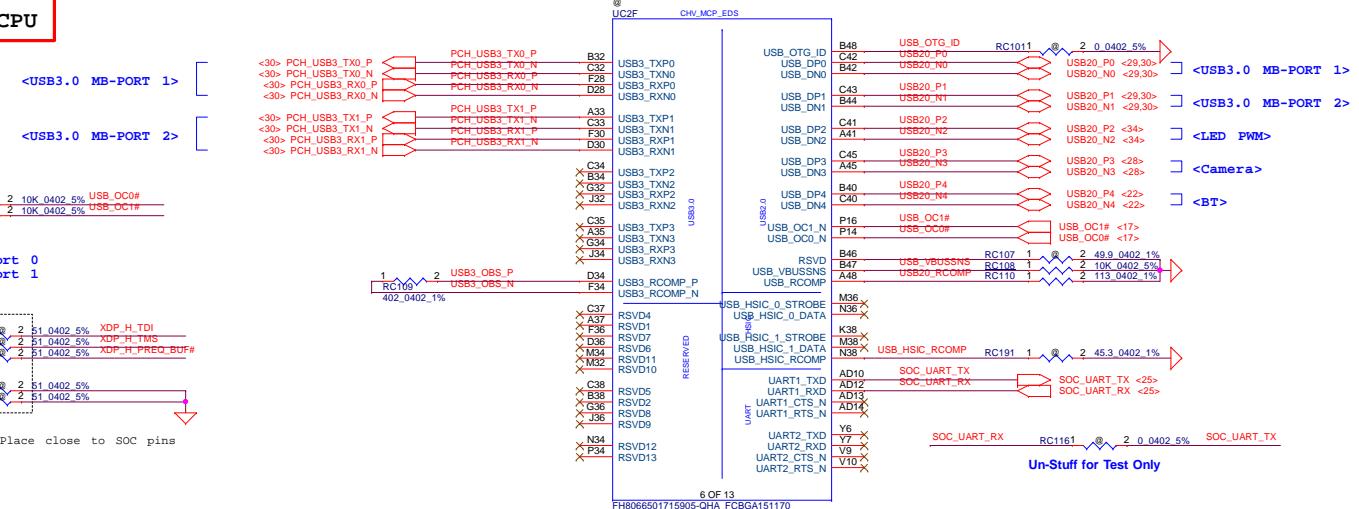
Vinifix.com Materials to two HDMI displays can be supported simultaneously. It is recommended to have the HDMI or DDO & DDI2 ports.



Main Func = CPU

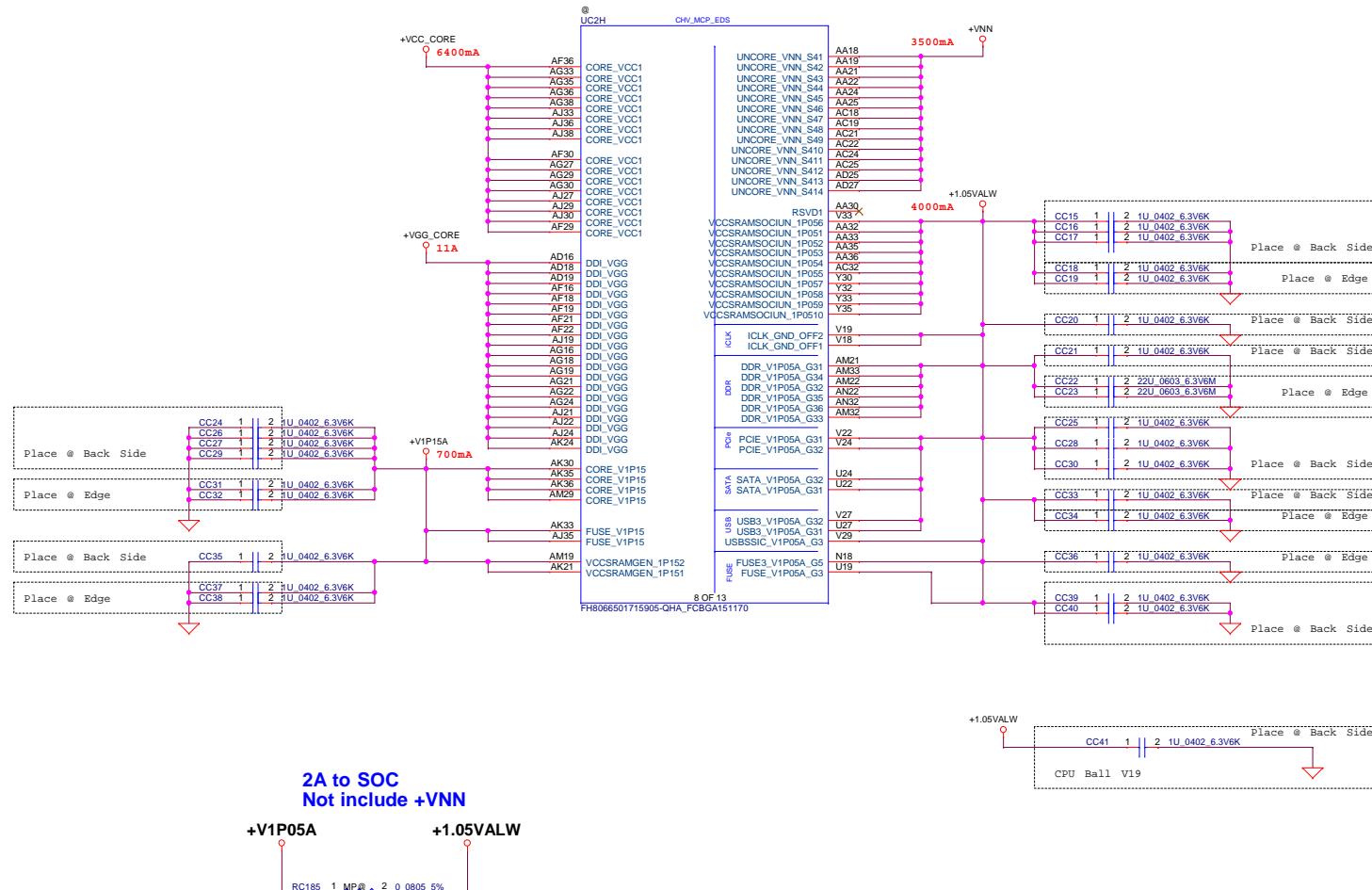


Main Func = CPU



Hardware Strap				
Pin Name	Purpose	PU/PD	Description	Default State
GPIO_SUS0	DDI0 Detect	PD	1: DDI0 detected 0: DDI0 not detected	High
GPIO_SUS1	DDI1 Detect	PD	1: DDI1 detected 0: DDI1 not detected	High
GPIO_SUS2	A16 swap overdrive	PU	1: Normal operation 0: Change Boot Loader address	High check list pull up 10K
GPIO_SUS3	DSI Display Detect	PD	1: DSI detected 0: DSI not detected	Low
GPIO_SUS4	Boot BIOS Strap BBS	PU	1: Boot from SPI 0: Boot from LPC	High
GPIO_SUS5	Flash Descriptor Security Override	PU	1: Security enabled 0: Security disabled	High check list pull up 100K
GPIO_SUS6	DFX Boot Halt Strap, VISA Early POSM Debug Enable	PU	1: Normal operation 0: Halt boot enable	High
SEC_GPIO_SUS8	ICLK, USB2, DDI SFR Supply Select	PU	1: 1.35V supply 0: 1.25V supply	Low check list pull up 10K
SEC_GPIO_SUS9	ICLK, USB2, DDI SFR Bypass	PD	1: Bypass with 1.05V 0: No bypass	Low
GP_CAMERASB08	ICLK Xtal OSC Bypass	PD	1: Bypass 0: No bypass	Low
GP_CAMERASB09	CCU SUS RO Bypass	PD	1: Bypass 0: No bypass	Low
GP_CAMERASB11	RTC OSC Bypass	PD	1: Bypass 0: No bypass	Low

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					LA-E372P	0.2			
				Date:	Monday, July 25, 2016	Sheet	12	of	47

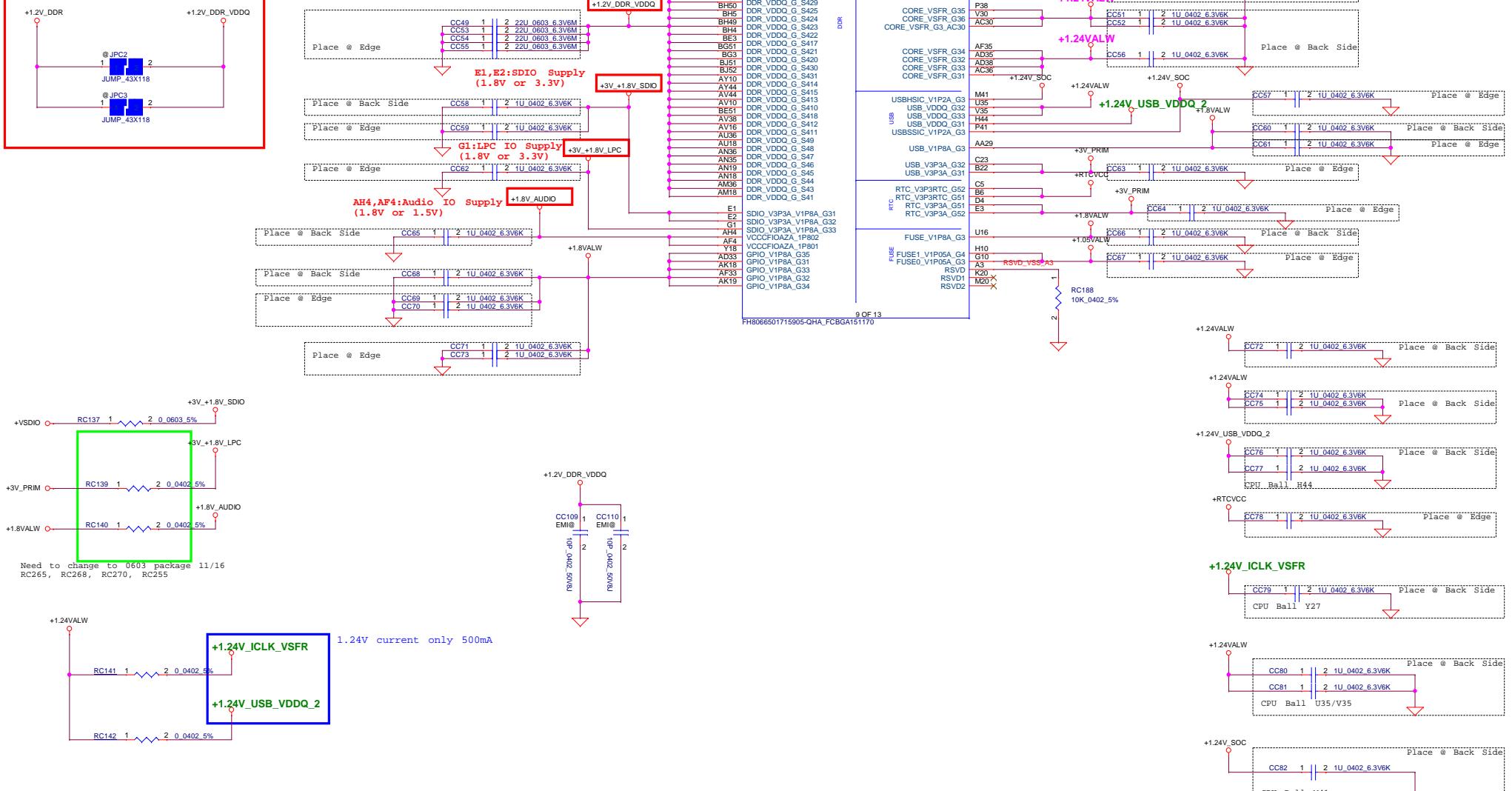


2A to SOC Not include +VNM

+V1P05A +1.05VAL
 RC185 1 MP 2 0 0805 5%

Main Func = CPU

Have to check 04/14



NOTE:

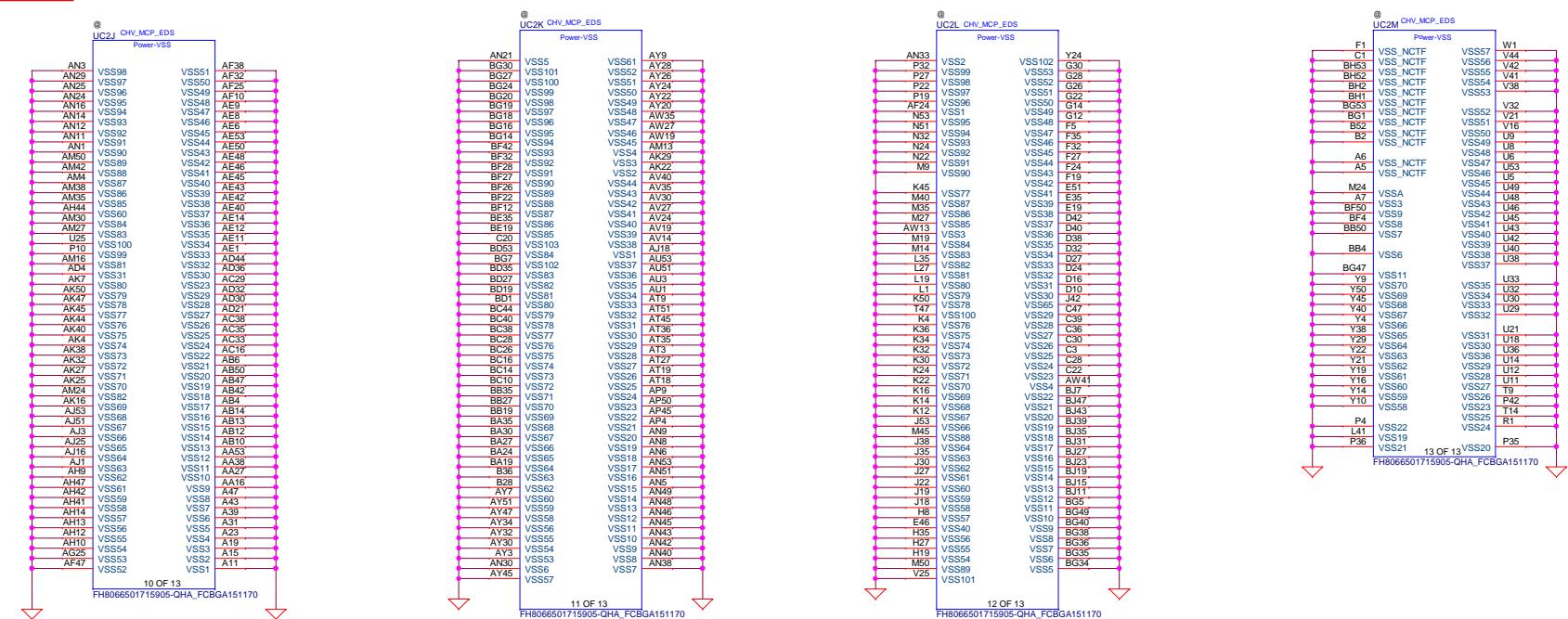
NOTE: +1.24V MIPI, +1.24V USBHSIC, +1.24V USBSSIC are +1.24V Only.

+1.24V_MIP1,
[PPG Rev0R92]

[FDG RevOp92 F.35] When SSIC, HSIC & CSI interface is not used, the following pins can be connected to ground:

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				Date	Sunday, July 17, 2016
				Sheet	14 of 47

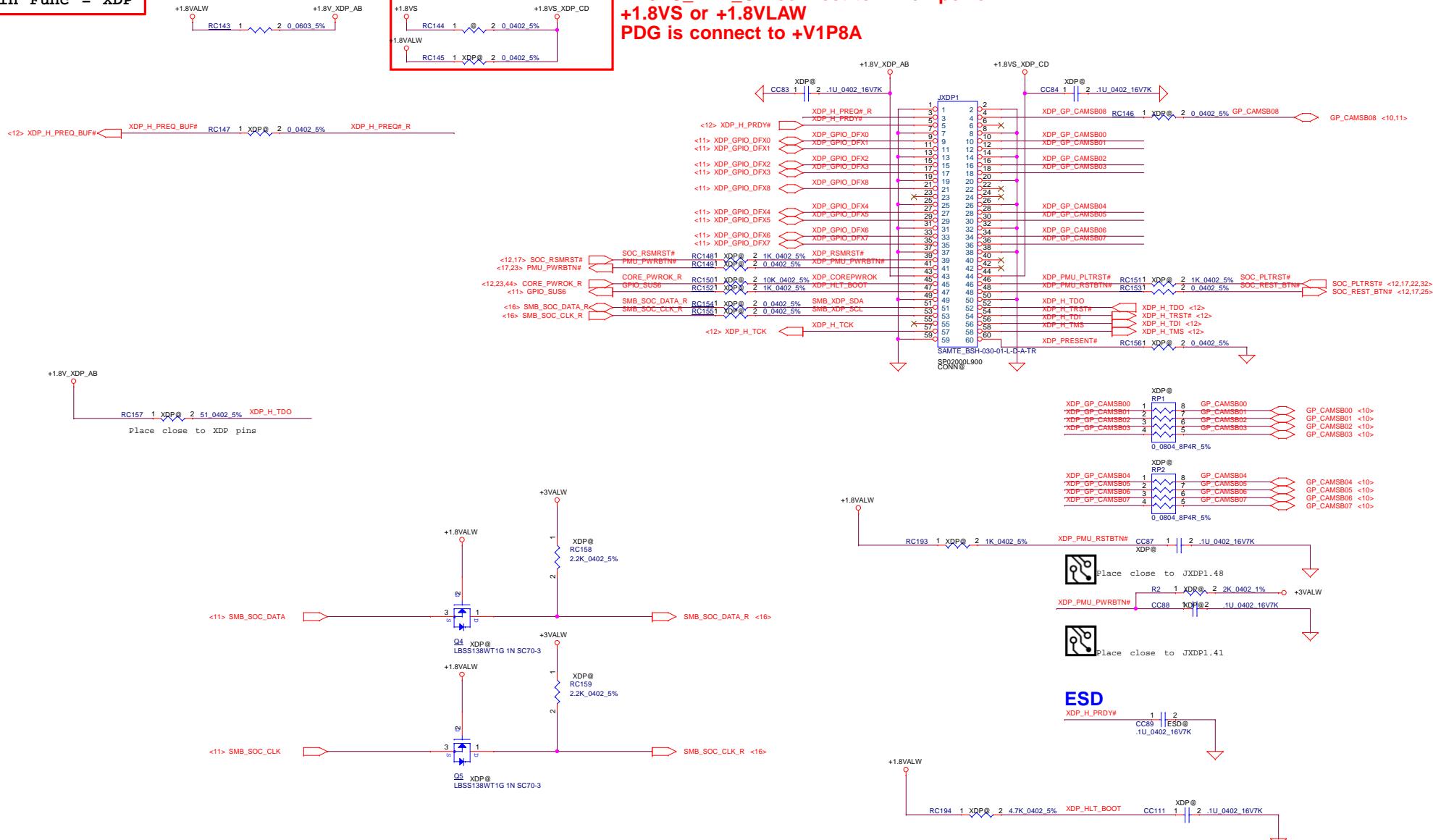
Main Func = CPU



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Issued Date	Deciphered Date	2014/11/10	2015/11/25	Title	P15-BSW(8/8) GND
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LA-E372P		Sunday, July 17, 2016		Date:	Sheet 15 of 47

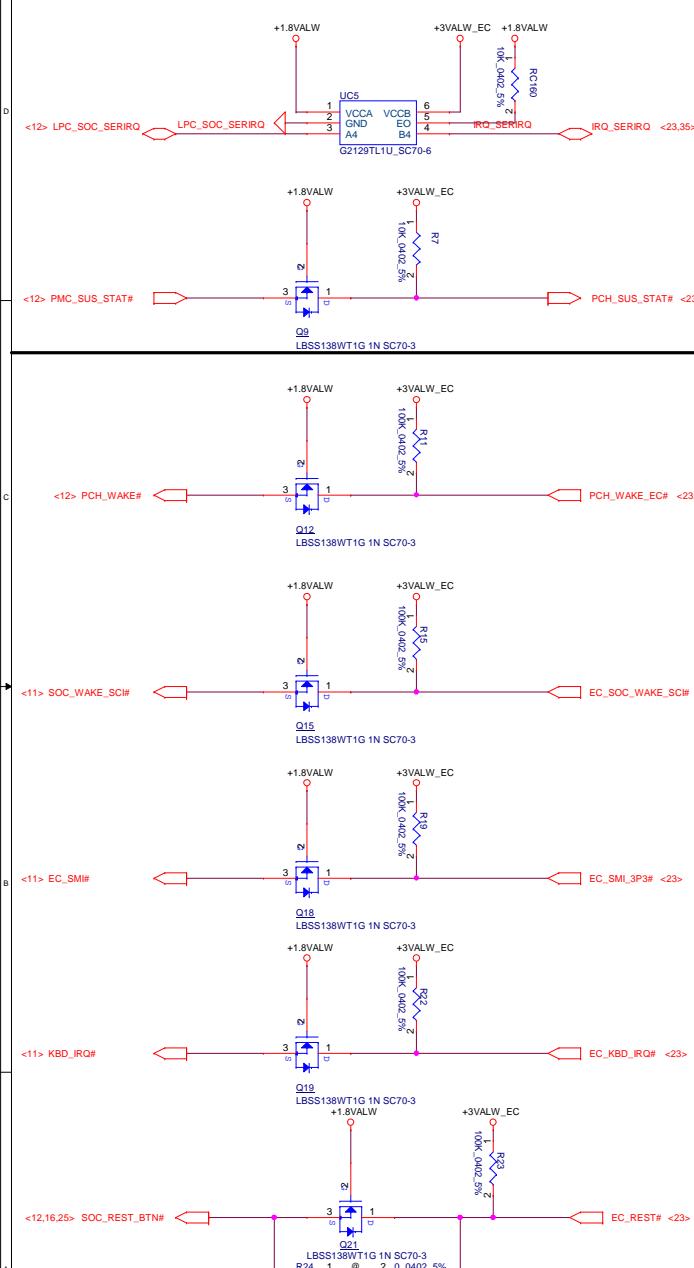
Main Func = XDP

+1.8VS_XDP_CD connect to which power
+1.8VS or +1.8V LAW
PDG is connect to +V1P8A

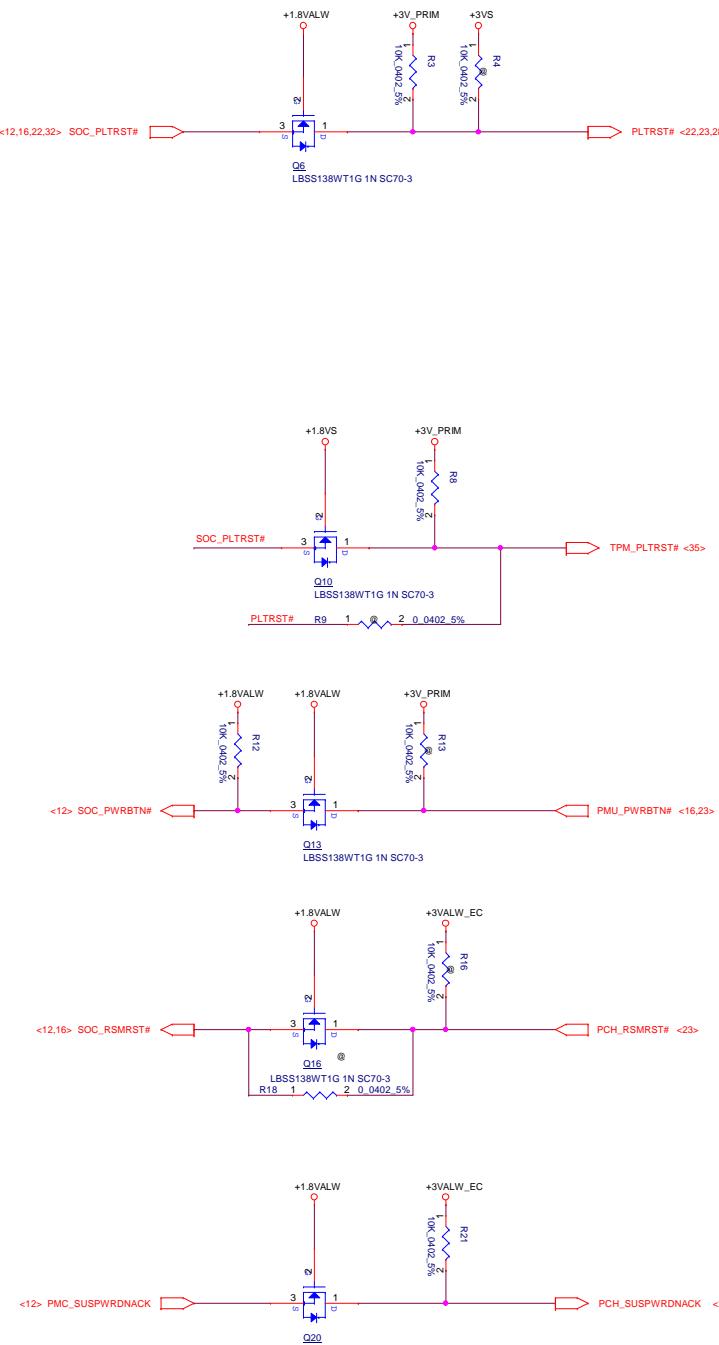


Main Func = Level Shift

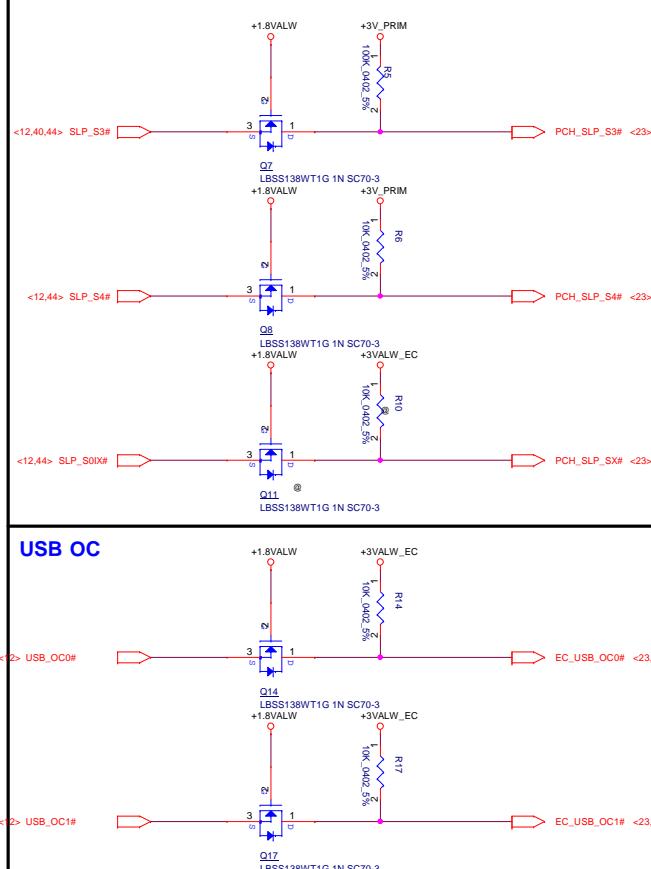
POWER ON SEQUENCE



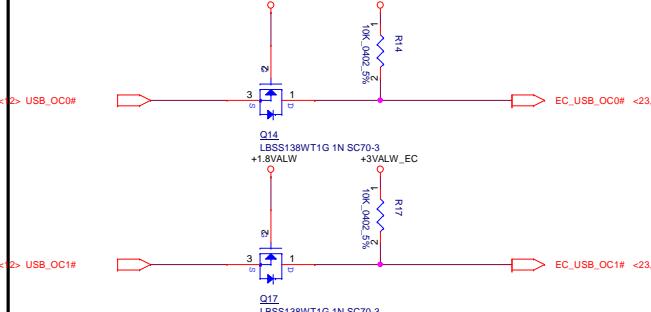
POWER ON SEQUENCE

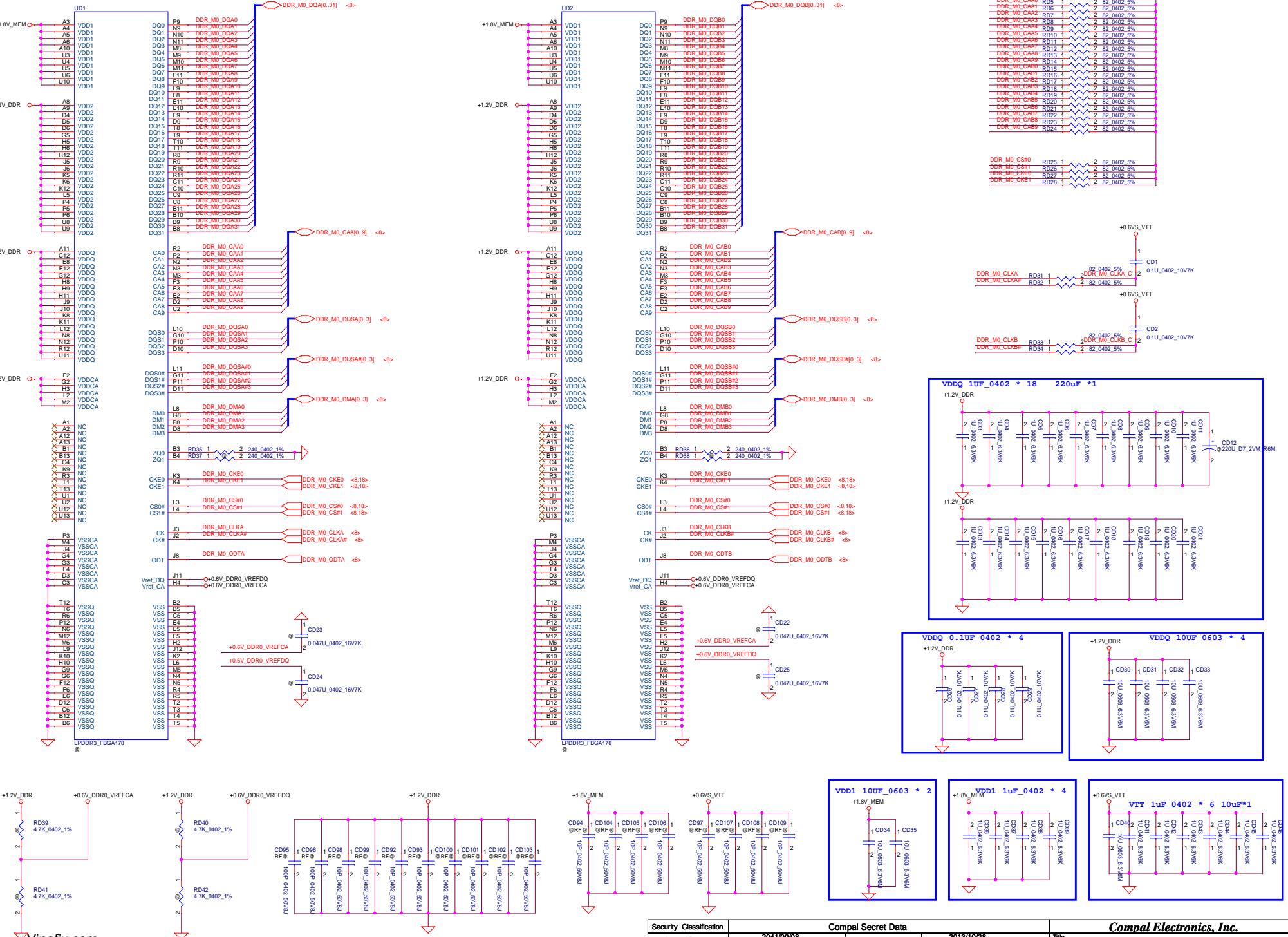


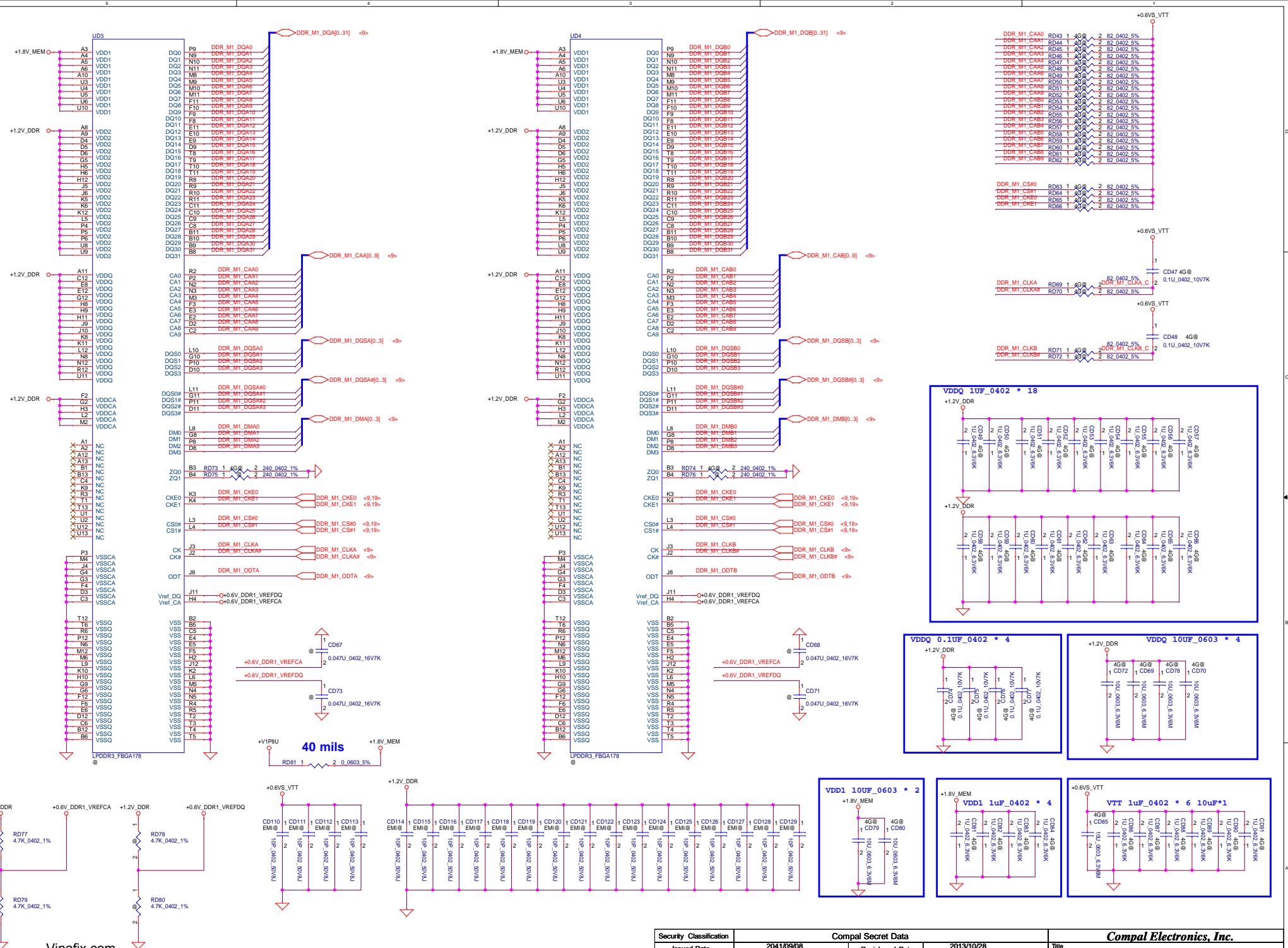
POWER ON SEQUENCE



USB OC



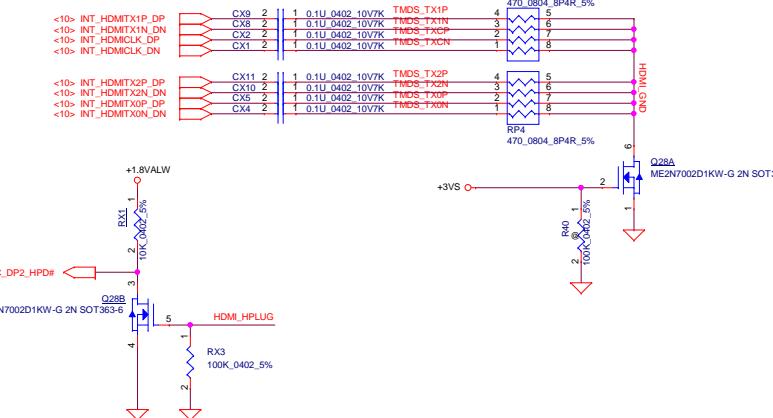




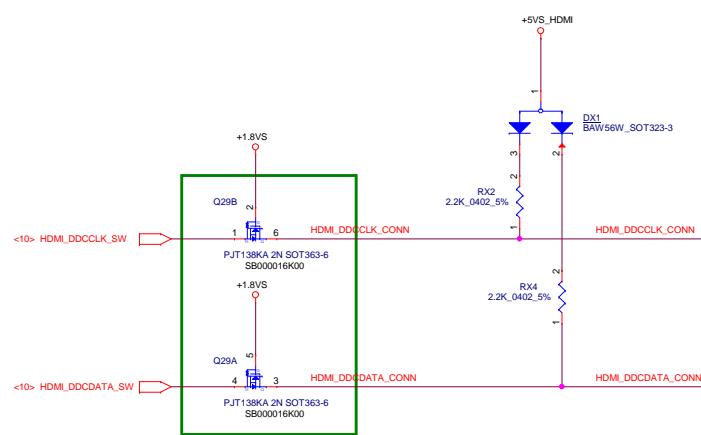
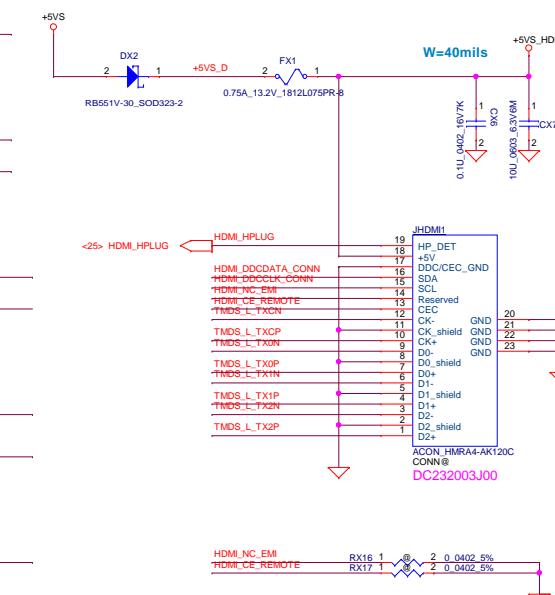
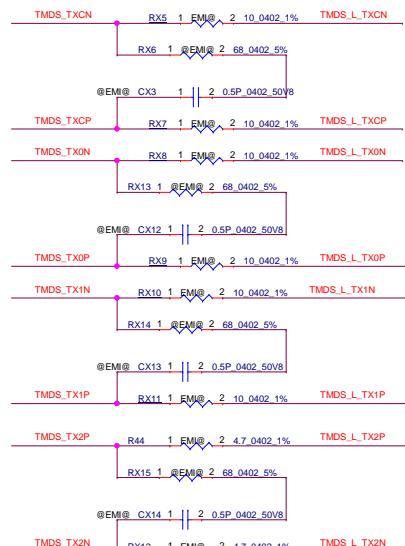
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2041/09/08	Deciphered Date	2013/10/28	Title	LPDDR3 Channel B	
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Size	Document Number				Rev	
	LA-E372P				0.2	
Date:	Sunday, July 17, 2016	Sheet	1	of	19	47

Main Func = HDMI

45@ ROYALTY HDMI W/LOGO	
Part Number	Description
RO00000021H	HDMI W/Logo:RO00000021H



Place close to JHDMI1

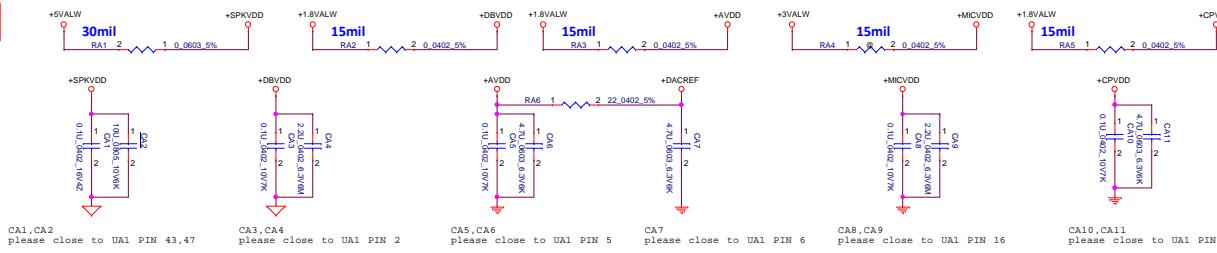


Level Shifter
Vinafix.com

Change the MOS 04/22
Sam

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/11/10	Deciphered Date	2015/11/25	Title
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Size	Document Number	P21-HDMI	Rev	0.2
	LA-E372P			
Date:	Monday, July 18, 2016	Sheet	20	of 47

Main Func = Codec



CA1, CA2
please close to UA1 PIN 43,47

CA3, CA4
please close to UA1 PIN 2

CA5, CA6
please close to UA1 PIN 5

CA7
please close to UA1 PIN 6

CA8, CA9
please close to UA1 PIN 16

CA10, CA11
please close to UA1 PIN 22

CA12_1

M

2 22P_0402_50VBJ DS_MCLK_R

CA21_1

2 47U_0603_6.3V6K MICBIAS1

CA21_2

2 47U_0603_6.3V6K MICBIAS2

DMIC

20mil (DCVDD)

CA13

+DBVDD

2 2.2U_0402_8.3V6M +DCVDD

AVDD

+CPVDD

+SPKVDD

SPKVDDR

SPKVDDL

MICBIAS1

RAT

2 0.0402 5%

MICBIAS2

RAB

2 0.0402 5%

MICBIAS1_R

MICBIAS2_R

RNG2_INP

RNG2_INT

SLEEVE_INN

IN1N_SLEEVE

SLEEVE_SENSE

IN1N_RING2

IN1N_RING1

SLEEVE_SENSE

IN2PIN/NU/DMIC2_SDA

DMIC_DATA

RA9

1

2 0.0402 5%

DMIC_DATA_R

RA11

1

2 15.0402 5%

I2S_MCLK_R

RA11

1

2 0.0402 5%

I2S_LRCLK_R

RA14

1

2 0.0402 5%

I2S_DIN

RA15

1

2 0.0402 5%

I2S_DOUT

RA15

1

2 0.0402 5%

CODEC

CA24

1

2 10U_0805_10V6K

VREF2

DACREF

CA25

1

2 47U_0603_6.3V6K

MICBIAS1

RA17

1

EMI²

2 0.0402 5%

GND

RA19

1

EMI²

2 0.0402 5%

GND

RA21

1

EMI²

2 0.0402 5%

GND

RA22

1

EMI²

2 0.0402 5%

GND

RA20

1

EMI²

2 0.0402 5%

GND

RA18

1

EMI²

2 0.0402 5%

GND

RA16

1

EMI²

2 0.0402 5%

GND

RA14

1

EMI²

2 0.0402 5%

GND

RA12

1

EMI²

2 0.0402 5%

GND

RA10

1

EMI²

2 0.0402 5%

GND

RA8

1

EMI²

2 0.0402 5%

GND

RA6

1

EMI²

2 0.0402 5%

GND

RA4

1

EMI²

2 0.0402 5%

GND

RA2

1

EMI²

2 0.0402 5%

GND

RA0

1

EMI²

2 0.0402 5%

GND

RA1

1

EMI²

2 0.0402 5%

GND

RA13

1

EMI²

2 0.0402 5%

GND

RA15

1

EMI²

2 0.0402 5%

GND

RA17

1

EMI²

2 0.0402 5%

GND

RA19

1

EMI²

2 0.0402 5%

GND

RA21

1

EMI²

2 0.0402 5%

GND

RA22

1

EMI²

2 0.0402 5%

GND

RA20

1

EMI²

2 0.0402 5%

GND

RA18

1

EMI²

2 0.0402 5%

GND

RA16

1

EMI²

2 0.0402 5%

GND

RA14

1

EMI²

2 0.0402 5%

GND

RA12

1

EMI²

2 0.0402 5%

GND

RA10

1

EMI²

2 0.0402 5%

GND

RA8

1

EMI²

2 0.0402 5%

GND

RA6

1

EMI²

2 0.0402 5%

GND

RA4

1

EMI²

2 0.0402 5%

GND

RA2

1

EMI²

2 0.0402 5%

GND

RA0

1

EMI²

2 0.0402 5%

GND

RA1

1

EMI²

2 0.0402 5%

GND

RA13

1

EMI²

2 0.0402 5%

GND

RA15

1

EMI²

2 0.0402 5%

GND

RA17

1

EMI²

2 0.0402 5%

GND

RA19

1

EMI²

2 0.0402 5%

GND

RA21

1

EMI²

2 0.0402 5%

GND

RA22

1

EMI²

2 0.0402 5%

GND

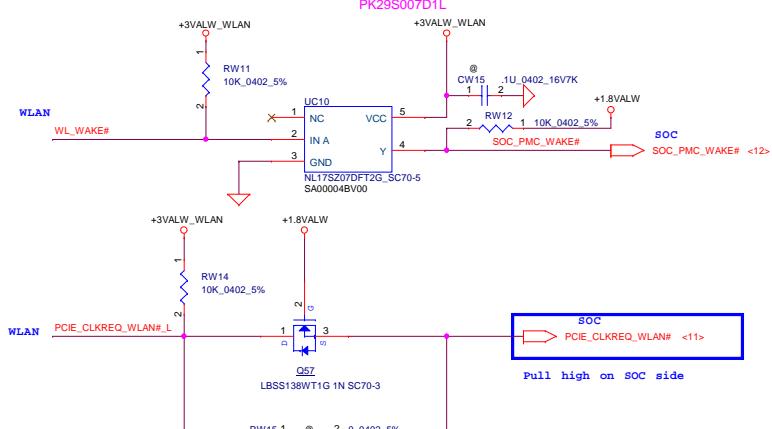
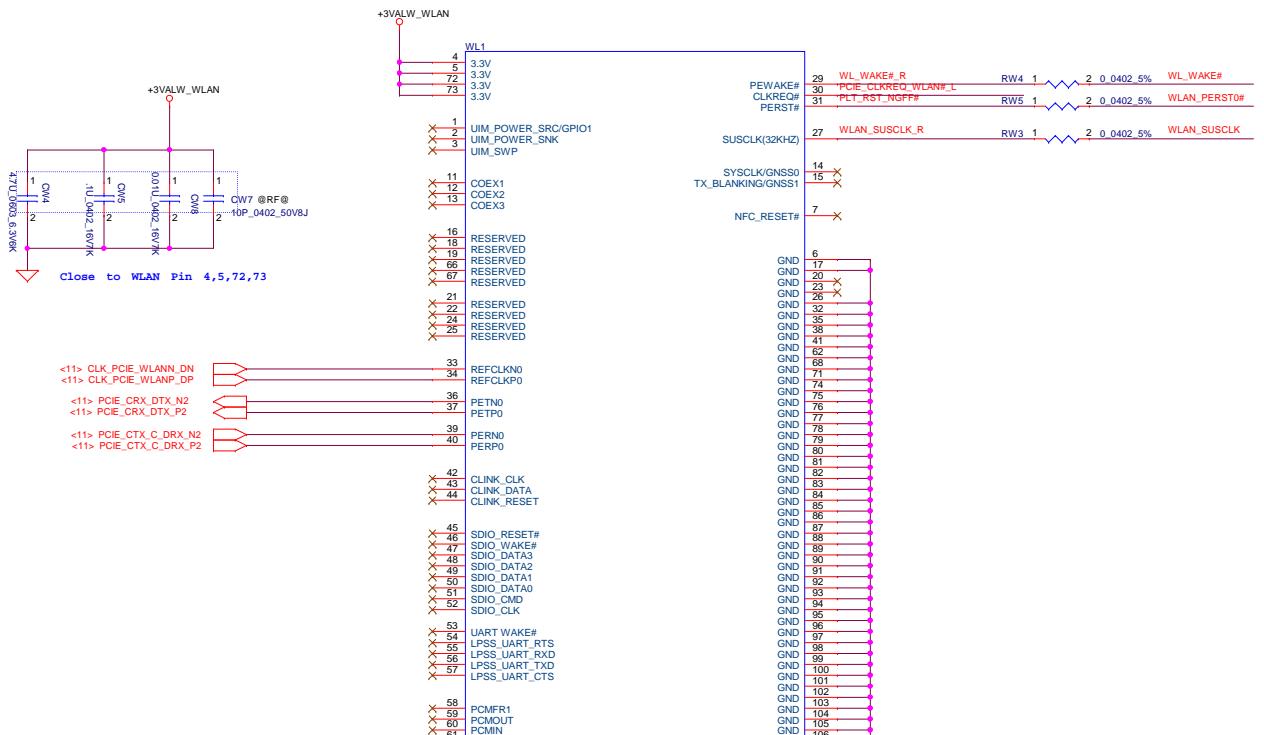
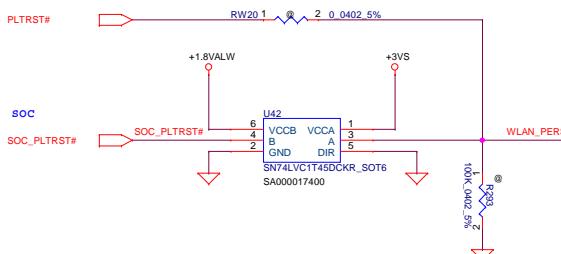
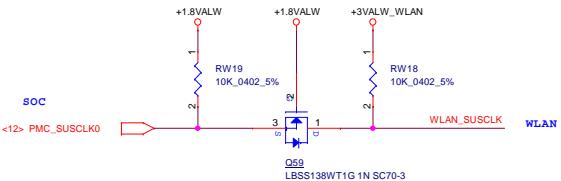
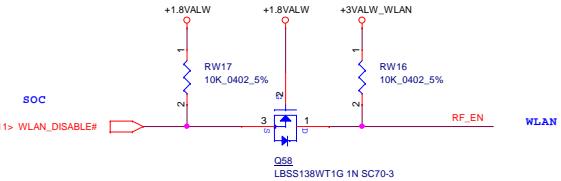
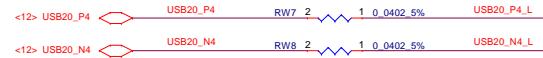
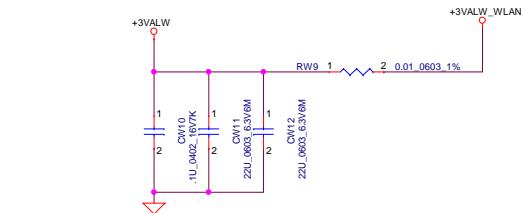
RA20

1

EMI²

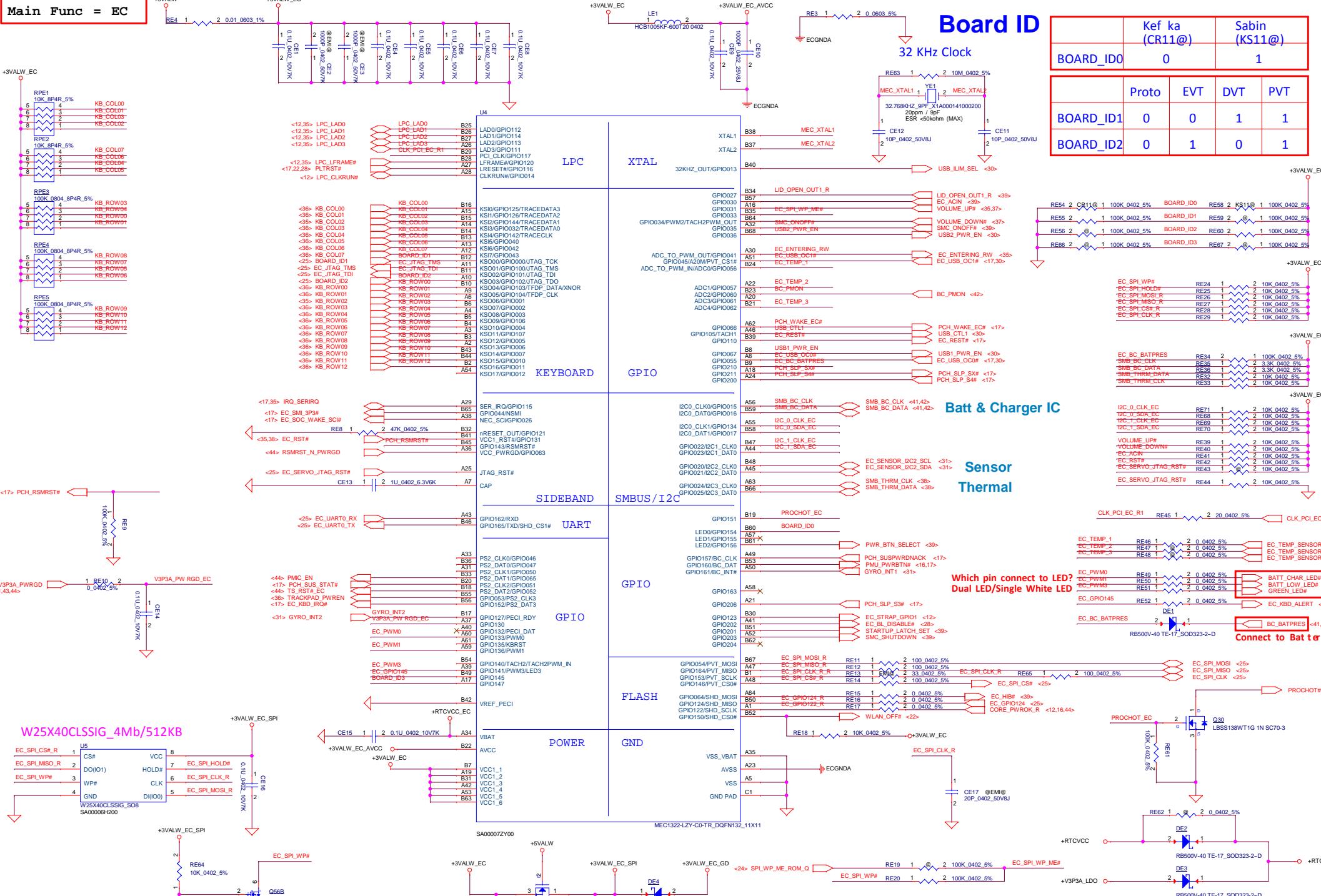
2 0.0402 5%

Main Func = WLAN

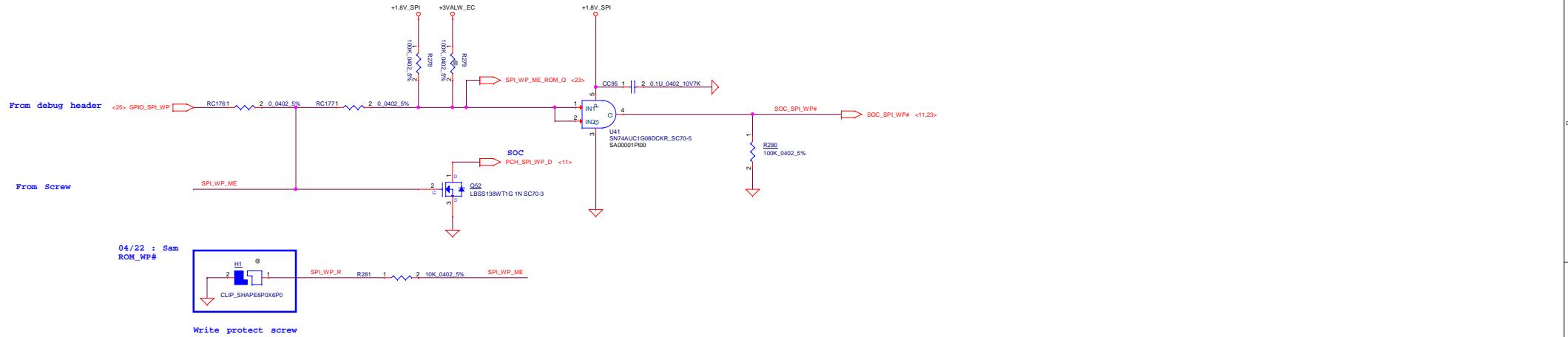


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Issued Date	Deciphered Date	2014/09/10	2015/12/10	Title	WLAN-BT/RTC
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Size	Document Number	LA-E372P	Rev	02	
Custom				Date:	Sunday, July 17, 2016
				Sheet	22 of 47

Main Func = EC

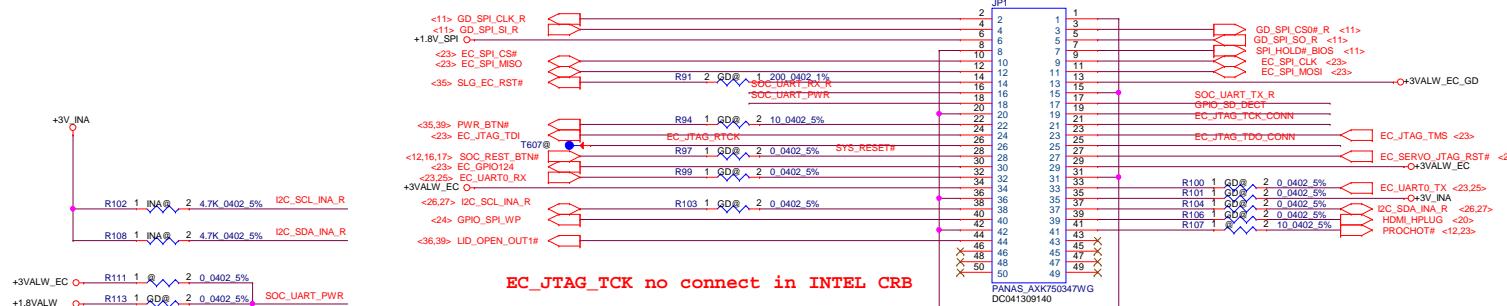


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Issued Date	2014/11/10	Deciphered Date	2015/11/25	P24-EC MEC-1322
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Size	Document Number	Rev. 0.2		
LA-E372P	Date:	Monday, July 25, 2016		Sheet 23 of 47

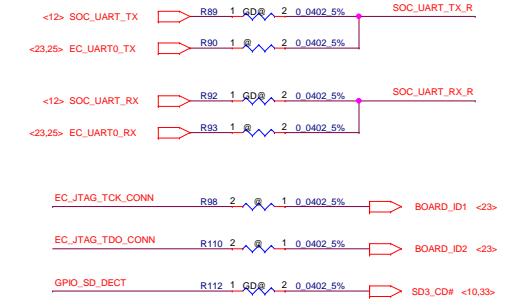


Main Func = Debug for Google

DEBUG CONNECTOR



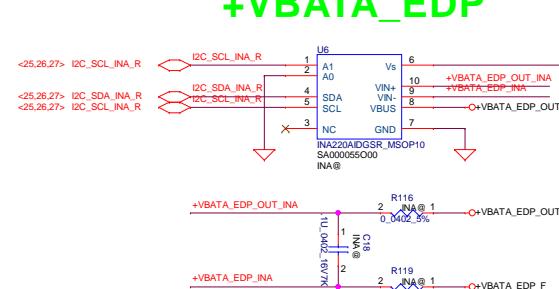
SOC



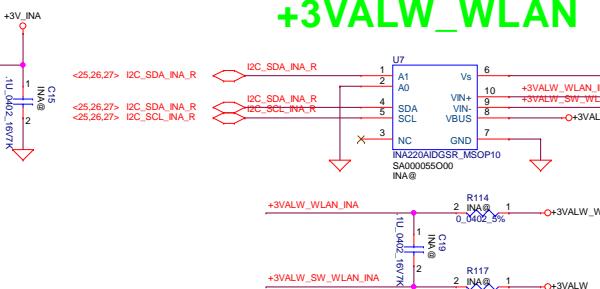
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	Deciphered Date	2014/11/10	2014/11/25	Title	P26-Google Debug
Size	Document Number	LA-E372P	Rev 0.2	Date:	Sunday, July 17, 2016
				Sheet	25 of 47

INA device

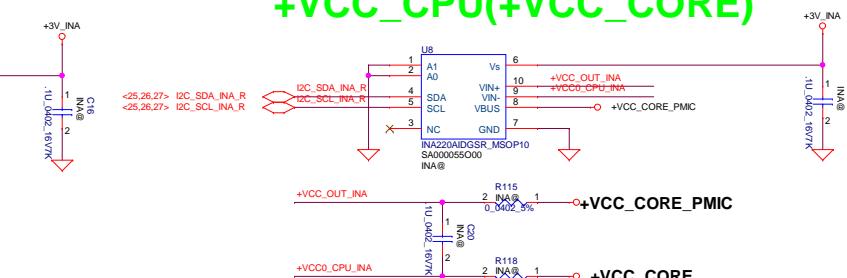
+VBATA_EDP



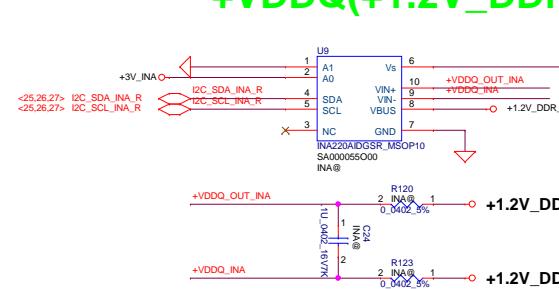
+3VALW_WLAN



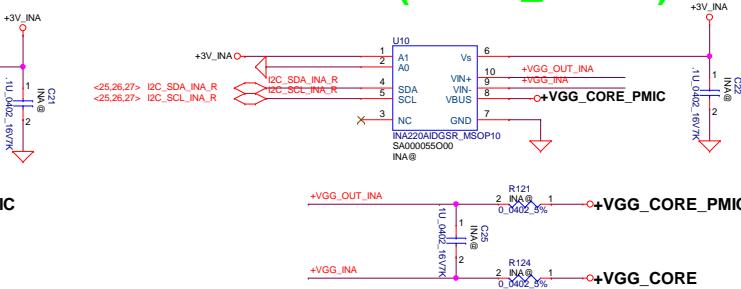
+VCC_CPU(+VCC_CORE)



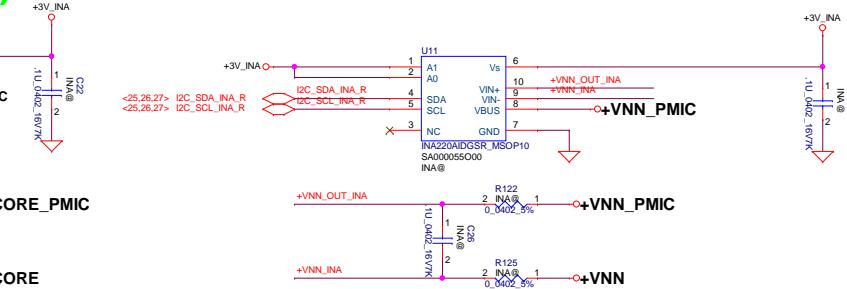
+VDDQ(+1.2V_DDR)



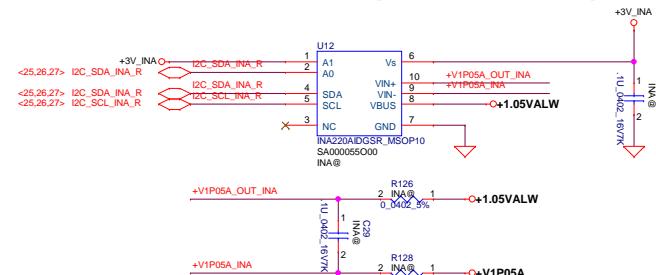
+VGG(+VGG_CORE)



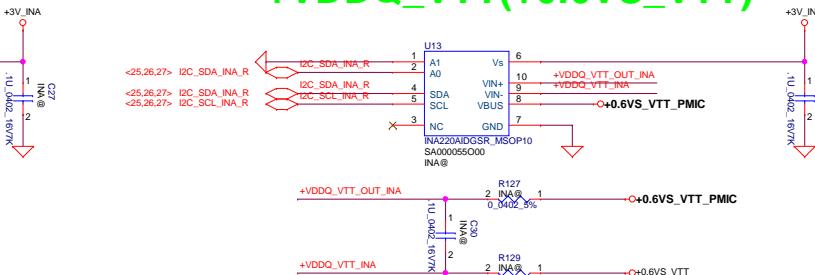
+VNN



+V1P05A(+1.05VALW)

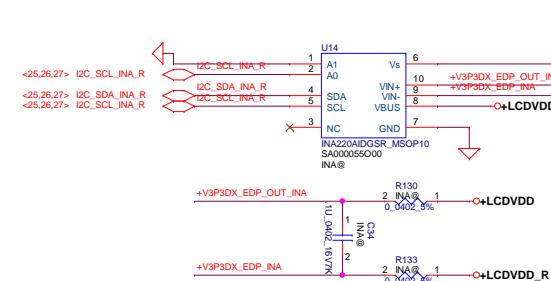


+VDDQ_VTT(+0.6VS_VTT)

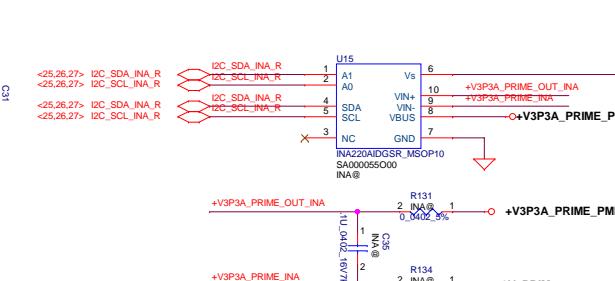


INA device

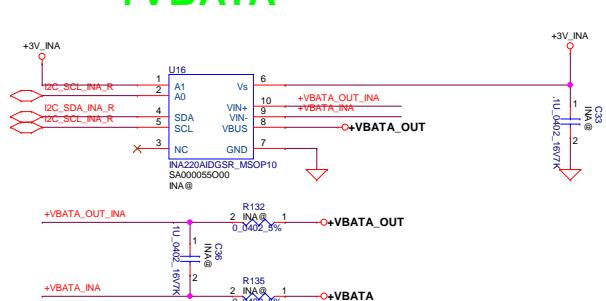
+V3P3DX_EDP(+LCDVDD)



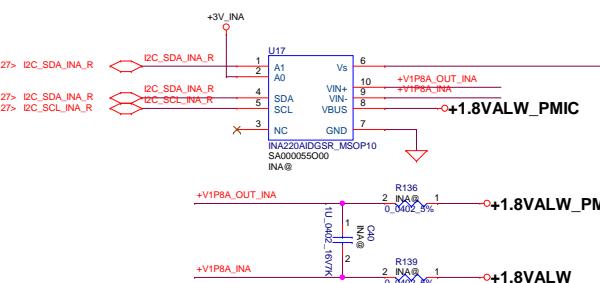
+V3P3A_PRIME(+3V_PRIM)



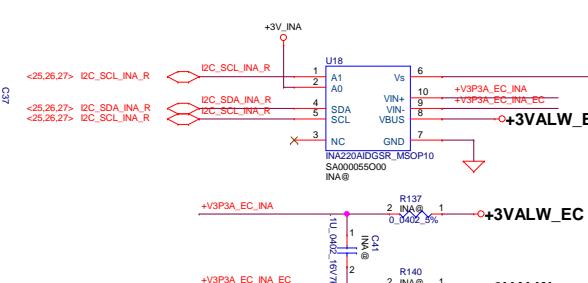
+VBATA



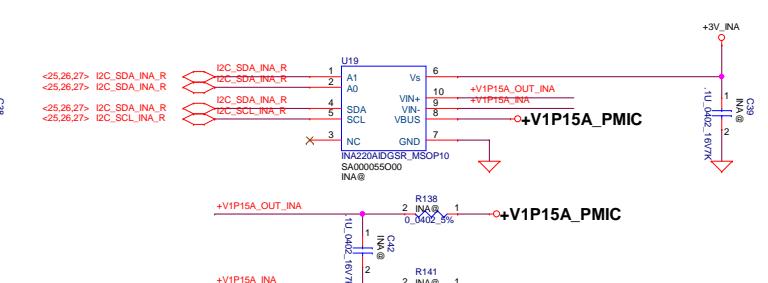
+V1P8A(+1.8VALW)

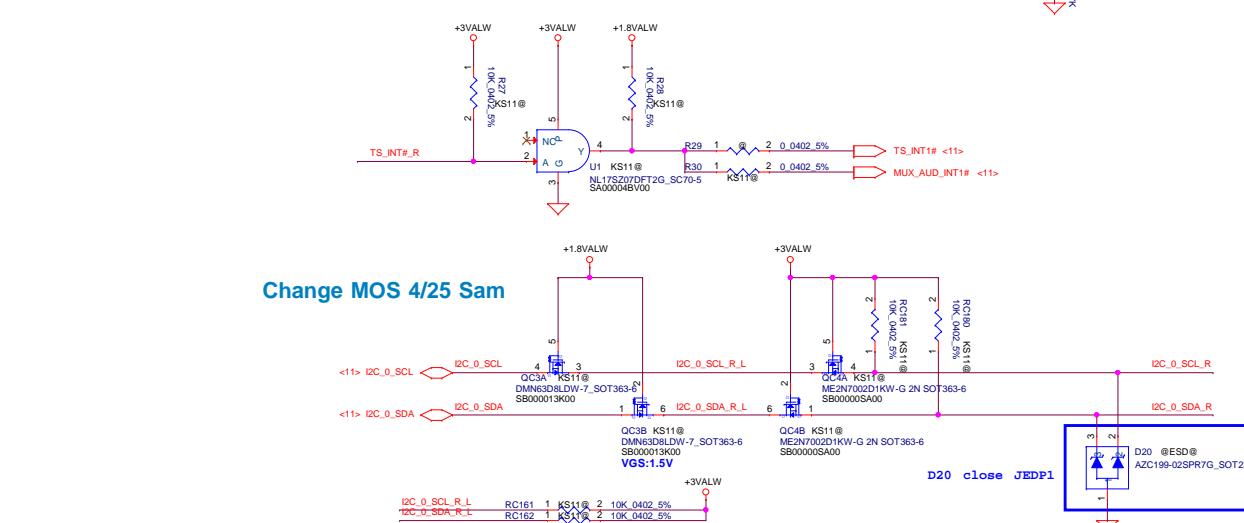
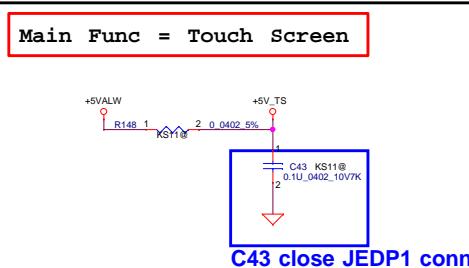
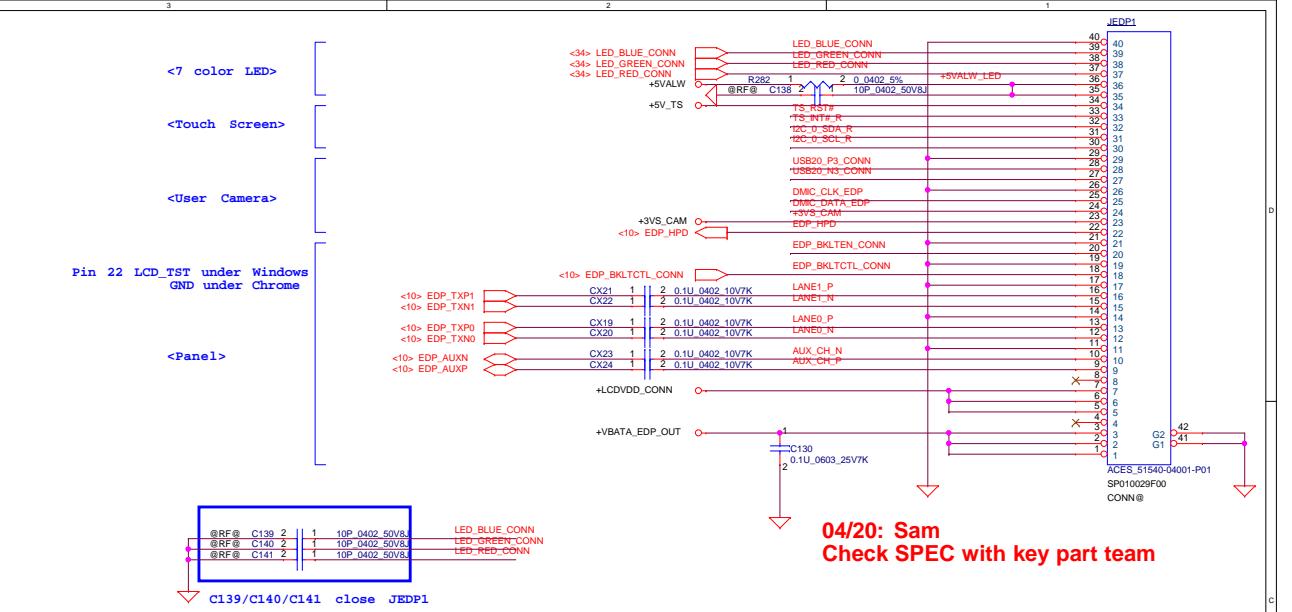
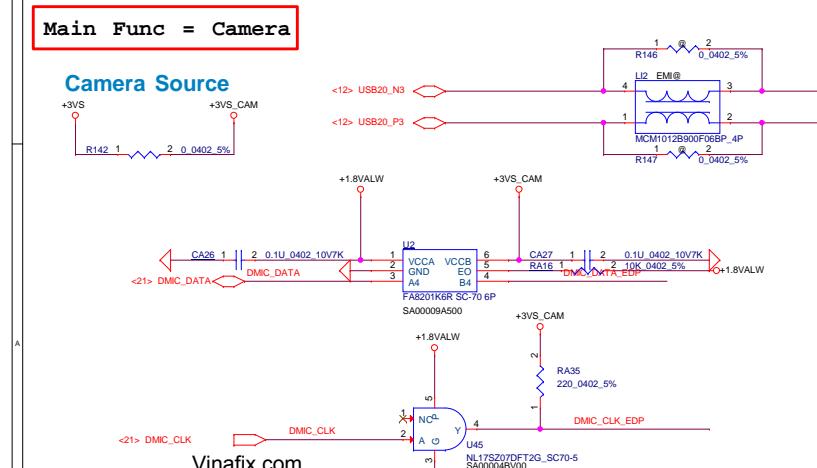
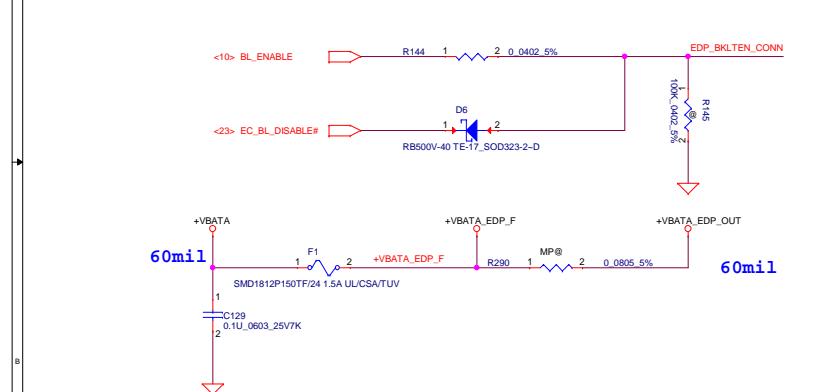
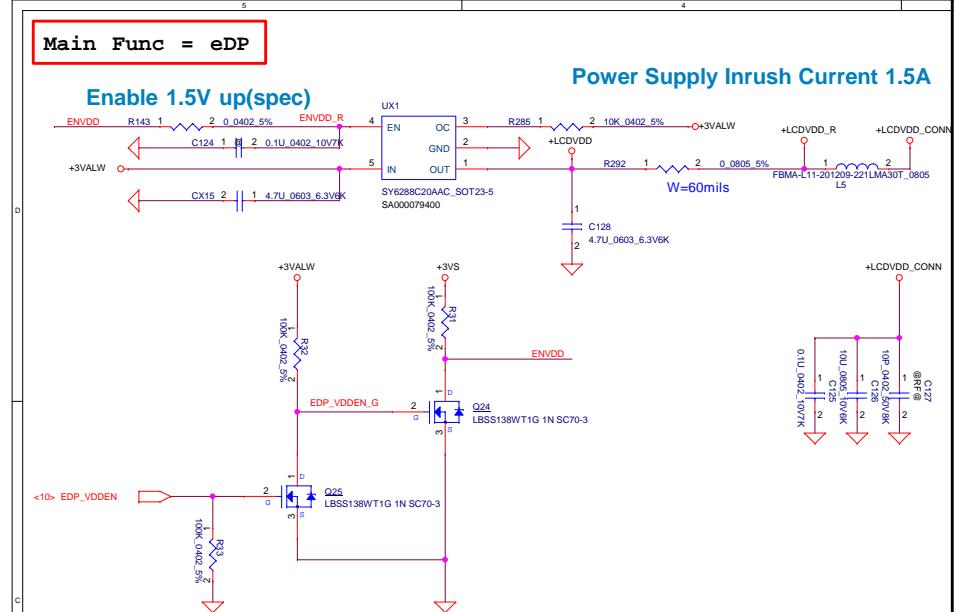


+3VALW_EC



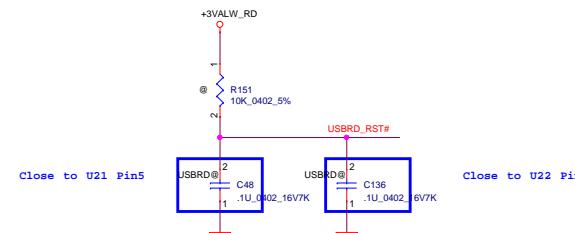
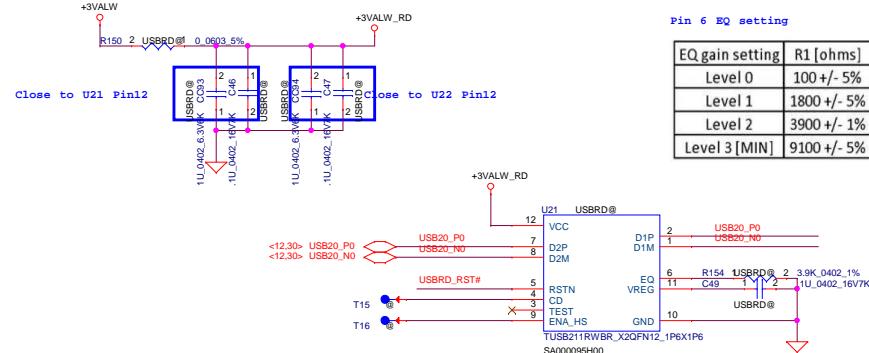
+1.15VALW



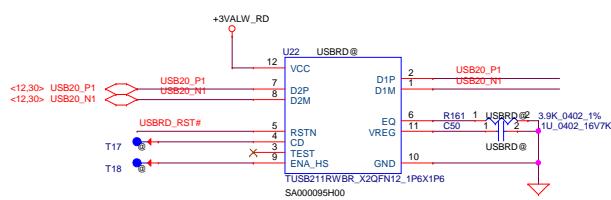


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Issued Date	2014/11/10	Deciphered Date	2015/11/25	Title	<i>P29-eDP/TS/Camera</i>	
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Size	Document Number					Rev 0.2
<i>LA-E372P</i>						
Date:	Thursday, July 28, 2016	Sheet	28	of	47	

USB 2.0 redriver for Power share_JUSB1



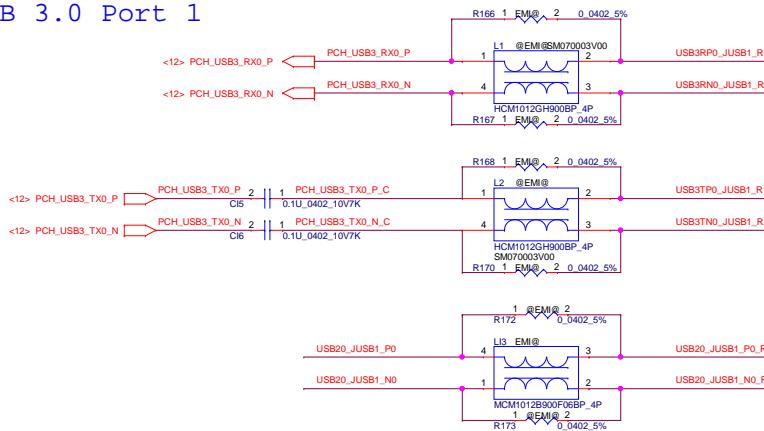
USB 2.0 redriver for Power share_JUSB2



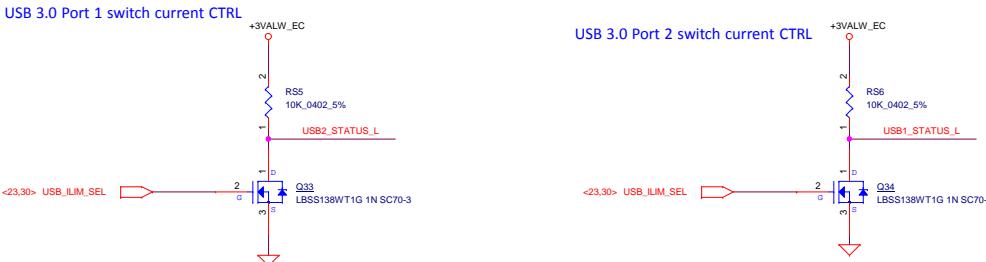
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	Deciphered Date	2015/11/25	Title	P30-USB2.0 redriver
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		LA-E372P	0.2	Date: Sunday, July 17, 2016

Main Func = USB3.0

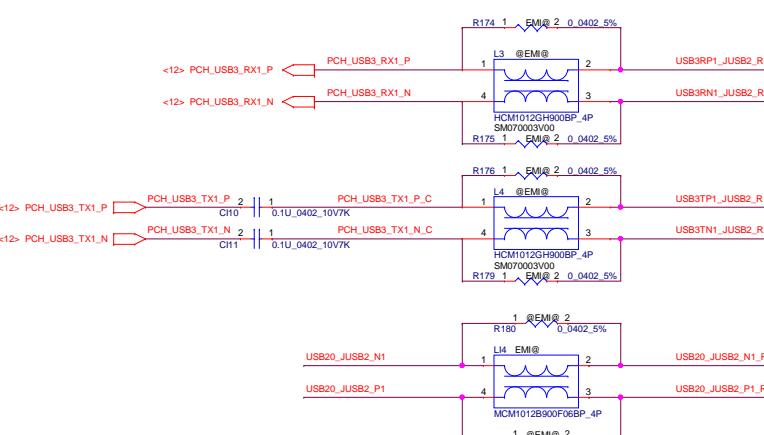
USB 3.0 Port 1



USB 3.0 Port 1 switch current CTRL



USB 3.0 Port 2



3

3

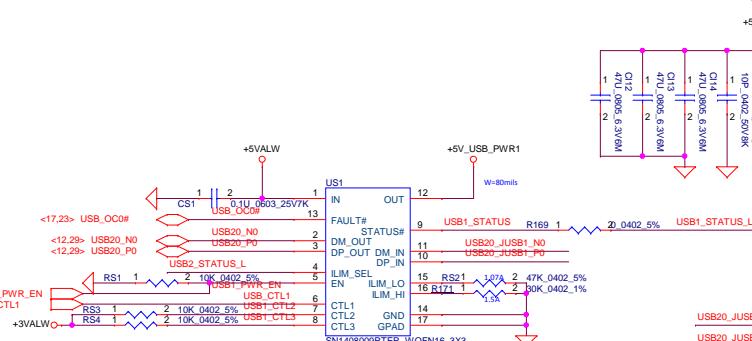
2

2

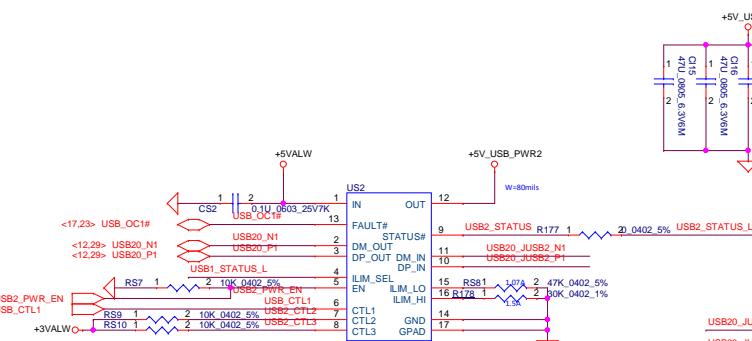
1

1

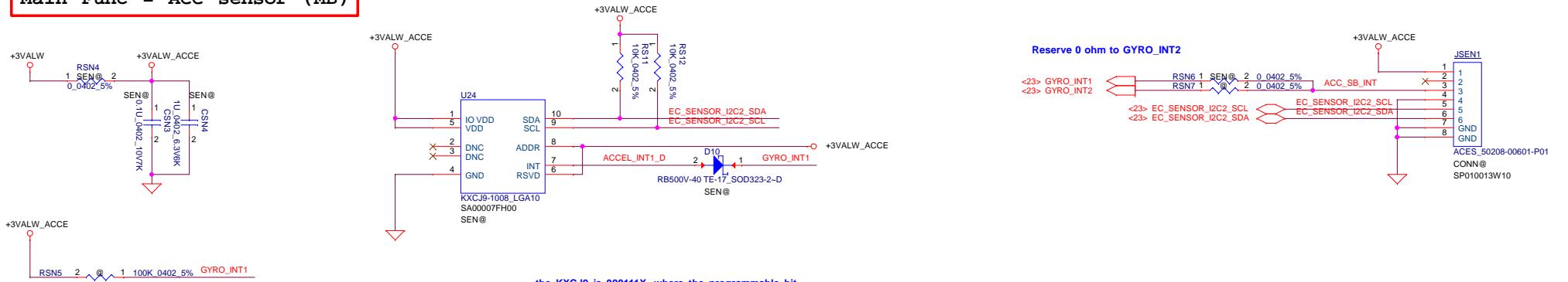
W=60mils



W=60mils



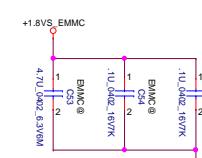
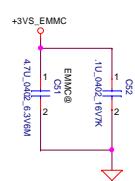
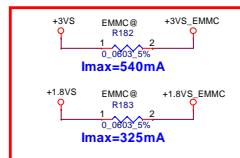
Main Func = ACC sensor (MB)



04/21:Sam
Check interrupt pin connect to which EC

Main Func = eMMC

Check eMMC power source



HYNIX

U25
EMMC_H16G @
SA0000A620L
16G_H26M51002HPR

U25
EMMC_H32G @
SA0000A700L
32G_H26M62002GMR

U25
EMMC_H64G @
SA0000A710L
32G_H26M74002EMR

SAMSUNG

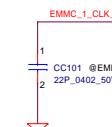
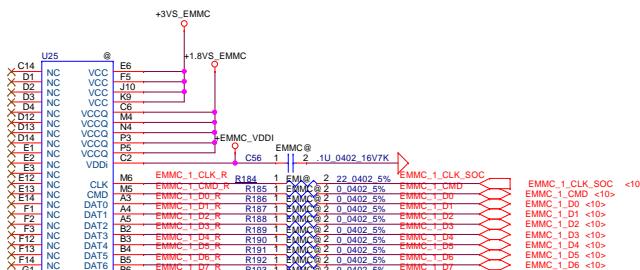
U25
EMMC_SAM16G @
SA0000R60L
16G_KLMAG1JENB-B041007

U25
EMMC_SAM32G @
SA0000QW0L
32G_KLMBG2JENB-B041007

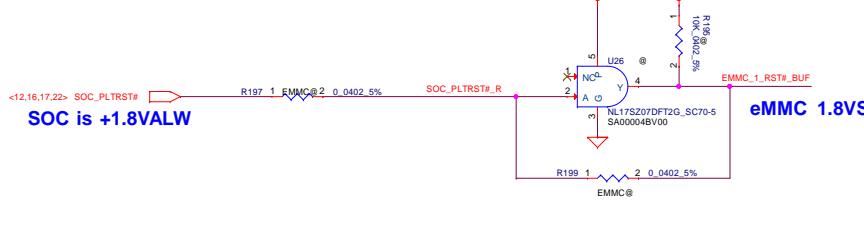
SANDISK

U25
EMMC_S16G @
SA0000A6Y0L
16G_SDINADF4-16G-859

U25
EMMC_S32G @
SA0000K91L
32G_SDINADF4-32G-859



SOC is +1.8VALW



eMMC 1.8VS

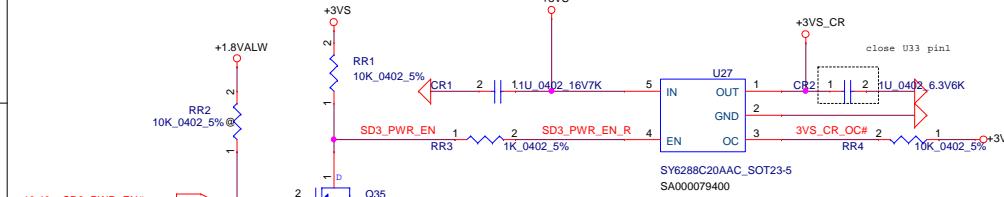
Use SDIN9DW4-16G symbol

H26M52208PR_FBG 153P
SA00009DK00

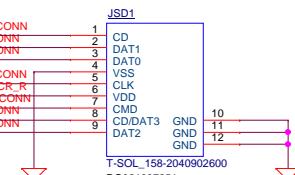
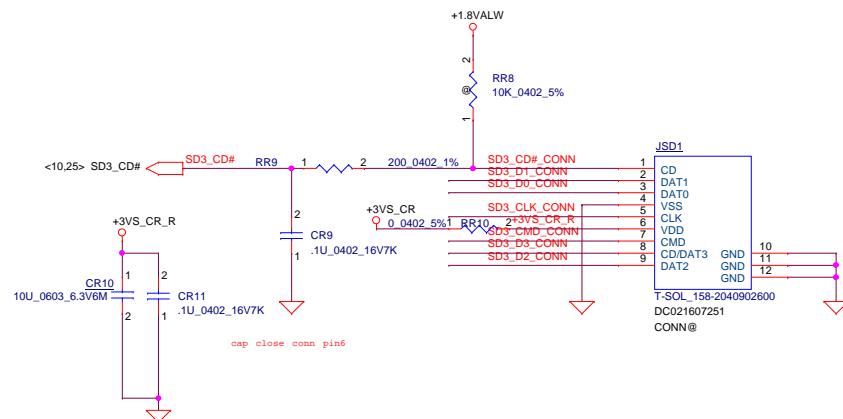
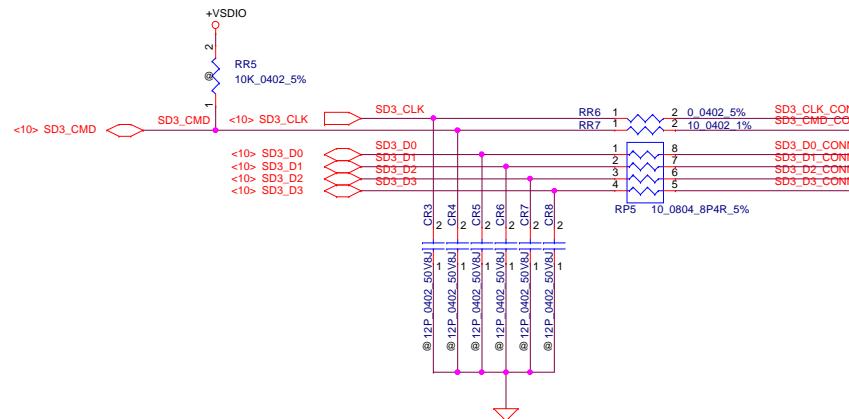
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Size	Document Number	Rev. 0.2		
	LA-E372P	Date: Thursday, July 28, 2016		
		Sheet 32 of 47		

CardReader

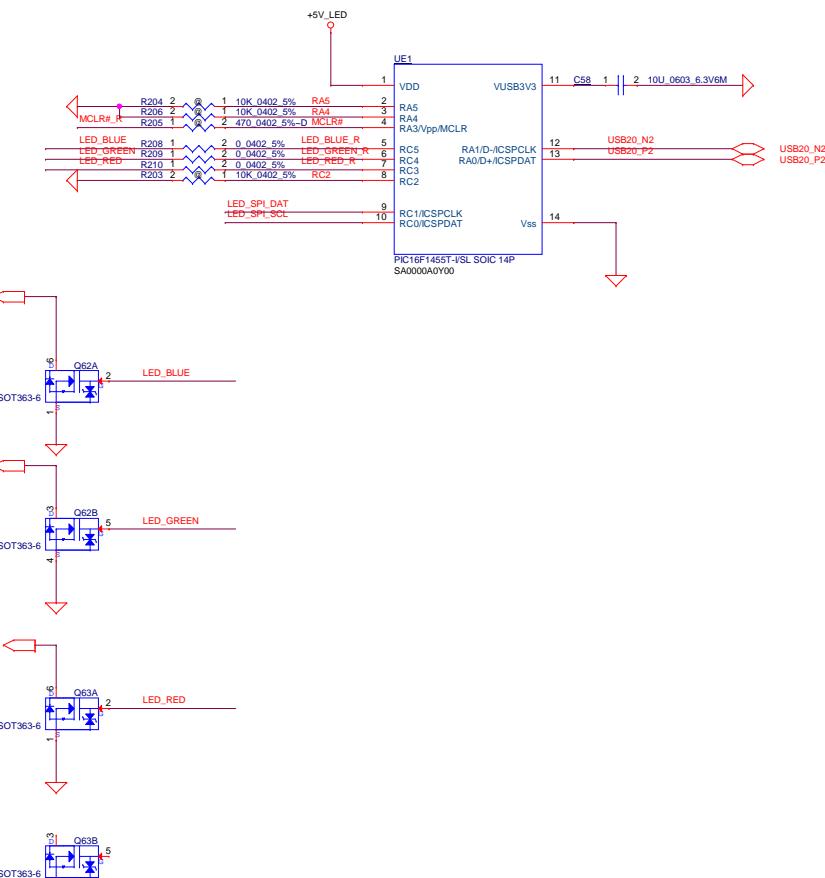
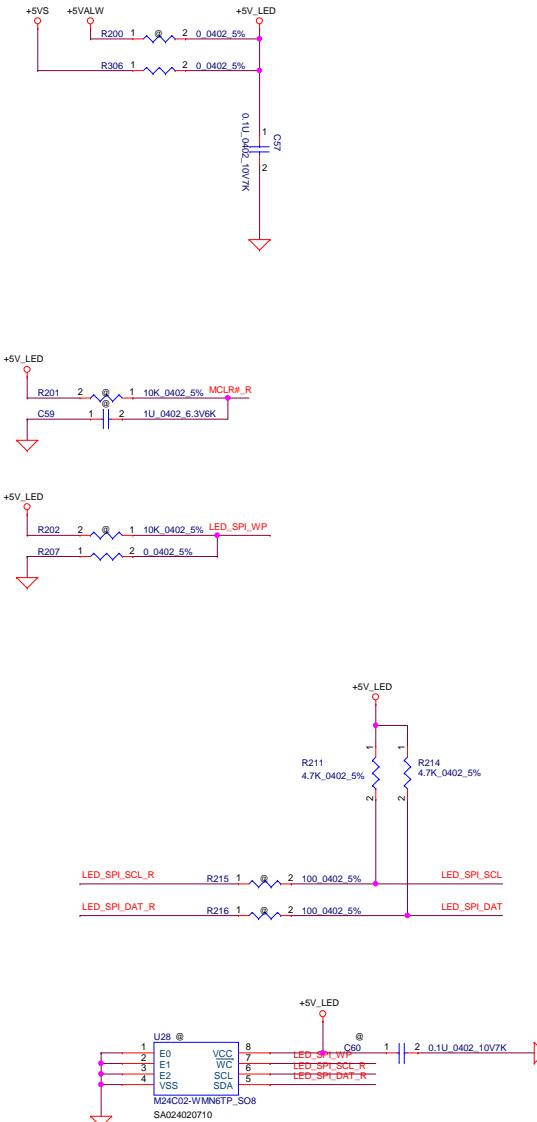
SDIO--->micro SD card



EN: Active high

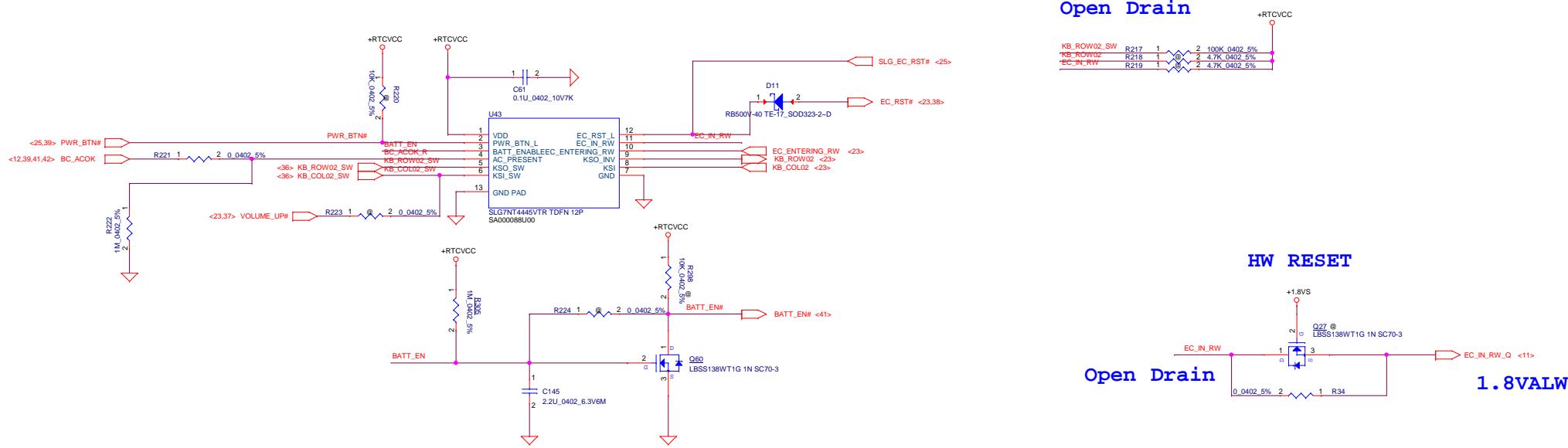


Main Func = LED PWM controller

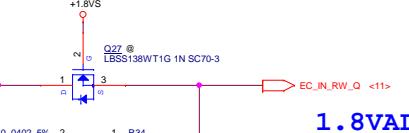


Only reserve connector footprint
Not pop connector for debug

Main Func = Holeless reset

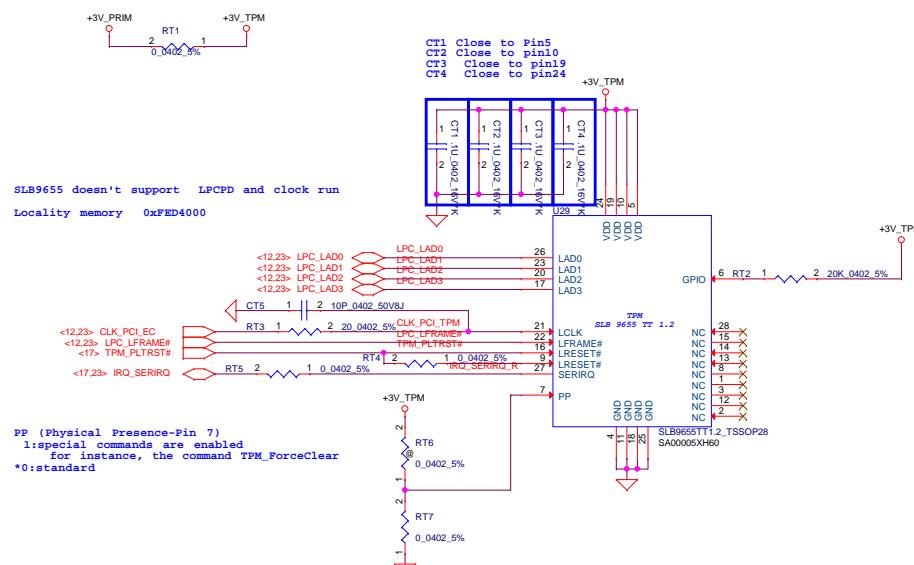


HW RESET



1.8VALW

Main Func = TPM

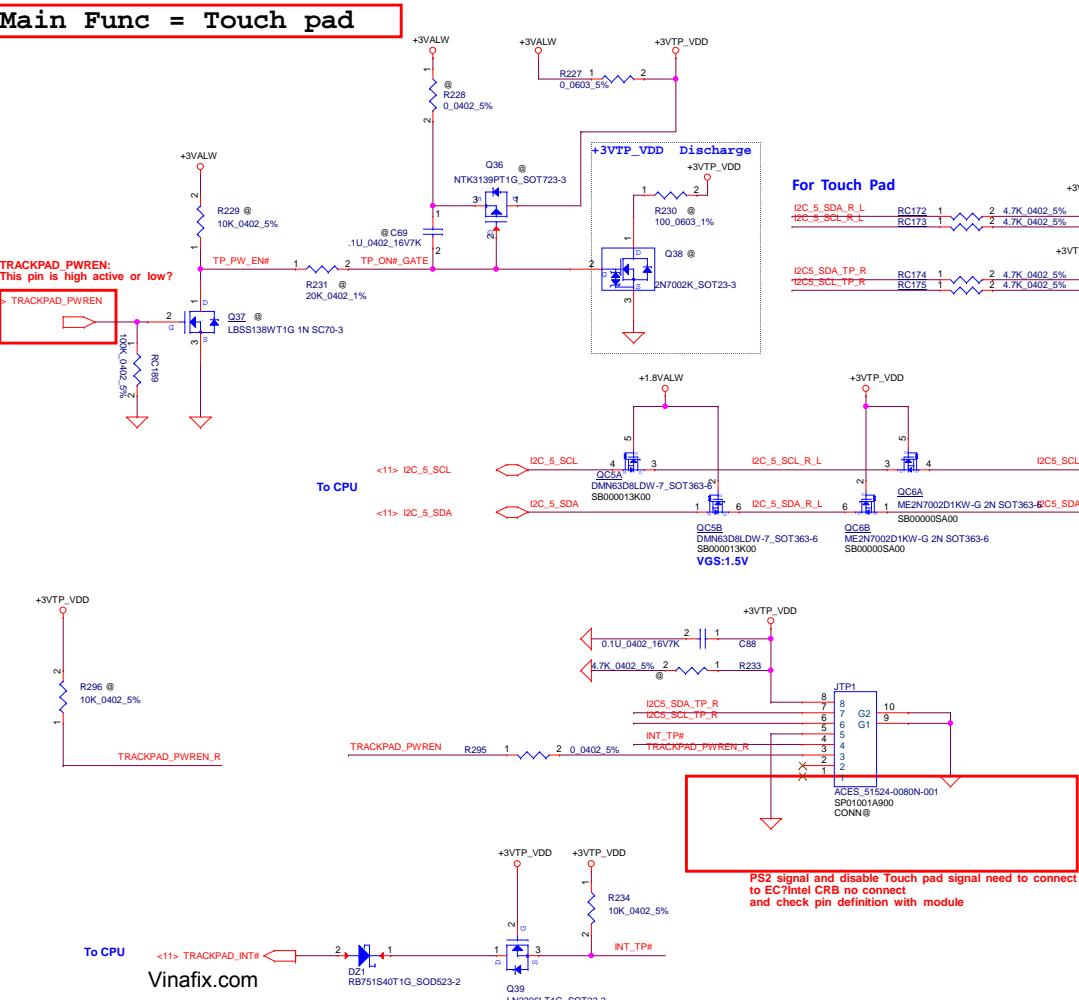


Main Func = LID switch

LID Switch(NB)



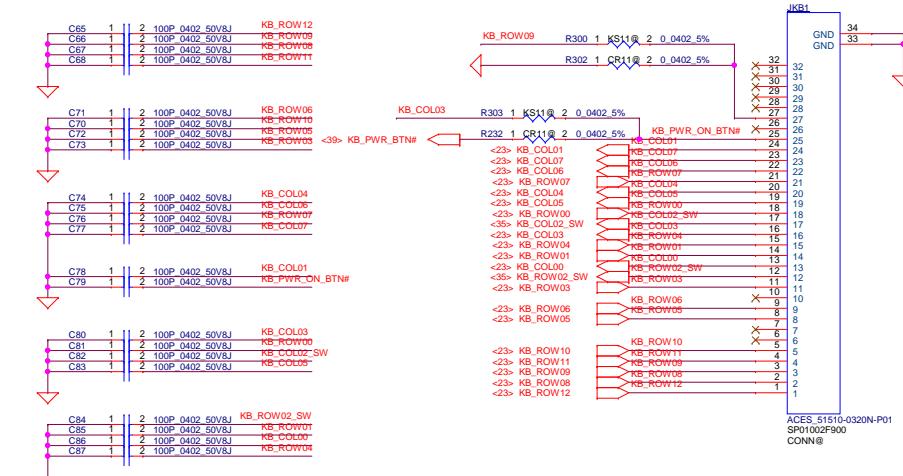
Main Func = Touch pad



PS2 signal and disable Touch pad signal need to connect to EC?Intel CRB no connect and check pin definition with module

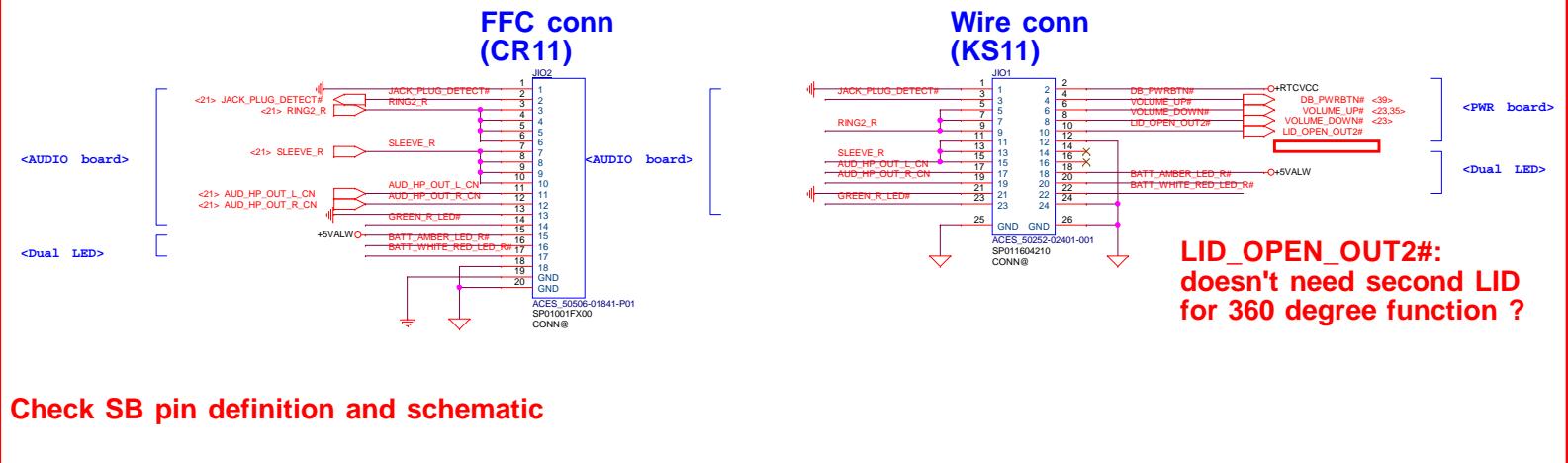
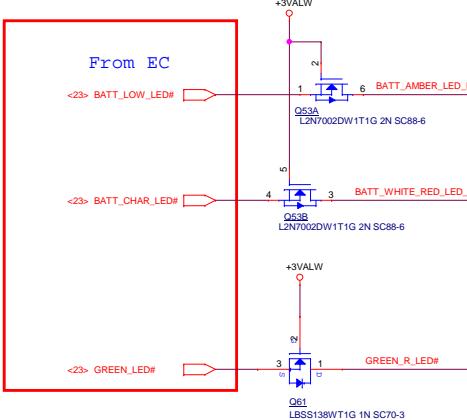
Vinafix.com

KBD Connector Have to change 04/21 Sam

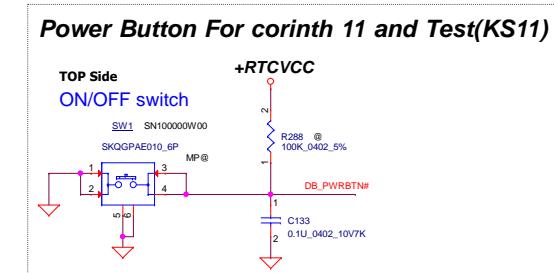


Event	PCH-TP_INT#	PCH-TP_INT#
S0	Interrupt	X
S3	X	Wake
1. Clamshell closed or Lid closed 2. Tablet mode for Convertible design 3. Disable TP function by ht-key	X	X

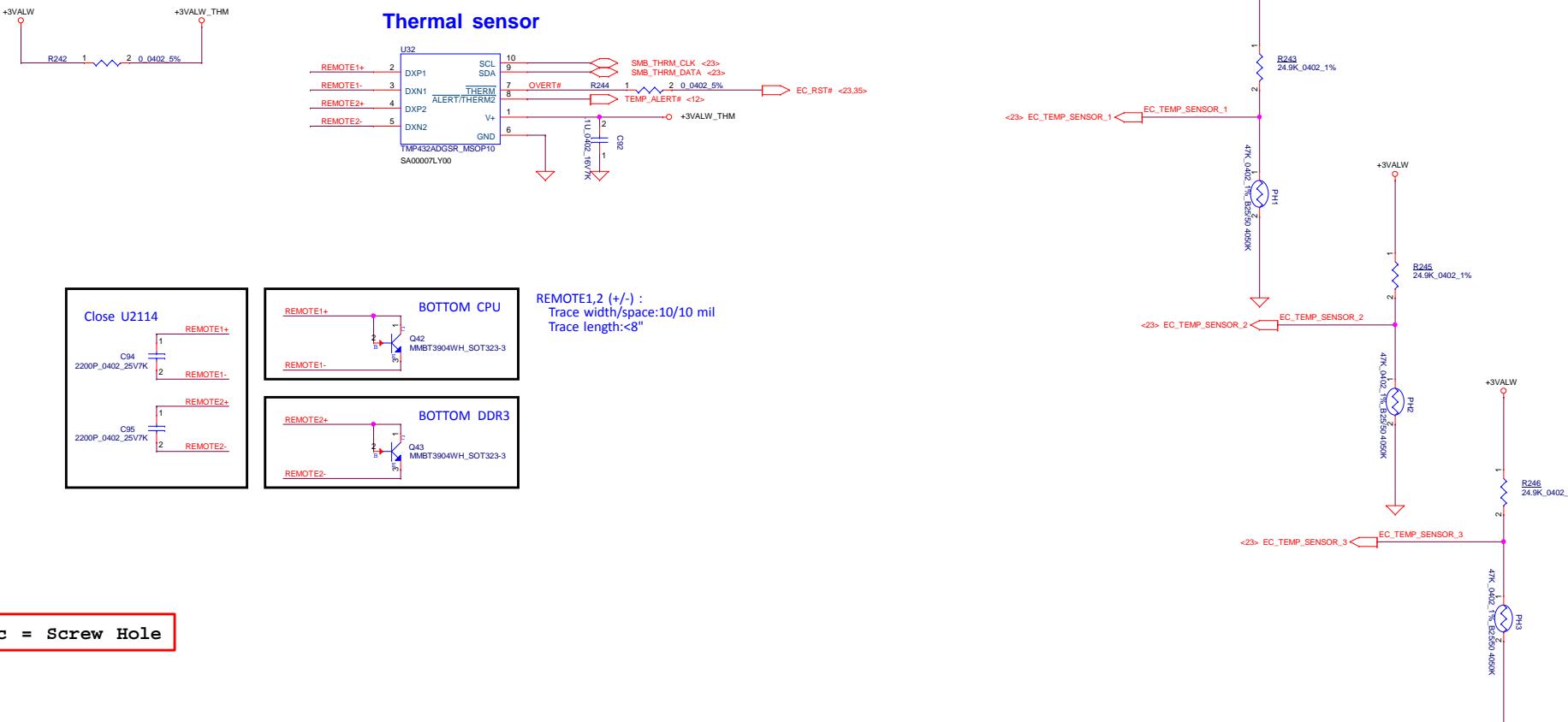
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	LA-E37P					
Date:	Sunday, July 17, 2016			Sheet	36	of 47



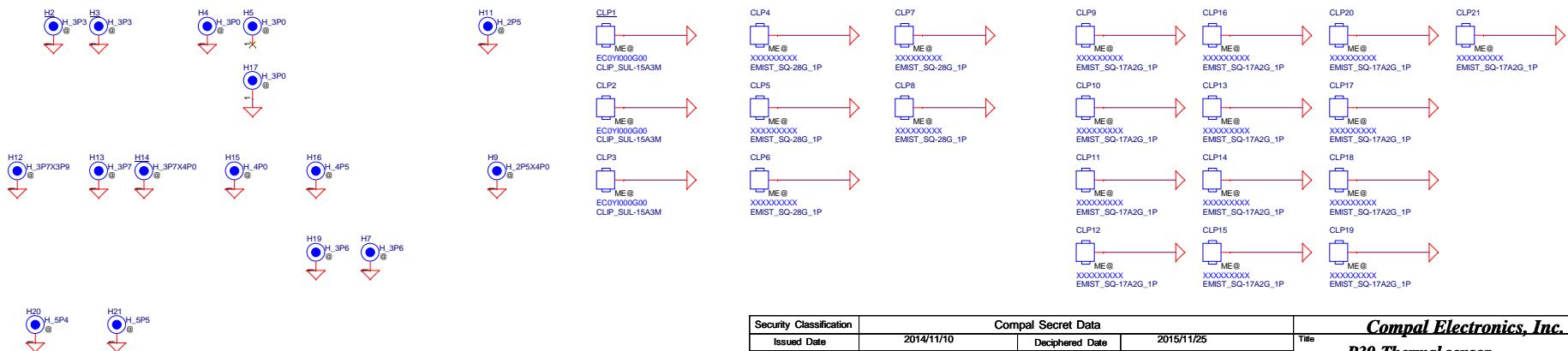
Check with EC which pin can connect



Main Func = Thermal



Main Func = Screw Hole



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Size	Document Number	Rev	
L4-E372P		0.2	
Date:	Monday, August 01, 2016	Sheet	38 of 47

For convertible Designs (power button on the side)
PWR_BTN_SELECT should not be controlled by EC

DB

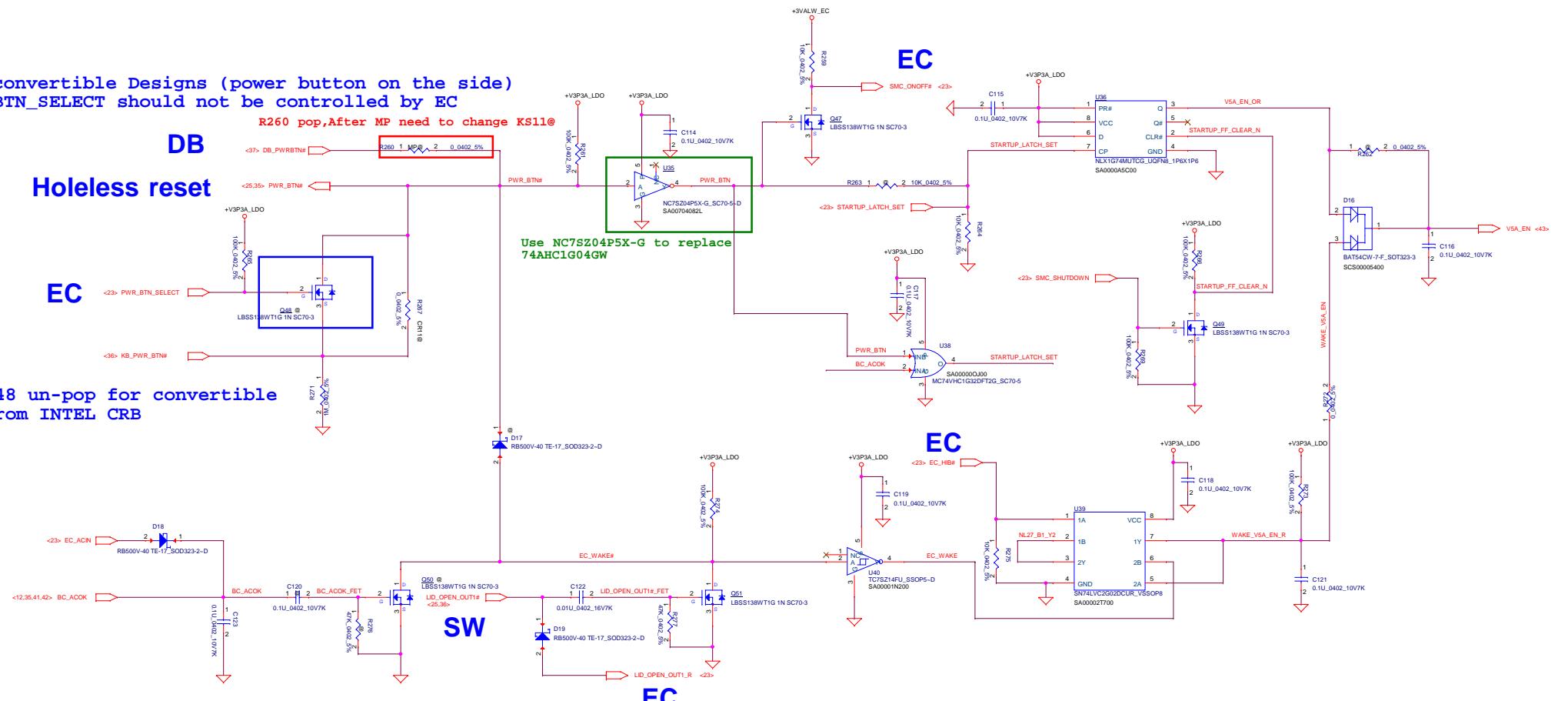
Holeless reset

EC

Q48 un-pop for convertible
from INTEL CRB

sw

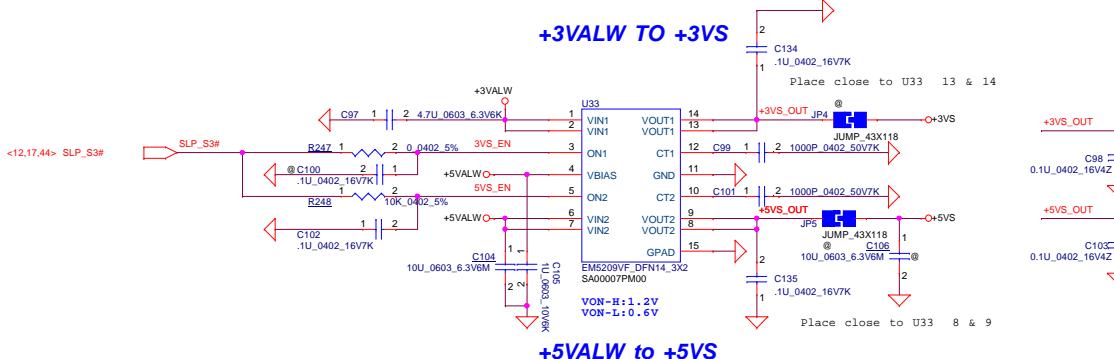
EC



Main Func = DC Interface

VS Power Gate

+3VALW TO +3V



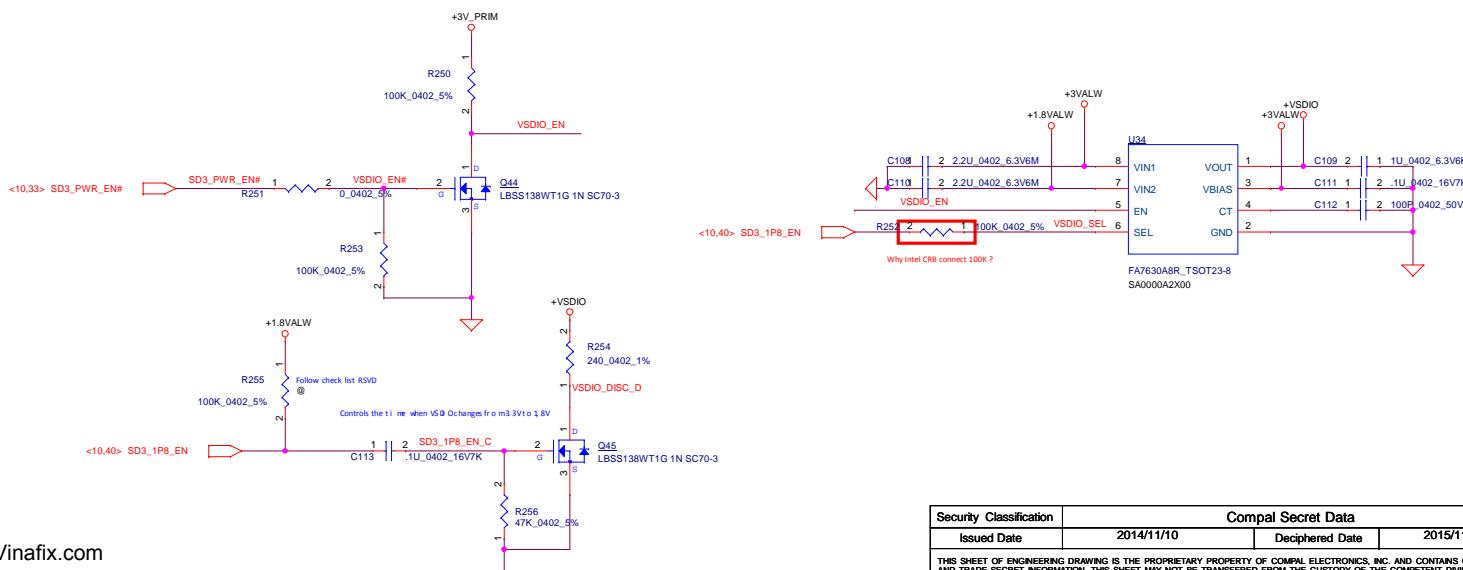
RTC CIRCUIT

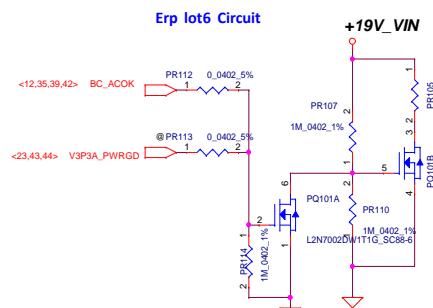
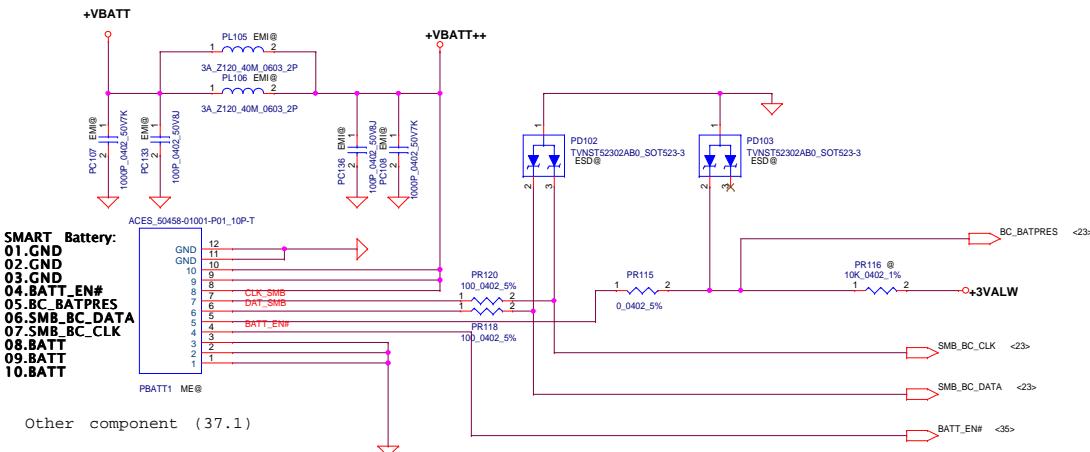
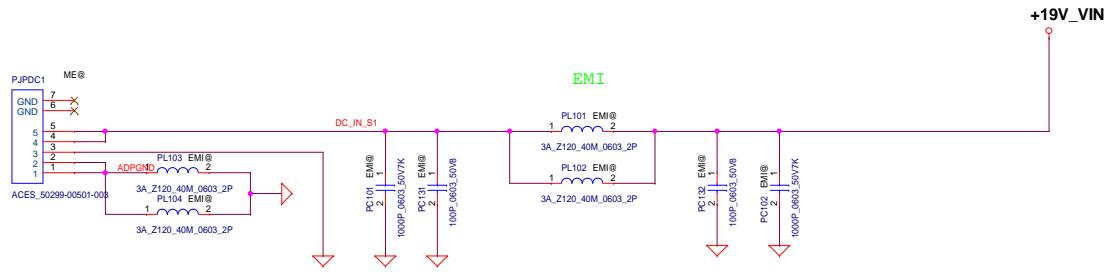


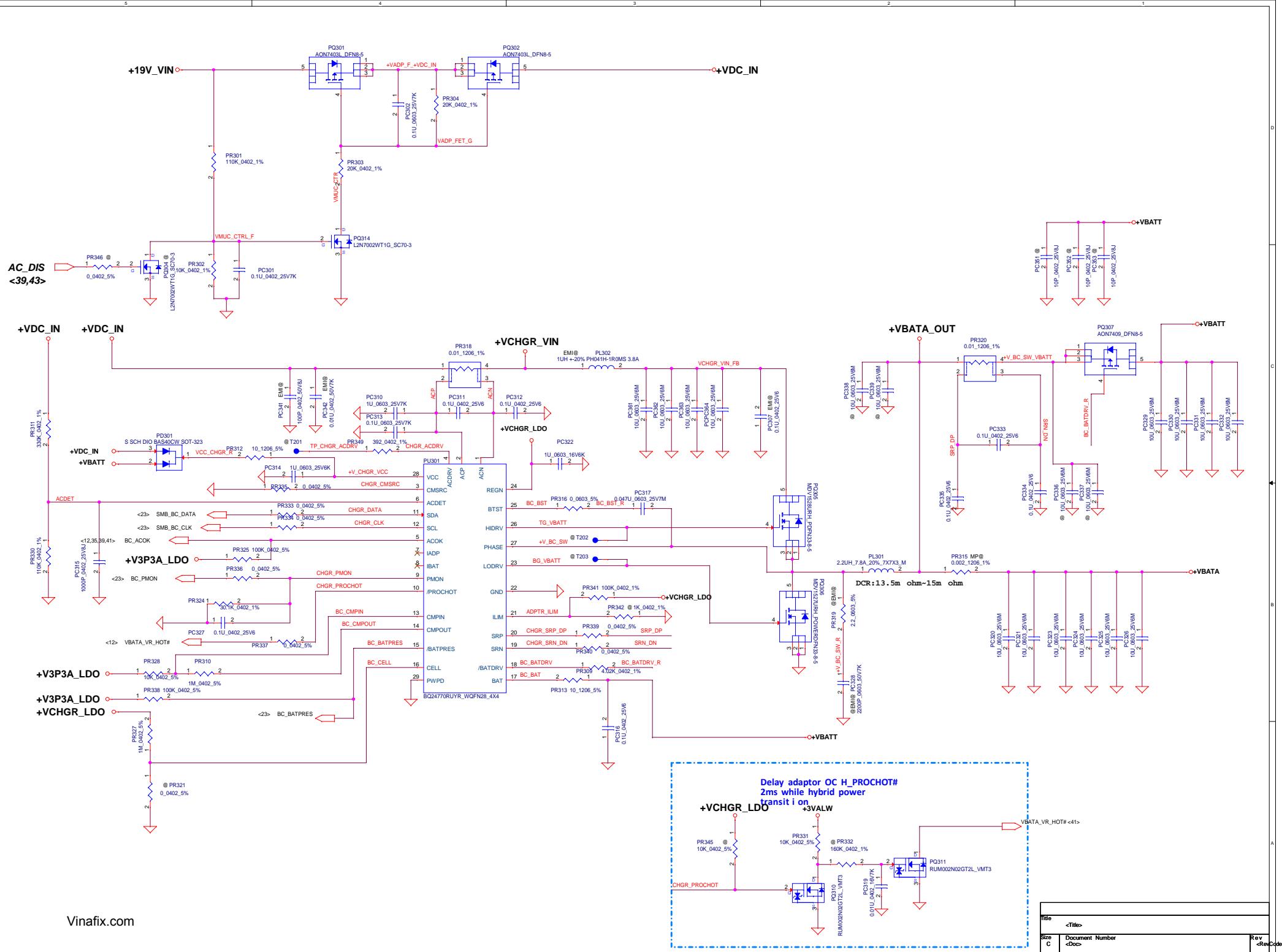
+VSDIO

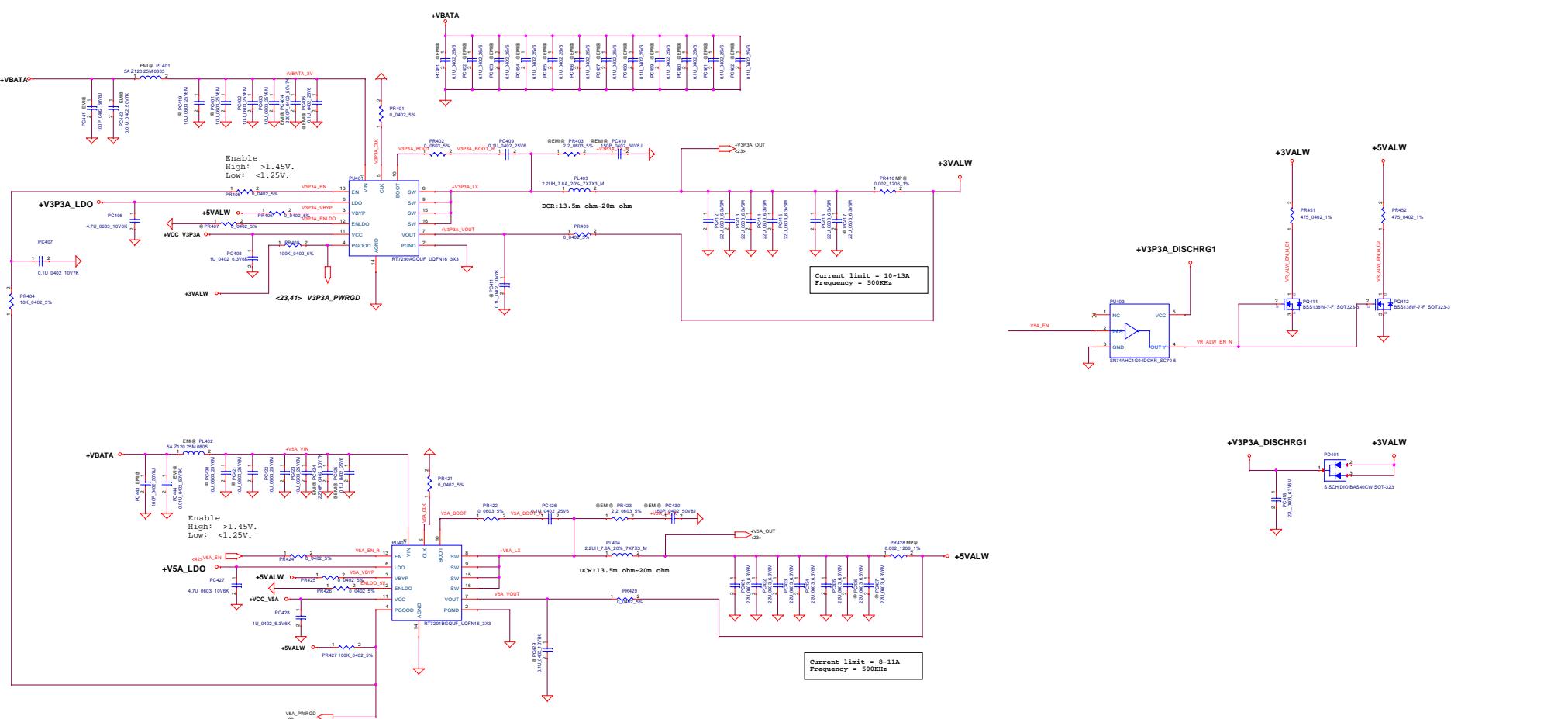
Table 22-5.VSDIO Voltage Setting

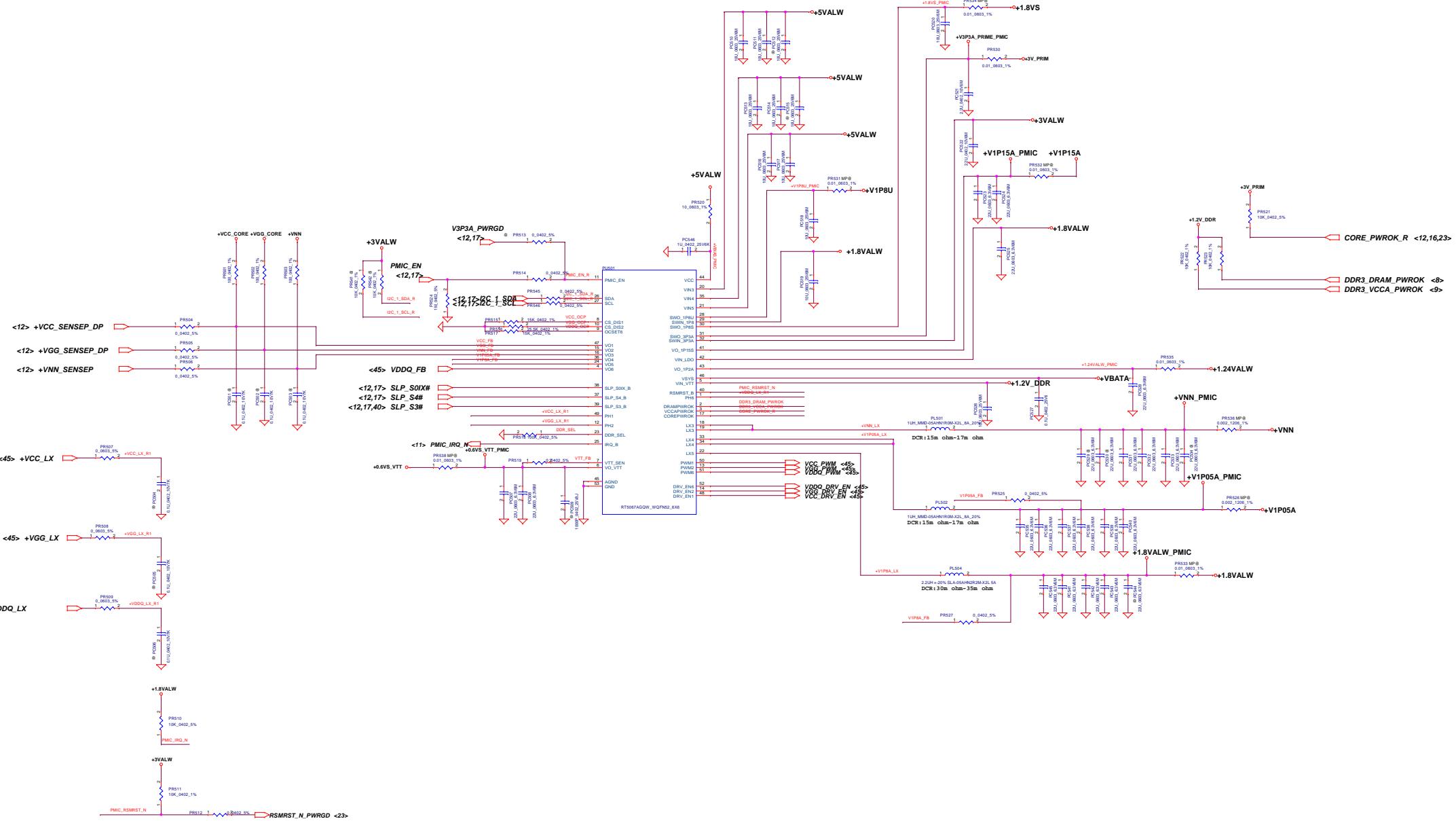
SDMMC3_PWR_EN_B	SDMMC3_1P8_EN	VSDIO(V)
1	0	0
1	1	0
0	0	3.3
0	1	1.8

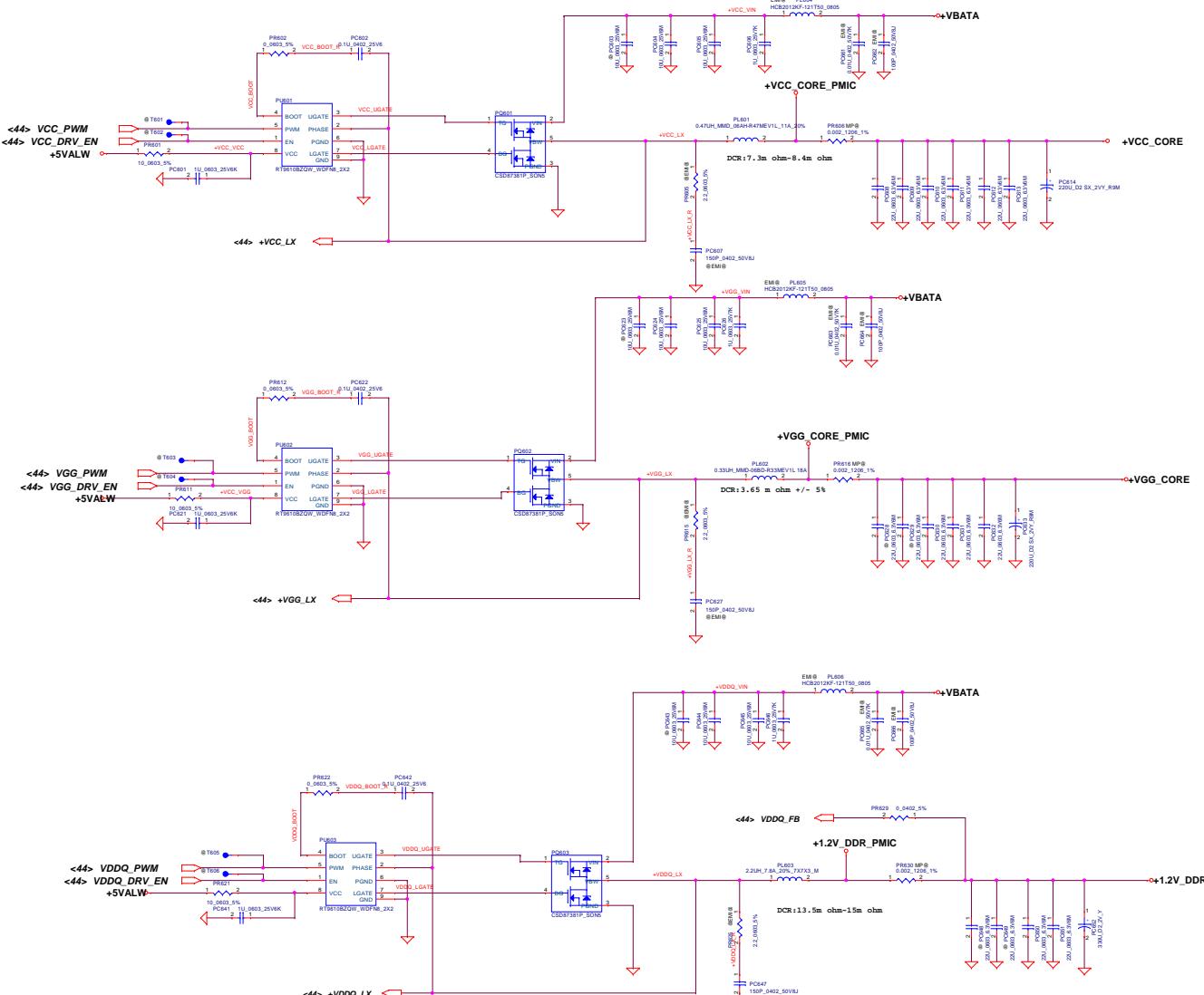




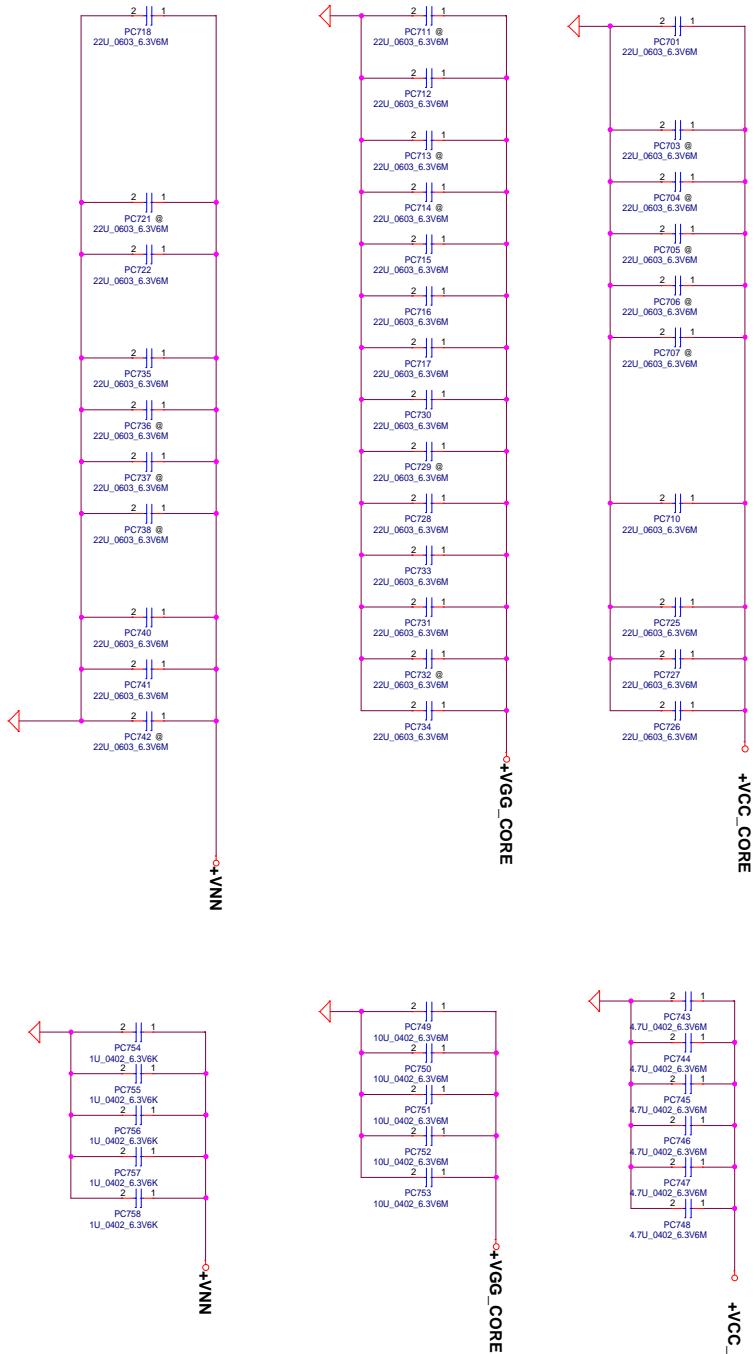








Rev	1	Document Number	00000000000000000000000000000000
Date	Wednesday, July 27, 2016	Sheet	45 of 48



Title	
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Document Number	
Size	
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Date:	Wednesday, JAN 27, 2016
Sheet	1
of	1
Rev.	97
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