

1. Schematic Page Description :

Origins Schematic Ver :

01

SoC I2C table

Function	Channel	Read	Write
NA	I2C0	0x?	
PMIC	I2C1	0x?	0x?
Audio codec	I2C4		
Track Pad	I2C5		
EC	I2C6		

EC SMBus/I2C table

Function	Channel	Address
Battery/charger	SMB0	
NA	SMB1	
PCH	I2C1	
NA	I2C2	
Thermal	I2C3	

Current sensor address

Function	Channel	Function	Channel
+VBATA	0x47	+VCC_OUT	0x40
+V5A	0x43	+VGG	0x44
+V3P3A	0x4B	+VNN	0x45
+V1P05A	0x46	+VDDQ_OUT	0x41
+V1P8A	0x49		

USB3/2 port mapping

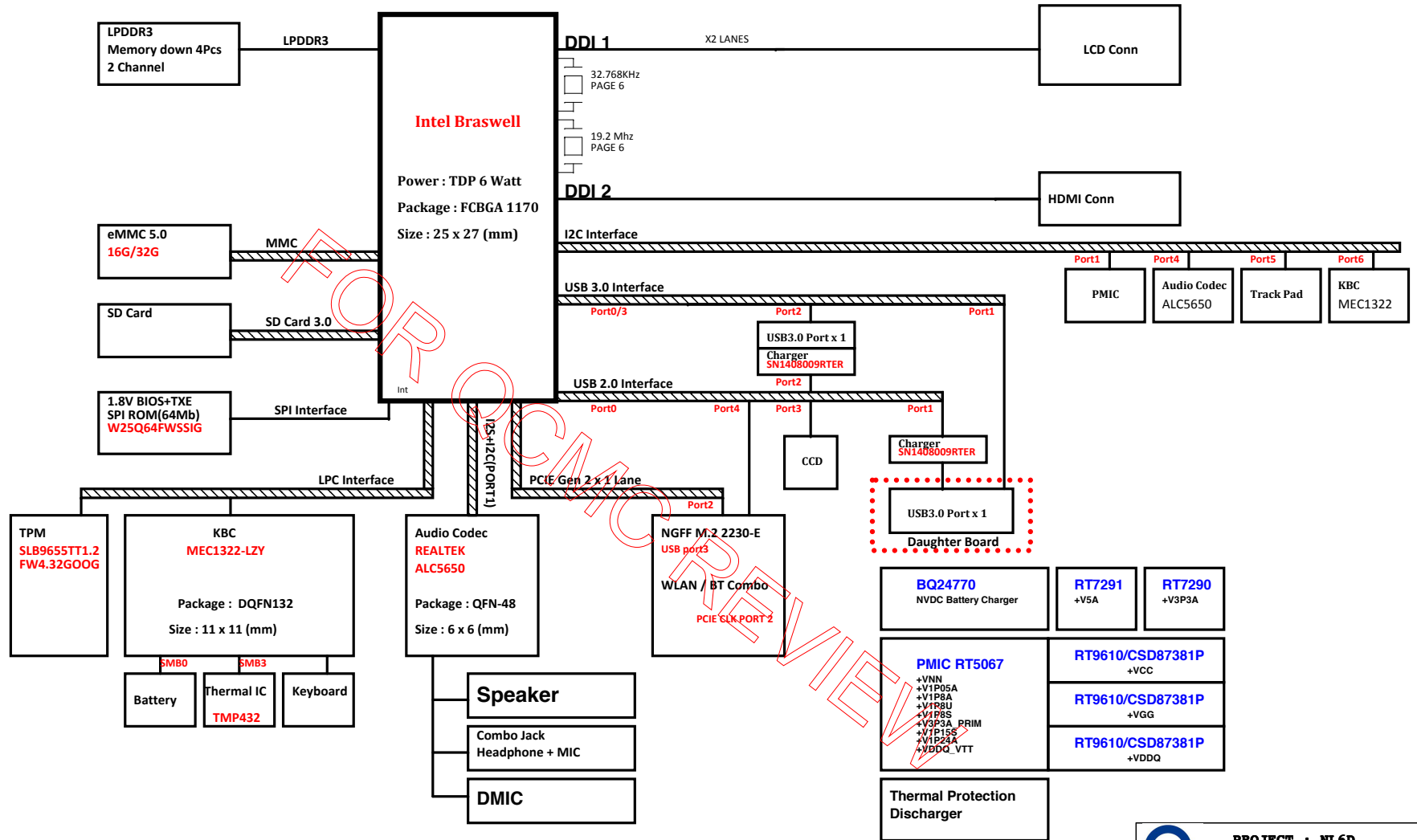
USB3 Port No#	Usage	USB2 Port No#	Usage
USB3P0	NA	USB2P0	NA
USB3P1	I/O	USB2P1	I/O(3.0)
USB3P2	I/O	USB2P2	I/O(3.0)
USB3P3	NA	USB2P3	CCD
		USB2P4	BT

PCIe port mapping

PCIe port No#	Usage	PCIe CLK#	Usage
PCIe_0	NA	PCIe_CLK0	NA
PCIe_1	NA	PCIe_CLK1	NA
PCIe_2	WLAN	PCIe_CLK2	WLAN
PCIe_3	NA	PCIe_CLK3	NA

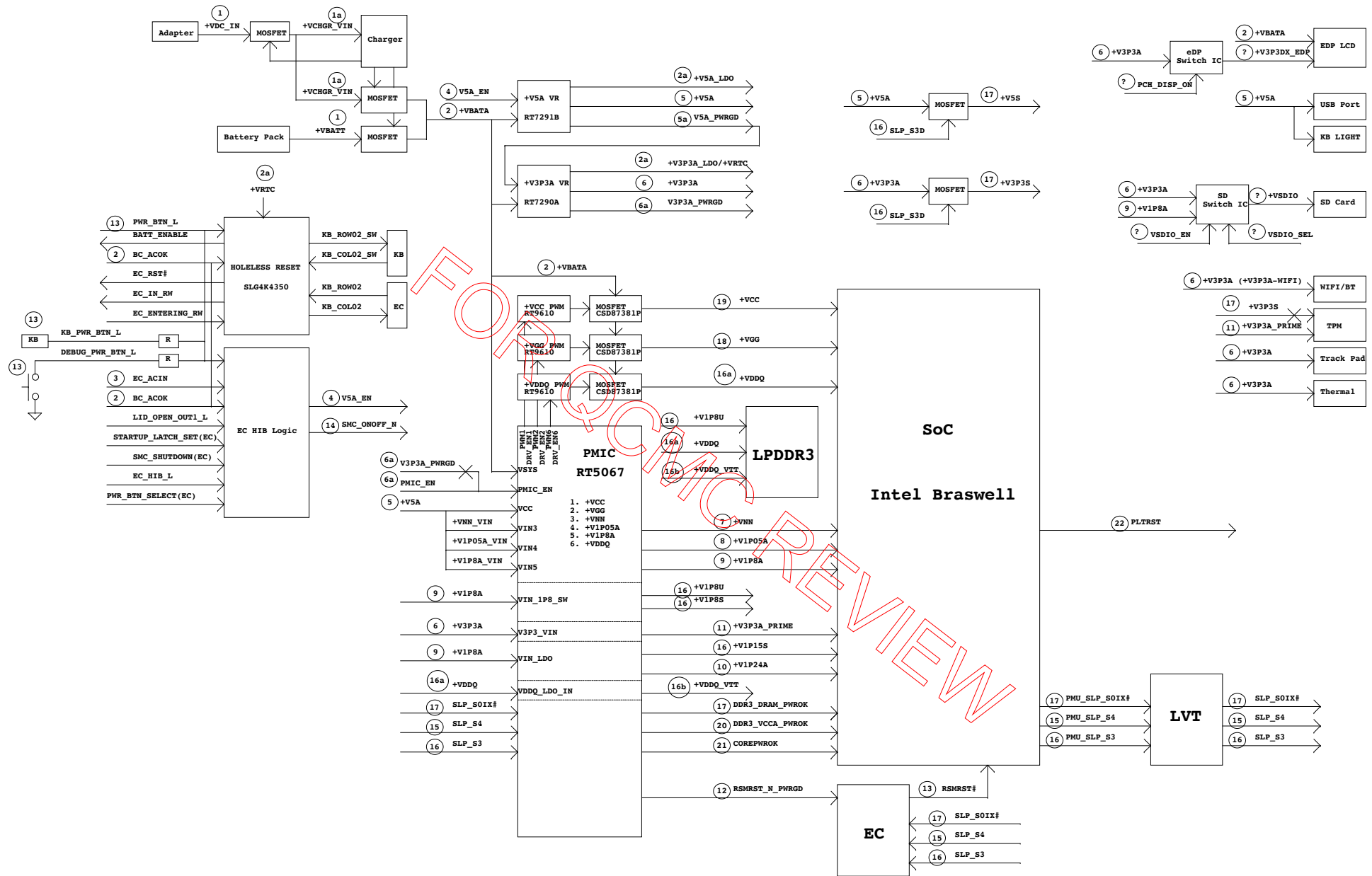
NL6D Chromebook

Intel Braswell Platform Block Diagram



FOR QCMC REVIEW

FOR QCMC REVIEW



BRASWELL SOC - MEMORY LPDDR3 CHANNEL A

06

SoC (CPU)

BSW_MCP_EDS

U17A

[39] DDR3_DRAM_PWROK

PLACE CA CAP NEAR SOC

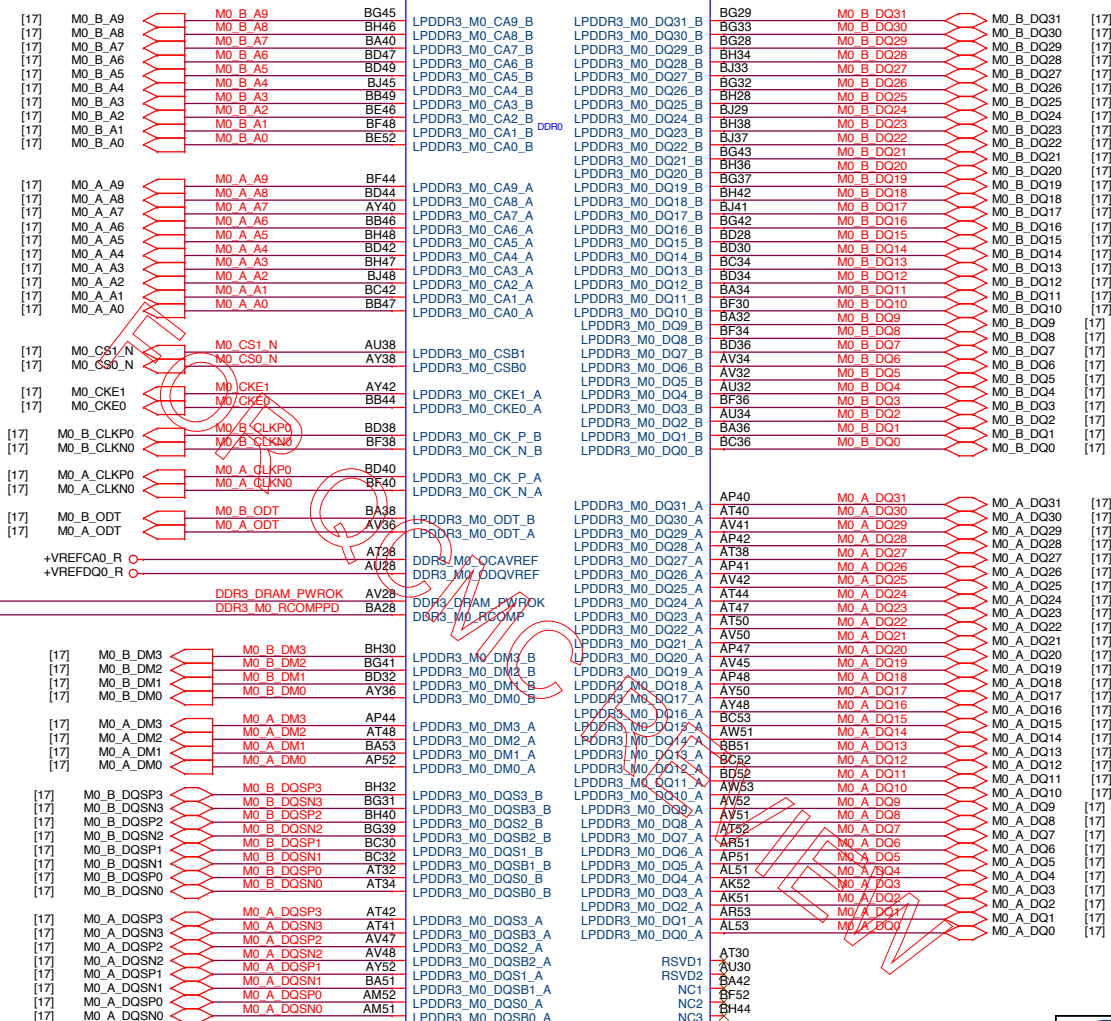
CA

C234

0.1U/16V_4

R403

182F_4



BSW_MCP_EDS

REV=1

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?

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BSW 1/10 (DDR4)

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Rev 1A

07

BSW_MCP_EDS



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3



BRASWELL SOC - DISPLAY, XDP, EMMC, SD

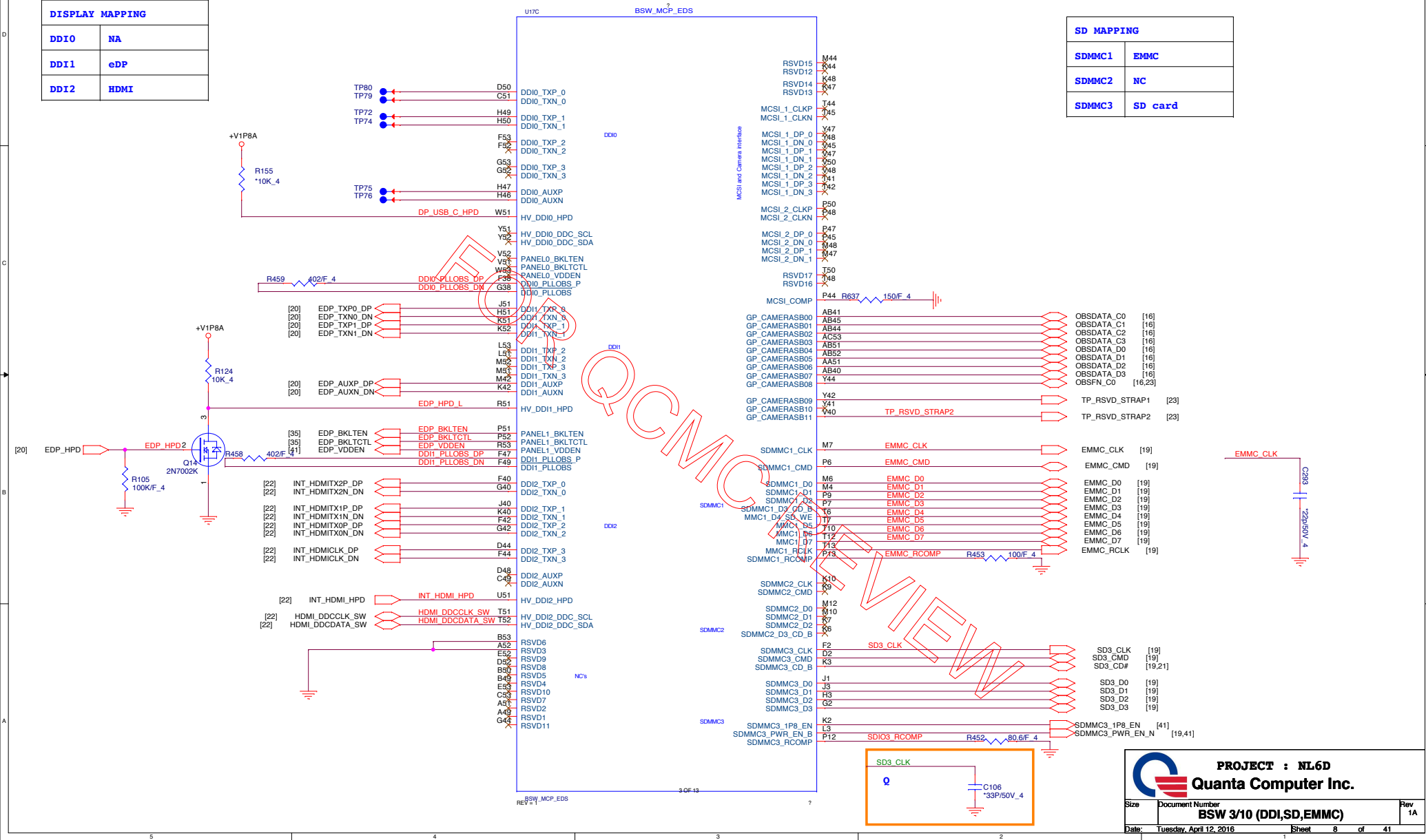
SoC (CPU)

DISPLAY MAPPING

DDI0	NA
DDI1	eDP
DDI2	HDMI

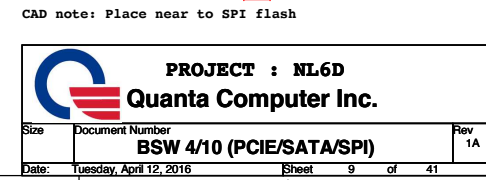
SD MAPPING

SDMMC1	EMMC
SDMMC2	NC
SDMMC3	SD card

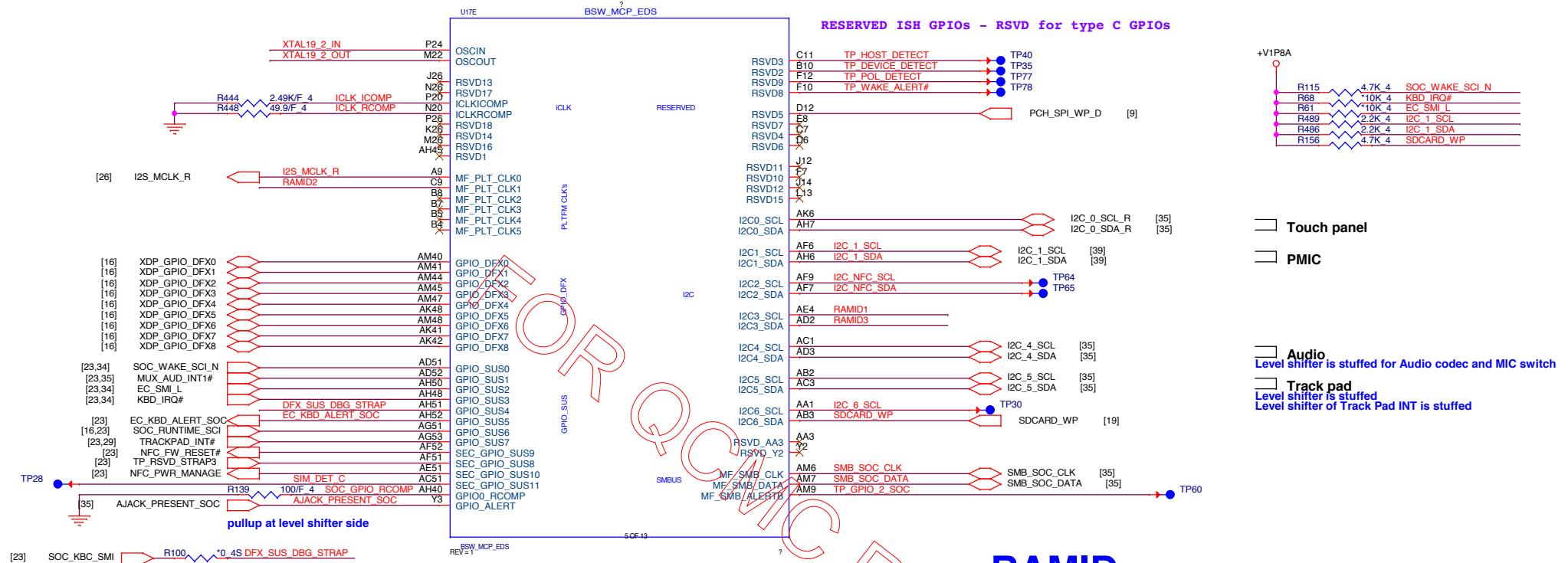


09

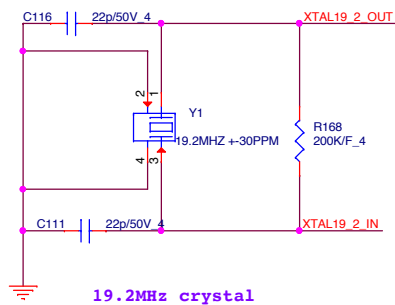
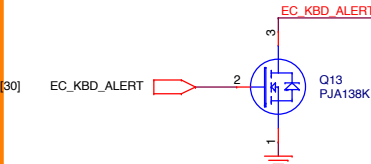
PCIe MAPPING	
PCIE0	NC
PCIE1	NC
PCIE2	WIFI (StP)
PCIE3	NC



SoC (CPU) BRASWELL - I2C, XDP, SM BUS

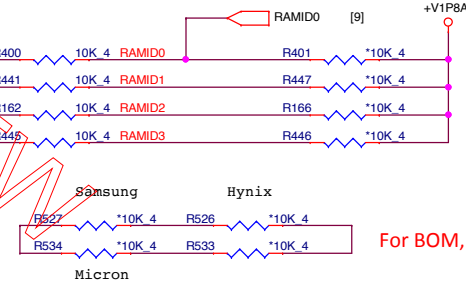


19.2MHz X'tal

0312 added KBD_ALERT pin to notify SoC to lock ME FW
Keep reserving this feature in DVT build

Vender	RAM_ID3	RAM_ID[2..0]	Q PN	Mfr. PN	Freq.	Size	Total Size
Samsung	0 (1-CH)	000	AKD5QWST508	K4E8E304EE-EGCF	1866MHz	4Gb	2Gb
Hynix	0 (1-CH)	001	AKD5RW0TW53	H9CCNNN8GTMLAR-NUD	1866MHz	4Gb	2Gb
Micron	0 (1-CH)	010	AKD5QWSTL01	MT52L256M32D1PF-107	1866MHz	4Gb	2Gb
Samsung	0 (1-CH)	011	AKD5QWST521	K4E8E324EB-EGCF	1866MHz	4Gb	2Gb
Micron	0 (1-CH)	100	AKD5QWWT401	EDF8132A3MA-JD-F-R	1866MHz	4Gb	2Gb
Samsung	1 (2-CH)	000	AKD5QWST508	K4E8E304EE-EGCF	1866MHz	4Gb	4Gb
Hynix	1 (2-CH)	001	AKD5RW0TW53	H9CCNNN8GTMLAR-NUD	1866MHz	4Gb	4Gb
Micron	1 (2-CH)	010	AKD5QWSTL01	MT52L256M32D1PF-107	1866MHz	4Gb	4Gb
Samsung	1 (2-CH)	011	AKD5QWST521	K4E8E324EB-EGCF	1866MHz	4Gb	4Gb
Micron	1 (2-CH)	100	AKD5QWWT401	EDF8132A3MA-JD-F-R	1866MHz	4Gb	4Gb

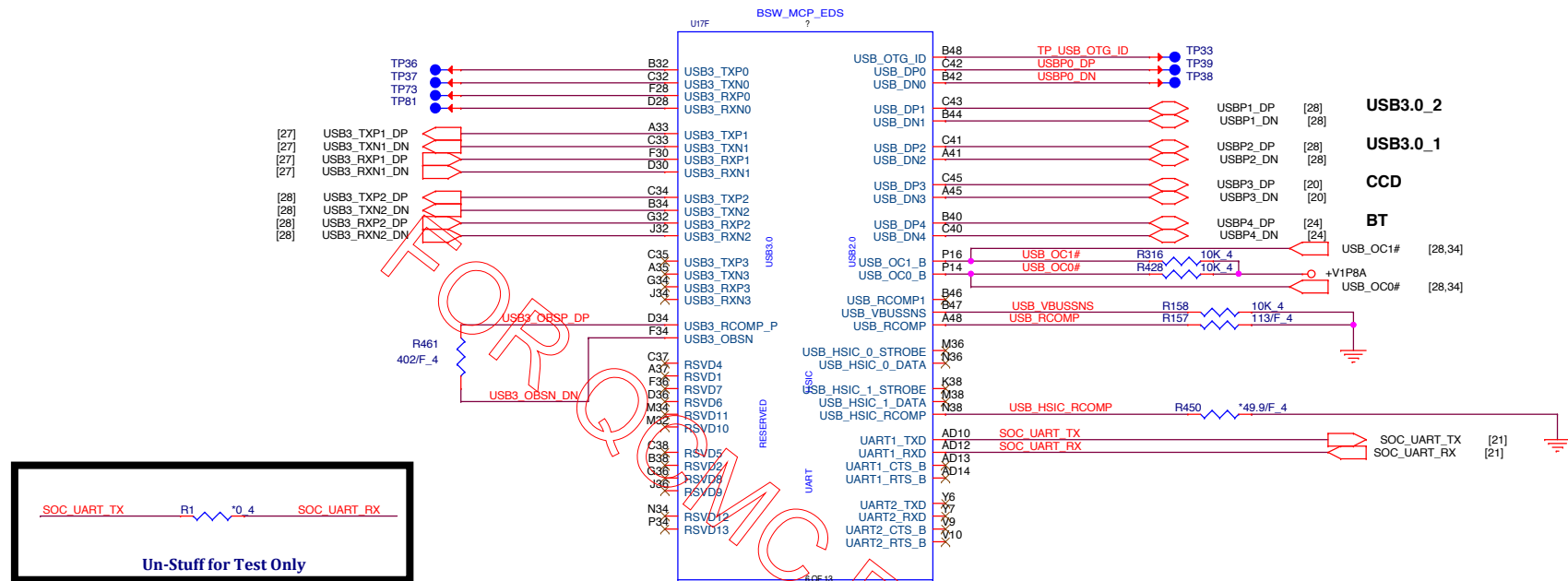
RAMID



BRASWELL - USB INTERFACE

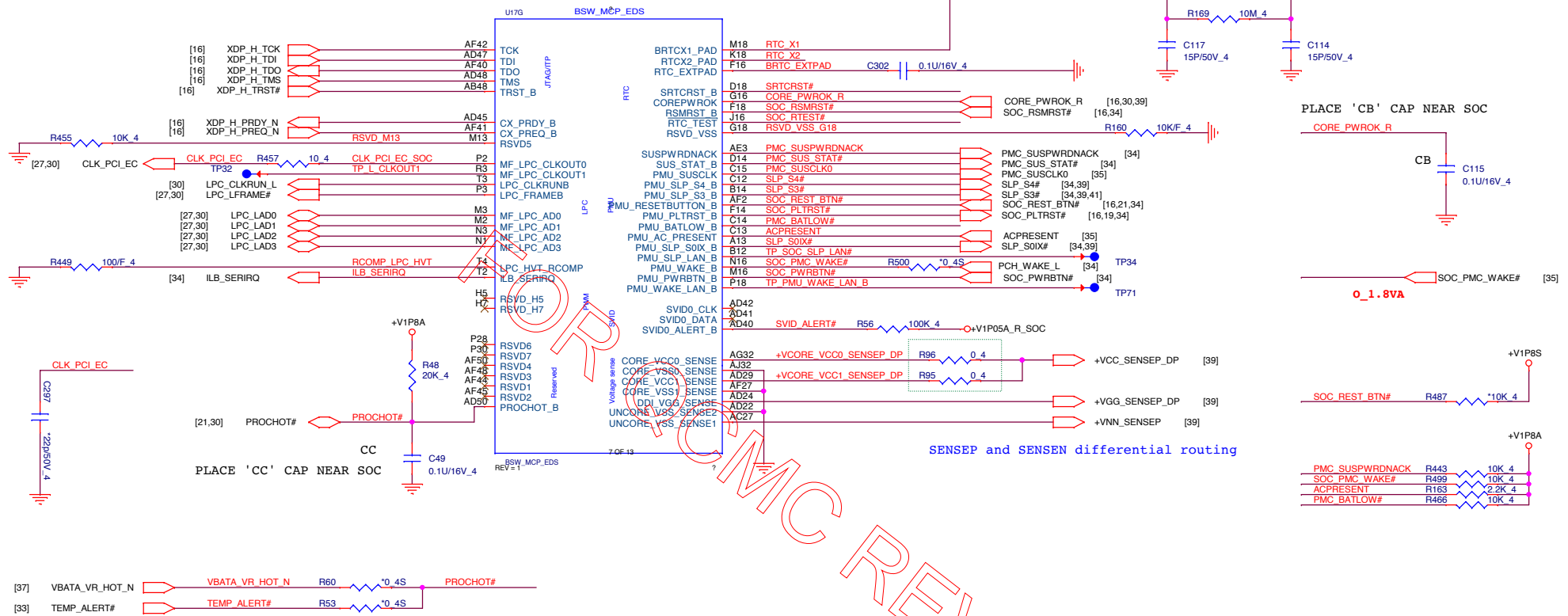
11

SoC (CPU)

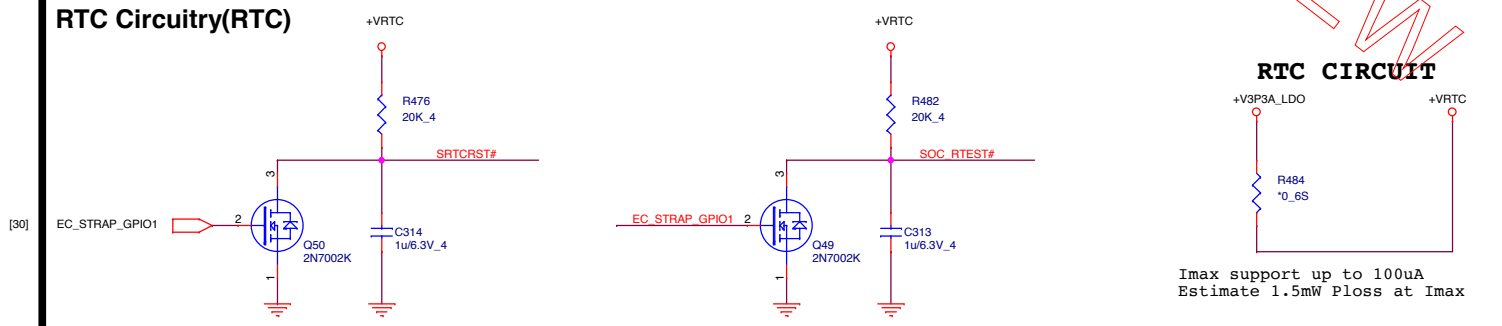


BRASWELL - JTAG, LPC, THERMAL, PMU

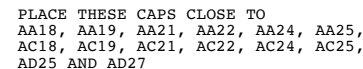
SoC (CPU)



RTC Circuitry(RTC)



Imax support up to 100uA
Estimate 1.5mW Ploss at Imax



PLACE THESE CAPS CLOSE TO
V33, AA32, AA33, AA35, AA36,
AC32, Y30, Y32, Y33 AND Y35

PLACE THIS CAP CLOSE TO V19 AND V18

PLACE THESE CAPS CLOSE TO
AM21, AM33, AM22, AN22, AN32
AND AM32

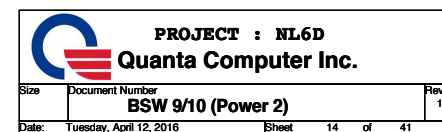
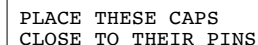
PLACE THESE CAPS CLOSE TO
V22, V24, U24, U22, V27 AND U27

PLACE THIS
CAP CLOSE TO
N18

PLACE THESE CAPS CLOSE TO U19

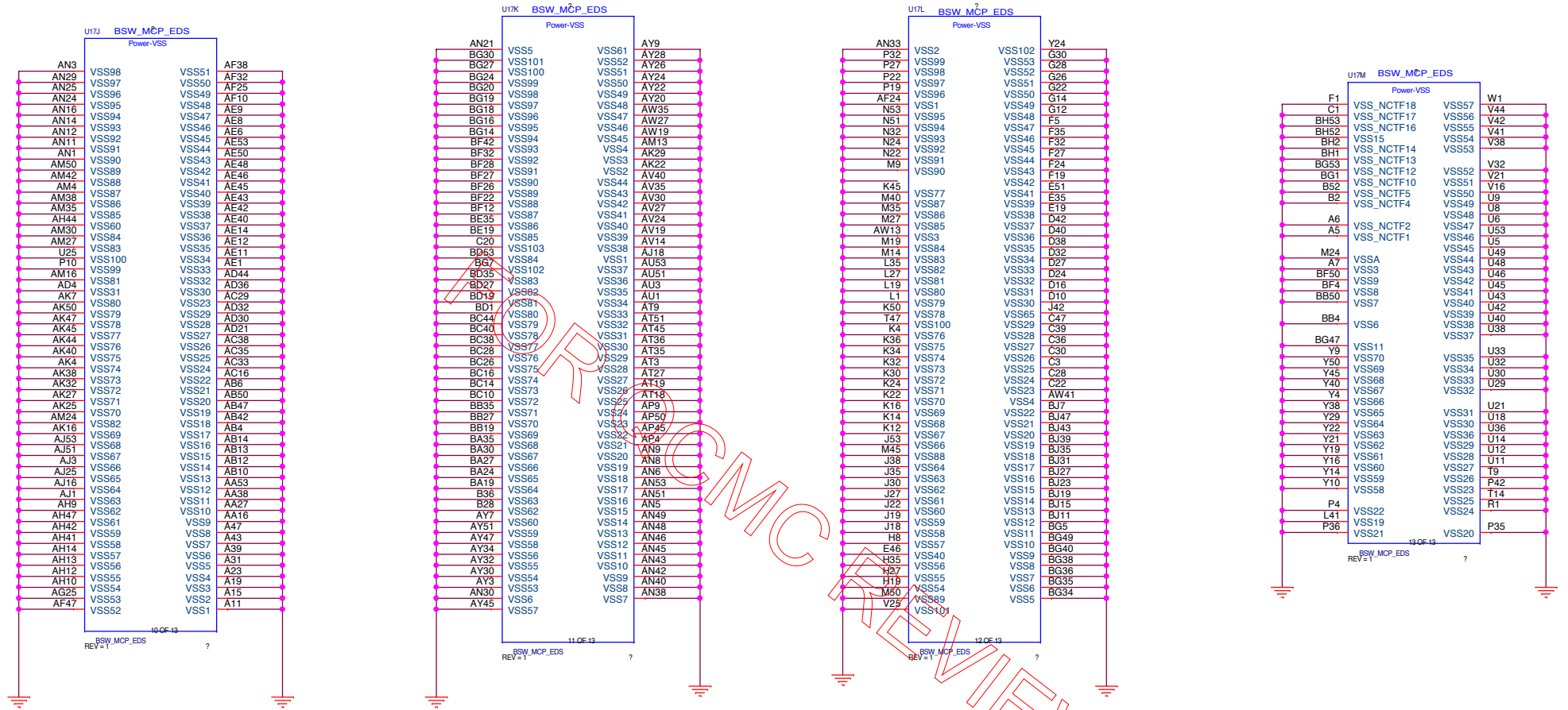
DUMMY CAPS. TO BE DELETED IN NEXT REVISION

CAD NOTE: PLACE CLOSE TO PIN AM21,
AM33, AM22, AN22, AN32 AND AM32 POWER PLANE



BRASWELL - GND

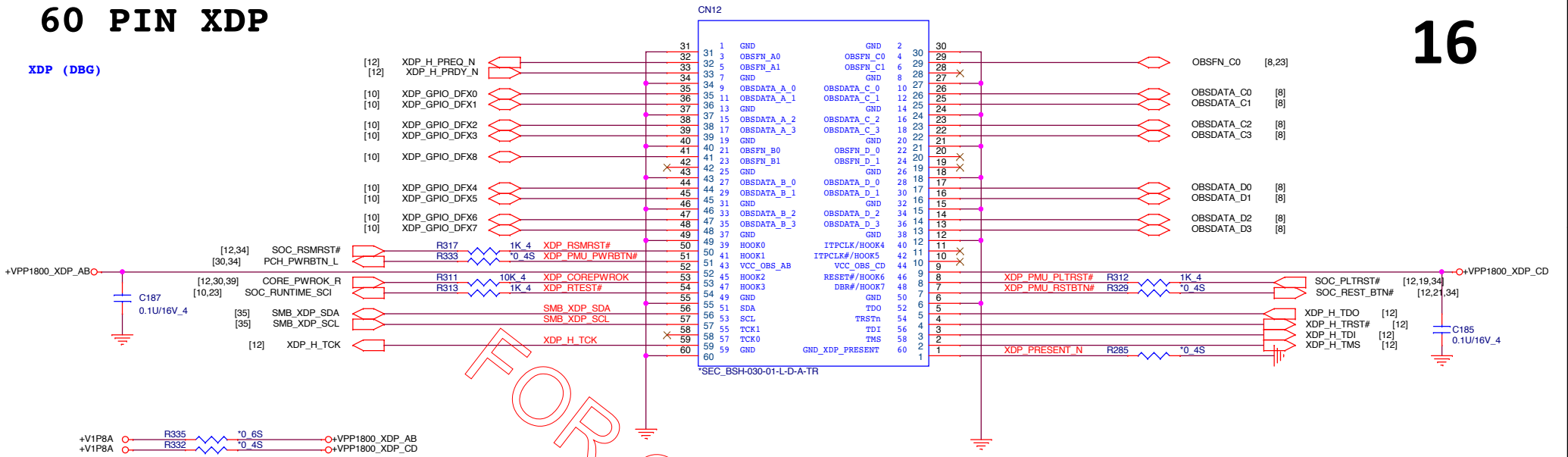
15



60 PIN XDP

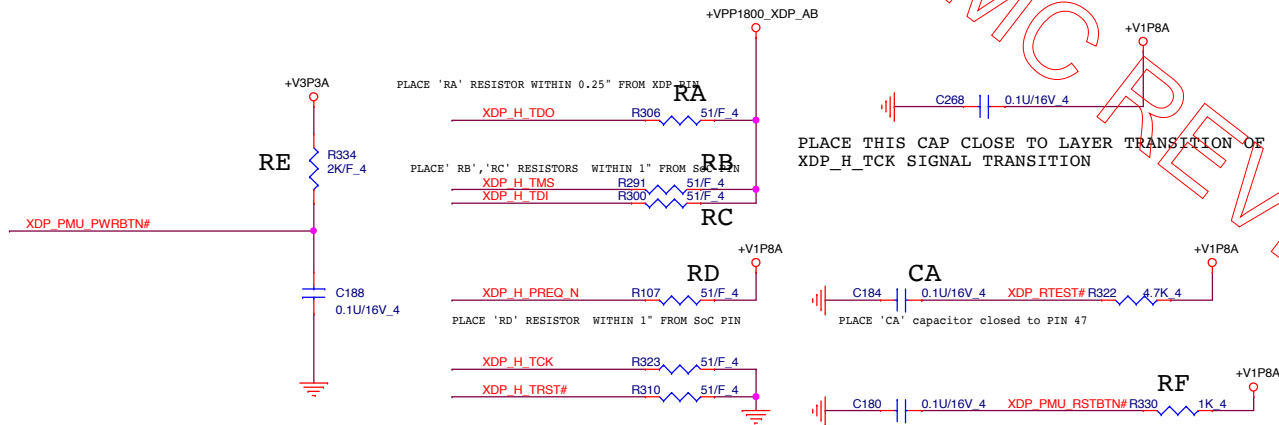
16

XDP (DBG)



PULL-UPS AND DOWNS FOR XDP SIGNALS

APS

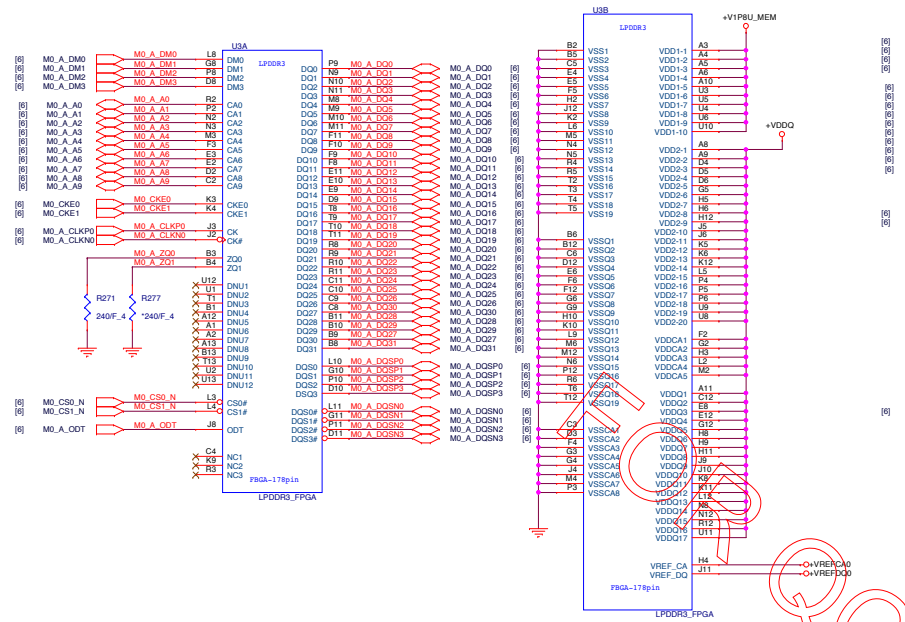


In reference board, RE is 2K and RF is stuffed

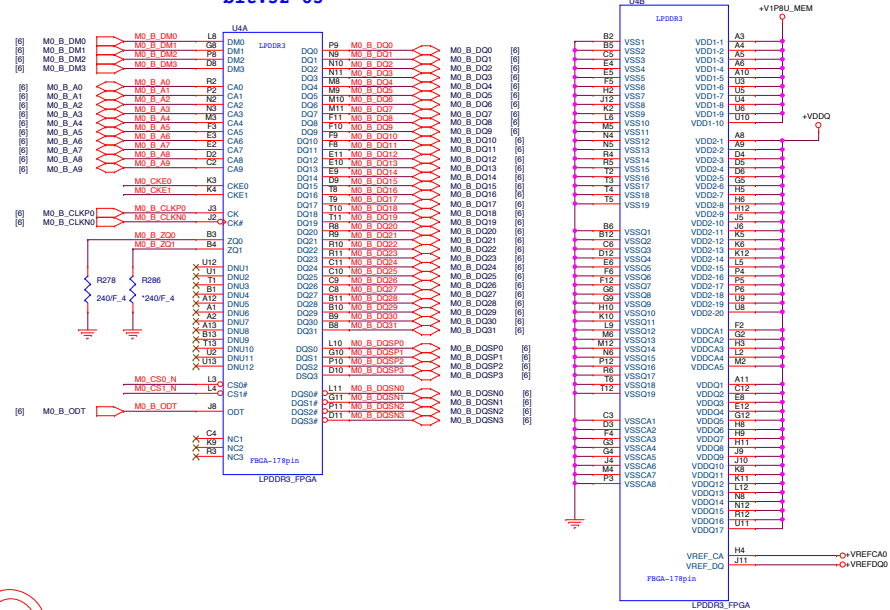
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Quanta Computer Inc.

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bit:0-31



bit:32-63

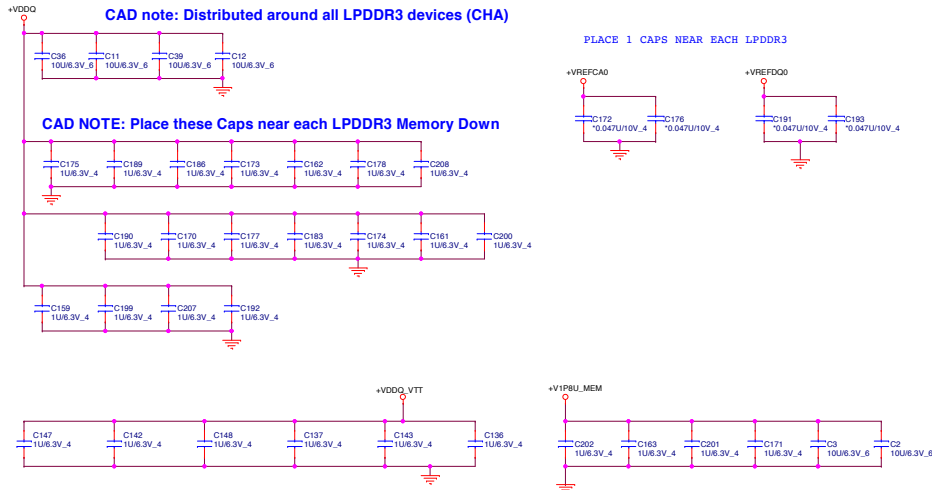


DE-CAPS FOR MEMORY CHANNEL A

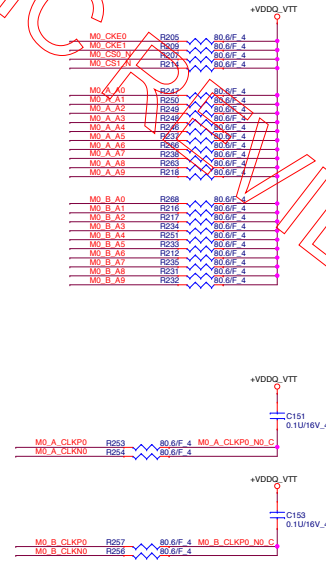
CAD note: Distributed around all LPDDR3 devices (CHA)

PLACE 1 CAPS NEAR EACH LPDDR3

CAD NOTE: Place these Caps near each LPDDR3 Memory Down



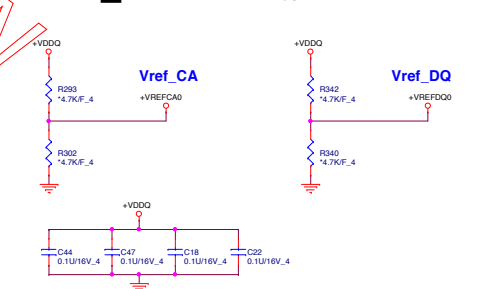
VTT TERMINATIONS



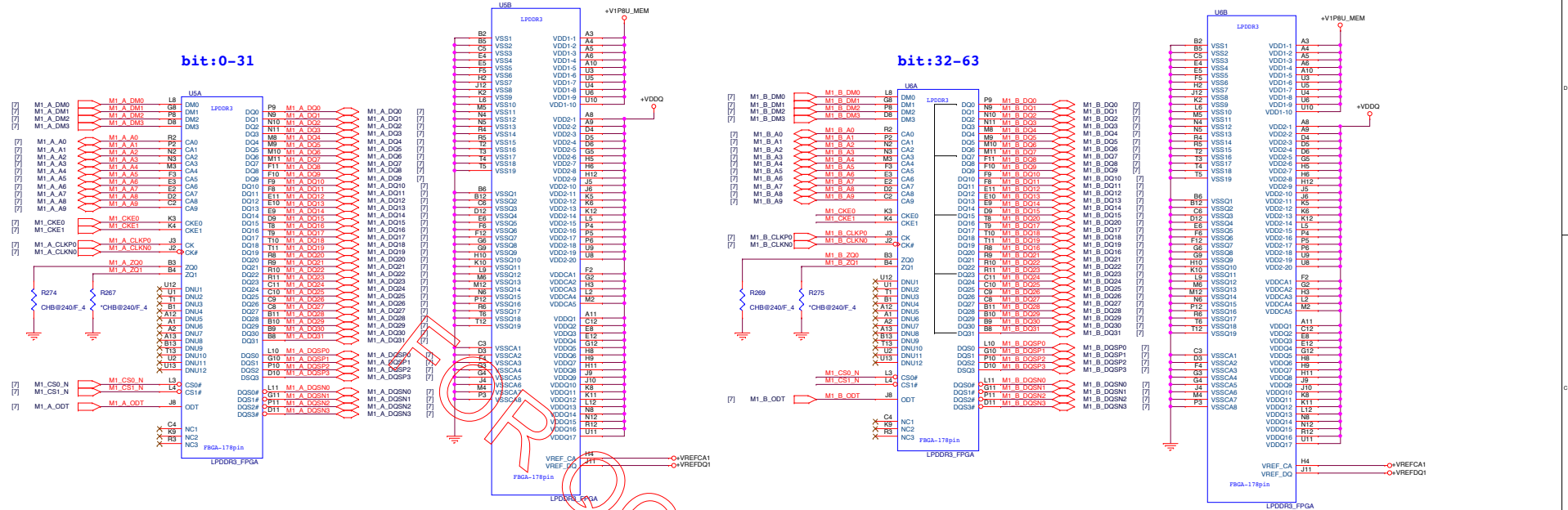
VOLTAGE MERGE



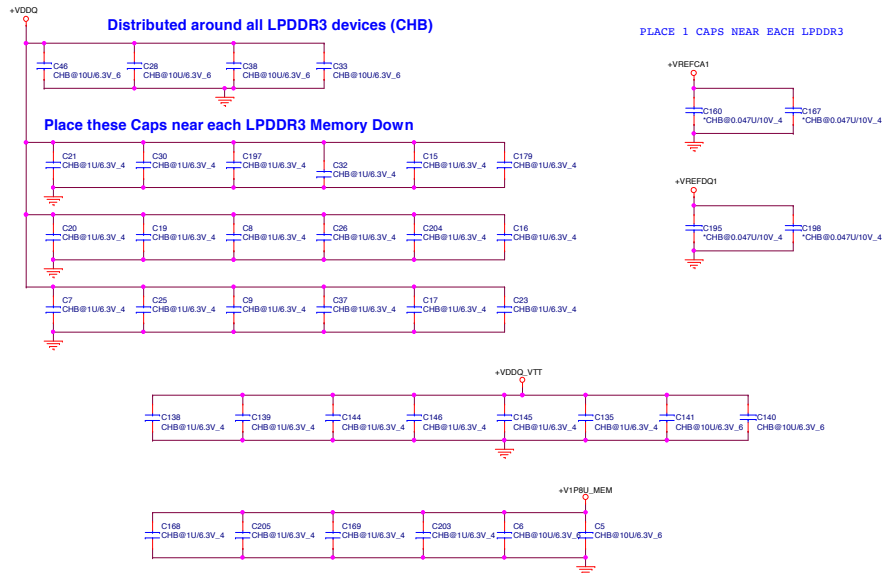
VREF_CA AND DQ CIRCUITS



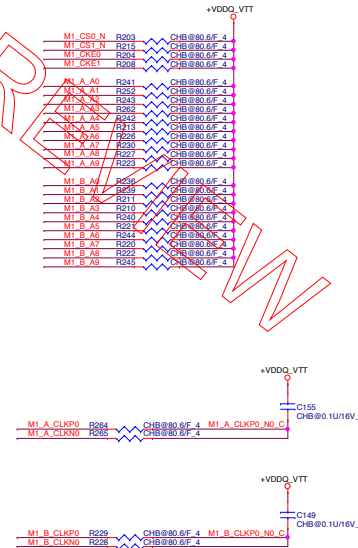
CHANNEL B:8Gb*2 LPDDR3



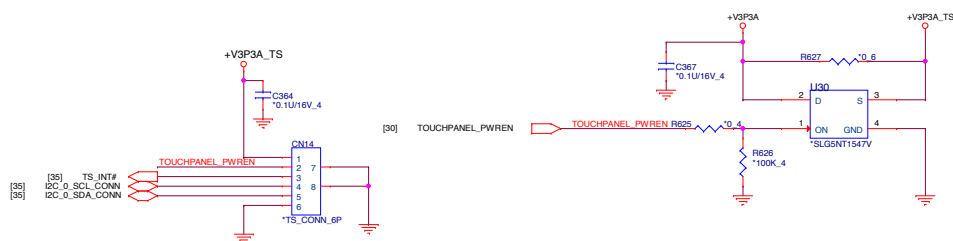
DE-CAPS FOR MEMORY CHANNEL B



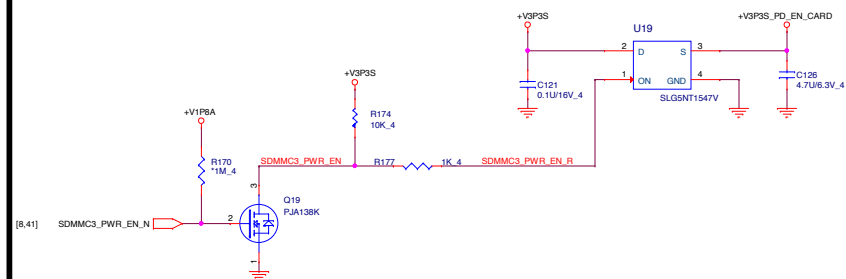
VTT TERMINATIONS



SD SLOT POWER SUPPLY



Card Reader (CRD)



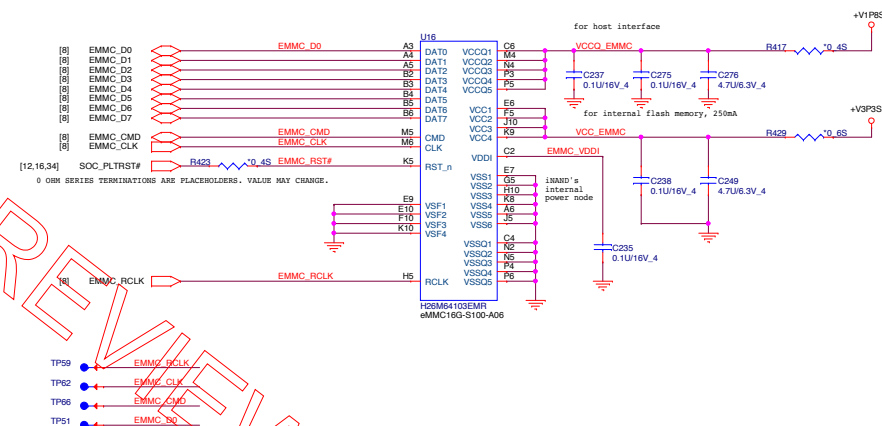
SD SLOT/EMI

This is full size SD card (push-push type)

Card Reader (CRD)

eMMC (MMC)

eMMC



```

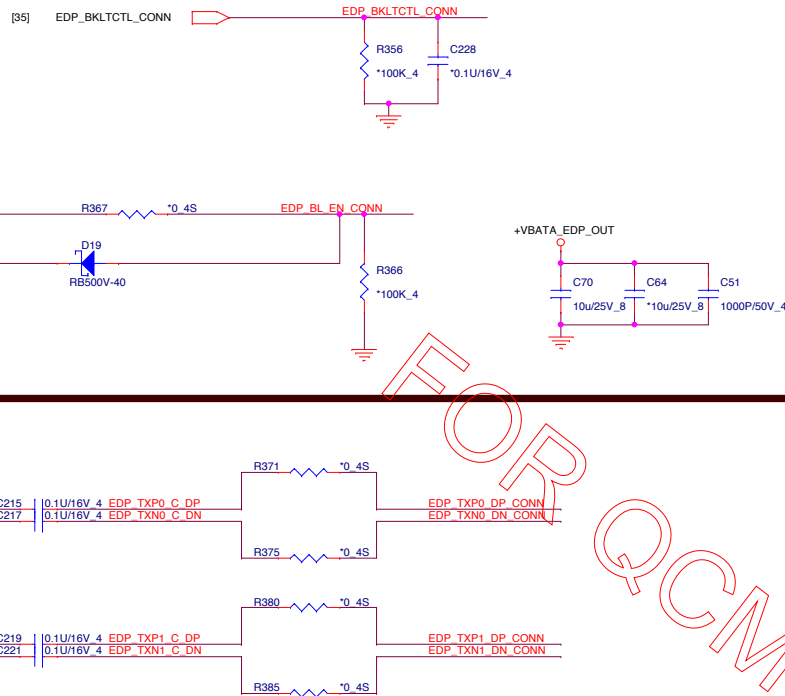
16g
Samsung-->KLMAG2WEMB-B031-AKE2RF-T505-- IC FLASH(153)KLMAG2WEMB-B031(FBGA)STNBSQ
Hynix--> H26M52103FMR (0x03)--AR0ZHQRI000--PROG IC FLASH(153P)H26M52103FMR STNBSQ

32g
Samsung-->KLMB44WECB-B031-AKE3SZ-T500--IC FLASH(153)KLMB44WECB-B031(FBGA)STNBSQ
Hynix--> H26M64103ZMR (0x03)--AR0ZHQRI001--PROG IC FLASH(153P)H26M64103ZMR STNBSQ

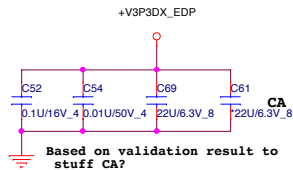
```

eDP PANEL CONTROL

LCD(LDS)



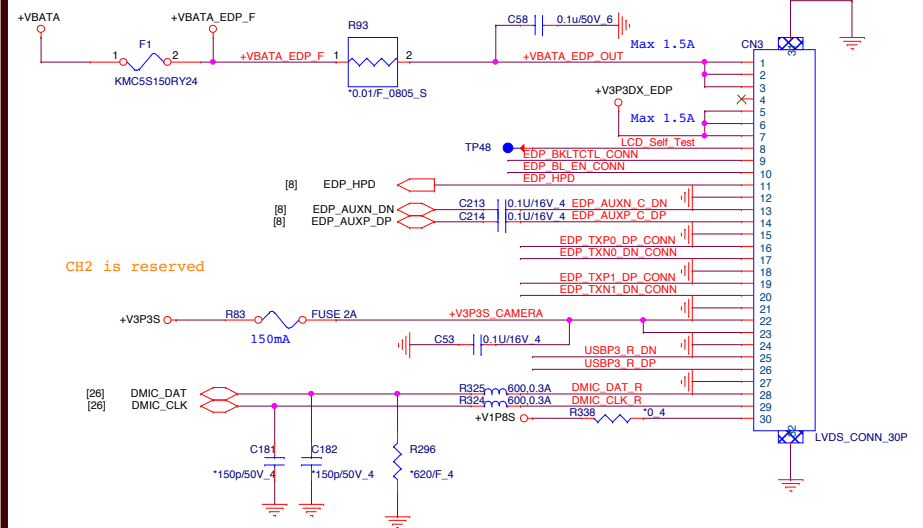
eDP Power



eDP CONNECTOR

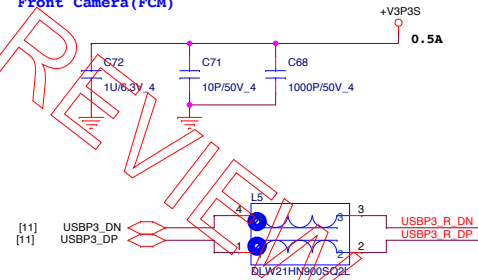
20

LCD(LDS)

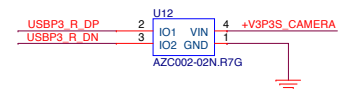


CAMERA - POWER AND USB CMC

Front Camera(FCM)

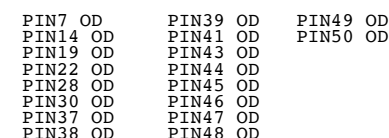


ESD

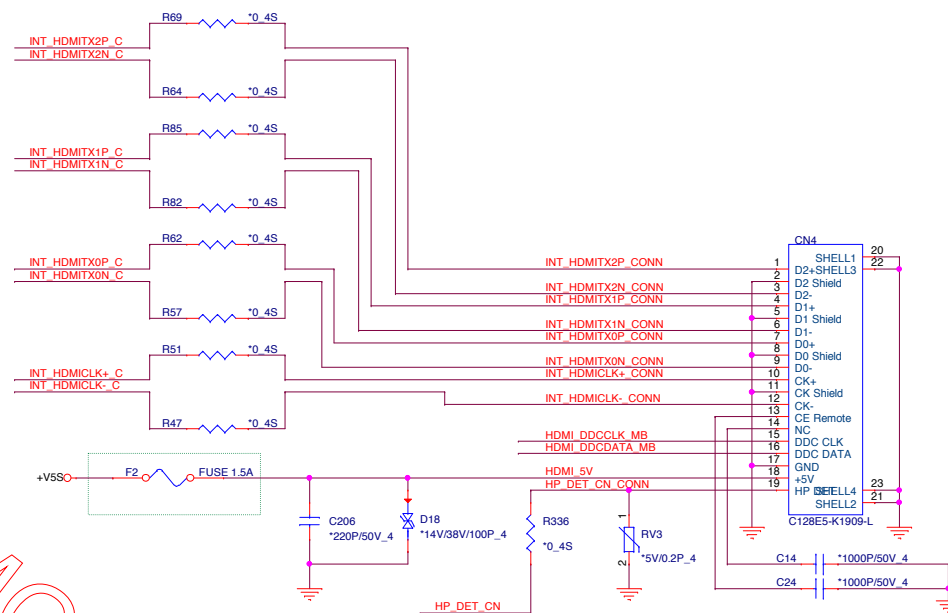
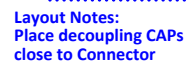


Layout note: Place close to CN9

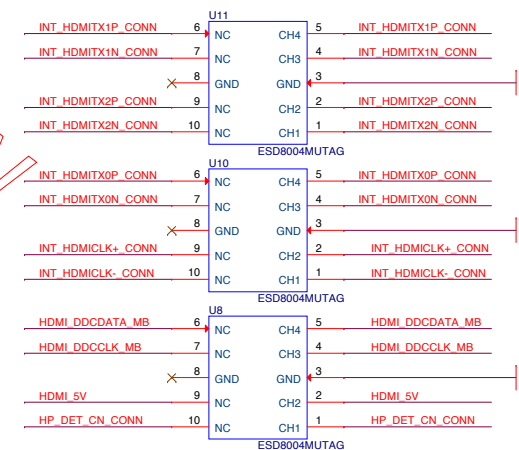
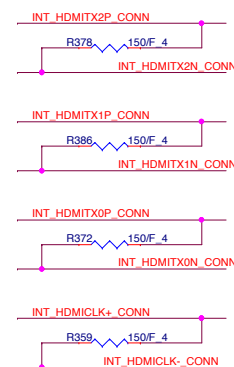
		PROJECT : NL6D	
		Quanta Computer Inc.	
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		1A	
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HDMI CONNECTOR



EMI

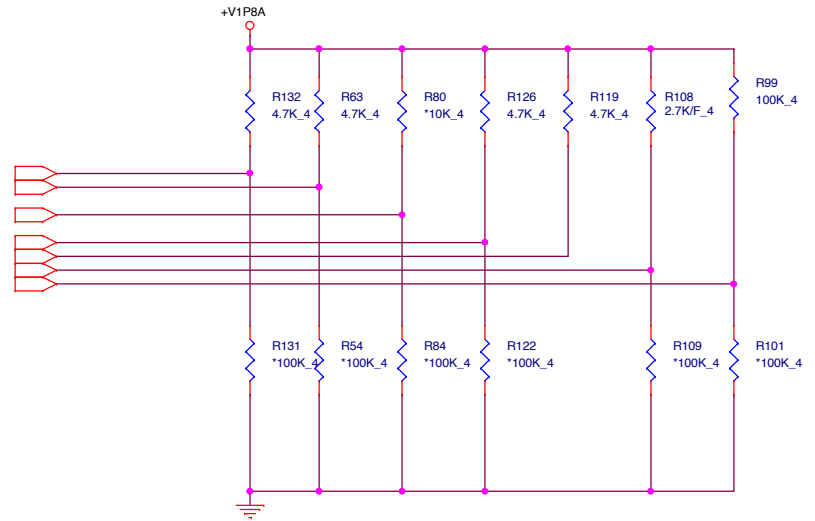


Layout note:Place close to HDMI Conn

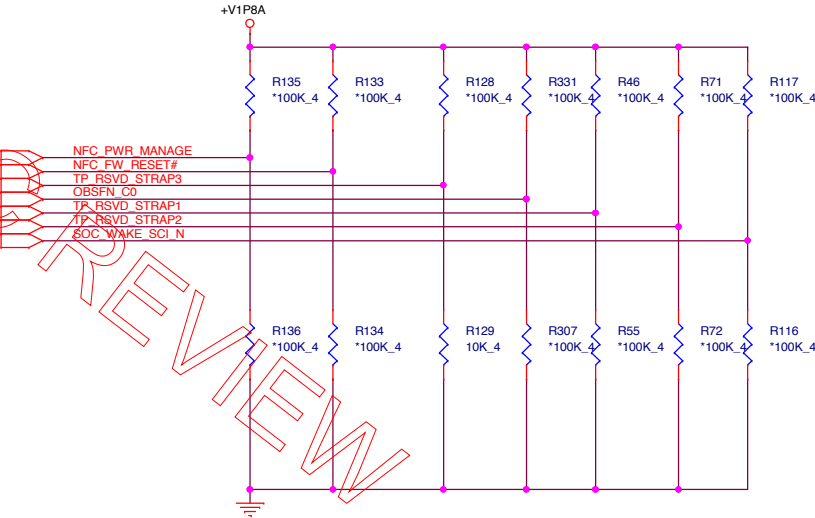
BSW Strapping Table (based on EDS V1.0), sampled on the rising edge of PMU_RSMRST_N

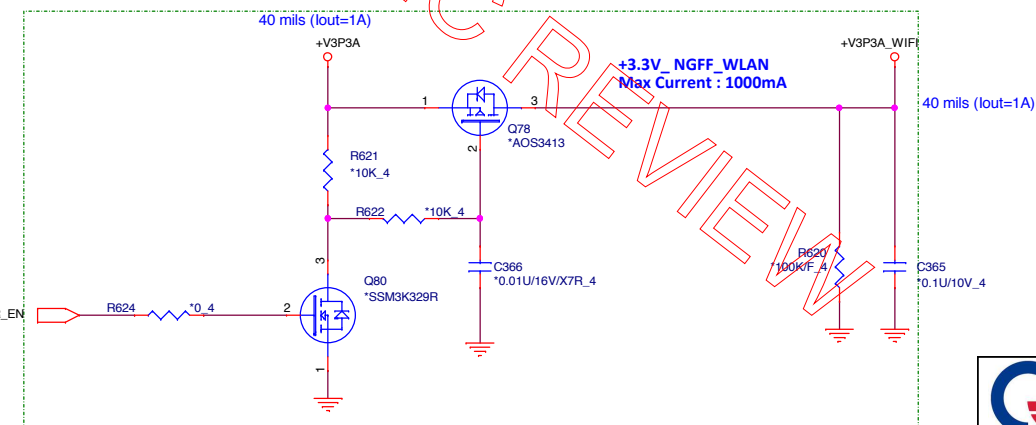
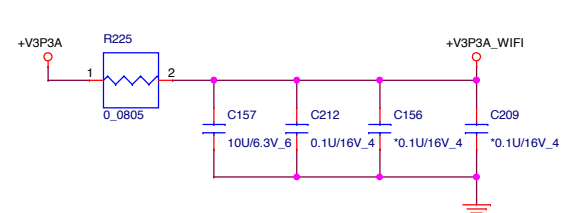
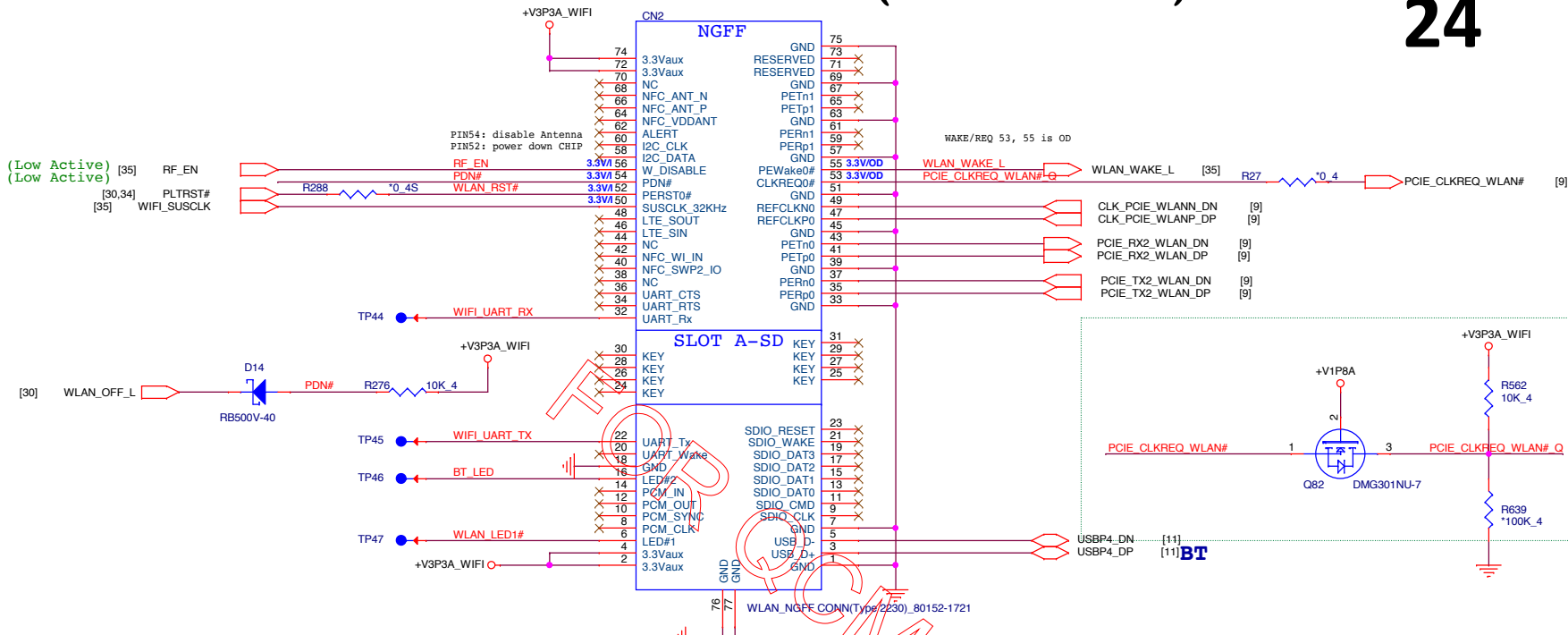
Pin Name	Strap description	Configuration
GPIO_SUS0	DDI0 Detect	0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS1	DDI1 Detect	0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS2	Top Swap (A16 Override)	0 = change boot loader address 1 = Normal operation
GPIO_SUS3	DSI Display Detect (Leave floating if GPIO functionality is not used, it is not POR)	0 = DSI not detected 1 = DSI detected
GPIO_SUS4	BIOS Boot Selection	0 = No SPI 1 = SPI
GPIO_SUS5	Security Flash Descriptors	0 = Not support 1 = Normal operation
GPIO_SUS6	Halt Boot strap	1 = Normal operation (MUST be high at RSMRST# de-assert to ensure proper platform operation and use of GPIO_DFX[8:0])
GPIO_SUS7	DFX SUS DEBUG strap	0 = SUSDUG 1 = No SUSDUG
GPIO_SUS8	PLLs, ICLK, USB2, DDI, SFR, supply select	0 = Supply is 1.25V 1 = Supply is 1.35V
GPIO_SUS9	ICLK, USB2, DDI, SFR Bypass	0 = No Bypass(Default) 1 = Bypass with 1.05V
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	0 = No Bypass(Default) 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	0 = No Bypass(Default) 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	0 = No Bypass(Default) 1 = Bypass

[10,35] MUX_AUD_INT1#
[10,34] EC_SMI_L
[10,34] KBD_IRQ#
[10,29] TRACKPAD_INT#
[10] EC_KBD_ALERT_SOC
[10,16] SOC_RUNTIME_SCI
[10] SOC_KBC_SMI



[10] NFC_PWR_MANAGE#
[10] NFC_FW_RESET#
[10] TP_RSVD_STRAP3
[8,16] OBSFN_C0
[8] TP_RSVD_STRAP1
[8] TP_RSVD_STRAP2
[10,34] SOC_WAKE_SCI_N



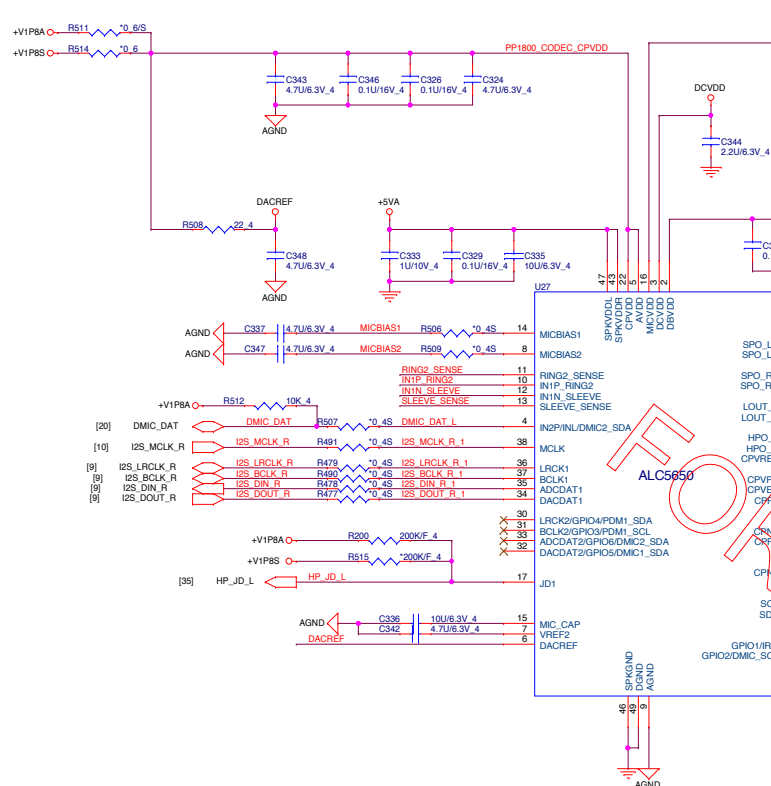


Removed (2015/03/27)

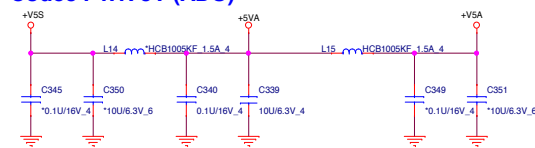
LTE NGFF (LTE)

FOR QCMC REVIEW

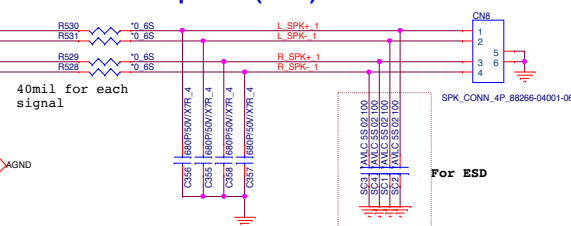
Codec (ADO)



Codec PWR 5V (ADO)



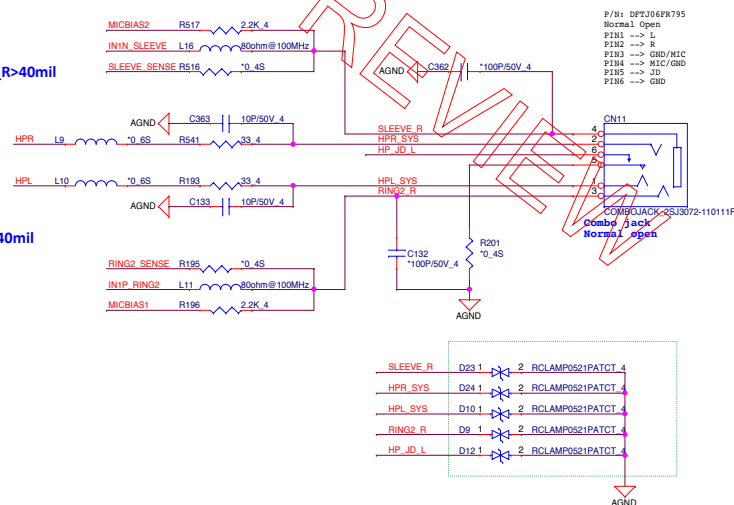
Internal Speaker (ADO)



Combo Jack (ADO)

IN1N_SLEEVE/SLEEVE_R>40mil
SLEEVE_SENSE>20mil

IN1P_Ring2/Ring2_R>40mil
Ring2_SENSE>20mil

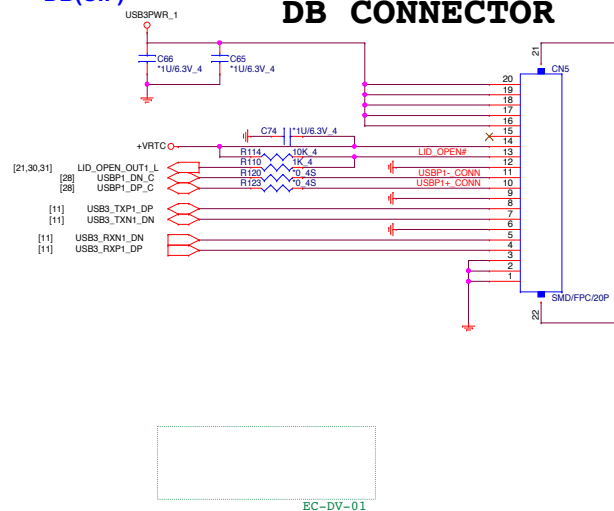


To be validated if ESD protections are un-stuffed

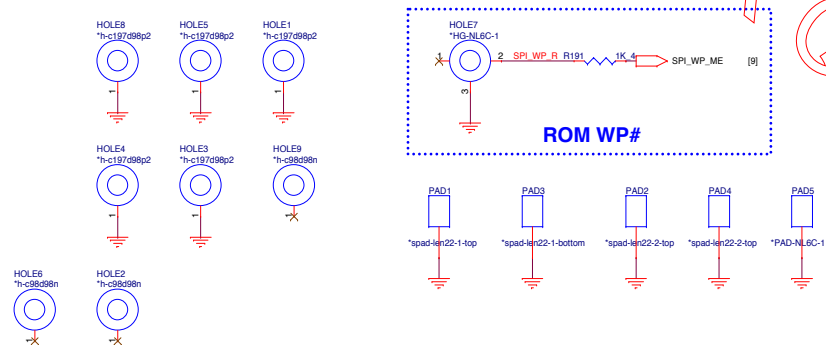
TPM



DB CONNECTOR



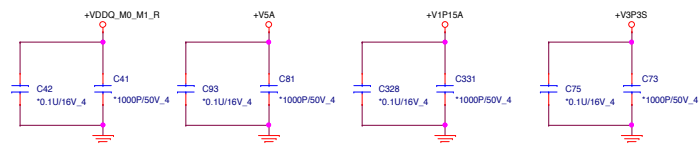
Holes(OTH) MOUNTING HOLES

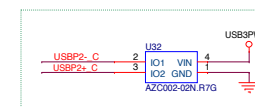
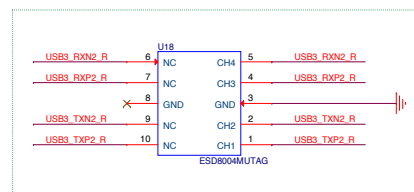
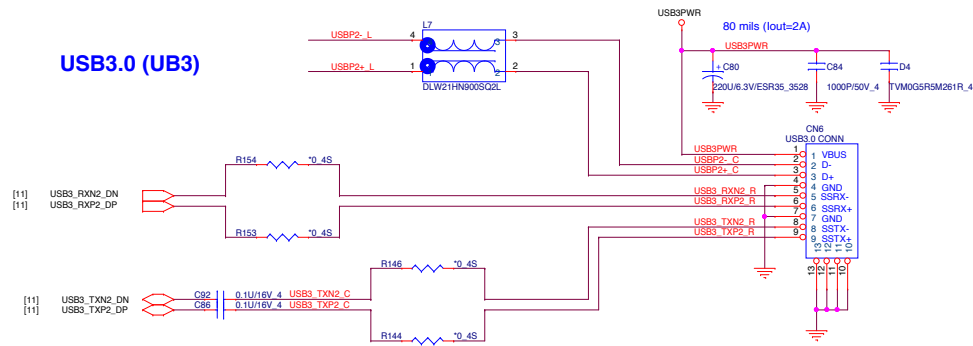


Battery LED

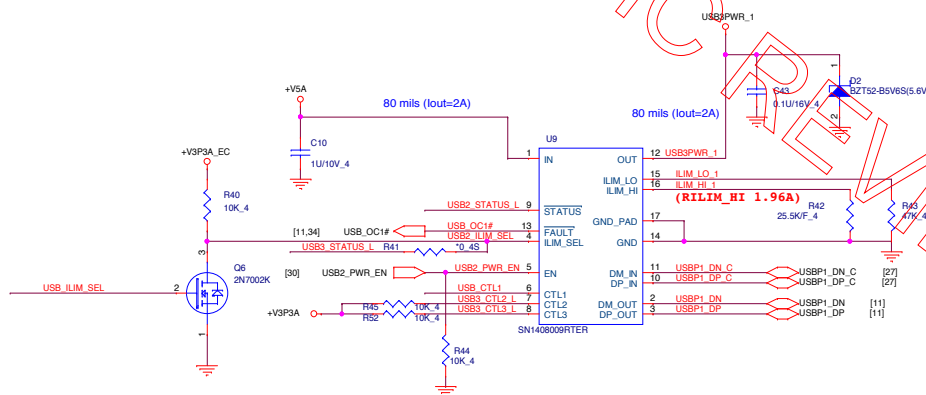


EMI caps

**RF caps**



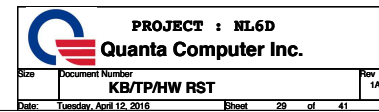
USB PWR(Charger)



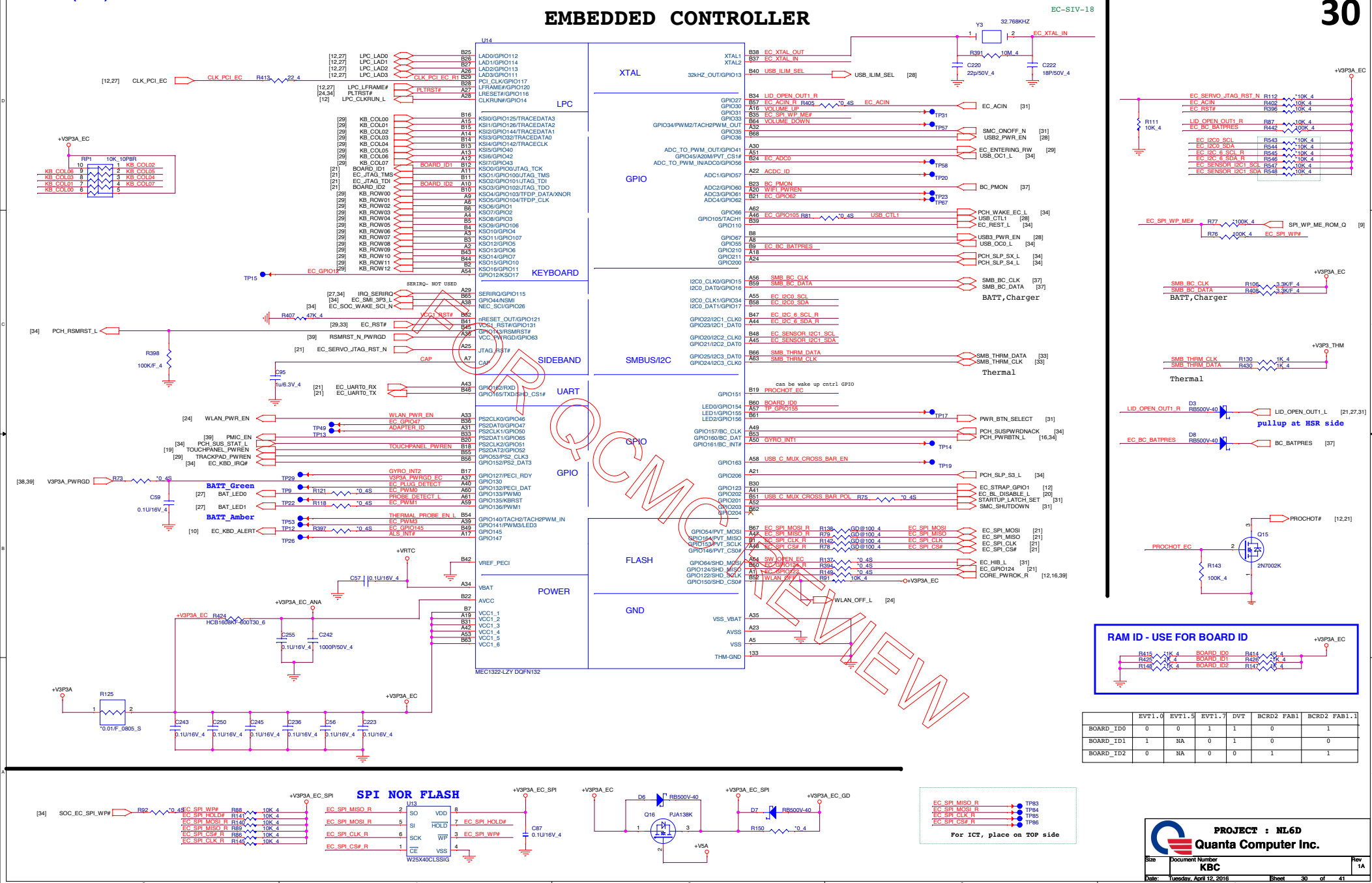
Trackpad(TPD)

HOLELESS RESET





1-CHIP (KBC)



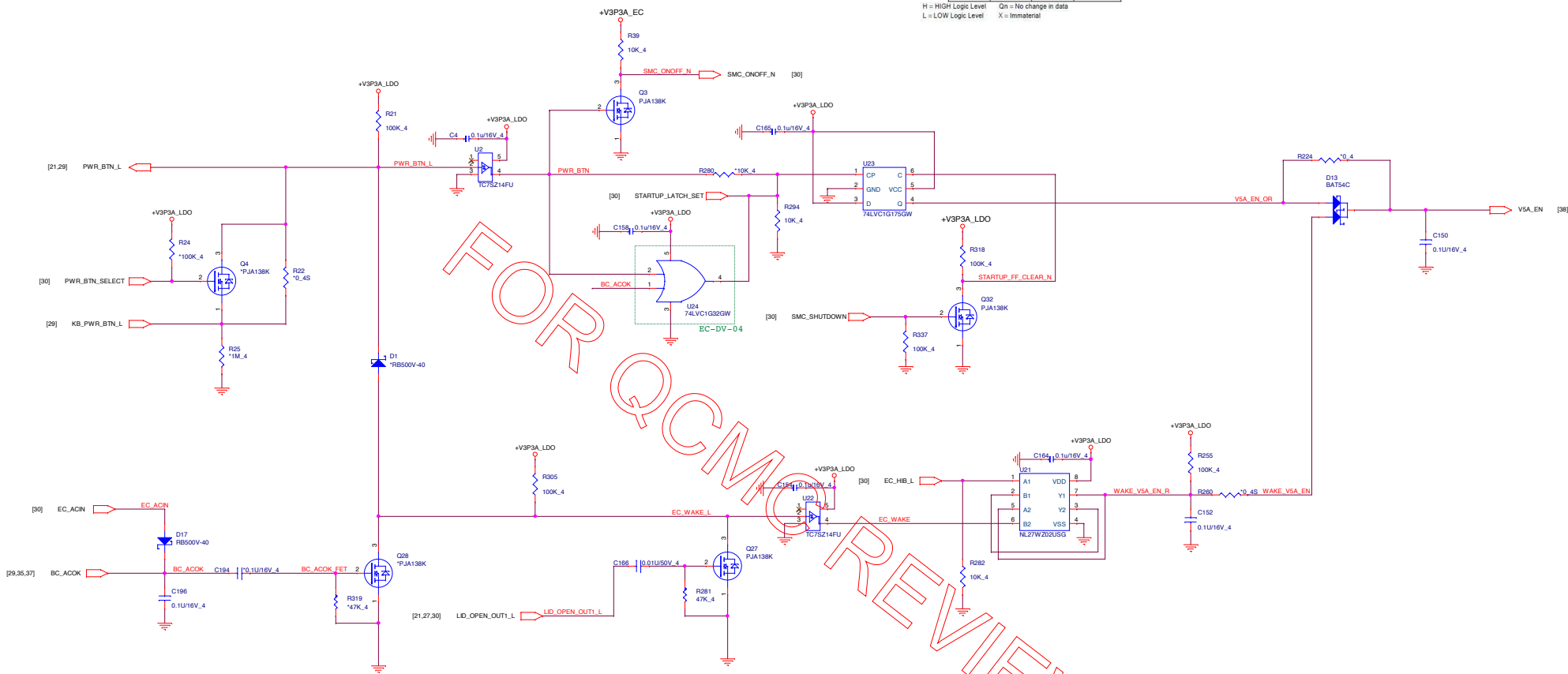
EMBEDDED CONTROLLER



Function Table

Inputs			Output
CP	D	C	Q
	L	H	L
	H	H	H
	X	H	Qn
	X	L	L

H = HIGH Logic Level
L = LOW Logic Level
Qn = No change in data
X = Immaterial



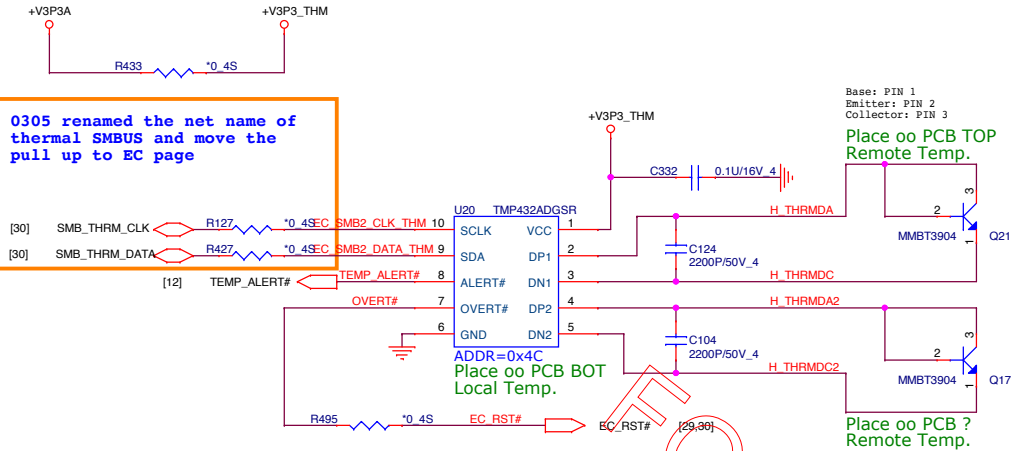
EC HIB WAKE SOURCES

Removed (2015/03/30)

FOR QCMC REVIEW

Thermal (THM)

THERMAL SENSOR



ACCELEROMETER

G-Sensor (ACS)

Touch screen(TSN)

Removed (2015/03/27)

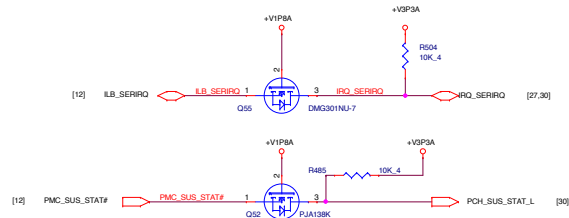
Touch screen(TSN)

Removed (2015/03/27)

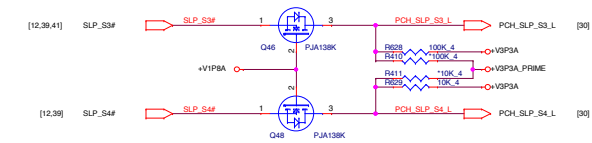
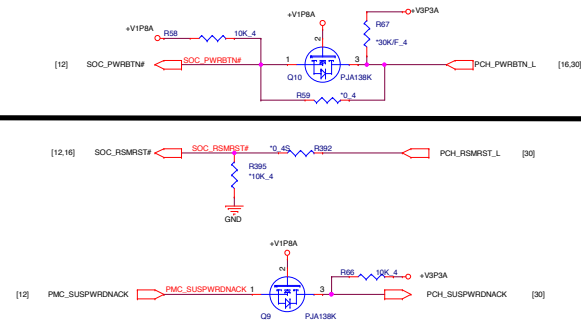
LED board(UIF)

Removed (2015/03/27)

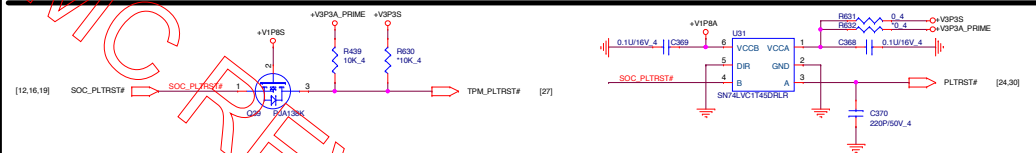
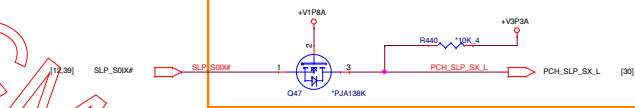
PWRON SEQUENCE



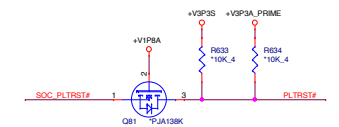
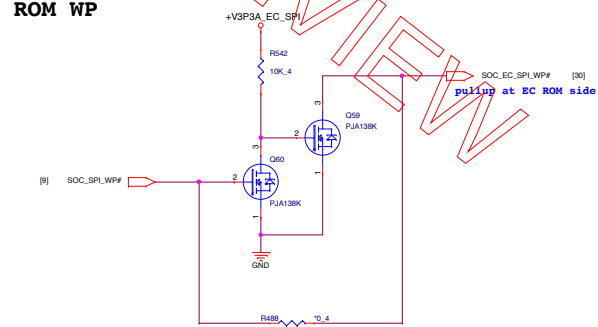
PWRON SEQUENCE



0305 SLP_SX related components are stuffed

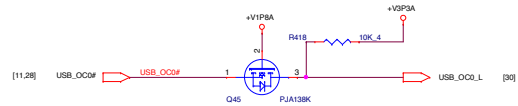


ROM WP

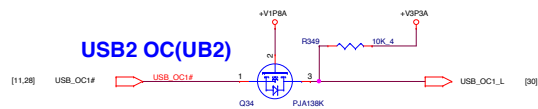


USB OC

USB3 OC(UB3)



USB2 OC(UB2)



0311 Added 5 FETs as level shifters on EC OD GPIOs

pulling at EC ROM side

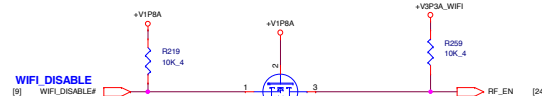
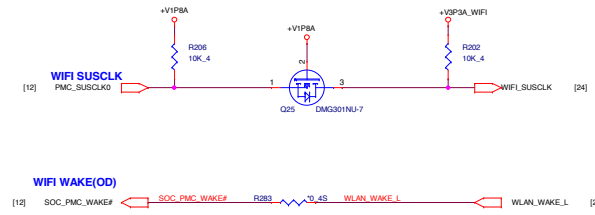
LTE(LTE)

Removed (2015/03/27)

WiFi(NGF)

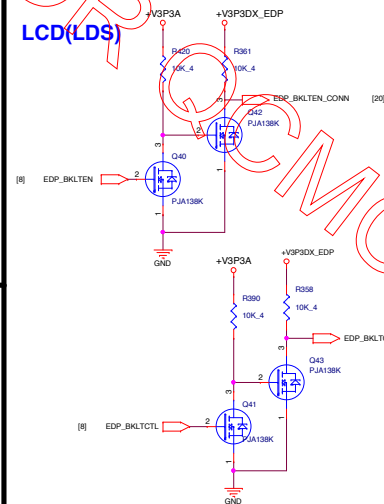
LEVEL TRANSLATOR 2

WIFI SIGNALS

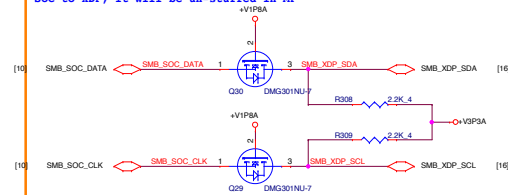


EDP CONTROL PIN

LCD(LDS)

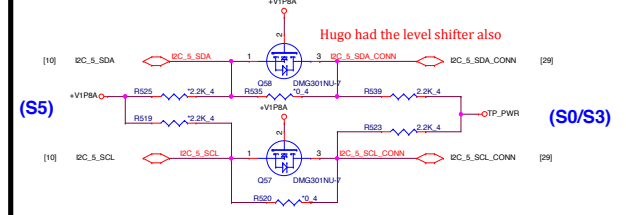


0310 Added level shifter on SMBUS from Soc to XDP, it will be un-stuffed in MP



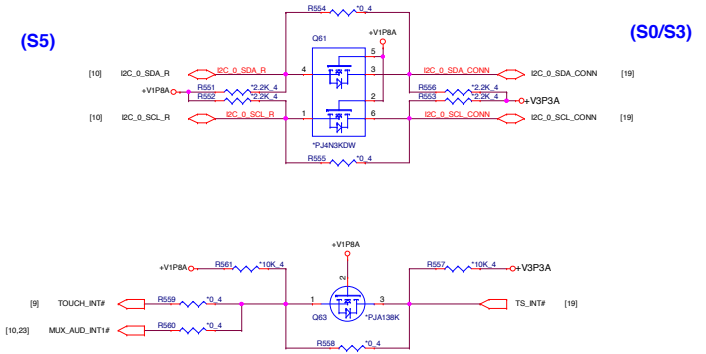
TRACK PAD I2C_5 SIGNALS

Trackpad(TPD)

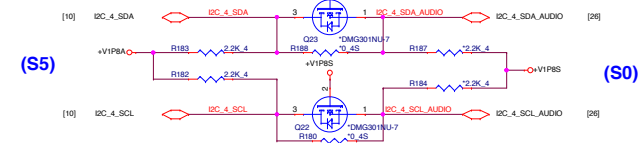


Touch Screen(TSN)

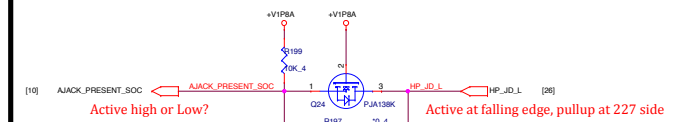
TOUCH SCREEN I2C_0 SIGNALS



Audio(ADO)



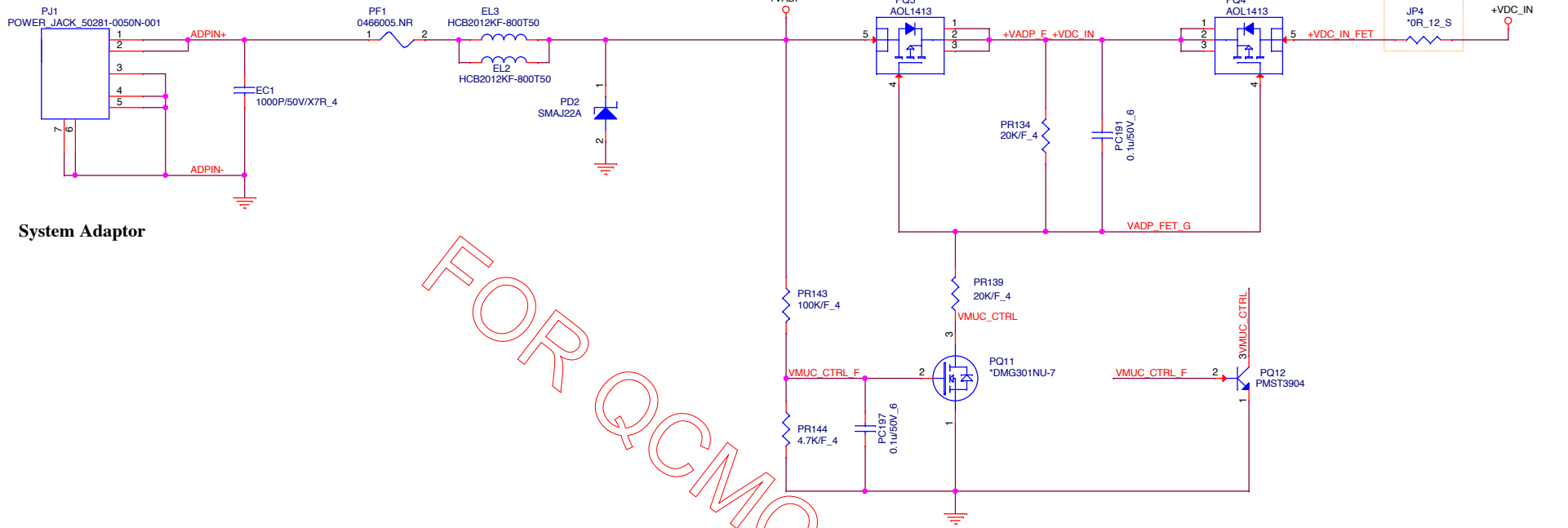
Removed (2015/04/09)



Active high or Low?

DC JACK

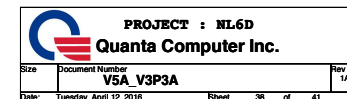
36

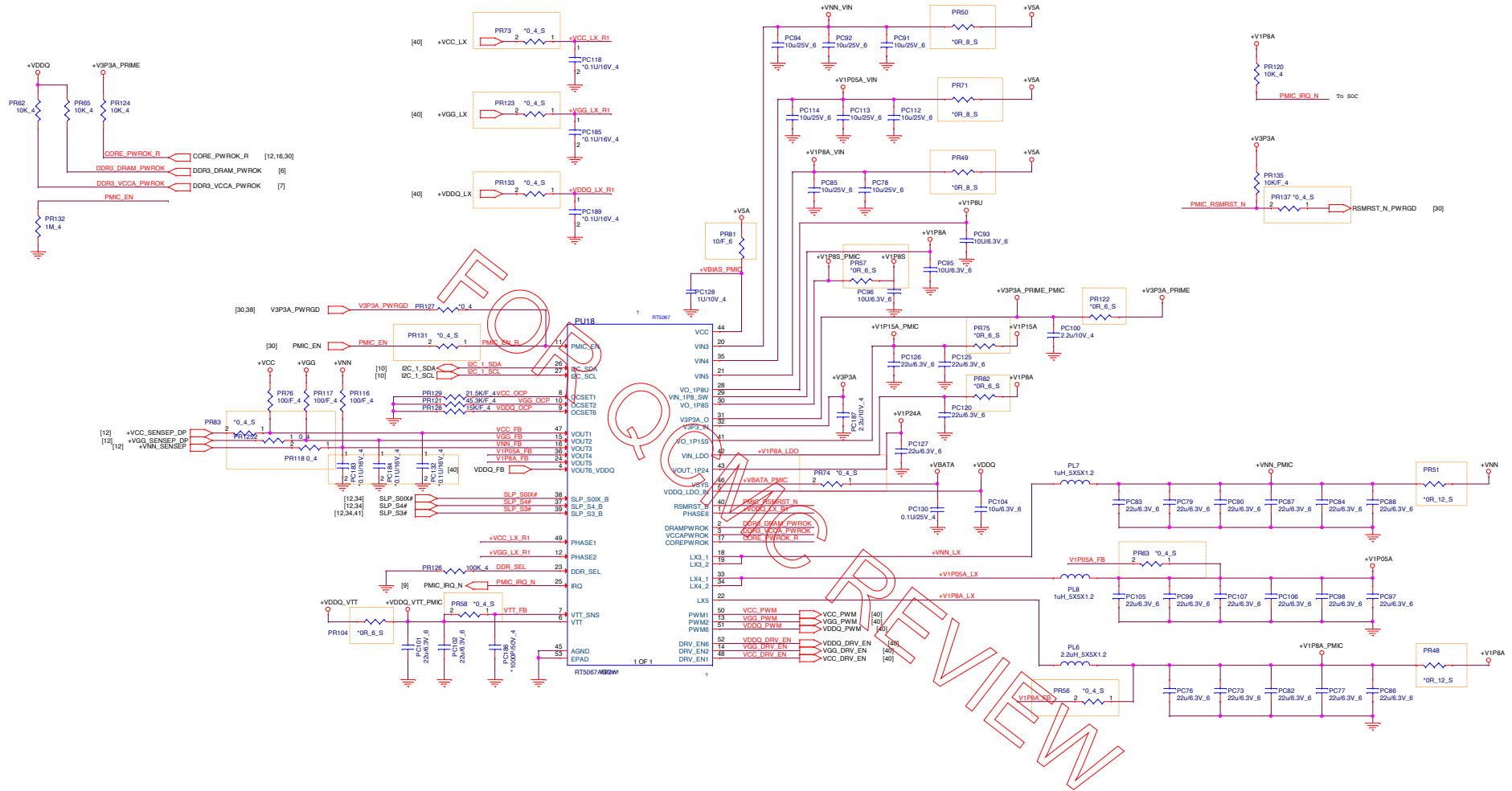


System Adaptor

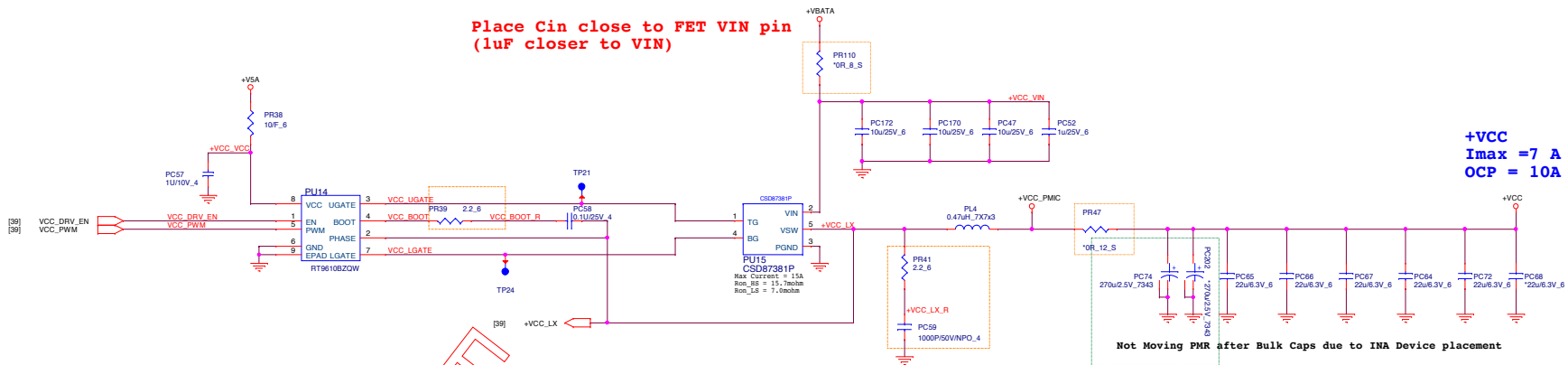
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[illegible]





Place Cin close to FET VIN pin
(1uF closer to VIN)



Place Cin close to FET VIN pin
(1uF closer to VIN)

