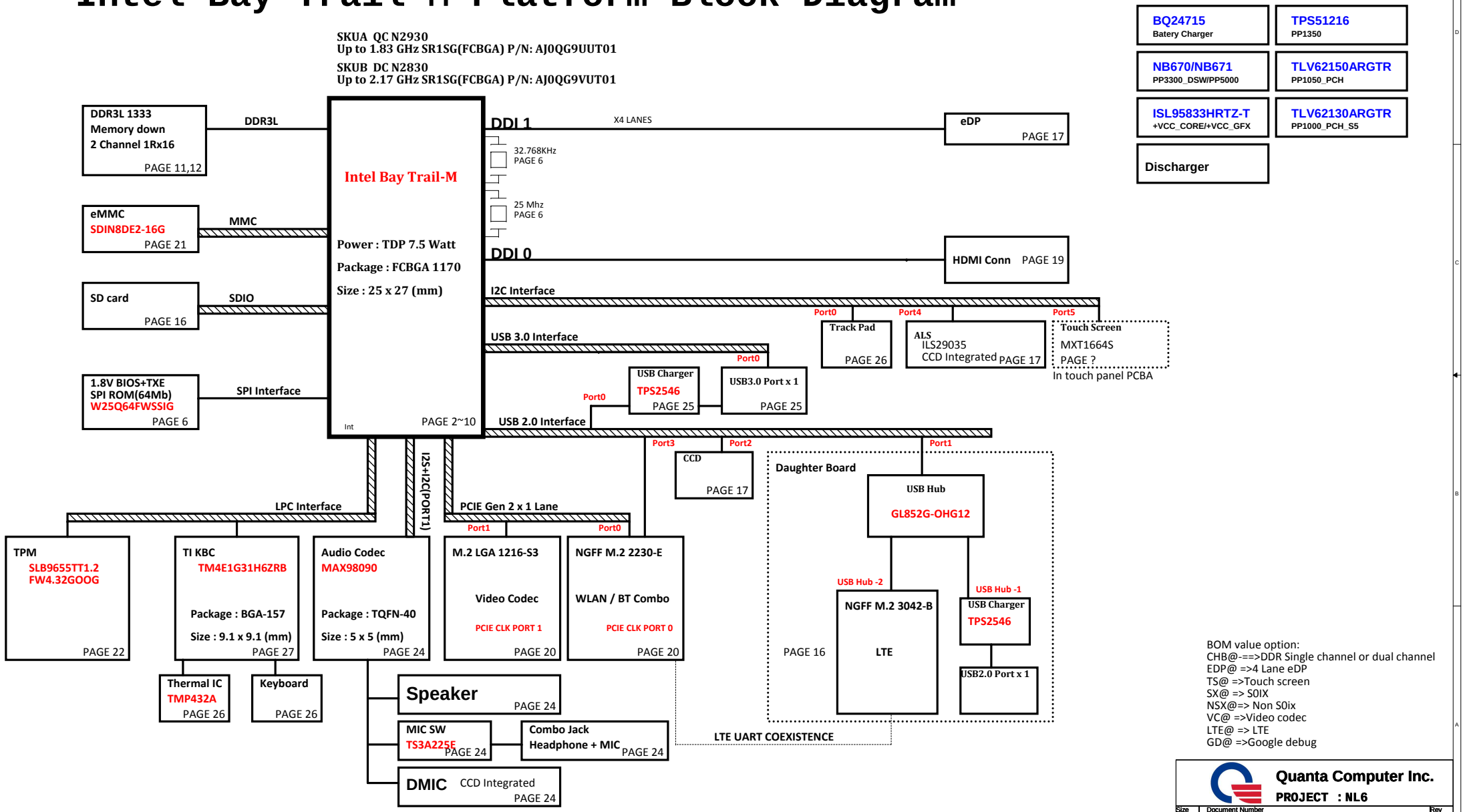
NL6

01

Intel Bay Trail-M Platform Block Diagram

SKUA QC N2930
Up to 1.83 GHz SR1SG(FCBGA) P/N: AJ0QG9UUT01

SKUB DC N2830
Up to 2.17 GHz SR1SG(FCBGA) P/N: AJ0QG9VUT01



BQ24715 Batery Charger	TPS51216 PP1350
NB670/NB671 PP3300_DSW/PP5000	TLV62150ARGTR PP1050_PCH
ISL95833HRTZ-T +VCC_CORE/+VCC_GFX	TLV62130ARGTR PP1000_PCH_S5
Discharger	

BOM value option:
CHB@-==>DDR Single channel or dual channel
EDP@ =>4 Lane eDP
TS@ =>Touch screen
SX@ => S0IX
NSX@=> Non S0ix
VC@ =>Video codec
LTE@ => LTE
GD@ =>Google debug

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	Intel Block Diagram	1A
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U14A

VLV_M_D

(12) M_A_A[15:0]

M_A_A0 K45 DRAM0_MA_00
M_A_A1 H47 DRAM0_MA_11
M_A_A2 L41 DRAM0_MA_22
M_A_A3 H44 DRAM0_MA_33
M_A_A4 H50 DRAM0_MA_44
M_A_A5 G53 DRAM0_MA_55
M_A_A6 H49 DRAM0_MA_66
M_A_A7 D50 DRAM0_MA_77
M_A_A8 G52 DRAM0_MA_88
M_A_A9 E52 DRAM0_MA_99
M_A_A10 K48 DRAM0_MA_1010
M_A_A11 E51 DRAM0_MA_1111
M_A_A12 F47 DRAM0_MA_1212
M_A_A13 J51 DRAM0_MA_1313
M_A_A14 B49 DRAM0_MA_1414
M_A_A15 B50 DRAM0_MA_1515

(12) M_A_DM0 M_A_DM0 G36 DRAM0_DM_00
(12) M_A_DM1 M_A_DM1 B36 DRAM0_DM_11
(12) M_A_DM2 M_A_DM2 F38 DRAM0_DM_22
(12) M_A_DM3 M_A_DM3 B42 DRAM0_DM_33
(12) M_A_DM4 M_A_DM4 P51 DRAM0_DM_44
(12) M_A_DM5 M_A_DM5 V42 DRAM0_DM_55
(12) M_A_DM6 M_A_DM6 Y50 DRAM0_DM_66
(12) M_A_DM7 M_A_DM7 Y52 DRAM0_DM_77

(12) M_A_RAS# M_A_RAS# M45 DRAM0_RAS
(12) M_A_CAS# M_A_CAS# M44 DRAM0_CAS
(12) M_A_WE# M_A_WE# H51 DRAM0_WE

(12) M_A_BS0 M_A_BS0 K47 DRAM0_BS_00
(12) M_A_BS1 M_A_BS1 K44 DRAM0_BS_11
(12) M_A_BS2 M_A_BS2 D52 DRAM0_BS_22

(12) M_A_CS#0 M_A_CS#0 P44 DRAM0_CS_0
P45 DRAM0_CS_2

(12) M_A_CKE0 M_A_CKE0 C47 DRAM0_CKE_00
D48 RESERVED_D48
F46 DRAM0_CKE_22
E46 RESERVED_E46

(12) M_A_ODT0 M_A_ODT0 T41 DRAM0_ODT_0
P42 DRAM0_ODT_2

(12) M_A_CLKP0 M_A_CLKP0 M50 DRAM0_CKP_0
(12) M_A_CLKN0 M_A_CLKN0 M48 DRAM0_CKN_0
P50 DRAM0_CKP_2
P48 DRAM0_CKN_2

(12) M_A_DRAMRST# M_A_DRAMRST# P41 DRAM0_DRAMRST

CPU_VREF AF44 DRAM_VREF

GND R15 100K/F_4 ICLK_DRAM_TERMN_0 AH42
R16 100K/F_4 ICLK_DRAM_TERMN_1 AF42
ICLK_DRAM_TERMN
ICLK_DRAM_TERMN_AF42

SOC_DRAM_PWROK AD42
SOC_VCCA_PWROK AB42
DRAM_VDD_S4_PWROK +1.35V_SUS
DRAM_CORE_PWROK +1.35V_SUS

GND R23 23.2/F_4 DRAM_RCOMP0 AD44
R19 29.4/F_4 DRAM_RCOMP1 AF45
R18 162/F_4 DRAM_RCOMP2 AD45
DRAM_RCOMP_00
DRAM_RCOMP_11
DRAM_RCOMP_22

AF40 RESERVED_AF40
AF41 RESERVED_AF41
AD40 RESERVED_AD40
AD41 RESERVED_AD41

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VLV_M_D/BGA
REV = 1.15

M_A_DQ[63:0] (12)

M36 M_A_DQ0 DRAM0_DQ_00
J36 M_A_DQ1 DRAM0_DQ_11
P40 M_A_DQ2 DRAM0_DQ_22
M40 M_A_DQ3 DRAM0_DQ_33
P36 M_A_DQ4 DRAM0_DQ_44
N36 M_A_DQ5 DRAM0_DQ_55
K40 M_A_DQ6 DRAM0_DQ_66
K42 M_A_DQ7 DRAM0_DQ_77
B32 M_A_DQ8 DRAM0_DQ_88
C32 M_A_DQ9 DRAM0_DQ09_C32
C36 M_A_DQ10 DRAM0_DQ_1010
A37 M_A_DQ11 DRAM0_DQ_1111
C33 M_A_DQ12 DRAM0_DQ_1212
A33 M_A_DQ13 DRAM0_DQ_1313
C37 M_A_DQ14 DRAM0_DQ_1414
B38 M_A_DQ15 DRAM0_DQ_1515
F36 M_A_DQ16 DRAM0_DQ_1616
G38 M_A_DQ17 DRAM0_DQ_1717
F42 M_A_DQ18 DRAM0_DQ_1818
J42 M_A_DQ19 DRAM0_DQ_1919
G40 M_A_DQ20 DRAM0_DQ_2020
C38 M_A_DQ21 DRAM0_DQ_2121
G44 M_A_DQ22 DRAM0_DQ_2222
D42 M_A_DQ23 DRAM0_DQ_2323
A41 M_A_DQ24 DRAM0_DQ_2424
C41 M_A_DQ25 DRAM0_DQ_2525
A45 M_A_DQ26 DRAM0_DQ_2626
B46 M_A_DQ27 DRAM0_DQ_2727
C40 M_A_DQ28 DRAM0_DQ_2828
B40 M_A_DQ29 DRAM0_DQ_2929
B48 M_A_DQ30 DRAM0_DQ_3030
B47 M_A_DQ31 DRAM0_DQ_3131
K52 M_A_DQ32 DRAM0_DQ_3232
K51 M_A_DQ33 DRAM0_DQ_3333
T52 M_A_DQ34 DRAM0_DQ_3434
T51 M_A_DQ35 DRAM0_DQ_3535
L51 M_A_DQ36 DRAM0_DQ_3636
L53 M_A_DQ37 DRAM0_DQ_3737
R51 M_A_DQ38 DRAM0_DQ_3838
R53 M_A_DQ39 DRAM0_DQ_3939
T47 M_A_DQ40 DRAM0_DQ_4040
T45 M_A_DQ41 DRAM0_DQ_4141
Y40 M_A_DQ42 DRAM0_DQ_4242
V41 M_A_DQ43 DRAM0_DQ_4343
T48 M_A_DQ44 DRAM0_DQ_4444
T50 M_A_DQ45 DRAM0_DQ_4545
Y42 M_A_DQ46 DRAM0_DQ_4646
AB40 M_A_DQ47 DRAM0_DQ_4747
V45 M_A_DQ48 DRAM0_DQ_4848
V47 M_A_DQ49 DRAM0_DQ_4949
AD48 M_A_DQ50 DRAM0_DQ_5050
AD50 M_A_DQ51 DRAM0_DQ_5151
V48 M_A_DQ52 DRAM0_DQ_5252
V50 M_A_DQ53 DRAM0_DQ_5353
AB44 M_A_DQ54 DRAM0_DQ_5454
Y45 M_A_DQ55 DRAM0_DQ_5555
V52 M_A_DQ56 DRAM0_DQ_5656
W51 M_A_DQ57 DRAM0_DQ_5757
AC53 M_A_DQ58 DRAM0_DQ_5858
AC51 M_A_DQ59 DRAM0_DQ_5959
W53 M_A_DQ60 DRAM0_DQ_6060
Y51 M_A_DQ61 DRAM0_DQ_6161
AD52 M_A_DQ62 DRAM0_DQ_6262
AD51 M_A_DQ63 DRAM0_DQ_6363

J38 M_A_DQSP0 DRAM0_DQSP_00
K38 M_A_DQSN0 DRAM0_DQSN_00
C35 M_A_DQSP1 DRAM0_DQSP_11
B34 M_A_DQSN1 DRAM0_DQSN_11
D40 M_A_DQSP2 DRAM0_DQSP_22
F40 M_A_DQSN2 DRAM0_DQSN_22
B44 M_A_DQSP3 DRAM0_DQSP_33
C43 M_A_DQSN3 DRAM0_DQSN_33
N53 M_A_DQSP4 DRAM0_DQSP_44
M52 M_A_DQSN4 DRAM0_DQSN_44
T42 M_A_DQSP5 DRAM0_DQSP_55
T44 M_A_DQSN5 DRAM0_DQSN_55
Y47 M_A_DQSP6 DRAM0_DQSP_66
Y48 M_A_DQSN6 DRAM0_DQSN_66
AB52 M_A_DQSP7 DRAM0_DQSP_77
AA51 M_A_DQSN7 DRAM0_DQSN_77

M_A_DQSP0 (12)
M_A_DQSN0 (12)
M_A_DQSP1 (12)
M_A_DQSN1 (12)
M_A_DQSP2 (12)
M_A_DQSN2 (12)
M_A_DQSP3 (12)
M_A_DQSN3 (12)
M_A_DQSP4 (12)
M_A_DQSN4 (12)
M_A_DQSP5 (12)
M_A_DQSN5 (12)
M_A_DQSP6 (12)
M_A_DQSN6 (12)
M_A_DQSP7 (12)
M_A_DQSN7 (12)

1023 unstuff R28 by Intel request
1121 remove R28,R25,C35

PP1350
R344 4.7K/F_4
CPU_VREF
R348 4.7K/F_4
C242 0.1U/10V_4
GND GND

PP3300_PCH_S5
PP1350
R151 4.7K_4
R195 10K_4
DRM_PWOK_C1
DRAM_PWROK R178 0_4 SOC_DRAM_PWROK
(6,11,14) SLP_S4# SLP_S4# 5
Q40A PJ4N3KDW
Q40B PJ4N3KDW
C102 *1u/10V_4
GND GND GND
R191 0_4 PP1350_PGOOD (31)

PP3300_PCH_S5
PP1350
R147 4.7K_4
R205 10K_4
DRM_PWOK_C2
SOC_VCCA_PWROK
(27) EC_PWROK EC_PWROK 5
Q28A PJ4N3KDW
Q28B PJ4N3KDW
C90 *0.1U/10V_4
GND GND

1128 place C90 to close SoC ball

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	Valley 1/9 (DDRA)	1A
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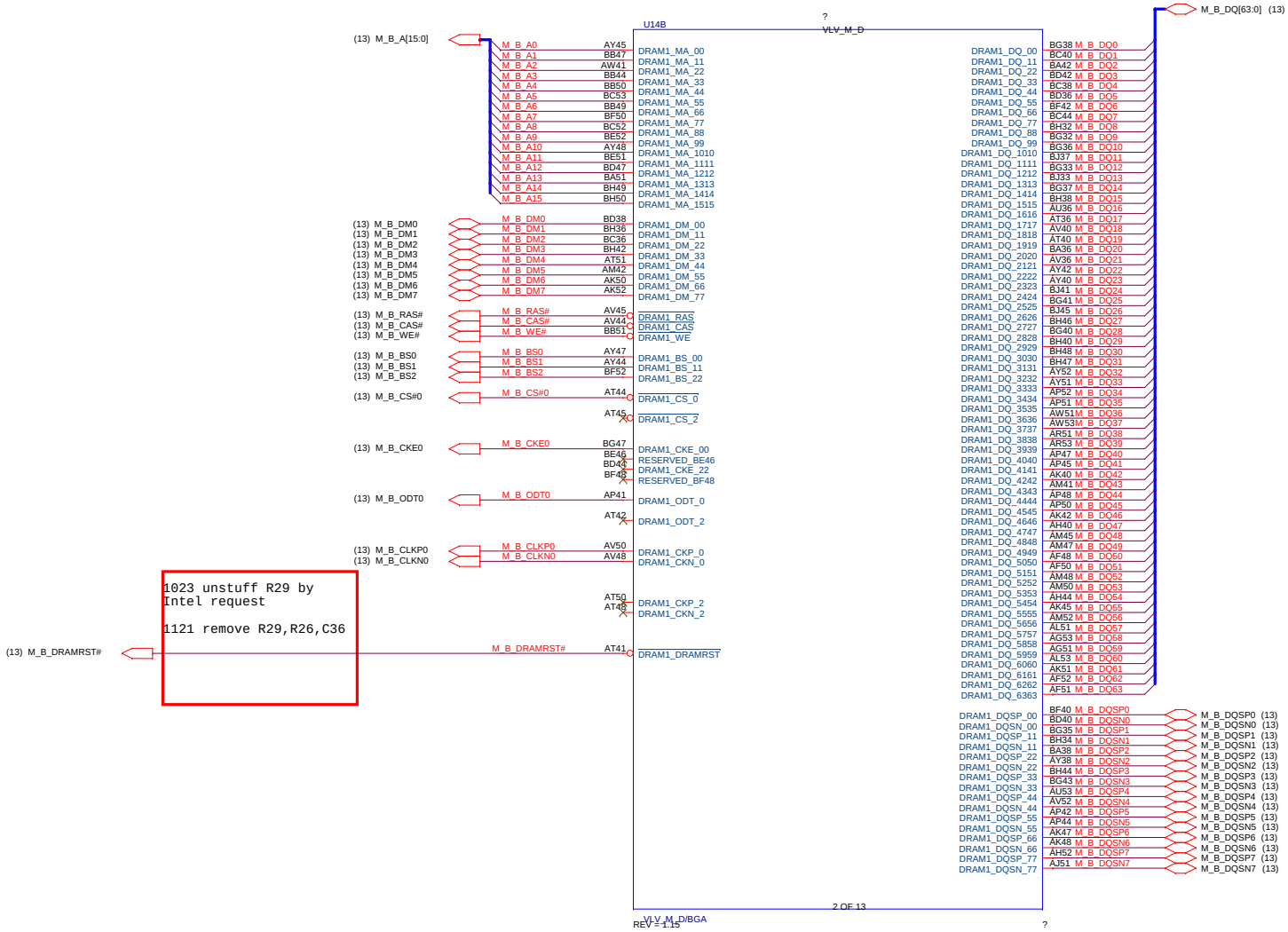

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Size	Document Number	Rev
	Valley 2/9 (DDRB)	1A

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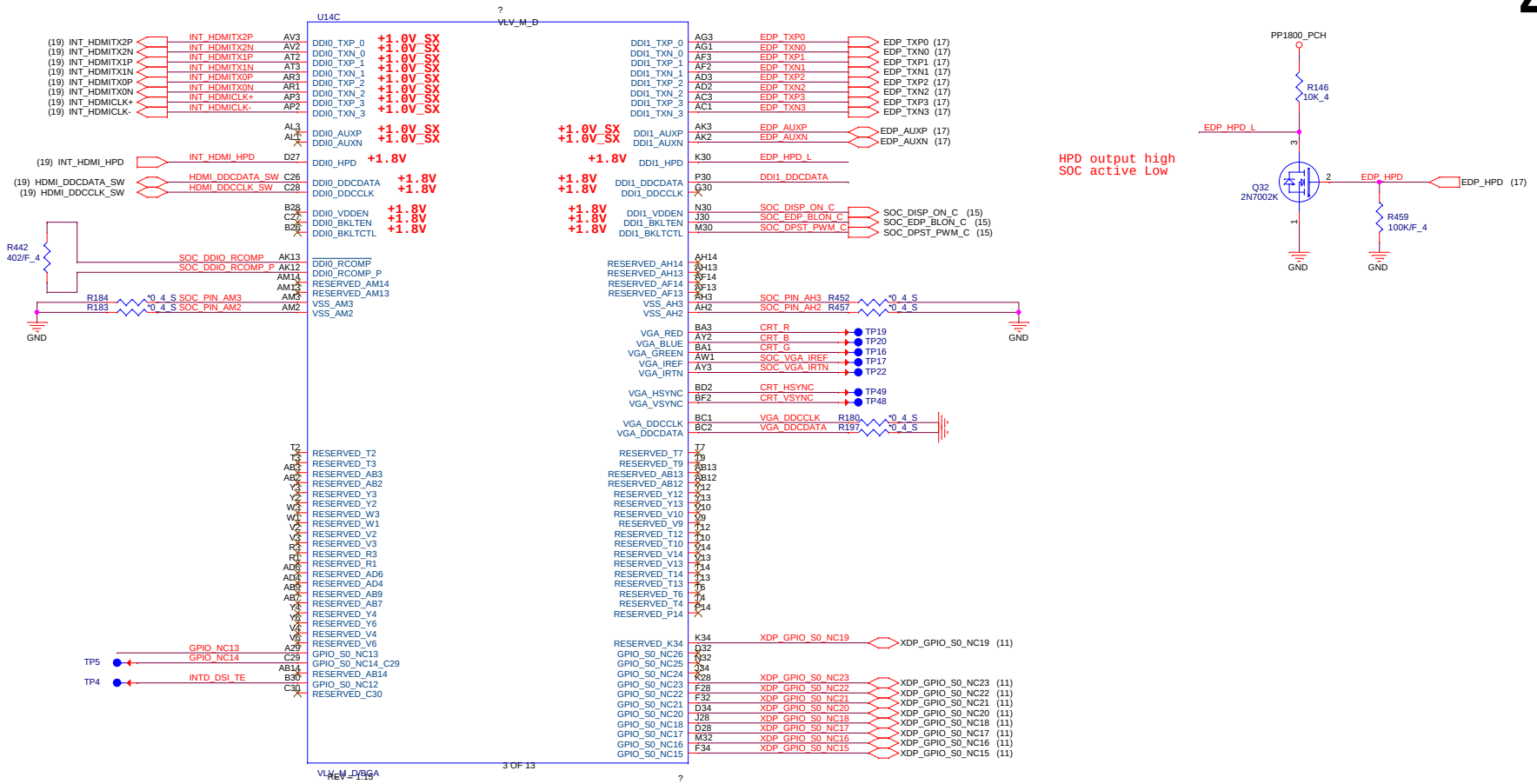

BTM Strapping Table

Pin Name	Strap description	Sampled	Configuration	Note
GPIO_SO_SC_56	Top Swap (A16 Override)	PWROK	0 = Top address bit is unchanged **1 = Top address bit is inverted**	1029 unstuff R128, using SoC internal PU
LPE_I2S2_FRM	BIOS Boot Selection	PWROK	0 = LPC **1 = SPI**	1029 unstuff R372, using SoC internal PU
GPIO_SO_SC_65	Security Flash Descriptors	PWROK	0 = Override **1 = Normal operation**	1115 stuff R372, system can't boot if un-stuff R372 on proto1.5 board, need intel double confirm before proto2
DDI0_DDCDATA	DDI0 Detect	PWROK	0 = DDI0 not detected **1 = DDI0 detected**	Pull up +1.8V at HDMI side
DDI1_DDCDATA	DDI1 Detect	PWROK	0 = DDI0 not detected **1 = DDI0 detected**	1029 unstuff R386, using SoC internal PU 1115 stuff R386, it is required for eDP connected
GPIO_SO_NC_13				

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	Valley 3/9 (Display)	1A
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1025 Delete complete SSD(connector and caps), unstuff R215 and add test points on SATA signals

PP1800_PCH
R215 *10K_4 SATA_DEVSLP_C
R198 *10K_4 SATA_LED_R_N

U14D
VLV_M_D

TP34 TP36 SATA_TXP0_SSD SATA_TXN0_SSD
TP37 TP38 SATA_RXP0_SSD SATA_RXN0_SSD
SATA_TXP1_SSD SATA_TXN1_SSD
SATA_RXP1_SSD SATA_RXN1_SSD
GND R131 *0_4_S ICLK_SATA_TERMP
R139 *0_4_S ICLK_SATA_TERMN
(14) SOC_KBC_SCI R204 *0_4_S SATA_GP0
SATA_DEVSLP_C
SATA_LED_R_N
SATA_RCOMP_DP
SATA_RCOMP_DN
R408 402/F_4
(21) EMMC_CLK
(21) EMMC_D0
(21) EMMC_D1
(21) EMMC_D2
(21) EMMC_D3
(21) EMMC_D4
(21) EMMC_D5
(21) EMMC_D6
(21) EMMC_D7
(21) EMMC_CMD
(21) EMMC_RST#
R409 49.9/F_4 EMMC_RCOMP
GND

0217 reserve C377 on SD CLK for EMI
SD3_CLK
C377 *33P/50V_4

(16) SD3_CLK
(16) SD3_D0
(16) SD3_D1
(16) SD3_D2
(16) SD3_D3
(16,18) SD3_CD#
(16) SD3_CMD
TP23 SDMMC3_1P8_EN
(16) SDIO3_PWR_EN# SDIO3_PWR_EN#
R403 49.9/F_4 SDIO3_RCOMP
GND

SATA_TXP_0 SATA_TXN_0
SATA_RXP_0 SATA_RXN_0
SATA_TXP1 SATA_TXN_1
SATA_RXP_1 SATA_RXN_1
ICLK_SATA_TERMP
ICLK_SATA_TERMN
SATA_GP0 +1.8V
SATA_GP1 +1.8V
SATA_LED +1.8V
SATA_RCOMP_P_AU18 +1.8V
SATA_RCOMP_N_AT18 +1.8V
MMC1_CLK
MMC1_D0
MMC1_D1
MMC1_D2
MMC1_D3
MMC1_D4
MMC1_D5
MMC1_D6
MMC1_D7
MMC1_CMD
MMC1_RST +1.8V
MMC1_RCOMP
SD2_CLK
SD2_D0
SD2_D1
SD2_D2
SD2_D3_CD
SD2_CMD
SD3_CLK +1.8V/+3.3V
SD3_D0 +1.8V/+3.3V
SD3_D1 +1.8V/+3.3V
SD3_D2 +1.8V/+3.3V
SD3_D3 +1.8V/+3.3V
SD3_CD# +1.8V
SD3_CMD +1.8V/+3.3V
SD3_1P8EN +1.8V
SD3_PWREN +1.8V
SD3_RCOMP

PCIE_TX0+_WLAN_C_C336 0.1U/10V_4
PCIE_TX0-_WLAN_C_C341 0.1U/10V_4
PCIE_TX0+_WLAN (20)
PCIE_TX0-_WLAN (20)
PCIE_RX0+_WLAN
PCIE_RX0-_WLAN
PCIE_RX0+_WLAN (20)
PCIE_RX0-_WLAN (20)
PCIE_TX1+_IMAGE_C_C322 0.1U/10V_4
PCIE_TX1-_IMAGE_C_C328 0.1U/10V_4
PCIE_TX1+_IMAGE (20)
PCIE_TX1-_IMAGE (20)
PCIE_RX1+_IMAGE
PCIE_RX1-_IMAGE
PCIE_RX1+_IMAGE (20)
PCIE_RX1-_IMAGE (20)

1213 swap CLKREQ_WLAN and CLKREQ_IMAGE for CLKREQ and CLK pins are aligned

VSS_BB7 R455 *0_4_S
VSS_BB5 R462 *0_4_S
GND
PCIE_CLKREQ_WLAN# (20)
PCIE_CLKREQ_IMAGE# (20)
PCIE_CLKREQ_LAN#
TP18
TP15
SD3_WP (16)
PCIE_RCOMP_P_AP14_AP14
PCIE_RCOMP_N_AP13_AP13
R431 402/F_4
RESERVED_BB4
RESERVED_BB3
RESERVED_AV10
RESERVED_AV9
HDA_LPE_RCOMP R410 49.9/F_4 GND
HDA_RST TP6
HDA_SYNC TP10
HDA_CLK TP7
HDA_SDO TP8
HDA_SDI0 TP9
HDA_SDI1
HDA_DOCKRST
HDA_DOCKEN
DET_TRIGGER (24)
AJACK_MICPRES_L (24)
LPE_I2S2_CLK I2S_BCLK R383 *0_4_S I2S_BCLK_R (24)
LPE_I2S2_FRM I2S_LRCLK R375 *0_4_S I2S_LRCLK_R (24)
LPE_I2S2_DATAOUT I2S_DOUT R381 *0_4_S I2S_DOUT_R (24)
LPE_I2S2_DATAIN I2S_DIN R379 *0_4_S I2S_DIN_R (24)
RESERVED_P34
RESERVED_N34
RESERVED_AK9
RESERVED_AK7
PROCHOT C24
R96 71.5/F_4 PP1000_PCH
SOC_PROCHOT# R103 *0_4_S H_PROCHOT#
R414 *0_4_S H_PROCHOT# (18,27,33)
R553 *0_4 IMVP7_PROCHOT# (28)
ALERT# (23)

1021 un-stuff R553

PP1800_PCH
PCIE_CLKREQ_IMAGE# R152 10K_4
PCIE_CLKREQ_WLAN# R148 10K_4
I2S_DOUT R364 *10K_4

1029 unstuff R364, using SoC internal PU

0 = LPC
1 = SPI
I2S_LRCLK
I2S_DOUT
I2S_LRCLK (4)
I2S_DOUT (4)

Security Flash Descriptors
0 = Override
1 = Normal Operation

Need check to see if MOSFET isolation needed or not

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VLV_M_D/PGA
REV = 1.15

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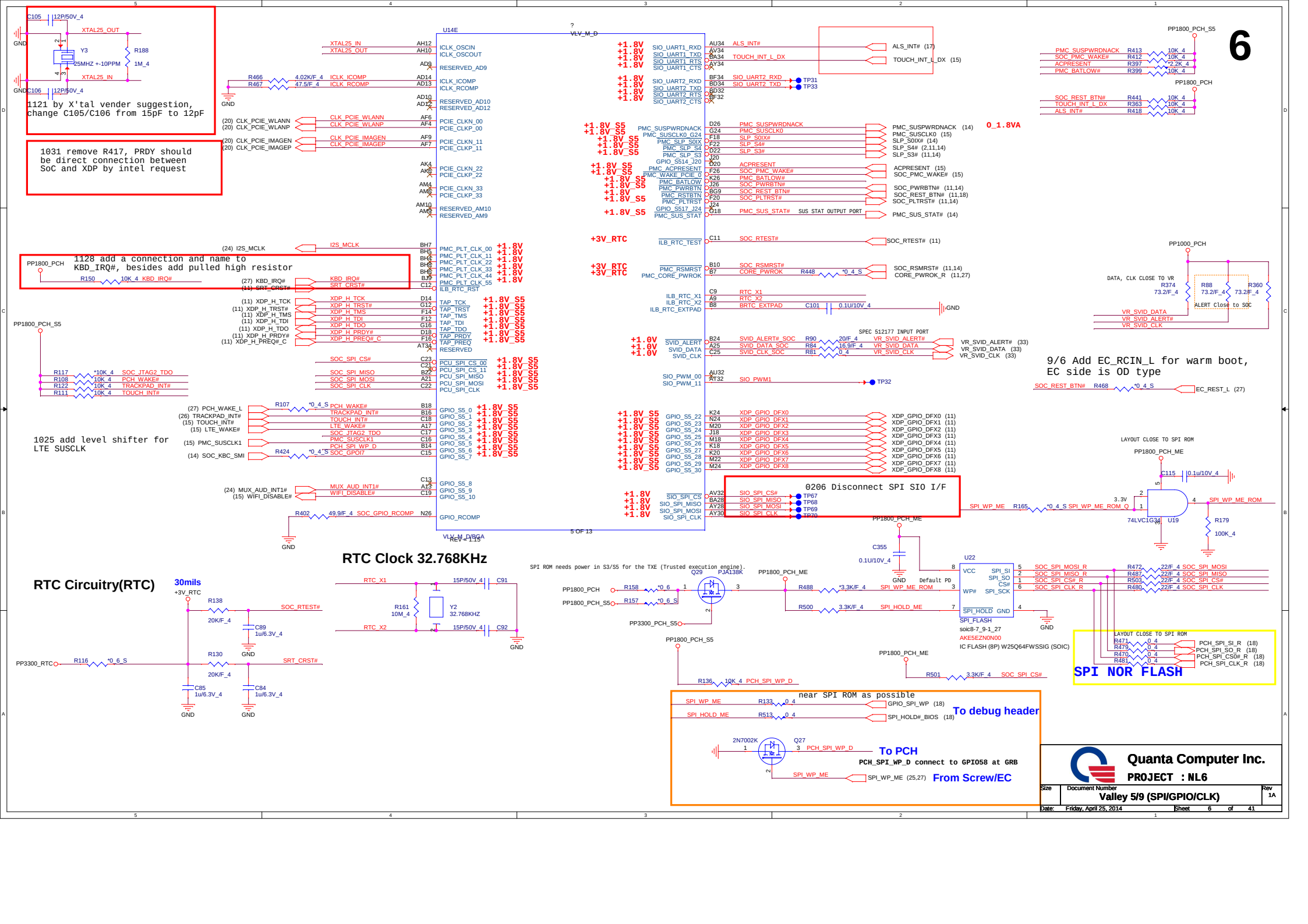
6
1121 by X'tal vender suggestion, change C105/C106 from 15pF to 12pF
1031 remove R417, PRDY should be direct connection between SoC and XDP by intel request
1128 add a connection and name to KBD_IRQ#, besides add pulled high resistor
1025 add level shifter for LTE SUSCLK
9/6 Add EC_RCIN_L for warm boot, EC side is OD type
0206 Disconnect SPI SIO I/F
RTC Clock 32.768KHz
RTC Circuitry(RTC)
30mils
SPI NOR FLASH
near SPI ROM as possible
To debug header
To PCH
From Screw/EC
PCH_SPI_WP_D connect to GPIO58 at GRB
SPI ROM needs power in S3/S5 for the TXE (Trusted execution engine).
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Valley 5/9 (SPI/GPIO/CLK)
Rev 1A
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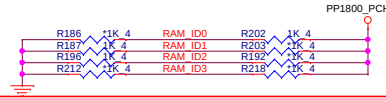
RAM ID

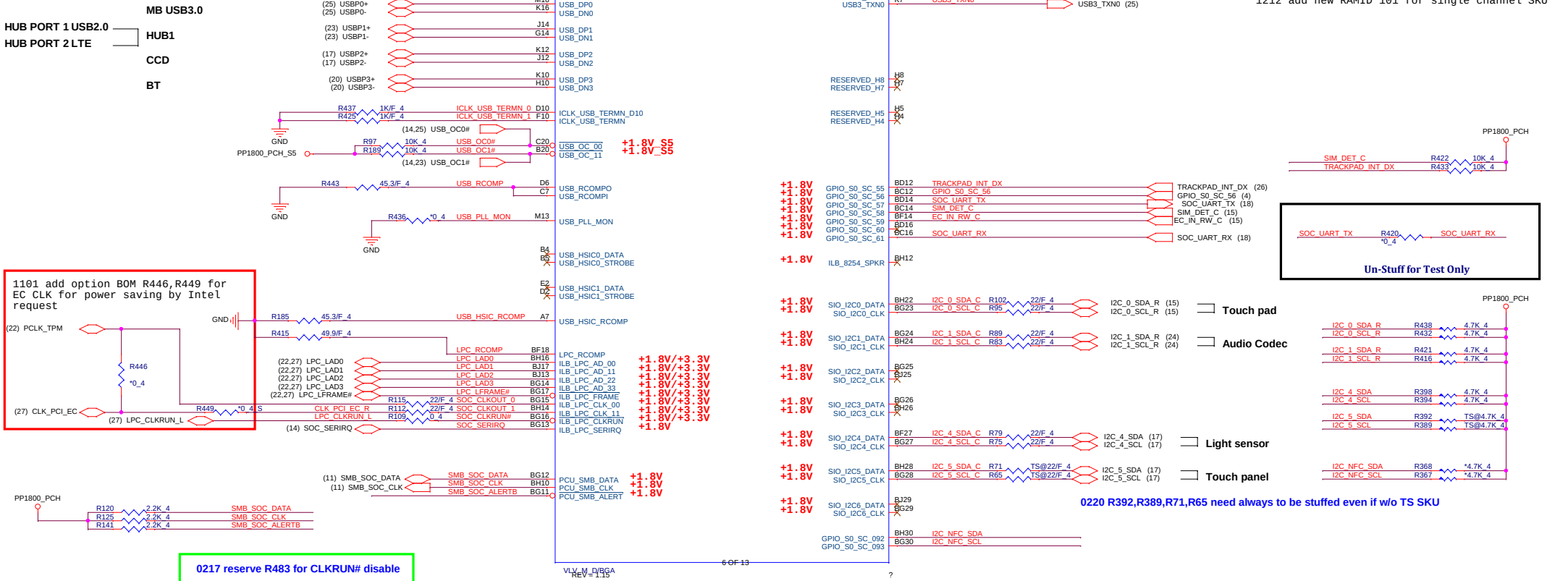


7

0220 reserve placeholder R212,R218
for additional RAM ID

Vender	RAM_ID	Q PN	Mfr. PN	Freq.	Size	Total Size
Micron	000	AKD5JGSTL02	MT41K256M16HA-125:E	1600MHz	4Gb	4GB
Hynix	001	AKD5JGETW00	H5TC4G63AFR-PBA	1600MHz	4Gb	4GB
Micron	010	AKD5DGSTL02	MT41K128M16JT-125:K	1600MHz	2Gb	2GB
Hynix	011	AKD5MG0TW02	H5TC2G63FFR-PBA	1600MHz	2Gb	2GB
Micron	100	AKD5JGSTL02	MT41K256M16HA-125:E	1600MHz	4Gb	2GB
Hynix	101	AKD5JGETW00	H5TC4G63AFR-PBA	1600MHz	4Gb	2GB

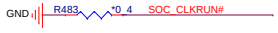
Proto1/1.5 stage use H2G & H4G
1212 add new RAMID 101 for single channel SKU



1101 add option BOM R446,R449 for EC CLK for power saving by Intel request

0220 R392,R389,R71,R65 need always to be stuffed even if w/o TS SKU

0217 reserve R483 for CLKRUN# disable



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1031 for layout suggestion by intel, VSS_AXG_SENSE didn't connect to VSS_SENSE, will connect the GND via near VCC_AXG_SENSE

1031 for layout, add 0hm between GND and VSS_AXG_SENSE

(33) VSS_AXG_SENSE — R385 *0_4_S — GND

+VCC_GFX +VCC_CORE

R458 100/F_4 R373 100/F_4

VCC_SENSE
VCC_AXG_SENSE
VSS_SENSE

R382 100/F_4 — GND

(33) VCC_SENSE — VCC_SENSE — P28
(33) VCC_AXG_SENSE — VCC_AXG_SENSE — BB8
(33) VSS_SENSE — VSS_SENSE — N28

PP1350 — R343 *0_4_S — PP1350_VSM — AD38
C231 1U/6.3V_4
C251 1U/6.3V_4
C38 0.1U/10V_4
GND
AF38 A48 AK38 AM38 AV41 AV42 BB46

PP1350

+VCC_CORE — AA27 AA29 AA30 AC27 AC29 AC30 AD27 AD29 AD30 AF27 AF29 AG27 AG29 AG30 P26 P27 U27 U29 V27 V29 V30 Y27 Y29 Y30

1030 for core power, change C271,C281,C280,C278,C273 to 10uF

1206 change C271,C273,C280 to 0603 22uF for ACLL issue

1204 for z-height issue, change C72,C75,C81 to 0.85mm cap

C271	22u/6.3V_6	
C281	10u/6.3V_4	
C280	22u/6.3V_6	
C278	10u/6.3V_4	
C273	22u/6.3V_6	
C72	22u/6.3V_8	
C83	22u/6.3V_8	
C75	22u/6.3V_8	
C81	22u/6.3V_8	
C79	22u/6.3V_8	
C80	22u/6.3V_8	
C76	22u/6.3V_8	

GND

U14G — ? VLV_M_D

CORE_VCC_SENSE_P28
UNCORE_VNN_SENSE
CORE_VSS_SENSE_N28

DRAM_VDD_S4_AD38
DRAM_VDD_S4_AF38
DRAM_VDD_S4
DRAM_VDD_S4_AK38
DRAM_VDD_S4_AM38
DRAM_VDD_S4_AV41
DRAM_VDD_S4_AV42
DRAM_VDD_S4_BB46

CORE_VCC_S0IX_AA27
CORE_VCC_S0IX_AA29
CORE_VCC_S0IX_AA30
CORE_VCC_S0IX_AC27
CORE_VCC_S0IX_AC29
CORE_VCC_S0IX_AC30
CORE_VCC_S0IX_AD27
CORE_VCC_S0IX_AD29
CORE_VCC_S0IX_AD30
CORE_VCC_S0IX_AF27
CORE_VCC_S0IX_AF29
CORE_VCC_S0IX_AG27
CORE_VCC_S0IX_AG29
CORE_VCC_S0IX_AG30
CORE_VCC_S0IX_P26
CORE_VCC_S0IX_P27
CORE_VCC_S0IX_U27
CORE_VCC_S0IX_U29
CORE_VCC_S0IX_V27
CORE_VCC_S0IX_V29
CORE_VCC_S0IX_V30
CORE_VCC_S0IX_Y27
CORE_VCC_S0IX_Y29
CORE_VCC_S0IX_Y30

AF30 — TP_CORE_V1P05_S4

DRAM_VDD_S4_BD49
DRAM_VDD_S4_BD52
DRAM_VDD_S4_BD53
DRAM_VDD_S4_BF44
DRAM_VDD_S4_BG51
DRAM_VDD_S4_BJ48
DRAM_VDD_S4_C51
DRAM_VDD_S4_D44
DRAM_VDD_S4_F49
DRAM_VDD_S4_F52
DRAM_VDD_S4_F53
DRAM_VDD_S4_H46
DRAM_VDD_S4_M41
DRAM_VDD_S4_M42
DRAM_VDD_S4_V38
DRAM_VDD_S4_Y38

UNCORE_VNN_S3_AA24
UNCORE_VNN_S3_AC22
UNCORE_VNN_S3_AC24
UNCORE_VNN_S3_AD22
UNCORE_VNN_S3_AD24
UNCORE_VNN_S3_AF22
UNCORE_VNN_S3_AF24
UNCORE_VNN_S3_AG22
UNCORE_VNN_S3_AG24
UNCORE_VNN_S3_AJ22
UNCORE_VNN_S3_AJ24
UNCORE_VNN_S3_AK22
UNCORE_VNN_S3_AK24
UNCORE_VNN_S3_AK25
UNCORE_VNN_S3_AK27
UNCORE_VNN_S3_AK29
UNCORE_VNN_S3_AK30
UNCORE_VNN_S3_AK32
UNCORE_VNN_S3_AM22

TP2_CORE_VCC_S0IX — AA22

7 OF 13

VLV_M_D/BGA

PP1350

BD49 BD52 BD53 BF44 BG51 BJ48 C51 D44 F49 F52 F53 H46 M41 M42 V38 Y38

C235 1U/6.3V_4 C240 1U/6.3V_4 C236 1U/6.3V_4 C237 1U/6.3V_4 C238 1U/6.3V_4 C239 1U/6.3V_4

GND

+VCC_GFX

AA24 AC22 AC24 AD22 AD24 AF22 AF24 AG22 AG24 AJ22 AJ24 AK22 AK24 AK25 AK27 AK29 AK30 AK32 AM22

C69 10U/6.3V_6 C65 10U/6.3V_6 C68 10U/6.3V_6

GND

C63 22u/6.3V_8 C70 22u/6.3V_8 C64 22u/6.3V_8

C266 22u/6.3V_6 C289 10u/6.3V_4 C290 10u/6.3V_4 C311 22u/6.3V_6 C315 22u/6.3V_6

1030 for Gfx power, change C266,C289,C290 to 10uF and add 2 caps 10uF

1206 change C266,C311,C315 to 0603 22uF for ACLL issue

1030 change C60 power netname for layout

+VCC_GFX

C60 22u/6.3V_8

REV = 1.15

1031 remove TP44 and TP35 for GND vias adding

Quanta Computer Inc.
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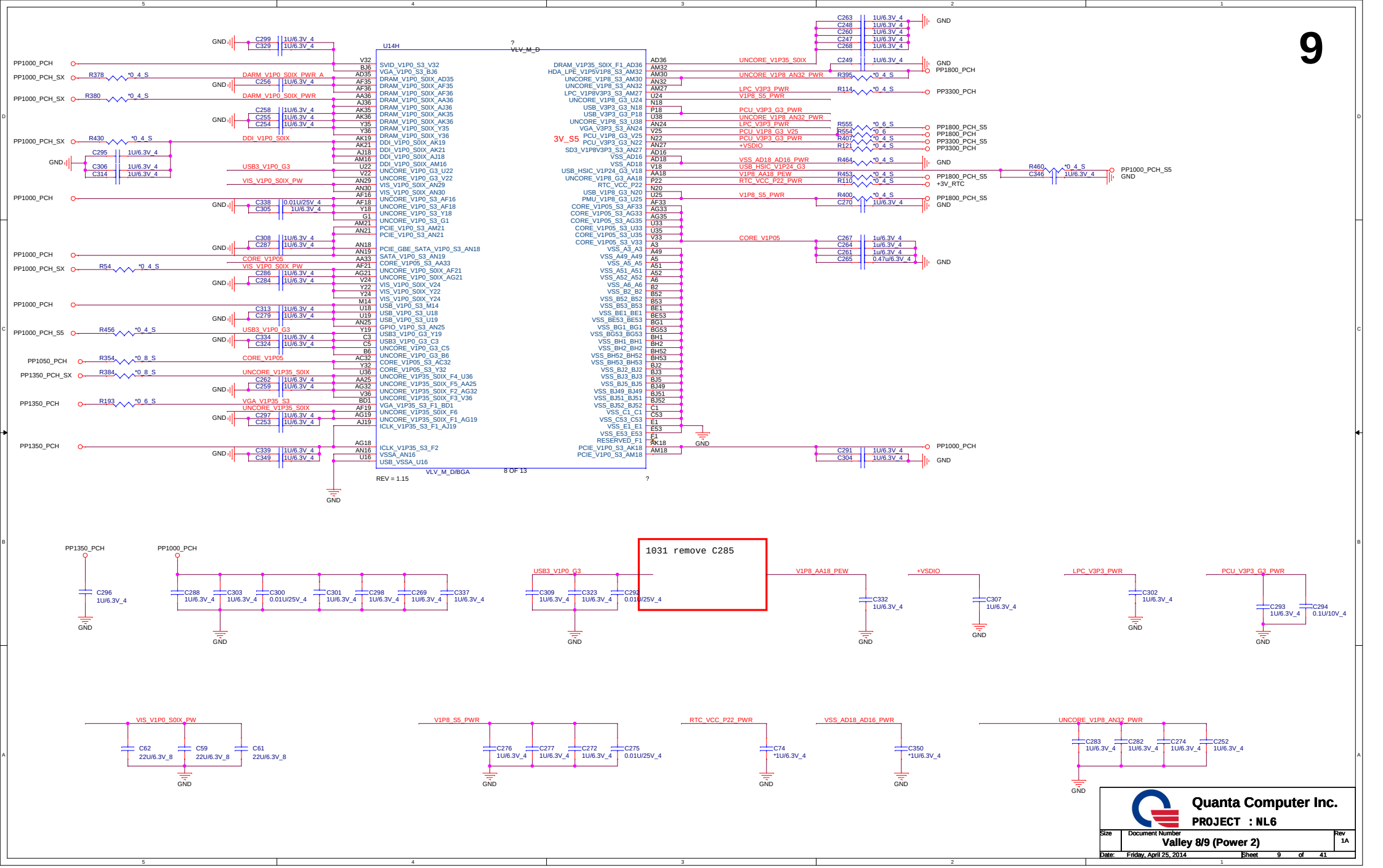
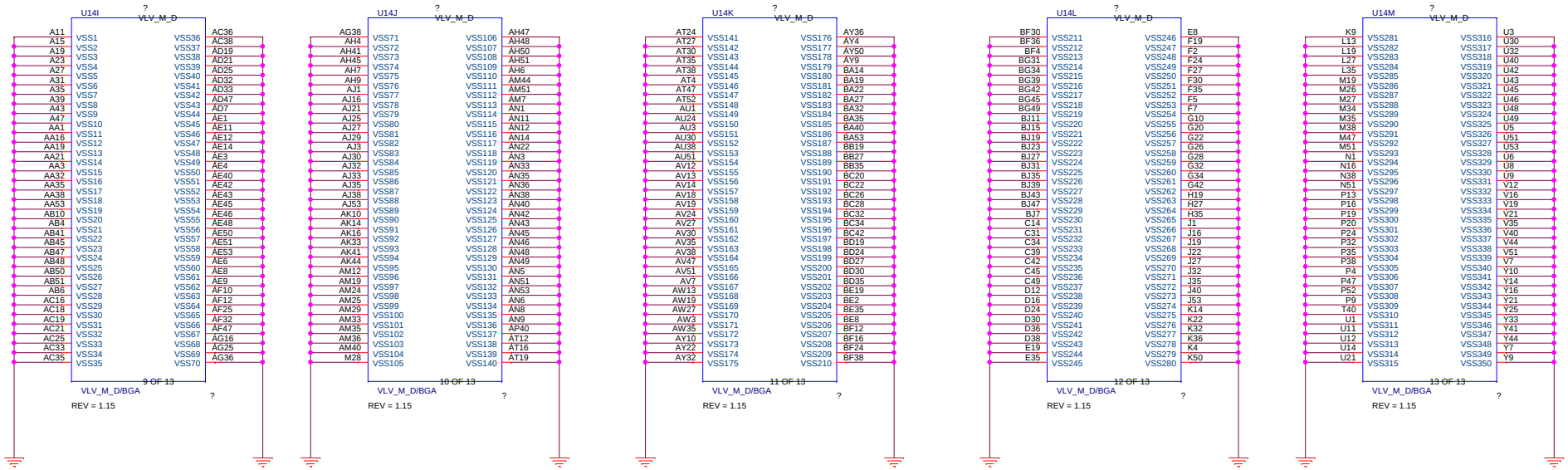
Size	Document Number	Rev
	Valley 7/9 (Power 1)	1A

Date: Friday, April 25, 2014 Sheet 8 of 41


9
U14H
VLV_M_D
VLV_M_D/BGA
8 OF 13
REV = 1.15
1031 remove C285
Quanta Computer Inc.
PROJECT : NL6
Valley 8/9 (Power 2)
Size
Document Number
Rev
1A
Date: Friday, April 25, 2014
Sheet 9 of 41



Quanta Computer Inc.

PROJECT : NL6

Size	Document Number	Rev
	Valley 9/9 (GND)	1A

Date: Friday, April 25, 2014 Sheet 10 of 41

INTEL Debug Port

11

CN13

*SEC_BSH-030-01-L-D-A-TR

PP1800_PCH_S5 R337 *0_6 PP1800_XDP_AB
PP1000_PCH_S5 R334 *0_6
PP1800_PCH R333 *0_4_S PP1800_XDP_CD

XDP_H_PREQ# XDP_H_PRDY# (6) XDP_H_PRDY#
XDP_GPIO_DFX1 XDP_GPIO_DFX2 (6) XDP_GPIO_DFX1 (6) XDP_GPIO_DFX2
XDP_GPIO_DFX3 XDP_GPIO_DFX4 (6) XDP_GPIO_DFX3 (6) XDP_GPIO_DFX4
XDP_GPIO_DFX5 XDP_GPIO_DFX6 (6) XDP_GPIO_DFX5 (6) XDP_GPIO_DFX6
XDP_GPIO_DFX7 XDP_GPIO_DFX8 (6) XDP_GPIO_DFX7 (6) XDP_GPIO_DFX8

XDP_GPIO_S0_NC15 XDP_GPIO_DFX0 XDP_GPIO_S0_NC15 (4) XDP_GPIO_DFX0 (6)
XDP_GPIO_S0_NC16 XDP_GPIO_S0_NC17 XDP_GPIO_S0_NC16 (4) XDP_GPIO_S0_NC17 (4)
XDP_GPIO_S0_NC18 XDP_GPIO_S0_NC19 XDP_GPIO_S0_NC18 (4) XDP_GPIO_S0_NC19 (4)
XDP_GPIO_S0_NC20 XDP_GPIO_S0_NC21 XDP_GPIO_S0_NC20 (4) XDP_GPIO_S0_NC21 (4)
XDP_GPIO_S0_NC22 XDP_GPIO_S0_NC23 XDP_GPIO_S0_NC22 (4) XDP_GPIO_S0_NC23 (4)

(6,14) SOC_RSMRST# SOC_RSMRST# R317 1K_4 XDP_RSMRST#
(14,27) PCH_PWRBTN_L PCH_PWRBTN_L R332 *0_4_S XDP_PMU_PWRBTN#
PP1800_XDP_AB (6,27) CORE_PWROK_R CORE_PWROK_R R322 1K_4 XDP_COREPWROK
XDP_RTEST_L R325 0_4 XDP_RTEST#
C199 *0.1u/10V_4
(7) SMB_SOC_DATA SMB_SOC_DATA R320 *0_4_S SMB_XDP_SDA
(7) SMB_SOC_CLK SMB_SOC_CLK R319 *0_4_S SMB_XDP_SCL
(6) XDP_H_TCK XDP_H_TCK

XDP_PMU_PLTRST# R306 1K_4 SOC_PLTRST# SOC_PLTRST# (6,14)
XDP_PMU_RSTBTN# R307 0_4 SOC_REST_BTN# SOC_REST_BTN# (6,18)
XDP_H_TDO XDP_H_TDO (6)
XDP_H_TRST# XDP_H_TRST# (6)
XDP_H_TDI XDP_H_TDI (6)
XDP_H_TMS XDP_H_TMS (6)
XDP_PRESENT_N R263 *0_4_S

PP1800_XDP_CD
C177 *0.1u/10V_4

PP3300_PCH_S5
R528 100K_4
SOC_RTEST# (6)
*2N7002K Q55
*2N7002K Q54
XDP_RTEST_L

PP3300_PCH_S5
GND C186 0.1u/10V_4 XDP_RTEST# R324 1K_4
PLACE C6601 closed to XDP HOOK PIN 54
PP1800_XDP_AB

PLACE R295 WITHIN 0.25" FROM XDP PIN
XDP_H_TDO R295 *51/F_4

PLACE R273,R286,R318 WITHIN 1" FROM SoC PIN
XDP_H_TMS R273 *51/F_4
XDP_H_TDI R286 *51/F_4
XDP_H_TCK R318 *51/F_4
XDP_H_TRST# R289 *51/F_4
XDP_PMU_PWRBTN# R321 *30K/F_4
PLACE R6866 closed to XDP
GND

1031 stuff
R273,R286,R289 for
Intel request

1030 remove PREQ# pulled up resistor R323
1031 put back R323

PP1800_PCH_S5
PLACE R323 WITHIN 1.1" OF BUFFER PIN
XDP_H_PREQ# R323 *200/F_4

1030 U10 change to 74AUP1G34 and stuff it
1031 N.C U10 pin1
1101 stuff C16

PP1800_PCH_S5
C16 0.1u/10V_4
(6) XDP_H_PREQ#_C XDP_H_PREQ#_C
U10 74AUP1G34GW
XDP_H_PREQ#
C15 *0.1u/10V_4
R329 *0_4

PP1800_PCH
GND C160 0.1u/10V_4 XDP_PMU_RSTBTN# R308 *1K_4
PLACE C6866 closed to XDP HOOK PIN48

APS

CN14
*ACES_88511-180N

PP3300_PCH_S5
APS1 R502 *0_6
PMC_SLP_S3# R512 *0_4 SLP_S3# SLP_S3# (6,14)
PMC_SLP_S4# R511 *0_4 SLP_S4# SLP_S4# (2,6,14)
ILB_RTC_RST# R510 *0_4 SRT_CRST# SRT_CRST# (6)
PMC_PWRBTN# R509 *0_4 SOC_PWRBTN# SOC_PWRBTN# (6,14)
PMC_RSTBTN# R508 *0_4 SOC_REST_BTN#

Quanta Computer Inc.
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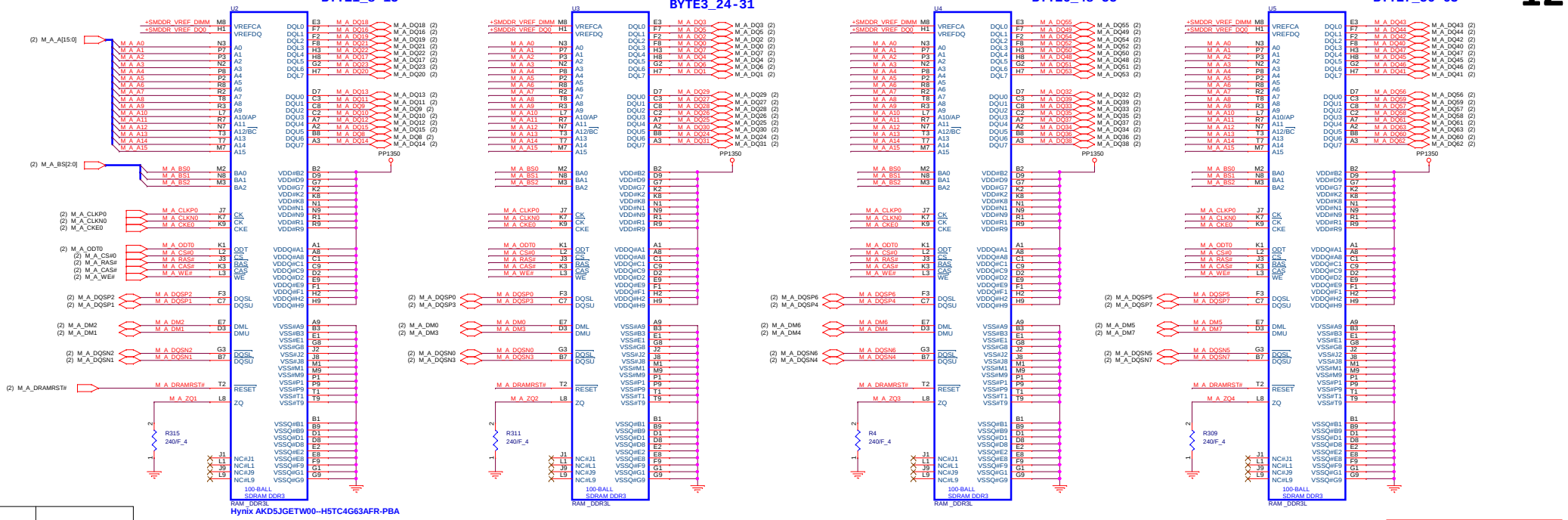
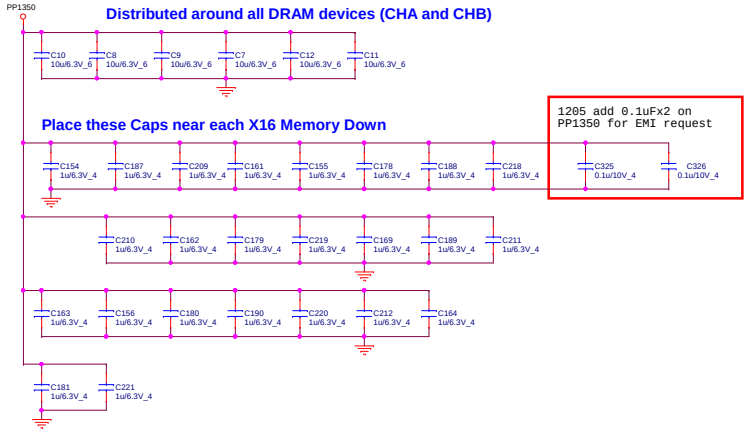
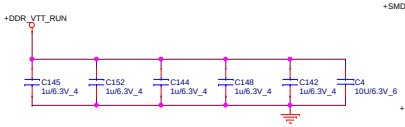
Size	Document Number	Rev
	CPU/PCH XDP	1A
Date: Friday, April 25, 2014	Sheet 11 of 41	

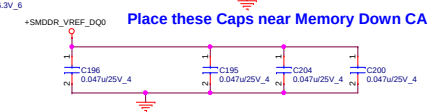
BYTE2_16-23
BYTE1_8-15
BYTE0_0-7
BYTE3_24-31
BYTE4_32-39
BYTE6_48-55
BYTE5_40-47
BYTE7_56-63

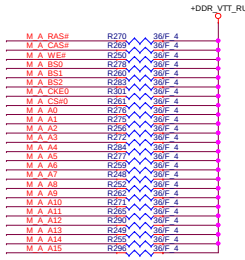


Vendor	P/N	
Hynix		
Elpida	AKD5JGST400	DDR3L 1333Mhz 4Gb
	AKD5JGST404	DDR3L 1600Mhz 4Gb

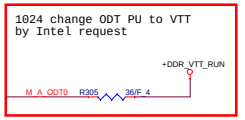


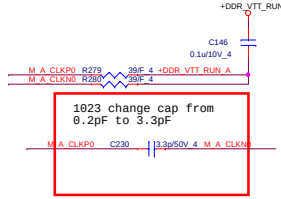




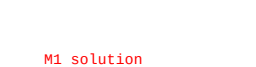


1024 change ODT PU to VTT by Intel request

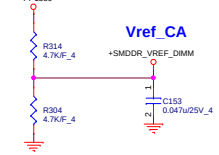




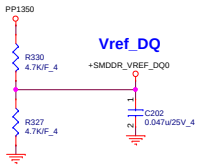
1023 change cap from 0.2pF to 3.3pF



M1 solution



M1 solution



Quanta Computer Inc.
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Size	Document Number	Rev
	DDR3L MEMORY DOWNx16 A	1A
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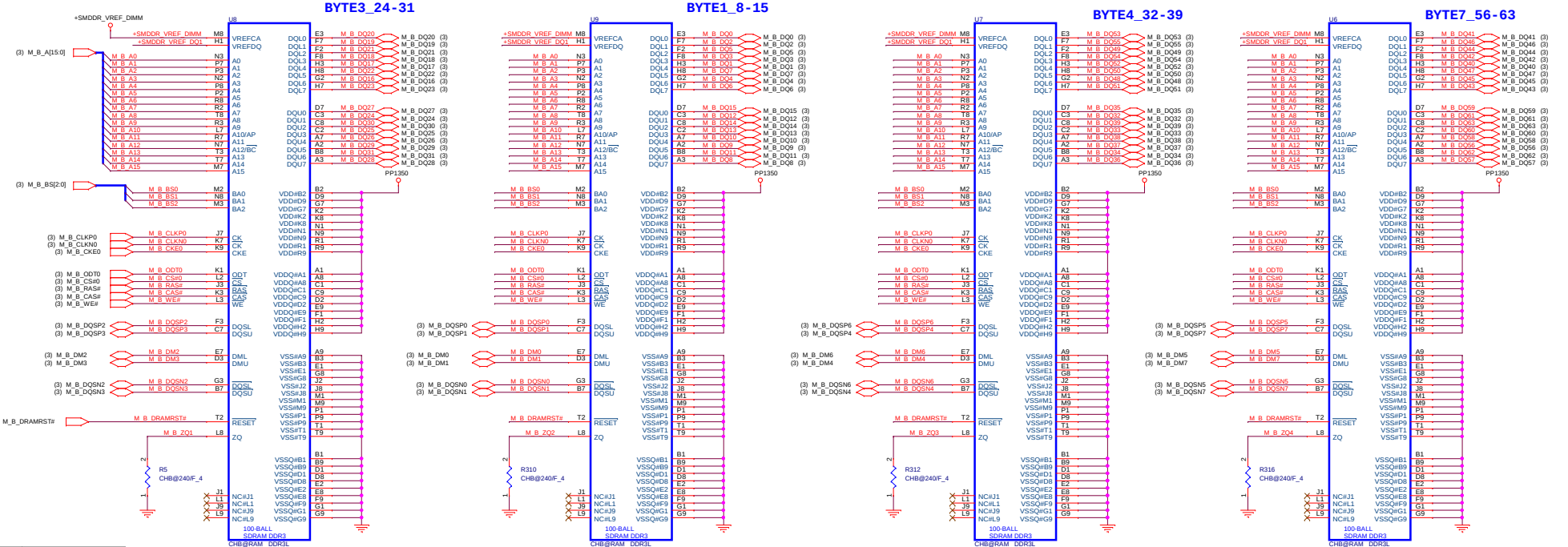
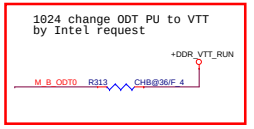
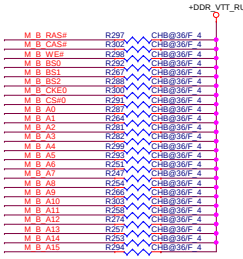
BYTE2_16-23
BYTE3_24-31
BYTE0_0-7
BYTE1_8-15
BYTE6_48-55
BYTE4_32-39
BYTE5_40-47
BYTE7_56-63

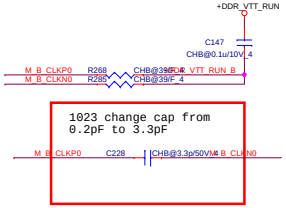


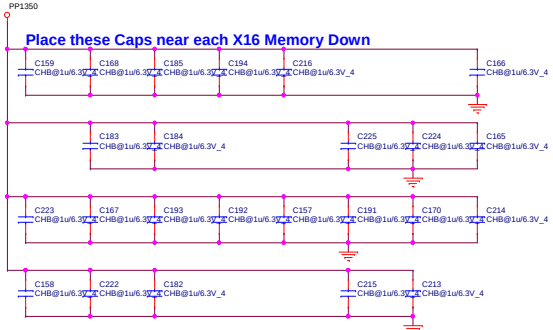
Vendor	P/N	
Micron	AKD5JGSTL02	MT41K256M16HA-125:E
Elpida	AKD5JGST400	
	AKD5JGST404	

1024 change ODT PU to VTT by Intel request

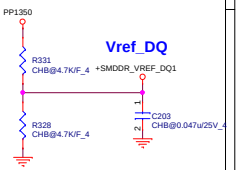


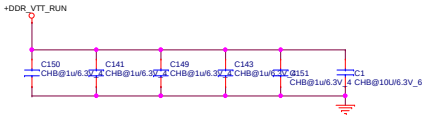


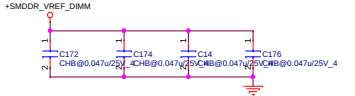


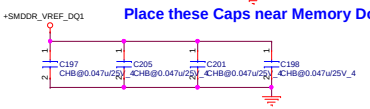


M1 solution









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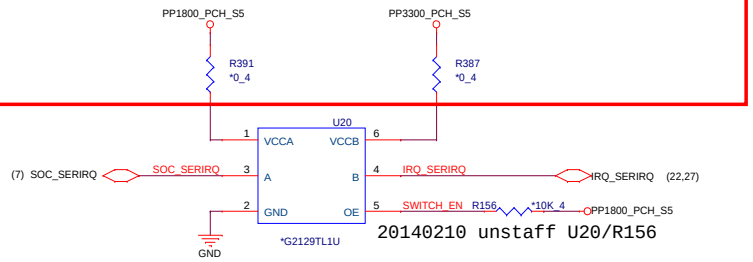
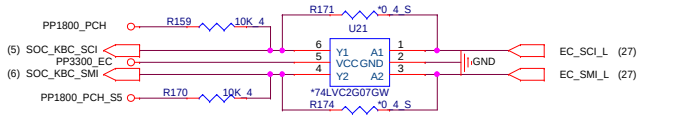
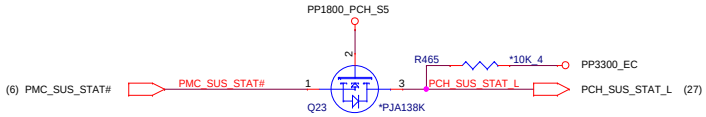
Size	Document Number		Rev
	DDR3L MEMORY DOWNx16 B		1A
Date: Friday, April 25, 2014	Sheet 13 of 41		

PWRON SEQUENCE

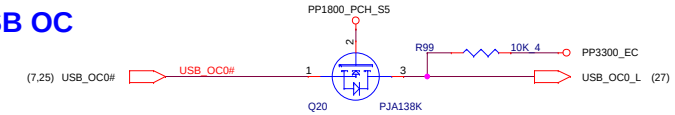
9/6 EC table says SERIRQ is OD pin, reserve for debugging
1128 remove R166, because SERIQR of TPM needs 3V
1128 reserve 0 ohm R387/R391 on VCCA and VCCB for debugging
20140210 unstaff R387/R391

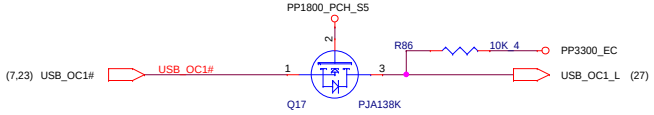






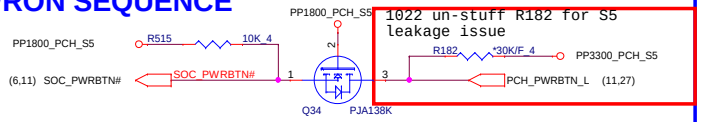
USB OC

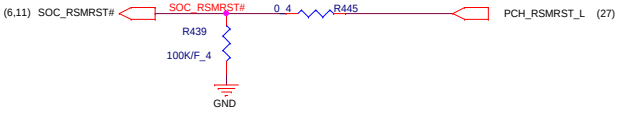


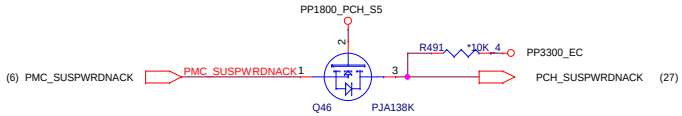


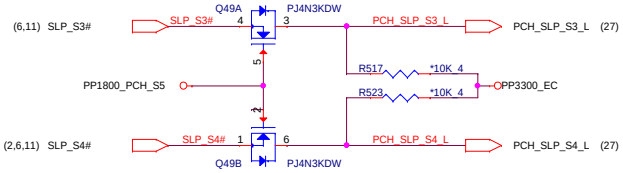
Stuffing for notifying EC

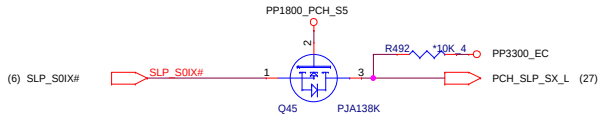
PWRON SEQUENCE

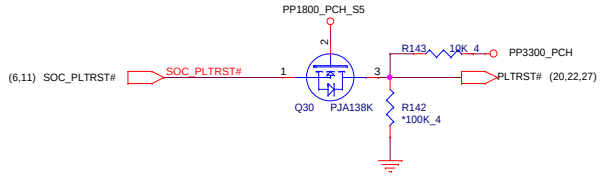












0128 change power rail of Q35,Q36,Q37,Q44 from PP1800_PCH_S5 to PP1800_PCH for PP1800_PCH leakage issue in S3 mode

0206 remove/delete SPI_SIO Interface, Q35,Q36,Q37,Q44,R486,R484,R485, R483,R426,R429,R427,R428

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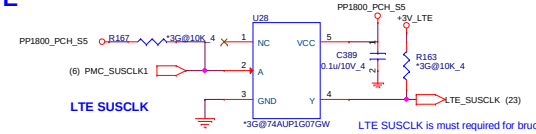
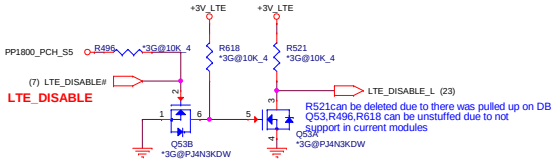
LTE



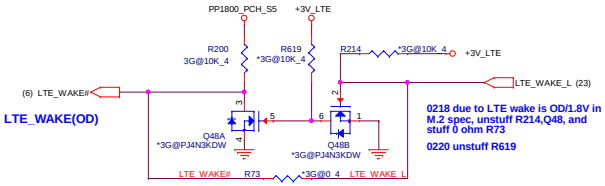
LTE SUSCLK

LTE SUSCLK is must required for bruce modem



LTE_DISABLE

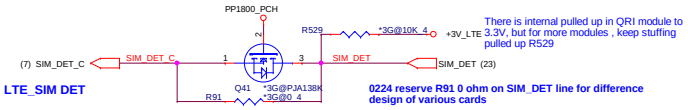
R521can be deleted due to there was pulled up on DB
Q53,R496,R618 can be unstuffed due to not support in current modules



LTE_WAKE(OD)

0218 due to LTE wake is OD/1.8V in M.2 spec, unstuff R214,Q48, and stuff 0 ohm R73

0220 unstuff R619

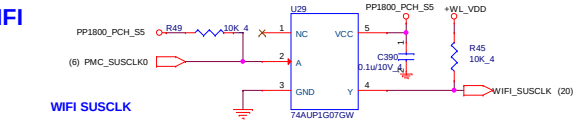


There is internal pulled up in QRI module to 3.3V, but for more modules , keep stuffing pulled up R529

LTE_SIM DET

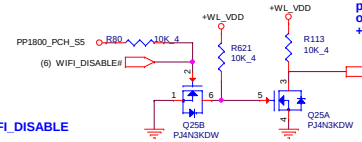
0224 reserve R91 0 ohm on SIM_DET line for difference design of various cards

WIFI

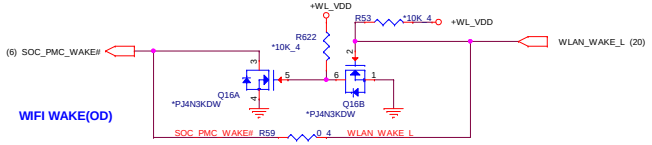


WIFI SUSCLK

0219 for layout smoothly, change pulled up power rail of level shifter of WiFi from PP3300_WLAN to +WL_VDD

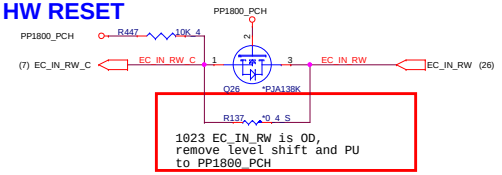


WIFI_DISABLE



WIFI WAKE(OD)

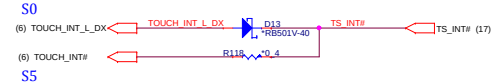
HW RESET



1023 EC_IN_RW is OD, remove level shift and PU to PP1800_PCH

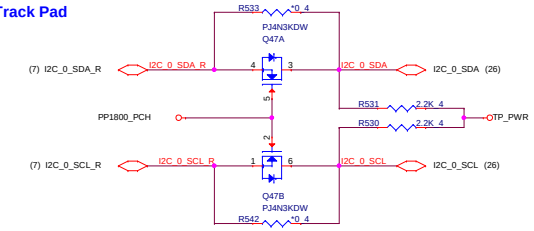
Touch Screen

S0



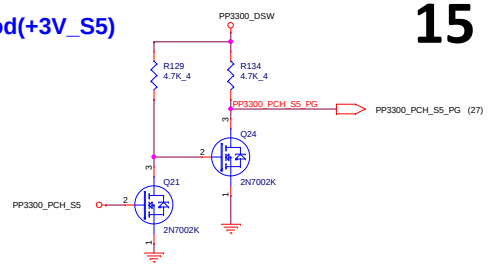
S5

Track Pad



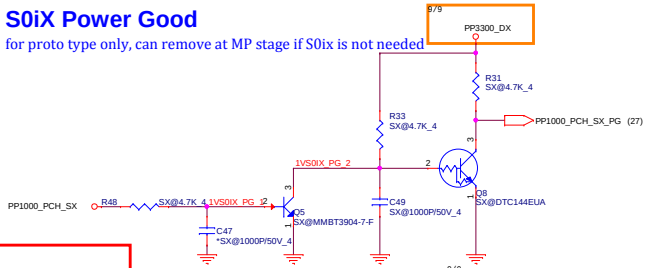
S5 Power Good(+3V_S5)

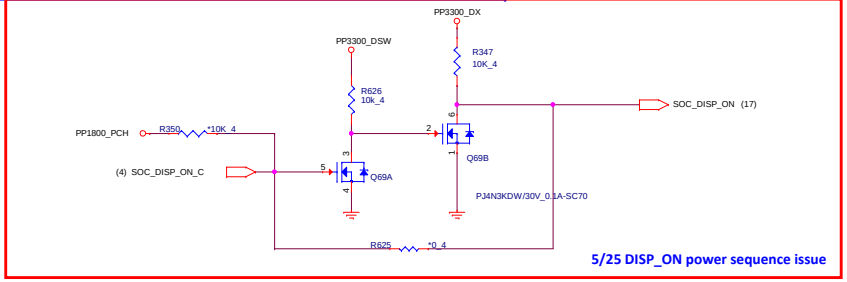
0830 A24



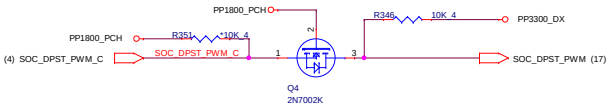
S0iX Power Good

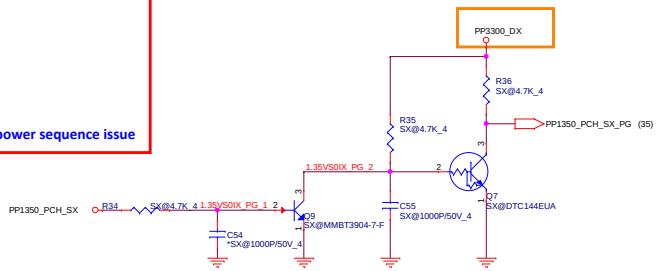
for proto type only, can remove at MP stage if S0ix is not needed



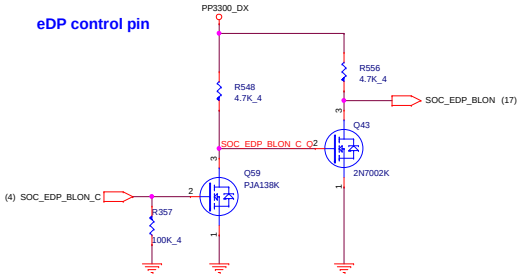


5/25 DISP_ON power sequence issue

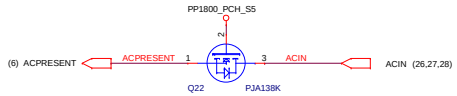




eDP control pin



AC Detect



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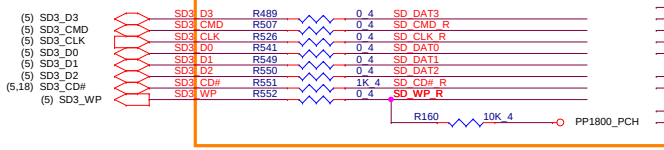
SD/MMC CARD READER CONNECTOR (MMC)

1025 the damping of SDIO change to 0 ohm by Intel request

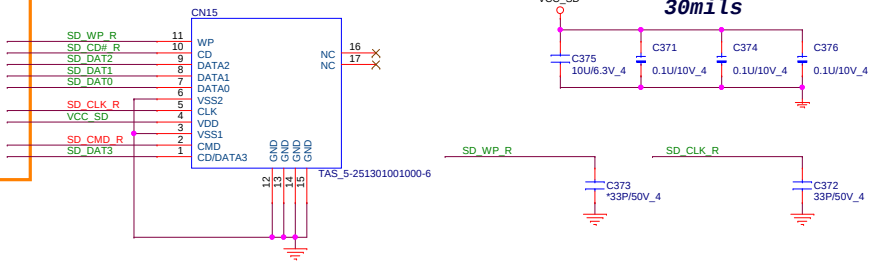
1025 add PU for SDIO WP by Intel request

1205 R551 changes to 1K to isolate SD socket and servo/SoC

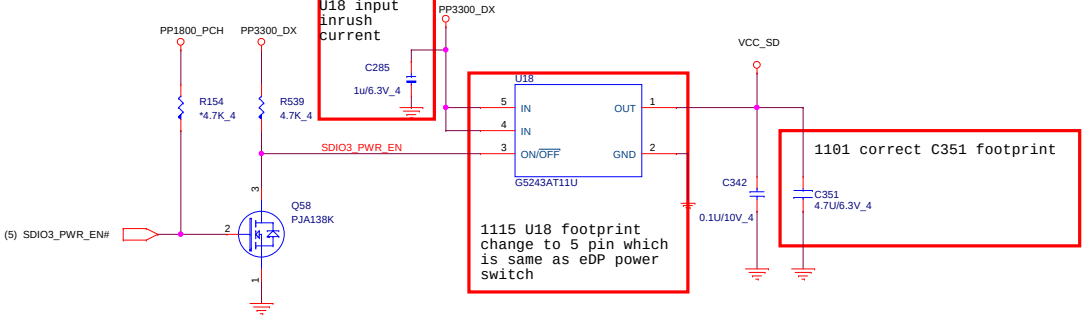
1205 SD3_WP is 1.8V power rail in SoC, change external Pulled up power well of SD3_WP to 1.8V power



This is full size SD card



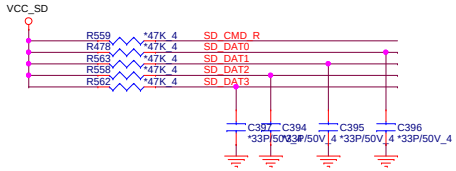
1202 add C285 for U18 input inrush current



1101 correct C351 footprint

1115 U18 footprint change to 5 pin which is same as eDP power switch

1211 add pulled up resistors on SDIO data/cmd lines
1212 all Pulled up resistors of SDIO data/cmd to be un-stuffed



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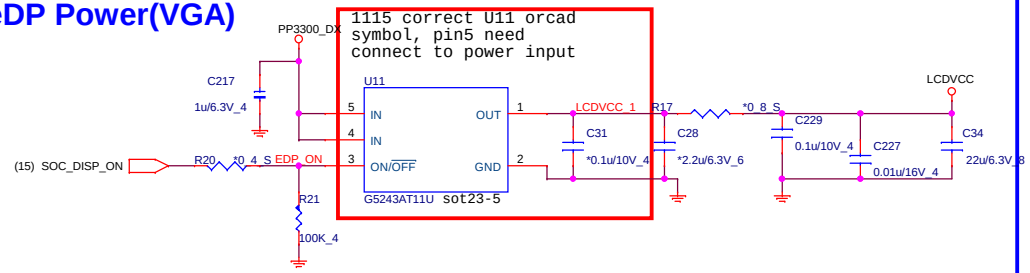
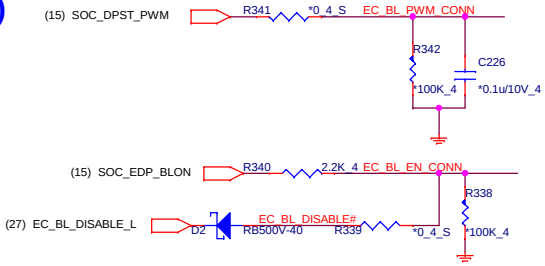
eDP Power(VGA)

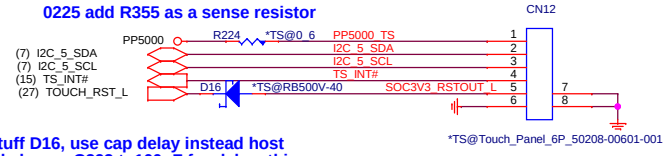


eDP panel control(VGA)



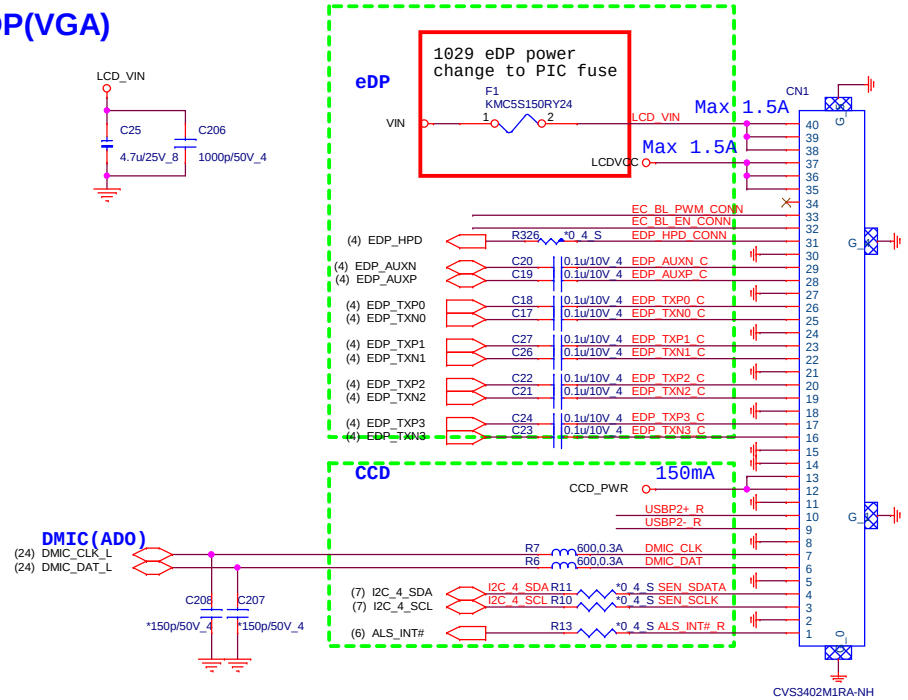
Touch Screen(VGA)

0225 add R355 as a sense resistor

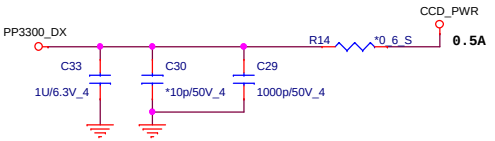


0225 unstuff D16, use cap delay instead host reset, and change C392 to100pF for delay, this value could be adjusted after sequence tuning

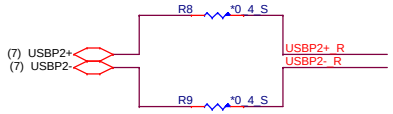
eDP(VGA)



CCD power(CCD)



CCD USB(CCD)



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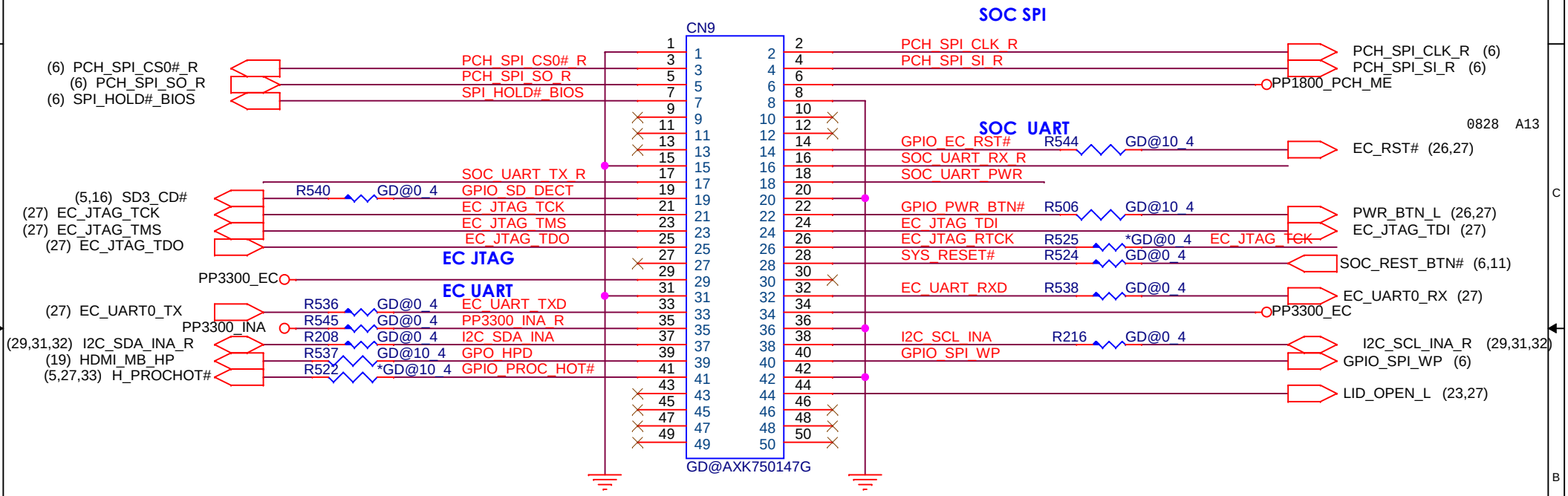
GOOGLE Debug Port(MPC)

50 pin BTB is MUST, don't use 42 pin

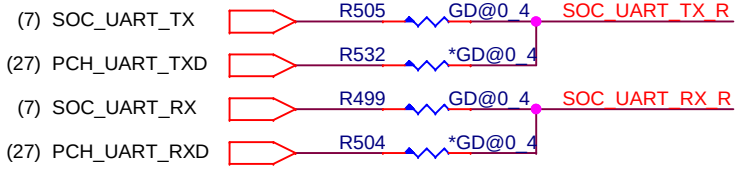
Socket part number AXK750147G

PIN7 OD
PIN14 OD
PIN19 OD
PIN22 OD
PIN28 OD
PIN30 OD
PIN37 OD
PIN38 OD
PIN39 OD
PIN41 OD
PIN43 OD
PIN44 OD
PIN45 OD
PIN46 OD
PIN47 OD
PIN48 OD
PIN49 OD
PIN50 OD

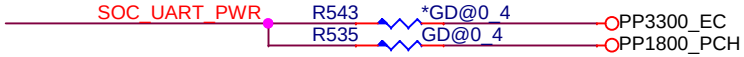
18



1021 change footprint and PN



9/13 add pull up



9/6 using optional instead of level shifted, defult is from SoC

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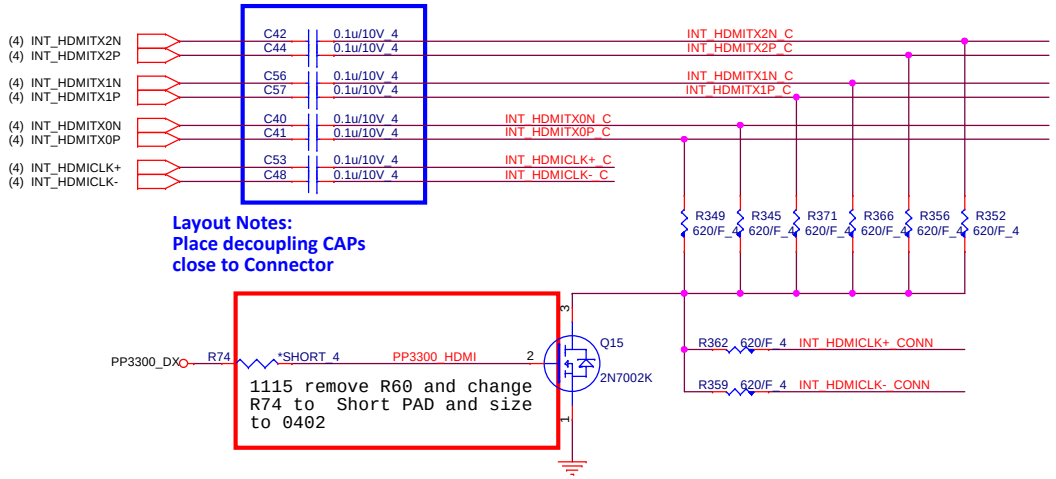
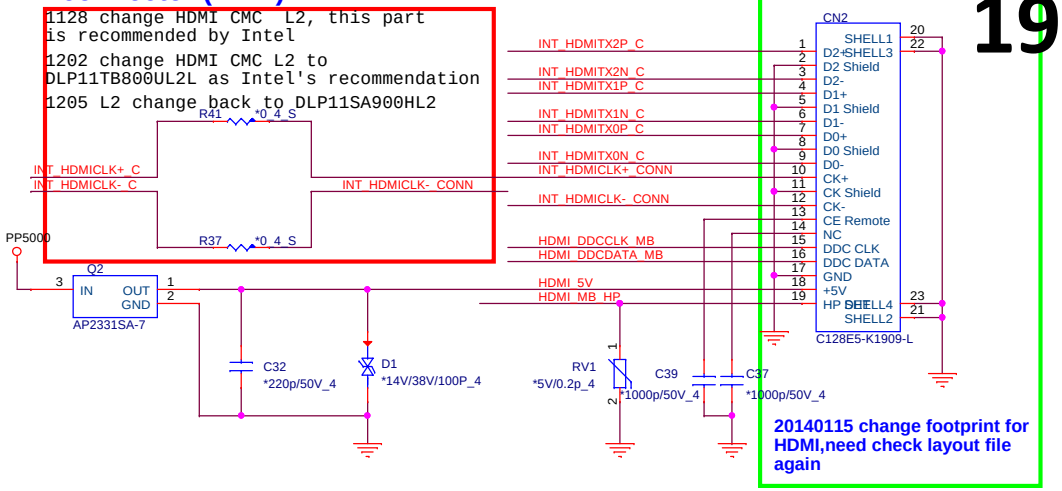
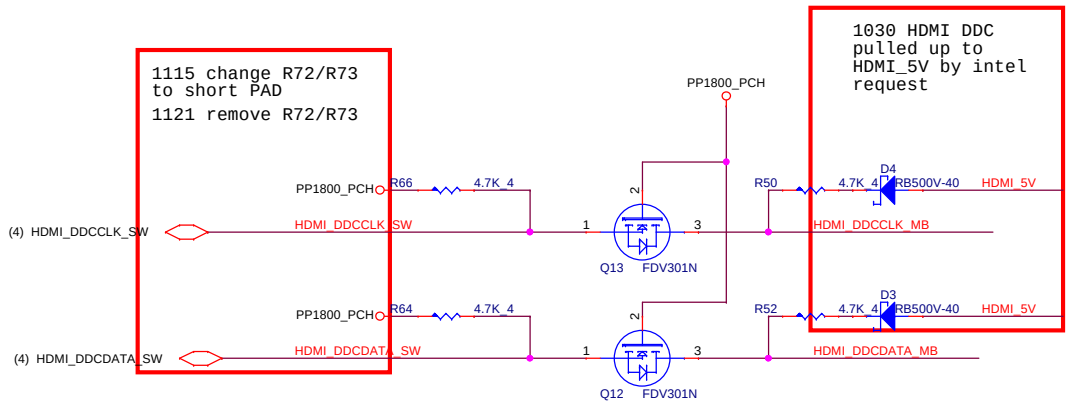
HDMI Cost Reduced level shift (HDM)



HDMI connector (HDM)

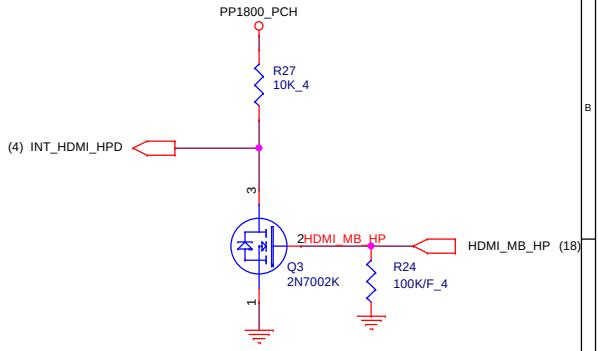


HDMI DDC (HDM)



EMI

HDMI-detect (HDM)



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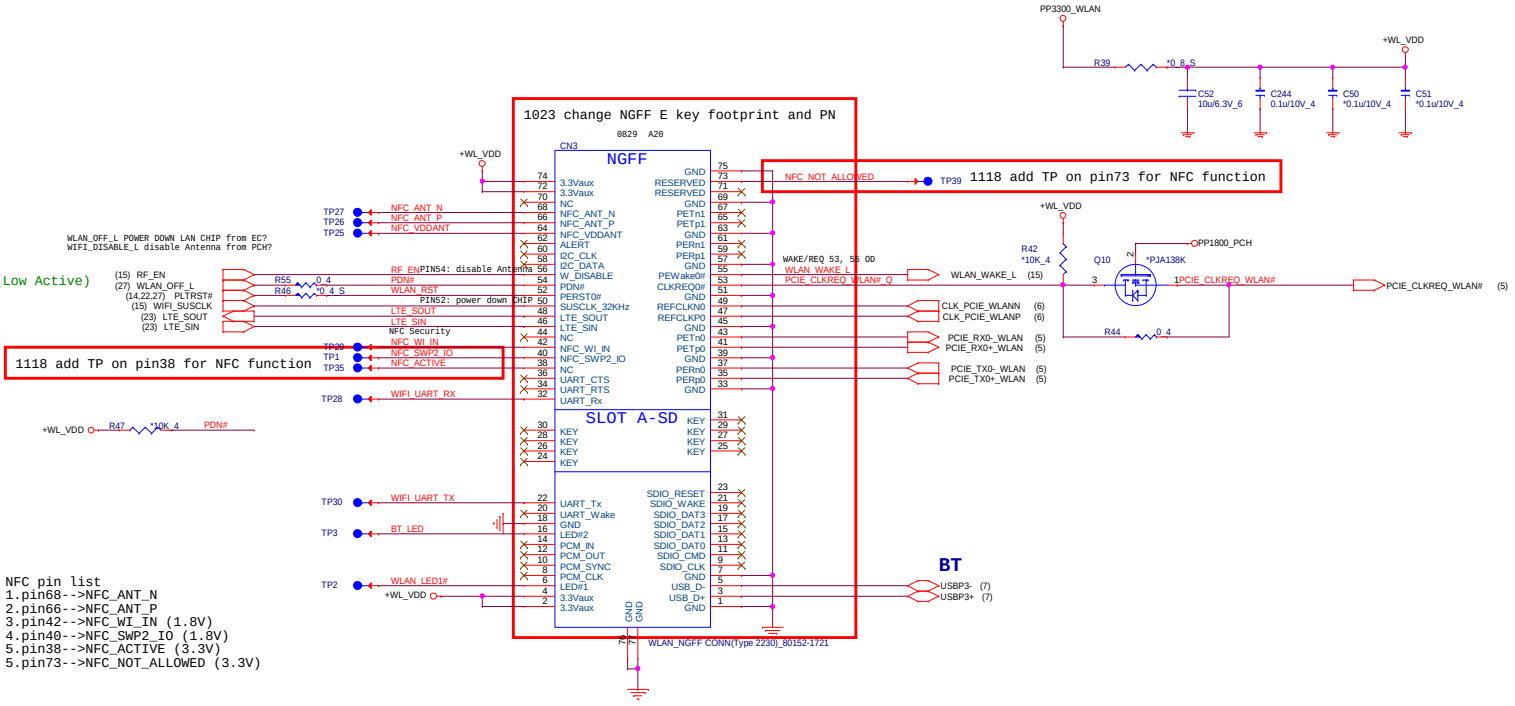
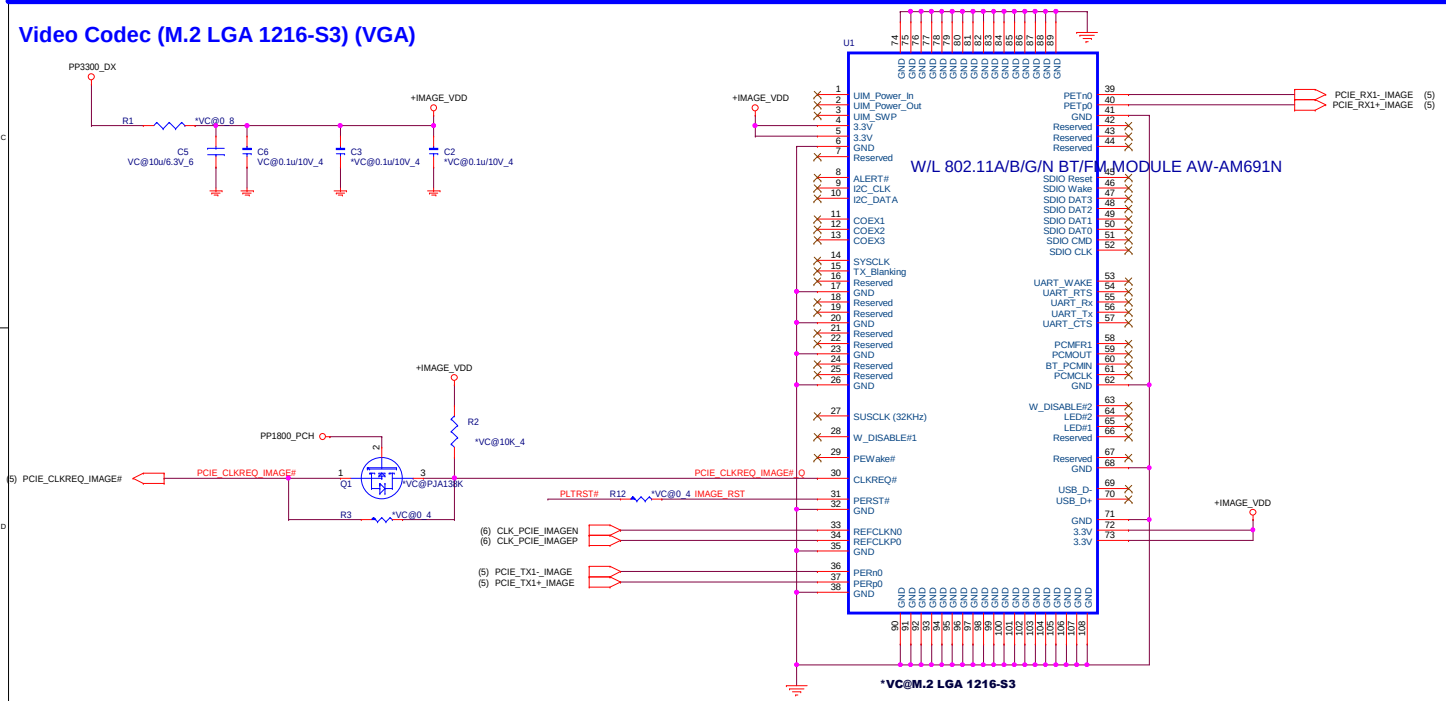
WIFI/BT COMBO (NGFF E KEY)



NFC pin list
1.pin68-->NFC_ANT_N
2.pin66-->NFC_ANT_P
3.pin42-->NFC_WI_IN (1.8V)
4.pin40-->NFC_SWP2_IO (1.8V)
5.pin38-->NFC_ACTIVE (3.3V)
5.pin73-->NFC_NOT_ALLOWED (3.3V)

LTE Coexistence pin list (based on V0.2 spec
1.pin48-->LTE_SOUT (3.3V)
2.pin46-->LTE_SIN (3.3V)

Video Codec (M.2 LGA 1216-S3) (VGA)



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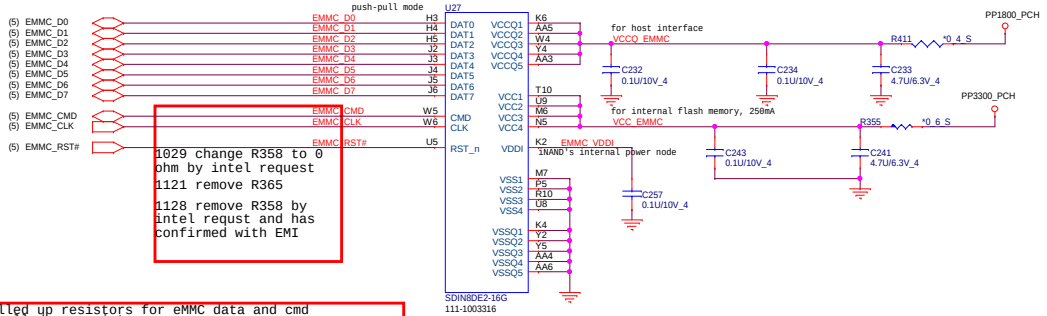
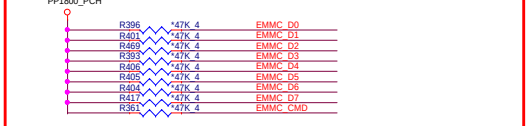
1025 Delete complete SSD(connector and caps)

EMMC (CBS)



1029 remove pulled up resistors for eMMC data and cmd
1211 add back pulled up resistors
1212 all Pulled up resistors of eMMC data/cmd to be un-stuffed, and R361 change to 47K ohm as well



SandisK (16G) 153 pin SDIN8DE2-16G (11.5x13mm) : QPN: AKE3RZ-T101

Quanta Computer Inc.
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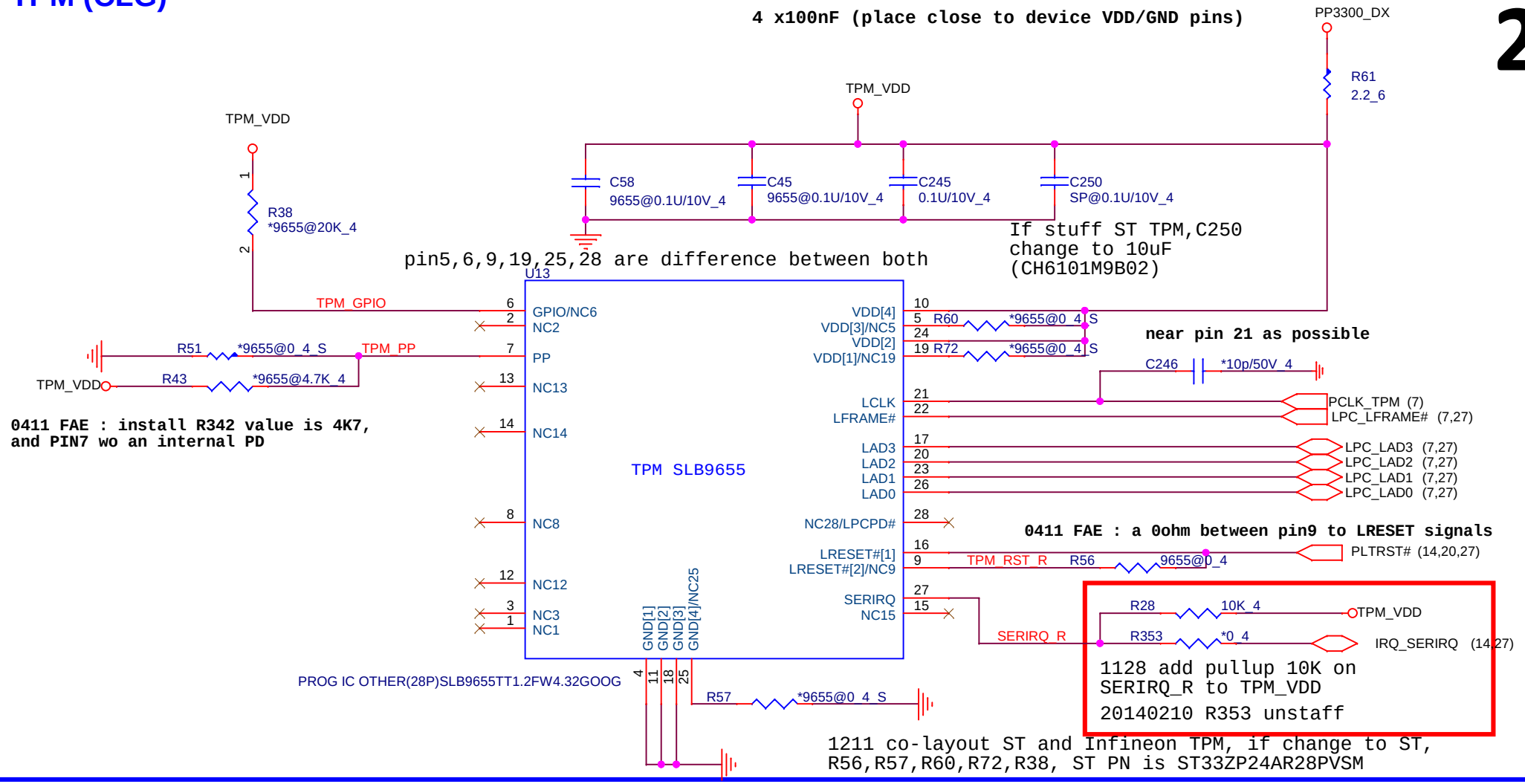
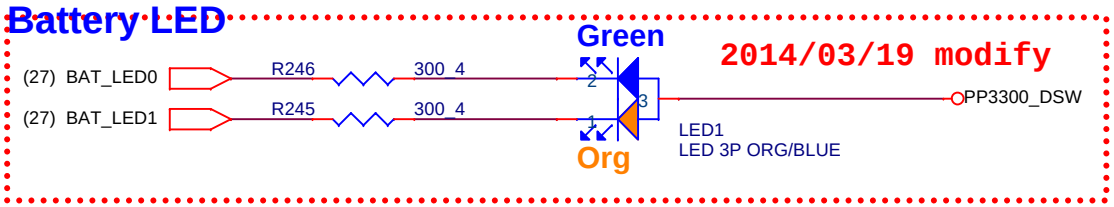
TPM (CLG)



LED(UIF)



0319 Del Power LED

Quanta Computer Inc.

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Size	Document Number	Rev
	TPM SLB9655 / LED	1A

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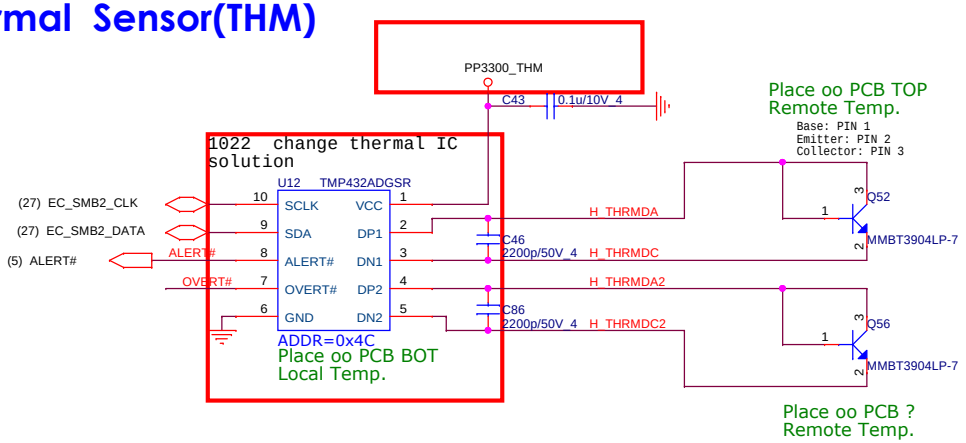
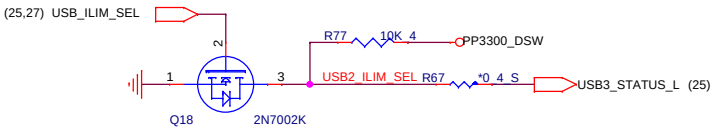
Thermal Sensor(THM)



1030 Thermal IC VDD has two option, ome is PP3300_DSW(=PP3300_EC), another is PP3300_DX, default is stuffing to DSW rail

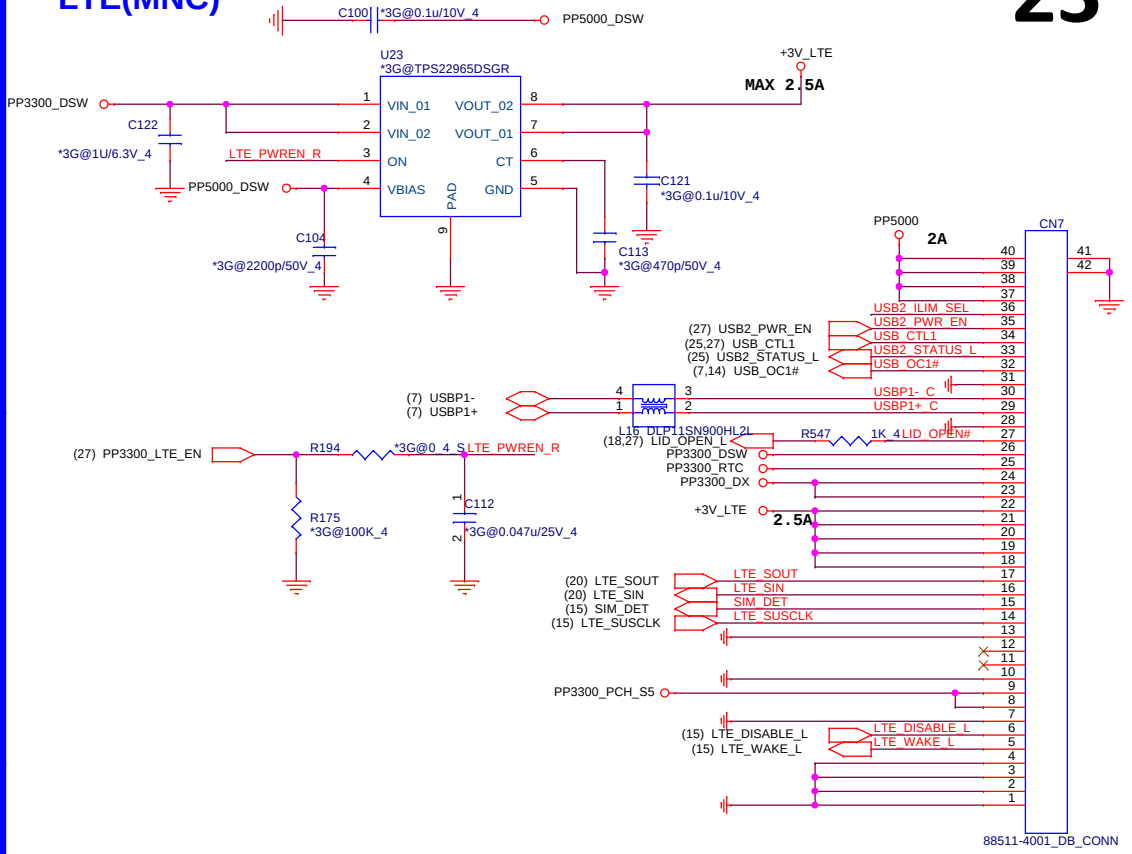
1025 remove Q31 becasue PU to PP3300_DSW at EC side already

USB Switch Current Control



FUNCTION DB
LTE(MNC)

23



Quanta Computer Inc.

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Size	Document Number	Rev
	DB/ALS/Thermal sensor	1A
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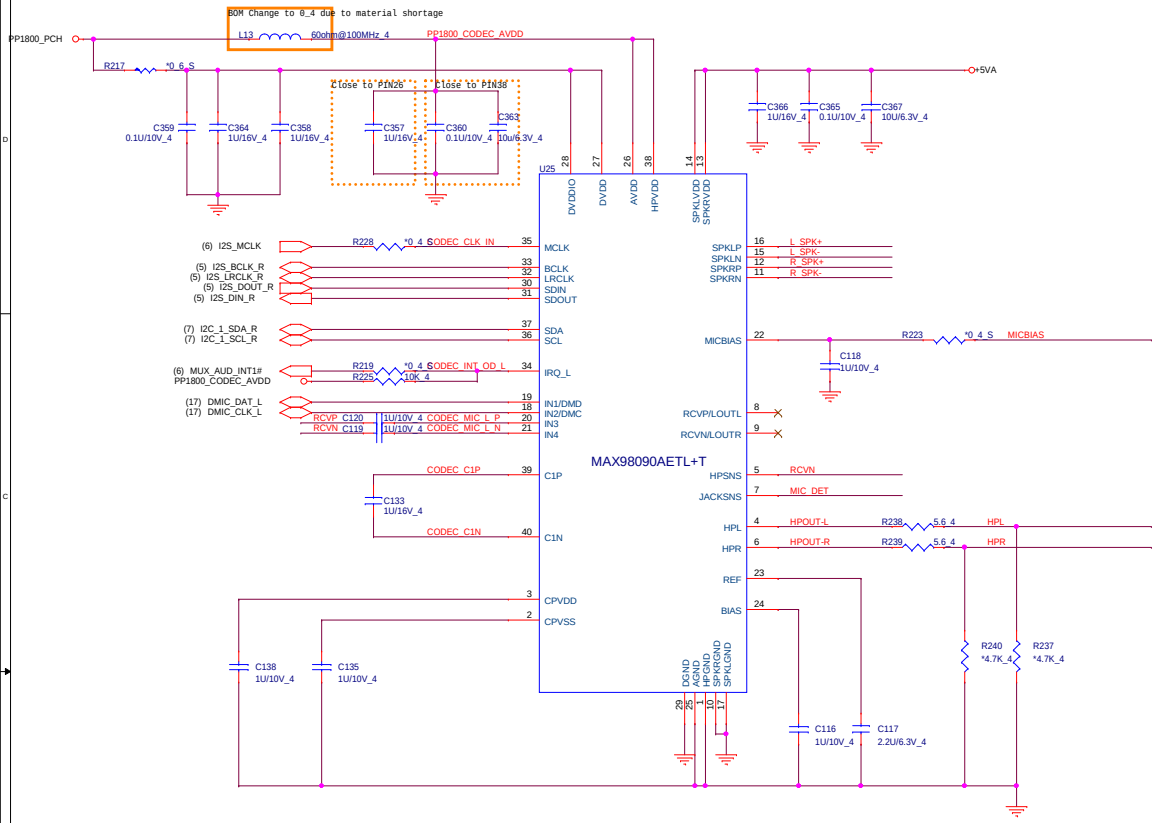
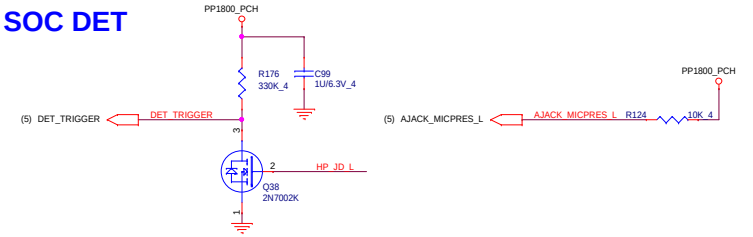
AUDIO CODEC (ADO)



SOC DET



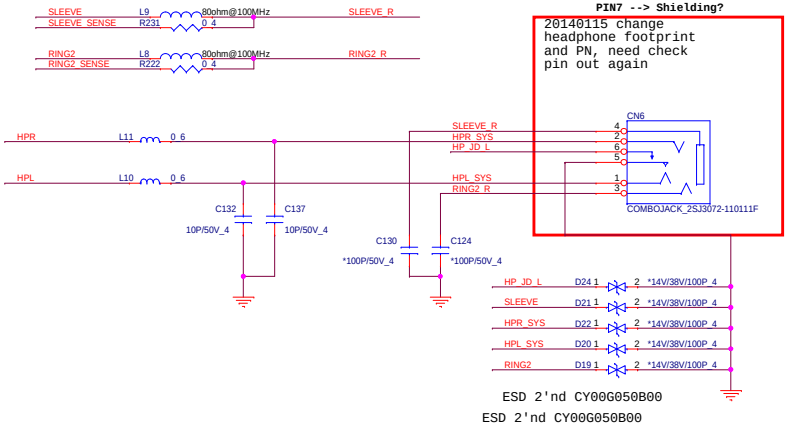
24

HEADPHONE/Mic combo(ADO)

combo jack
Normal open

P/N: DFTJ06FR652
Normal Open
PIN1 --> L?
PIN2 --> R?
PIN3 --> GND/MIC?
PIN4 --> MIC/GND?
PIN5 --> JD?
PIN6 --> GND?
PIN7 --> Shielding?

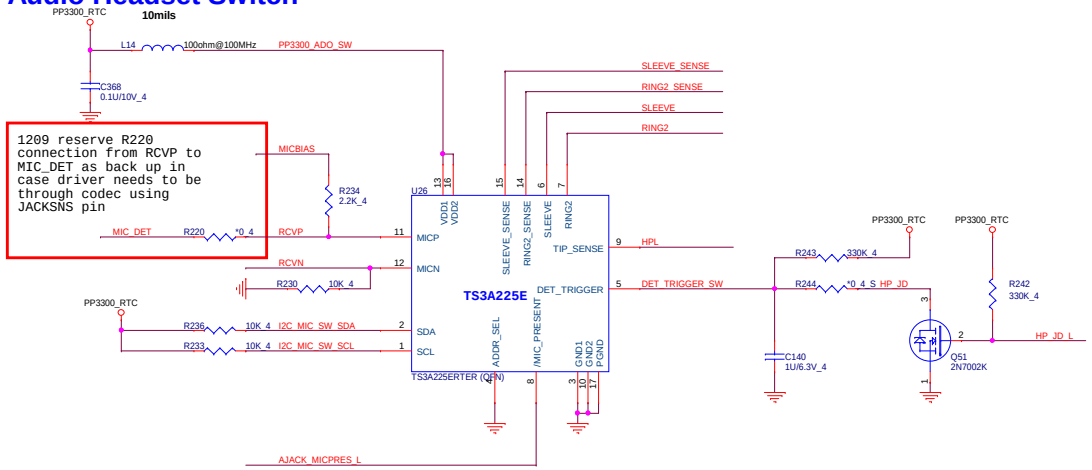
20140115 change
headphone footprint
and PN, need check
pin out again



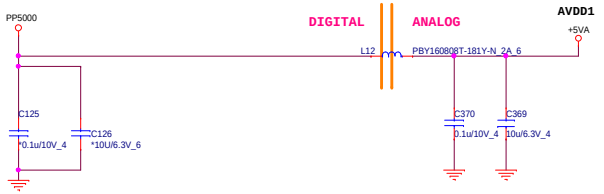
ESD 2'nd CY00G050B00

ESD 2'nd CY00G050B00

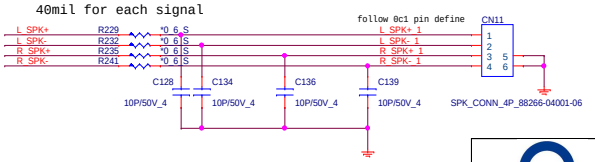
Audio Headset Switch



Codec PWR 5V(ADO)



Internal Speaker



Quanta Computer Inc.
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Size	Document Number	Rev
	MAX98090/HP/SPK	1A

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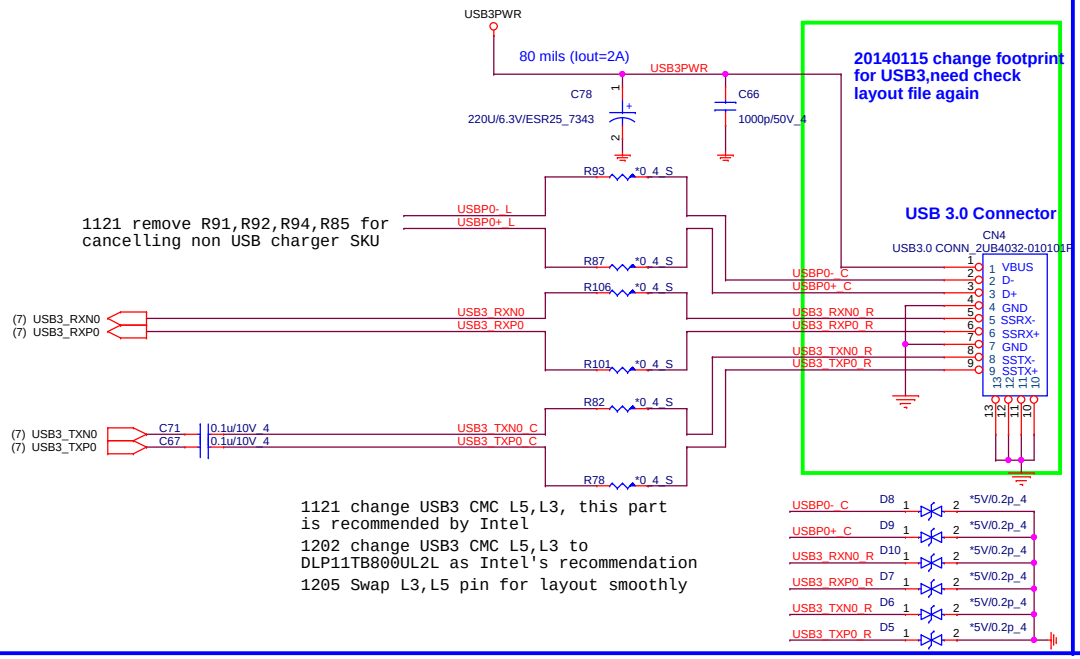
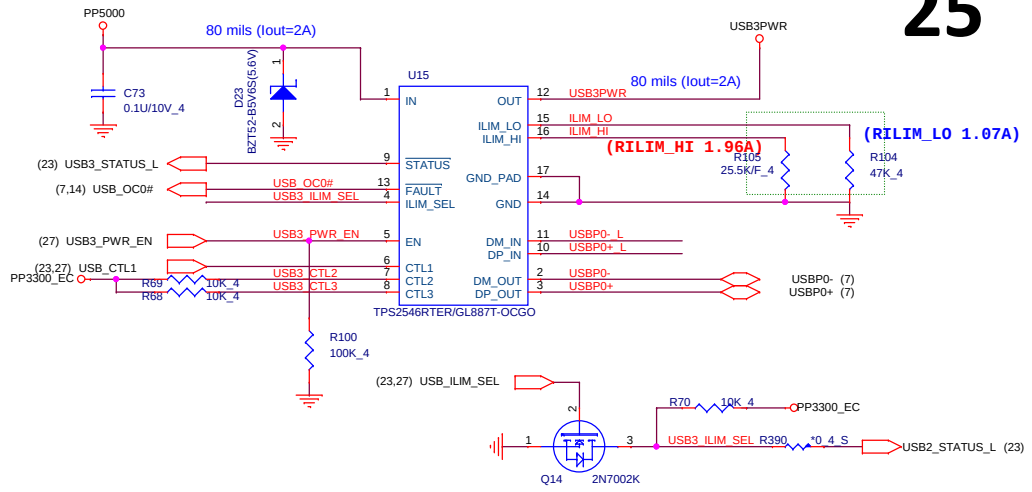
USB3.0(USB)



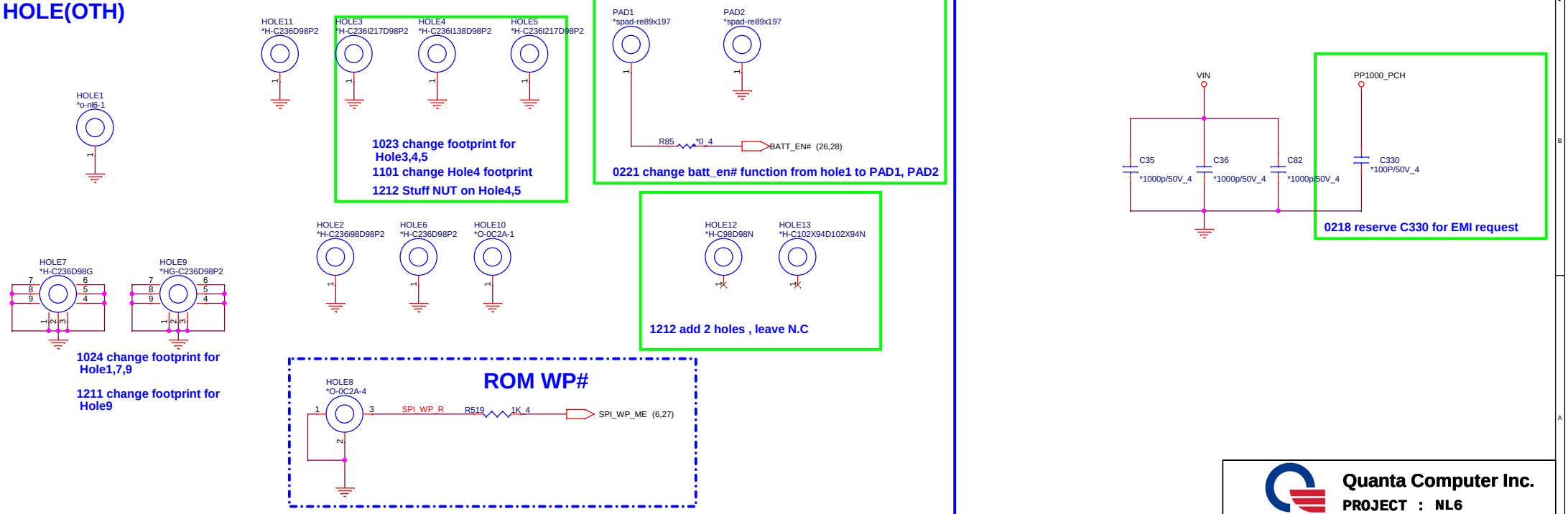
USB Charger



RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$IOS\_typ(mA) = 50{,}250/\{RILIM\_XX(K\Omega)+0.1\}$$

HOLE(OTH)



Quanta Computer Inc.		
PROJECT : NL6		
Size	Document Number: USB3/Charger/Hole	Rev: 1A
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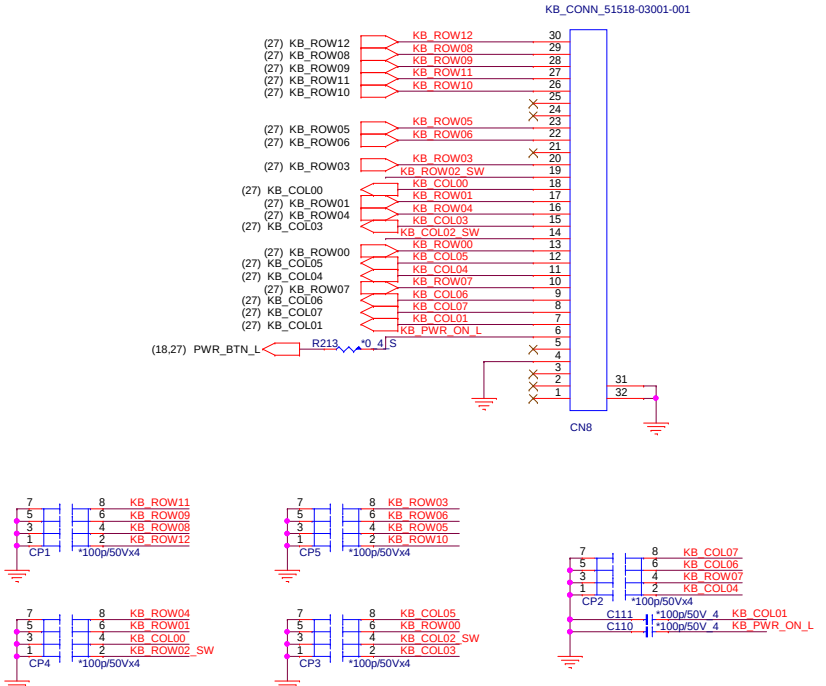
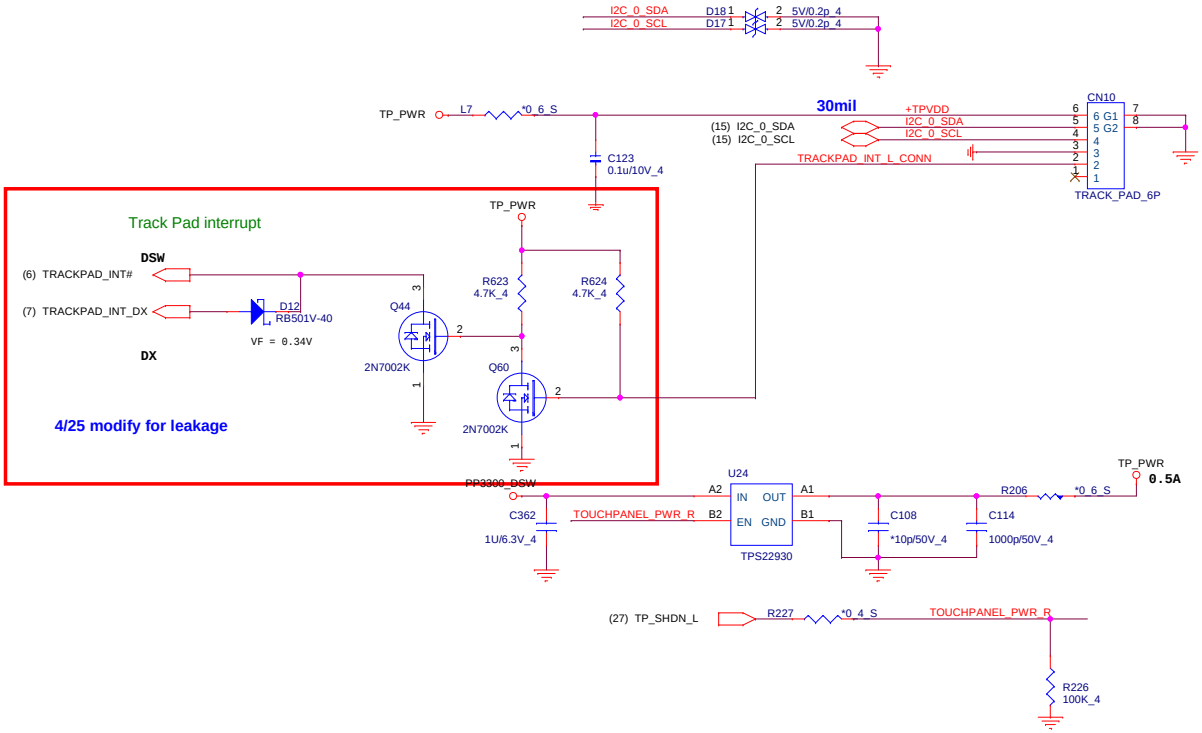
K/B (KBC)

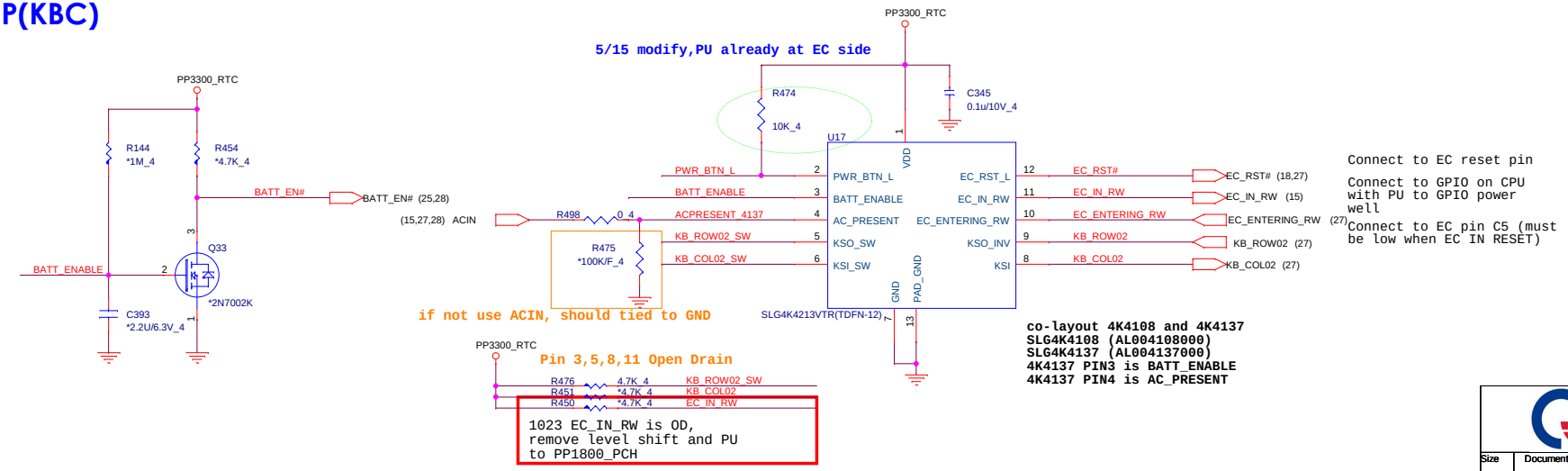
20140127 Change KB CONN for ME require



Track PAD BOARD CONN (TPD)



HOLELESS RESET 2-CHIP(KBC)



Quanta Computer Inc.

PROJECT : NL6

Size	Document Number	Rev
	KB/TP/FAN/HW Reset	1A

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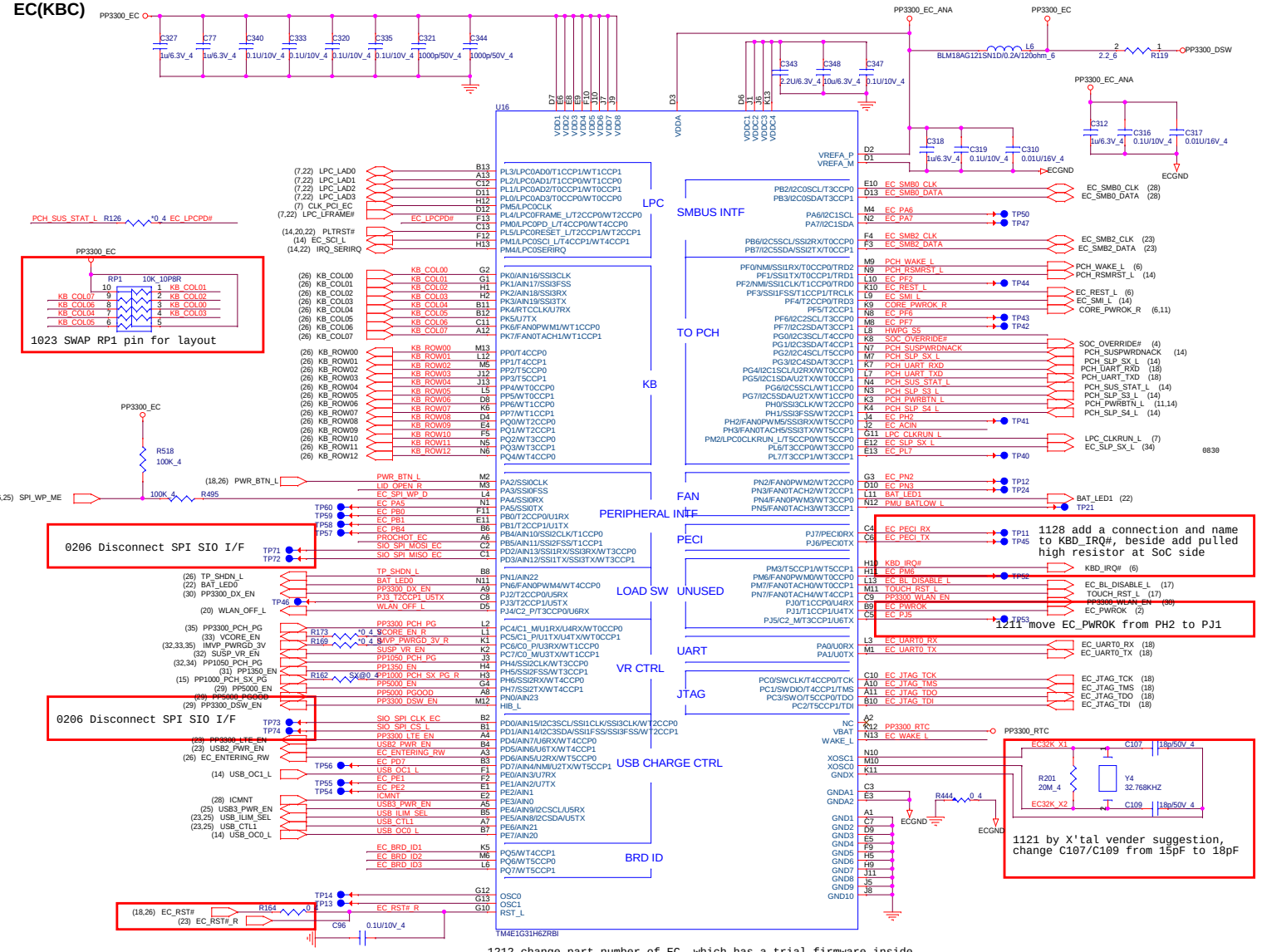
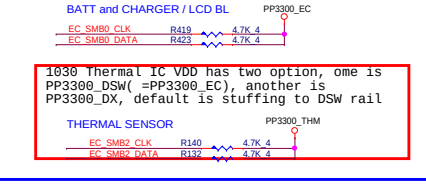
EC(KBC)



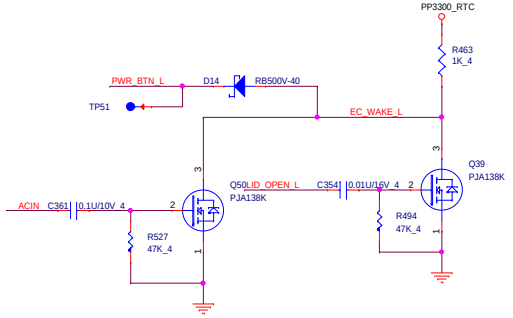
SM BUS ARRANGEMENT TABLE

SM Bus 0	BATT and CHARGER
SM Bus 1	NA
SM Bus 2	THERMAL SENSOR

SM BUS/I2C PU(KBC)



EC HIB WAKE SOURCES

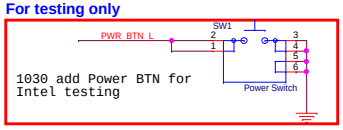


HWPG(KBC)

OD pin list

- EC_REST_L
- BAT_LED0
- BAT_LED1
- PCH_RSMRST_L
- SMBUS
- IRQ_SERIRQ
- EC_BL_DISABLE_L

For testing only



Stage	EC_ID3	EC_ID2	EC_ID1	
Proto1/1.5/2.0	0	0	0	
Proto2.0	0	0	1	

1213 Board ID of proto2 change to 001

Quanta Computer Inc.
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Size	Document Number	Rev
	KBC TI TM4E1G31H6ZRBI	1A
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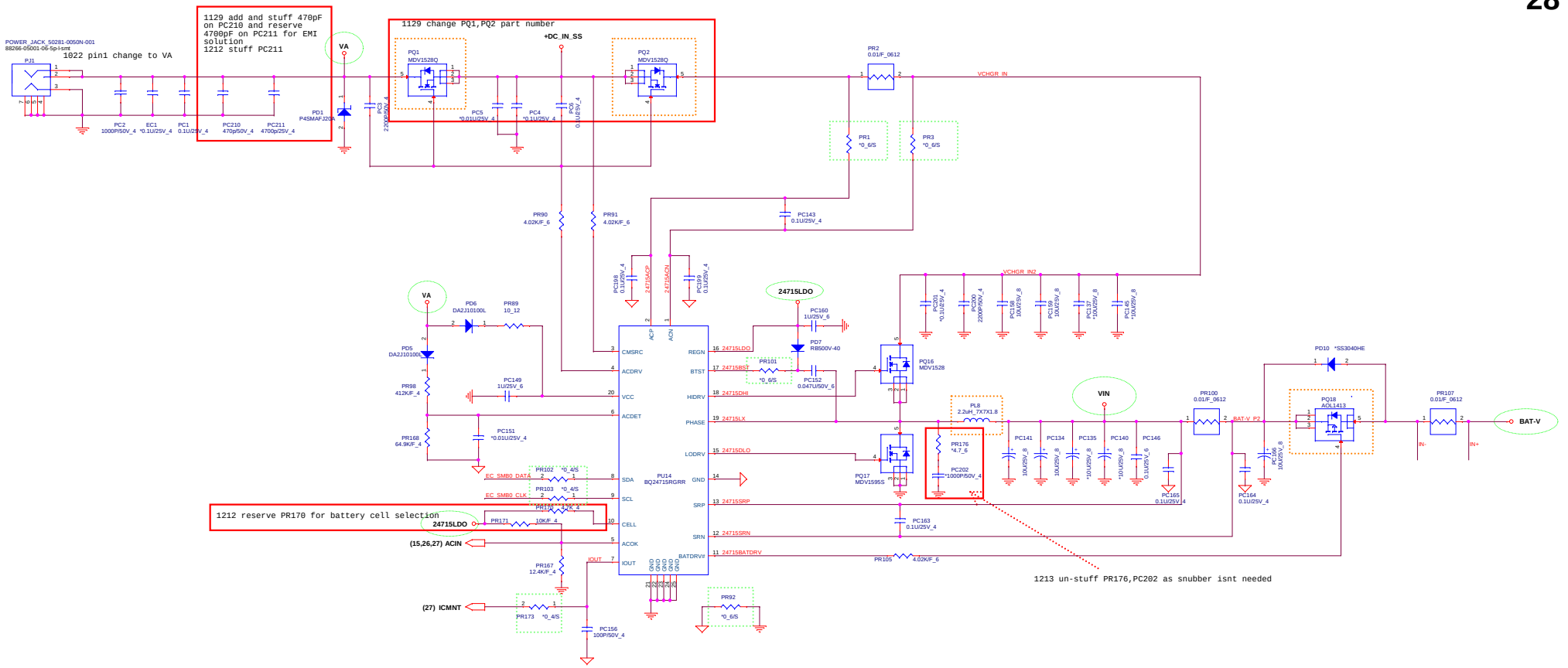
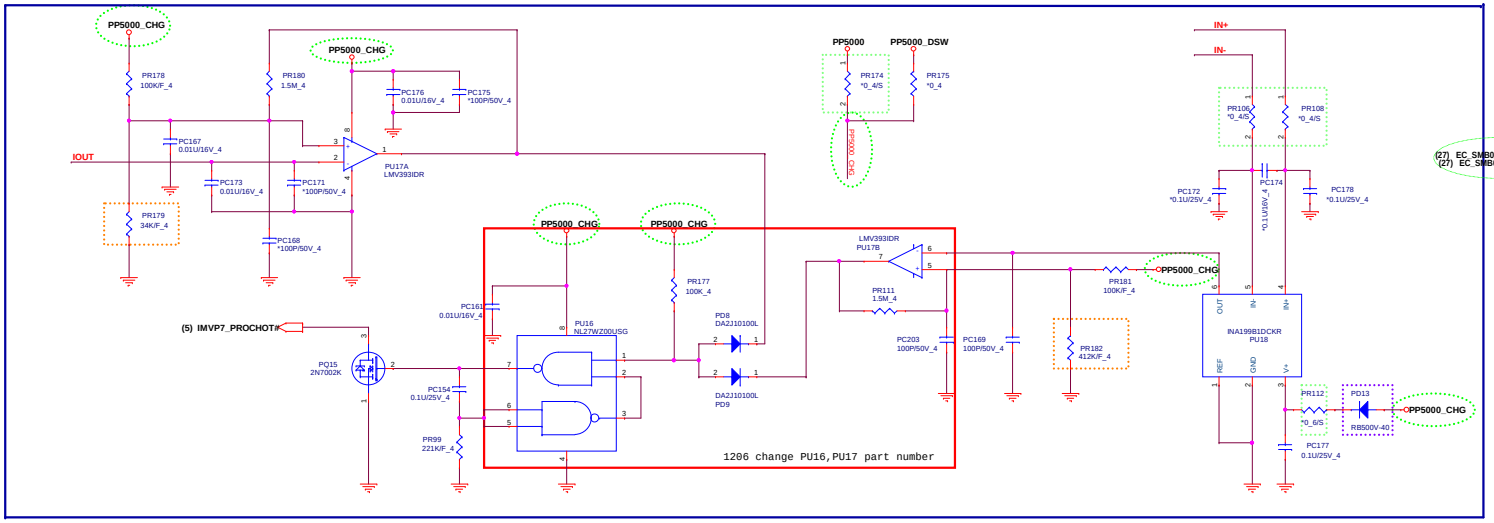


10ms one-shot circuit



Quanta Computer Inc.			
PROJECT :			
Size	Document Number		Rev
	Charger(BQ24715)		1A
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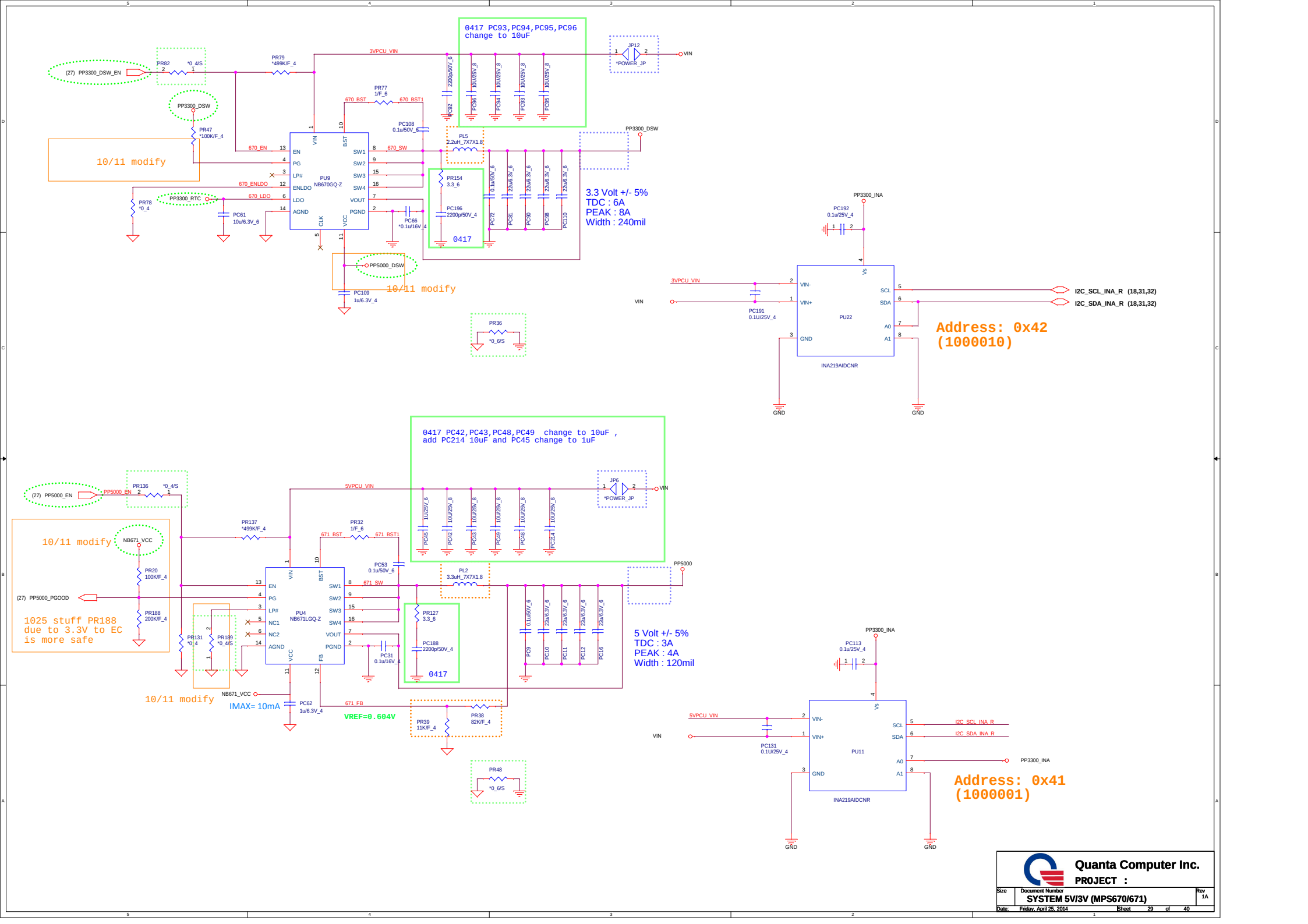
0417 PC93,PC94,PC95,PC96
change to 10uF
3VPCU_VIN
PR82
*0_4/S
(27) PP3300_DSW_EN
PR79
*499K/F_4
PR77
1/F_6
670_BST
670_BST1
PC108
0.1u/50V_6
PP3300_DSW
PR47
*100K/F_4
10/11 modify
670_EN
670_ENLDO
670_LDO
PP3300_RTC
PR78
*0_4
PC61
10u/6.3V_6
PU9
NB670GQ-Z
VIN
BST
EN
PG
LP#
ENLDO
LDO
AGND
CLK
VCC
SW1
SW2
SW3
SW4
VOUT
PGND
670_SW
PL5
2.2uH_7X7X1.8
PR154
3.3_6
PC196
2200p/50V_4
0417
PC66
*0.1u/16V_4
PP5000_DSW
PC109
1u/6.3V_4
10/11 modify
PR36
*0_6/S
JP12
*POWER_JP
VIN
2200p/50V_6
PC92
100/25V_8
PC96
PC94
PC93
PC95
0.1u/50V_6
22u/6.3V_6
PC72
PC81
PC90
PC98
PC110
3.3 Volt +/- 5%
TDC : 6A
PEAK : 8A
Width : 240mil
PP3300_INA
PC192
0.1u/25V_4
3VPCU_VIN
VIN
PC191
0.1U/25V_4
PU22
INA219AIDCNR
VIN-
VIN+
GND
Vs
SCL
SDA
A0
A1
I2C_SCL_INA_R (18,31,32)
I2C_SDA_INA_R (18,31,32)
Address: 0x42
(1000010)
0417 PC42,PC43,PC48,PC49 change to 10uF ,
add PC214 10uF and PC45 change to 1uF
(27) PP5000_EN
PP5000_EN
PR136
*0_4/S
5VPCU_VIN
JP6
*POWER_JP
VIN
1U/25V_6
PC45
PC42
PC43
PC49
PC48
PC214
10/11 modify
NB671_VCC
PR20
100K/F_4
(27) PP5000_PGOOD
PR188
200K/F_4
1025 stuff PR188
due to 3.3V to EC
is more safe
PR137
*499K/F_4
PR32
1/F_6
671_BST
671_BST1
PC53
0.1u/50V_6
PU4
NB671LGQ-Z
EN
PG
LP#
NC1
NC2
AGND
VCC
FB
SW1
SW2
SW3
SW4
VOUT
PGND
671_SW
PL2
3.3uH_7X7X1.8
PP5000
PR127
3.3_6
PC188
2200p/50V_4
0417
PC31
0.1u/16V_4
PR131
*0_4
PR189
*0_4/S
10/11 modify
NB671_VCC
PC62
1u/6.3V_4
IMAX= 10mA
671_FB
VREF=0.604V
PR39
11K/F_4
PR38
82K/F_4
PR48
*0_6/S
PC9
PC10
PC11
PC12
PC16
22u/6.3V_6
5 Volt +/- 5%
TDC : 3A
PEAK : 4A
Width : 120mil
PP3300_INA
PC113
0.1u/25V_4
5VPCU_VIN
VIN
PC131
0.1U/25V_4
PU11
INA219AIDCNR
VIN-
VIN+
GND
Vs
SCL
SDA
A0
A1
I2C_SCL_INA_R
I2C_SDA_INA_R
PP3300_INA
Address: 0x41
(1000001)
Quanta Computer Inc.
PROJECT :
Size
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SYSTEM 5V/3V (MPS670/671)
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1A
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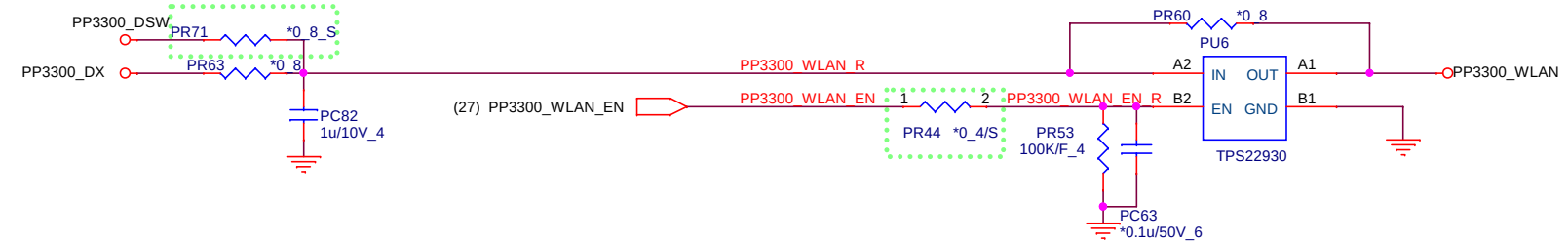
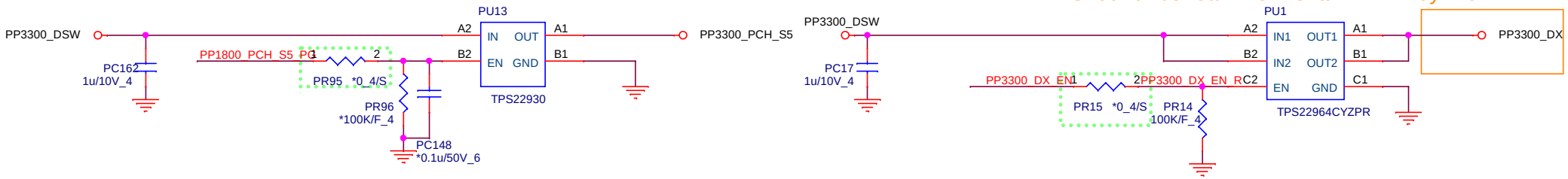
(35) PP1800_PCH_S5_PG
(27) PP3300_DX_EN

PP1800_PCH_S5_PG
PP3300_DX_EN



DX should be earlier than VREN by EC.



Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	Load Switch	1A
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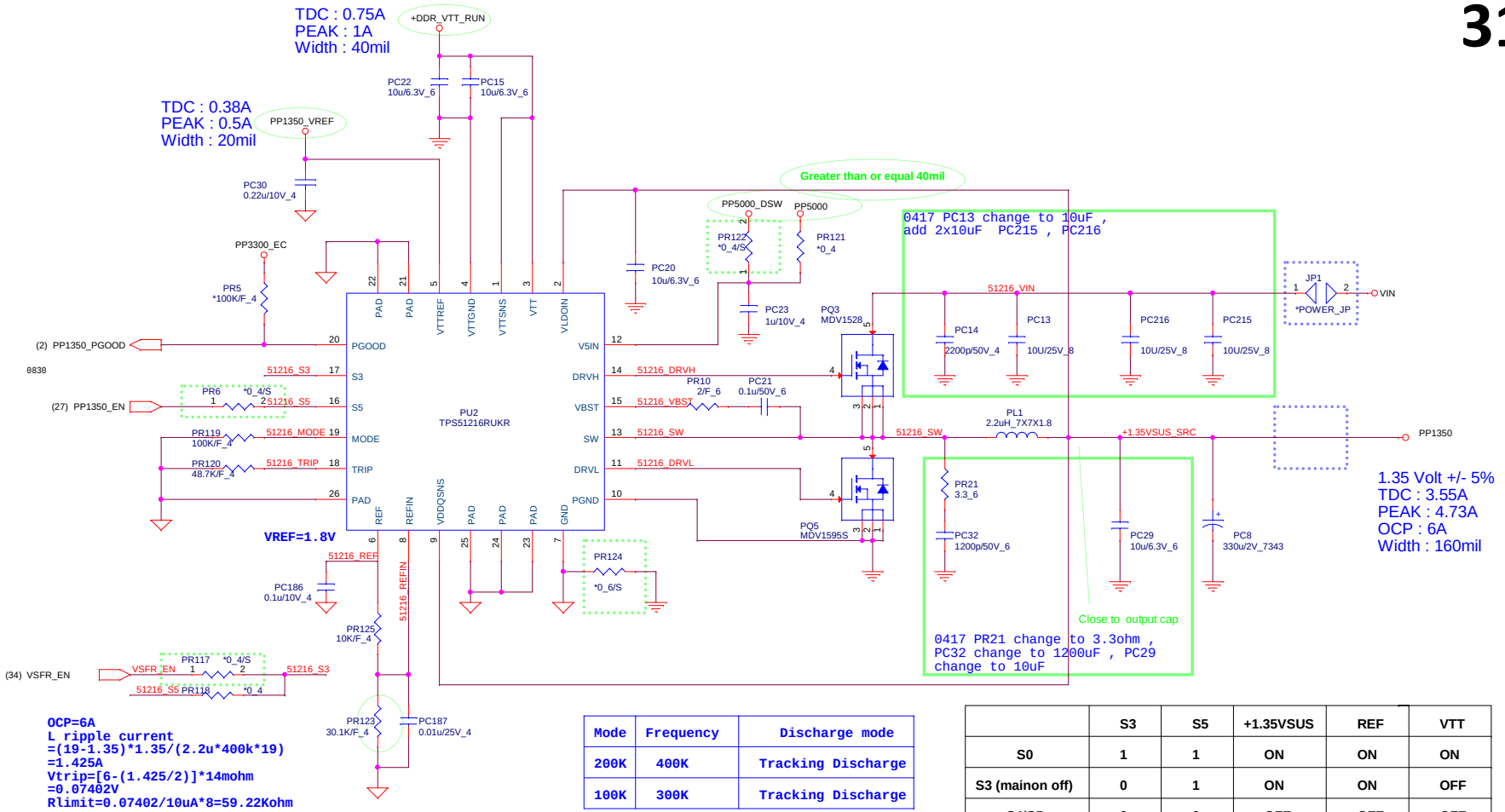
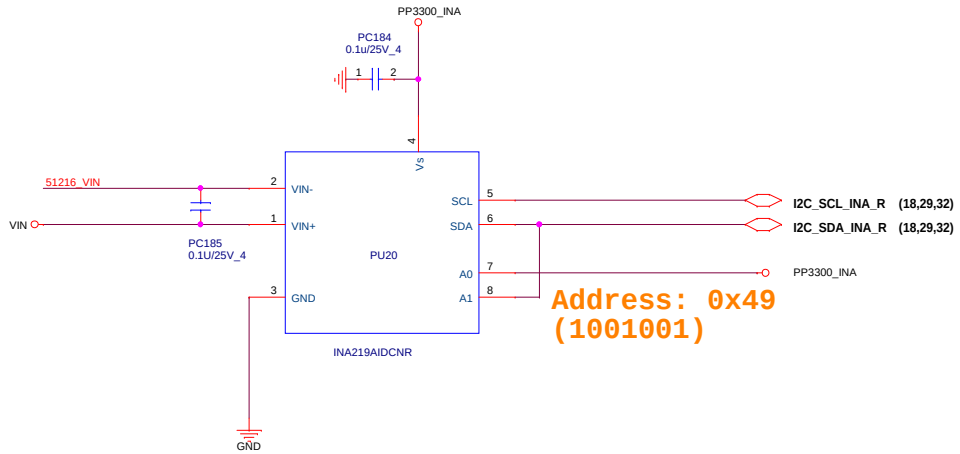


Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



Quanta Computer Inc.

PROJECT :

Size	Document Number	Rev
	DDR 1.35V(TPS51216)	1A

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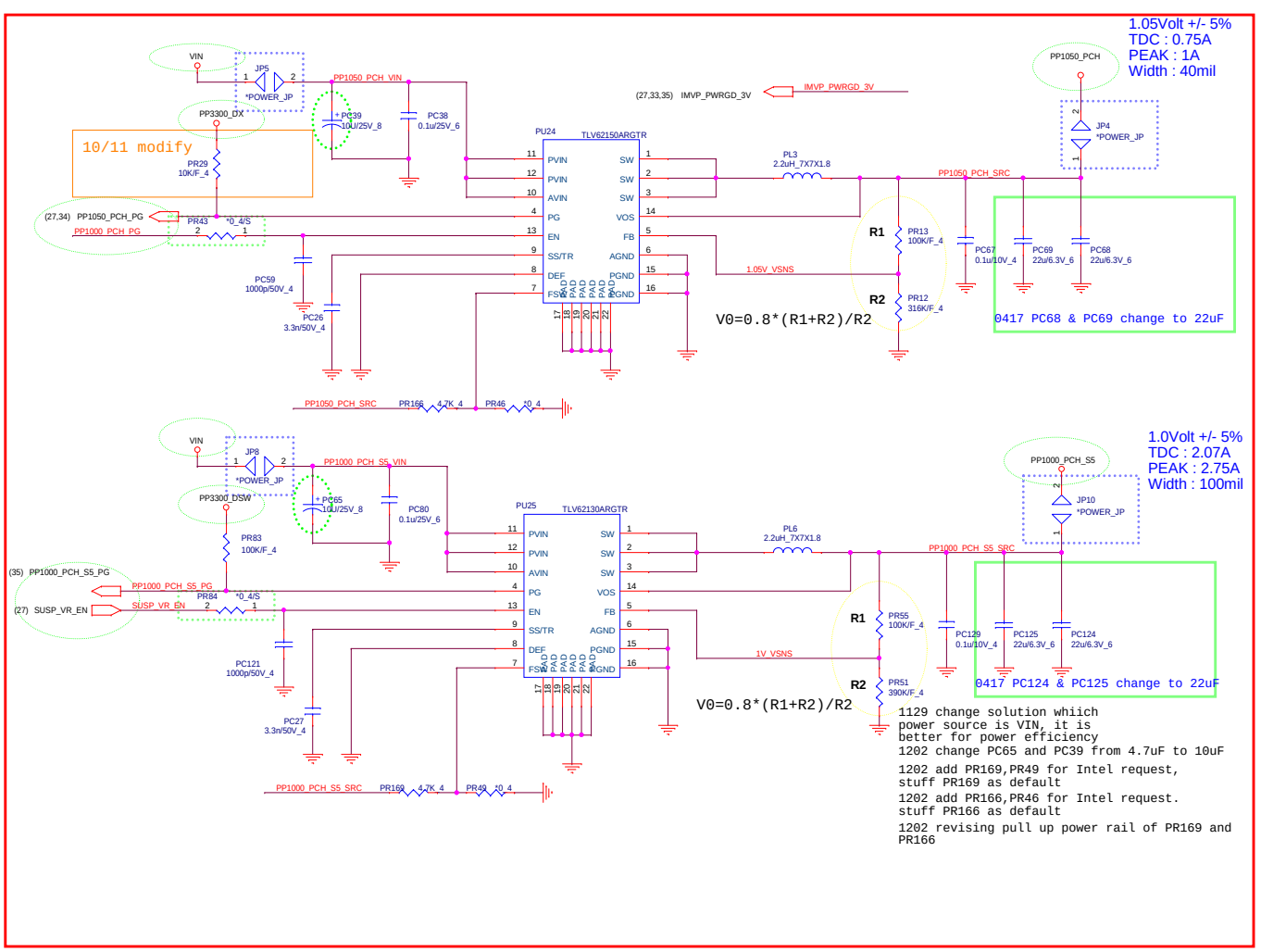
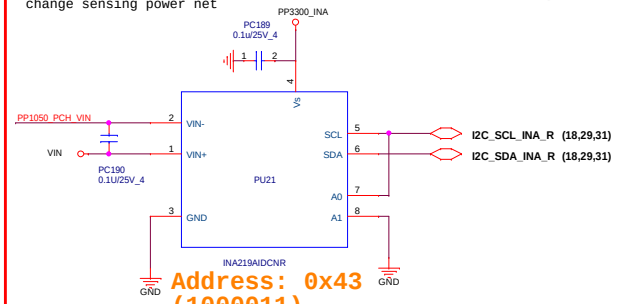
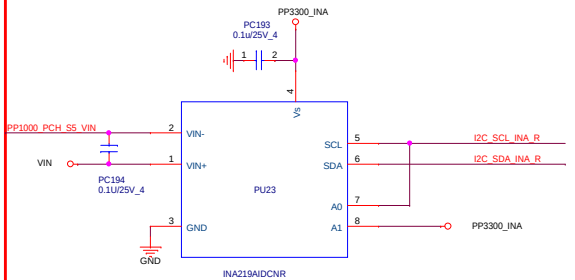
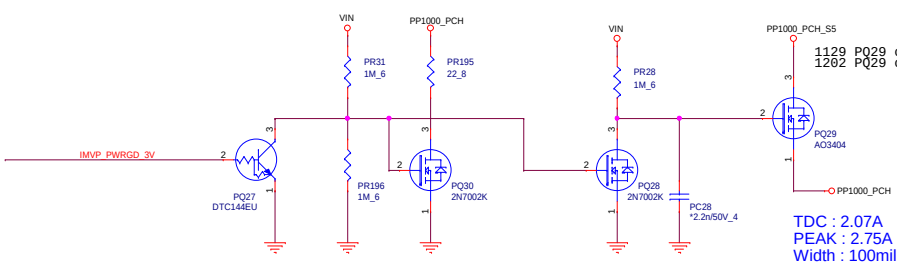


1129 because of power
source of PU24,PU25 chagen
to VIN, so that need
change sensing power net







1129 PP1000_PCH changes from convert to power MOSFET type for power efficiency improvement

Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	+1.05V/+1V(TPS54318)	1A
Date: Friday, April 25, 2014	Sheet 32 of 40	

1025 PC57 change from 68p to 120p
PC50 change from 150p to 2200p
for proto1 issue

1030 PR26 change to 16.9K
PR23 change 10 ohm
PC50 change 1200pF
PC40 change to 270pF
un-stuff PR22,PC54

1031 un-stuff PR129 and PC37

1115 PR128 change to 1.62K

20140321 Intel request change
PL4 & PL7 0.22uH to 0.47uH .
Change PR130 change to 124K ohm
& PR62 and PR30 change to 0 ohm
.

0417 PC87 & PC88 change to 10uF

AXG

1209 remove JP9 for ACLL improvement

+VCC_GFX
PEAK : 14A
OCP : 18A
Width : 600mil

GFX_CORE Load Line : -5.9mV/A for SDP=4.5W

1213 un-stuff PR74,PC104 as snubber isnt needed

Close to the VR side.

Close with AXG inductor

Parallel

Close to the CPU side.

VRON PD 100K AT EC

PU7
ISL95833HRTZ-T

0417 PC119 & PC126 change to 10uF

Core

1209 remove JP13 for ACLL improvement

+VCC_CORE
PEAK : 12A
OCP : 18A
Width : 500mil

VCORE Load Line : -5.9mV/A for SDP=4.5W

1213 un-stuff PR81,PC115 as snubber isnt needed

Close to the VR side.

1031 add 0.1u on PP1000_PCH for power request

1025 PR155 change from 300 to 340 ohm for proto1 issue

1025 PC99 change from 68p to 120p
PC106 change from 150p to 2200p
for proto1 issue

1030 PR76 change to 16.9K
PR86 change 10 ohm
PC106 change 1200pF
PC114 change to 270pF
un-stuff PR80,PC101

1031 un-stuff PR158 and PC118

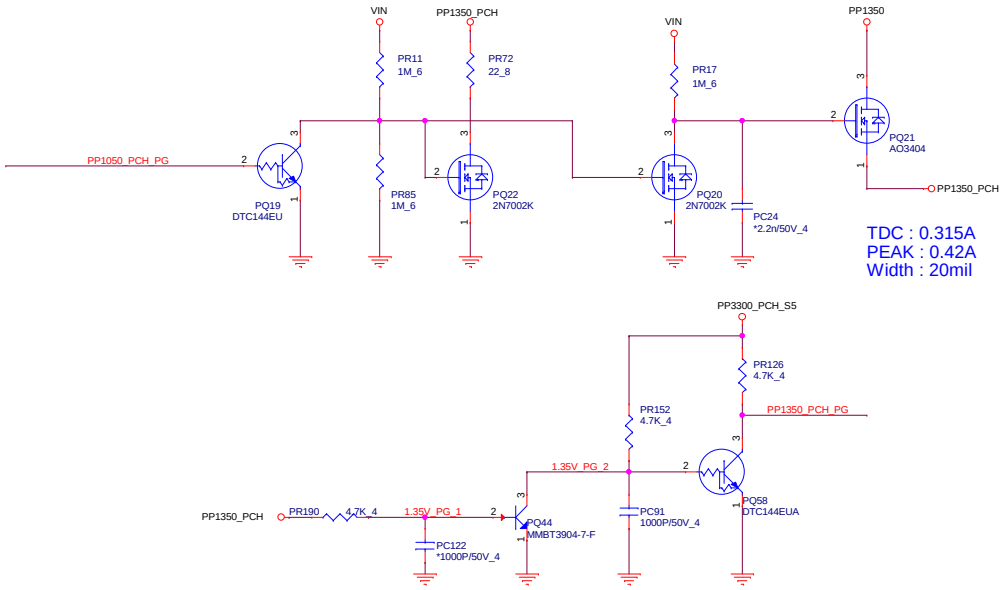
Parallel

Close to the CPU side.

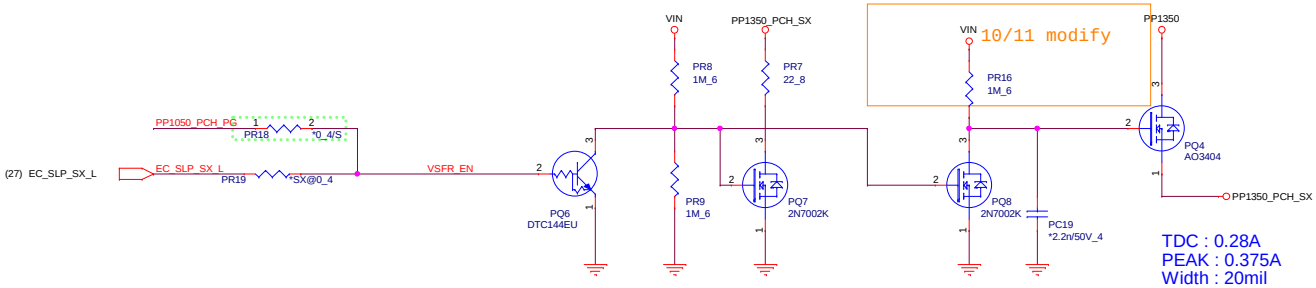
Quanta Computer Inc.
PROJECT :

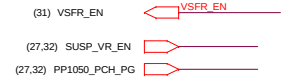
Size	Document Number	Rev
	+VCC_CORE(ISL95833)	1A
Date: Friday, April 25, 2014	Sheet 33 of 40	

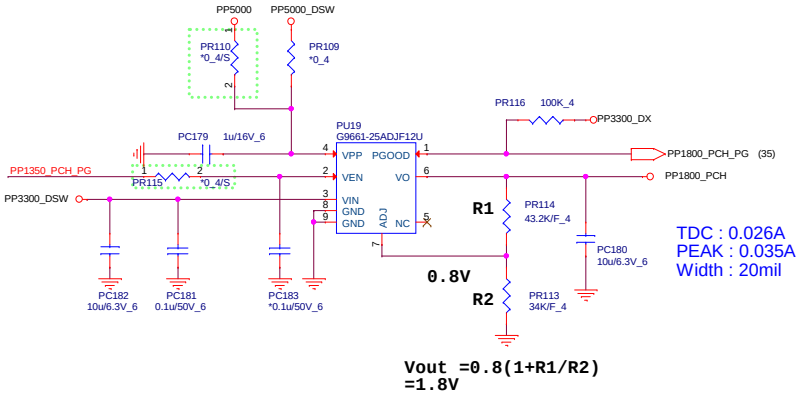
1129 PP1000_PCH_S5 change from LDO to switching power



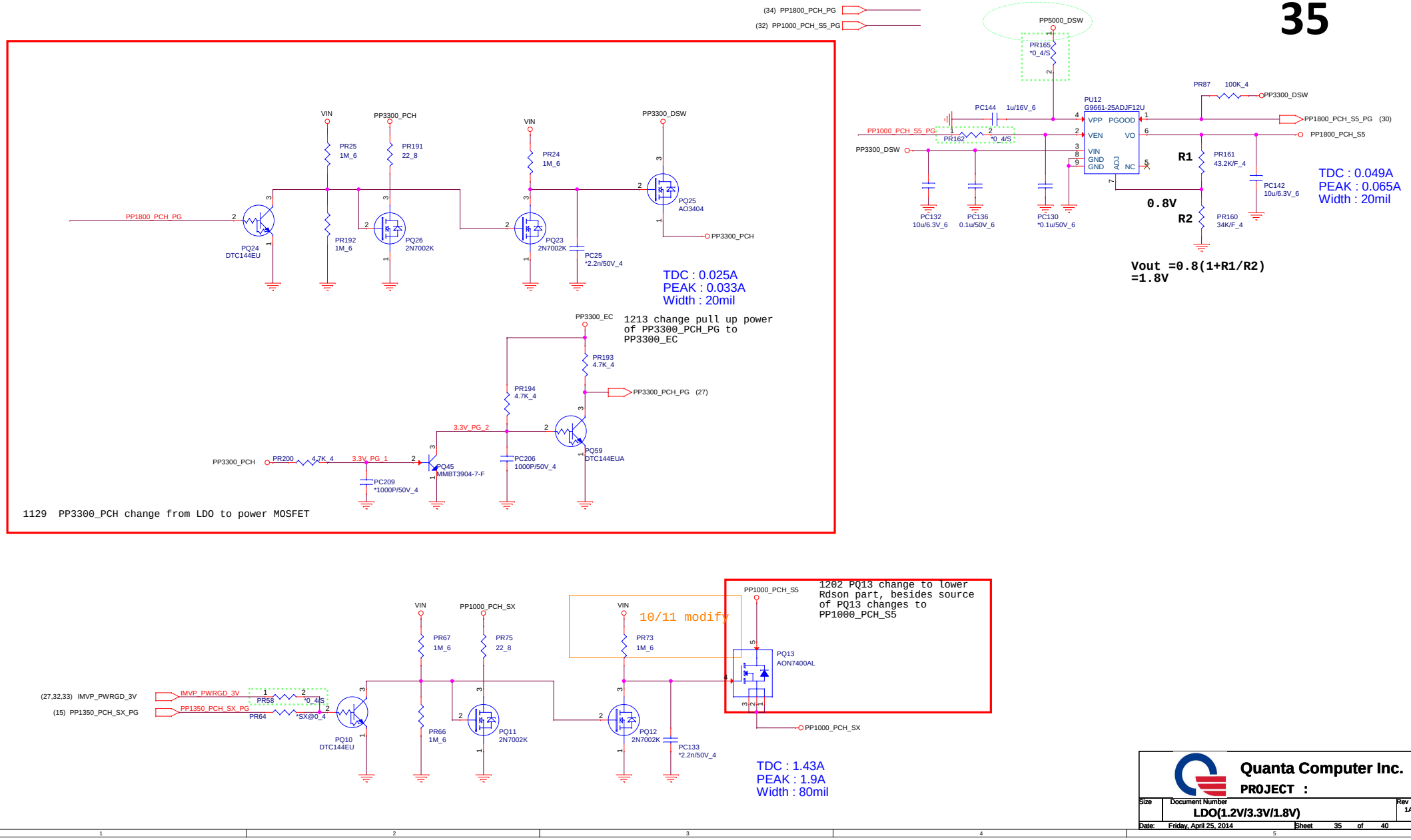
1129 PP1350_PCH change from LDO to power MOSFET







Quanta Computer Inc.		
PROJECT :		
Size	Document Number: LDO (1V/1.35V/1.5V/1.8V)	Rev: 1A
Date: Friday, April 25, 2014	Sheet 34 of 40	



Quanta Computer Inc.

PROJECT :

Size	Document Number	Rev
	LDO(1.2V/3.3V/1.8V)	1A

Date: Friday, April 25, 2014 Sheet 35 of 40

Quanta Computer Inc.			
PROJECT :			
Size	Document Number: Thermal protect		Rev: 1A
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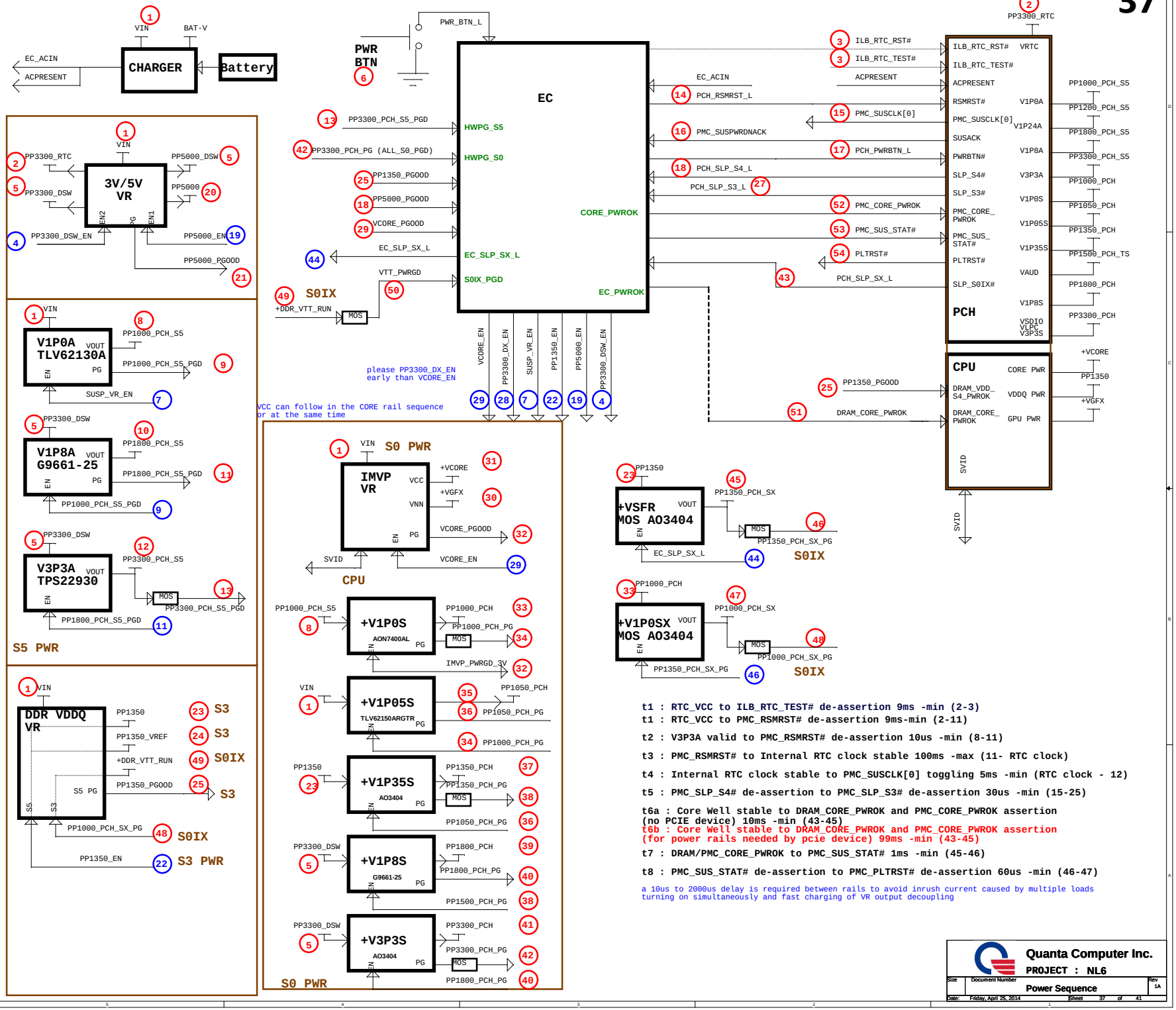
Support S0iX



t1 : RTC_VCC to ILB_RTC_TEST# de-assertion 9ms -min (2-3)
t1 : RTC_VCC to PMC_RSMRST# de-assertion 9ms-min (2-11)

t2 : V3P3A valid to PMC_RSMRST# de-assertion 10us -min (8-11)

t3 : PMC_RSMRST# to Internal RTC clock stable 100ms -max (11- RTC clock)

t4 : Internal RTC clock stable to PMC_SUSCLK[0] toggling 5ms -min (RTC clock - 12)

t5 : PMC_SLP_S4# de-assertion to PMC_SLP_S3# de-assertion 30us -min (15-25)

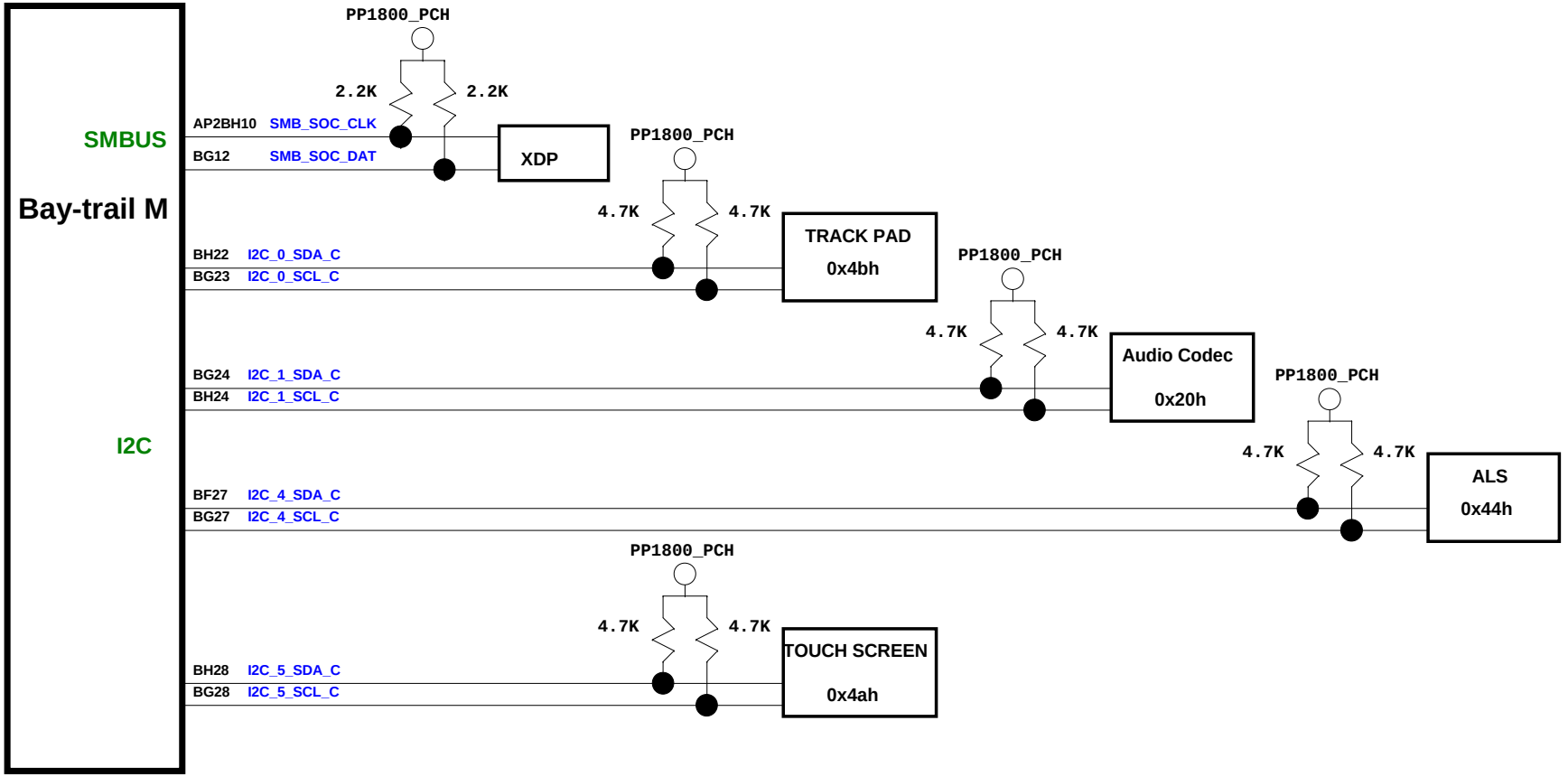
t6a : Core Well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion (no PCIE device) 10ms -min (43-45)
t6b : Core Well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion (for power rails needed by pcie device) 99ms -min (43-45)

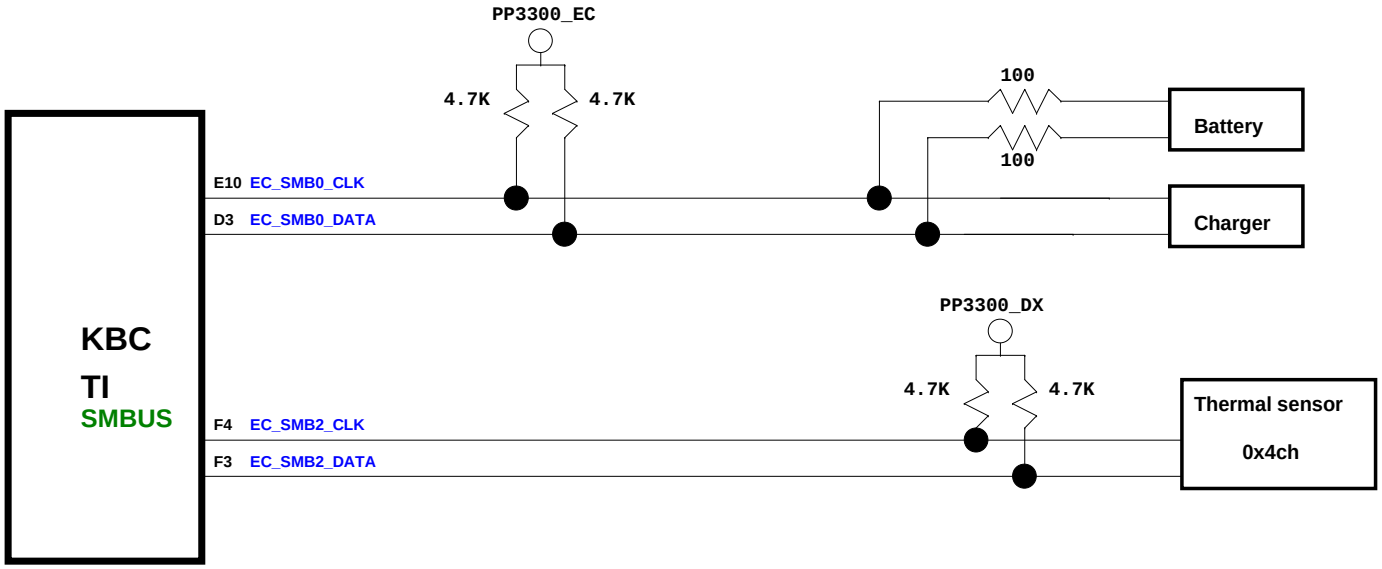
t7 : DRAM/PMC_CORE_PWROK to PMC_SUS_STAT# 1ms -min (45-46)

t8 : PMC_SUS_STAT# de-assertion to PMC_PLTRST# de-assertion 60us -min (46-47)

a 10us to 2000us delay is required between rails to avoid inrush current caused by multiple loads turning on simultaneously and fast charging of VR output decoupling

Quanta Computer Inc.	
PROJECT : NL6	
Size	Document Number: Power Sequence
Rev	1A
Date: Friday, April 25, 2014	Sheet 37 of 41

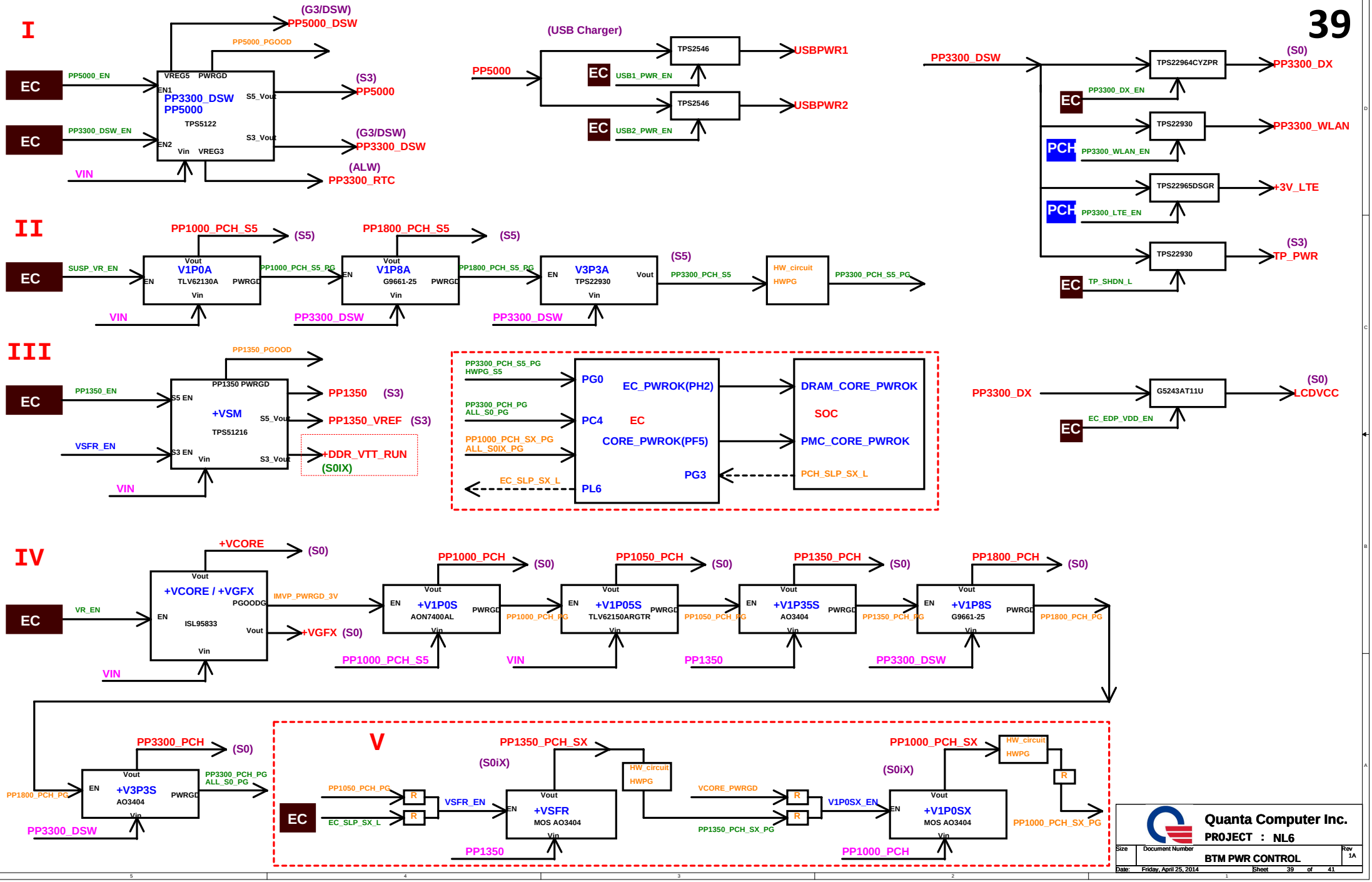




Quanta Computer Inc.
PROJECT : NL6

Size	Document Number	Rev
	SMBUS_I2C	1A

Date: Friday, April 25, 2014 Sheet 38 of 41



Quanta Computer Inc.
PROJECT : NL6

Size	Document Number	Rev
	BTM PWR CONTROL	1A

Date: Friday, April 25, 2014 Sheet 39 of 41

CHANGE LIST

Model: 0CX | Version: 1A

10/11
B01 Change PU9 VCC, CLK, PG (Page 29)
B02 Change PU4 VCC, PG (Page 29)
B03 Change PR29 from 100K/F_4 to 10K/F_4 (Page 32)
B04 Remove 15V, PR17. Mount PR16 (Page 34)
B05 Remove 15V, PR72. Mount PR73 (Page 35)
10/14
B06 Change U11 LVDS power switch footprint to sot23-5 (Page 17)
B07 Unstuff PR188 due to PP5000_PGOOD (PN0) is 5V tolerant input pin (Page 29)
10/16
B08 Change PJ1 from DFPJ06MR007 to DFHD05MR080 (Page 28)

10/17
B09 Change C126 from *10U/6.3V_8 to *10U/6.3V_6 due to height limit (Page 24)
B10 Change USB3.0 ESD D8,D9 route (Page 24)
B11 Change R384 from 0_4 to 0_8, remove R376,R377. Merge UNCORE_V1P35_S0IX_A, UNCORE_V1P35_S0IX_B & UNCORE_V1P35_S0IX (Page 9)
B12 Change R354 from 0_4 to 0_8, remove R357. Merge CORE_V1P05_S3_PW, & CORE_V1P05. They are of the same power state and rail (Page 9)

10/18
B13 Correct BIOS Strap, mount R128 and dismount R434 (Page 4)
B14 Add R553 0_4, connect U12 pin 6 ALERT# to H_PROCHOT# (Page 5, 23)
B15 Change Y2 from BG332768224 to BG332768111 due to height limit, change C91,C92 from 18pf to 15pf (Page 6)
B16 Add R554,R555 0_6 option S0 & S5 for PCU_V1P8_G3_V25 (Page 9)
B17 Change R469, EC_RST#_Q pull up from PP3300_DX to PP3300_DSW (Page 23)
B18 Swap L4 vertically (Page 25)
B19 Power modified:
Change PD1 from BCMAJ22AZ00 to BCAFJ20AZ00 (Page 28)
10/21
B20 un-stuff R553 (Page 5)
B21 change SEL debugf footprint and PN(Page 18)
B22 change footprint and PN for HDMI (Page 19)
B23 change footprint and PN for USB3(Page 25)
B24 change footprint for Hole3,4,5,7 and add hole11(Page 25)

10/22
B25 un-stuff R182 for S5 leakage issue (Page 14)
B26 change thermal IC (Page 23)
B27 PJ1 pin1 change to VA (Page 28)

10/23
B28 unstuff R28 by Intel reques (Page 2)
B29 unstuff R29 by Intel reques (Page 3)
B30 RAM ID strap pin resistor change to 1K, would be stronger (Page 7)
B31 change cap C230 from 0.2pF to 3.3pF (Page 12)
B32 change cap C228 from 0.2pF to 3.3pF (Page 13)
B33 EC_IN_RW is OD,remove level shift and PU to PP1800_PCH (Page 15,26)
B34 change NGFF E key footprint and PN (Page 20)
B35 change footprint for Hole3,4,5 and add 2 PAD for BATT_EN reserve (Page 25)
B36 SWAP L4 pin for layout (Page 25)
B37 SWAP RP1 pin for layout (Page 27)

10/24

B38 change M_A_ODT0 PU to VTTby Intel request (Page 12)
B39 change M_B_ODT0 PU to VTTby Intel request (Page 13)
B40 correct schematic for R469 PU power rail (Page 23)
B41 SWAP L4 pin again for layout (Page 25)
B42 change footprint for Hole1,7,9 (Page 25)
10/25
B43 Delete complete SSD(connector and caps), unstuff R215 and add test points on SATA signals (Page 5,15,21)
B44 1025 add LTE SUSCLK feature (Page 6,15,23)
B45 the damping of SDIO change to 0 ohm by Intel request Page 16)
B46 add PU for SDIO WP by Intel request (Page 16)
B47 remove Q31 becasue PU to PP3300_DSW at EC side already (Page 23)
B48 change headphone CN6 footprint and PN (Page 24)
B49 stuff PR188 due to 3.3V to EC is more safe(Page 29)
B50 PR135 change from 300 to 348 ohm for proto1 issue (Page 33)
B51 PR155 change from 300 to 340 ohm for proto1 issue (Page 33)
B52 PC57 change from 68p to 120p PC50 change from 150p to 2200p for proto1 issue (Page 33)
B53 PC99 change from 68p to 120p PC106 change from 150p to 2200p for proto1 issue (Page 33)
10/29
B54 unstuff R128,R372,R386,R364 using SoC internal PU (Page 4,5)
B55 eDP power change to PIC fuse (Page 17)
B56 change R358 to 0 ohm by intel request(Page 21)
B57 remove pulled up resistors for eMMC data and cmd (Page 21)
10/30
B58 change C60 power netname for layout (Page 8)
B59 U10 change to 74AUP1G34 and stuff it (Page 11)
B60 remove PREQ# pulled up resistor R323(Page 11)
B61 stuff Q47,R531,R530 and un-stuff R533,R542 for Track Pad I2C (Page 15)
B62 HDMI DDC pulled up to HDMI_5V by intel request (Page 19)
B63 add Power LED for Intel testing (Page 22)
B64 Thermal IC VDD has two option, ome is PP3300_DSW(=PP3300_EC), another is PP3300_DX, default is stuffing to DSW rail(Page 23,27)
B65 add Power BTN for Intel testing(Page 27)
B66 for Gfx power, change C266,C289,C290 to 10uF and add 2 caps 10uF (Page 8)
B67 for core power, change C271,C281,C280,C278,C273 to 10uF(Page 8)
B68 for VR compensation, PR26 change to 16.9K,PR23 change 10 ohm,PC50 change 1200pF,PC40 change to 270pF,un-stuff PR22,PC54(Page 33)
B69 for VR compensation, PR76 change to 16.9K,PR86 change 10 ohm,PC106 change 1200pF,PC114 change to 270pF,un-stuff PR80,PC101(Page 33)
10/31
B70 remove TP44 and TP35 for GND vias adding (Page 8)
B71 remove C285(Page 9)
B72 N.C U10 pin1(Page 11)
B73 un-stuff PR129,PC37,PR158,PC118(Page 33)
B74 stuff R273,R286,R289,R323 for Intel request(Page 11)
B75 for layout suggestion by intel, VSS_AXG_SENSE didn't connect to VSS_SENSE, will connect the GND via near VCC_AXG_SENSE(Page 8)
B76 add 0.1u on PP1000_PCH for power request(Page 33)
B77 remove R417, PRDY should be direct connection between SoC and XDP by intel request (Page 6)
B78 for layout, add 0hm between GND and VSS_AXG_SENSE (Page 8)
11/1
B79 add option BOM R446,R449 for EC CLK for power saving by Intel request (Page 7)
B80 stuff C16(Page 11)
B81 correct C351 footprint(Page 16)
B82 change Hole4 footprint (Page 25)
11/4
B83 Change PR135 from 348/F_4 to 340/F_4 (Page 33)
11/11
C01 Remove CH@ USB charge option,eMMC@ eMMC option (Page 25)
C02 Add CHB@ option for single channel SKU (Page 13)
11/15
C03 stuff R372, system can't boot if un-stuff R372 on proto1.5 board, need intel double confirm before proto2 (Page 4)
C04 stuff R386, it is required for eDP (Page4)
C05 U18 footprint change to 5 pin which is same as eDP power switch (Page 16)
C06 correct U11 orcad symbol, pin5 needs connect to power input (Page 17)
C07 remove R60 and change R74 to Short PAD and size to 0402 (Page 19)
C08 change R72/R73/R22 to short PAD(Page 19)
C09 PR128 change to 1.62K (Page 33)
C10 Revising block diagram (Page 1)
11/18
C11 add TP on pin38/73 for NFC function (Page 20)
11/21
C12 remove R28,R25,C35 (Page2)
C13 remove R29,R26,C36 (Page 3)
C14 by X'tal vender suggestion,change C105/C106 from 15pF to 12pF (Page 6)
C15 remove R22/R72/R73 (Page 19)
C16 remove R365(Page 21)
C17 remove R91,R92,R94,R85 for cancelling non USB charger SKU (Page 25)
C18 change USB3 CMC L5,L3, this part is recommended by Intel (Page 25)
C19 by X'tal vender suggestion, change C107/C109 from 15pF to 18pF (Page 27)
11/28
C20 add a connection and name to KBD_IRQ#, besides add pulled high resistor (Page6)
C21 remove R29,R26,C36 (Page 3)
C22 by X'tal vender suggestion,change C105/C106 from 15pF to 12pF (Page 6)
C23 remove R166, because SERIQR of TPM needs 3V (Page 14)
C24 reserve 0 ohm R387/R391 on VCCA and VCCB for debugging(Page 14)
C25 change HDMI CMC L2, this part is recommended by Intel (Page 19)
C26 remove HDMI EMI solution R30,R32,R40,R57 (Page 19)
C27 remove R358 by intel requst and has confirmed with EMI (Page 21)
C28 add pullup 10K on SERIRQ_R to TPM_VDD (Page 22)
11/29
C29 change PQ1,PQ2 part number (Page28)
C30 add and stuff 470pF on PC7 and reserve 4700pF on PC18 for EMI solution (Page 28)
C31 because of power source of PU24,PU25 change to VIN, so that need change sensing power net (Page 32)
C32 PQ29 change MOSFET with lower Rdson(Page 32)
C33 change solutions of PP1050_PCH and P1000_PCH_S5 ,which power sources are VIN, it is better for power efficiency (Page 32)
C34 PP1000_PCH changes from convert to power MOSFET type for power efficiency improvement(Page 32)
C35 PP1350_PCH change from LDO to power MOSFET (Page 34)
C36 PP3300_PCH change from LDO to power MOSFET(Page 35)
C37 Revising block diagram,power sequence, and power tree for power changes by Intel suggestion(Page 1,37,39)
12/02
C38 add C285 for U18 input inrush current (Page16)
C39 PJ2 changes footprint for layout (Page 28)
C40 change PC65 and PC39 from 4.7uF to 10uF (Page 32)
C41 add PR169,PR49 for Intel request,stuff PR169 as default(Page 32)
C42 add PR166,PR46 for Intel request,stuff PR166 as default(Page 32)
C43 PQ29 change back AO3404(Page 32)
C44 PQ13 change to lower Rdson part, besides source of PQ13 changes to PP1000_PCH_S5 (Page 32)
C45 revising pull up power rail of PR169 and PR166(Page 32)
C46 change L2,(HDMI CMC),L3,L5(USB3)to DLP11TB800UL2L as Intel's recommendation (Page 19,25)
12/04
C47 for z-height issue, change C72,C75,C81 to 0.85mm cap (Page8)
C48 reserve 3x1000pF cap for EMI(Page 25)
C49 change Hole1 to be battery enable function (Page 25)
C50 for z-height issue changePC48,PC49 to 0.85mm cap(Page 29)
C51 del PAD1 and PAD2(Page 25)
12/05
C52 add 0.1uFx2 on PP1350 for EMI request (Page12)
C53 To prevent the backlight flash, add a pull down on SoC_EDP_BLON_C and using double inverting OD FETs structure(Page 15)
C54 R551 changes to 1K to isolate SD socket and servo/SoC (Page 16)
C55 SD3_WP is 1.8V power rail in SoC,change external Pulled up power well of SD3_WP to 1.8V power(Page 16)
C56 L2 change back to DLP11SA900HL2(Page 19)
C57 Swap L3,L5 pin for layout smoothly(Page 25)
12/06
C58 change PU16,PU17 part number(Page 28)
C59 change C271,C273,C280,C266,C311,C315 to 0603 22uF for ACLL issue(Page 8)
12/09
C60 reserve R220connection from RCVP to MIC_DET as back up in case driver needs to be through codec using JACKSNS pinr(Page 24)
C61 remove JP9,JP13 for ACLL improvement(Page 33)
12/11
C62 add pulled up resistors on SDIO data/cmd lines (Page16)
C63 add back pulled up resistors for eMMC I/F(Page 21)
C64 co-layout ST and Infineon TPM, if change to ST,R56,R57,R60,R72,R38, ST PN is ST33ZP24AR28PVSM(Page 22)
C65 change footprint for Hole9(Page 25)
C66 move EC_PWROK from PH2 to PJ1(Page 27)
C67 add Test points on unused pins, need check layout to see if all points are ok(Page 27)
12/12
C68 add new RAMID 101 for single channel SKU (Page7)
C69 all Pulled up resistors of SDIO data/cmd to be un-stuffed(Page 16)
C70 all Pulled up resistors of eMMC data/cmd to be un-stuffed,and R361 change to 47K ohm as well(Page 21)
C71 add 2 holes , leave N.C(Page 25)
C72 Stuff NUT on Hole4,5(Page 25)
C73 change part number of EC ,which has a trial firmware inside(Page 27)
C74 reserve PR170 for battery cell selection(Page 28)
C75 stuff PC211(Page 28)
12/13
C76 swap CLKREQ_WLAN and CLKREQ_IMAGE for CLKREQ and CLK pins are aligned (Page5)
C77 change pull up power of PP3300_PCH_PG to PP3300_EC (Page 35)
C78 Board ID of proto2 change to 001 (Page27)
C79 un-stuff PR176,PC202 as snubber isnt needed (Page 28)
C80 un-stuff PR74,PC104,PR81,PC115 as snubber isnt needed (Page33)
01/15
C81 change CN15 USB3.0 connector type
C82 change CN6 Audio Jack connector type
C83 change CN2 HDMI connector type
01/27
C84 change CN8 Keyboard connector type
02/10
C85 unstuff U20, R156, R387, R391, R353 for SERIRQ leakage issue (Page14,22)

DOC NO.	PROJECT MODEL :	Chrome	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISON:	

CHANGE LIST

Model	Version	
NL6	PVT1	2/20 1. un-stuff R156 for SERIRQ skipped (Page14) 2. change power rail of Q35,Q36,Q37,Q44 from PP1800_PCH_S5 to PP1800_PCH for PP1800_PCH leakage issue in S3 mode (Page14) 3. unstuff R337 for S3 leakage issue(Page 11) 4. Delete LED2, R127 (Page 22,27) 5. Change LED1 type to right angle , same as 0C7 (Page22) 6. unstuff R454,Q33,Q144 for auto power on issue when insert battery first time(Page 26) 7. change PR130 to 124K ohm for efficiency improvement (Page 33) 8. change PL7/PL4 to 0.47uH and PR30/PR62 to 0ohm for efficiency improvement (Page 28) 9. unstuff NUT of Hole4,Hole5(Page 25)
	PVT2	3/19 1. Disconnect SPI SIO I/F (Page6, 27) 2. Delete SPI_SIO Interface,Q35,Q36,Q37,Q44,R486,R484,R485,R483,R426,R429,R427,R428 (Page14) 3. reserve C377 on SD CLK for EMI (Page 5) 4. reserve R483 for CLKRUN# disable (Page 7) 5. change level shifter of PMC_SUSCLK1,LTE_DISABLE#,LTE_WAKE#,PMC_SUSCLK0,SOC_PMC_WAKE#,WIFI_DISABLE# to double inverter for S3 leakage issue (Page 15) 6. stuff C372 for EMI issue(Page 16) 7. add PD13 for S3 leakage(Page 28) 8. reserve C330 for EMI request (Page 25) 9. reserve placeholder R212,R218 for additional RAM ID (Page 7) 10. change bi-direction level shifter of LTE_DISABLE#,LTE_WAKE#, SOC_PMC_WAKE#,WIFI_DISABLE# to double inverter for S3 leakage issue, and PMC_SUSCLK0 and PMC_SUSCLK1 to buffer type (Page 15) 11. Reserve load switch(U1007,C391,R623) for touch screen power(Page 17) 12. reserve R91 0 ohm on SIM_DET line for difference design of various cards(Page 15) 13. Change below 0 ohm to short pad for cost saving: 0402: R180,R197,R204,R123,R131,R139,R455,R462,R103,R414,R383,R375,R381,R379,R183,R452,R457,R58,R165,R468,R448,R107,R424, R449,R343,R385,R54,R378,R380,R430,R456,R110,R114,R121,R395,R400,R407,R453,R464,R460,R319,R320,R332,R263,R333,R171,R174, R137,R10,R11,R13,R326,R341,R339,R20,R46,R411,R51,R60,R72,R57,R370,R67,R194,R244,R390,R213,R546,R227,R173,R169 0603: R116,R157,R193,R555,R14,R224,R355,R229,R232,R235,R241,R217,L7,R206 0805: R354,R384,R17,R39 14. Change LED1 to Green/Orange 15. Change C78 to 220uF 16. Add C393 2.2uF at Q33 pin2, change R414 to 1Mohm 17. Add D23 for Pp5000

Quanta Computer Inc.
PROJECT : 0C2A

Size	Document Number	Rev
	Change list-2	1A

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