NL6

01

Intel Bay Trail-M Platform Block Diagram

SKUA QC N2920
AJ0QFW3UT05--CPU (1170P)N2920 1.86G QFW3(FCBGA)

SKUB DC N2820
AJ0QFW4UT02--CPU (1170P)N2820 2.13G QFW4(FCBGA)

BQ24715 Batery Charger	TPS51216 PP1350
NB670/NB671 PP3300_DSW/PP5000	TLV62150ARGTR PP1050_PCH
ISL95833HRTZ-T +VCC_CORE/+VCC_GFX	TLV62130ARGTR PP1000_PCH_S5
Discharger	

DDR3L 1333
Memory down
2 Channel 1Rx16
PAGE 11,12

DDR3L

eMMC
SDIN8DE2-16G
PAGE 21

MMC

SD card
PAGE 16

SDIO

1.8V BIOS+TXE
SPI ROM(64Mb)
W25Q64FWSSIG
PAGE 6

SPI Interface

Intel Bay Trail-M

Power : TDP 7.5 Watt

Package : FCBGA 1170

Size : 25 x 27 (mm)

Int

PAGE 2~10

DDI 1 — X4 LANES — eDP PAGE 17

32.768KHz PAGE 6

25 Mhz PAGE 6

DDI 0 — HDMI Conn PAGE 19

I2C Interface

Port0 — Track Pad PAGE 26

Port4 — ALS ILS29035 CCD Integrated PAGE 17

Port5 — Touch Screen MXT1664S PAGE ?
In touch panel PCBA

USB 3.0 Interface

Port0 — USB Charger TPS2546 PAGE 25 — USB3.0 Port x 1 PAGE 25

Port0

USB 2.0 Interface

Port3 — CCD PAGE 17

Port2

Port1 — Daughter Board

- USB Hub GL852G-OHG12
  - USB Hub -2 — NGFF M.2 3042-B LTE PAGE 16
  - USB Hub -1 — USB Charger TPS2546 — USB2.0 Port x 1

LPC Interface

I2S+I2C(PORT1)

PCIE Gen 2 x 1 Lane

- TPM SLB9655TT1.2 FW4.32GOOG PAGE 22
- TI KBC TM4E1G31H6ZRB Package : BGA-157 Size : 9.1 x 9.1 (mm) PAGE 27
  - Thermal IC TMP432A PAGE 26
  - Keyboard PAGE 26
- Audio Codec MAX98090 Package : TQFN-40 Size : 5 x 5 (mm) PAGE 24
  - Speaker PAGE 24
  - MIC SW TS3A225E PAGE 24
  - Combo Jack Headphone + MIC PAGE 24
  - DMIC CCD Integrated PAGE 24
- Port1 — M.2 LGA 1216-S3 Video Codec PCIE CLK PORT 1 PAGE 20
- Port0 — NGFF M.2 2230-E WLAN / BT Combo PCIE CLK PORT 0 PAGE 20

LTE UART COEXISTENCE

BOM value option:
CHB@-==>DDR Single channel or dual channel
EDP@ =>4 Lane eDP
TS@ =>Touch screen
SX@ => S0IX
NSX@=> Non S0ix
VC@ =>Video codec
LTE@ => LTE
GD@ =>Google debug

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Size	Document Number	Rev
	Intel Block Diagram	1A

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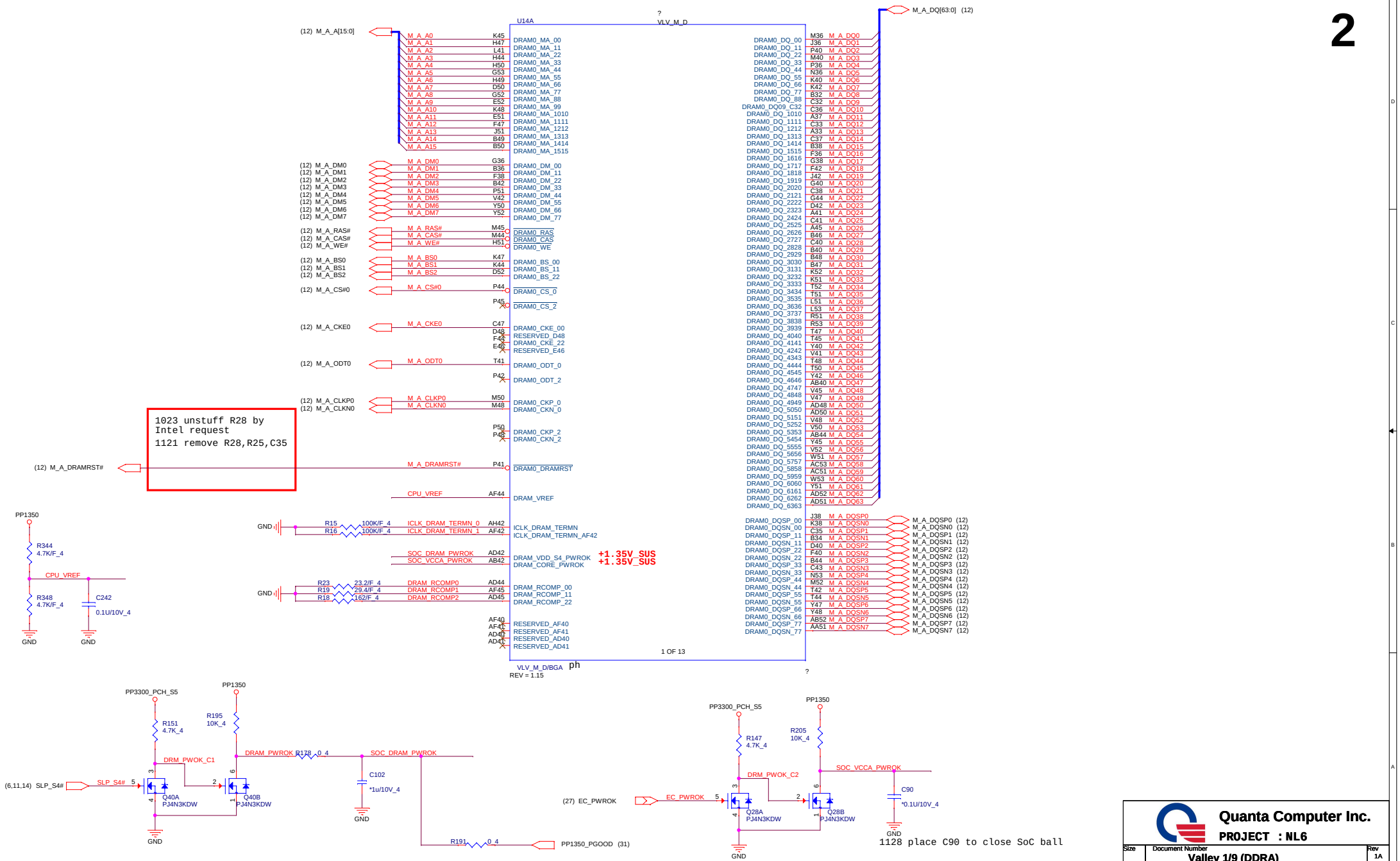

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Size	Document Number: Valley 1/9 (DDRA)	Rev: 1A
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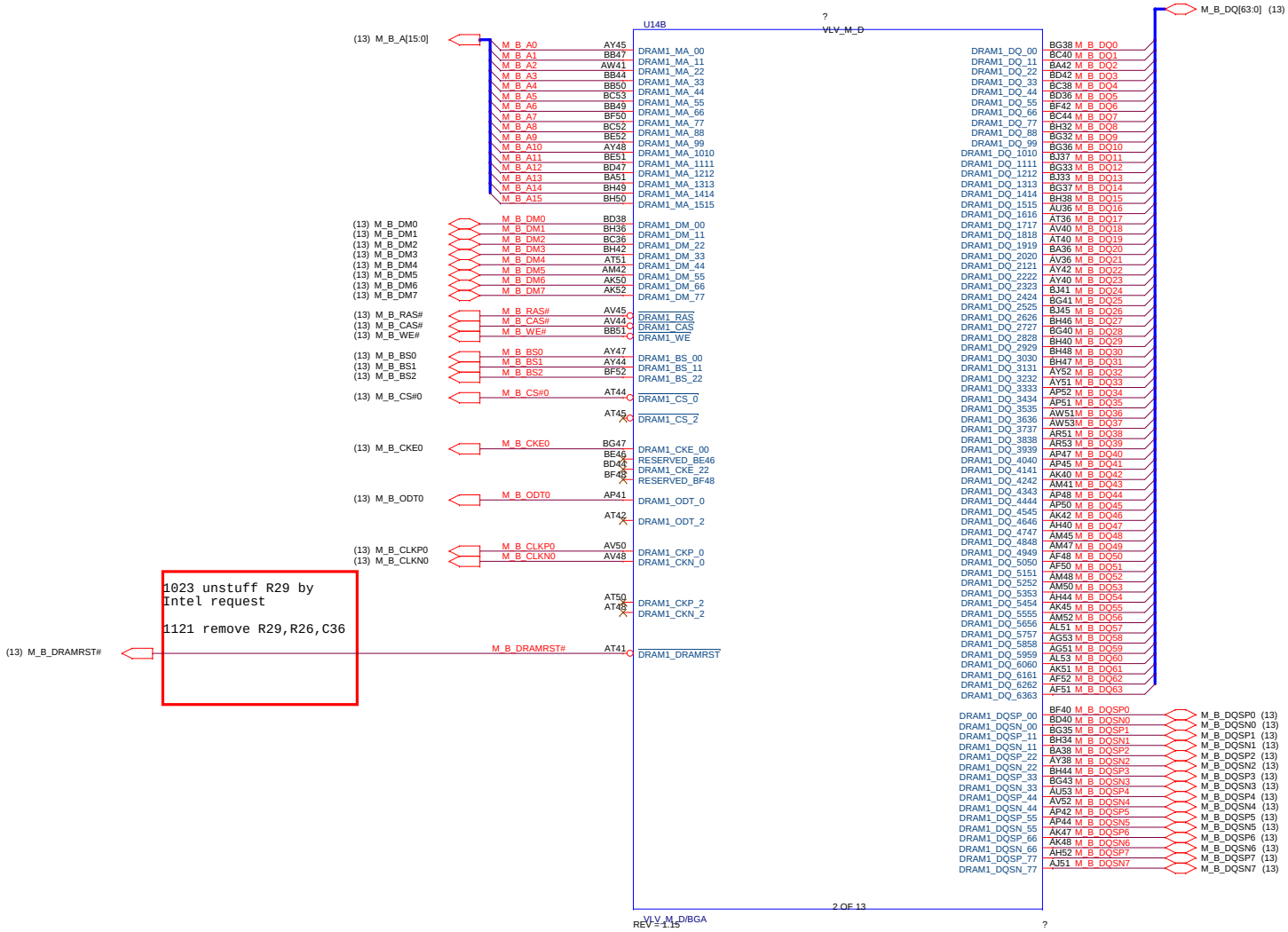

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Size	Document Number: Valley 2/9 (DDRB)	Rev: 1A
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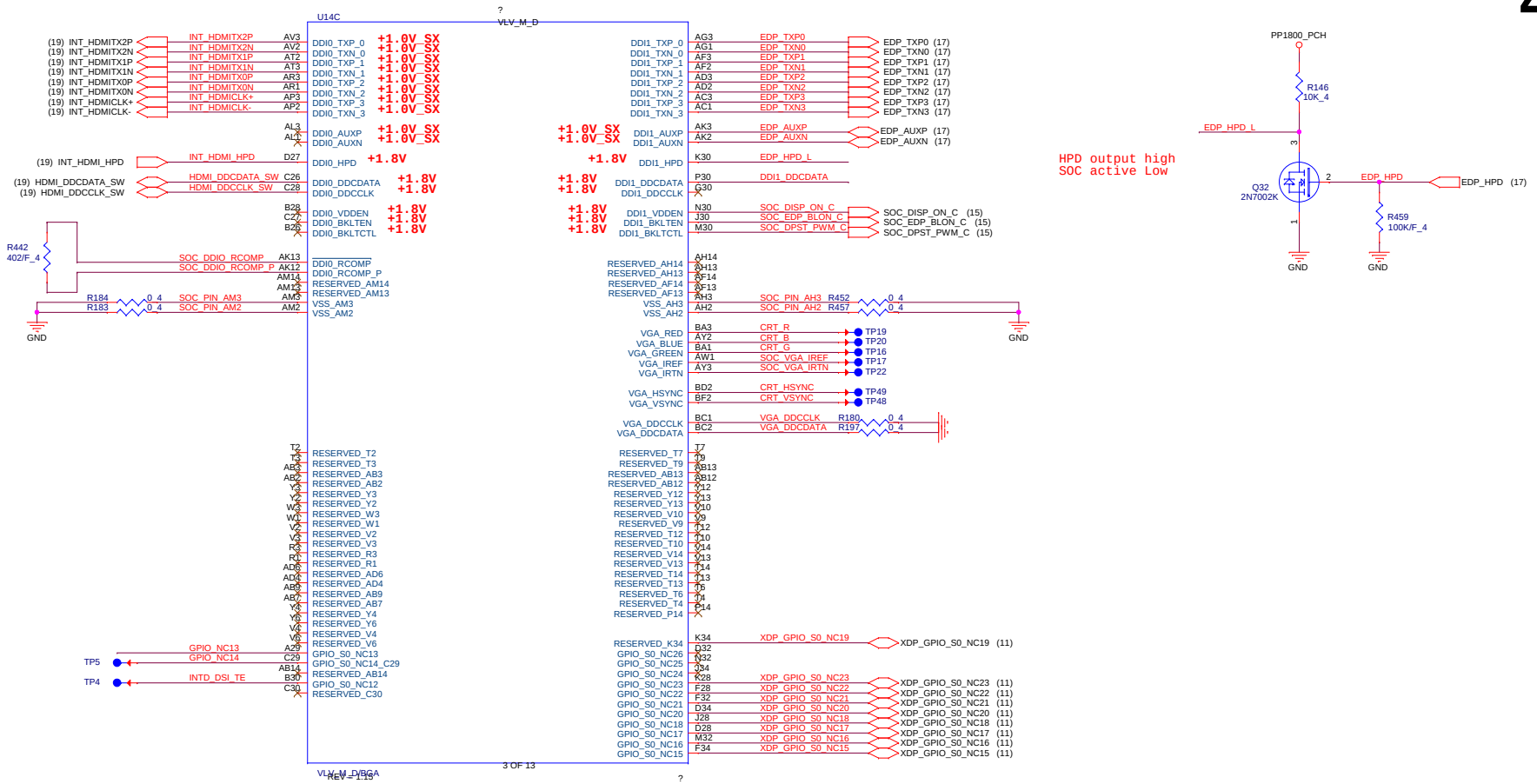

BTM Strapping Table

Pin Name	Strap description	Sampled	Configuration	Note
GPIO_SO_SC_56	Top Swap (A16 Override)	PWROK	0 = Top address bit is unchanged **1 = Top address bit is inverted**	1029 unstuff R128, using SoC internal PU
LPE_I2S2_FRM	BIOS Boot Selection	PWROK	0 = LPC **1 = SPI**	1029 unstuff R372, using SoC internal PU
GPIO_SO_SC_65	Security Flash Descriptors	PWROK	0 = Override **1 = Normal operation**	1115 stuff R372, system can't boot if un-stuff R372 on proto1.5 board, need intel double confirm before proto2
DDI0_DDCDATA	DDI0 Detect	PWROK	0 = DDI0 not detected **1 = DDI0 detected**	Pull up +1.8V at HDMI side
DDI1_DDCDATA	DDI1 Detect	PWROK	0 = DDI0 not detected **1 = DDI0 detected**	1029 unstuff R386, using SoC internal PU 1115 stuff R386, it is required for eDP connected
GPIO_SO_NC_13				

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	Valley 3/9 (Display)	1A

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1025 Delete complete SSD(connector and caps), unstuff R215 and add test points on SATA signals

PP1800_PCH
R215 *10K_4 SATA_DEVSLP_C
R198 *10K_4 SATA_LED_R_N

U14D
VLV_M_D

TP34 TP36 SATA_TXP0_SSD SATA_TXN0_SSD
TP37 TP38 SATA_RXP0_SSD SATA_RXN0_SSD
SATA_TXP_0 SATA_TXN_0
SATA_RXP_0 SATA_RXN_0
SATA_TXP1 SATA_TXN_1
SATA_RXP_1 SATA_RXN_1
GND R131 0_4 R139 0_4 ICLK_SATA_TERMP ICLK_SATA_TERMN
ICLK_SATA_TERMP ICLK_SATA_TERMN
(14) SOC_KBC_SCI R204 0_4 SATA_GP0
SATA_GP0 SATA_DEVSLP_C SATA_LED_R_N
SATA_GP0 SATA_GP1 SATA_LED +1.8V
SATA_RCOMP_DP SATA_RCOMP_DN
R408 402/F_4
SATA_RCOMP_P_AU18 SATA_RCOMP_N_AT18 +1.8V +1.8V

(21) EMMC_CLK
(21) EMMC_D0 (21) EMMC_D1 (21) EMMC_D2 (21) EMMC_D3 (21) EMMC_D4 (21) EMMC_D5 (21) EMMC_D6 (21) EMMC_D7
(21) EMMC_CMD (21) EMMC_RST#
R409 49.9/F_4 EMMC_RCOMP
MMC1_CLK MMC1_D0 MMC1_D1 MMC1_D2 MMC1_D3 MMC1_D4 MMC1_D5 MMC1_D6 MMC1_D7
MMC1_CMD MMC1_RST +1.8V
MMC1_RCOMP
GND

SD2_CLK SD2_D0 SD2_D1 SD2_D2 SD2_D3_CD SD2_CMD

(16) SD3_CLK (16) SD3_D0 (16) SD3_D1 (16) SD3_D2 (16) SD3_D3 (16,18) SD3_CD# (16) SD3_CMD
TP23 (16) SDIO3_PWR_EN#
SD3_CLK SD3_D0 SD3_D1 SD3_D2 SD3_D3 SD3_CD# SD3_CMD SDMMC3_1P8_EN SDIO3_PWR_EN#
SD3_CLK SD3_D0 SD3_D1 SD3_D2 SD3_D3 SD3_CD# SD3_CMD SD3_1P8EN SD3_PWREN +1.8V/+3.3V +1.8V
R403 49.9/F_4 SDIO3_RCOMP
SD3_RCOMP
GND

VLV_M_D/BGA
REV = 1.15
4 OF 13

PCIE_TX0+_WLAN_C_C336 PCIE_TX0-_WLAN_C_C341 0.1U/10V_4
PCIE_TX0+_WLAN (20) PCIE_TX0-_WLAN (20)
PCIE_RX0+_WLAN PCIE_RX0-_WLAN
PCIE_RX0+_WLAN (20) PCIE_RX0-_WLAN (20)
PCIE_TX1+_IMAGE_C_C322 PCIE_TX1-_IMAGE_C_C328 0.1U/10V_4
PCIE_TX1+_IMAGE (20) PCIE_TX1-_IMAGE (20)
PCIE_RX1+_IMAGE PCIE_RX1-_IMAGE
PCIE_RX1+_IMAGE (20) PCIE_RX1-_IMAGE (20)

1213 swap CLKREQ_WLAN and CLKREQ_IMAGE for CLKREQ and CLK pins are aligned

VSS_BB7 VSS_BB5 R455 0_4 R462 0_4 GND
PCIE_CLKREQ_IMAGE# PCIE_CLKREQ_WLAN# I2S_DOUT
R152 10K_4 R148 10K_4 R364 *10K_4
PP1800_PCH
1029 unstuff R364, using SoC internal PU

PCIE_CLKREQ_0 PCIE_CLKREQ_1 PCIE_CLKREQ_2 PCIE_CLKREQ_3 SD3_WP_BD5 +1.8V
PCIE_CLKREQ_WLAN# PCIE_CLKREQ_IMAGE# PCIE_CLKREQ_LAN# PCIE_CLKREQ3# SD3_WP
PCIE_CLKREQ_WLAN# (20) PCIE_CLKREQ_IMAGE# (20)
TP18 TP15 SD3_WP (16)

PCIE_RCOMP_P_AP14_AP14 PCIE_RCOMP_N_AP13_AP13
SOC_PCIE_COMP SOC_PCIE_COMN
R431 402/F_4
RESERVED_BB4 RESERVED_BB3 RESERVED_AV10 RESERVED_AV9

HDA_LPE_RCOMP HDA_RST HDA_SYNC HDA_CLK HDA_SDO HDA_SDI0 HDA_SDI1 HDA_DOCKRST HDA_DOCKEN +1.8V/1.5V
HDA_RCOMP R410 49.9/F_4 GND
ACZ_RST# ACZ_SYNC ACZ_BCLK ACZ_SDOUT PCH_AZ_CODEC_SDIN0 DET_TRIGGER HDA_DOCKEN# R123 0_4
TP6 TP10 TP7 TP8 TP9
DET_TRIGGER (24) AJACK_MICPRES_L (24)

LPE_I2S2_CLK LPE_I2S2_FRM LPE_I2S2_DATAOUT LPE_I2S2_DATAIN +1.8V
I2S_BCLK I2S_LRCLK I2S_DOUT I2S_DIN
R383 R375 R381 R379 0_4
I2S_BCLK_R (24) I2S_LRCLK_R (24) I2S_DOUT_R (24) I2S_DIN_R (24)

RESERVED_P34 RESERVED_N34
RESERVED_AK9 RESERVED_AK7
R96 71.5/F_4 PP1000_PCH
SOC_PROCHOT# R103 0_4 H_PROCHOT#
PROCHOT +1.0V
R414 0_4 R553 0_4
H_PROCHOT# (18,27,33) IMVP7_PROCHOT# (28) ALERT# (23)

1021 un-stuff R553

0 = LPC
1 = SPI
I2S_LRCLK I2S_DOUT
I2S_LRCLK (4) I2S_DOUT (4)
Security Flash Descriptors
0 = Override
1 = Normal Operation
Need check to see if MOSFET isolation needed or not

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6

1121 by X'tal vender suggestion, change C105/C106 from 15pF to 12pF

1031 remove R417, PRDY should be direct connection between SoC and XDP by intel request

1128 add a connection and name to KBD_IRQ#, besides add pulled high resistor

1025 add level shifter for LTE SUSCLK

9/6 Add EC_RCIN_L for warm boot, EC side is OD type

U14E — VLV_M_D — 5 OF 13 — VLV_M_D/BGA REV = 1.15

RTC Clock 32.768KHz

RTC Circuitry(RTC)

30mils

SPI ROM needs power in S3/S5 for the TXE (Trusted execution engine).

U22 — SPI_FLASH — soic8-7_9-1_27 — AKE5EZN0N00 — IC FLASH (8P) W25Q64FWSSIG (SOIC)

LAYOUT CLOSE TO SPI ROM

SPI NOR FLASH

near SPI ROM as possible

To debug header

To PCH

PCH_SPI_WP_D connect to GPIO58 at GRB

From Screw/EC

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Size | Document Number: Valley 5/9 (SPI/GPIO/CLK) | Rev 1A

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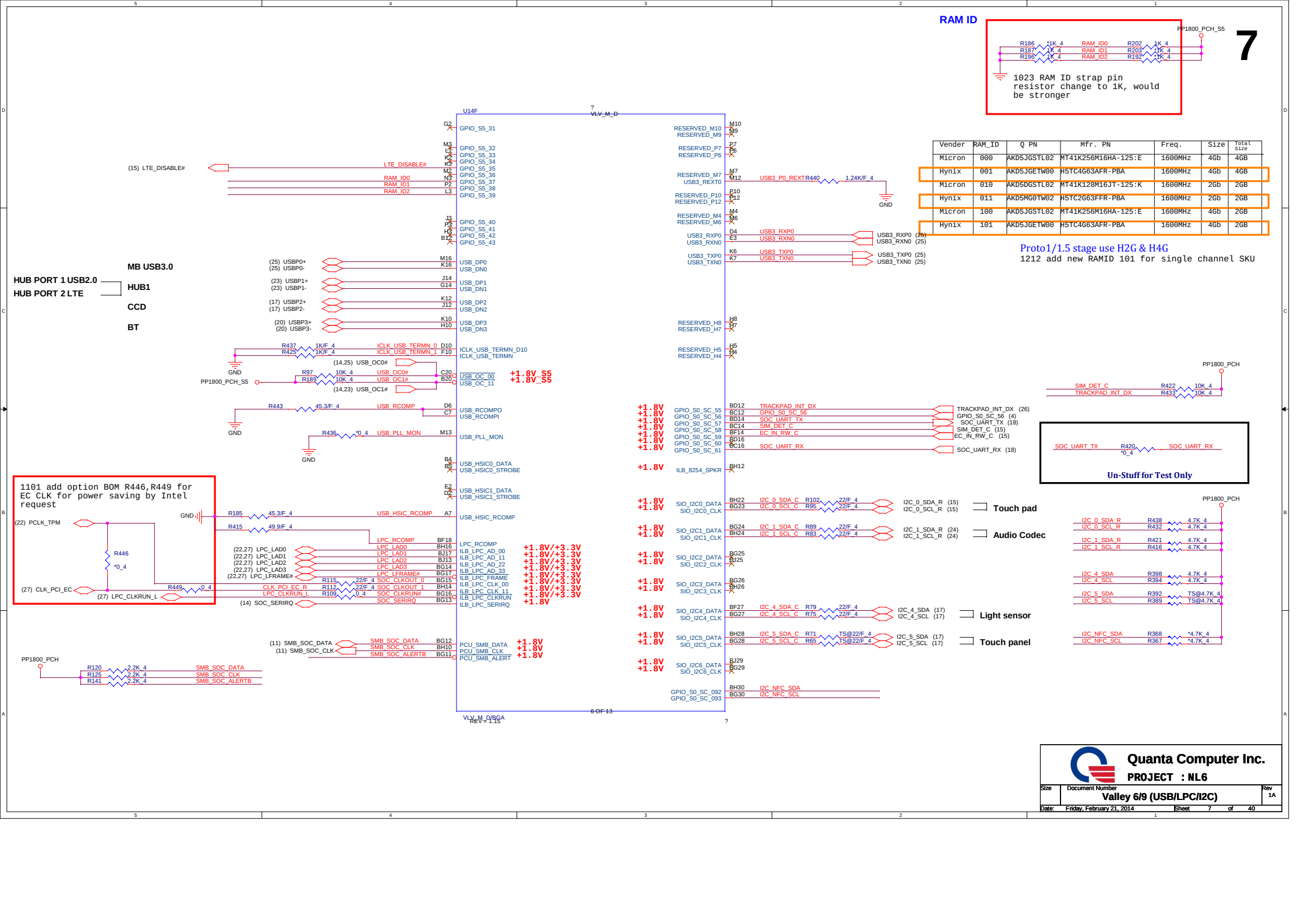

Vender	RAM_ID	Q PN	Mfr. PN	Freq.	Size	Total Size
Micron	000	AKD5JGSTL02	MT41K256M16HA-125:E	1600MHz	4Gb	4GB
Hynix	001	AKD5JGETW00	H5TC4G63AFR-PBA	1600MHz	4Gb	4GB
Micron	010	AKD5DGSTL02	MT41K128M16JT-125:K	1600MHz	2Gb	2GB
Hynix	011	AKD5MG0TW02	H5TC2G63FFR-PBA	1600MHz	2Gb	2GB
Micron	100	AKD5JGSTL02	MT41K256M16HA-125:E	1600MHz	4Gb	2GB
Hynix	101	AKD5JGETW00	H5TC4G63AFR-PBA	1600MHz	4Gb	2GB

Proto1/1.5 stage use H2G & H4G
1212 add new RAMID 101 for single channel SKU

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1031 for layout suggestion by intel, VSS_AXG_SENSE didn't connect to VSS_SENSE, will connect the GND via near VCC_AXG_SENSE

1031 for layout, add 0hm between GND and VSS_AXG_SENSE

(33) VSS_AXG_SENSE — R385 0_4 — GND

+VCC_GFX +VCC_CORE

R458 100/F_4 R373 100/F_4

VCC_SENSE

VCC_AXG_SENSE

VSS_SENSE

R382 100/F_4

GND

U14G

?

VLV_M_D

(33) VCC_SENSE — VCC_SENSE — P28 CORE_VCC_SENSE_P28

(33) VCC_AXG_SENSE — VCC_AXG_SENSE — BB8 UNCORE_VNN_SENSE

(33) VSS_SENSE — VSS_SENSE — N28 CORE_VSS_SENSE_N28

PP1350 — R343 0_4 — PP1350_VSM

C231 1U/6.3V_4
C251 1U/6.3V_4
C38 0.1U/10V_4

AD38 DRAM_VDD_S4_AD38
AF38 DRAM_VDD_S4_AF38
A48 DRAM_VDD_S4
AK38 DRAM_VDD_S4_AK38
AM38 DRAM_VDD_S4_AM38
AV41 DRAM_VDD_S4_AV41
AV42 DRAM_VDD_S4_AV42
BB46 DRAM_VDD_S4_BB46

PP1350

DRAM_VDD_S4_BD49 BD49
DRAM_VDD_S4_BD52 BD52
DRAM_VDD_S4_BD53 BD53
DRAM_VDD_S4_BF44 BF44
DRAM_VDD_S4_BG51 BG51
DRAM_VDD_S4_BJ48 BJ48
DRAM_VDD_S4_C51 C51
DRAM_VDD_S4_D44 D44
DRAM_VDD_S4_F49 F49
DRAM_VDD_S4_F52 F52
DRAM_VDD_S4_F53 F53
DRAM_VDD_S4_H46 H46
DRAM_VDD_S4_M41 M41
DRAM_VDD_S4_M42 M42
DRAM_VDD_S4_V38 V38
DRAM_VDD_S4_Y38 Y38

C235 1U/6.3V_4 C240 1U/6.3V_4 C236 1U/6.3V_4 C237 1U/6.3V_4 C238 1U/6.3V_4 C239 1U/6.3V_4

GND

+VCC_CORE

AA27 CORE_VCC_S0IX_AA27
AA29 CORE_VCC_S0IX_AA29
AA30 CORE_VCC_S0IX_AA30
AC27 CORE_VCC_S0IX_AC27
AC29 CORE_VCC_S0IX_AC29
AC30 CORE_VCC_S0IX_AC30
AD27 CORE_VCC_S0IX_AD27
AD29 CORE_VCC_S0IX_AD29
AD30 CORE_VCC_S0IX_AD30
AF27 CORE_VCC_S0IX_AF27
AF29 CORE_VCC_S0IX_AF29
AG27 CORE_VCC_S0IX_AG27
AG29 CORE_VCC_S0IX_AG29
AG30 CORE_VCC_S0IX_AG30
P26 CORE_VCC_S0IX_P26
P27 CORE_VCC_S0IX_P27
U27 CORE_VCC_S0IX_U27
U29 CORE_VCC_S0IX_U29
V27 CORE_VCC_S0IX_V27
V29 CORE_VCC_S0IX_V29
V30 CORE_VCC_S0IX_V30
Y27 CORE_VCC_S0IX_Y27
Y29 CORE_VCC_S0IX_Y29
Y30 CORE_VCC_S0IX_Y30

1030 for core power, change C271,C281,C280,C278,C273 to 10uF

1206 change C271,C273,C280 to 0603 22uF for ACLL issue

1204 for z-height issue, change C72,C75,C81 to 0.85mm cap

C271 22u/6.3V_6
C281 10u/6.3V_4
C280 22u/6.3V_6
C278 10u/6.3V_4
C273 22u/6.3V_6
C72 22u/6.3V_8
C83 22u/6.3V_8
C75 22u/6.3V_8
C81 22u/6.3V_8
C79 22u/6.3V_8
C80 22u/6.3V_8
C76 22u/6.3V_8

GND

+VCC_GFX

UNCORE_VNN_S3_AA24 AA24
UNCORE_VNN_S3_AC22 AC22
UNCORE_VNN_S3_AC24 AC24
UNCORE_VNN_S3_AD22 AD22
UNCORE_VNN_S3_AD24 AD24
UNCORE_VNN_S3_AF22 AF22
UNCORE_VNN_S3_AF24 AF24
UNCORE_VNN_S3_AG22 AG22
UNCORE_VNN_S3_AG24 AG24
UNCORE_VNN_S3_AJ22 AJ22
UNCORE_VNN_S3_AJ24 AJ24
UNCORE_VNN_S3_AK22 AK22
UNCORE_VNN_S3_AK24 AK24
UNCORE_VNN_S3_AK25 AK25
UNCORE_VNN_S3_AK27 AK27
UNCORE_VNN_S3_AK29 AK29
UNCORE_VNN_S3_AK30 AK30
UNCORE_VNN_S3_AK32 AK32
UNCORE_VNN_S3_AM22 AM22

C69 10U/6.3V_6 C65 10U/6.3V_6 C68 10U/6.3V_6

GND

C63 22u/6.3V_8 C70 22u/6.3V_8 C64 22u/6.3V_8

C266 22u/6.3V_6 C289 10u/6.3V_4 C290 10u/6.3V_4 C311 22u/6.3V_6 C315 22u/6.3V_6

1030 for Gfx power, change C266,C289,C290 to 10uF and add 2 caps 10uF

1206 change C266,C311,C315 to 0603 22uF for ACLL issue

1030 change C60 power netname for layout

+VCC_GFX

C60 22u/6.3V_8

AF30 TP_CORE_V1P05_S4

TP2_CORE_VCC_S0IX AA22

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VLV_M_D/BGA

REV = 1.15

1031 remove TP44 and TP35 for GND vias adding?

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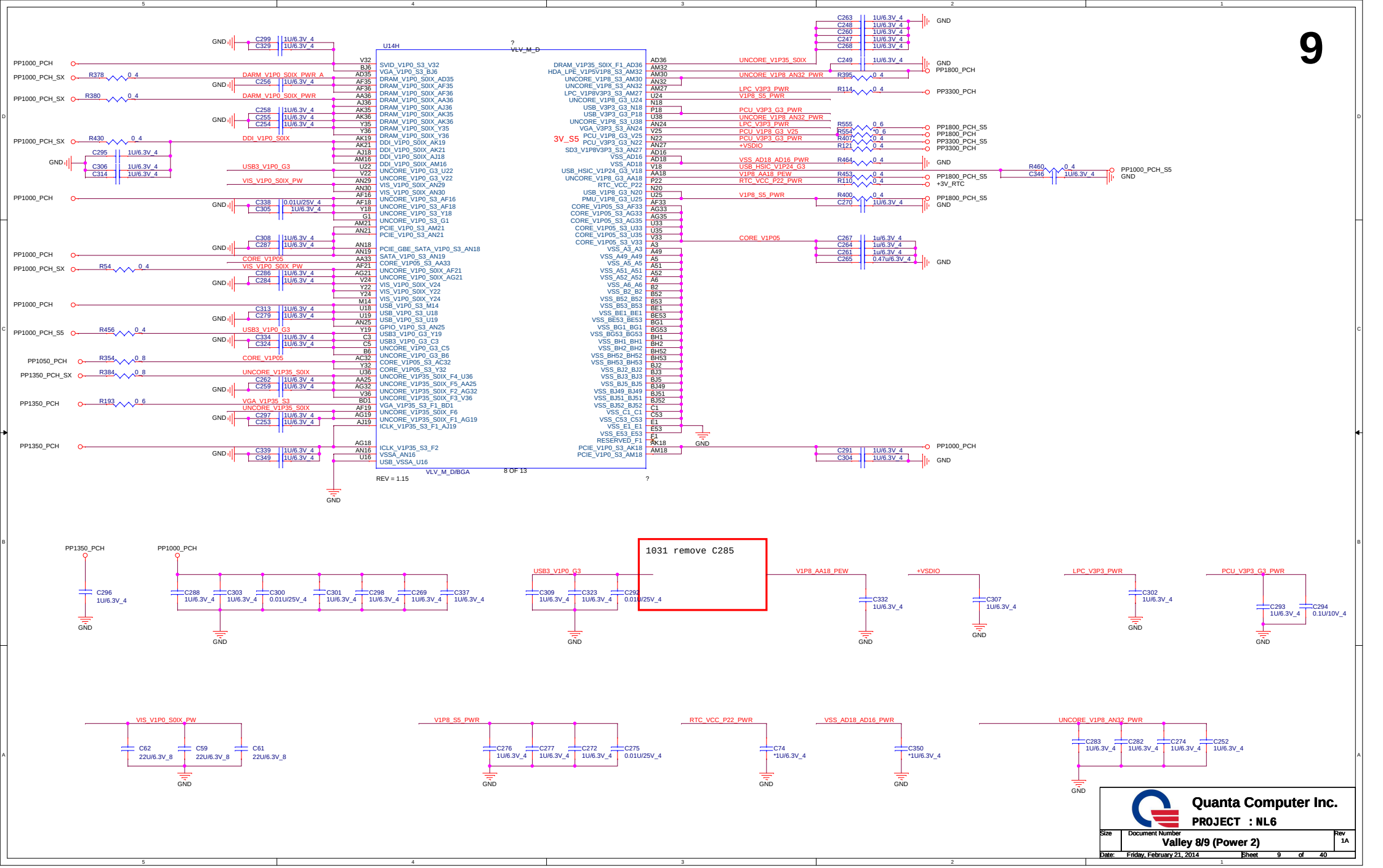
9
U14H
VLV_M_D
VLV_M_D/BGA
8 OF 13
REV = 1.15
1031 remove C285
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Valley 8/9 (Power 2)
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Rev
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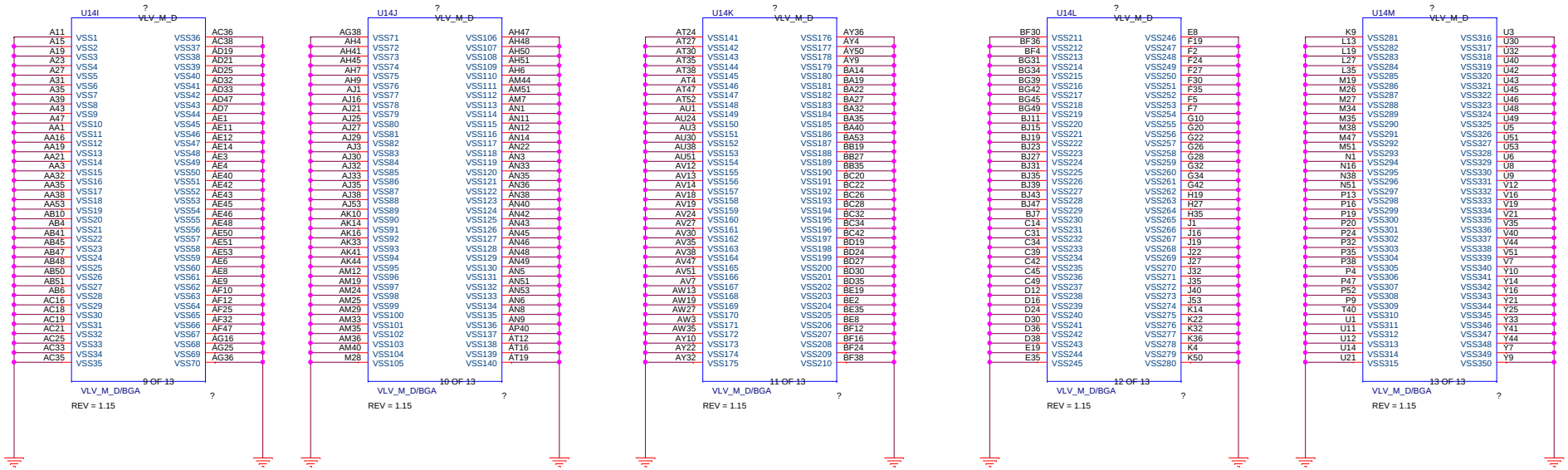

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	Valley 9/9 (GND)	1A

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INTEL Debug Port

11

CN13

*SEC_BSH-030-01-L-D-A-TR

PP1800_PCH_S5 R337 0_6 PP1800_XDP_AB
PP1000_PCH_S5 R334 *0_6
PP1800_PCH R333 0_4 PP1800_XDP_CD

XDP_H_PREQ# XDP_H_PRDY# (6) XDP_H_PRDY#
XDP_GPIO_DFX1 (6) XDP_GPIO_DFX1 (6) XDP_GPIO_DFX2
XDP_GPIO_DFX3 (6) XDP_GPIO_DFX3 (6) XDP_GPIO_DFX4
XDP_GPIO_DFX5 (6) XDP_GPIO_DFX5 (6) XDP_GPIO_DFX6
XDP_GPIO_DFX7 (6) XDP_GPIO_DFX7 (6) XDP_GPIO_DFX8

XDP_GPIO_S0_NC15 XDP_GPIO_DFX0 — XDP_GPIO_S0_NC15 (4) XDP_GPIO_DFX0 (6)
XDP_GPIO_S0_NC16 XDP_GPIO_S0_NC17 — XDP_GPIO_S0_NC16 (4) XDP_GPIO_S0_NC17 (4)
XDP_GPIO_S0_NC18 XDP_GPIO_S0_NC19 — XDP_GPIO_S0_NC18 (4) XDP_GPIO_S0_NC19 (4)
XDP_GPIO_S0_NC20 XDP_GPIO_S0_NC21 — XDP_GPIO_S0_NC20 (4) XDP_GPIO_S0_NC21 (4)
XDP_GPIO_S0_NC22 XDP_GPIO_S0_NC23 — XDP_GPIO_S0_NC22 (4) XDP_GPIO_S0_NC23 (4)

(6,14) SOC_RSMRST# SOC_RSMRST# R317 1K_4 XDP_RSMRST#
(14,27) PCH_PWRBTN_L PCH_PWRBTN_L R332 0_4 XDP_PMU_PWRBTN#
PP1800_XDP_AB (6,27) CORE_PWROK_R CORE_PWROK_R R322 1K_4 XDP_COREPWROK
XDP_RTEST_L R325 0_4 XDP_RTEST#
C199 *0.1u/10V_4
(7) SMB_SOC_DATA SMB_SOC_DATA R320 0_4 SMB_XDP_SDA
(7) SMB_SOC_CLK SMB_SOC_CLK R319 0_4 SMB_XDP_SCL
(6) XDP_H_TCK XDP_H_TCK

XDP_PMU_PLTRST# R306 1K_4 SOC_PLTRST# — SOC_PLTRST# (6,14)
XDP_PMU_RSTBTN# R307 0_4 SOC_REST_BTN# — SOC_REST_BTN# (6,18)
PP1800_XDP_CD
XDP_H_TDO — XDP_H_TDO (6)
XDP_H_TRST# — XDP_H_TRST# (6)
XDP_H_TDI — XDP_H_TDI (6)
XDP_H_TMS — XDP_H_TMS (6)
XDP_PRESENT_N R263 0_4
C177 *0.1u/10V_4

PP3300_PCH_S5
R528 100K_4
SOC_RTEST# (6)
*2N7002K Q55
XDP_RTEST_L
*2N7002K Q54

PP3300_PCH_S5
GND C186 0.1u/10V_4 XDP_RTEST# R324 1K_4
PLACE C6601 closed to XDP HOOK PIN 54
PP1800_XDP_AB
PLACE R295 WITHIN 0.25" FROM XDP PIN
XDP_H_TDO R295 51/F_4

1031 stuff
R273,R286,R289 for
Intel request

PLACE R273,R286,R318 WITHIN 1" FROM SoC PIN
XDP_H_TMS R273 51/F_4
XDP_H_TDI R286 51/F_4
XDP_H_TCK R318 51/F_4
XDP_H_TRST# R289 51/F_4
XDP_PMU_PWRBTN# R321 *30K/F_4
PLACE R6866 closed to XDP
GND

1030 remove PREQ# pulled up resistor R323
1031 put back R323

PLACE R323 WITHIN 1.1" OF BUFFER PIN
XDP_H_PREQ# R323 200/F_4
PP1800_PCH_S5

PP1800_PCH_S5
1030 U10 change to 74AUP1G34 and stuff it
1031 N.C U10 pin1
1101 stuff C16
C16 0.1u/10V_4
(6) XDP_H_PREQ#_C XDP_H_PREQ#_C
U10 74AUP1G34GW
XDP_H_PREQ#
C15 *0.1u/10V_4
R329 *0_4

PP1800_PCH
GND C160 0.1u/10V_4 XDP_PMU_RSTBTN# R308 *1K_4
PLACE C6866 closed to XDP HOOK PIN48

APS

CN14
*ACES_88511-180N

PP3300_PCH_S5
APS1 R502 *0_6
PMC_SLP_S3# R512 *0_4 SLP_S3# — SLP_S3# (6,14)
PMC_SLP_S4# R511 *0_4 SLP_S4# — SLP_S4# (2,6,14)
ILB_RTC_RST# R510 *0_4 SRT_CRST# — SRT_CRST# (6)
PMC_PWRBTN# R509 *0_4 SOC_PWRBTN# — SOC_PWRBTN# (6,14)
PMC_RSTBTN# R508 *0_4 SOC_REST_BTN#

Quanta Computer Inc.
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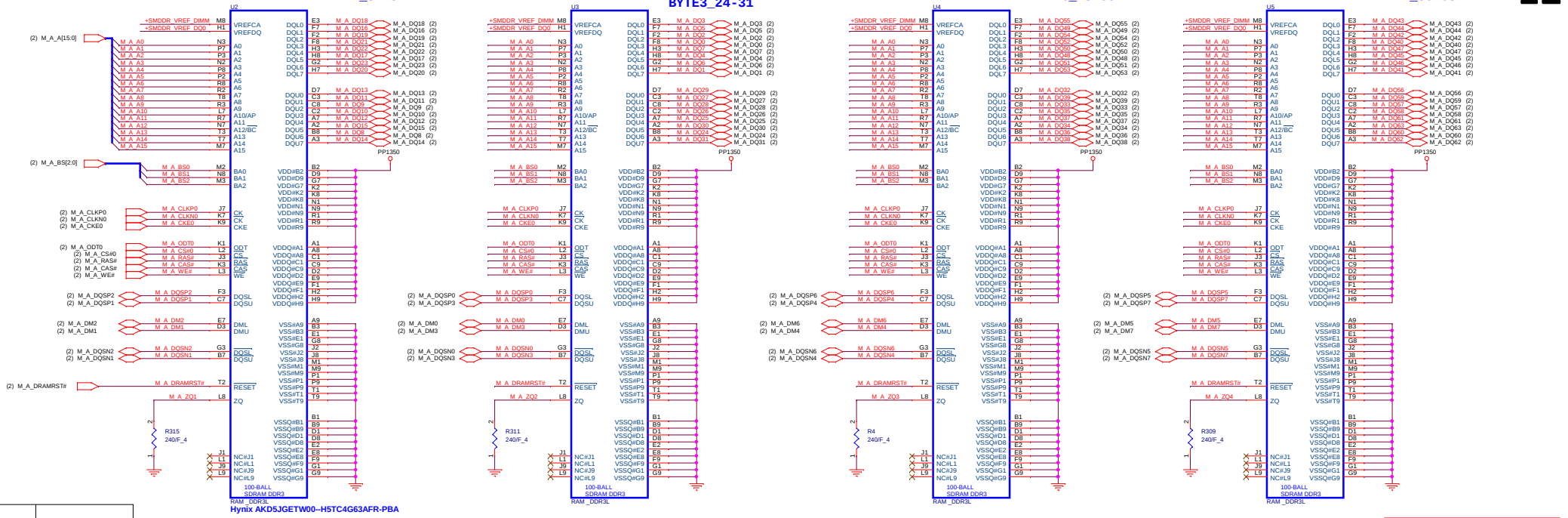
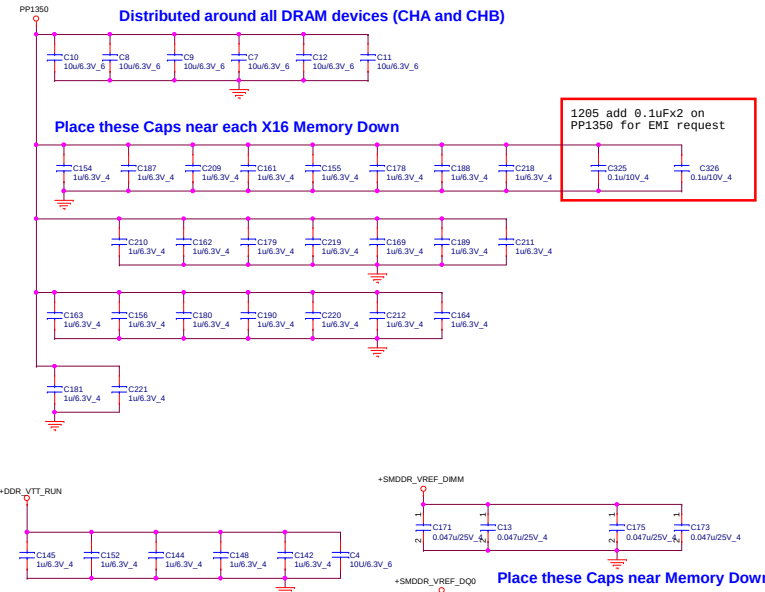
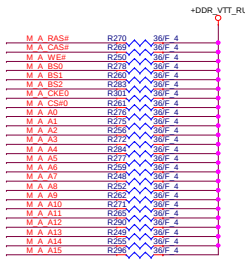
	CPU/PCH XDP	1A
Date: Friday, February 21, 2014	Sheet 11 of 40	

BYTE2_16-23
BYTE1_8-15
BYTE0_0-7
BYTE3_24-31
BYTE4_32-39
BYTE6_48-55
BYTE5_40-47
BYTE7_56-63

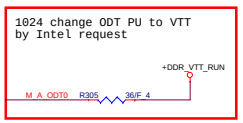


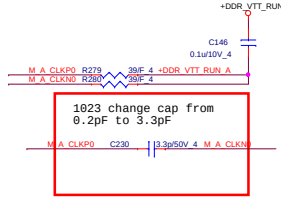
Vendor	P/N	
Hynix		
Elpida	AKD5JGST400	DDR3L 1333Mhz 4Gb
	AKD5JGST404	DDR3L 1600Mhz 4Gb



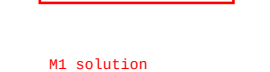


1024 change ODT PU to VTT by Intel request

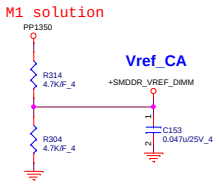




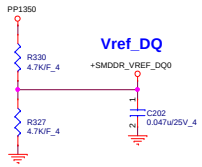
1023 change cap from 0.2pF to 3.3pF



M1 solution



M1 solution



Quanta Computer Inc.
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Size	Document Number	Rev
	DDR3L MEMORY DOWNx16 A	1A
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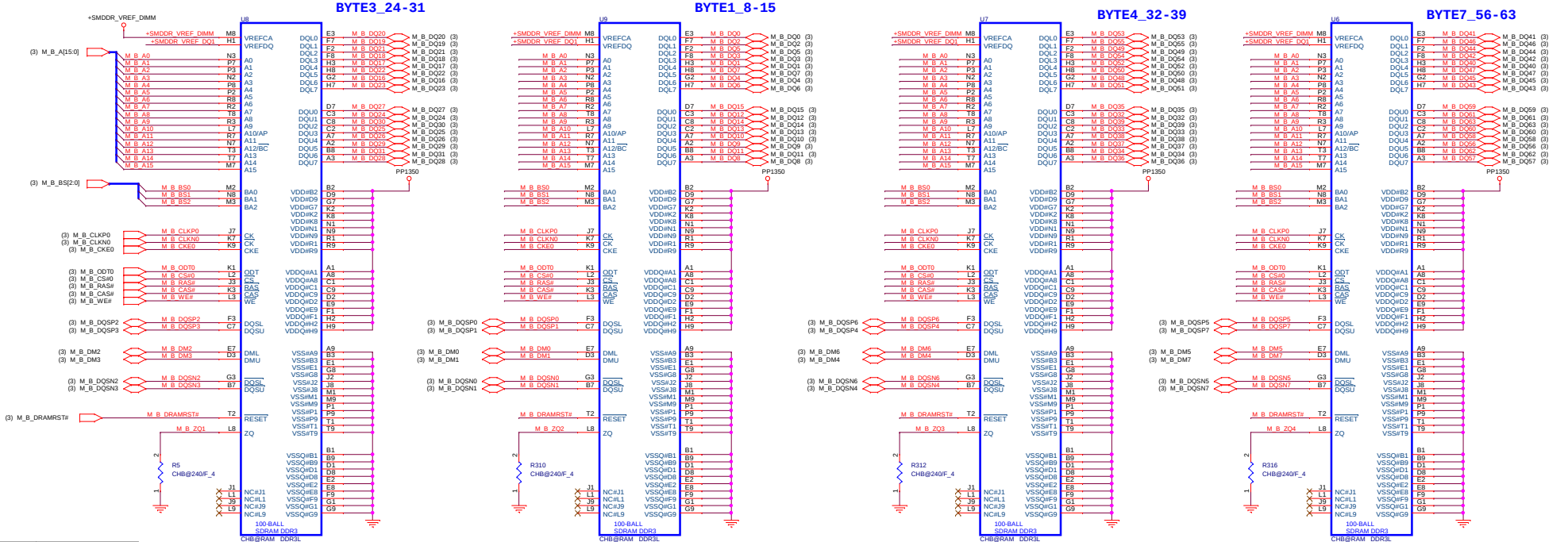
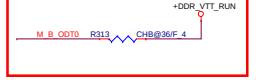
BYTE2_16-23
BYTE3_24-31
BYTE0_0-7
BYTE1_8-15
BYTE6_48-55
BYTE4_32-39
BYTE5_40-47
BYTE7_56-63

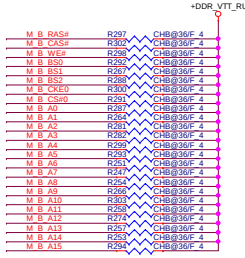


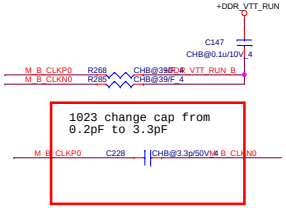
Hynix AKD5JGETW00--H5TC4G63AFR-PBA

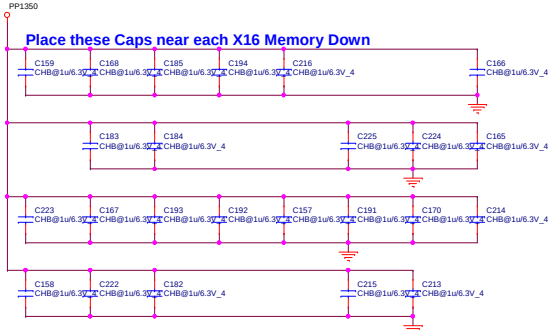
Vendor	P/N	
Micron	AKD5JGSTL02	MT41K256M16HA-125:E
Elpida	AKD5JGST400	
	AKD5JGST404	

1024 change ODT PU to VTT by Intel request

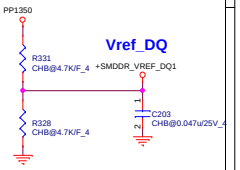


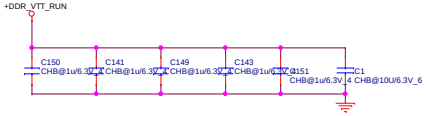


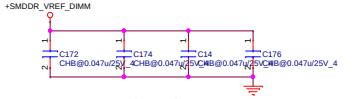




M1 solution







Quanta Computer Inc.	PROJECT : NL6	
Size	Document Number: DDR3L MEMORY DOWNx16 B	Rev: 1A
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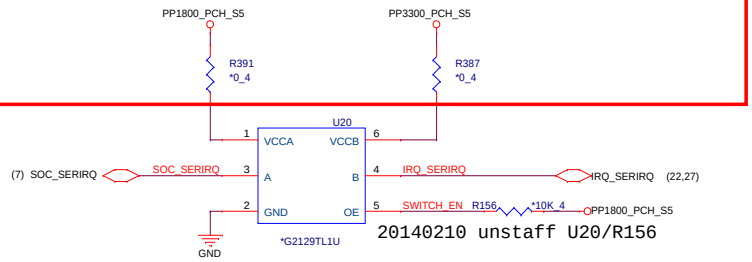
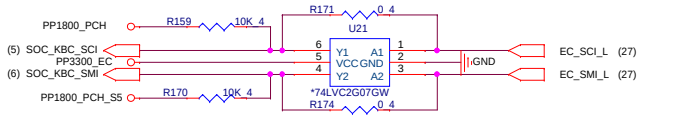
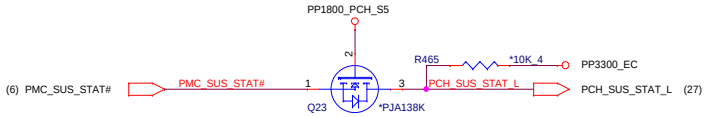
PWRON SEQUENCE

9/6 EC table says SERIRQ is OD pin, reserve for debugging
1128 remove R166, because SERIQR of TPM needs 3V
1128 reserve 0 ohm R387/R391 on VCCA and VCCB for debugging
20140210 unstaff R387/R391

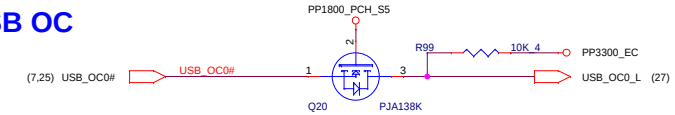


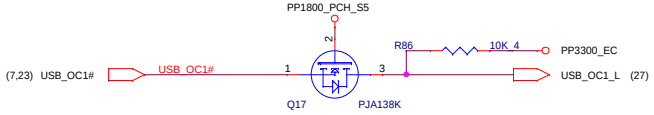
20140210 unstaff U20/R156





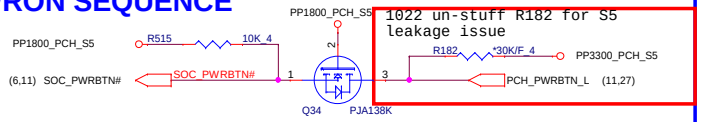
USB OC



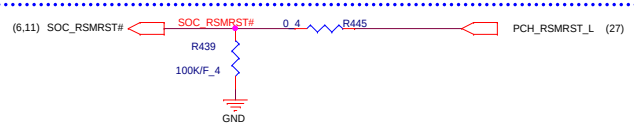


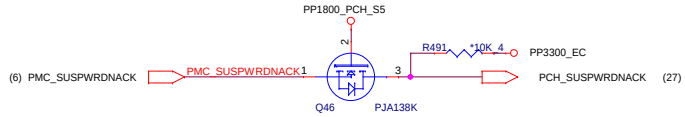
Stuffing for notifying EC

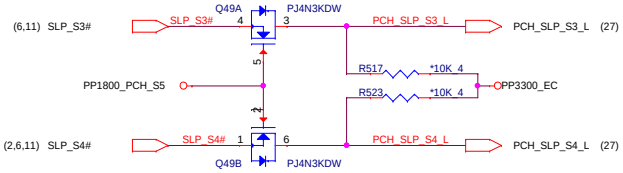
PWRON SEQUENCE

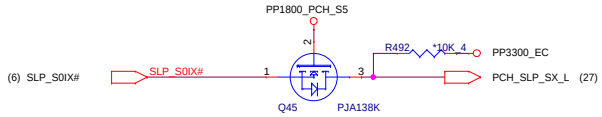


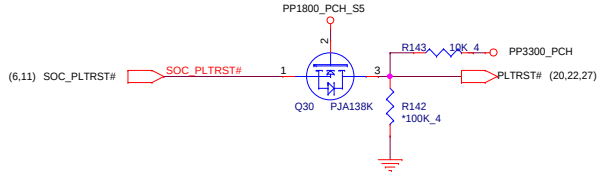
1022 un-stuff R182 for S5 leakage issue

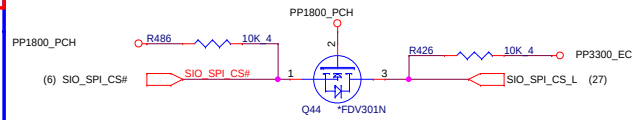


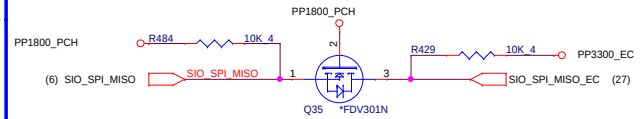


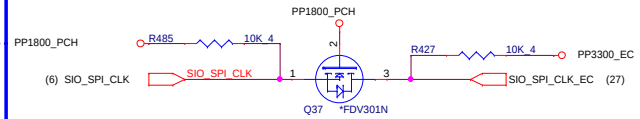


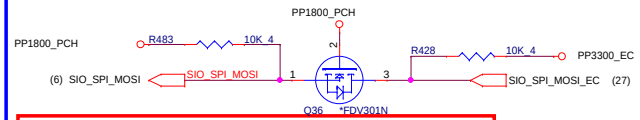












9/6 Need check MOSFET switching speed>15MHz

14

Quanta Computer Inc.
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Size	Document Number	Rev
	Level Shfiter (SOC_EC)	1A
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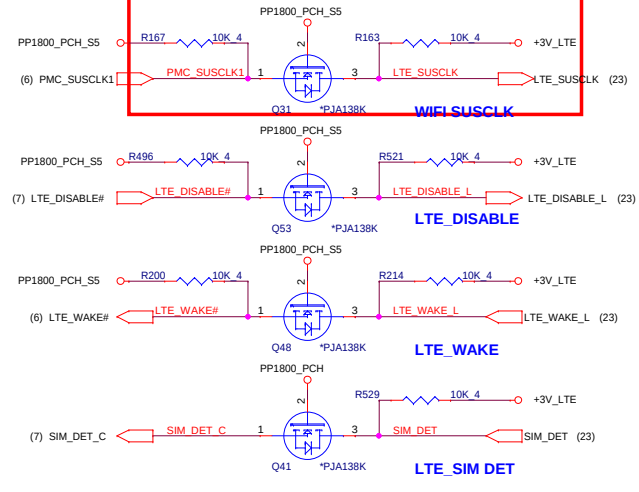
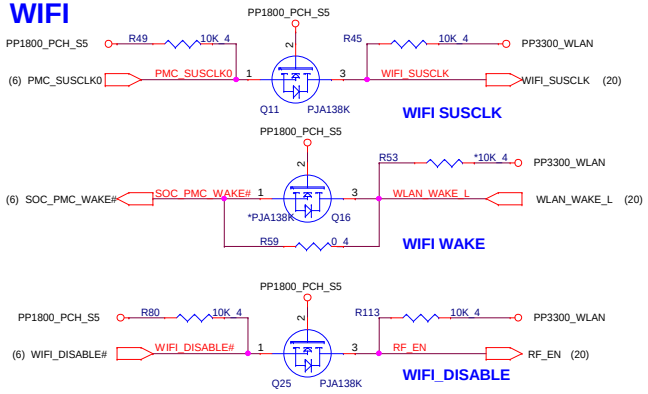
LTE

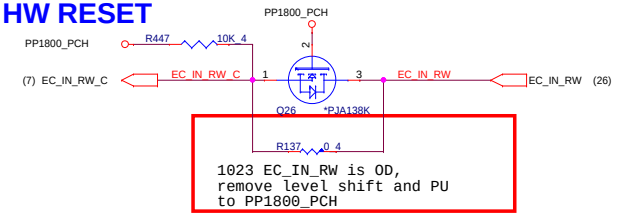
1025 add level shifter for LTE SUSCLK



WIFI



HW RESET



1023 EC_IN_RW is OD, remove level shift and PU to PP1800_PCH

Touch Screen

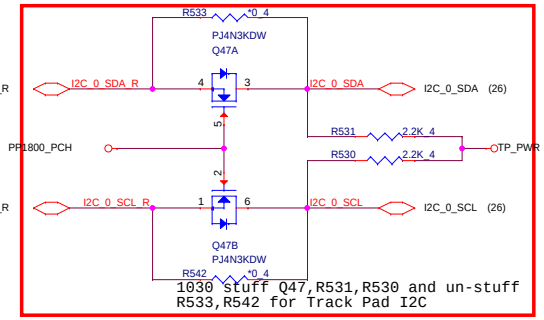
S0

S5

SATA

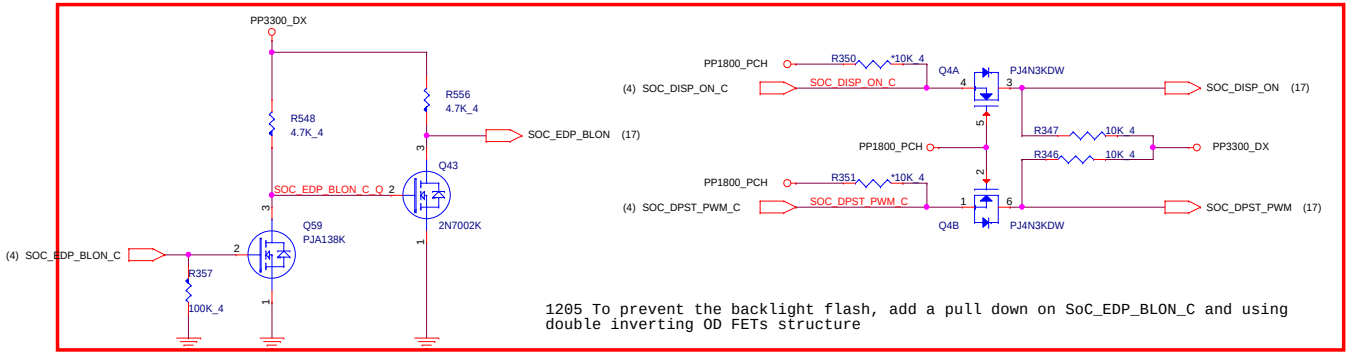
1025 Delete complete SSD(connector and caps)

Track Pad



1030 Stuff Q47,R531,R530 and un-stuff R533,R542 for Track Pad I2C

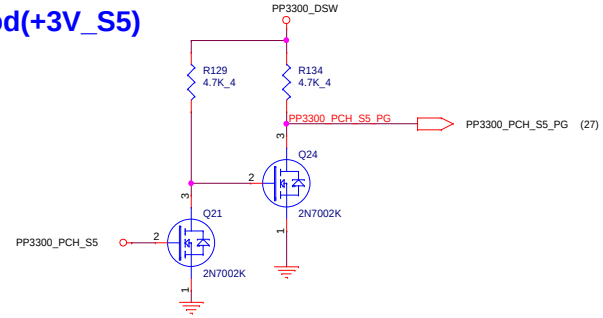
eDP control pin



1205 To prevent the backlight flash, add a pull down on SoC_EDP_BLON_C and using double inverting OD FETs structure

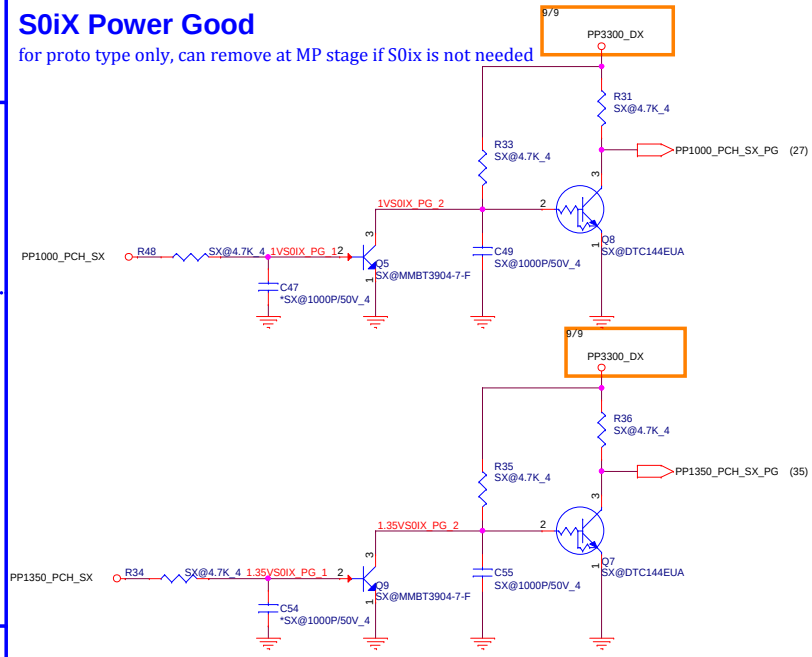
S5 Power Good(+3V_S5)

0830 A24

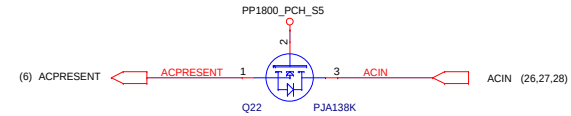


S0iX Power Good

for proto type only, can remove at MP stage if S0ix is not needed



AC Detect



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Size	Document Number	Rev
	Level Shfiter (SOC_DEV)	1A
Date: Friday, February 21, 2014	Sheet 15 of 40	

SD/MMC CARD READER CONNECTOR (MMC)

1025 the damping of SDIO change to 0 ohm by Intel request

1025 add PU for SDIO WP by Intel request

1205 R551 changes to 1K to isolate SD socket and servo/SoC

1205 SD3_WP is 1.8V power rail in SoC, change external Pulled up power well of SD3_WP to 1.8V power

(5) SD3_D3
(5) SD3_CMD
(5) SD3_CLK
(5) SD3_D0
(5) SD3_D1
(5) SD3_D2
(5,18) SD3_CD#
(5) SD3_WP

SD3_D3 R489 0_4 SD_DAT3
SD3_CMD R507 0_4 SD_CMD_R
SD3_CLK R526 0_4 SD_CLK_R
SD3_D0 R541 0_4 SD_DAT0
SD3_D1 R549 0_4 SD_DAT1
SD3_D2 R550 0_4 SD_DAT2
SD3_CD# R551 1K_4 SD_CD#_R
SD3_WP R552 0_4 SD_WP_R

R160 10K_4 PP1800_PCH

This is full size SD card

CN15

SD_WP_R 11 WP
SD_CD#_R 10 CD
SD_DAT2 9 DATA2
SD_DAT1 8 DATA1
SD_DAT0 7 DATA0
6 VSS2
SD_CLK_R 5 CLK
VCC_SD 4 VDD
3 VSS1
SD_CMD_R 2 CMD
SD_DAT3 1 CD/DATA3

NC 16
NC 17

GND 12
GND 13
GND 14
GND 15

TAS_5-251301001000-6

VCC_SD

30mils

C375 10U/6.3V_4
C371 0.1U/10V_4
C374 0.1U/10V_4
C376 0.1U/10V_4

SD_WP_R
SD_CLK_R

C373 *33P/50V_4
C372 *33P/50V_4

1202 add C285 for U18 input inrush current

PP1800_PCH
PP3300_DX

R154 *4.7K_4
R539 4.7K_4

C285 1u/6.3V_4

PP3300_DX

SDIO3_PWR_EN

U18
5 IN
4 IN
3 ON/OFF
OUT 1
GND 2
G5243AT11U

VCC_SD

C342 0.1U/10V_4

C351 4.7U/6.3V_4

1101 correct C351 footprint

1115 U18 footprint change to 5 pin which is same as eDP power switch

(5) SDIO3_PWR_EN#

Q58
PJA138K

1211 add pulled up resistors on SDIO data/cmd lines
1212 all Pulled up resistors of SDIO data/cmd to be un-stuffed

VCC_SD

R559 *47K_4 SD_CMD_R
R478 *47K_4 SD_DAT0
R563 *47K_4 SD_DAT1
R558 *47K_4 SD_DAT2
R562 *47K_4 SD_DAT3

Quanta Computer Inc.
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Size	Document Number	Rev
	SDIO CardReader	1A

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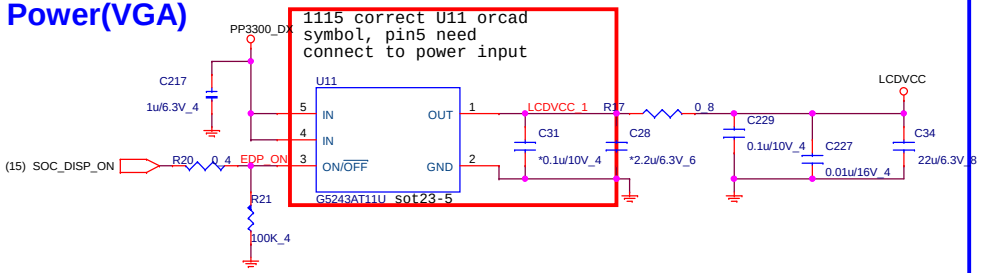
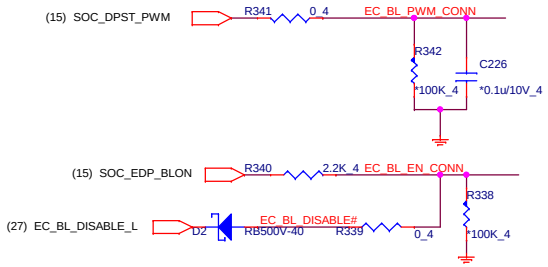
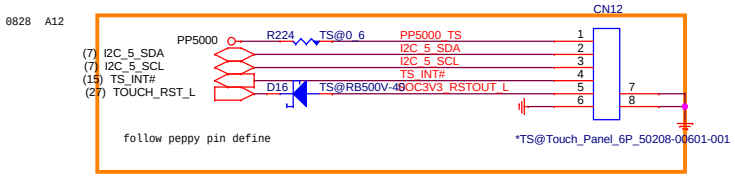
eDP Power(VGA)



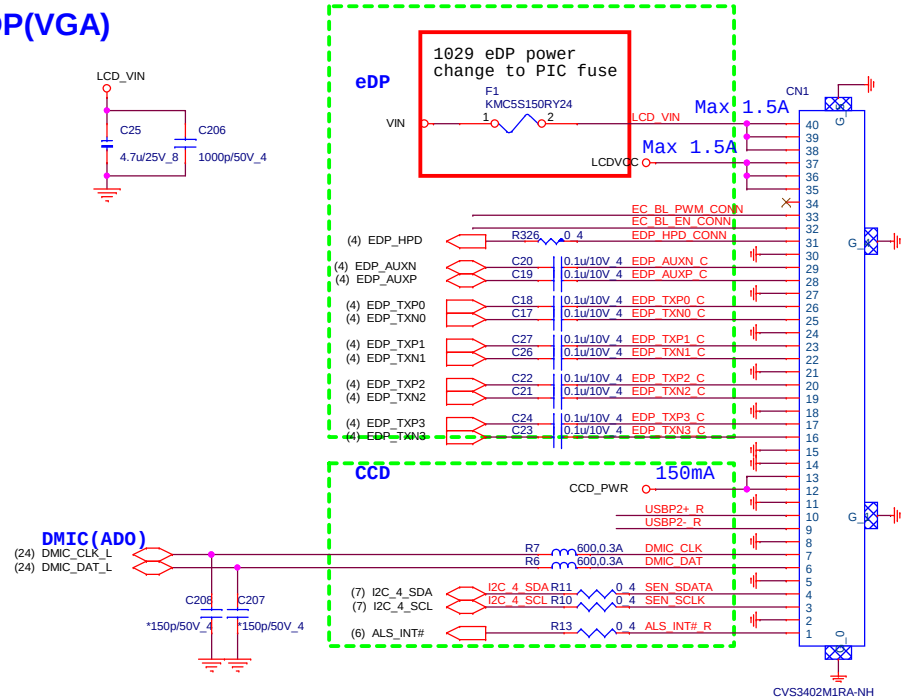
eDP panel control(VGA)



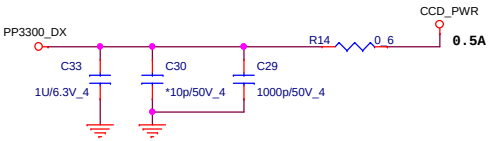
Touch Screen(VGA)



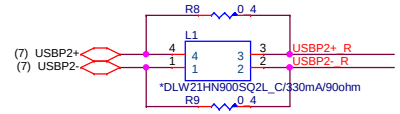
eDP(VGA)



CCD power(CCD)



CCD USB(CCD)



Quanta Computer Inc.

PROJECT : NL6

Size	Document Number	Rev
	LVDS/CCD/DMIC/TS	1A

Date: Friday, February 21, 2014 Sheet 17 of 40

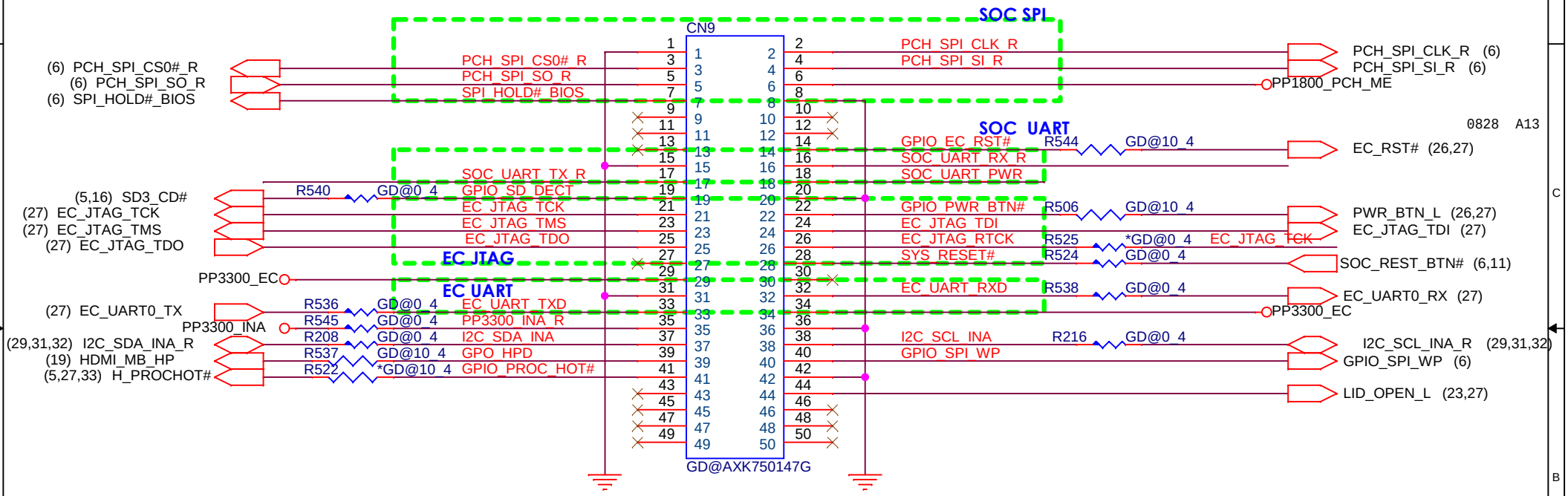
GOOGLE Debug Port(MPC)

50 pin BTB is MUST, don't use 42 pin

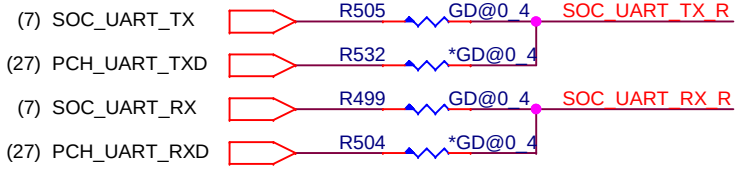
Socket part number AXK750147G

PIN7 OD
PIN14 OD
PIN19 OD
PIN22 OD
PIN28 OD
PIN30 OD
PIN37 OD
PIN38 OD
PIN39 OD
PIN41 OD
PIN43 OD
PIN44 OD
PIN45 OD
PIN46 OD
PIN47 OD
PIN48 OD
PIN49 OD
PIN50 OD

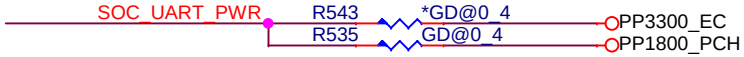
18



1021 change footprint and PN



9/13 add pull up



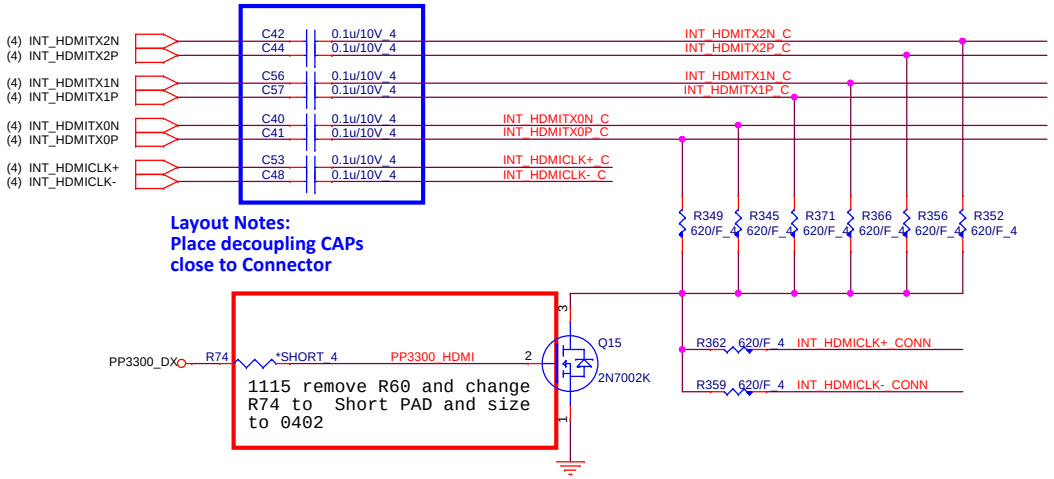
9/6 using optional instead of level shifted, defult is from SoC

Quanta Computer Inc.

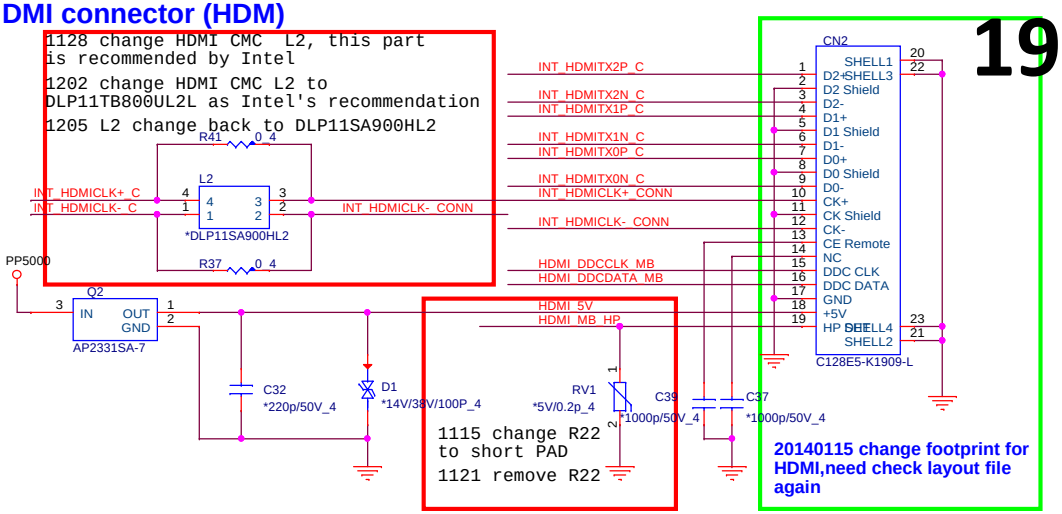
PROJECT : NL6

Size	Document Number	Rev
	Google Debug	1A
Date: Friday, February 21, 2014	Sheet 18 of 40	

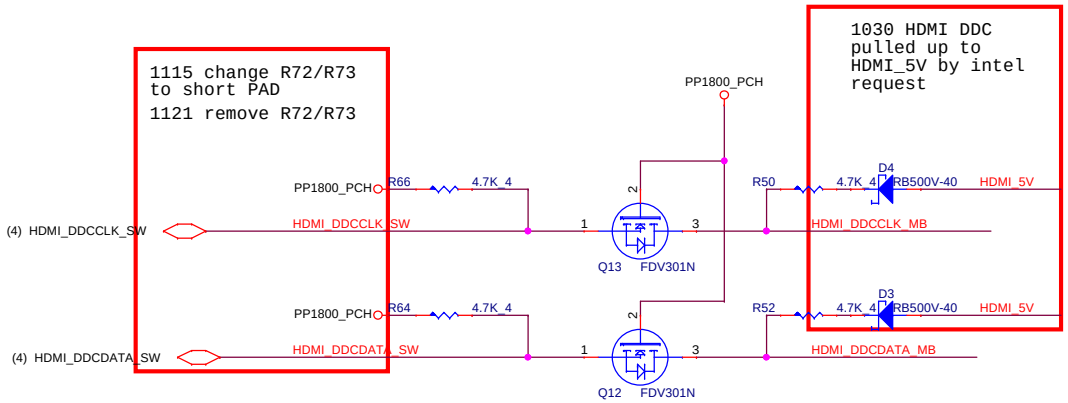
HDMI Cost Reduced level shift (HDM)



HDMI connector (HDM)

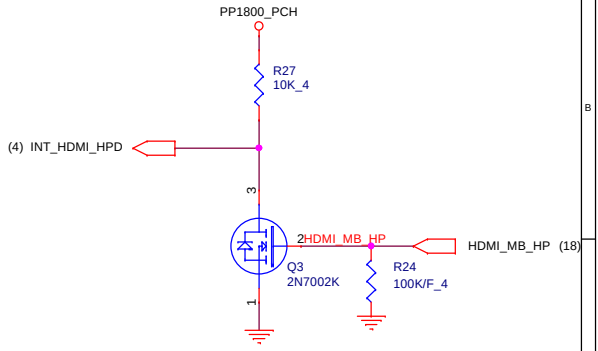


HDMI DDC (HDM)



EMI

HDMI-detect (HDM)



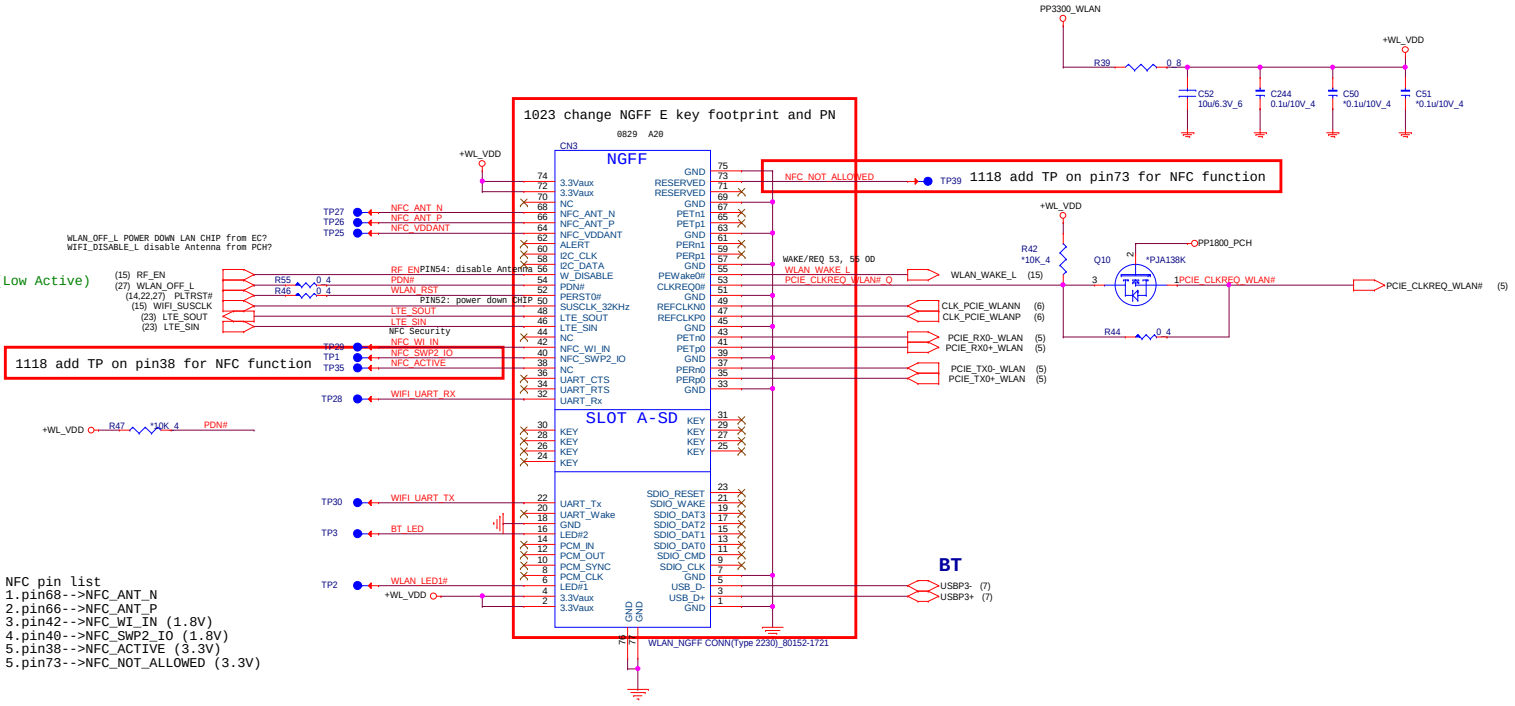
Quanta Computer Inc.

PROJECT : NL6

Size	Document Number	Rev
	HDMI	1A

Date: Friday, February 21, 2014 Sheet 19 of 40

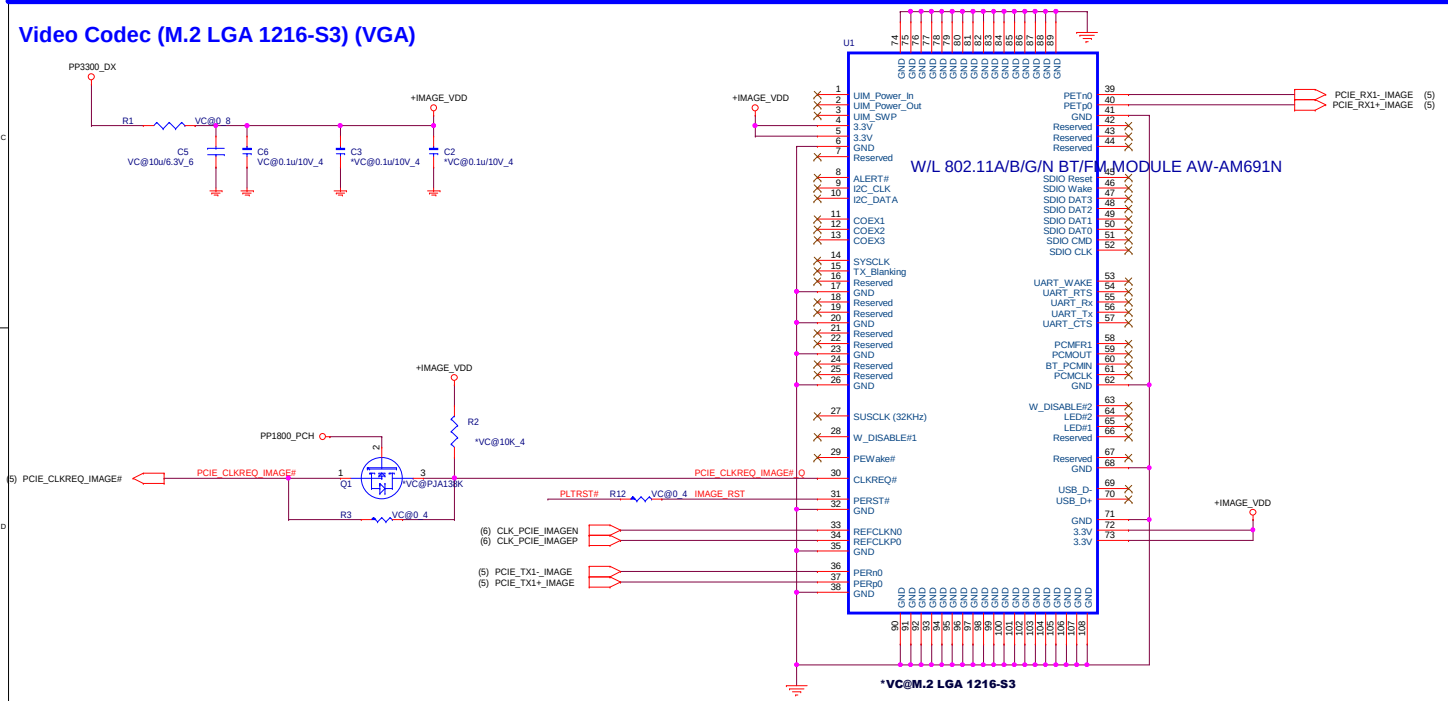
WIFI/BT COMBO (NGFF E KEY)



NFC pin list
1.pin68-->NFC_ANT_N
2.pin66-->NFC_ANT_P
3.pin42-->NFC_WI_IN (1.8V)
4.pin40-->NFC_SWP2_IO (1.8V)
5.pin38-->NFC_ACTIVE (3.3V)
5.pin73-->NFC_NOT_ALLOWED (3.3V)

LTE Coexistence pin list (based on V0.2 spec
1.pin48-->LTE_SOUT (3.3V)
2.pin46-->LTE_SIN (3.3V)

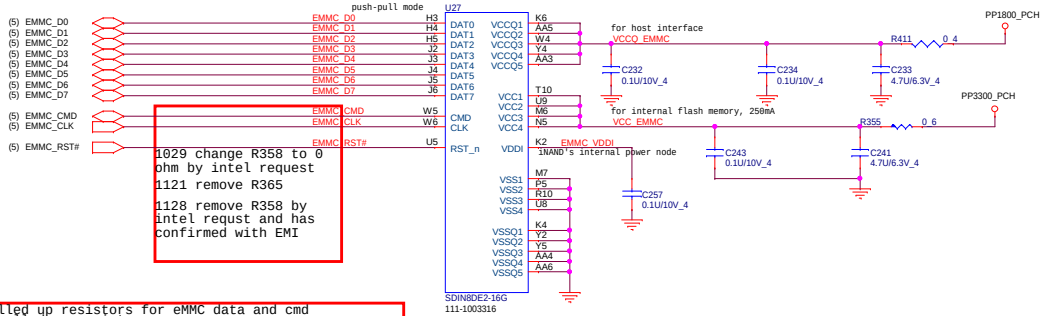
Video Codec (M.2 LGA 1216-S3) (VGA)



Quanta Computer Inc.			
PROJECT : NL6			
Size	Document Number	WIFI / BT / Image Codec	Rev 1A
Date: Friday, February 21, 2014		Sheet 20 of 40	

1025 Delete complete SSD(connector and caps)

EMMC (CBS)



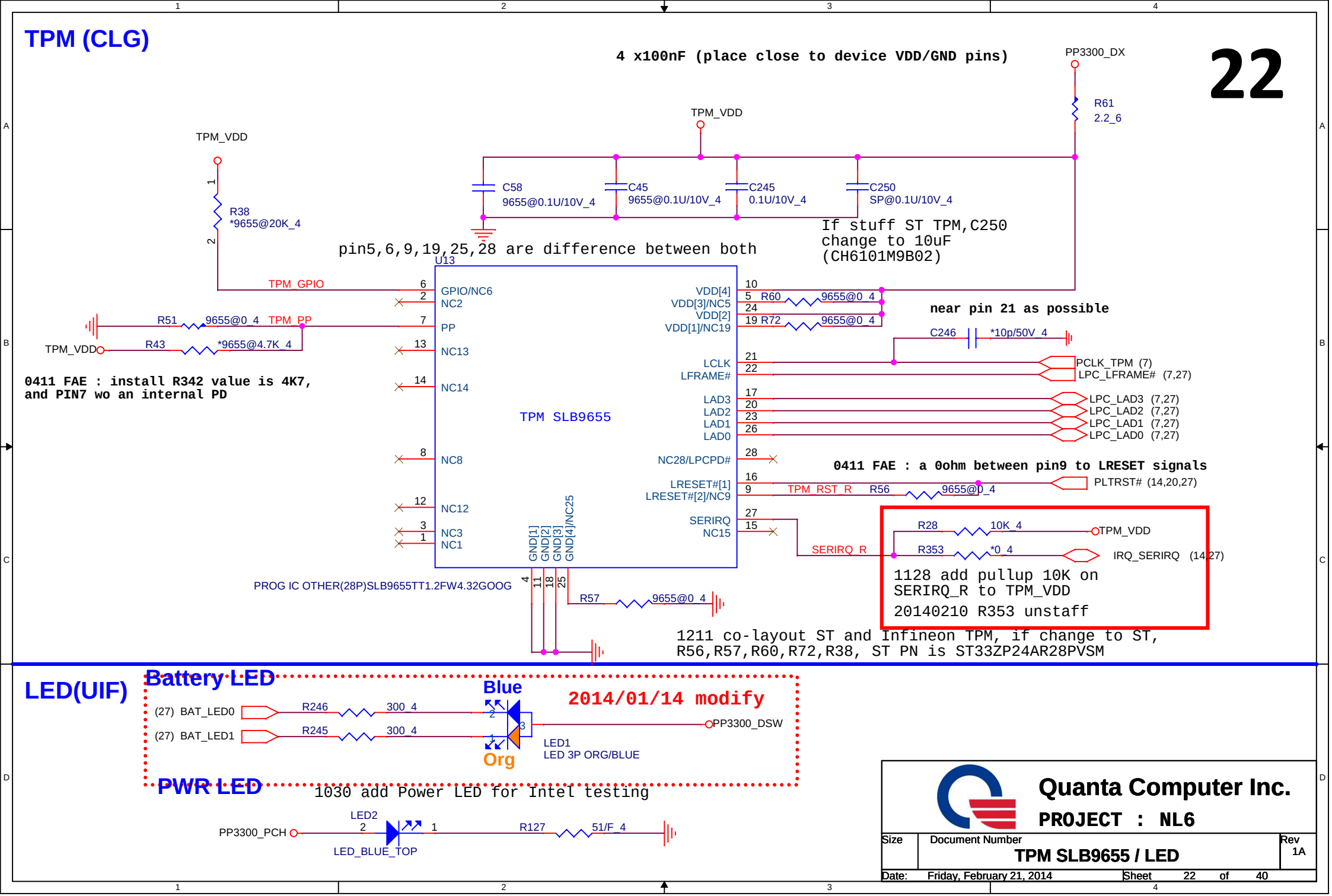
SandisK (16G) 153 pin SDIN8DE2-16G (11.5x13mm) : QPN: AKE3RZ-T101

1029 remove pulled up resistors for eMMC data and cmd
1211 add back pulled up resistors
1212 all Pulled up resistors of eMMC data/cmd to be un-stuffed, and R361 change to 47K ohm as well

Quanta Computer Inc.
PROJECT : NL6

Size	Document Number	Rev
	SSD NGFF/ EMMC	1A
Date: Friday, February 21, 2014	Sheet 21 of 40	

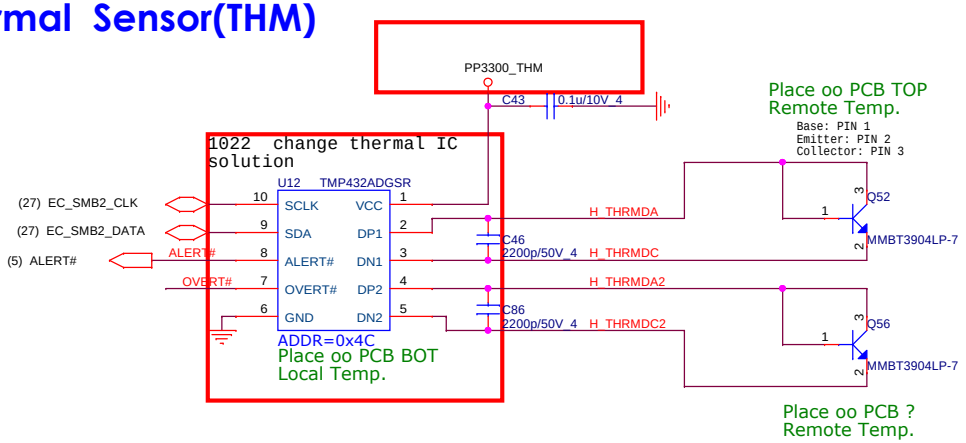
TPM (CLG)



LED(UIF)

Quanta Computer Inc.		
PROJECT : NL6		
Size	Document Number: TPM SLB9655 / LED	Rev: 1A
Date: Friday, February 21, 2014	Sheet 22 of 40	

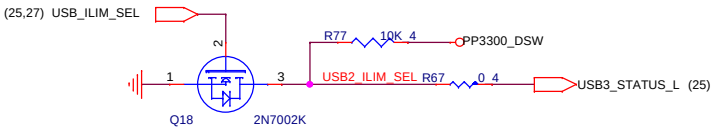
Thermal Sensor(THM)



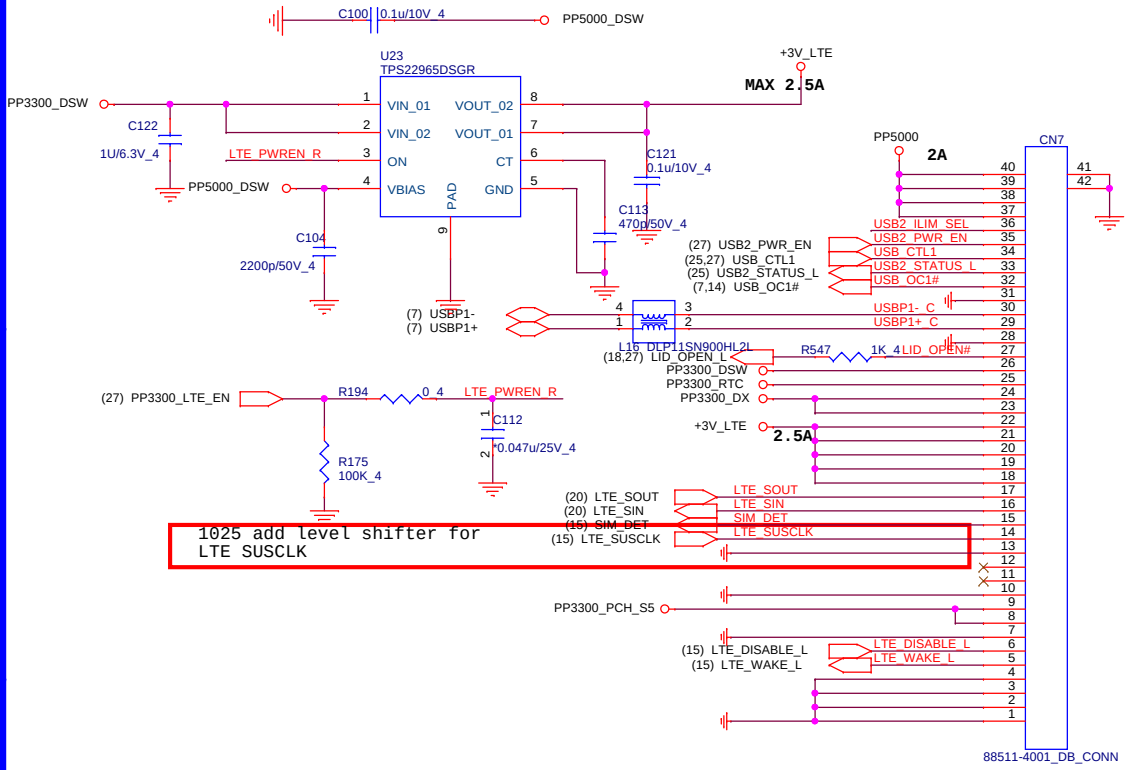
1030 Thermal IC VDD has two option, ome is PP3300_DSW(=PP3300_EC), another is PP3300_DX, default is stuffing to DSW rail

1025 remove Q31 becasue PU to PP3300_DSW at EC side already

USB Switch Current Control



FUNCTION DB
LTE(MNC)



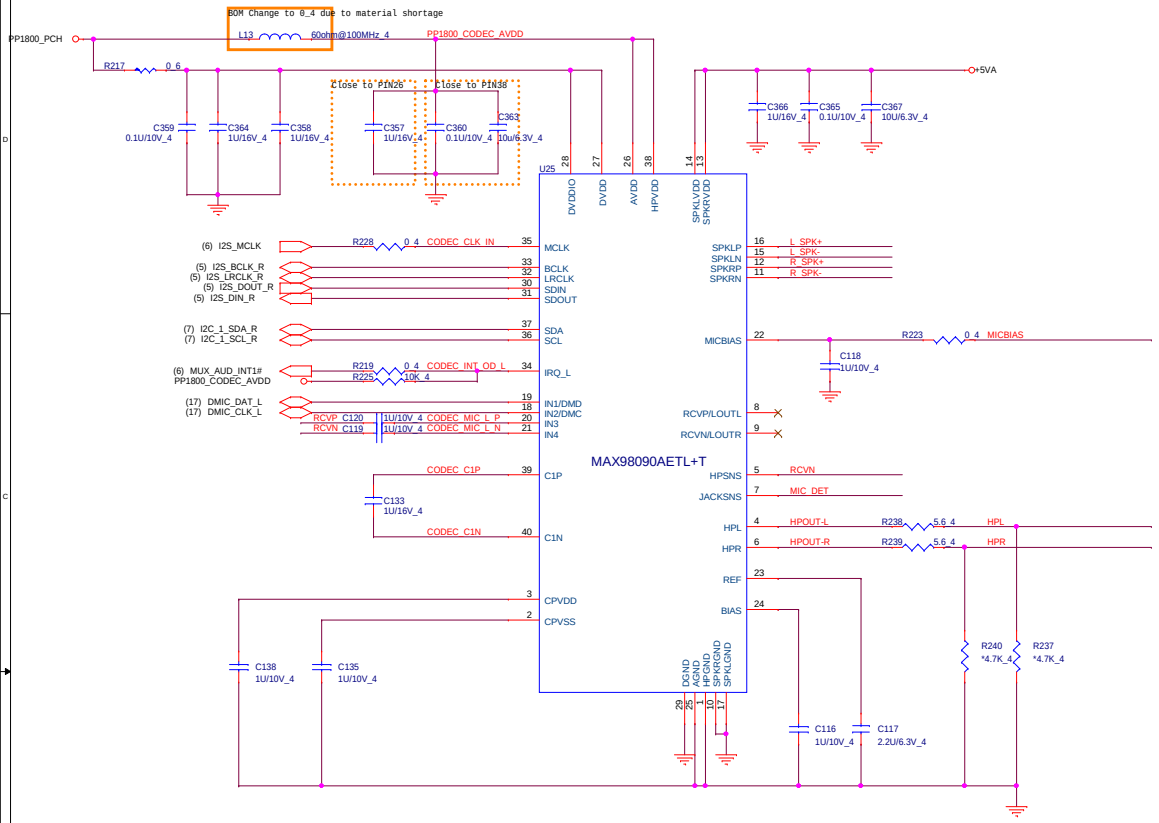
1025 add level shifter for LTE SUSCLK

Quanta Computer Inc.

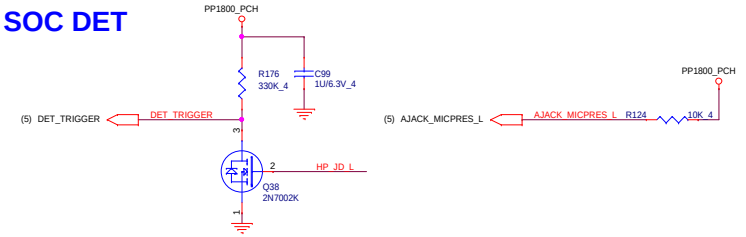
PROJECT : NL6

Size	Document Number	Rev
	DB/ALS/Thermal sensor	1A
Date: Friday, February 21, 2014	Sheet 23 of 40	

AUDIO CODEC (ADO)



SOC DET

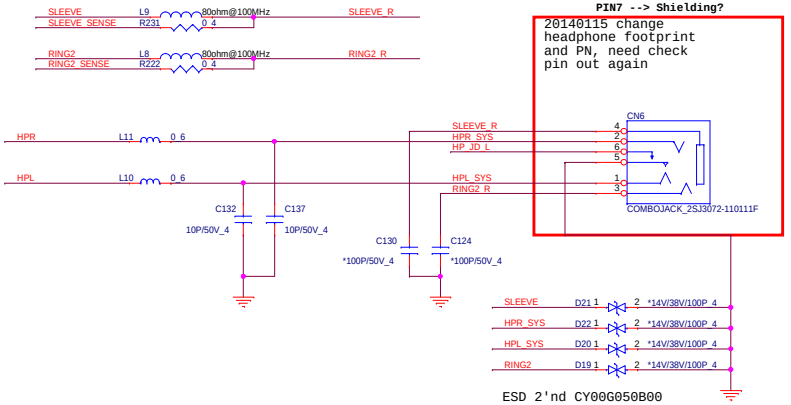


HEADPHONE/Mic combo(ADO)

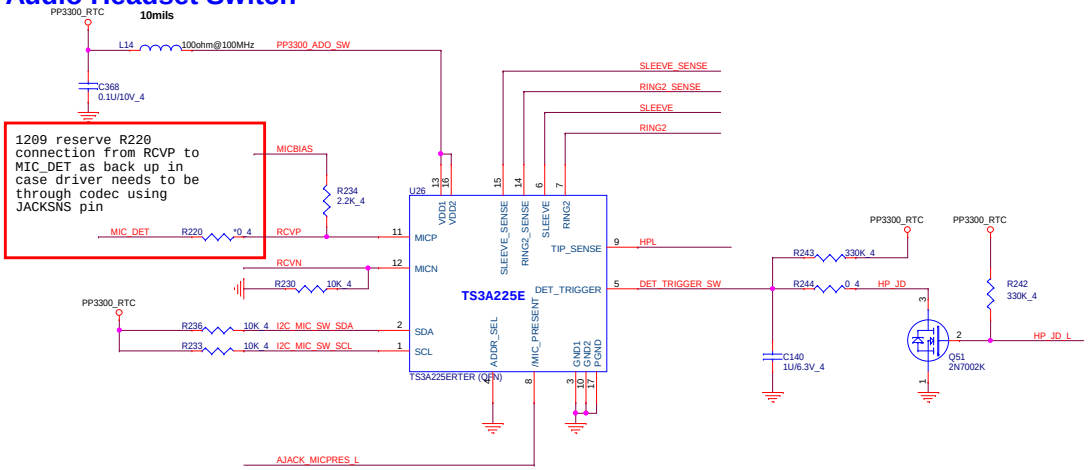
combo jack Normal open

P/N: DFTJ06FR652
Normal Open
PIN1 --> L?
PIN2 --> R?
PIN3 --> GND/MIC?
PIN4 --> MIC/GND?
PIN5 --> JD?
PIN6 --> GND?
PIN7 --> Shielding?

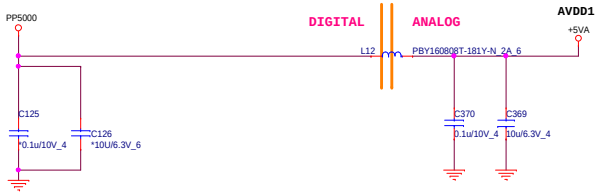
20140115 change headphone footprint and PN, need check pin out again



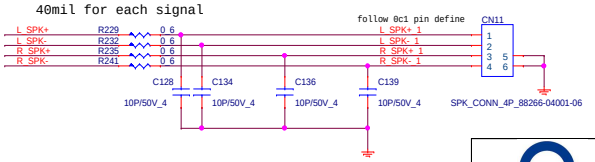
Audio Headset Switch



Codec PWR 5V(ADO)



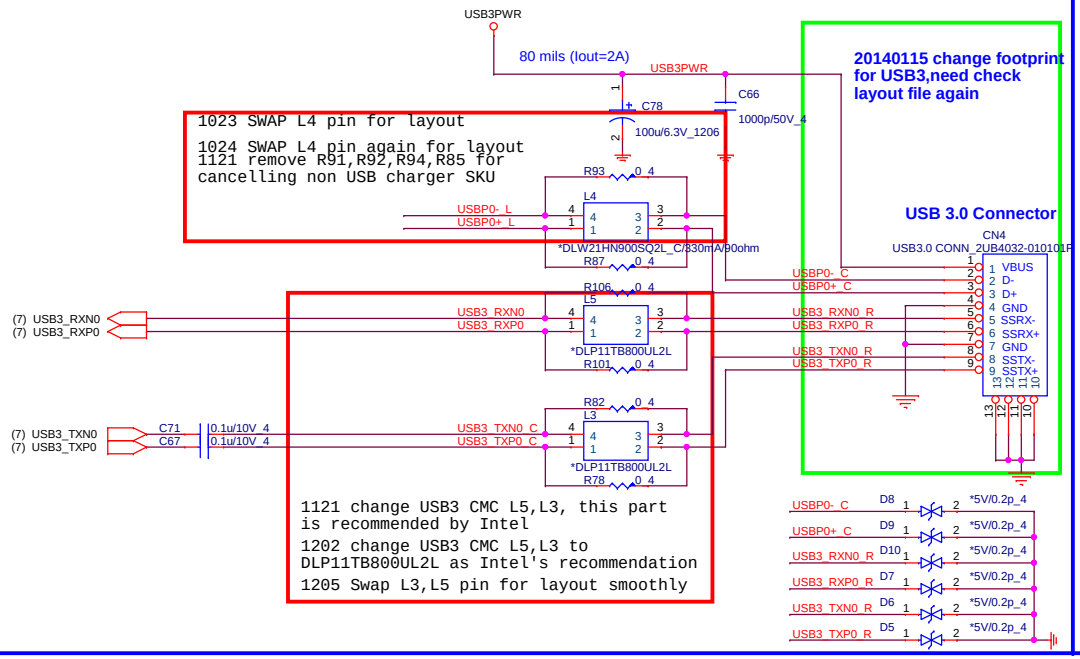
Internal Speaker



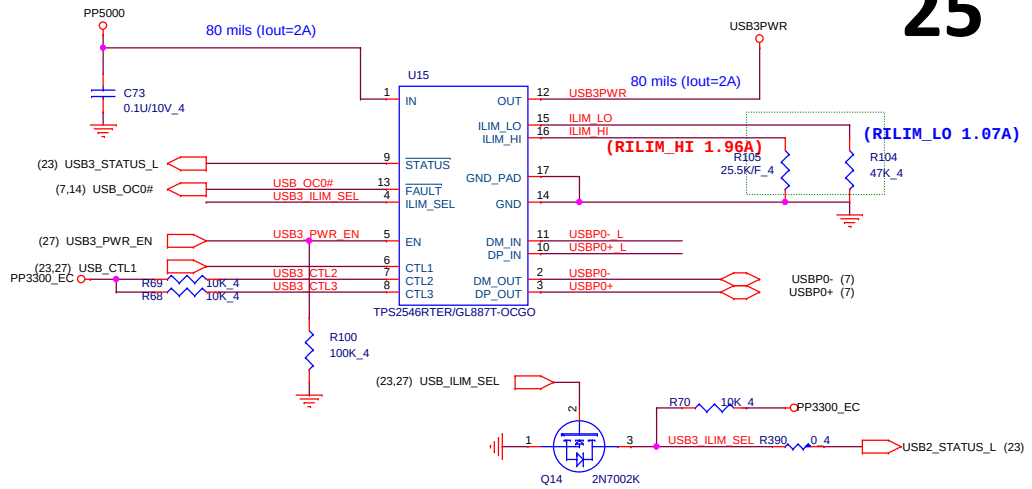
Quanta Computer Inc.
PROJECT : NL6

Size	Document Number	Rev
	MAX98090/HP/SPK	1A
Date: Friday, February 21, 2014	Sheet 24 of 40	

USB3.0(USB)



USB Charger



RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used

If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.

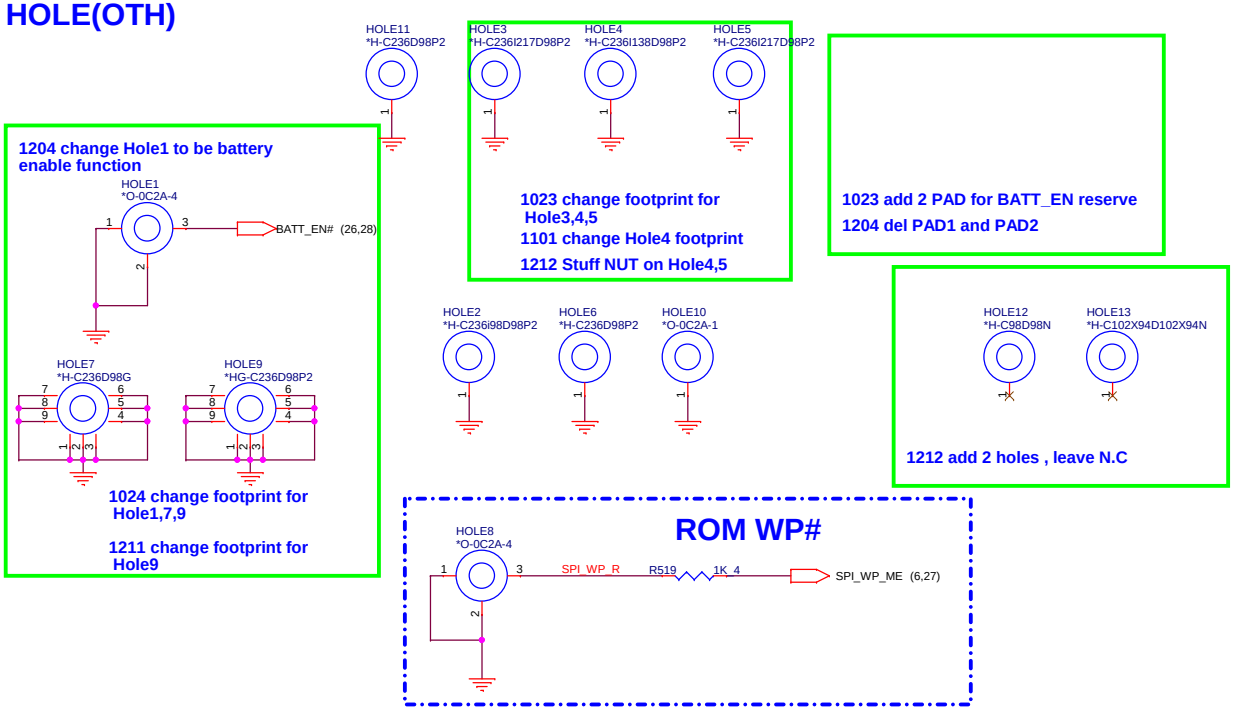
The following equation programs the typical current limit:

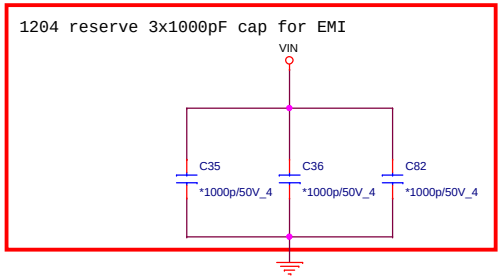
(1)

RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$IOS\_typ(mA) = 50{,}250/\{RILIM\_XX(K\Omega)+0.1\}$$

HOLE(OTH)

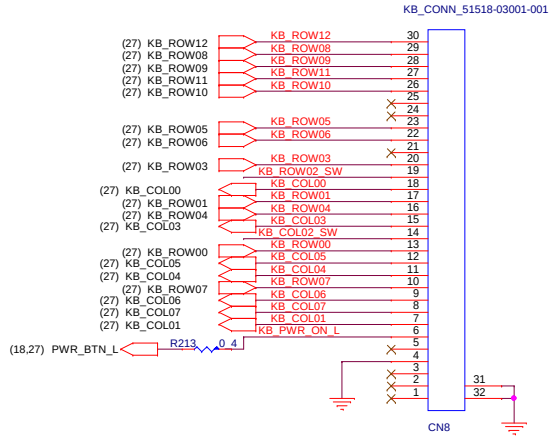


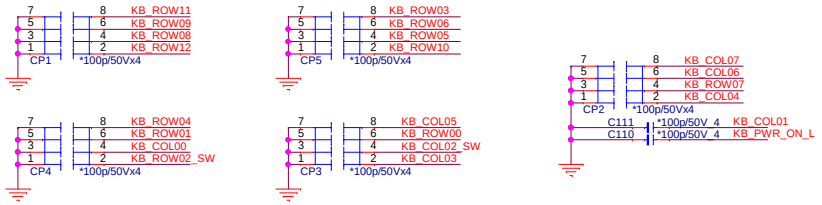


Quanta Computer Inc.		
PROJECT : NL6		
Size	Document Number: USB3/Charger/Hole	Rev: 1A
Date: Friday, February 21, 2014	Sheet 25 of 40	

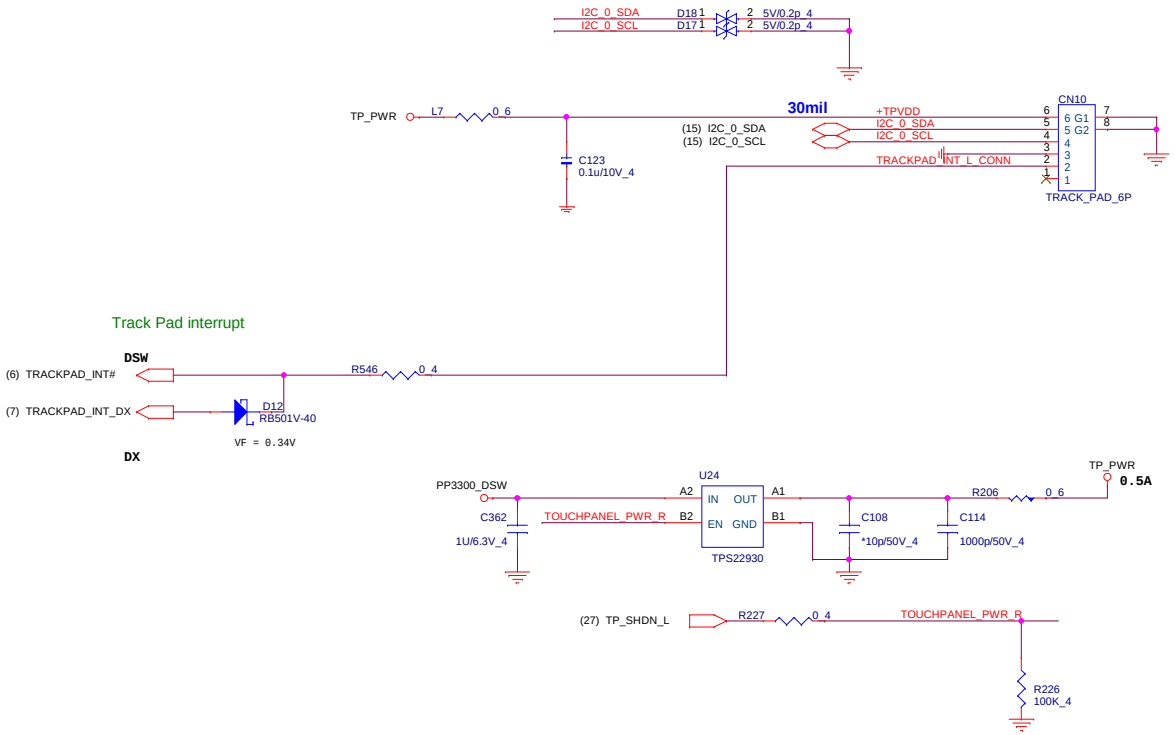
K/B (KBC)

20140127 Change KB CONN for ME require

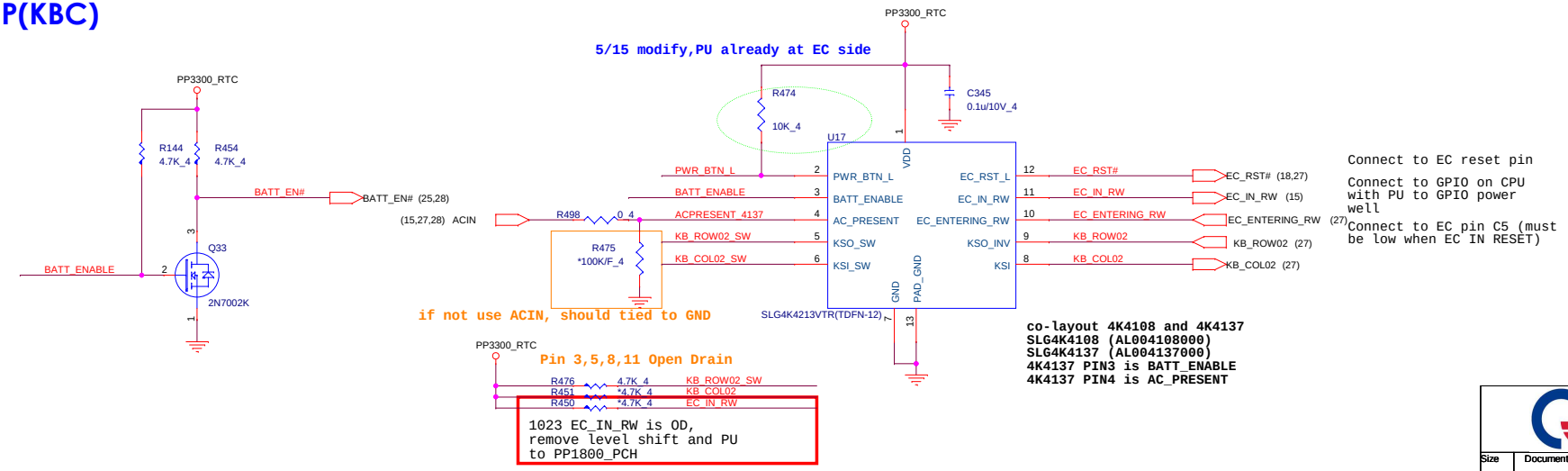




Track PAD BOARD CONN (TPD)



HOLELESS RESET 2-CHIP(KBC)



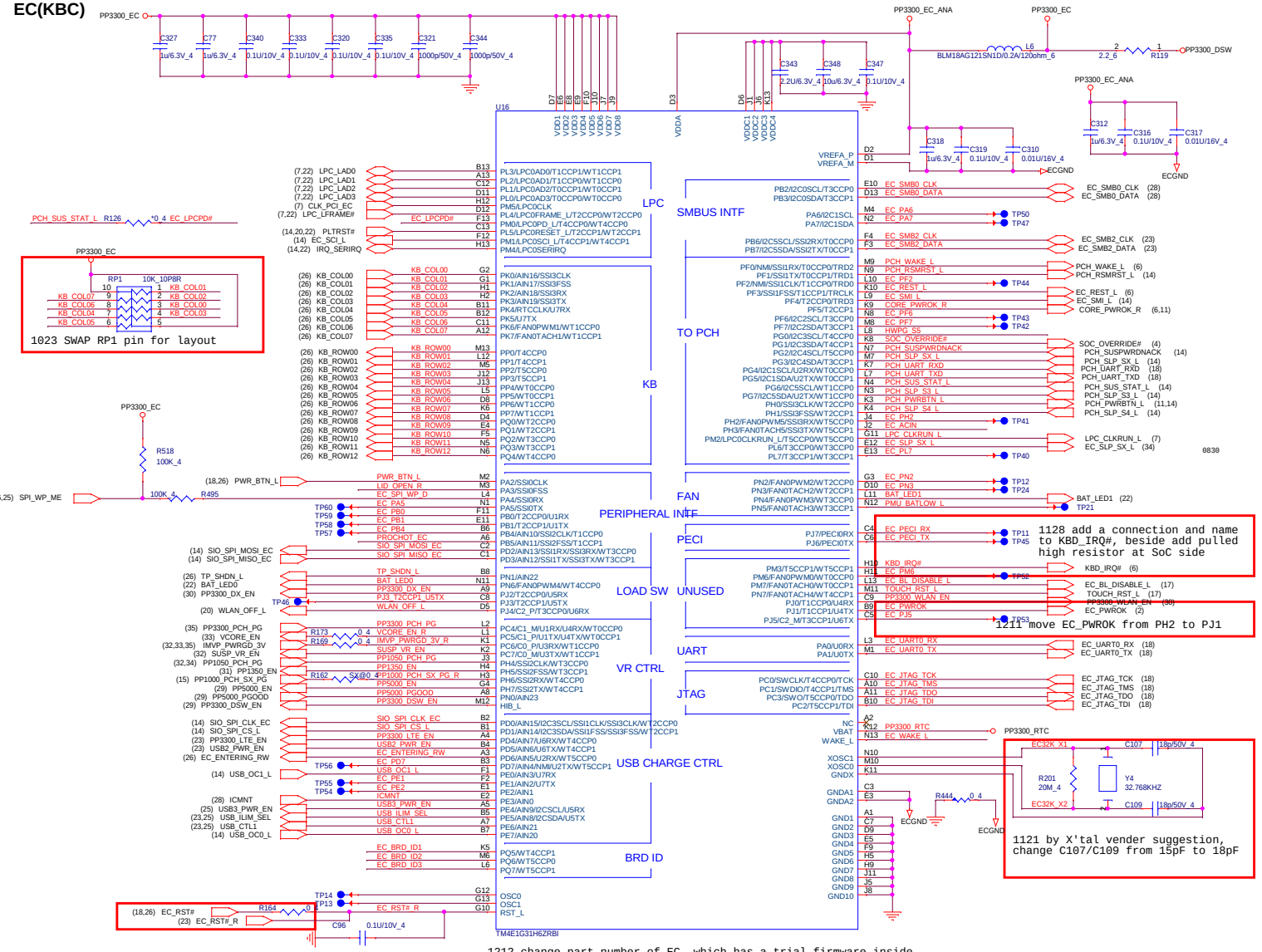
Quanta Computer Inc.

PROJECT : NL6

Size	Document Number	Rev
	KB/TP/FAN/HW Reset	1A

Date: Friday, February 21, 2014 Sheet 26 of 40

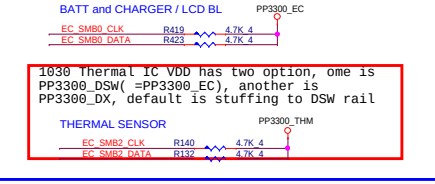
EC(KBC)



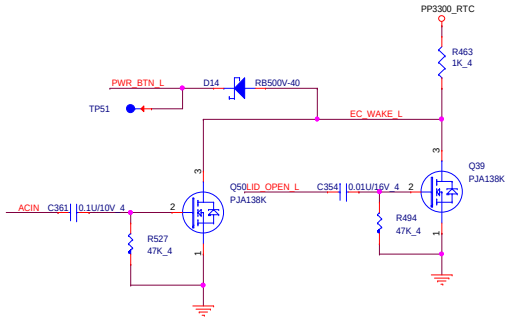
SM BUS ARRANGEMENT TABLE

SM Bus 0	BATT and CHARGER
SM Bus 1	NA
SM Bus 2	THERMAL SENSOR

SM BUS/I2C PU(KBC)



EC HIB WAKE SOURCES

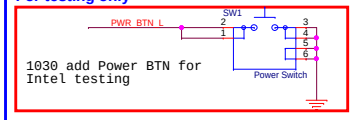


HWPG(KBC)

OD pin list

- EC_REST_L
- BAT_LED0
- BAT_LED1
- PCH_RSMRST_L
- SMBUS
- IRQ_SERIRQ
- EC_BL_DISABLE_L

For testing only

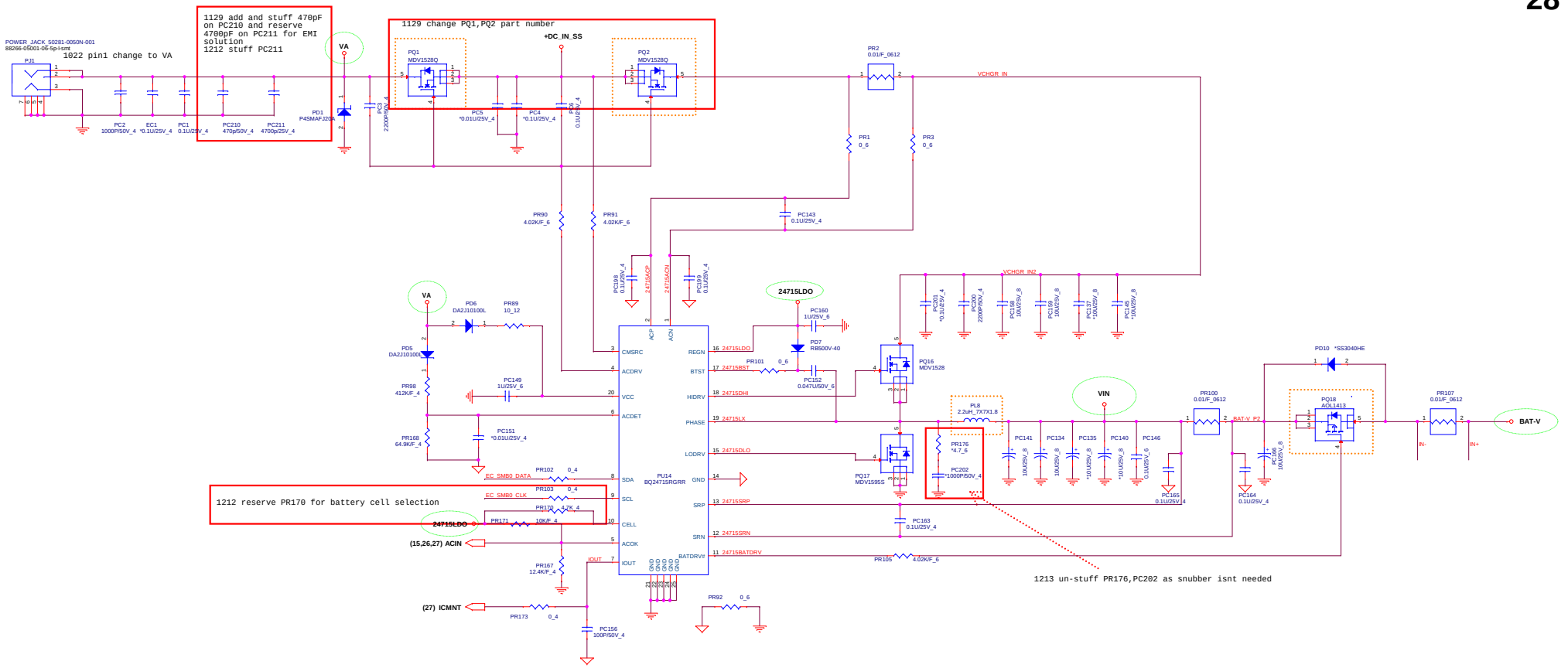


Stage	EC_ID3	EC_ID2	EC_ID1	
Proto1/1.5/2.0	0	0	0	
Proto2.0	0	0	1	

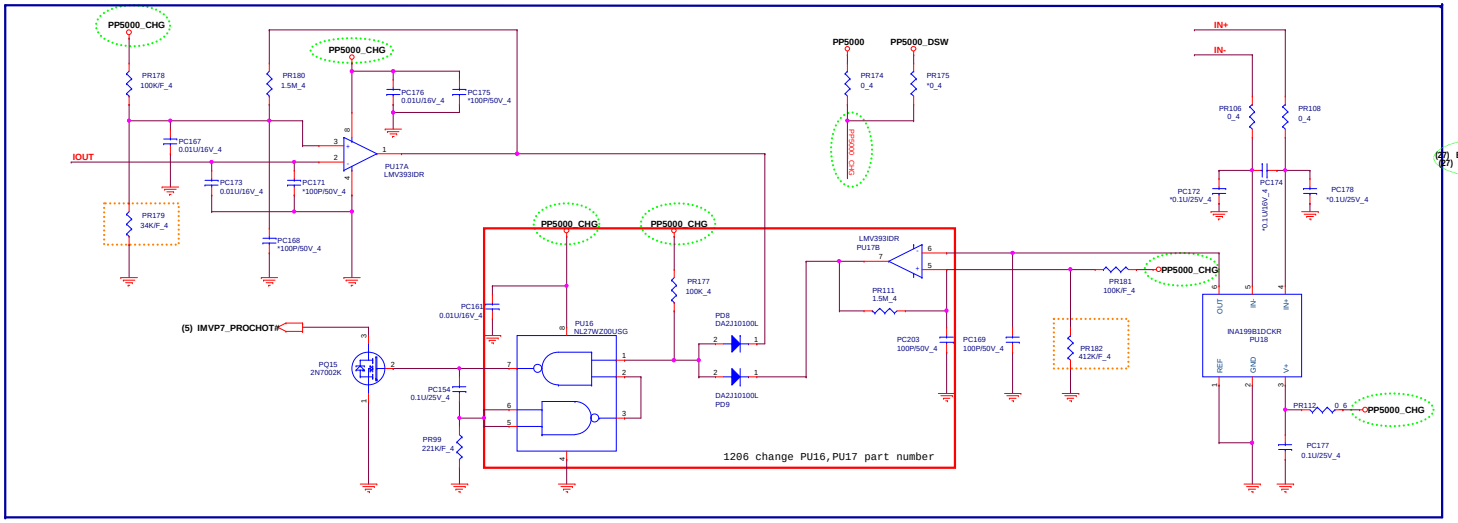
1213 Board ID of proto2 change to 001

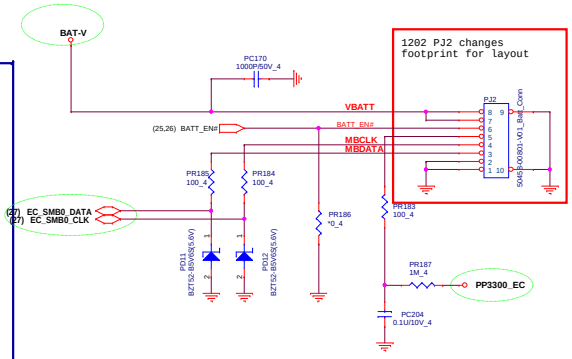
Quanta Computer Inc.
PROJECT : NL6

Size	Document Number	Rev
	KBC TI TM4E1G31H6ZRBI	1A
Date: Monday, February 24, 2014	Sheet 27 of 40	

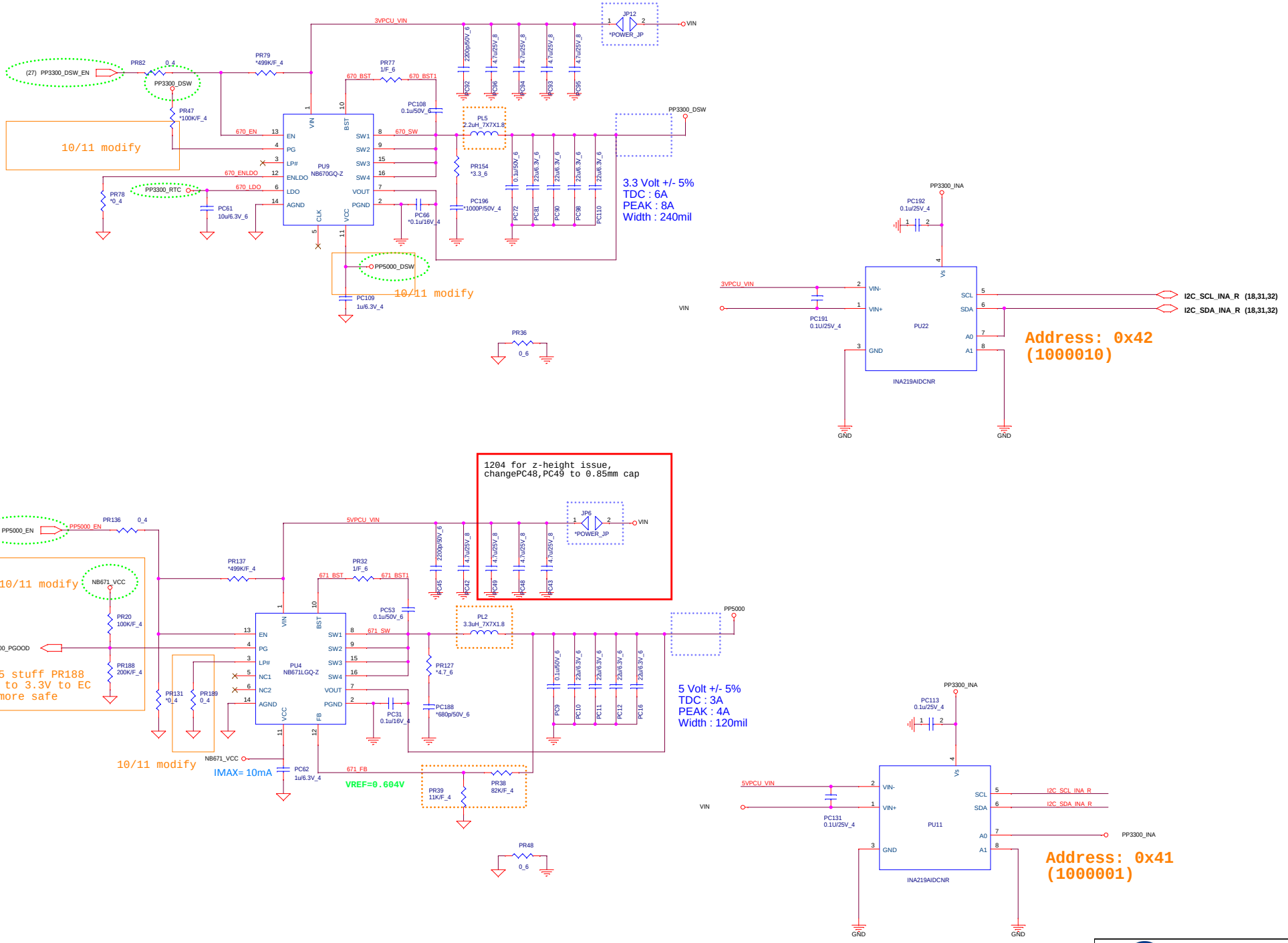


10ms one-shot circuit





Quanta Computer Inc.			
PROJECT : Charger(BQ24715)			
Size	Document Number		Rev 1A
Date: Friday, February 21, 2014	Sheet 28 of 40		



Quanta Computer Inc.		
PROJECT :		
Size	Document Number: SYSTEM 5V/3V (MPS670/671)	Rev: 1A
Date: Friday, February 21, 2014	Sheet 29 of 40	

(35) PP1800_PCH_S5_PG
(27) PP3300_DX_EN

PP1800_PCH_S5_PG
PP3300_DX_EN

PP3300_DSW
PR71 0_8
PP3300_DX
PR63 *0_8
PC82 1u/10V_4

PR60 *0_8
PU6
PP3300_WLAN_R
A2 IN OUT A1
EN GND
B2 B1
PP3300_WLAN
TPS22930
(27) PP3300_WLAN_EN
PP3300_WLAN_EN
PR44 0_4
PP3300_WLAN_EN_R
PR53 100K/F_4
PC63 *0.1u/50V_6

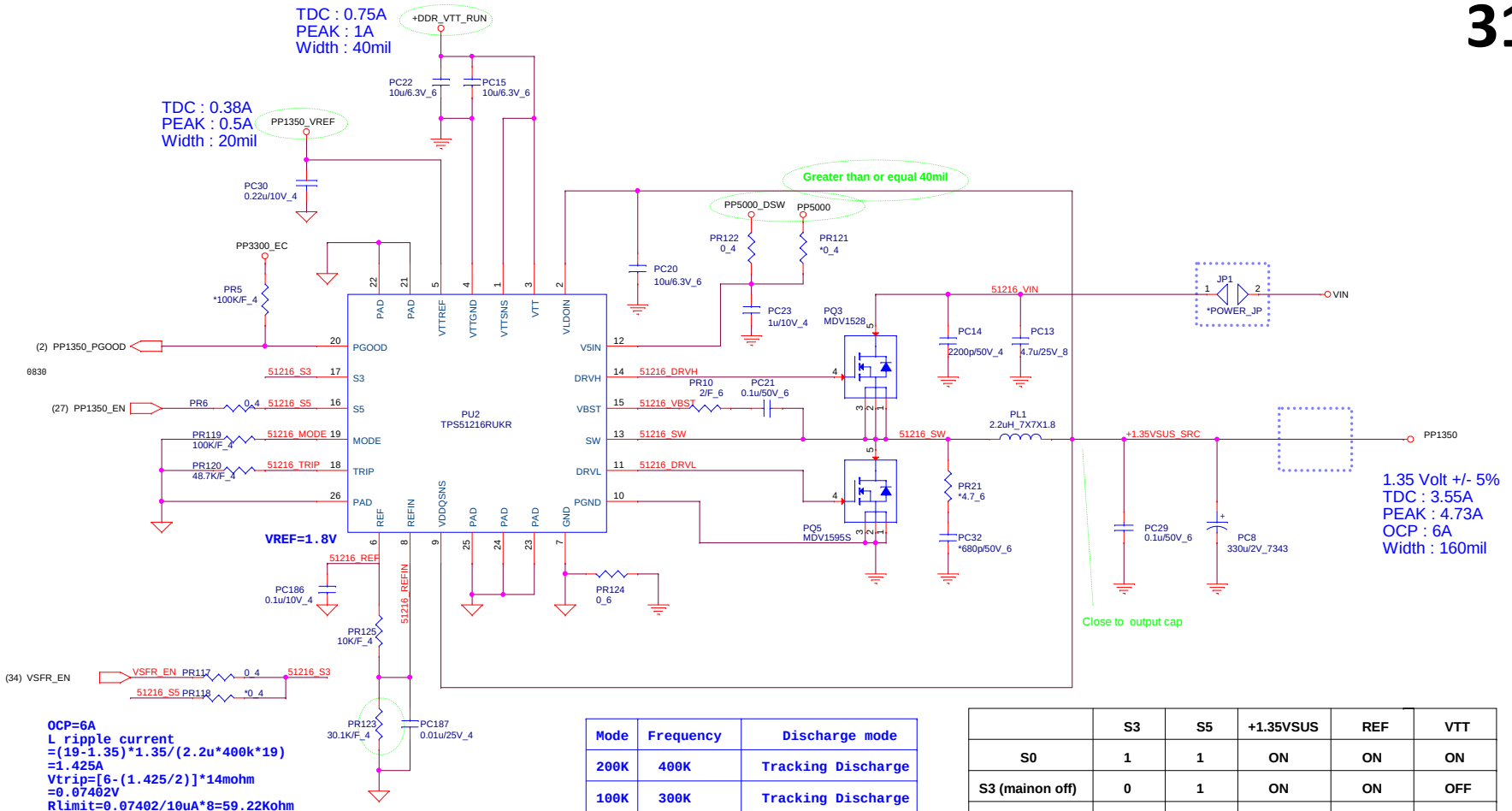
DX should be earlier than VREN by EC.

PP3300_DSW
PC162 1u/10V_4
PU13
A2 IN OUT A1
PP1800_PCH_S5_PG
PR95 0_4
B2 EN GND B1
PR96 *100K/F_4
PC148 *0.1u/50V_6
TPS22930

PP3300_PCH_S5
PP3300_DSW
PC17 1u/10V_4
PU1
A2 IN1 OUT1 A1
B2 IN2 OUT2 B1
PP3300_DX_EN
PR15 0_4
PP3300_DX_EN_R
EN GND C2 C1
PR14 100K/F_4
TPS22964CYZPR
PP3300_DX

Quanta Computer Inc.
PROJECT :

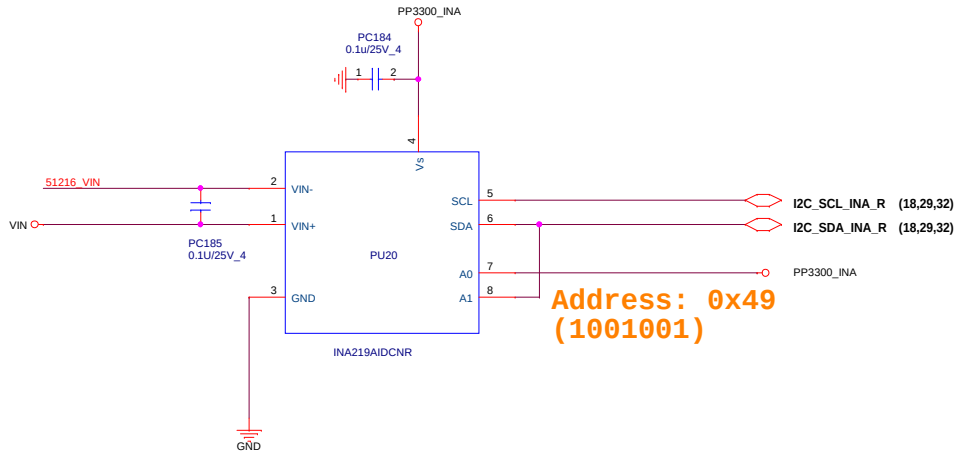
Size	Document Number	Rev
	Load Switch	1A
Date: Friday, February 21, 2014	Sheet 30 of 40	



OCP=6A
L ripple current
=(19-1.35)*1.35/(2.2u*400k*19)
=1.425A
Vtrip=[6-(1.425/2)]*14mohm
=0.07402V
Rlimit=0.07402/10uA*8=59.22Kohm

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



Quanta Computer Inc.	PROJECT :	
Size	Document Number: DDR 1.35V(TPS51216)	Rev 1A
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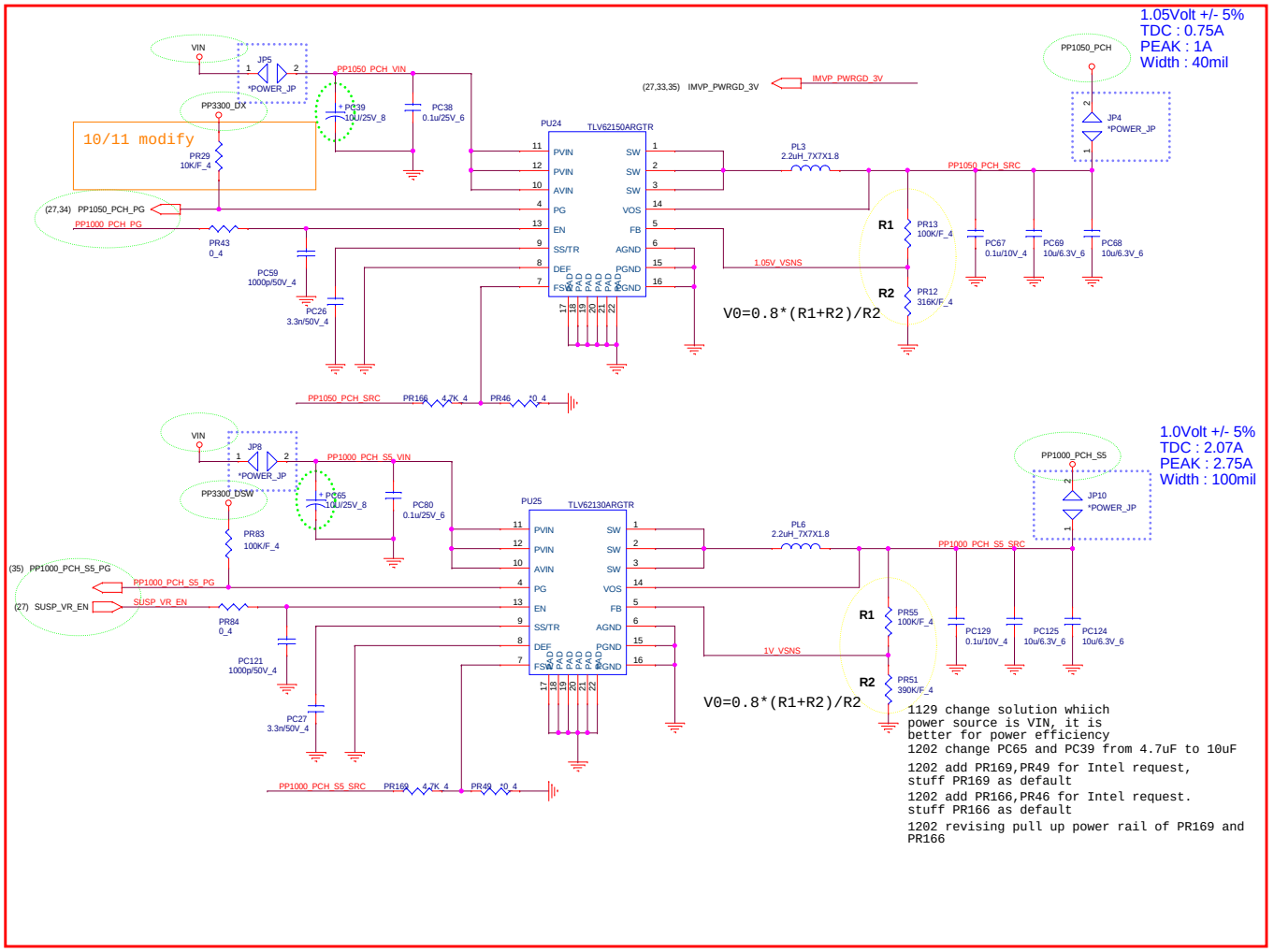
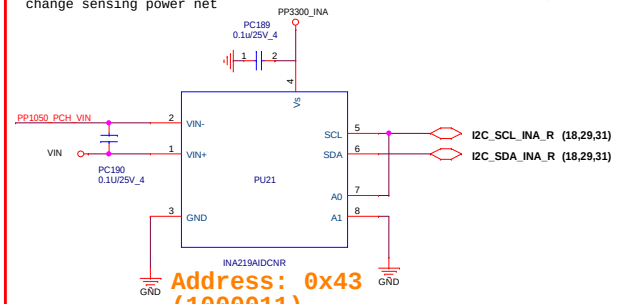
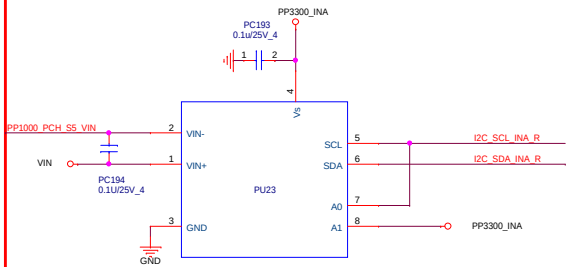
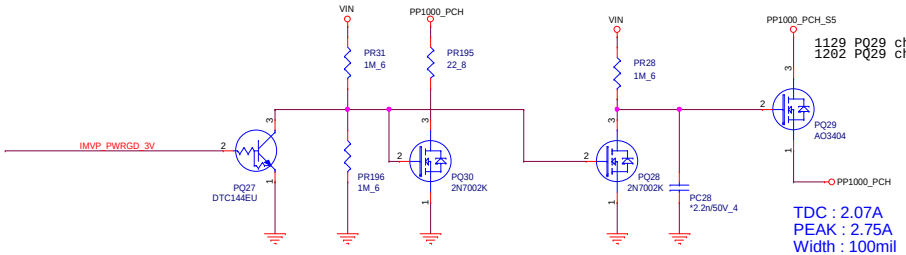
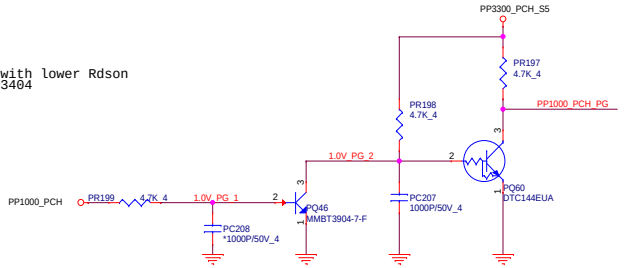


1129 because of power source of PU24,PU25 chagen to VIN, so that need change sensing power net









1129 PP1000_PCH changes from convert to power MOSFET type for power efficiency improvement

Quanta Computer Inc.		
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Size	Document Number: +1.05V/+1V(TPS54318)	Rev: 1A
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1025 PC57 change from 68p to 120p
PC50 change from 150p to 2200p
for proto1 issue

1030 PR26 change to 16.9K
PR23 change 10 ohm
PC50 change 1200pF
PC40 change to 270pF
un-stuff PR22,PC54

1031 un-stuff PR129 and PC37

1115 PR128 change to 1.62K

AXG

1209 remove JP9 for ACLL improvement

+VCC_GFX
PEAK : 14A
OCP : 18A
Width : 600mil

GFX_CORE Load Line : -5.9mV/A for SDP=4.5W

1213 un-stuff PR74,PC104 as snubber isnt needed

Close to the VR side.

Close with AXG inductor

Parallel

Close to the CPU side.

VRON PD 100K AT EC

1031 add 0.1u on PP1000_PCH for power request

1025 PR155 change from 300 to 340 ohm for proto1 issue

Core

1209 remove JP13 for ACLL improvement

+VCC_CORE
PEAK : 12A
OCP : 18A
Width : 500mil

VCORE Load Line : -5.9mV/A for SDP=4.5W

1213 un-stuff PR81,PC115 as snubber isnt needed

Close to the VR side.

1025 PC99 change from 68p to 120p
PC106 change from 150p to 2200p
for proto1 issue

1030 PR76 change to 16.9K
PR86 change 10 ohm
PC106 change 1200pF
PC114 change to 270pF
un-stuff PR80,PC101
1031 un-stuff PR158 and PC118

Parallel

Close to the CPU side.

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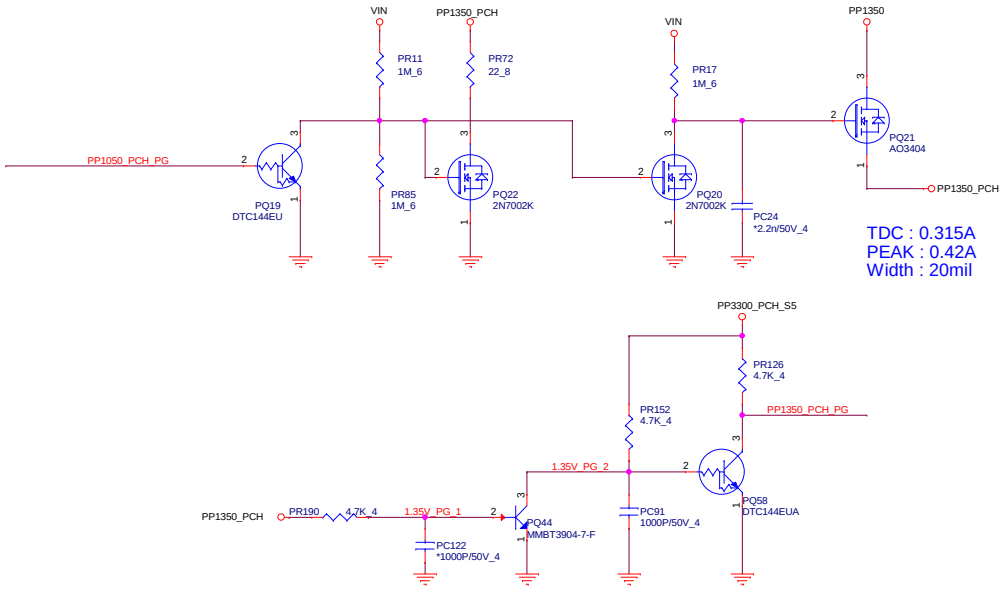
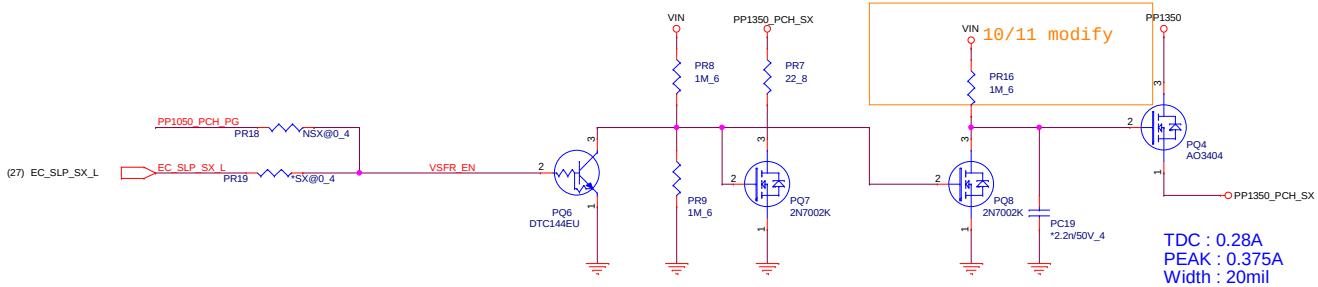
1129 PP1000_PCH_S5 change from LDO to switching power



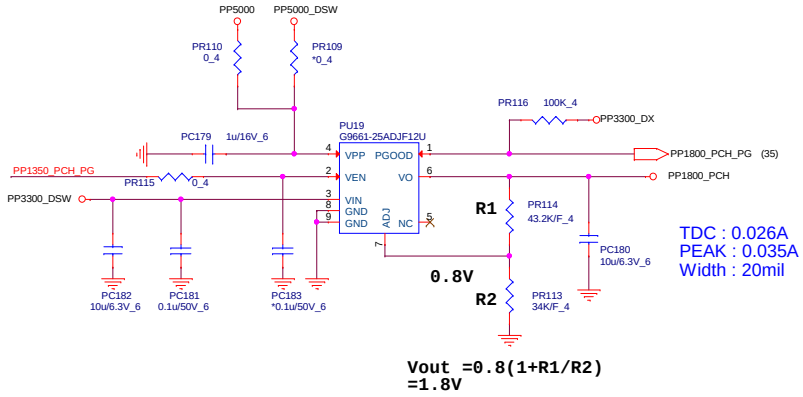
1129 PP1350_PCH change from LDO to power MOSFET



(31) VSFR_EN — VSFR_EN

(27,32) SUSP_VR_EN

(27,32) PP1050_PCH_PG



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PROJECT :		
Size	Document Number: LDO (1V/1.35V/1.5V/1.8V)	Rev: 1A
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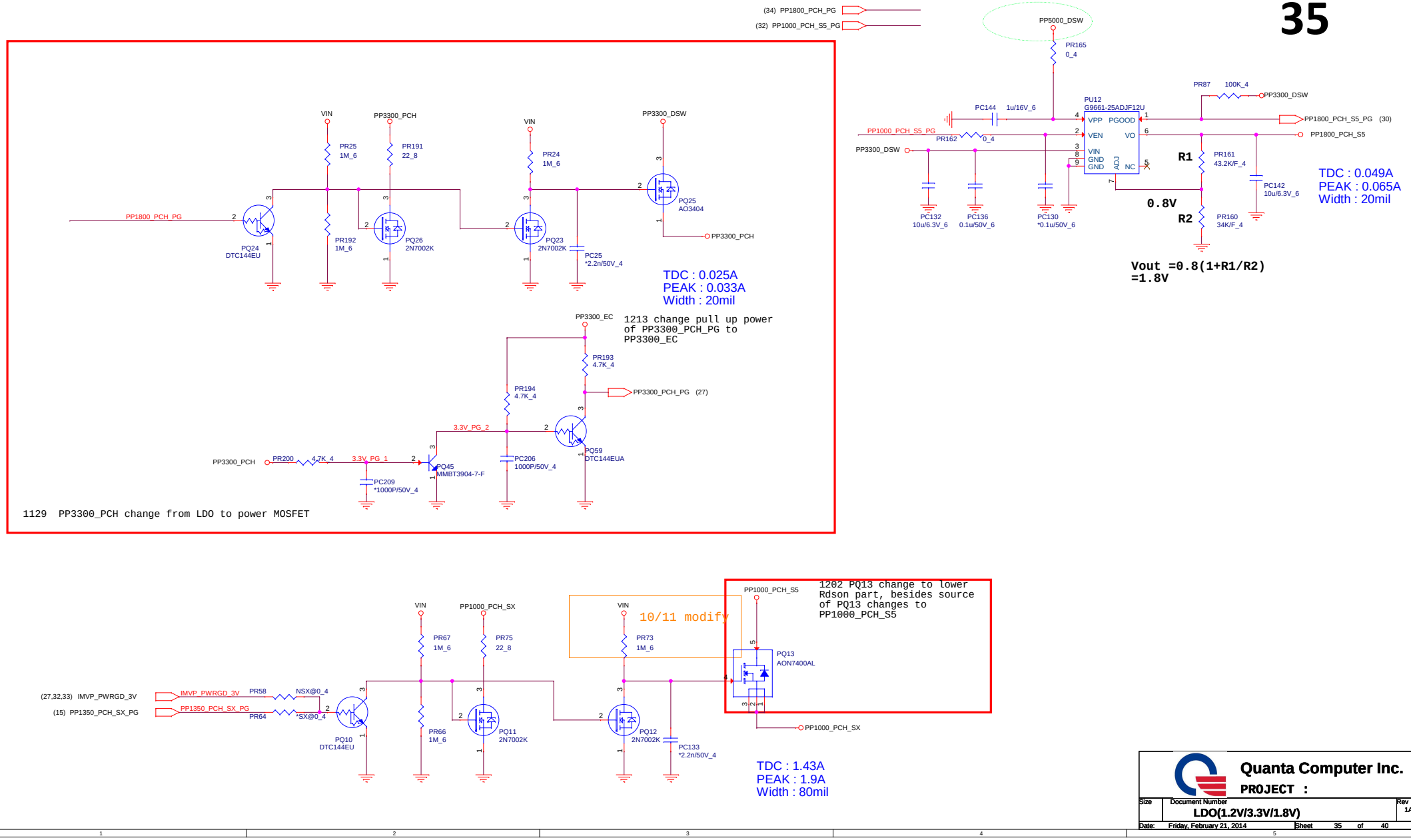

Quanta Computer Inc.		
PROJECT :		
Size	Document Number	Rev
	LDO(1.2V/3.3V/1.8V)	1A
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Quanta Computer Inc.			
PROJECT :			
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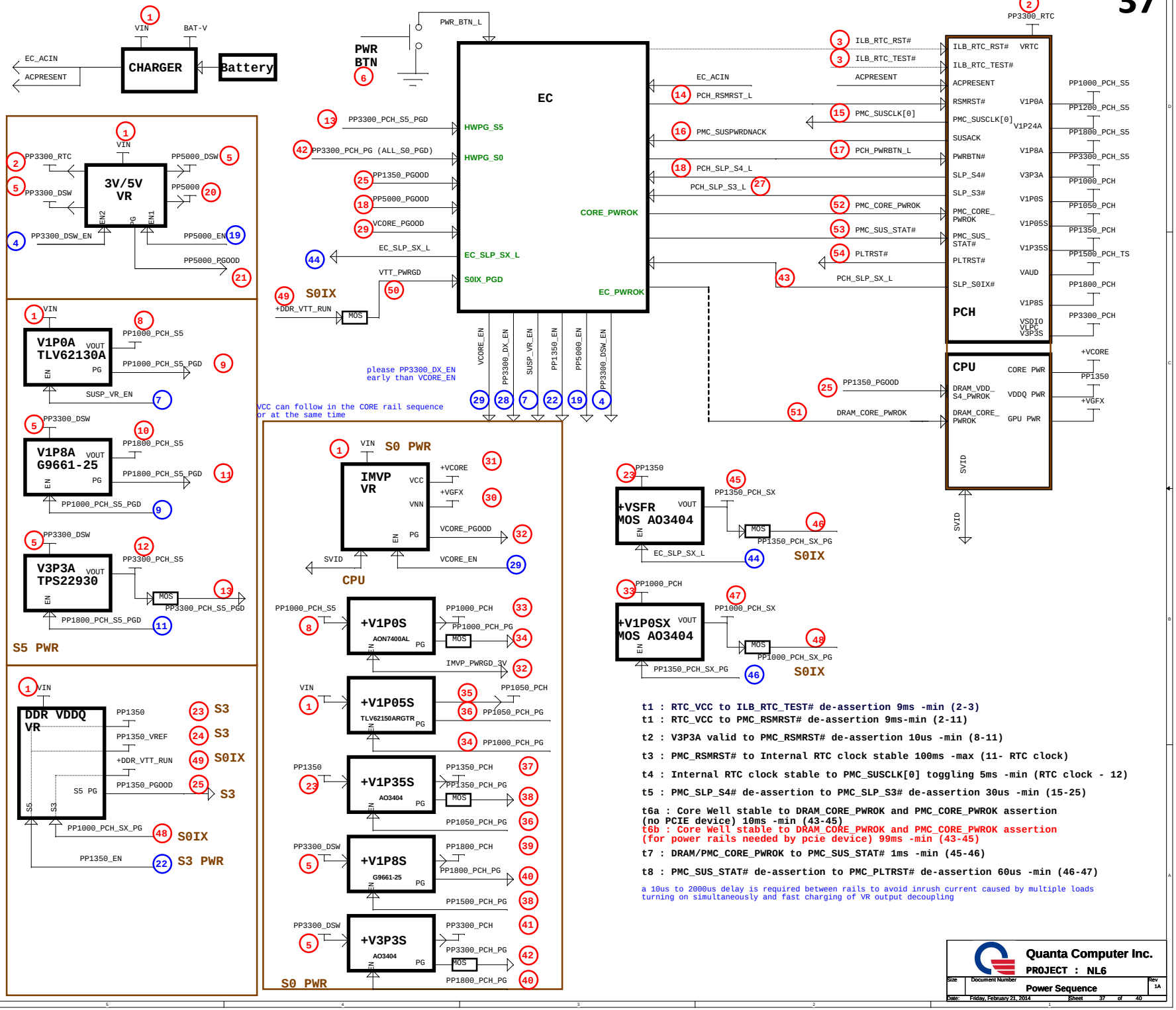
Support S0iX



t1 : RTC_VCC to ILB_RTC_TEST# de-assertion 9ms -min (2-3)
t1 : RTC_VCC to PMC_RSMRST# de-assertion 9ms-min (2-11)

t2 : V3P3A valid to PMC_RSMRST# de-assertion 10us -min (8-11)

t3 : PMC_RSMRST# to Internal RTC clock stable 100ms -max (11- RTC clock)

t4 : Internal RTC clock stable to PMC_SUSCLK[0] toggling 5ms -min (RTC clock - 12)

t5 : PMC_SLP_S4# de-assertion to PMC_SLP_S3# de-assertion 30us -min (15-25)

t6a : Core Well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion (no PCIE device) 10ms -min (43-45)
t6b : Core Well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion (for power rails needed by pcie device) 99ms -min (43-45)

t7 : DRAM/PMC_CORE_PWROK to PMC_SUS_STAT# 1ms -min (45-46)

t8 : PMC_SUS_STAT# de-assertion to PMC_PLTRST# de-assertion 60us -min (46-47)

a 10us to 2000us delay is required between rails to avoid inrush current caused by multiple loads turning on simultaneously and fast charging of VR output decoupling

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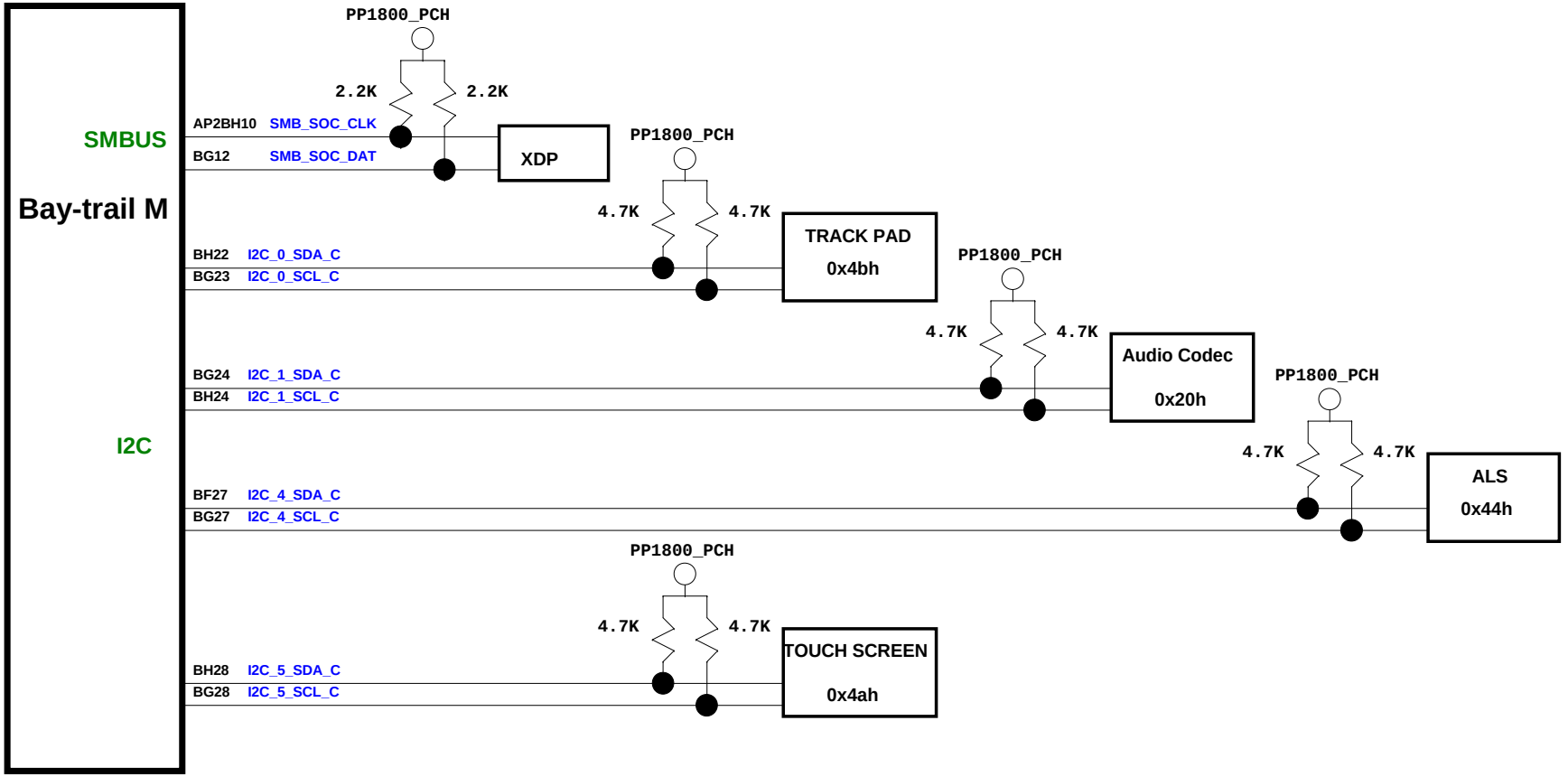

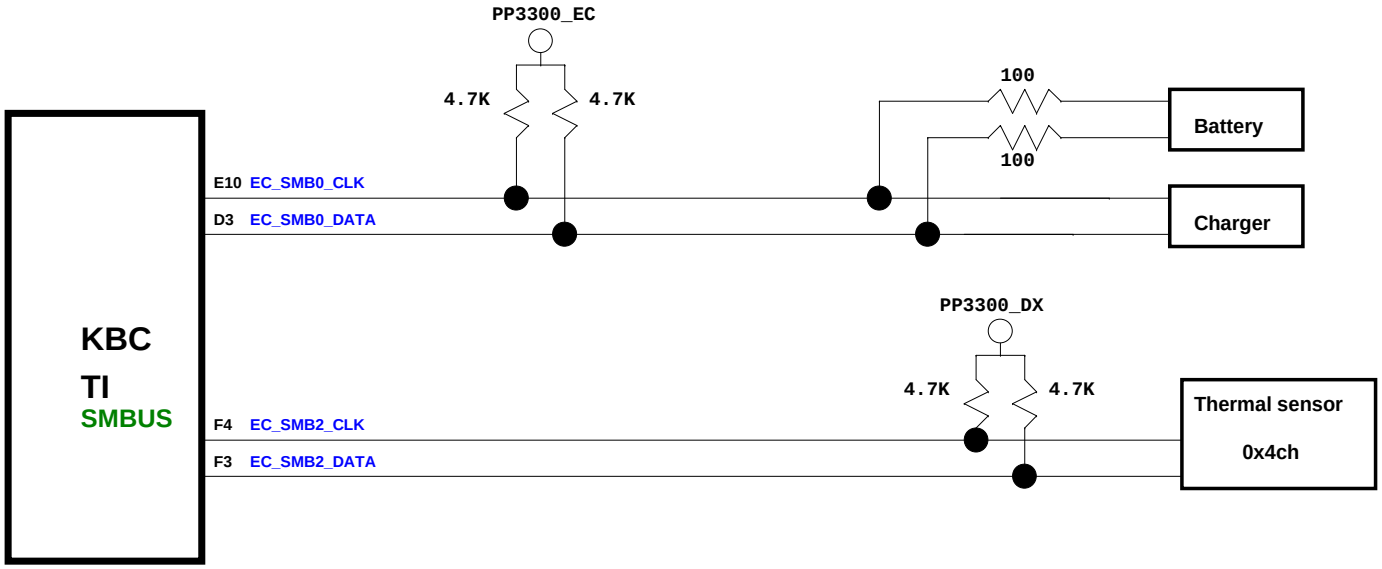

Quanta Computer Inc.
PROJECT : NL6

Size	Document Number	Rev
	SMBUS_I2C	1A

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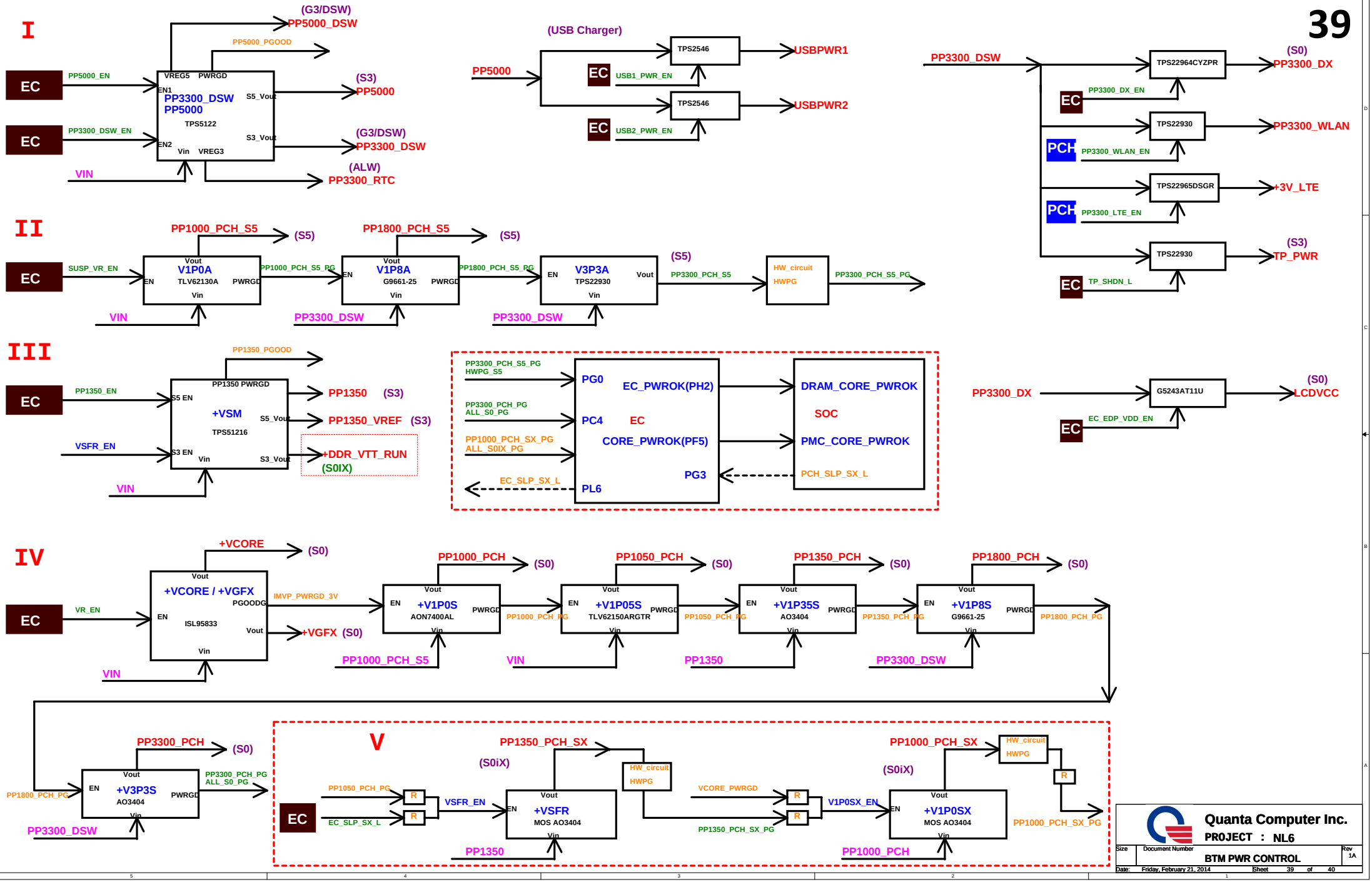
I
(G3/DSW)
PP5000_DSW
PP5000_PGOOD
EC
PP5000_EN
VREG5 PWRGD
EN1
PP3300_DSW
PP5000
S5_Vout
(S3)
PP5000
TPS5122
EC
PP3300_DSW_EN
S3_Vout
(G3/DSW)
PP3300_DSW
EN2
Vin VREG3
VIN
(ALW)
PP3300_RTC
(USB Charger)
PP5000
EC
TPS2546
USB1_PWR_EN
USBPWR1
TPS2546
EC
USB2_PWR_EN
USBPWR2
PP3300_DSW
(S0)
TPS22964CYZPR
PP3300_DX
EC
PP3300_DX_EN
TPS22930
PP3300_WLAN
PCH
PP3300_WLAN_EN
TPS22965DSGR
+3V_LTE
PCH
PP3300_LTE_EN
(S3)
TPS22930
TP_PWR
EC
TP_SHDN_L
II
PP1000_PCH_S5
(S5)
PP1800_PCH_S5
(S5)
EC
SUSP_VR_EN
Vout
V1P0A
TLV62130A
EN
PWRGD
Vin
PP1000_PCH_S5_PG
Vout
V1P8A
G9661-25
EN
PWRGD
Vin
PP1800_PCH_S5_PG
EN
V3P3A
TPS22930
Vout
Vin
(S5)
PP3300_PCH_S5
HW_circuit
HWPG
PP3300_PCH_S5_PG
VIN
PP3300_DSW
PP3300_DSW
III
PP1350_PGOOD
EC
PP1350_EN
PP1350 PWRGD
S5 EN
+VSM
TPS51216
S5_Vout
PP1350
(S3)
PP1350_VREF
(S3)
VSFR_EN
S3 EN
Vin
S3_Vout
+DDR_VTT_RUN
(S0iX)
VIN
PP3300_PCH_S5_PG
HWPG_S5
PG0
EC_PWROK(PH2)
DRAM_CORE_PWROK
PP3300_PCH_PG
ALL_S0_PG
PC4
EC
SOC
PP1000_PCH_SX_PG
ALL_S0iX_PG
CORE_PWROK(PF5)
PMC_CORE_PWROK
PG3
PCH_SLP_SX_L
EC_SLP_SX_L
PL6
PP3300_DX
G5243AT11U
(S0)
LCDVCC
EC
EC_EDP_VDD_EN
IV
+VCORE
(S0)
EC
VR_EN
Vout
+VCORE / +VGFX
PGOODG
EN
ISL95833
Vout
IMVP_PWRGD_3V
+VGFX
(S0)
Vin
VIN
PP1000_PCH
(S0)
Vout
EN
+V1P0S
AON7400AL
PWRGD
Vin
PP1000_PCH_PG
PP1000_PCH_S5
PP1050_PCH
(S0)
Vout
EN
+V1P05S
TLV62150ARGTR
PWRGD
Vin
PP1050_PCH_PG
VIN
PP1350_PCH
(S0)
Vout
EN
+V1P35S
AO3404
PWRGD
Vin
PP1350_PCH_PG
PP1350
PP1800_PCH
(S0)
Vout
EN
+V1P8S
G9661-25
PWRGD
Vin
PP1800_PCH_PG
PP3300_DSW
PP3300_PCH
(S0)
Vout
EN
+V3P3S
AO3404
PWRGD
Vin
PP3300_PCH_PG
ALL_S0_PG
PP1800_PCH_PG
PP3300_DSW
V
PP1350_PCH_SX
(S0iX)
EC
PP1050_PCH_PG
R
R
EC_SLP_SX_L
VSFR_EN
Vout
EN
+VSFR
MOS AO3404
Vin
HW_circuit
HWPG
PP1350
VCORE_PWRGD
R
R
PP1350_PCH_SX_PG
V1P0SX_EN
Vout
EN
+V1P0SX
MOS AO3404
Vin
PP1000_PCH
PP1000_PCH_SX
(S0iX)
HW_circuit
HWPG
R
PP1000_PCH_SX_PG
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BTM PWR CONTROL
Rev
1A
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10/11
001 Change PU9 VCC, CL4, PG (Page 29)
002 Change PU4 VCC, PG (Page 29)
003 Change PR29 from 100K/F_4 to 10K/F_4 (Page 32)
004 Remove 15V, PR57. Mount PR56 (Page 34)
005 Remove 15V, PR72. Mount PR73 (Page 35)
10/14
006 Change U11 LVDS power switch footprint to sot23-5 (Page 17)
007 Unstuff PR198 due to PP5060_PGOOD (PWR) is 5V tolerant input pin (Page 29)
10/16
008 Change PJ1 from DFP20H8807 to DFHD09H8089 (Page 28)
10/17
009 Change C126 from "10U/6.3V_8 to "10U/6.3V_6 due to height limit (Page 24)
010 Change USB3.0 ESD D8,D9 route (Page 24)
011 Change R384 from 0_4 to 0_8, remove R275,R277. Merge UNCORE_V1P35_S0IX_A, UNCORE_V1P35_S0IX_B & UNCORE_V1P35_S0IX (Page 9)
012 Change R354 from 0_4 to 0_0, remove R357. Merge CORE_V1P05_S3_PW, & CORE_V1P05. They are of the same power state and rail (Page 9)

10/19
013 Correct BIOS Strap, mount R128 and dismount R434 (Page 4)
014 Add RSSI 0_4, connect U12 pin 6 ALERT# to H_PROCHOT# (Page 5, 23)
015 Change Y2 from 80J3270B224 to 80J3270B311 due to height limit, change C91,C92 from 18pF to 15pF (Page 6)
016 Add RSSA,RSSG 0_6 option S0 & S5 for PCU_V1P8_G3_V25 (Page 9)
017 Change R469, EC_RST# 0 pull up from PP3300_DX to PP3300_DSW (Page 23)
018 Swap L4 vertically (Page 25)
019 Change PJ1 (Page 28)
Change PD1 from BCMA122A280 to BCAF120A280 (Page 28)
10/21
020 un-stuff RSS3 (Page 5)
021 change SG1 debug# footprint and PN(Page 18)
022 change footprint and PN for HDMI (Page 19)
023 change footprint and PN for USB3(Page 25)
024 change footprint for hole3,4,5,7 and add hole11(Page 25)

10/22
025 un-stuff R182 for S5 leakage issue (Page 14)
026 change thermal IC (Page 23)
027 P31 pin1 change to VA (Page 28)

10/23
028 unstuff R28 by Intel reques (Page 2)
029 unstuff R29 by Intel reques (Page 2)
030 RAM ID strap pin resistor change to 1K, would be stronger (Page 7)
031 change cap C238 from 6.2pF to 3.3pF (Page 12)
032 change cap C228 from 6.2pF to 3.3pF (Page 13)
033 EC_IN_RW is OD,remove level shift and PU to PP3300_PCH (Page 15,26)
034 change NGFF E key footprint and PN (Page 20)
035 change footprint for hole3,4,5 and add 2 PAD for BATT_EN reserve (Page 25)
036 SWAP L4 pin for layout (Page 25)
037 SWAP RP1 pin for layout (Page 27)

10/24

038 change M_A_DQ7S PU to VTTby Intel request (Page 12)
039 change M_B_DQ7S PU to VTTby Intel request (Page 13)
040 correct schematic for R459 PU power rail (Page 23)
041 SWAP L4 pin again for layout (Page 25)
042 change footprint for hole1,7,9 (Page 25)
10/25
043 Delete complete SSD(connector and caps), unstuff R215 and add test points on SATA signals (Page 5,15,21)
044 SSD3 add LTE SSDCLK feature (Page 6,15,23)
045 the damping of SDIO change to 0 ohm by Intel request Page 16)
046 add PU for SDIO WP by Intel request (Page 16)
047 remove Q31 because PU to PP3300_DSW at EC side already (Page 23)
048 change headphone CN6 footprint and PN (Page 24)
049 stuff PR188 due to 3.3V to EC is more safe(Page 29)
050 PR135 change from 300 to 348 ohm for protol issue (Page 33)
051 PR155 change from 300 to 348 ohm for protol issue (Page 33)
052 PC57 change from 68p to 120p PC58 change from 150p to 220Op for protol issue (Page 33)
053 PC59 change from 68p to 120p PC186 change from 150p to 220Op for protol issue (Page 33)
10/29
054 unstuff R129,R372,R380,R364 using SoC internal PU (Page 4,5)
055 eDP power change to P3C fuse (Page 17)
056 change R358 to 0 ohm by intel request(Page 21)
057 remove pulled up resistors for eMMC data and cmd (Page 21)

10/30
058 change C68 power netname for layout (Page 8)
059 SSD change to 74AUP1G34 and stuff it (Page 11)
060 remove PD82@ pulled up resistor R323(Page 11)
061 stuff Q47,R321,R328 and un-stuff R323,R142 for Track Pad I2C (Page 15)
062 HDMI DDC pulled up to HDMI_5V by intel request (Page 19)
063 add Power LED for Intel testing (Page 22)
064 Thermal IC VGD has two option, ome is PP3300_DSW(*PP3300_EC), another is PP3300_DX, default is stuffing to DSW rail(Page 23,27)
065 add Power BTN for Intel testing(Page 27)
066 for GFx power, change C266,C269,C298 to 10uF and add 2 caps 10uF (Page 8)
067 for core power, change C271,C261,C259,C276,C273 to 10uF(Page 8)
068 for VR compensation, PR26 change to 16.9K,PR23 change 10 ohm,PC50 change 1200pF,PC49 change to 270pF,un-stuff PR22,PC54(Page 33)
069 for VR compensation, PR76 change to 16.9K,PR86 change 10 ohm,PC166 change 1200pF,PC114 change to 270pF,un-stuff PR88,PC161(Page 33)
10/31
070 remove TP44 and TP35 for GND vias adding (Page 8)
071 remove C285(Page 9)
072 N.C SIO pin1(Page 11)
073 un-stuff PR129,PC37,PR158,PC118(Page 33)
074 stuff R273,R286,R288,R323 for Intel request(Page 11)
075 for layout suggestion by intel, VSS_AXG_SENSE didn't connect to VSS_SENSE, will connect the GND via near VCC_AXG_SENSE(Page 8)
076 add 0.1u on PP1800_PCH for power request(Page 33)
077 remove R417, PRDY should be direct connection between SoC and XDP by intel request (Page 6)
078 for layout, add 0R between GND and VSS_AXG_SENSE (Page 8)
11/1
079 add option BOM R446,R449 for EC CLK for power saving by Intel request (Page 7)
080 stuff C16(Page 11)
081 correct C261 footprint(Page 16)
082 change Holed footprint (Page 25)
11/4
083 Change PR135 from 348/F_4 to 340/F_4 (Page 33)
11/11
C01 Remove CHG USB charge option,eMMC@ eMMC option (Page 25)
C02 Add CHG@ option for single channel SKU (Page 13)
11/15
C03 stuff R372, system can't boot if un-stuff R372 on proto1.5 board, need intel double confirm before proto2 (Page 4)
C04 stuff R386, it is required for eDP (Page4)
C05 USB footprint change to 5 pin which is same as eDP power switch (Page 16)
C06 correct U11 orcad symbol, pin5 needs connect to power input (Page 17)
C07 remove R58 and change R74 to Short PAD and size to 84X2 (Page 19)
C08 change R72/R73/R22 to short PAD(Page 19)
C09 PR128 change to 1.62K (Page 33)
C10 Revising block diagram (Page 1)
11/18
C11 add TP on pin38/73 for NFC function (Page 20)
11/21
C12 remove R28,R25,C35 (Page2)
C13 remove R29,R24,C36 (Page 3)
C14 by X'tal vender suggestion,change C105/C106 from 15pF to 12pF (Page 6)
C15 remove R22/R72/R73 (Page 19)
C16 remove R365(Page 21)
C17 remove R91,R92,R94,R85 for cancelling non USB charger SKU (Page 25)
C18 change USB3 CMC L5,L3, this part is recommended by Intel (Page 26)
C19 by X'tal vender suggestion, change C107/C109 from 15pF to 18pF (Page 27)
11/28
C20 add a connection and name to KBD_IRQ#, besides add pulled high resistor (Page6)
C21 remove R29,R26,C36 (Page 3)
C22 by X'tal vender suggestion,change C105/C106 from 15pF to 12pF (Page 6)
C23 remove R166, because SERIRQ# of TPM needs 3V (Page 14)
C24 reserve 0 ohm R387/R391 on VCCA and VCCB for debugging(Page 14)
C25 change HDMI CMC L2, this part is recommended by Intel (Page 19)
C26 remove HDMI EMI solution R38,R32,R40,R57 (Page 19)
C27 remove R318 by intel request and has confirmed with EMI (Page 21)
C28 add pullup 10K on SERIRQ_0 to TPM_VDD (Page 22)
11/29
C29 change PQ1,PQ2 part number (Page28)
C30 add and stuff 470pF on PC7 and reserve 470pF on PC18 for EMI solution (Page 28)
C31 because of power source of PU24,PU25 change to VIN, so that need change sensing power net (Page 32)
C32 PQ26 change MOSFET with lower Rdson(Page 32)
C33 change solutions of PP1050_PCH and PP090_PCH_SS ,which power sources are VIN, it is better for power efficiency (Page 32)
C34 PP1800_PCH changes from convert to power MOSFET type for power efficiency improvement(Page 32)
C35 PP1350_PCH change from LDO to power MOSFET (Page 34)
C36 PP3300_PCH change from LDO to power MOSFET(Page 35)
C37 Revising block diagram,power sequence, and power tree for power changes by Intel suggestion(Page 1,37,39)
12/02
C38 add C285 for USB input inrush current (Page16)
C39 PJ2 changes footprint for layout (Page 28)
C40 change PC65 and PC36 from 4.7uF to 10uF (Page 32)
C41 add PR169,PR49 for Intel request,stuff PR169 as default(Page 32)
C42 add PR165,PR66 for Intel request,stuff PR165 as default(Page 32)
C43 PQ29 change back AO3400(Page 32)
C44 PQ13 change to lower Rdson part, besides source of PQ13 changes to PP1000_PCH_SS (Page 32)
C45 revising pull up power rail of PR169 and PR166(Page 32)
C46 change L2,(HDMI CMC),L3,L5(USB3)to DLP11TB680HL3L as Intel's recommendation (Page 19,25)
12/06
C47 for z-height issue, change C72,C75,C81 to 0.85mm cap (Page8)
C48 reserve 2x100Kpf cap for EMI(Page 25)
C49 change Hole1 to be battery enable function (Page 25)
C50 for z-height issue change@C40,PC49 to 0.85mm cap(Page 29)
C51 del PAD1 and PAD2(Page 25)
12/05
C52 add 0.1uFx2 on PP1350 for EMI request (Page12)
C53 To prevent the backlight flash, add a pull down on SoC_EDP_BLON_C and using double inverting GO FETs structure(Page 15)
C54 RSSi changes to 1A to isolate SD socket and servo/SoC (Page 16)
C55 SD3_WP is 1.8V power rail in SoC,change external Pulled up power well of SD3_WP to 1.8V power(Page 16)
C56 L2 change back to DLP11SA680HL2(Page 19)
C57 Swap L3,L5 pin for layout smoothly(Page 25)
12/06
C58 change PU16,PU17 part number(Page 28)
C59 change C271,C273,C280,C266,C311,C315 to 0603 22uF for ACLL issue(Page 8)
12/09
C60 reserve R226connnection from RCV0 to MIC_DET as back up in case driver needs to be through codec using JACKSNS pinr(Page 24)
C61 remove JP9,JP13 for ACLL improvement(Page 33)
12/11
C62 add pulled up resistors on SDIO data/cmd lines (Page16)
C63 add back pulled up resistors for eMMC I/F(Page 21)
C64 co-layout ST and Infineon TPM, if change to ST,R56,R57,R69,R72,R38, ST PN is ST33ZP24AR28PVSM(Page 22)
C65 change footprint for hole9(Page 25)
C66 move EC_PWROK from PA2 to P21(Page 27)
C67 add Test points on unused pins, need check layout to see if all points are ok(Page 27)
12/12
C68 add new BAMID 1@1 for single channel SKU (Page7)
C69 all Pulled up resistors of SDIO data/cmd to be un-stuffed(Page 16)
C70 all Pulled up resistors of eMMC data/cmd to be un-stuffed,and R161 change to 47K ohm as well(Page 21)
C71 add 2 holes , leave N.C(Page 25)
C72 Stuff NUT on Hole1,5(Page 25)
C73 change part number of EC ,which has a trial firmware inside(Page 27)
C74 reserve PR170 for battery cell selection(Page 28)
C75 stuff PC211(Page 29)
12/13
C76 swap CLKREQ_WLAN and CLKREQ_IMAGE for CLKREQ and CLK pins are aligned (Page6)
C77 change pull up power of PP3300_PCH_PG to PP3300_EC (Page 35)
C78 Board ID of protol change to 001 (Page27)
C79 un-stuff PR178,PC202 as snubber isnt needed (Page 28)
C80 un-stuff PR74,PC184,PR81,PC115 as snubber isnt needed (Page33)
01/15
C81 change CN15 USB3.0 connector type
C82 change CN6 Audio Jack connector type
C83 change CN3 HDMI connector type
01/27
C84 change CN8 Keyboard connector type
02/18
C85 unstuff U20, R156, R387, R391, R353 for SERIRQ leakage issue (Page14,22)