Microprocessors Module 1 Important Topics

Register organisation of 8086

- 8086 contains
  - General purpose register
    - Used to hold data, variables and intermediate results temporarily
  - Special purpose registers
    - Used as
      - segment register
      - pointer
      - index register
      - offset storage register
- All registers are 16 bit registers
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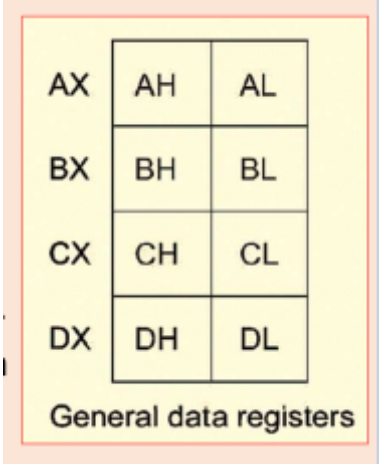
General Data Register

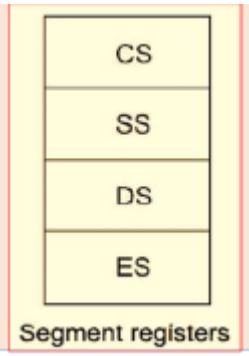
- The registers AX, BX, CX and DX are the general purpose 16 bit registers



- AX
  - Used as 16 bit accumulator
  - Lower 8 bits of AX = AL
  - Higher 8 bits of AX = AH
  - L = Lower
  - H = Higher
  - X = Complete 16 bit register
- BX

    - Used as offset storage for forming physical address
    - Used as base register
- CX
    - Used as default counter
- DX
    - Used as destination

Segment Register



Segmentation

- Segmentation is the process in which the main memory of the computer is logically divided into different segments
    - each segment has its own base address
- Its used to enhance speed of execution
- Segment is a logical unit of memory
    - Minimum size = 16 bytes
    - Maximum Size = 64 KB
- CS - Code Segment Register
    - contains the segment address for the code where the executable program is stored
- DS - Data Segment Register
    - points to the data segment of the memory where the data is stored
- ES - Extra Segment Register
    - points to another data segment of the memory .It also contains data
- SS - Stack Segment Register
    - used for addressing stack segment of the memory.
    - Stack segment is used to store stack data

Pointer and index register

- Here the pointers are

    - SP = Stack Pointer
        - Contains offset in stack segment
    - BP = Base Pointer
        - Offset in data segment
    - IP = Instruction Pointer
        - Offset is code segment
- Index Registers
    - SI = Source Index
        - Offset of source data in data segment
    - DI = Destination Index
        - Offset of Destination in data segment/extra segment

Flag Register

- Contains result of computations in ALU
- Contains Flag bits to control CPU

8086 architecture with figure

- 8086 Provides
    - 16 Bit ALU
    - 16 Bit Registers
    - Segmented memory addressing capabilities
- Architecture can be divided into 2
    - Bus Interface Unit (BIU)
    - Execution EU

Bus interface unit(BIU)

- Fetches instructions
- Reads data from memory, I/O ports
- Writes data to memory and I/O Ports
- Responsible for Establishing communication (Through bus) with
    - external devices
    - peripherals
    - Memory
- Contains circuit for
    - address generation unit
        - Creating physical addresses

- bus control unit
- segment registers
- instruction pointer
- instruction queue

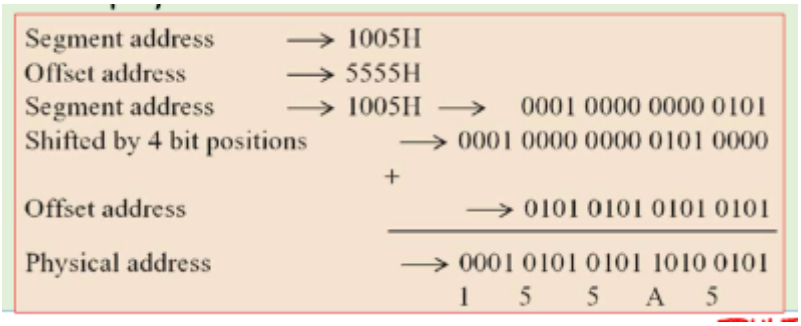
Execution Unit (EU)

- Executes instruction which is fetches by BIU

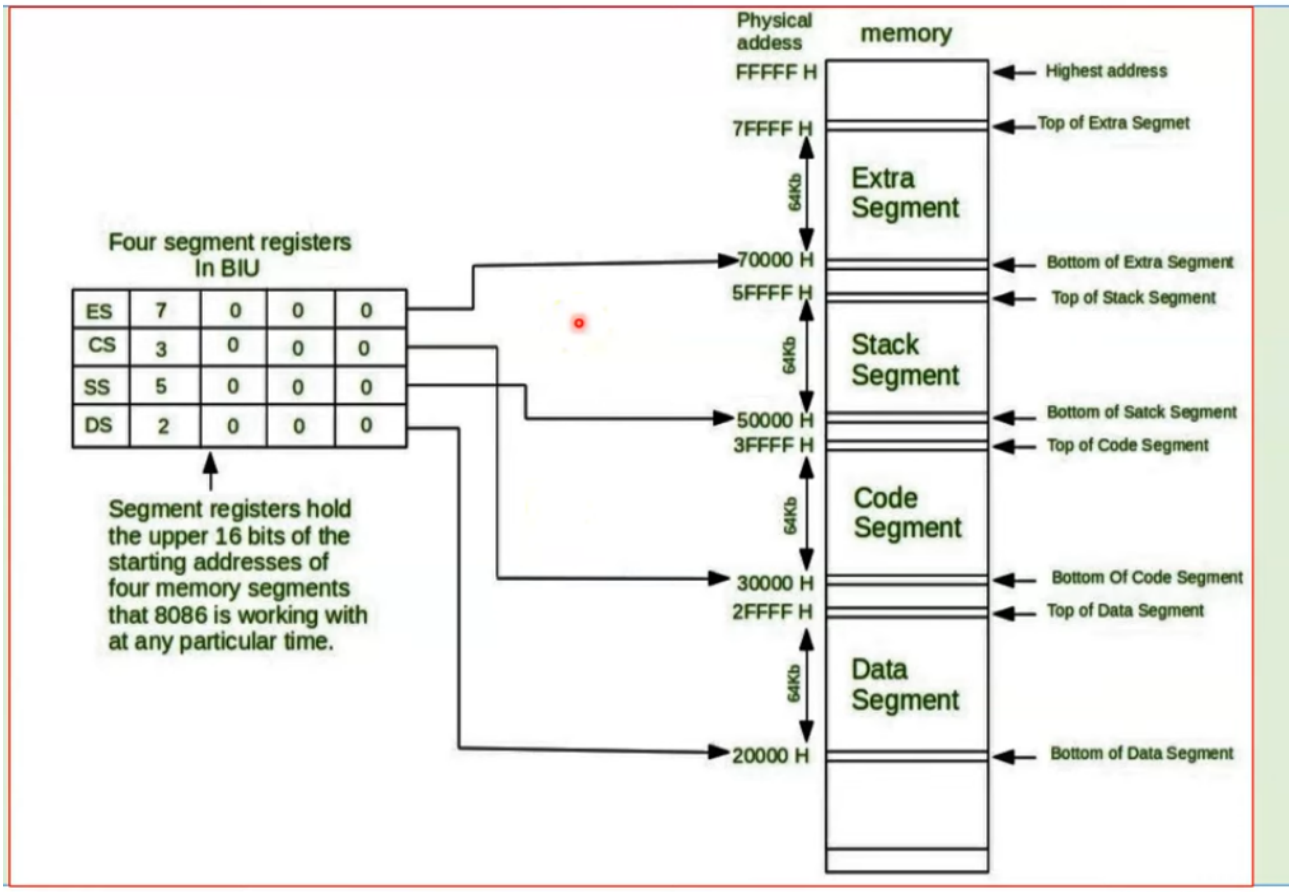
Instruction Queue

- FIFO -> First in First Out
- Size of queue -> 6 bytes
- BIU fetches instruction code from memory and store in queue
- EU Fetches instruction code from the queue

Physical Address

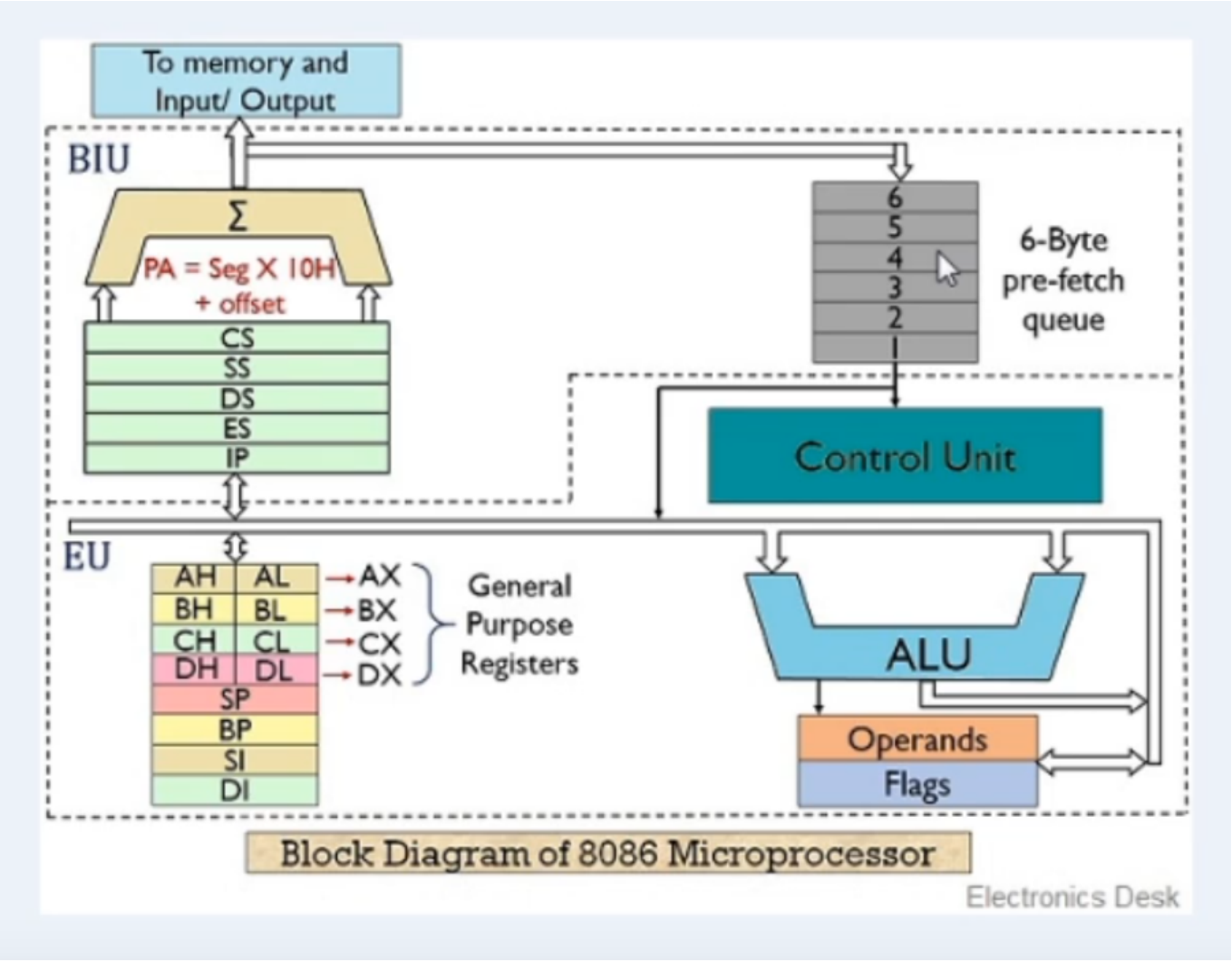
- 20 Bit Long
- Generated using segment and offset registers
  - Each 16 bit long
- Content of segment register = segment address
- Content of offset register = offset address
- For generating a physical address
  - Shift segment address to the left 4 times
    - Example
      - Before -> Segment address = 1005H -> 0001 0000 0000 0101
      - After -> Segment Address ->
        - 4 times shift to the left -> 0001 0000 0000 0101 0000
  - Add offset address to it, to get 20 bit physical address
  - 

Pictorial view of segmentation



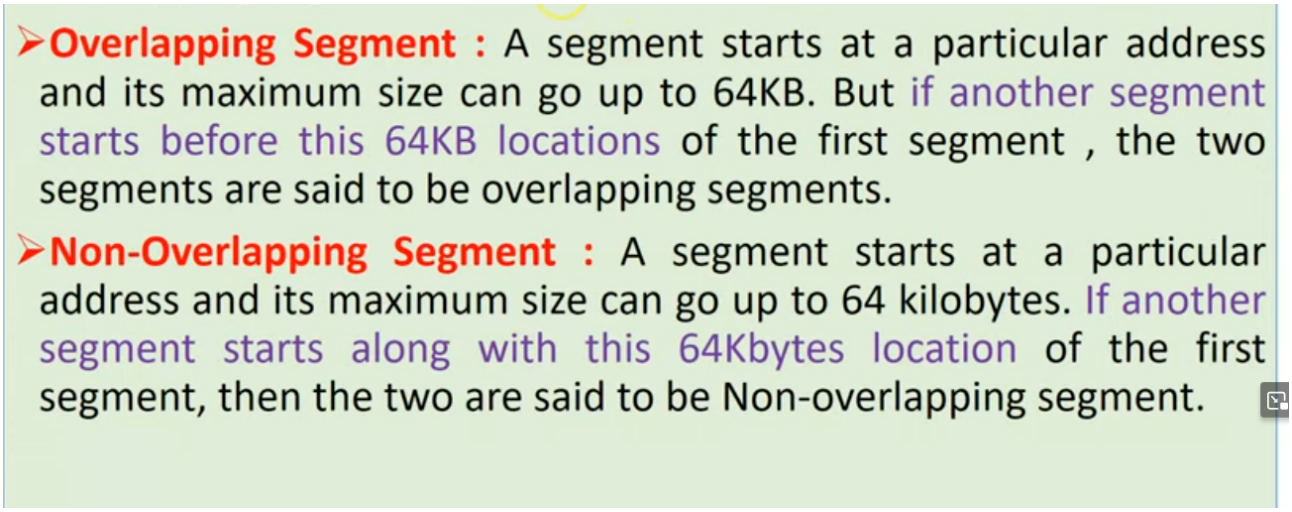
- Here we have ES,CS,SS,DS
- The table is having the base addresses of each
- For example ES, has base 70000 and goes upto 7FFFF

Block diagram



- Segment register contains base address to the particular segment
- Offset indicates distance between memory location and base address in the segment
- In execution unit
  - the 16 bit ALU performs arithmetic and logical operations
  - 16 bit flag register contains result of execution by ALU

Types of segments

- 

Flag Register

- A flag is a flip-flop used to store the information about the status of the processor and the status of the instruction executed most recently. 8086 has 9 flags.

Acronym (ODIT SZ CAP)

- Overflow Flag
  - Set if overflow occurs
- Direction Flag
  - Flag= 0
    - String processed lowest -> highest
  - Flag = 1
    - String processed highest -> lowest
- Interrupt flag
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  - Flag = 1 when maskable interrupt is recognised by CPU
- Trap Flag
  - Flag = 1 when trap interrupt is generated after execution of each instruction
- Sign Flag
  - Flag = 1 when result of computation is negative
- Zero Flag
  - Flag = 1 when result of computation is 0
- Ac Auxiliary carry flag
  - Flag = 1 if there's a carry from the lowest nibble
- P - Parity Flag
  - Flag = 1 when result has even parity
  - Flag = 0, when odd parity

- Cy - Carry Flag
  - Set when there's a carry from addition or borrow from subtraction
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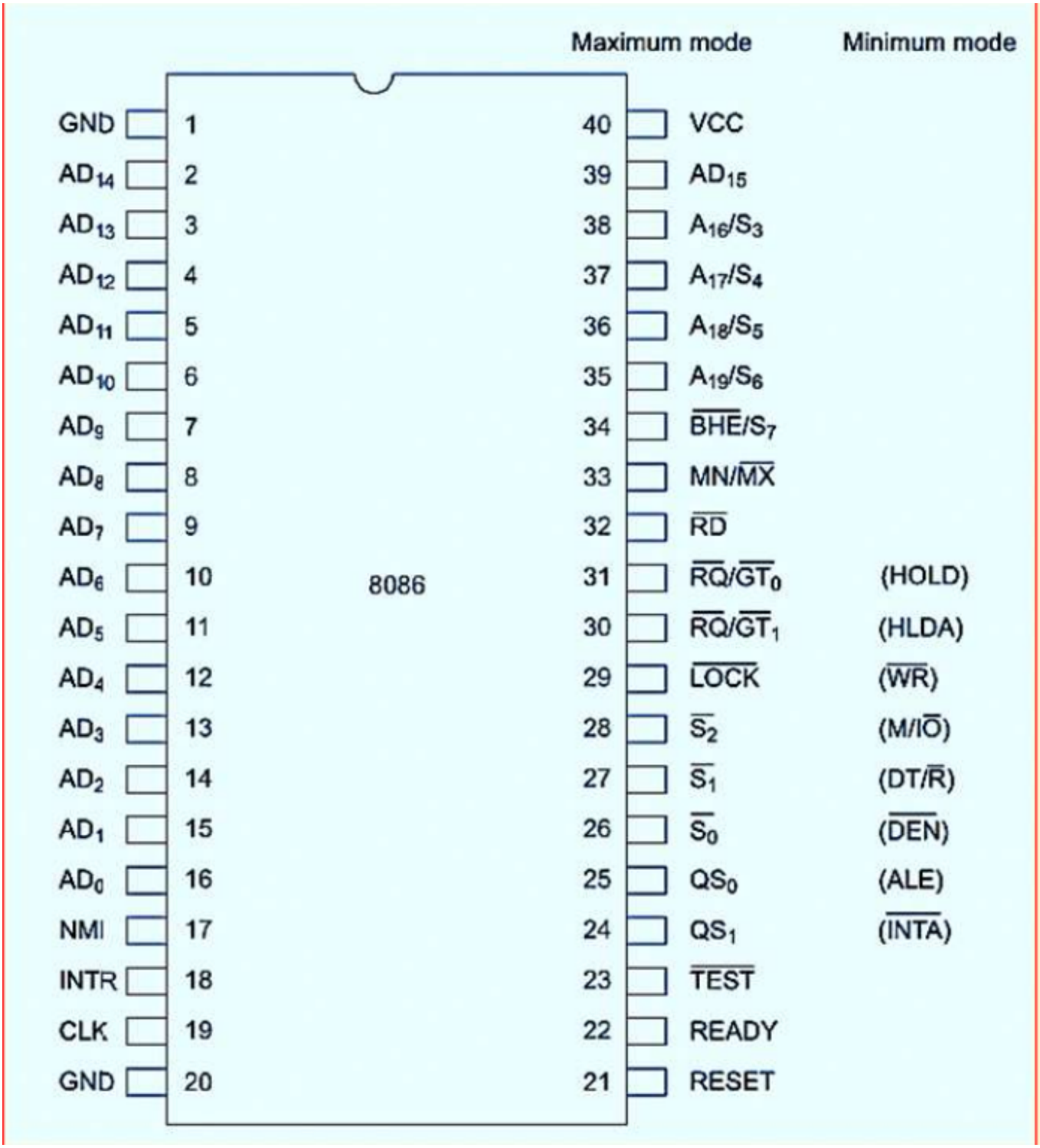
8086 signal descriptions

- Signals can be divided to 3 groups
  - Signals having common functions for maximum Mode
  - Signals having special functions for minimum mode
  - Signals having special functions for maximum mode

Pin Configuration of 8086



Simple story to learn about pin diagram

- First Half
  - We start from Ground
  - We start from AD14 to AD0
  - Our characters Name is N I C
    - N -> NMI
    - I -> INTR

        - C -> CLK
    - We end in Ground
- 2nd Half
    - Start from VCC
    - AD15 -> NIC has no supply
    - A16,A17,A18,A19 -> NIC has Supply in S3,S4,S5,S6
    - Frustrated with supply, NIC decides to make a BOMB using BHE in S7
    - NIC meets twins MN and MX
    - They make bomb on Road RD
    - One twin made RQ GT0
    - Other twin made RQ GT1
    - They got caught and got LOCKd up
    - While in jail, NIC remembers his golden days
        - S2,S1,S0 Full Pass
    - Then the teach from QS1 and QS0 meets them gives them motivation
    - Then NIC writes the Test
    - NIC is READY and passed
    - NIC is reset back to normal

Definition of each of the pins

- AD15 - AD0 (Address/Data Bus)
    - AD0 - AD7 carries low order byte data
    - AD8 - AD15 carries high order byte data
    - First Clock cycle -> Carries 16 bit address
        - After that carries 16 bit data
- A19/S6, A18/S5, A17/S4, A16/S3 (Address/ Status Bus)
    - First Clock cycle -> 4 bit Address
        - Later -> status signals
- BHE /S7 (Bus High Enable/ Status)
    - Indicate transfer of data using data bus D5 to D8
- RD (Read)
    - Read signal for read operation
    - Active when low
- READY
    - Acknowledgement from slow devices or memory that they completed data transfer
    - Active when high

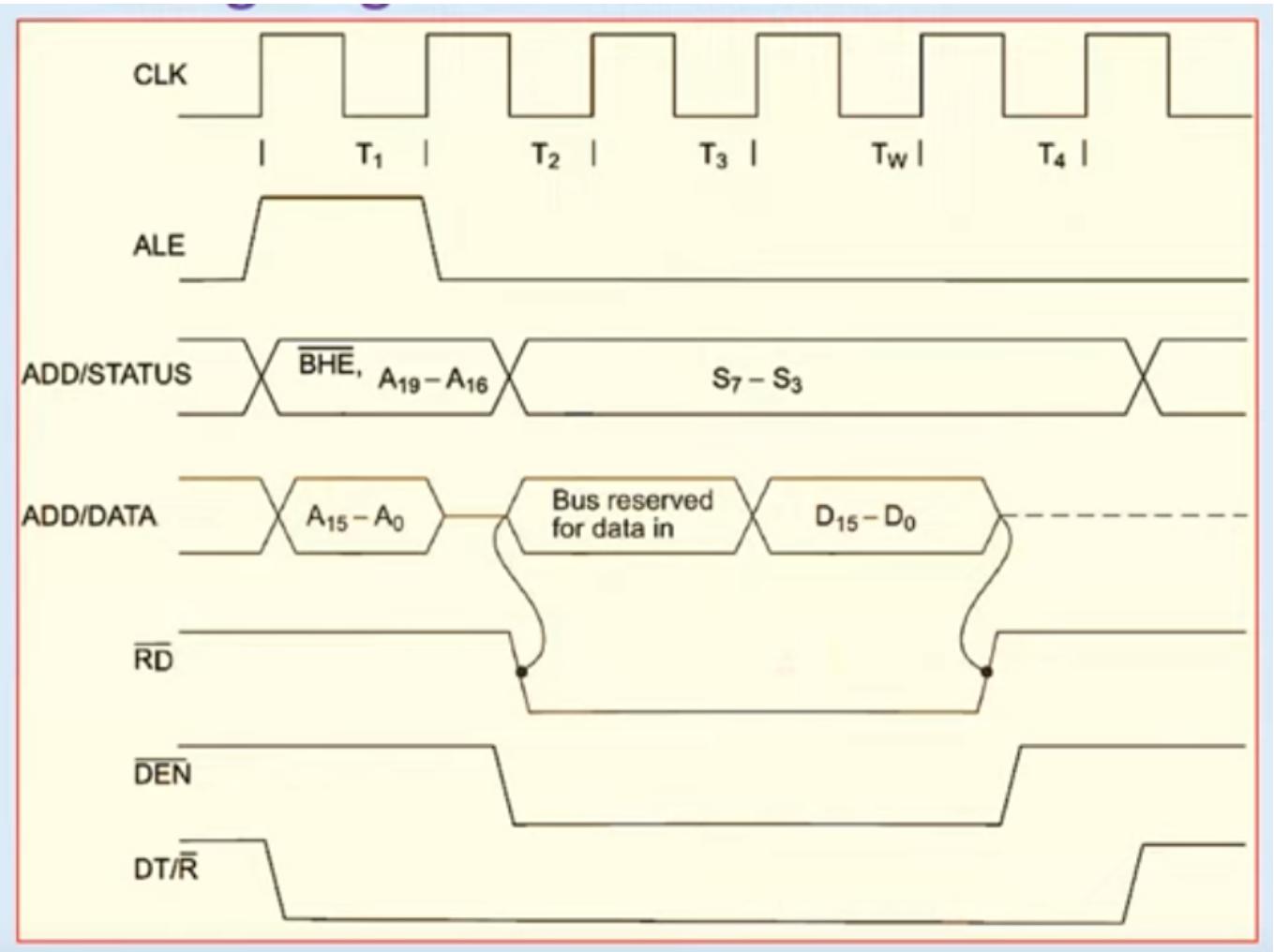
- INTR (Interupt request)
  - Enabled at the last clock cycle of each instruction
  - To determine when processor considers this as an interupt
- TEST
  - if TEST is low
    - Execution continues
  - else
    - processor remains in idle state
- NMI (Non Maskable interupt)
- RESET
  - Used to restart the execution
  - Causes processor to immediately terminate present activity
  - Active when high
- CLK (Clock Input)
  - Provides basic timing for processor operation/bus control activity
- VCC
  - Power supply +5V
- GND
  - Ground
- MN/MX
  - Indicates the mode of operations (Maximum or minimum)
- M/IO (Memory/IO)
  - Used to distinguish between memory and I/O operations
  - Low
    - CPU has I/O operations
  - High
    - CPU has memory operation
- INTA (Interrupt Acknowledge)
  - Acknowledges interrupt
  - Low
    - Processor has accepted the interrupt
- ALE (Address Latch Enable)
  - Indicates availability of valid address on address/data line
- DT/R (Data Transmit/ Receive)
  - High
    - When data is transmitted
  - Low

        - Processor is receiving data
- DEN (Data enable)
    - Indicates availability of valid data over address/data lines
- HOLD
    - Indicates external devies are requesting to access Address/Data Buses
- HLDA (Hold Acknowledge
    - Acknowledges hold signal
- S2,S1,S0
    - Status lines that provide status of operation
- LOCK
    - Active when low
    - Other bus masters will be prevented from gaining system bus
- QS1,QS0 (Queue status)
    - Status of instruction queue
- RQ/GT0, RQ/GT1 (Request/Grant)
    - For requesting the CPU to release system BUS

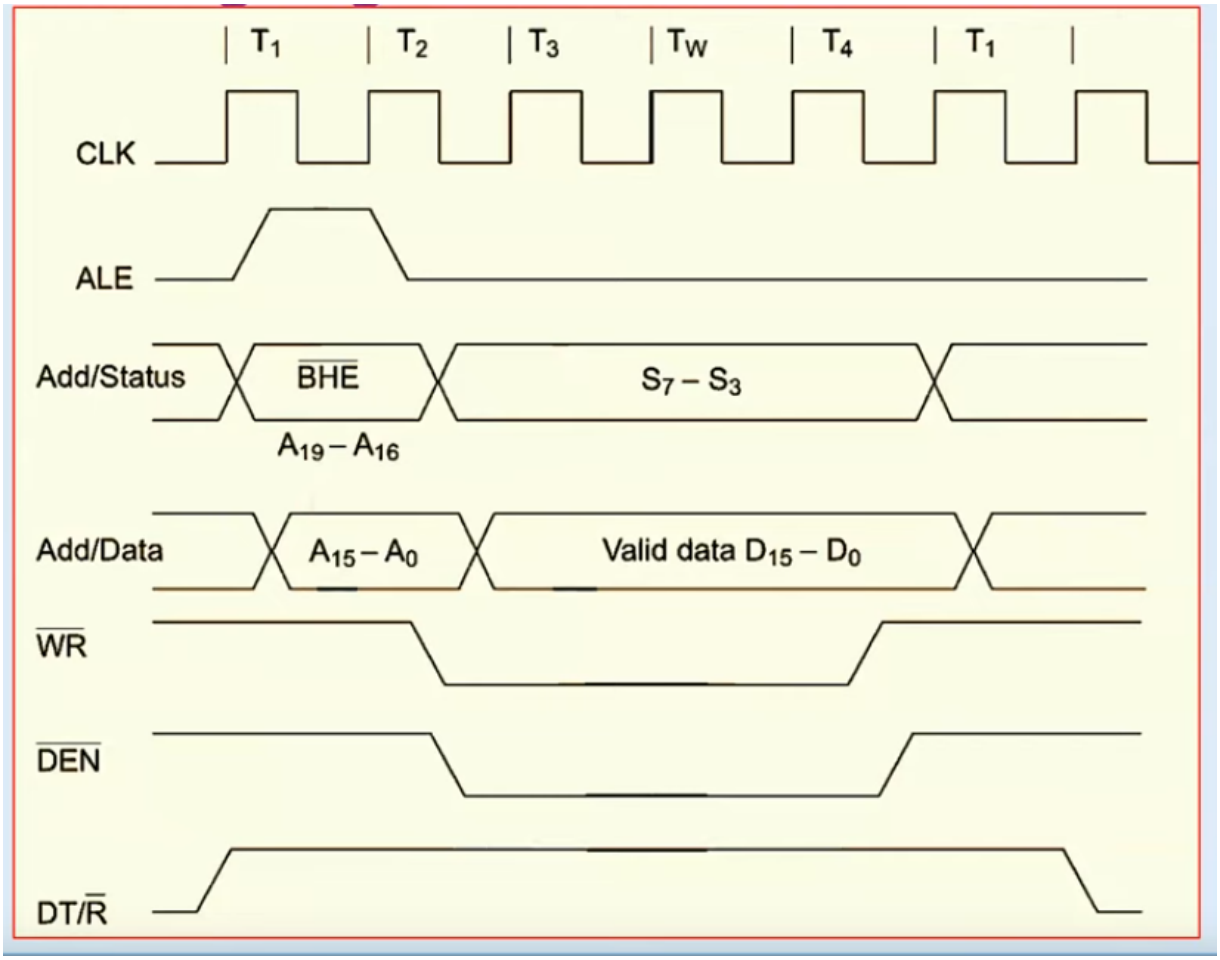
Minimum mode timing diagram

Minimum Mode

- There is a single microprocessor in minimum mode system



- The above is the Read Cycle Timing diagram for minimum mode
- T1,T2,T3,T4 are clock pulse
- One timing cycle have 4 clock pulse, including waiting time
- During T1 Clock pulse
  - Address Latch becomes high
    - When ALE is High
      - We can send address and data into the bus
    - Address is active
      - Remaining S7-S3 status is active instead of address
    - A15-A0 is active
      - Remaining Data is active
    - RD is not active in address
      - RD is active in data
    - DEN (Data Enable)
      - High on Address
    - DT/R (Data Transmit/Receive)
      - Receive mode

- Similarly Write cycle timing diagram
- 

Comparison 8086 & 8088

COMPARISON OF 8086 &8088

8086	8088
• It has 16 bit data bus • It can read or write 8/16 bit data at a time • Memory space is organized as two 512KB (2×512KB = 1 MB) banks • It can operate at three clock speed , ie ; 5MHz , 8MHz and 10MHz • Instruction queue is 6 bit long • It has BHE pin • It draws maximum supply current of 360MA	• It has 8 bit data bus • It can only do so for 8 bit data • It is implemented as a single 1MB bank • It is available only in two clock speed , ie; 5MHz and 8MHz • Instruction queue is 4 bit long • This pin is replaced by status output (SSO),since it can read or write only 8 bit data • It draws maximum supply current of 340MA