



# NVIDIA BlueField-3 DPU User Guide

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## About This Manual

This User Manual describes NVIDIA® BlueField®-3 InfiniBand/Ethernet DPU (Data Processing Unit). It provides details as to the interfaces of the board, specifications, required software and firmware for operating the board, and a step-by-step plan of how to bring up the BlueField-3 DPUs.

## Ordering Part Numbers

The tables below list the ordering part numbers (OPNs) for available BlueField-3 DPUs in Full-Height Half-Length (FHHL) form factor.

| Form Factor      | NVIDIA OPN          | Model   | Series / Cores          | Data Transmission Rate                                   | No. of Ports     | PCIe Support     | x16 PCIe Extension Option | External Power Connector | Crypto | On-Board DDR5 Memory | Integrated BMC | Bracket Type | Device ID | PSID         | Lifecycle           |
|------------------|---------------------|---------|-------------------------|--|------------------|------------------|---------------------------|--------------------------|--------|----------------------|----------------|--------------|-----------|--------------|---------------------|
| Single-Slot FHHL | 900-9 D3B4-00EN-EA0 | B31 40L | E-Series / 8 Arm-Cores  | InfiniBand: NDR 400Gb/s (Default)<br>Ethernet: 400GbE    | 1-Port QSFP 112  | PCIe Gen 5.0 x16 | -                         | -                        | ✓      | 16GB                 | ✓              | Tall         | 416 92    | MT_000001010 | Engineering Samples |
|                  | 900-9 D3B4-00PN-EA0 | B31 40L | E-Series / 8 Arm-Cores  | InfiniBand: NDR 400Gb/s (Default)<br>Ethernet: 400GbE    | 1-Port QSFP 112  | PCIe Gen 5.0 x16 | -                         | -                        | -      | 16GB                 | ✓              | Tall         | 416 92    | MT_000001011 | Engineering Samples |
|                  | 900-9 D3B6-00CC-EA0 | B32 10E | E-Series / 16 Arm-Cores | InfiniBand: HDR100 100Gb/s<br>Ethernet: 100GbE (Default) | 2-Ports QSFP 112 | PCIe Gen 5.0 x16 | ✓                         | ✓                        | ✓      | 32GB                 | ✓              | Tall         | 416 92    | MT_000001024 | Engineering Samples |
|                  | 900-9 D3B6-00SC-EA0 | B32 10E | E-Series / 16 Arm-Cores | InfiniBand: HDR100 100Gb/s<br>Ethernet: 100GbE (Default) | 2-Ports QSFP 112 | PCIe Gen 5.0 x16 | ✓                         | ✓                        | -      | 32GB                 | ✓              | Tall         | 416 92    | MT_000001025 | Engineering Samples |
|                  | 900-9 D3B6-00CV-AA0 | B32 20  | P-Series / 16 Arm-cores | InfiniBand: NDR200 200Gb/s<br>Ethernet: 200GbE (Default) | 2-Ports QSFP 112 | PCIe Gen 5.0 x16 | ✓                         | ✓                        | ✓      | 32GB                 | ✓              | Tall         | 416 92    | MT_000000884 | Mass Production     |

| Form Factor   | NVIDIA OPN          | Model | Series/ Cores           | Data Transmission Rate                                | No. of Ports     | PCIe Support     | x16 PCIe Extension Option | External Power Connector | Crypto | On-Board DDR5 Memory | Integrated BMC | Bracket Type | Device ID | PSID         | Lifecycle           |
|---------------|---------------------|-------|-------------------------|---|------------------|------------------|---------------------------|--------------------------|--------|----------------------|----------------|--------------|-----------|--------------|---------------------|
|               | 900-9 D3B6-00SV-AA0 | B3220 | P-Series / 16 Arm-cores | InfiniBand: NDR200 200Gb/s Ethernet: 200GbE (Default) | 2-Ports QSFP 112 | PCIe Gen 5.0 x16 | ✓                         | ✓                        | -      | 32GB                 | ✓              | Tall         | 41692     | MT_000000965 | Mass Production     |
| Dual-Slot FHH | 900-9 D3B6-00CN-AB0 | B3240 | P-Series / 16 Arm-Cores | InfiniBand: NDR 400Gb/s (Default) Ethernet: 400GbE    | 2-Ports QSFP 112 | PCIe Gen 5.0 x16 | ✓                         | ✓                        | ✓      | 32GB                 | ✓              | Tall         | 41692     | MT_000000883 | Engineering Samples |
|               | 900-9 D3B6-00SN-AB0 | B3240 | P-Series / 16 Arm-Cores | InfiniBand: NDR 400Gb/s (Default) Ethernet: 400GbE    | 2-Ports QSFP 112 | PCIe Gen 5.0 x16 | ✓                         | ✓                        | -      | 32GB                 | ✓              | Tall         | 41692     | MT_000000964 | Engineering Samples |

## EOL'ed (End of Life) DPUs

## Intended Audience

This manual is intended for the installer and user of these cards. The manual assumes basic familiarity with InfiniBand/Ethernet network and architecture specifications.

## Technical Support

Customers who purchased NVIDIA products directly from NVIDIA are invited to contact us through the following methods:

- URL: [www.nvidia.com](http://www.nvidia.com) → Support
- E-mail: [enterprisesupport@nvidia.com](mailto:enterprisesupport@nvidia.com)

Customers who purchased NVIDIA M-1 Global Support Services, please see your contract for details regarding Technical Support.

Customers who purchased NVIDIA products through an NVIDIA-approved reseller should first seek assistance through their reseller.

## Related Documentation

|   |  |
|---|--|
| <a href="#"><u>InfiniBand Architecture Specification</u></a>    | InfiniBand Trade Association (IBTA) InfiniBand® specification Release 1.3.1, November 2, 2016 and Vol. 2, Release 1.4 , and Vol 2 - Release 1.5.   |
| <a href="#"><u>IEEE Std 802.3 Specification</u></a>             | IEEE Ethernet specification.   |
| <a href="#"><u>PCI Express Specifications</u></a>               | Industry Standard PCI Express Base and Card Electromechanical Specifications.  |
| <a href="#"><u>NVIDIA LinkX Interconnect Solutions</u></a>      | The NVIDIA® LinkX® product family of cables and transceivers provide the industry's broadest portfolio of QDR/FDR10 (40Gb/s), FDR (56Gb/s), EDR/HDR100 (100Gb/s), HDR (200Gb/s) and NDR (400Gb/s) cables, including Direct Attach Copper cables (DACs), copper splitter cables, Active Optical Cables (AOCs) and transceivers in a wide range of lengths from 0.5m to 10km. In addition to meeting IBTA standards, NVIDIA tests every product in an end-to-end environment ensuring a Bit Error Rate of less than 1E-15. |
| <a href="#"><u>BlueField DPU Platform BSP Documentation</u></a> | This guide provides product release notes as well as information on the BSP and how to develop and/or customize applications, system software, and file system images for the BlueField platform.  |
| <a href="#"><u>DOCA SDK Software Documentation</u></a>          | NVIDIA DOCA SDK software.  |

## Document Conventions

When discussing memory sizes, GB and GBytes are used in this document to mean size in gigabytes. The use of Gb or Gbits (small b) indicates size in gigabits. In this document PCIe is used to mean PCI Express.

## Revision History



A list of the changes made to this document are provided in [Document Revision History](#).

# Introduction

The NVIDIA® BlueField®-3 data processing unit (DPU) is the 3rd-generation data center infrastructure-on-a-chip that enables organizations to build software-defined, hardware-accelerated IT infrastructures from cloud to core data center to edge. With 400Gb/s Ethernet or NDR 400Gb/s InfiniBand network connectivity, BlueField-3 DPU offloads, accelerates, and isolates software-defined networking, storage, security, and management functions in ways that profoundly improve data center performance, efficiency, and security. Providing powerful computing, and a broad range of programmable acceleration engines in the I/O path, BlueField-3 is perfectly positioned to address the infrastructure needs of the most demanding applications, while delivering full software backward compatibility through the NVIDIA DOCA™ software framework.

BlueField-3 DPUs transform traditional computing environments into secure and accelerated virtual private clouds, allowing organizations to run application workloads in secure, multi-tenant environments. Decoupling data center infrastructure from business applications, BlueField-3 enhances data center security, streamlines operations, and reduces the total cost of ownership. Featuring NVIDIA's in-network computing technology, BlueField-3 enables the next generation of supercomputing platforms, delivering optimal bare-metal performance and native support for multi-node tenant isolation.

## System Requirements

| Item                | Description   |
|---------------------|---|
| PCI Express slot    | <b>In PCIe x16 Configuration</b><br>PCIe Gen 5.0 (32GT/s) through x16 edge connector.<br><b>In PCIe x16 Extension Option - Switch DSP (Data Stream Port)</b> <ul style="list-style-type: none"><li>• PCIe Gen 5.0 SERDES @32GT/s through edge connector</li><li>• PCIe Gen 5.0 SERDES @32GT/s through PCIe Auxiliary Connection Card</li></ul>  |
| System Power Supply | Minimum 75W or greater system power supply for all cards.<br><br>P-Series DPUs with PCIe Gen 5.0 x16 require a supplementary 8-pin ATX power supply connectivity available through the external power supply connector.<br><br><div> NOTE: The power supply harness is not included in the package.</div><br><div> To power-up the DPU, power the ATX power supply and the PCIe golden fingers simultaneously. Failure to do so may harm the DPU.</div> |
| Operating System    | BlueField-3 DPU is shipped with Ubuntu - a Linux commercial operating system - which includes the NVIDIA OFED stack (MLNX_OFED), and is capable of running all customer-based Linux applications seamlessly. For more information, please refer to the DOCA SDK documentation or NVIDIA BlueField-3 Software User Manual.   |
| Connectivity        | <ul style="list-style-type: none"><li>• Interoperable with 1/10/25/40/50/100/200/400 Gb/s Ethernet switches and SDR/DDR/EDR/HDR100/HDR/NDR200/NDR InfiniBand switches</li><li>• Passive copper cable with ESD protection</li><li>• Powered connectors for optical and active cable support</li></ul>  |

For detailed information, see [Specifications](#).



## Package Contents

Prior to unpacking your DPU, it is important to make sure your server meets all the system requirements listed above for a smooth installation. Be sure to inspect each piece of equipment shipped in the packing box. If anything is missing or damaged, contact your reseller.

## Card Package



For FHHL P-Series DPUs, you need an 8-pin PCIe external power cable to activate the card. The cable is not included in the package. For further details, please refer to [External PCIe Power Supply Connector](#).

| Item        | Description                                     |
|-------------|---|
| Card        | 1x BlueField-3 DPU                              |
| Accessories | 1x tall bracket (shipped assembled on the card) |

## Accessories Kit



This is an optional accessories kit used for debugging purposes and can be ordered separately.

| Kit OPN    | Contents                                      |
|------------|---|
| MBF35-DKIT | 4-pin USB to female USB Type-A cable          |
|            | 20-pin shrouded connector to USB Type-A cable |

## PCIe Auxiliary Card Package



This is an optional kit which applies to following OPNs: 900-9D3B6-00CV-AA0, 900-9D3B6-00SV-AA0, 900-9D3B6-00CC-AA0, 900-9D3B6-00SC-AA0, 900-9D3B6-00CN-AB0 and 900-9D3B6-00SN-AB0.

The PCIe auxiliary kit can be purchased separately to operate selected DPUs in a dual-socket server. For package contents, refer to [PCIe Auxiliary Card Kit](#).

## Features and Benefits



This section describes hardware features and capabilities. Please refer to the relevant driver and/or firmware release notes for feature availability.

| Feature  | Description  |                 |                   |                    |                                    |
|--|--|-----------------|-------------------|--------------------|------------------------------------|
| InfiniBand Architecture Specification v1.5 compliant | BlueField-3 DPU delivers low latency, high bandwidth, and computing efficiency for high-performance computing (HPC), artificial intelligence (AI), and hyperscale cloud data centers applications. |                 |                   |                    |                                    |
|  | BlueField-3 DPU is InfiniBand Architecture Specification v1.5 compliant.   |                 |                   |                    |                                    |
|  | <b>InfiniBand Network Protocols and Rates:</b>   |                 |                   |                    |                                    |
|  | Protocol   | Standard        | Rate (Gb/s)       |                    | Comments                           |
|  |  |                 | 4x Port (4 Lanes) | 2x Ports (2 Lanes) |                                    |
|  | NDR/NDR200   | IBTA Vol2 1.5   | 425               | 212.5              | PAM4 256b/257b encoding and RS-FEC |
|  | HDR/HDR100   | IBTA Vol2 1.4   | 212.5             | 106.25             | PAM4 256b/257b encoding and RS-FEC |
|  | EDR  | IBTA Vol2 1.3.1 | 103.125           | 51.5625            | NRZ 64b/66b encoding               |
|  | FDR  | IBTA Vol2 1.2   | 56.25             | N/A                | NRZ 64b/66b encoding               |

| Feature                    | Description   |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|----------------------------|---|---|----------|-------------|---|---|---|------------------------------|----------------------|---------------------------------------|------------------------|--------------|---------------------|--------------|---------------------|--------------|---|--------------|--|------------------------------|------------------|---|--|---|--|
| Up to 400 Gigabit Ethernet | BlueField-3 DPU complies with the following IEEE 802.3 standards:<br>400GbE / 200GbE / 100GbE / 50GbE / 40GbE / 25GbE / 10GbE   |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            | <table><tr><th>Protocol</th><th>MAC Rate</th></tr><tr><td>IEEE802.3ck</td><td>400/200/100 Gigabit Ethernet<br/>(Include ETC enhancement)</td></tr><tr><td>IEEE802.3cd<br/>IEEE802.3bs<br/>IEEE802.3cm<br/>IEEE802.3cn<br/>IEEE802.3cu</td><td>400/200/100 Gigabit Ethernet<br/>(Include ETC enhancement)</td></tr><tr><td>IEEE 802.3bj<br/>IEEE 802.3bm</td><td>100 Gigabit Ethernet</td></tr><tr><td>IEEE 802.3by<br/>Ethernet Consortium25</td><td>50/25 Gigabit Ethernet</td></tr><tr><td>IEEE 802.3ba</td><td>40 Gigabit Ethernet</td></tr><tr><td>IEEE 802.3ae</td><td>10 Gigabit Ethernet</td></tr><tr><td>IEEE 802.3cb</td><td>2.5/5 Gigabit Ethernet<br/>(For 2.5: support only 2.5 x1000BASE-X)</td></tr><tr><td>IEEE 802.3ap</td><td>Based on auto-negotiation and KR startup</td></tr><tr><td>IEEE 802.3ad<br/>IEEE 802.1AX</td><td>Link Aggregation</td></tr><tr><td>IEEE 802.1Q<br/>IEEE 802.1P VLAN tags and priority</td><td></td></tr><tr><td>IEEE 802.1Qau (QCN)<br/>Congestion Notification<br/>IEEE 802.1Qaz (ETS)<br/>EEE 802.1Qbb (PFC)<br/>IEEE 802.1Qbg<br/>IEEE 1588v2<br/>IEEE 802.1AE (MACSec)<br/>Jumbo frame support (9.6KB)</td><td></td></tr></table> | Protocol  | MAC Rate | IEEE802.3ck | 400/200/100 Gigabit Ethernet<br>(Include ETC enhancement) | IEEE802.3cd<br>IEEE802.3bs<br>IEEE802.3cm<br>IEEE802.3cn<br>IEEE802.3cu | 400/200/100 Gigabit Ethernet<br>(Include ETC enhancement) | IEEE 802.3bj<br>IEEE 802.3bm | 100 Gigabit Ethernet | IEEE 802.3by<br>Ethernet Consortium25 | 50/25 Gigabit Ethernet | IEEE 802.3ba | 40 Gigabit Ethernet | IEEE 802.3ae | 10 Gigabit Ethernet | IEEE 802.3cb | 2.5/5 Gigabit Ethernet<br>(For 2.5: support only 2.5 x1000BASE-X) | IEEE 802.3ap | Based on auto-negotiation and KR startup | IEEE 802.3ad<br>IEEE 802.1AX | Link Aggregation | IEEE 802.1Q<br>IEEE 802.1P VLAN tags and priority |  | IEEE 802.1Qau (QCN)<br>Congestion Notification<br>IEEE 802.1Qaz (ETS)<br>EEE 802.1Qbb (PFC)<br>IEEE 802.1Qbg<br>IEEE 1588v2<br>IEEE 802.1AE (MACSec)<br>Jumbo frame support (9.6KB) |  |
|                            | Protocol  | MAC Rate  |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            | IEEE802.3ck   | 400/200/100 Gigabit Ethernet<br>(Include ETC enhancement)         |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            | IEEE802.3cd<br>IEEE802.3bs<br>IEEE802.3cm<br>IEEE802.3cn<br>IEEE802.3cu   | 400/200/100 Gigabit Ethernet<br>(Include ETC enhancement)         |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            | IEEE 802.3bj<br>IEEE 802.3bm  | 100 Gigabit Ethernet  |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            | IEEE 802.3by<br>Ethernet Consortium25   | 50/25 Gigabit Ethernet  |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            | IEEE 802.3ba  | 40 Gigabit Ethernet   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            | IEEE 802.3ae  | 10 Gigabit Ethernet   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            | IEEE 802.3cb  | 2.5/5 Gigabit Ethernet<br>(For 2.5: support only 2.5 x1000BASE-X) |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            | IEEE 802.3ap  | Based on auto-negotiation and KR startup                          |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            | IEEE 802.3ad<br>IEEE 802.1AX  | Link Aggregation  |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            | IEEE 802.1Q<br>IEEE 802.1P VLAN tags and priority   |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            | IEEE 802.1Qau (QCN)<br>Congestion Notification<br>IEEE 802.1Qaz (ETS)<br>EEE 802.1Qbb (PFC)<br>IEEE 802.1Qbg<br>IEEE 1588v2<br>IEEE 802.1AE (MACSec)<br>Jumbo frame support (9.6KB)   |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            |   |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            |   |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            |   |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            |   |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            |   |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            |   |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            |   |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            |   |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            |   |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            |   |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            |   |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            |   |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            |   |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
|                            |   |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
| On-board Memory            | <ul style="list-style-type: none"><li>• Quad SPI NOR FLASH - includes 256Mbit for Firmware image.</li><li>• UVPS EEPROM - includes 2Mbit.</li><li>• FRU EEPROM - Stores the parameters and personality of the card. The EEPROM capacity is 128Kbit. FRU I2C address is (0x50) and is accessible through the PCIe SMBus.</li><li>• DPU_BMC Flashes:<ul style="list-style-type: none"><li>• 2x 64MByte for BMC Image</li><li>• 512MByte for Config Data</li></ul></li><li>• eMMC pSLC 40GB with 30K Write Cycles eMMC for SoC BIOS and OS.</li><li>• SSD (onboard BGA) 128GByte for user SoC OS, logs and application SW.</li><li>• DDR5 SDRAM - 16GB/32GB @5600MT/s single/dual-channel DDR5 SDRAM memory. Solder down on-board. 128bit + 16bit ECC</li></ul>  |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |
| BlueField-3 IC             | The NVIDIA BlueField-3 DPU integrates x8 / x16 Armv8.2+ A78 Hercules cores (64-bit) is interconnected by a coherent mesh network, one DRAM controller, an RDMA intelligent network adapter supporting up to 400Gb/s, an embedded PCIe switch with endpoint and root complex functionality, and up to 32 lanes of PCIe Gen 5.0.  |   |          |             |   |   |   |                              |                      |                                       |                        |              |                     |              |                     |              |   |              |  |                              |                  |   |  |   |  |

| Feature  | Description  |
|--|--|
| <b>Overlay Networks</b>  | In order to better scale their networks, data center operators often create overlay networks that carry traffic from individual virtual machines over logical tunnels in encapsulated formats such as NVGRE and VXLAN. While this solves network scalability issues, it hides the TCP packet from the hardware offloading engines, placing higher loads on the host CPU. NVIDIA DPU effectively addresses this by providing advanced NVGRE and VXLAN hardware offloading engines that encapsulate and de-capsulate the overlay protocol.   |
| <b>RDMA and RDMA over Converged InfiniBand/Ethernet (RoCE)</b> | NVIDIA DPU, utilizing IBTA RDMA (Remote Data Memory Access) and RoCE (RDMA over Converged InfiniBand/Ethernet) technology, delivers low-latency and high-performance over InfiniBand/Ethernet networks. Leveraging data center bridging (DCB) capabilities as well as advanced congestion control hardware mechanisms, RoCE provides efficient low-latency RDMA services over Layer 2 and Layer 3 networks.  |
| <b>Quality of Service (QoS)</b>                                | Support for port-based Quality of Service enabling various application requirements for latency and SLA.   |
| <b>Storage Acceleration</b>                                    | <ul style="list-style-type: none"> <li>A consolidated compute and storage network achieves significant cost-performance advantages over multi-fabric networks. Standard block and file access protocols can leverage RDMA for high-performance storage access: NVMe over Fabric offloads for the target machine</li> <li>BlueField-3 DPU may operate as a co-processor offloading specific storage tasks from the host, isolating part of the storage media from the host, or enabling abstraction of software-defined storage logic using the NVIDIA BlueField-3 Arm cores. On the storage initiator side, NVIDIA BlueField-3 DPU can prove an efficient solution for hyper-converged systems to enable the host CPU to focus on compute while all the storage interface is handled through the Arm cores.</li> </ul> |
| <b>NVMe-oF</b>   | Non-volatile Memory Express (NVMe) over Fabrics is a protocol for communicating block storage IO requests over RDMA to transfer data between a host computer and a target solid-state storage device or system over a network. NVIDIA BlueField-3 DPU may operate as a co-processor offloading specific storage tasks from the host using its powerful NVMe over Fabrics Offload accelerator.  |
| <b>SR-IOV</b>  | NVIDIA DPU SR-IOV technology provides dedicated adapter resources and guaranteed isolation and protection for virtual machines (VM) within the server.   |
| <b>High-Performance Accelerations</b>                          | <ul style="list-style-type: none"> <li>Tag Matching and Rendezvous Offloads</li> <li>Adaptive Routing on Reliable Transport</li> <li>Burst Buffer Offloads for Background Checkpointing</li> </ul>   |
| <b>GPU Direct</b>  | GPUDirect RDMA is a technology that provides a direct P2P (Peer-to-Peer) data path between the GPU Memory directly to/from the NVIDIA HCA devices. This provides a significant decrease in GPU-GPU communication latency and completely offloads the CPU, removing it from all GPU-GPU communications across the network. NVIDIA DPU uses high-speed DMA transfers to copy data between P2P devices resulting in more efficient system applications  |
| <b>Isolation</b>   | BlueField-3 DPU functions as a “computer-in-front-of-a-computer,” unlocking unlimited opportunities for custom security applications on its Arm processors, fully isolated from the host’s CPU. In the event of a compromised host, BlueField-3 may detect/block malicious activities in real-time and at wire speed to prevent the attack from spreading further.   |
| <b>Cryptography Accelerations</b>                              | From IPsec and TLS data-in-motion inline encryption to AES-XTS block-level data-at-rest encryption and public key acceleration, BlueField-3 DPU hardware-based accelerations offload the crypto operations and free up the CPU, reducing latency and enabling scalable crypto solutions. BlueField-3 “host-unaware” solutions may transmit and receive data, while BlueField-3 acts as a bump-in-the-wire for crypto.  |
| <b>Securing Workloads</b>                                      | BlueField-3 DPU accelerates connection tracking with its ASAP2 technology to enable stateful filtering on a per-connection basis. Moreover, BlueField-3 includes a Titan IC regular expression (RXP) acceleration engine supported by IDS/IPS tools to detect host introspection and Application Recognition (AR) in real-time.  |

| Feature                       | Description   |
|-------------------------------|---|
| <b>Security Accelerators</b>  | A consolidated compute and network solution based on DPU achieves significant advantages over a centralized security server solution. Standard encryption protocols and security applications can leverage NVIDIA BlueField-3 compute capabilities and network offloads for security application solutions such as Layer4 Statefull Firewall.   |
| <b>Virtualized Cloud</b>      | By leveraging BlueField-3 DPU virtualization offloads, data center administrators can benefit from better server utilization, allowing more virtual machines and more tenants on the same hardware, while reducing the TCO and power consumption  |
| <b>Out-of-Band Management</b> | The NVIDIA BlueField-3 DPU incorporates a 1GbE RJ45 out-of-band port that allows the network operator to establish trust boundaries in accessing the management function to apply it to network resources. It can also be used to ensure management connectivity (including the ability to determine the status of any network component) independent of the status of other in-band network components.  |
| <b>BMC</b>                    | Some BlueField-3 DPUs incorporate local NIC BMC (Baseboard Management Controller) hardware on the board. The BMC SoC (system on a chip) can utilize either shared or dedicated NICs for remote access. The BMC node enables remote power cycling, board environment monitoring, BlueField-3 chip temperature monitoring, board power and consumption monitoring, and individual interface resets. The BMC also supports the ability to push a bootstream to BlueField-3.<br>Having a trusted on-board BMC that is fully isolated for the host server ensures highest security for the DPU boards. |

# BlueField DPU Administrator Quick Start Guide

This page is tailored for system administrators wishing to install BlueField and perform sample administrative actions on it. For a quick start guide aimed at software developers wishing to develop applications on the BlueField DPU using the DOCA framework, please refer to the [NVIDIA DOCA Developer Quick Start Guide](#).



Not sure which guide to follow? For more details on the different BlueField user types, please refer to the [NVIDIA BlueField and DOCA User Types](#) document.

## Verifying DPU Connection and Setting Up Host Environment

This section takes you through the basic steps of installing BlueField DPU and performing a sample administrative task on it.

1. Install your DPU into your host server according to the instructions under [Hardware Installation](#).



Ensure your host OS is included in the [supported operating systems](#) list and that the BlueField's out-of-band (OOB) management interface is connected to the network. The OOB interface must be connected to a DHCP/DNS server. The MAC address of the OOB port is found [on the sticker](#) on the BlueField DPU.

2. Verify that the host server correctly identifies the BlueField DPU. The following commands rescan the PCIe bus and list the BlueField's name and PCIe address:

```
# sudo update-pciids
# sudo lspci | grep BlueField
```

The list of identified devices should include a network controller for every physical (Ethernet) port and a DMA controller for DPU management. Expected output example:

```
17:00.0 Ethernet controller: Mellanox Technologies MT43244 BlueField-3 integrated ConnectX-7 network controller (rev 01)
17:00.1 Ethernet controller: Mellanox Technologies MT43244 BlueField-3 integrated ConnectX-7 network controller (rev 01)
17:00.2 DMA controller: Mellanox Technologies MT43244 BlueField-3 SoC Management Interface (rev 01)
```

3. If an older DOCA software version is installed on your host, make sure to uninstall it before proceeding with the installation of the new version:
  - For Ubuntu/Debian:

```
$ for f in $( dpkg --get-selections | grep doca | awk '{print $2}' ); do echo $f ; apt remove --purge $f -y ; done
$ sudo apt-get autoremove
```

- For CentOS/RHEL/Rocky:

```
host# for f in $(rpm -qa |grep -i doca ) ; do yum -y remove $f; done
host# yum autoremove
host# yum makecache
```

4. Download and install the latest "DOCA for Host" package compatible with your specific operating system and version listed [here](#) under the "BlueField Drivers" tab.

 Make sure to accept cookies from the website when prompted.

At this stage the host environment is all set and you can now perform administrative tasks on the DPU.

## Connecting to BlueField and Verifying Version

To connect to your DPU:


1. SSH to the DPU using the OOB IP or the RShim IP (192.168.100.2) using the default credentials (ubuntu/ubuntu).
2. When logging into the DPU for the first time after installing the BFB, you must change the default password.

```
WARNING: Your password has expired.
You must change your password now and login again!
Changing password for ubuntu.
Current password:
New password:
```

3. To check the current running BFB:

```
dpu# sudo cat /etc/mlnx-release
```

## Updating BlueField BFB Image

 These instructions are tailored for installing the BlueField BFB image on the default Ubuntu OS. To install it on other OSs, please contact [NVIDIA Support](#).

The BlueField BFB image includes all the DOCA packages.

1. Installing a new BFB on the DPU is performed using the `bfb-install` utility that is included in the RShim tool.

```
# bfb-install --bfb <BFB-image>.bfb --rshim rshim0
```

Expected output example:

```
Pushing bfb
Collecting BlueField booting status. Press Ctrl+C to stop...
INFO[BL2]: start
...
INFO[MISC]: Ubuntu installation started
INFO[MISC]: Installation finished
INFO[MISC]: Rebooting...
```

2. Upgrade the firmware of the BlueField DPU:
  - a. Upgrade the BlueField DPU's firmware:

```
dpu# sudo /opt/mellanox/mlnx-fw-updater/mlnx_fw_updater.pl --force-fw-update
```

Expected output example:

```
Device #1:
-----
Device Type:      BlueField-3  [...]
Versions:         Current      Available
                  <Old_FW_ver> <New_FW_ver>
FW               [...]
Done
```

- b. Power cycle the host for the changes to take effect.
3. Verify that the BFB has been installed and the firmware has been upgraded successfully by accessing the DPU again:
  - a. SSH to the BlueField DPU from the host using OOB IP or RShim IP:

```
ssh <ip>
```

- b. Check the versions of the DPU image and firmware:

```
# sudo bfvcheck
```

Expected output example:

```
Beginning version check...

-RECOMMENDED VERSIONS-
ATF: v2.2(release):4.0.3-3-g886241c
UEFI: 4.0.3-1-g2162ecf
FW: 32.37.1300

-INSTALLED VERSIONS-
ATF: v2.2(release):4.0.3-3-g886241c
UEFI: 4.0.3-1-g2162ecf
FW: 32.37.1300

Version check complete.
No issues found.
```

## Additional Reading

To learn more about BlueField please see:

- [BlueField hardware troubleshooting](#)
- [BlueField software installation](#)
- [BlueField software troubleshooting](#)



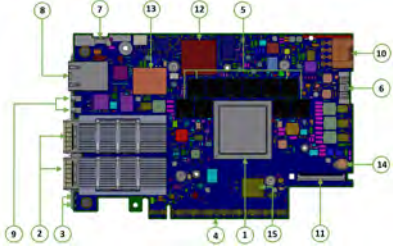
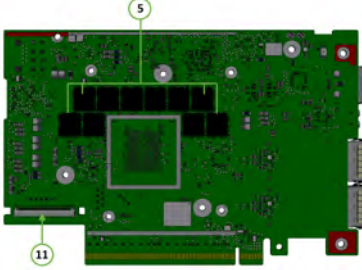
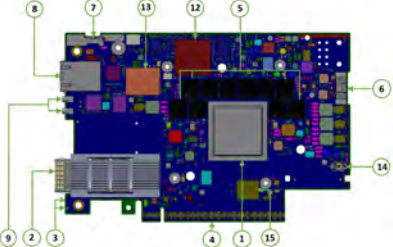
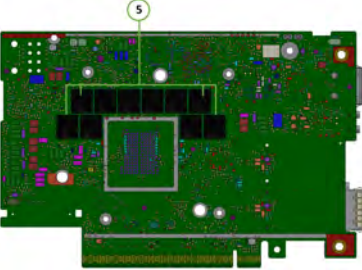
# Supported Interfaces

This section describes the DPU-supported interfaces. Each numbered interface referenced in the figures is described in the following table with a link to detailed information.



The below figures are for illustration purposes only and might not reflect the current revision of the DPU.

## FHHL DPU Layout and Interface Information

| OPN  | DPU Component Side   | DPU Print Side  |
|--|--|---|
| 900-9D3B6-00CC-EA0<br>900-9D3B6-00SC-EA0<br>900-9D3B6-00CV-AA0<br>900-9D3B6-00SV-AA0<br>900-9D3B6-00CC-AA0<br>900-9D3B6-00SC-AA0<br>900-9D3B6-00CN-AB0<br>900-9D3B6-00SN-AB0 |   |   |
| 900-9D3B4-00EN-EA0<br>900-9D3B4-00PN-EA0   |  |  |

| Item | Interface                                       | Description   |
|------|---|---|
| 1    | <a href="#">DPU System on Chip</a>              | <ul style="list-style-type: none"> <li>• <b>BlueField-3 P-Series</b> - 16 Arm-Cores - 560MHz/2133MHz</li> <li>• <b>BlueField-3 E-Series</b> - 8 Arm-Cores - 505MHz/2000MHz</li> </ul>   |
| 2    | <a href="#">Networking Interface</a>            | The network traffic is transmitted through the DPU QSFP112 connectors. The QSFP112 connectors allow the use of modules and optical and passive cable interconnect solutions   |
| 3    | <a href="#">Networking Ports LEDs Interface</a> | One bi-color I/O LEDs <b>per port</b> to indicate link and physical status  |
| 4    | <a href="#">PCI Express Interface</a>           | PCIe Gen 5.0 through an x16 edge connector  |
| 5    | <a href="#">DDR5 SDRAM On-Board Memory</a>      | Single-Channel Cards: 10 units of DDR5 SDRAM for a total of 16GB @ 5600MT/s 64bit + 8bit ECC, solder-down memory<br>Dual-Channel Cards: 20 units of DDR5 SDRAM for a total of 32GB @ 5600MT/s. 128bit + 16bit ECC, solder-down memory |

| Item | Interface  | Description   |
|------|--|---|
| 6    | <a href="#">NC-SI Management Interface</a>           | NC-SI 20 pins BMC connectivity for remote management  |
| 7    | <a href="#">USB 4-pin RA Connector</a>               | Used for OS image loading   |
| 8    | <a href="#">1GbE OOB Management Interface</a>        | 1GbE BASE-T OOB management interface  |
| 9    | <a href="#">MMCX RA PPS IN/OUT</a>                   | Allows PPS IN/OUT   |
| 10   | <a href="#">External PCIe Power Supply Connector</a> | An external 12V power connection through an 8-pin ATX connector   |
| 11   | <a href="#">Cabline CA-II Plus Connectors</a>        | Two Cabline CA-II plus connectors are populated to allow connectivity to an additional PCIe x16 Auxiliary card<br>Applies to OPNs: Applies to OPNs 900-9D3B6-00CV-AA0, 900-9D3B6-00SV-AA0, 900-9D3B6-00CC-AA0, 900-9D3B6-00SC-AA0, 900-9D3B6-00CN-AB0, 900-9D3B6-00SN-AB0 |
| 12   | <a href="#">Integrated BMC</a>                       | DPU BMC   |
| 13   | <a href="#">SSD Interface</a>                        | 128GB   |
| 14   | <a href="#">RTC Battery</a>                          | Battery holder for RTC  |
| 15   | <a href="#">eMMC</a>                                 | x8 NAND flash   |

## Interfaces Detailed Description

### DPU SoC (System on Chip)

NVIDIA® BlueField®-3 DPU is a family of advanced DPU IC solutions that integrate a coherent mesh of 64-bit Armv8.2+ A78 Hercules cores, an NVIDIA® ConnectX®-7 network adapter front-end, and a PCI Express switch into a single chip. The powerful DPU IC architecture includes an Armv multicore processor array, enabling customers to develop sophisticated applications and highly differentiated feature sets. Leverages the rich Arm software ecosystem and introduces the ability to offload the x86 software stack.

At the heart of BlueField-3, the ConnectX-7 network offload controller with RDMA and RDMA over Converged Ethernet (RoCE) technology delivers cutting-edge performance for networking and storage applications such as NVMe over Fabrics. Advanced features include an embedded virtual switch with programmable access lists (ACLs), transport offloads, and stateless encaps/decaps of NVGRE, VXLAN, and MPLS overlay protocols.


### Encryption



Applies to Crypto enabled OPNs.

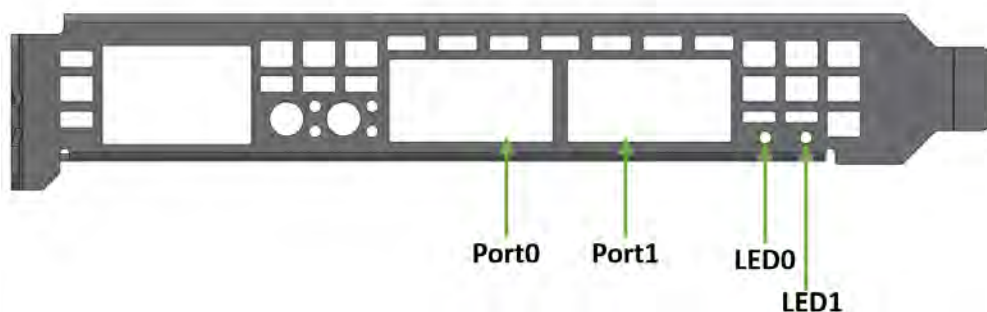
DPU addresses the concerns of modern data centers by combining hardware encryption accelerators with embedded software and fully integrated advanced network capabilities, making it an ideal platform for developing proprietary security applications. It enables a distributed security architecture by isolating and protecting each workload and providing flexible control and visibility at the server and workload level; controlling risk at the server access layer builds security into the DNA of the data center and enables prevention, detection, and response to potential threats in real-time. DPU can deliver powerful functionality, including encryption of data-in-motion, bare-metal provisioning, stateful L4 firewall, and more.

## Networking Interface

 The DPU includes special circuits to protect the card/server from ESD shocks when plugging copper cables.



The network ports are compliant with the InfiniBand Architecture Specification, Release 1.5. InfiniBand traffic is transmitted through the cards' QSFP112 connectors.

## Networking Ports LEDs Interface



One bicolor (Yellow and Green) I/O LED per port indicates speed and link status.

### Link Indications

| State  | Bi-Color LED (Yellow/Green)  |   |
|--|--|---|
| Beacon command for locating the adapter card | 1Hz blinking Yellow  |  |
| Error  | 4Hz blinking Yellow Indicates an error with the link. The error can be one of the following: |   |
|  | Error Type   | Description   |
|  | I <sup>2</sup> C   | I <sup>2</sup> C access to the networking ports fails                                 |
|  | Over-current   | Over-current condition of the networking ports  |
|  |  | LED Behavior  |
|  |  | Blinks until error is fixed   |
|  |  | Blinks until error is fixed   |
|  |  |  |

| State                              | Bi-Color LED (Yellow/Green) |   |
|------------------------------------|-----------------------------|---|
| Physical Activity                  | Blinking Green              |  |
| Link Up                            | Solid Green                 |  |
| Physical Up (InfiniBand Mode Only) | Solid Yellow                |  |

## PCI Express Interface

The DPU supports PCI Express Gen 5.0/4.0 through x16 edge connectors. Some cards allow connectivity to an additional PCIe x16 Auxiliary card through the Cabline CA-II Plus connectors.

The following lists PCIe interface features:

- PCIe Gen 5.0, 4.0, 3.0, 2.0 and 1.1 compatible
- 2.5, 5.0, or 8.0, 16.0 or 32.0 GT/s link rate x16 lanes
- Auto-negotiates to x16, x8, x4, x2, or x1

## DDR5 SDRAM On-Board Memory

The DPUs incorporate 10 or 20 units of DDR5 SDRAM. See the following table for DDR5 SDRAM memory specifications per ordering part number.

| OPNs   | DDR5 SDRAM On-Board Memory  |
|--|---|
| 900-9D3B4-00EN-EA0<br>900-9D3B4-00PN-EA0   | Single-channel with 10 DDR5 + ECC (64bit + 8bit ECC) for a total of 16GB @ 5200MT/s |
| 900-9D3B6-00CC-EA0<br>900-9D3B6-00SC-EA0   | Dual-channel with 20 DDR5 + ECC (128bit + 16bit ECC) for a total of 32GB @ 5200MT/s |
| 900-9D3B6-00CV-AA0<br>900-9D3B6-00SV-AA0<br>900-9D3B6-00CC-AA0<br>900-9D3B6-00SC-AA0<br>900-9D3B6-00CN-AB0<br>900-9D3B6-00SN-AB0 | Dual-channel with 20 DDR5 + ECC (128bit + 16bit ECC) for a total of 32GB @ 5600MT/s |

## NC-SI Management Interface

The DPU enables the connection of a Baseboard Management Controller (BMC) to a set of Network Interface Controller (NICs) to enable out-of-band remote manageability. The NC-SI management is supported over RMII and has a connector on the DPU. Please refer to [NC-SI Management Interface](#) for pins.

## UART Interface Connectivity

A UART debug interface is available on DPU cards via a 20-pin NC-SI connector. For DPUs without onboard BMC hardware, the UART interface is that of the BlueField-3 device. For DPUs with onboard BMC hardware, the UART interface is that of the NIC BMC device. The connectivity for both cases is shown in the following table:

| NC-SI Connector Pin # | Signal on DPU without BMC | Signal on DPU with BMC |
|-----------------------|---------------------------|------------------------|
| 14                    | BF_UART0_RX               | BMC_RX5                |
| 16                    | BF_UART0_TX               | BMC_TX5                |
| 12                    | GND                       | GND                    |

The UART interface is compliant with the TTL 3.3V voltage level. Use a USB-to-UART cable that supports TTL voltage levels to connect the UART Interface for Arm console access.



It is prohibited to connect any RS-232 cable directly! Only TTL 3.3V voltage level cables are supported.



Do not use the USB-to-UART cable for NC-SI management purposes.

## USB 4-pin RA Connector

The USB 4-pin RA USB connector is used to load operating system images. Use a 4-pin male connector to a male Type-A cable to connect to the board.



The male connector to the male Type-A cable is not included in the shipped DPU card box and should be ordered separately as part of the accessories kit (P/N: MBF35-DKIT).

## 1GbE OOB Management Interface

The DPU incorporates a 1GbE RJ45 out-of-band port that allows the network operator to establish trust boundaries in accessing the management function to apply it to network resources. It can also be used to ensure management connectivity (including the ability to determine the status of any network component) independent of other in-band network components' status.



For DPUs with integrated BMC: 1GbE OOB Management can be performed via the integrated BMC.

## 1GbE OOB Management LEDs Interface

Two OOB management LEDs, one Green and one Yellow, behave as described in the table below.

| Green LED | Yellow LED | Link/Activity                  |
|-----------|------------|--------------------------------|
| OFF       | OFF        | Link off                       |
| ON        | OFF        | 1 Gb/s link / No activity      |
| Blinking  | OFF        | 1 Gb/s link / Activity (RX,TX) |
| OFF       | ON         | Not supported                  |
| OFF       | Blinking   |                                |
| ON        | ON         |                                |
| Blinking  | Blinking   |                                |

## PPS IN/OUT Interface

The DPU incorporates an integrated Hardware Clock (PHC) that allows the DPU to achieve sub-20u Sec accuracy and also offers many timing-related functions such as time-triggered scheduling or time-based SND accelerations (time-based ASAP<sup>2</sup>). Furthermore, 5T technology enables the software application to transmit fronthaul (ORAN) at high bandwidth. The PTP part supports the subordinate clock, master clock, and boundary clock.

The DPU PTP solution allows you to run any PTP stack on your host.

With respect to testing and measurements, selected NVIDIA DPUs allow you to use the PPS-out signal from the onboard MMCX RA connector. The DPU also allows measuring PTP in scale with the PPS-In signal. The PTP HW clock on the Network adapter is sampled on each PPS-In signal, and the timestamp is sent to the SW.

## External PCIe Power Supply Connector



Applies to following DPUs only: 900-9D3B6-00CC-EA0, 900-9D3B6-00SC-EA0, 900-9D3B6-00CV-AA0, 900-9D3B6-00SV-AA0, 900-9D3B6-00CC-AA0, 900-9D3B6-00SC-AA0, 900-9D3B6-00CN-AB0 and 900-9D3B6-00SN-AB0.

The external ATX power cable is not supplied with the DPU package; however, this is a standard cable usually available in servers.

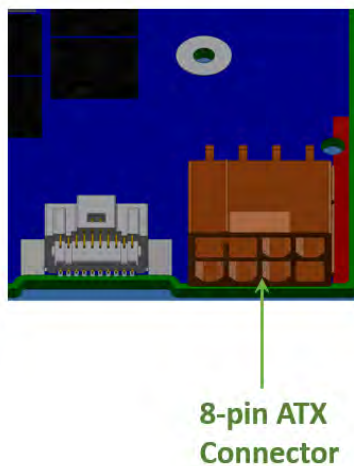


To power-up the DPU, power the ATX power supply and the PCIe golden fingers simultaneously. Failure to do so may harm the DPU. For more information, refer to [DPU Power-Up Instructions](#).

The FHHL P-Series DPUs incorporate an external 12V power connection through an ATX 8-pin PCI connector (Molex 455860005). The DPU includes a special circuitry that provides current balancing between the two power supplies; the 12V from the PCIe x16 standard slot and the 12V from the ATX 8-pin connector. Since the power provided by the PCIe golden fingers is limited to 75W, a total maximum of up to 150W is enabled through the ATX 8-pin connector and the PCIe x16 golden fingers (the ATX 8-pin connector draws its power from the server and can supply up to 150W, per ATX specifications).

The maximum power consumption which does not exceed 150W, is in accordance with the mode of operation of the DPU, and is split between the two power sources as follows:

- Up to 66W from the PCIe golden fingers (12V)
- The rest of the consumed power is drawn from the external PCIe power supply connector



Please refer to [External PCIe Power Supply Connector Pins](#) for the external PCIe power supply pins.

## Cabline CA-II Plus Connectors



Applies to OPNs: 900-9D3B6-00CC-EA0, 900-9D3B6-00SC-EA0, 900-9D3B6-00CV-AA0, 900-9D3B6-00SV-AA0, 900-9D3B6-00CC-AA0, 900-9D3B6-00SC-AA0, 900-9D3B6-00CN-AB0 and 900-9D3B6-00SN-AB0.


The Cabline CA-II connectors on the DPU enable connectivity to an additional PCIe x16 bus in addition to the PCIe x16 bus available through the golden-fingers. The Cabline CA-II Plus connectors allow connectivity to flash cards and NVMe SSD drives.

Specific applications have an interest in direct connectivity to the far end of the Cabline CA-II cables, through the two 60-pin Cabline CA-II connectors, directly to the motherboard, in order to cut the insertion loss and/or the additional space associated with a PCIe x16 Flash Auxiliary Board.

The Cabline CA-II connectors mate with two 60-pin Cabline CA-II cables that can be distinguished by their black or white external insulators and connector pinouts. The black Cabline CA-II cable mates with the DPU's component (top) side, whereas the white Cabline CA-II cable mates with the DPU print (bottom) side. The Cabline CA-II cables are offered in three standard lengths; 150mm, 350mm, and 550mm.


For connector pinouts, please refer to [Cabline CA-II Plus Connectors Pinouts](#).

## Integrated BMC Interface

 The BMC Interface applies to DPUs with integrated BMC only.

The DPU incorporates an onboard integrated NIC BMC and an Ethernet switch. The BMC becomes available once the host server powers up the card. The NIC BMC can control the DPU's power and enables DPU shutdown and power-up.

## NVMe SSD Interface

 The Self Encrypting Disk (SED) capability is not supported.

The NVMe SSD interface is used for storing the user applications and logs. The NVMe SSD interface size is 128GB.

## RTC Battery

The DPU incorporates a Coin type Lithium battery CR621 for RTC (Real Time Clock).

## eMMC Interface

The eMMC is an x8 NAND flash used for Arm boot and operating system storage. Memory size is 128GB, where it is effectively pSLC 40GB.



# Pinouts Description

## PCI Express Interface

The following table lists the PCI Express pins description. For further details, please refer to [PCI Express Interface](#).

DPU PCI Express x16 Pin Description

| Pin # | Signal Name | Description  | Pin # | Signal Name | Description  |
|-------|-------------|--|-------|-------------|--|
| A1    | PRSNT1#     | Mechanical Present   | B1    | 12V         |  |
| A2    | 12V         |  | B2    | 12V         |  |
| A3    | 12V         |  | B3    | 12V         |  |
| A4    | GND         |  | B4    | GND         |  |
| A5    | TCK         | JTAG - Not Connected   | B5    | SMCLK       | Host SMBus   |
| A6    | TDI         | JTAG - Not Connected   | B6    | SMDAT       | Host SMBus   |
| A7    | TDO         | JTAG - Not Connected   | B7    | GND         |  |
| A8    | TMS         | JTAG - Not Connected   | B8    | 3.3V        | 3.3V - (Connected in 900-9D3B4-00CC-EA0 & 900-9D3B4-00SC-EA0 only) |
| A9    | 3.3V        | 3.3V - (Connected in 900-9D3B4-00CC-EA0 & 900-9D3B4-00SC-EA0 only) | B9    | TRST#       | JTAG - Not Connected   |
| A10   | 3.3V        | 3.3V - (Connected in 900-9D3B4-00CC-EA0 & 900-9D3B4-00SC-EA0 only) | B10   | 3.3V_AUX    |  |
| A11   | PERST#      | PCIe Reset   | B11   | WAKW#/RSVD  |  |
| A12   | GND         |  | B12   | RSVD        |  |
| A13   | REFCLK+     | Host Reference Clock   | B13   | GND         |  |
| A14   | REFCLK-     | Host Reference Clock   | B14   | PETP0       |  |
| A15   | GND         |  | B15   | PETN0       |  |
| A16   | PERP0       |  | B16   | GND         |  |
| A17   | PERN0       |  | B17   | RSVD        |  |
| A18   | GND         |  | B18   | GND         |  |
| A19   | RSVD        |  | B19   | PETP1       |  |
| A20   | GND         |  | B20   | PETN1       |  |
| A21   | PERP1       |  | B21   | GND         |  |
| A22   | PERN1       |  | B22   | GND         |  |
| A23   | GND         |  | B23   | PETP2       |  |
| A24   | GND         |  | B24   | PETN2       |  |
| A25   | PERP2       |  | B25   | GND         |  |
| A26   | PERN2       |  | B26   | GND         |  |
| A27   | GND         |  | B27   | PETP3       |  |
| A28   | GND         |  | B28   | PETN3       |  |

| Pin # | Signal Name | Description | Pin # | Signal Name | Description |
|-------|-------------|-------------|-------|-------------|-------------|
| A29   | PERP3       |             | B29   | GND         |             |
| A30   | PERN3       |             | B30   | RSVD        |             |
| A31   | GND         |             | B31   | RSVD        |             |
| A32   | RSVD        |             | B32   | GND         |             |
| A33   | RSVD        |             | B33   | PETP4       |             |
| A34   | GND         |             | B34   | PETN4       |             |
| A35   | PERP4       |             | B35   | GND         |             |
| A36   | PERN4       |             | B36   | GND         |             |
| A37   | GND         |             | B37   | PETP5       |             |
| A38   | GND         |             | B38   | PETN5       |             |
| A39   | PERP5       |             | B39   | GND         |             |
| A40   | PERN5       |             | B40   | GND         |             |
| A41   | GND         |             | B41   | PETP6       |             |
| A42   | GND         |             | B42   | PETN6       |             |
| A43   | PERP6       |             | B43   | GND         |             |
| A44   | PERN6       |             | B44   | GND         |             |
| A45   | GND         |             | B45   | PETP7       |             |
| A46   | GND         |             | B46   | PETN7       |             |
| A47   | PERP7       |             | B47   | GND         |             |
| A48   | PERN7       |             | B48   | RSVD        |             |
| A49   | GND         |             | B49   | GND         |             |
| A50   | RSVD        |             | B50   | PETP8       |             |
| A51   | GND         |             | B51   | PETN8       |             |
| A52   | PERP8       |             | B52   | GND         |             |
| A53   | PERN8       |             | B53   | GND         |             |
| A54   | GND         |             | B54   | PETP9       |             |
| A55   | GND         |             | B55   | PETN9       |             |
| A56   | PERP9       |             | B56   | GND         |             |
| A57   | PERN9       |             | B57   | GND         |             |
| A58   | GND         |             | B58   | PETP10      |             |
| A59   | GND         |             | B59   | PETN10      |             |
| A60   | PERP10      |             | B60   | GND         |             |
| A61   | PERN10      |             | B61   | GND         |             |
| A62   | GND         |             | B62   | PETP11      |             |
| A63   | GND         |             | B63   | PETN11      |             |
| A64   | PERP11      |             | B64   | GND         |             |
| A65   | PERN11      |             | B65   | GND         |             |
| A66   | GND         |             | B66   | PETP12      |             |
| A67   | GND         |             | B67   | PETN12      |             |
| A68   | PERP12      |             | B68   | GND         |             |
| A69   | PERN12      |             | B69   | GND         |             |

| Pin # | Signal Name | Description | Pin # | Signal Name | Description        |
|-------|-------------|-------------|-------|-------------|--------------------|
| A70   | GND         |             | B70   | PETP13      |                    |
| A71   | GND         |             | B71   | PETN13      |                    |
| A72   | PERP13      |             | B72   | GND         |                    |
| A73   | PERN13      |             | B73   | GND         |                    |
| A74   | GND         |             | B74   | PETP14      |                    |
| A75   | GND         |             | B75   | PETN14      |                    |
| A76   | PERP14      |             | B76   | GND         |                    |
| A77   | PERN14      |             | B77   | GND         |                    |
| A78   | GND         |             | B78   | PETP15      |                    |
| A79   | GND         |             | B79   | PETN15      |                    |
| A80   | PERP15      |             | B80   | GND         |                    |
| A81   | PERN15      |             | B81   | PRSNT2#     | Mechanical Present |
| A82   | GND         |             | B82   | GND         |                    |

## External Power Supply Connector

The following table provides the External Power Supply pins of the external power supply interfaces on the DPU. For further details, please refer to [External PCIe Power Supply Connector](#).



The mechanical pinout of the 8-pin external +12V power connector is shown below. The +12V connector is a GPU power PCIe standard connector. Care should be taken to ensure the power is applied to the correct pins as some 8-pin ATX-type connectors can have different pinouts.

| Pin Number | Description |
|------------|-------------|
| 1          | 12V         |
| 2          | 12V         |
| 3          | 12V         |
| 4          | Sense1      |
| 5          | GND         |
| 6          | Sense0      |
| 7          | GND         |
| 8          | GND         |

## NC-SI Management Interface

The following table list the NC-SI management interface pinout descriptions. For further details, please refer to [NC-SI Management Interface](#).

| Pin# | Signal Name   | I/O                       | Signal Description  |
|------|---------------|---------------------------|---|
| 1    | GND           | GND                       | Ground  |
| 2    | PKG_ID1       | Input (to BlueField-3)    | NC-SI PKG_ID<br>Should be connected to the Primary controller NC-SI PKG_ID pins to set the appropriate package ID.<br>PKG_ID0 should be connected to the endpoint device GPIO associated with Package ID[0]. PKG_ID1 should be associated with Package ID[1].<br>Baseboard should connect to GND or leave floating.<br>DPU should have a 4.7k PU.   |
| 3    | RBT_RXD0      | Output (from BlueField-3) | Receive data. Data signals from the network controller to the BMC.<br>For baseboards, this pin should be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 kΩ pull down resistor to GND on the baseboard between the BMC and the RBT isolator to prevent the signal from floating when no card is installed.<br>For DPUs, this pin should be connected between the connector and the RBT PHY. External termination determined by the DPU RBT PHY requirements.   |
| 4    | RBT_REF_CLK   | Input                     | RBT Reference clock. Synchronous clock reference for receive, transmit and control interface. The clock should have a typical frequency of 50MHz ±50 ppm.<br>For baseboards, this pin should be connected between the baseboard NC-SI over RBT PHY and the DPU cable connector. The RBT_REF_CLK should not be driven until 3.3V AUX is present on the DPU. The RBT_REF_CLK should be continuous once it has started.<br>For DPUs, this pin should be connected between the connector and the RBT PHY. No external termination is required.                          |
| 5    | RBT_RXD1      | Output                    | Receive data. Data signals from the network controller to the BMC.<br>For baseboards, this pin should be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 kΩ pull down resistor to GND on the baseboard between the BMC and the RBT isolator to prevent the signal from floating when no card is installed.<br>For DPUs, this pin should be connected between the connector and the RBT PHY. External termination determined by the DPU RBT PHY requirements.   |
| 6    | GND           | GND                       | Ground  |
| 7    | RBT_CRS_DV    | Output                    | Carrier sense/receive data valid. This signal is used to indicate to the baseboard that the carrier sense/receive data is valid.<br>For baseboards, this pin should be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 kΩ pull down resistor on the baseboard between the BMC and the RBT isolator to prevent the signal from floating when no DPU is installed.<br>For DPUs, this pin should be connected between the connector and the RBT PHY. External termination determined by the DPU RBT PHY requirements. |
| 8    | RBT_ISOLATE_N | Output                    | This signal is used to indicate the DPU has powered and is ready for NC-SI physical layer connection to be present. When low the baseboard circuitry will isolate the NC-SI connection to the DPU. When high normal NC-SI RBT connectivity is available.<br>Baseboards should terminate this with a 47K-100K PD resistor.<br>DPUs should terminate with a 10k PU resistor.  |
| 9    | GND           | GND                       | Ground  |
| 10   | PKG_ID0       | Input                     | NC-SI PKG_ID<br>should be connected to the Primary controller NC-SI PKG_ID pins to set the appropriate package ID.<br>PKG_ID0 should be connected to the endpoint device GPIO associated with Package ID[0]. PKG_ID1 should be associated with Package ID[1].<br>Baseboard should connect to GND or leave floating.<br>DPU should have a 4.7k PU.   |

| Pin# | Signal Name | I/O    | Signal Description  |
|------|-------------|--------|---|
| 11   | RBT_TX_EN   | Input  | Transmit enable.<br>For baseboards, this pin should be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 k $\Omega$ pull down resistor to ground on the baseboard between the RBT isolator and the DPU cable connector to prevent the card-side signals from floating when the RBT signals are isolated.<br>For DPUs, this pin should be connected between the connector and the RBT PHY. External termination determined by the DPU RBT PHY requirements.   |
| 12   | GND         | GND    | Ground  |
| 13   | RBT_TXD0    | Input  | Transmit data. Data signals from the BMC to the network controller.<br>For baseboards, this pin should be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 k $\Omega$ pull down resistor to GND on the baseboard between the RBT isolator and the DPU cable connector to prevent the card-side signals from floating when the RBT signals are isolated.<br>For DPUs, this pin should be connected between the connector and the RBT PHY. External termination determined by the DPU RBT PHY requirements. |
| 14   | UART_TX     | Input  | 3.3V UART TX signal from the baseboard  |
| 15   | RBT_TXD1    | Input  | Transmit data. Data signals from the BMC to the network controller.<br>For baseboards, this pin should be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 k $\Omega$ pull down resistor to GND on the baseboard between the RBT isolator and the DPU cable connector to prevent the card-side signals from floating when the RBT signals are isolated.<br>For DPUs, this pin should be connected between the connector and the RBT PHY. External termination determined by the DPU RBT PHY requirements. |
| 16   | UART_RX     | Output | 3.3V UART RX signal to the baseboard  |
| 17   | PRESENCE_N  |        | Presence of DPU. Baseboard should implement a 200 $\Omega$ series resistor and 4.7k $\Omega$ pull-up resistor to 3.3V AUX.<br>DPU should tie this to GND.   |
| 18   | GND         | GND    | Ground  |
| 19   | RBT_ARB_OUT | Input  | NC-SI hardware arbitration output.<br>If the baseboard supports multiple DPUs cards connected to the same RBT interface, it should implement logic that connects the RBT_ARB_OUT pin of the first populated DPU card to its RBT_ARB_IN pin if it is the only card present or to the RBT_ARB_IN pin of the next populated card and so on sequentially for all cards on the specified RBT bus to ensure the arbitration ring is complete. This logic should bypass slots that are not populated or powered off.   |
| 20   | RBT_ARB_IN  | Output | NC-SI hardware arbitration input.<br>If the baseboard supports multiple DPUs cards connected to the same RBT interface, it should implement logic that connects the RBT_ARB_IN pin of the first populated DPU card to its RBT_ARB_OUT pin if it is the only card present or to the RBT_ARB_OUT pin of the next populated card and so on sequentially for all cards on the specified RBT bus to ensure the arbitration ring is complete. This logic should bypass slots that are not populated or powered off.   |

## Cabline CA-II Plus Connectors Pinouts

### Component Side

| Pin# | Signal Name     | Wire Type  | AWG# | Pin# on other end |
|------|-----------------|------------|------|-------------------|
| 1    | GND             | GND BAR    |      | 1                 |
| 2    | PCIE_REFCLK1_P  | Micro coax | 38   | 2                 |
| 3    | PCIE_REFCLK1_N  | Micro coax | 38   | 3                 |
| 4    | GND             | GND BAR    |      | 4                 |
| 5    | PCIE_CPU_CX_15N | Micro coax | 38   | 5                 |
| 6    | PCIE_CPU_CX_15P | Micro coax | 38   | 6                 |
| 7    | GND             | GND BAR    |      | 7                 |
| 8    | PCIE_CPU_CX_14N | Micro coax | 38   | 8                 |
| 9    | PCIE_CPU_CX_14P | Micro coax | 38   | 9                 |
| 10   | GND             | GND BAR    |      | 10                |
| 11   | PCIE_CPU_CX_13N | Micro coax | 38   | 11                |
| 12   | PCIE_CPU_CX_13P | Micro coax | 38   | 12                |
| 13   | GND             | GND BAR    |      | 13                |
| 14   | PCIE_CPU_CX_12N | Micro coax | 38   | 14                |
| 15   | PCIE_CPU_CX_12P | Micro coax | 38   | 15                |
| 16   | GND             | GND BAR    |      | 16                |
| 17   | PCIE_CPU_CX_11N | Micro coax | 38   | 17                |
| 18   | PCIE_CPU_CX_11P | Micro coax | 38   | 18                |
| 19   | GND             | GND BAR    |      | 19                |
| 20   | PCIE_CPU_CX_10N | Micro coax | 38   | 20                |
| 21   | PCIE_CPU_CX_10P | Micro coax | 38   | 21                |
| 22   | GND             | GND BAR    |      | 22                |
| 23   | PCIE_CPU_CX_9N  | Micro coax | 38   | 23                |
| 24   | PCIE_CPU_CX_9P  | Micro coax | 38   | 24                |
| 25   | GND             | GND BAR    |      | 25                |
| 26   | PCIE_CPU_CX_8N  | Micro coax | 38   | 26                |
| 27   | PCIE_CPU_CX_8P  | Micro coax | 38   | 27                |
| 28   | GND             | GND BAR    |      | 28                |
| 29   | PCIE_CPU_CX_7N  | Micro coax | 38   | 29                |
| 30   | PCIE_CPU_CX_7P  | Micro coax | 38   | 30                |
| 31   | GND             | GND BAR    |      | 31                |
| 32   | CIE_CPU_CX_6N   | Micro coax | 38   | 32                |
| 33   | PCIE_CPU_CX_6P  | Micro coax | 38   | 33                |
| 34   | GND             | GND BAR    |      | 34                |
| 35   | PCIE_CPU_CX_5N  | Micro coax | 38   | 35                |

| Pin# | Signal Name     | Wire Type  | AWG# | Pin# on other end |
|------|-----------------|------------|------|-------------------|
| 36   | PCIE_CPU_CX_5P  | Micro coax | 38   | 36                |
| 37   | GND             | GND BAR    |      | 37                |
| 38   | PCIE_CPU_CX_4N  | Micro coax | 38   | 38                |
| 39   | PCIE_CPU_CX_4P  | Micro coax | 38   | 39                |
| 40   | GND             | GND BAR    |      | 40                |
| 41   | PCIE_CPU_CX_3N  | Micro coax | 38   | 41                |
| 42   | PCIE_CPU_CX_3P  | Micro coax | 38   | 42                |
| 43   | GND             | GND BAR    |      | 43                |
| 44   | PCIE_CPU_CX_2N  | Micro coax | 38   | 44                |
| 45   | PCIE_CPU_CX_2P  | Micro coax | 38   | 45                |
| 46   | GND             | GND BAR    |      | 46                |
| 47   | PCIE_CPU_CX_1N  | Micro coax | 38   | 47                |
| 48   | PCIE_CPU_CX_1P  | Micro coax | 38   | 48                |
| 49   | GND             | GND BAR    |      | 49                |
| 50   | PCIE_CPU_CX_0N  | Micro coax | 38   | 50                |
| 51   | PCIE_CPU_CX_0P  | Micro coax | 38   | 51                |
| 52   | GND             | GND BAR    |      | 52                |
| 53   | I2C_DPU_BMC_SDA | Micro coax | 38   | 53                |
| 54   | I2C_DPU_BMC_SCL | Micro coax | 38   | 54                |
| 55   | AUX_PGOOD       | Micro coax | 38   | 55                |
| 56   | No wire         | Micro coax | 38   | 56                |
| 57   | I2C_AUX_SCL     | Micro coax | 38   | 57                |
| 58   | I2C_AUX_SDA     | Micro coax | 38   | 58                |
| 59   | S_PRSENT1_L     | Micro coax | 38   | 59                |
| 60   | No wire         |            |      | 60                |

## Print Side

| Pin# | Signal Name     | Wire Type  | AWG# | Pin# on other end |
|------|-----------------|------------|------|-------------------|
| 1    | SER_CLK         | Micro coax | 38   | 1                 |
| 2    | SER_CAPTURE     | Micro coax | 38   | 2                 |
| 3    | SER_DO          | Micro coax | 38   | 3                 |
| 4    | S_PERST2_CONN_L | Micro coax | 38   | 4                 |
| 5    | SER_DI          | Micro coax | 38   | 5                 |
| 6    | Reserved_06     | Micro coax | 38   | 6                 |
| 7    | Reserved_07     | Micro coax | 38   | 7                 |
| 8    | Reserved_08     | Micro coax | 38   | 8                 |
| 9    | GND             | GND BAR    |      | 9                 |
| 10   | PCIE_CPU_CX_0P  | Micro coax | 38   | 10                |

| Pin# | Signal Name     | Wire Type  | AWG# | Pin# on other end |
|------|-----------------|------------|------|-------------------|
| 11   | PCIE_CPU_CX_0N  | Micro coax | 38   | 11                |
| 12   | GND             | GND BAR    |      | 12                |
| 13   | PCIE_CPU_CX_1P  | Micro coax | 38   | 13                |
| 14   | PCIE_CPU_CX_1N  | Micro coax | 38   | 14                |
| 15   | GND             | GND BAR    |      | 15                |
| 16   | PCIE_CPU_CX_2P  | Micro coax | 38   | 16                |
| 17   | PCIE_CPU_CX_2N  | Micro coax | 38   | 17                |
| 18   | GND             | GND BAR    |      | 18                |
| 19   | PCIE_CPU_CX_3P  | Micro coax | 38   | 19                |
| 20   | PCIE_CPU_CX_3N  | Micro coax | 38   | 20                |
| 21   | GND             | GND BAR    |      | 21                |
| 22   | PCIE_CPU_CX_4P  | Micro coax | 38   | 22                |
| 23   | PCIE_CPU_CX_4N  | Micro coax | 38   | 23                |
| 24   | GND             | GND BAR    |      | 24                |
| 25   | PCIE_CPU_CX_5P  | Micro coax | 38   | 25                |
| 26   | PCIE_CPU_CX_5N  | Micro coax | 38   | 26                |
| 27   | GND             | GND BAR    |      | 27                |
| 28   | PCIE_CPU_CX_6P  | Micro coax | 38   | 28                |
| 29   | PCIE_CPU_CX_6N  | Micro coax | 38   | 29                |
| 30   | GND             | GND BAR    |      | 30                |
| 31   | PCIE_CPU_CX_7P  | Micro coax | 38   | 31                |
| 32   | PCIE_CPU_CX_7N  | Micro coax | 38   | 32                |
| 33   | GND             | GND BAR    |      | 33                |
| 34   | PCIE_CPU_CX_8P  | Micro coax | 38   | 34                |
| 35   | PCIE_CPU_CX_8N  | Micro coax | 38   | 35                |
| 36   | GND             | GND BAR    |      | 36                |
| 37   | PCIE_CPU_CX_9P  | Micro coax | 38   | 37                |
| 38   | PCIE_CPU_CX_9N  | Micro coax | 38   | 38                |
| 39   | GND             | GND BAR    |      | 39                |
| 40   | PCIE_CPU_CX_10P | Micro coax | 38   | 40                |
| 41   | PCIE_CPU_CX_10N | Micro coax | 38   | 41                |
| 42   | GND             | GND BAR    |      | 42                |
| 43   | PCIE_CPU_CX_11P | Micro coax | 38   | 43                |
| 44   | PCIE_CPU_CX_11N | Micro coax | 38   | 44                |
| 45   | GND             | GND BAR    |      | 45                |
| 46   | PCIE_CPU_CX_12P | Micro coax | 38   | 46                |
| 47   | PCIE_CPU_CX_12N | Micro coax | 38   | 47                |
| 48   | GND             | GND BAR    |      | 48                |
| 49   | PCIE_CPU_CX_13P | Micro coax | 38   | 49                |
| 50   | PCIE_CPU_CX_13N | Micro coax | 38   | 50                |
| 51   | GND             | GND BAR    |      | 51                |



| Pin# | Signal Name     | Wire Type  | AWG# | Pin# on other end |
|------|-----------------|------------|------|-------------------|
| 52   | PCIE_CPU_CX_14P | Micro coax | 38   | 52                |
| 53   | PCIE_CPU_CX_14N | Micro coax | 38   | 53                |
| 54   | GND             | GND BAR    |      | 54                |
| 55   | PCIE_CPU_CX_15P | Micro coax | 38   | 55                |
| 56   | PCIE_CPU_CX_15N | Micro coax | 38   | 56                |
| 57   | GND             | GND BAR    |      | 57                |
| 58   | S_PERST1_CONN_L | Micro coax | 38   | 58                |
| 59   | No wire         | No Wire    |      | 59                |
| 60   | S_PRST2_L       | Micro coax | 38   | 60                |

# Hardware Installation

Installation and initialization of the DPU require attention to the mechanical attributes, power specification, and precautions for electronic equipment.

## Safety Warnings

 Safety warnings are provided here in the English language.

Please observe all safety warnings to avoid injury and prevent damage to system components. Note that not all warnings are relevant to all models.

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## Installation Procedure Overview

The installation procedure of DPU involves the following steps:

| Step | Procedure   | Direct Link  |
|------|---|--|
| 1    | Check the system's requirements.                                  | Refer to <a href="#">System Requirements</a>             |
| 2    | Pay attention to the airflow consideration within the host system | Refer to <a href="#">Airflow Requirements</a>            |
| 3    | Follow the safety precautions                                     | Refer to <a href="#">Safety Precautions</a>              |
| 4    | Unpack the package  | Refer to <a href="#">Unpacking</a>                       |
| 5    | Follow the pre-installation checklist                             | Refer to <a href="#">Pre-Installation Checklist</a>      |
| 7    | Install the DPU according to the form-factor you have purchased.  | Refer to <a href="#">DPU Installation</a>                |
| 8    | Connect cables or modules to the DPU                              | Refer to <a href="#">Cables and Modules Installation</a> |
| 9    | Power-up the DPU  | Refer to <a href="#">DPU Power-Up Instructions</a>       |

## System Requirements

### Hardware Requirements

 Unless otherwise specified, products are designed to work in an environmentally controlled data center with low levels of gaseous and dust (particulate) contamination.


The operating environment should meet severity level G1 as per ISA 71.04 for gaseous contamination and ISO 14644-1 class 8 for cleanliness level.

The below table lists the motherboard and power supply requirements per DPU series.

|                      |   |
|----------------------|---|
| <b>FHHL<br/>DPUs</b> | <b>E-Series:</b> A minimum of 75W system power supply through the PCIe x16 interface (Relevant for 900-9D3B4-00EN-EA0 and 900-9D3B4-00PN-EA0)   |
|                      | <b>P-Series:</b> Require a supplementary 8-pin ATX power supply connectivity available through the external power supply connector (Relevant for OPNs: 900-9D3B6-00CV-AA0, 900-9D3B6-00SV-AA0, 900-9D3B6-00CC-AA0, 900-9D3B6-00SC-AA0, 900-9D3B6-00CN-AB0 and 900-9D3B6-00SN-AB0) |

## Airflow Requirements

DPU is offered with one airflow direction: from the heatsink to the network ports.

-  Any use of the product in the opposite airflow direction (from network ports to heatsink) must be validated thermally to ensure proper cooling of the product.

Please refer to the [Specifications](#) section for airflow numbers per DPU model.

## Software Requirements

- See [System Requirements](#) section under the Introduction section.
- Software Stacks - The DPU is shipped with Linux based Operating System burned on it which includes all needed drivers. For more information, please refer to the Software User Manual.


## Safety Precautions

The DPU being installed in a system that operates with voltages that can be lethal. Before opening the case of the system, observe the following precautions to avoid injury and prevent damage to system components.

- Remove any metallic objects from your hands and wrists.
- Make sure to use only insulated tools.
- Verify that the system is powered off and is unplugged.
- It is strongly recommended to use an ESD strap or other antistatic devices.

## Unpacking

Check against the package contents list that all the parts have been sent. Check the parts for visible damage that may have occurred during shipping. Please note that the DPUs must be placed on an antistatic surface.

-  Please note that if the DPU is removed hastily from the antistatic bag, the plastic ziplock may harm the EMI fingers on the networking connector. Carefully remove the DPU from the antistatic bag to avoid damaging the EMI fingers.

For package contents, please refer to [Package Contents](#).

## Pre-Installation Checklist

1. Verify that your system meets the hardware and software requirements stated above.
2. Shut down your system if active.  
Turn off the power to the system, and disconnect the power cord. Refer to the system documentation for instructions. Before you install the DPU, make sure that the system is disconnected from power.

## Installation Instructions

This section provides detailed instructions on how to install your DPU in a system.

Choose the installation instructions according to the DPU configuration you would like to use.

| OPNs   | Installation Instructions   |
|--|---|
| All DPUs   | <a href="#">PCIe x16 DPUs Installation Instructions</a>                       |
| 900-9D3B6-00CV-AA0<br>900-9D3B6-00SV-AA0<br>900-9D3B6-00CC-AA0<br>900-9D3B6-00SC-AA0<br>900-9D3B6-00CN-AB0<br>900-9D3B6-00SN-AB0 | <a href="#">PCIe Extension Option (2x PCIe x16) Installation Instructions</a> |

## Cables and Modules

### Networking Cable Installation

1. All cables can be inserted or removed with the unit powered on.
2. To insert a cable, press the connector into the port receptacle until the connector is firmly seated.
  - a. Support the weight of the cable before connecting the cable to the DPU. Do this by using a cable holder or tying the cable to the rack.
  - b. Determine the correct orientation of the connector to the DPU before inserting the connector. Do not try and insert the connector upside down. This may damage the DPU.
  - c. Insert the connector into the DPU. Be careful to insert the connector straight into the cage. Do not apply any torque, up or down, to the connector cage in the DPU.
  - d. Make sure that the connector locks in place.



When installing cables make sure that the latches engage.



Always install and remove cables by pushing or pulling the cable and connector in a straight line with the DPU.

3. After inserting a cable into a port, the Green LED indicator will light when the physical connection is established (that is, when the unit is powered on and a cable is plugged into the port with the other end of the connector plugged into a functioning port). See Networking Ports LEDs interface under the [Supported Interfaces](#) section.
4. After plugging in a cable, lock the connector using the latching mechanism particular to the cable vendor. When data is being transferred the Green LED will blink.
5. Make sure not to impede the air exhaust flow through the ventilation holes. Use cable lengths that allow for routing horizontally around to the side of the chassis before bending upward or downward in the rack.
6. To remove a cable, disengage the locks and slowly pull the connector away from the port receptacle. LED indicator will turn off when the cable is unseated.

## DPU Power-Up Instructions

To power-up the DPU, power the ATX power supply and the PCIe goldfinger interface simultaneously. Failure to do so may harm the DPU.

In all DPU operation states, it is important to turn on or off both the ATX power supply and the PCIe golden fingers at the same time. It is prohibited that the DPU ATX power supply is powered on while the PCIe golden-finger interface is powered-down or powered-up.

## PCIe x16 DPUs Installation Instructions

### Installation Instructions

This section provides detailed instructions on how to install your DPU in a system.



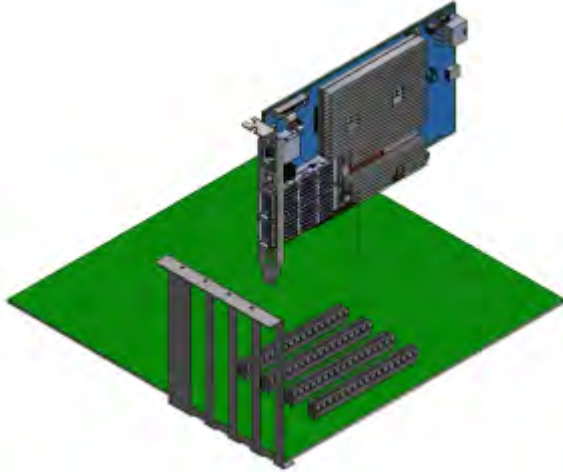
Please note that the following figures are for illustration purposes only.



To power-up the FHHL P-Series DPUs, you need to connect a PCIe external power cable. The PCIe external power cable should be supplied by the customer. Refer to [External Power Supply Connector](#) for pin descriptions.

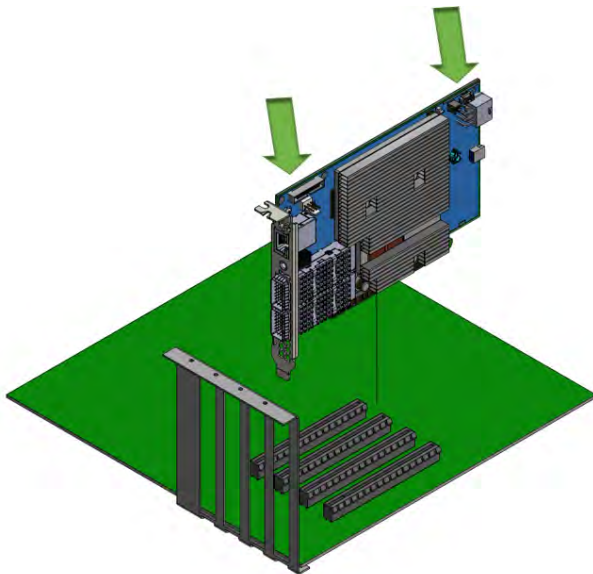
1. Open the system case.

2. Place the DPU in an available PCI Express slot.

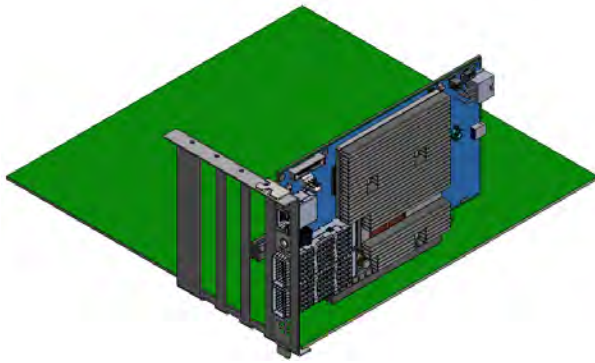


3. Applying even pressure at both corners of the card, insert the DPU into the PCI Express slot until firmly seated.

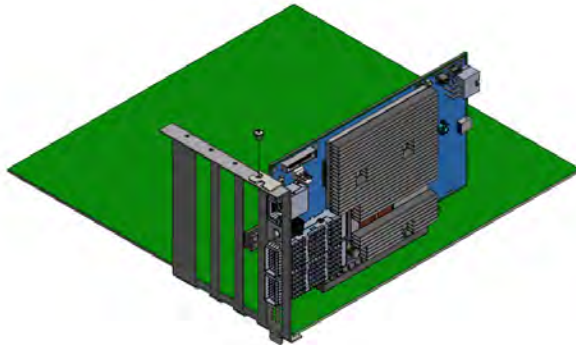
⚠ Do not use excessive force when seating the card, as this may damage the system or the DPU.



4. When the DPU is properly seated, the port connectors are aligned with the slot opening, and the DPU faceplate is visible against the system chassis.



5. Secure the DPU with the screw.



6. For the FHHL 100Gb/s P-Series DPUs, install the PCIe external power cable. Connect the 6-pin power connector from the power supply to the power connector on the top edge of the DPU. Note that the connector and socket on the graphics card have a unique shape and connect one way only.  
For further instructions, please refer to the cable vendor documentation. Please refer to the pinout description in [External Power Supply Connector](#).
7. Close the system case.
8. Install the networking cables. For instructions, please refer to [Networking Cable Installation](#).

## Uninstalling the DPU

### Safety Precautions

The DPU is installed in a system that operates with voltages that can be lethal. Before uninstalling the DPU, please observe the following precautions to avoid injury and prevent damage to system components.

1. Remove any metallic objects from your hands and wrists.
2. It is strongly recommended to use an ESD strap or other antistatic devices.
3. Turn off the system and disconnect the power cord from the server.

### Card Removal

Please note that the following images are for illustration purposes only.

1. Verify that the system is powered off and unplugged.
2. Wait 30 seconds.
3. To remove the card, disengage the retention mechanism on the bracket (screws).

4. Holding the DPU from its center, gently pull the DPU out of the PCI Express slot.
5. When the port connectors reach the top of the chassis window, gently pull the DPU in parallel to the motherboard.

## PCIe Extension Option (2x PCIe x16) Installation Instructions



This section applies to the following DPUs when used as Socket Direct cards in dual-socket servers:

- 900-9D3B6-00CV-AA0, 900-9D3B6-00SV-AA0
- 900-9D3B6-00CC-AA0, 900-9D3B6-00SC-AA0
- 900-9D3B6-00CN-AB0, 900-9D3B6-00SN-AB0
- 900-9D3B6-00CC-EA0, 900-9D3B6-00SC-EA0

For more information on the PCIe Auxiliary Kit, refer to [PCIe Auxiliary Card Kit](#).



The below images are for illustration purposes only.

The hardware installation section uses the terminology of white and black harnesses to differentiate between the two supplied cables. Due to supply chain variations, some DPUs may be supplied with two black harnesses instead. To clarify the difference between these two harnesses, one black harness was marked with a “WHITE” label and the other with a “BLACK” label.

The Cabline harness marked with a “WHITE” label should be connected to the connector on the DPU and Auxiliary PCIe card engraved with “White Cable”, while the one marked with a “BLACK” label should be connected to the connector on the DPU and Auxiliary PCIe card engraved with “Black Cable”.



The harnesses' minimal bending radius is 10[mm].

## Installing the DPU



The installation instructions include steps that involve a retention clip to be used while connecting the Cabline harnesses to the DPUs. Please note that this is an optional accessory.



Please make sure to install the DPU cards in a PCIe slot that is capable of supplying the required power and airflow as stated in [Specifications](#).

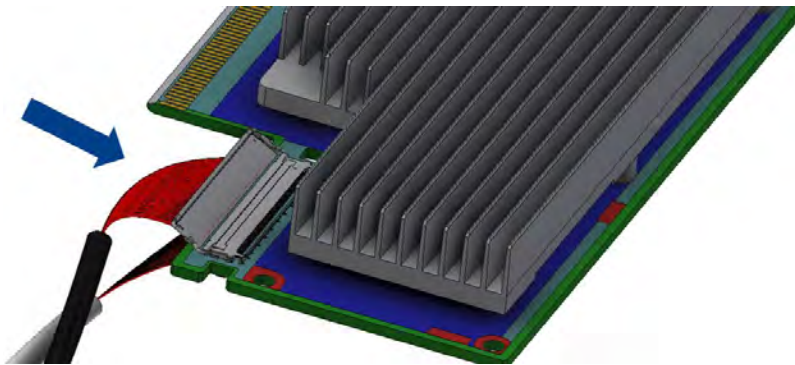
 Connect the DPU with the Auxiliary connection card using the supplied Cabline CA-II Plus harnesses.



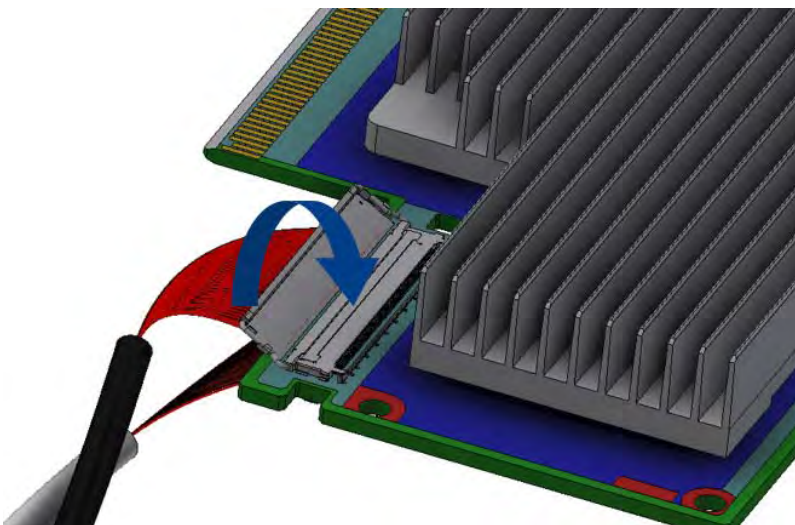
Step 1: Slide the black and white Cabline CA-II Plus harnesses through the retention clip while making sure the clip opening is facing the plugs.



Step 2: Plug the Cabline CA-II Plus harnesses on the DPU while paying attention to the color-coding. As indicated on both sides of the card; plug the black harness to the component side and the white harness to the print side.



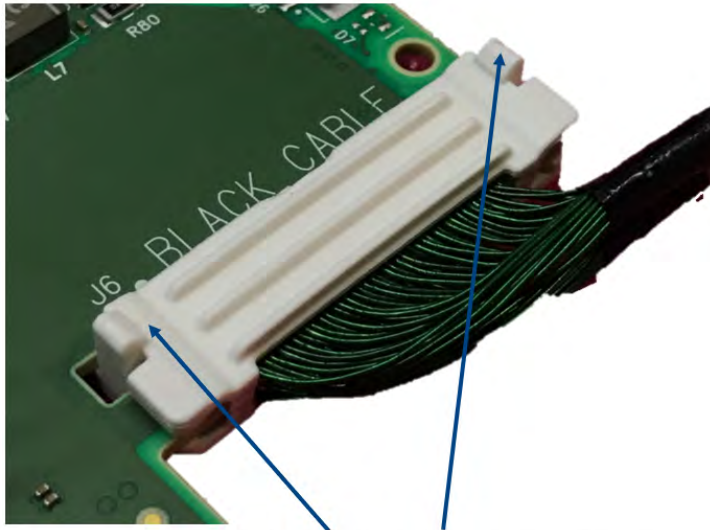
Step 3: Verify the plugs are locked.



**Step 4:** Slide the retention clip latches through the cutouts on the PCB. The latches should face the annotation on the PCB.



**Step 4:** Clamp the retention clip. Verify both latches are firmly locked.



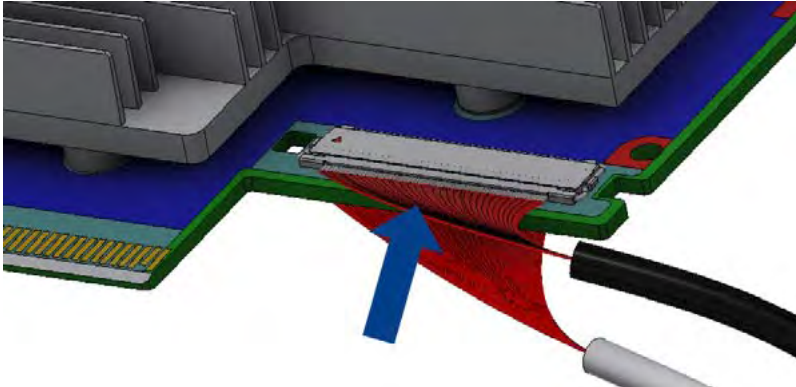
Verify that both latches are firmly snapped



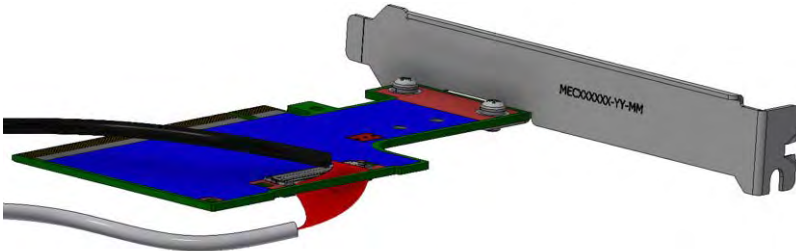
Step 5: Slide the Cabline CA-II Plus harnesses through the retention clip. Make sure that the clip opening is facing the plugs.



Step 6: Plug the Cabline CA-II Plus harnesses on the PCIe Auxiliary Card. As indicated on both sides of the Auxiliary connection card; plug the black harness to the component side and the white harness to the print side.



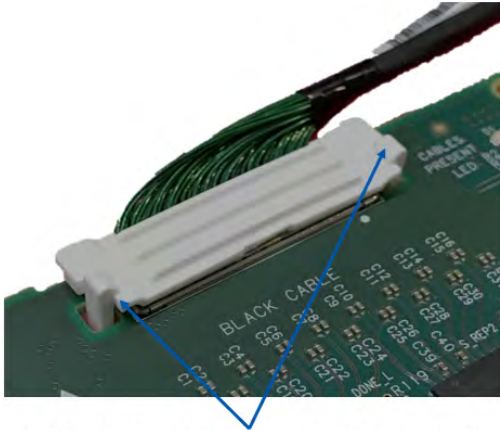
Step 7: Verify the plugs are locked.



Step 8: Slide the retention clip through the cutouts on the PCB. Make sure latches are facing "Black Cable" annotation as seen in the below picture.



Step 9: Clamp the retention clip. Verify both latches are firmly locked.



Verify that both latches are firmly snapped

➤ Connect the DPU and PCIe Auxiliary Connection cards in available PCI Express x16 slots in the chassis.

Step 1: Locate two available PCI Express x16 slots.

Step 2: Applying even pressure at both corners of the cards, insert the DPU in the PCI Express slots until firmly seated.



Do not use excessive force when seating the cards, as this may damage the system or the cards.

Step 3: Applying even pressure at both corners of the cards, insert the Auxiliary Connection card in the PCI Express slots until firmly seated.



Secure the DPU and PCIe Auxiliary Connection Cards to the chassis.

Secure the brackets to the chassis with the bracket screws.

## Uninstalling the Cards

### Safety Precautions

The DPU is installed in a system that operates with voltages that can be lethal. Before uninstalling the DPU, please observe the following precautions to avoid injury and prevent damage to system components.

1. Remove any metallic objects from your hands and wrists.
2. It is strongly recommended to use an ESD strap or other antistatic devices.
3. Turn off the system and disconnect the power cord from the server.

### Card Removal

1. Verify that the system is powered off and unplugged.
2. Wait 30 seconds.
3. To remove the card, disengage the retention mechanisms on the brackets (clips or screws).

4. Holding the DPU from its center, gently pull the DPU and Auxiliary Connections card out of the PCI Express slot.

## Setting High-Speed-Port Link Type

The following table lists the BlueField-3 supported speeds and the default networking port link type per OPN.

| OPN  | Data Transmission Rate                         | Default Protocol and Rate |
|--|--|---------------------------|
| 900-9D3B4-00EN-EA0<br>900-9D3B4-00PN-EA0<br>900-9D3B6-00CN-AB0<br>900-9D3B6-00SN-AB0 | InfiniBand: NDR 400Gb/s<br>Ethernet: 400GbE    | InfiniBand NDR 400Gb/s    |
| 900-9D3B6-00CV-AA0<br>900-9D3B6-00SV-AA0   | InfiniBand: NDR200 200Gb/s<br>Ethernet: 200GbE | Ethernet 200GbE           |
| 900-9D3B6-00CC-AA0<br>900-9D3B6-00SC-AA0<br>900-9D3B6-00CC-EA0<br>900-9D3B6-00SC-EA0 | InfiniBand: HDR100 100Gb/s<br>Ethernet: 100GbE | Ethernet 100GbE           |

To configure the high-speed networking port mode, you can either use the [mlxconfig](#) or the [UEFI](#) tools.

UEFI can configure the DPU device before the operating system is up, while mlxconfig configures the card once the operating system is up. According to your preference, use one of the below tools:

### mlxconfig

The mlxconfig tool allows users to change device configurations without burning the firmware. The configuration is also kept after reset. By default, mlxconfig shows the configurations that will be loaded in the next boot. For more information and instructions, refer to [Using mlxconfig to Set IB/ETH Parameters](#).

### UEFI

PreBoot drivers initialize the adapter device, check the port protocol type - Ethernet or InfiniBand - and bring up the port. Then it connects to a DHCP server to obtain its assigned IP address and network parameters and obtain the source location of the kernel/OS to boot from. The DHCP server instructs the PreBoot drivers to access the kernel/OS through a TFTP server, an iSCSI target, or some other service. For more information and instructions, refer to [UEFI](#).



# Troubleshooting

|   |   |
|---|---|
| Server unable to find the DPU                           | <ul style="list-style-type: none"><li>• Ensure that the DPU is placed correctly</li><li>• Make sure the DPU slot and the DPU are compatible</li><li>• Install the DPU in a different PCI Express slot</li><li>• Use the drivers that came with the DPU or download the latest</li><li>• Make sure your motherboard has the latest BIOS</li><li>• Try to reboot the server</li></ul> |
| The DPU no longer works                                 | <ul style="list-style-type: none"><li>• Reseat the DPU in its slot or a different slot, if necessary</li><li>• Try using another cable</li><li>• Reinstall the drivers for the network driver files may be damaged or deleted</li><li>• Reboot the server</li></ul>   |
| DPU stopped working after installing another DPU        | <ul style="list-style-type: none"><li>• Try removing and re-installing all DPUs</li><li>• Check that cables are connected properly</li><li>• Make sure your motherboard has the latest BIOS</li></ul>   |
| Link indicator light is off                             | <ul style="list-style-type: none"><li>• Try another port on the switch</li><li>• Make sure the cable is securely attached</li><li>• Check you are using the proper cables that do not exceed the recommended lengths</li><li>• Verify that your switch and DPU port are compatible</li></ul>  |
| Link light is on, but with no communication established | <ul style="list-style-type: none"><li>• Check that the latest driver is loaded</li><li>• Check that both the DPU and its link are set to the same speed and duplex settings</li></ul>   |
| Forgot password needed to install/upgrade the DPU image | Refer to the latest version of <a href="#">BlueField DPU SW Manual</a> and follow instructions under "Upgrading NVIDIA BlueField DPU Software" section.   |



# Specifications



Ensure your system supports the following system hardware and power supply requirements prior to installing your card.

|             |  |
|-------------|--|
| <b>FHHL</b> | <b>E-Series DPUs:</b> A maximum of 75W system power supply through the PCIe x16 interface.   |
|             | <b>P-Series DPUs:</b> A minimum of 75W or greater system power supply through the PCIe x16 interface, <b>and</b> a supplementary 8-pin ATX power supply connectivity available through the external power supply connector |

## 900-9D3B4-00EN-EA0 / 900-9D3B4-00PN-EA0 Specifications

|                                       |  |   |                                |
|---------------------------------------|--|---|--------------------------------|
| BlueField-3 SoC                       | BlueField-3 E-Series - 8 Arm-Cores - 505MHz/2000MHz  |   |                                |
|                                       | <ul style="list-style-type: none"><li>900-9D3B4-00EN-EA0: Crypto Enabled with integrated BMC</li><li>900-9D3B4-00PN-EA0: Crypto Disabled with integrated BMC</li></ul>   |   |                                |
| Physical                              | Single-Slot FHHL Card Dimensions: 111.15mm x 167.65mm<br>Tall Bracket Dimensions: 121.0mm x 21.6mm<br>Heatsink Dimensions (Length, Width, Height): 139.6mm x 92.7mm x 10.2mm   |   |                                |
| Interfaces                            | See <a href="#">Supported Interfaces</a>   |   |                                |
|                                       | On-board Memory  | <ul style="list-style-type: none"><li>Single-channel with 10 DDR5 + ECC (64bit + 8bit ECC) for a total of <b>16GB</b>@ 5200MT/s</li><li>40GB pSLC eMMC memory + 128GB SSD</li></ul> |                                |
|                                       | PCI Express Interface  | Gen 5.0 SERDES @ 32.0GT/s, 16 lanes (4.0, 3.0, 2.0 and 1.1 compatible)  |                                |
|                                       | Networking Connector   | Single-port QSFP112 (copper and optical)  |                                |
| Data Rate                             | InfiniBand (Default Speed)   | NDR/NDR200/HDR/HDR100/EDR/FDR/SDR   |                                |
|                                       | Ethernet   | 400/200/100/50/25/10 Gb/s   |                                |
| Protocol Support                      | <b>InfiniBand:</b> IBTA v1.5 <sup>(a)</sup><br>Auto-Negotiation: NDR (4 lanes x 100Gb/s per lane) port, NDR200 (2 lanes x 100Gb/s per lane) port, HDR (50Gb/s per lane) port, HDR100 (2 lane x 50Gb/s per lane), EDR (25Gb/s per lane) port, FDR (14.0625Gb/s per lane), 1X/2X/4X SDR (2.5Gb/s per lane)                                       |   |                                |
|                                       | <b>Ethernet:</b> 400GAUI-4 C2M, 400GBASE-CR4, 200GAUI-2 C2M, 200GAUI-4 C2M, 200GBASE-CR4, 100GAUI-2 C2M, 100GAUI-1 C2M, 100GBASE-CR4, 100GBASE-CR2, 100GBASE-CR1, 50GAUI-2 C2M, 50GAUI-1 C2M, 50GBASE-CR, 50GBASE-R2 , 40GBASE-CR4, 40GBASE-R2, 25GBASE-R, 10GBASE-R, 10GBASE-CX4, 1000BASE-CX, CAUI-4 C2M, 25GAUI C2M, XLAUI C2M , XLPPI, SFI |   |                                |
| Electrical and Thermal Specifications | Voltage  | 12V   |                                |
|                                       | Electrical and thermal specifications are provided in " <b>NVIDIA BlueField-3 DPUs Electrical and Thermal Specifications</b> " document. You can access the document either by logging into NVOnline or by contacting your NVIDIA representative.  |   |                                |
| Environmental                         | Temperature  | Operational   | 0 °C to 55 °C                  |
|                                       |  | Non-operational   | -40 °C to 70 °C <sup>(b)</sup> |

|            |                        |                              |                              |
|------------|------------------------|------------------------------|------------------------------|
|            | Humidity               | Operational                  | 10% to 85% relative humidity |
|            |                        | Non-operational              | 10% to 90% relative humidity |
|            | Altitude (Operational) | 3050m                        |                              |
| Regulatory | Safety                 | CB / cTUVus / CE             |                              |
|            | EMC                    | CE / FCC / VCCI / ICES / RCM |                              |
|            | RoHS                   | RoHS compliant               |                              |

Notes:

(a) The BlueField-3 DPU supplement the IBTA auto-negotiation specification to get better bit error rates and longer cable reaches. This supplemental feature only initiates when connected to another NVIDIA InfiniBand product.

(b) The non-operational storage temperature specifications apply to the product without its package.

## 900-9D3B6-00CV-AA0 / 900-9D3B6-00SV-AA0 Specifications

|                                       |  |   |
|---------------------------------------|--|---|
| BlueField-3 SoC                       | BlueField-3 P-Series - 16 Arm-Cores - 560MHz/2133MHz   |   |
|                                       | <ul style="list-style-type: none"><li>900-9D3B6-00CV-AA0: Crypto Enabled with integrated BMC</li><li>900-9D3B6-00SV-AA0: Crypto Disabled with integrated BMC</li></ul>   |   |
| Physical                              | Single-Slot FHHL Card Dimensions: 111.15mm x 167.65mm<br>Tall Bracket Dimensions: 121.0mm x 21.6mm<br>Heatsink Dimensions (Length, Width, Height): 139.6mm x 92.7mm x 10.2mm   |   |
| Interfaces                            | See <a href="#">Supported Interfaces</a>   |   |
|                                       | PCI Express Interface  | Gen 5.0 SERDES @ 32.0GT/s, 16 lanes (4.0, 3.0, 2.0 and 1.1 compatible)<br><br><b>Optional:</b> Additional PCIe x16 Gen 5.0 @ SERDES 32GT/s through the PCIe auxiliary passive card and Cabline SA-II Plus harnesses |
|                                       | On-Board Memory  | <ul style="list-style-type: none"><li>Dual-channel with <b>20</b> DDR5 + ECC (128bit + 16bit ECC) for a total of <b>32GB</b> @ 5600MT/s</li><li>40GB pSLC eMMC memory + 128GB SSD</li></ul>                         |
|                                       | Networking Connector   | Dual-port QSFP112 (copper and optical)  |
|                                       |  |   |
| Data Rate                             | InfiniBand   | NDR200/HDR/HDR100/EDR/FDR/SDR   |
|                                       | Ethernet (Default Speed)   | 200/100/50/25/10 Gb/s   |
| Protocol Support                      | InfiniBand: IBTA v1.5 <sup>(a)</sup><br>Auto-Negotiation: NDR200 (2 lanes x 100Gb/s per lane) port, HDR (50Gb/s per lane) port, HDR100 (2 lane x 50Gb/s per lane), EDR (25Gb/s per lane) port, FDR (14.0625Gb/s per lane), 1X/2X/4X SDR (2.5Gb/s per lane).  |   |
|                                       | Ethernet: 200GAUI-2 C2M, 200GAUI-4 C2M, 200GBASE-CR4, 100GAUI-2 C2M, 100GAUI-1 C2M, 100GBASE-CR4, 100GBASE-CR2, 100GBASE-CR1, 50GAUI-2 C2M, 50GAUI-1 C2M, 50GBASE-CR, 50GBASE-R2 , 40GBASE-CR4, 40GBASE-R2, 25GBASE-R, 10GBASE-R, 10GBASE-CX4, 1000BASE-CX, CAUI-4 C2M, 25GAUI C2M, XLAUI C2M , XLPPI, SFI |   |
| Electrical and Thermal Specifications | Voltage: 12V   |   |
|                                       | Electrical and thermal specifications are provided in " <b>NVIDIA BlueField-3 DPUs Electrical and Thermal Specifications</b> " document. You can access the document either by logging into NVOnline or by contacting your NVIDIA representative.  |   |

|               |                        |                              |                                |
|---------------|------------------------|------------------------------|--------------------------------|
| Environmental | Temperature            | Operational                  | 0° C to 55° C                  |
|               |                        | Non-operational              | -40° C to 70° C <sup>(b)</sup> |
|               | Humidity               | Operational                  | 10% to 85% relative humidity   |
|               |                        | Non-operational              | 10% to 90% relative humidity   |
|               | Altitude (Operational) | 3050m                        |                                |
| Regulatory    | Safety                 | CB / cTUVus / CE             |                                |
|               | EMC                    | CE / FCC / VCCI / ICES / RCM |                                |
|               | RoHS                   | RoHS compliant               |                                |

Notes:

(a) The BlueField-3 DPU supplement the IBTA auto-negotiation specification to get better bit error rates and longer cable reaches. This supplemental feature only initiates when connected to another NVIDIA InfiniBand product.

(b) The non-operational storage temperature specifications apply to the product without its package.

## 900-9D3B6-00CC-EA0 / 900-9D3B6-00SC-EA0 Specifications



Requires a supplementary 8-pin ATX power supply connectivity available through the external power supply connector.

|                 |  |   |  |
|-----------------|--|---|--|
| BlueField-3 SoC | BlueField-3 E-Series - 16 Arm-Cores - 505MHz/2000MHz   |   |  |
|                 | <ul style="list-style-type: none"> <li>900-9D3B6-00CC-EA0: Crypto Enabled with integrated BMC</li> <li>900-9D3B6-00SC-EA0: Crypto Disabled with integrated BMC</li> </ul>    |   |  |
| Physical        | Single-Slot FHHL Card Dimensions: 111.15mm x 167.65mm<br>Tall Bracket Dimensions: 121.0mm x 21.6mm<br>Heatsink Dimensions (Length, Width, Height): 139.6mm x 92.7mm x 10.2mm |   |  |
| Interfaces      | See <a href="#">Supported Interfaces</a>   |   |  |
|                 | PCI Express Interface  | Gen 5.0 SERDES @ 32.0GT/s, 16 lanes (4.0, 3.0, 2.0 and 1.1 compatible)<br><br><b>Optional:</b> Additional PCIe x16 Gen 5.0 @ SERDES 32GT/s through the PCIe auxiliary passive card and Cabline SA-II Plus harnesses |  |
|                 | On-board Memory  | <ul style="list-style-type: none"> <li>Dual-channel with <b>20</b> DDR5 + ECC (128bit + 16bit ECC) for a total of <b>32GB</b> @ 5200MT/s</li> <li>40GB pSLC eMMC memory + 128GB SSD</li> </ul>                      |  |
|                 | Networking Connector   | Dual-port QSFP112 (copper and optical)  |  |
| Data Rate       | InfiniBand   | HDR100/EDR/FDR/SDR  |  |
|                 | Ethernet (Default Speed)   | 100/50/25/10 Gb/s   |  |

|                                       |  |                              |                                |
|---------------------------------------|--|------------------------------|--------------------------------|
| Protocol Support                      | InfiniBand: IBTA v1.5 <sup>(a)</sup><br>Auto-Negotiation: HDR100 (2 lane x 50Gb/s per lane), EDR (25Gb/s per lane) port, FDR (14.0625Gb/s per lane), 1X/2X/4X SDR (2.5Gb/s per lane).  |                              |                                |
|                                       | Ethernet: 100GAUI-2 C2M, 100GAUI-1 C2M, 100GBASE-CR4, 100GBASE-CR2, 100GBASE-CR1, 50GAUI-2 C2M, 50GAUI-1 C2M, 50GBASE-CR, 50GBASE-R2 , 40GBASE-CR4, 40GBASE-R2, 25GBASE-R, 10GBASE-R, 10GBASE-CX4, 1000BASE-CX, CAUI-4 C2M, 25GAUI C2M, XLAUI C2M , XLPPI, SFI |                              |                                |
| Electrical and Thermal Specifications | Voltage: 12V   |                              |                                |
|                                       | Electrical and thermal specifications are provided in " <b>NVIDIA BlueField-3 DPUs Electrical and Thermal Specifications</b> " document. You can access the document either by logging into NVOnline or by contacting your NVIDIA representative.              |                              |                                |
| Environmental                         | Temperature  | Operational                  | 0° C to 55° C                  |
|                                       |  | Non-operational              | -40° C to 70° C <sup>(b)</sup> |
|                                       | Humidity   | Operational                  | 10% to 85% relative humidity   |
|                                       |  | Non-operational              | 10% to 90% relative humidity   |
|                                       | Altitude (Operational)   | 3050m                        |                                |
| Regulatory                            | Safety   | CB / cTUVus / CE             |                                |
|                                       | EMC  | CE / FCC / VCCI / ICES / RCM |                                |
|                                       | RoHS   | RoHS compliant               |                                |

Notes:  
<sup>(a)</sup> The BlueField-3 DPU supplement the IBTA auto-negotiation specification to get better bit error rates and longer cable reaches. This supplemental feature only initiates when connected to another NVIDIA InfiniBand product.  
<sup>(b)</sup> The non-operational storage temperature specifications apply to the product without its package.

## 900-9D3B6-00CC-AA0 / 900-9D3B6-00SC-AA0 Specifications

|                        |   |   |
|------------------------|---|---|
| <b>BlueField-3 SoC</b> | <b>BlueField-3 P-Series</b> - 16 Arm-Cores - 560MHz/2133MHz   |   |
|                        | <ul style="list-style-type: none"> <li>900-9D3B6-00CC-AA0: Crypto Enabled with integrated BMC</li> <li>900-9D3B6-00SC-AA0: Crypto Disabled with integrated BMC</li> </ul>                         |   |
| <b>Physical</b>        | <b>Single-Slot FHHL Card Dimensions:</b> 111.15mm x 167.65mm<br><b>Tall Bracket Dimensions:</b> 121.0mm x 21.6mm<br><b>Heatsink Dimensions (Length, Width, Height):</b> 139.6mm x 92.7mm x 10.2mm |   |
| <b>Interfaces</b>      | See <a href="#">Supported Interfaces</a>  |   |
|                        | <b>PCI Express Interface</b>  | Gen 5.0 SERDES @ 32.0GT/s, 16 lanes (4.0, 3.0, 2.0 and 1.1 compatible)<br><br><b>Optional:</b> Additional PCIe x16 Gen 5.0 @ SERDES 32GT/s through the PCIe auxiliary passive card and Cabline SA-II Plus harnesses |
|                        | <b>On-board Memory</b>  | <ul style="list-style-type: none"> <li>Dual-channel with <b>20</b> DDR5 + ECC (128bit + 16bit ECC) for a total of <b>32GB</b> @ 5600MT/s</li> <li>40GB pSLC eMMC memory + 128GB SSD</li> </ul>                      |
|                        | <b>Networking Connector</b>   | Dual-port QSFP112 (copper and optical)  |
| <b>Data Rate</b>       | <b>InfiniBand</b>   | HDR100/EDR/FDR/SDR  |

|   |   |                              |                                |
|---|---|------------------------------|--------------------------------|
|   | <b>Ethernet (Default Speed)</b>   |                              | 100/50/25/10 Gb/s              |
| <b>Protocol Support</b>   | <b>InfiniBand:</b> IBTA v1.5 <sup>(a)</sup><br>Auto-Negotiation: HDR100 (2 lane x 50Gb/s per lane), EDR (25Gb/s per lane) port, FDR (14.0625Gb/s per lane), 1X/2X/4X SDR (2.5Gb/s per lane).  |                              |                                |
|   | <b>Ethernet:</b> 100GAUI-2 C2M, 100GAUI-1 C2M, 100GBASE-CR4, 100GBASE-CR2, 100GBASE-CR1, 50GAUI-2 C2M, 50GAUI-1 C2M, 50GBASE-CR, 50GBASE-R2 , 40GBASE-CR4, 40GBASE-R2, 25GBASE-R, 10GBASE-R, 10GBASE-CX4, 1000BASE-CX, CAUI-4 C2M, 25GAUI C2M, XLAUI C2M , XLPPI, SFI |                              |                                |
| <b>Electrical and Thermal Specifications</b>  | <b>Voltage:</b> 12V   |                              |                                |
|   | Electrical and thermal specifications are provided in " <b>NVIDIA BlueField-3 DPUs <i>Electrical and Thermal Specifications</i></b> " document. You can access the document either by logging into NVOnline or by contacting your NVIDIA representative.              |                              |                                |
| <b>Environmental</b>  | <b>Temperature</b>  | <b>Operational</b>           | 0 °C to 55 °C                  |
|   |   | <b>Non-operational</b>       | -40 °C to 70 °C <sup>(b)</sup> |
|   | <b>Humidity</b>   | <b>Operational</b>           | 10% to 85% relative humidity   |
|   |   | <b>Non-operational</b>       | 10% to 90% relative humidity   |
|   | <b>Altitude (Operational)</b>   | 3050m                        |                                |
| <b>Regulatory</b>   | <b>Safety</b>   | CB / cTUVus / CE             |                                |
|   | <b>EMC</b>  | CE / FCC / VCCI / ICES / RCM |                                |
|   | <b>RoHS</b>   | RoHS compliant               |                                |
| Notes:  |   |                              |                                |
| <sup>(a)</sup> The BlueField-3 DPU supplement the IBTA auto-negotiation specification to get better bit error rates and longer cable reaches. This supplemental feature only initiates when connected to another NVIDIA InfiniBand product. |   |                              |                                |
| <sup>(b)</sup> The non-operational storage temperature specifications apply to the product without its package.   |   |                              |                                |

## 900-9D3B6-00CN-AB0 / 900-9D3B6-00SN-AB0 Specifications

|                       |   |  |
|-----------------------|---|--|
| <b>BlueField-3 IC</b> | <b>BlueField-3 P-Series - 16 Arm-Cores - 560MHz/2133MHz</b>   |  |
|                       | <ul style="list-style-type: none"> <li>900-9D3B6-00CN-AB0: Crypto Enabled with integrated BMC</li> <li>900-9D3B6-00SN-AB0: Crypto Disabled with integrated BMC</li> </ul>                       |  |
| <b>Physical</b>       | <b>Dual-Slot FHHL Card Dimensions:</b> 111.15mm x 167.65mm<br><b>Tall Bracket Dimensions:</b> 121.0mm x 21.6mm<br><b>Heatsink Dimensions (Length, Width, Height):</b> 139.6mm x 92.7mm x 29.3mm |  |
| <b>Interfaces</b>     | See <a href="#">Supported Interfaces</a>  |  |
|                       | <b>PCI Express Interface</b>  | Gen 5.0 SERDES @ 32.0GT/s, 16 lanes (4.0, 3.0, 2.0 and 1.1 compatible)   |
|                       |   | <b>Optional:</b> Additional PCIe x16 Gen 5.0 @ SERDES 32GT/s through the PCIe auxiliary passive card and Cabline SA-II Plus harnesses  |
|                       | <b>On-board Memory</b>  | <ul style="list-style-type: none"> <li>Dual-channel with <b>20</b> DDR5 + ECC (128bit + 16bit ECC) for a total of <b>32GB</b> @ 5600MT/s</li> <li>40GB pSLC eMMC memory + 128GB SSD</li> </ul> |

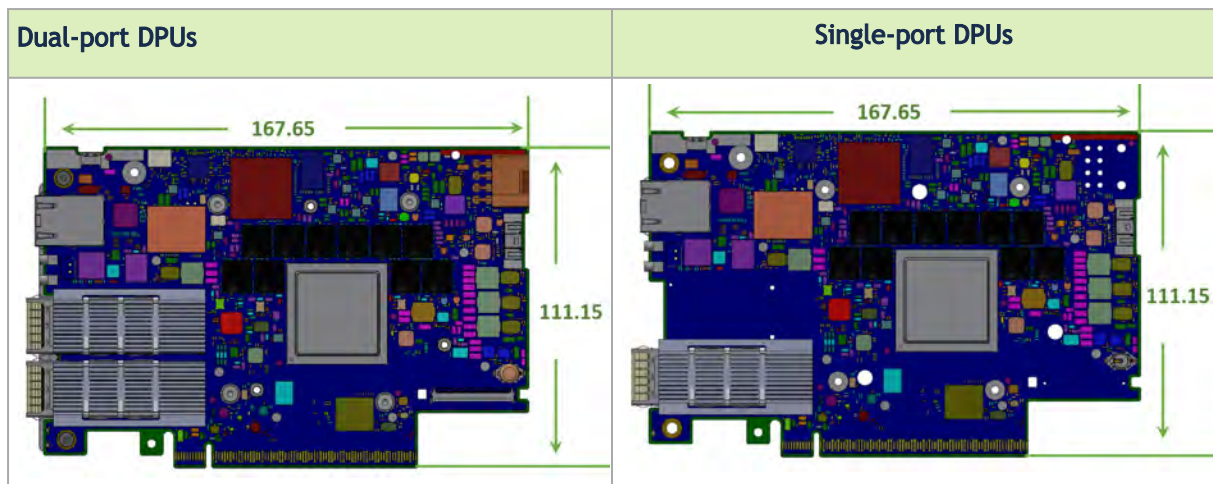
|   |   |                                   |                                |
|---|---|-----------------------------------|--------------------------------|
|   | Networking Connector  | Dual QSFP112 (copper and optical) |                                |
| Data Rate   | InfiniBand (Default Speed)  | NDR/NDR200/HDR/HDR100/EDR/FDR/SDR |                                |
|   | Ethernet  | 400/200/100/50/25/10 Gb/s         |                                |
| Protocol Support  | InfiniBand: IBTA v1.5 <sup>(a)</sup><br>Auto-Negotiation: NDR (4 lanes x 100Gb/s per lane) port, NDR200 (2 lanes x 100Gb/s per lane) port, HDR (50Gb/s per lane) port, HDR100 (2 lane x 50Gb/s per lane), EDR (25Gb/s per lane) port, FDR (14.0625Gb/s per lane), 1X/2X/4X SDR (2.5Gb/s per lane)                                       |                                   |                                |
|   | Ethernet: 400GAUI-4 C2M, 400GBASE-CR4, 200GAUI-2 C2M, 200GAUI-4 C2M, 200GBASE-CR4, 100GAUI-2 C2M, 100GAUI-1 C2M, 100GBASE-CR4, 100GBASE-CR2, 100GBASE-CR1, 50GAUI-2 C2M, 50GAUI-1 C2M, 50GBASE-CR, 50GBASE-R2 , 40GBASE-CR4, 40GBASE-R2, 25GBASE-R, 10GBASE-R, 10GBASE-CX4, 1000BASE-CX, CAUI-4 C2M, 25GAUI C2M, XLAUI C2M , XLPPI, SFI |                                   |                                |
|   | PCI Express 5.0: SERDES @ 32.0GT/s, 16 lanes (4.0, 3.0, 2.0 and 1.1 compatible)   |                                   |                                |
| Electrical and Thermal Specifications   | Voltage: 12V  |                                   |                                |
|   | Electrical and thermal specifications are provided in " <i>NVIDIA BlueField-3 DPUs Electrical and Thermal Specifications</i> " document. You can access the document either by logging into NVOnline or by contacting your NVIDIA representative.   |                                   |                                |
| Environmental   | Temperature   | Operational                       | 0° C to 55° C                  |
|   |   | Non-operational                   | -40° C to 70° C <sup>(b)</sup> |
|   | Humidity  | Operational                       | 10% to 85% relative humidity   |
|   |   | Non-operational                   | 10% to 90% relative humidity   |
|   | Altitude (Operational)  | 3050m                             |                                |
| Regulatory  | Safety  | CB / cTUVus / CE                  |                                |
|   | EMC   | CE / FCC / VCCI / ICES / RCM      |                                |
|   | RoHS  | RoHS compliant                    |                                |
| Notes:  |   |                                   |                                |
| <sup>(a)</sup> The BlueField-3 DPU supplement the IBTA auto-negotiation specification to get better bit error rates and longer cable reaches. This supplemental feature only initiates when connected to another NVIDIA InfiniBand product. |   |                                   |                                |
| <sup>(b)</sup> The non-operational storage temperature specifications apply to the product without its package.   |   |                                   |                                |

## DPU Mechanical Drawing and Dimensions



All dimensions are in millimeters. The PCB mechanical tolerance is +/- 0.13mm.

The diagrams may differ for different cards and are provided here for illustration purposes only.



## Bracket Mechanical Drawings

All dimensions are in millimeters.

| DPU Configuration |                 | Tall Bracket                           |
|-------------------|-----------------|--|
| Single-slot DPUs  | Dual-port DPU   | <p>120.9</p> <p>21.59</p> <p>18.42</p> |
|                   | Single-port DPU | <p>120.9</p> <p>21.59</p> <p>18.42</p> |
| Dual-slot DPUs    | Dual-port DPU   | <p>120.9</p> <p>41.92</p> <p>38.74</p> |



# Monitoring

## Thermal Sensors

The DPU incorporates the DPU SoC, which operates in the range of temperatures between 0°C and 105°C.

Three thermal threshold definitions impact the overall system operation state:

- Warning - 105°C: On managed systems only: When the device crosses the 105°C threshold, a Warning Threshold message is issued by the management SW, indicating to system administration that the card has crossed the warning threshold. Note that this temperature threshold does not require nor lead to any action by hardware (such as DPU shutdown).
- Critical - 115°C: When the device crosses this temperature, the firmware automatically shuts down the device.
- Emergency - 130°C: If the firmware fails to shutdown the device upon crossing the critical threshold, the device automatically shuts down upon crossing the emergency (130°C) threshold.

The DPU's thermal sensors can be read through the system's SMBus. The user can read these thermal sensors and adapt the system airflow following the readouts and the needs of the above-mentioned SoC thermal requirements.

## Heatsink

The heatsink is attached to the DPU by three screws to dissipate the heat from the SoC. The DPU SoC has a thermal shutdown safety mechanism that automatically shuts down the DPU in cases of high-temperature events, improper thermal coupling, or heatsink removal.

Refer to the below table for heatsink details per card configuration. For the required airflow (LFM) per OPN, please refer to [Specifications](#).


| Card Configuration | OPN   | Maximum Dimensions                               |
|--------------------|---|--|
| Single-slot DPUs   | 900-9D3B4-00EN-EA0, 900-9D3B4-00PN-EA0,<br>900-9D3B6-00CV-AA0, 900-9D3B6-00SV-AA0,<br>900-9D3B6-00CC-AA0, 900-9D3B6-00SC-AA0,<br>900-9D3B6-00CC-EA0, 900-9D3B6-00SC-EA0 | Length, Width, Height: 139.6mm x 92.7mm x 10.2mm |
| Dual-slot DPUs     | 900-9D3B6-00CN-AB0, 900-9D3B6-00SN-AB0  | Length, Width, Height: 139.6mm x 92.7mm x 29.3mm |



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## Finding the GUID/MAC on the DPU

Each DPU has a different identifier printed on the label: serial number and the card MAC (for the Ethernet protocol) and the card GUID (for the InfiniBand protocol). VPI cards have both a GUID and a MAC (derived from the GUID).


 The product revisions indicated on the labels in the following figures do not necessarily represent the latest revisions of the cards.


 The board label contains the base GUID.

The DPU labels contain five MAC addresses (Host, ECPF, BMC, MPF, and OOB).

- Host (Base MAC)
- ECPF: Embedded CPU Function (the embedded Arm system controls the NIC resources and datapath)
- DPU BMC: Connection of a Baseboard Management Controller (BMC)
- MPF: Multi/Management Physical Function
- OOB: Out-of-Band Management (Management Port)

The barcode supports all of the available MAC addresses.

 The HOST MAC in the board label is the product's base MAC.  
In dual-port cards, the HOST MAC belongs to the first port, and the HOST MAC of the second port increases by 1 (in HEX).  
For example:  
The HOST MAC address of the second port is HOST: 00 02 C9 27 05 01.

 The allocation of MAC addresses to the embedded CPU is derived from a few configuration factors which set some variables.

The gap between the MAC addresses is set by constant numbers in HEX.  
The OOB, ECPF, and MPF MAC addresses depend on the BASE MAC address.

DPU Board Label (Example)

**NVIDIA BlueField-3 DPU 200GbE**

**P/N: 900-9D3B6-00CV-AA0**

**Rev: A9**

**Model No: D3B6**

**2022-04-07**

**GUID: 946DAE0300F5A1CC**

**Made in Israel**

**HOST:946DAEF5A1CC**

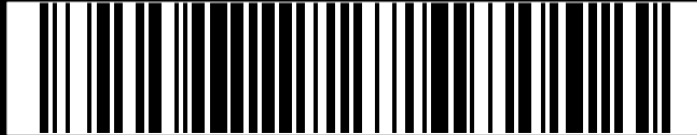
**OOB:946DAEF5A1F0**

**ECPF:946DAEF5A1DC**

**DPU BMC:946DAEF5A1F1**

**MPF:946DAEF5A1EC**

**S/N: MT23273005C9**



## PCIe Auxiliary Card Kit



This section applies to the following DPU's when used as Socket Direct cards in dual-socket servers.

- 900-9D3B6-00CN-AB0
- 900-9D3B6-00SN-AB0
- 900-9D3B6-00CV-AA0
- 900-9D3B6-00SV-AA0

Socket Direct network cards, which cost-effectively integrate a single network adapter silicon on a primary board, and an auxiliary PCIe connection card and [Cabline SA-II Plus Harness](#) connecting the two. Socket Direct enables direct access from each CPU to the network through its dedicated PCIe interface as the card's 32-lane PCIe bus is split into two 16-lane buses, with one bus accessible through a PCIe x16 edge connector and the other bus through an x16 Auxiliary PCIe Connection card. The two cards should be installed into two PCIe x16 slots and connected using two Cabline SA-II Plus harnesses.

The PCIe auxiliary kit can be purchased separately to operate in a dual-socket server. The below table lists the available PCIe auxiliary kit ordering part numbers, depending on the desired length of the Cabline SA-II Plus harnesses and the PCI Express interface, Gen 4.0 or Gen 5.0.

| Ordering Part Number | Passive Auxiliary Connection                | Cabline SA-II Plus Harnesses Length |
|----------------------|---|-------------------------------------|
| MTMK9100-T15         | PCIe Gen <b>4.0/5.0</b> x16 connection card | 2x 150mm harnesses                  |
| MTMK9100-T25         | PCIe Gen <b>4.0</b> x16 connection card     | 2x 250mm harnesses                  |
| MTMK9100-T35         | PCIe Gen <b>4.0</b> x16 connection card     | 2x 350mm harnesses                  |

The two [Cabline SA-II Plus harnesses](#) in the PCIe auxiliary kit have different routings. To distinguish between these two harnesses, one black harness is marked with a "WHITE" label while the harness is marked with a "BLACK" label.

The Cabline harness marked with the "WHITE" label should be connected to the connector on the networking card and PCIe Auxiliary card engraved with "White Cable" while the one marked with the "BLACK" label should be connected to the connector on the networking card and the PCIe Auxiliary card engraved with "Black Cable". The [Cabline SA-II Plus harness](#) mates with two 60-pin connectors (P/N 20790-060E-01), on both sides. The black [Cabline SA-II Plus harness](#) mates with the connector on the component side (top side) of the network card, while the White [Cabline SA-II Plus harnesses](#) mates with the pint side (bottom side) of the main network card. For hardware installation, please refer to [PCIe Extension Option \(2x PCIe x16\) Installation Instructions](#).

## PCIe Auxiliary Card Package Contents

| Category           | Qty | Item   |
|--------------------|-----|--|
| <b>Cards</b>       | 1   | MTMK9100-T15: PCIe x16 Gen <b>5.0/4.0</b> Auxiliary Connection Card<br>MTMK9100-T25 and MTMK9100-T35: PCIe x16 Gen 4.0 Auxiliary Connection Card |
| <b>Harnesses</b>   | 1   | Cabline CA-II Plus harness (white) - Length according to kit OPN (15, 25 or 35cm)  |
|                    | 1   | Cabline CA-II Plus harness (black) - Length according to kit OPN (15, 25 or 35cm)  |
| <b>Accessories</b> | 2   | Retention Clip for Cabeline harness (shipped assembled on the harnesses - optional)  |
|                    | 1   | PCIe Auxiliary card short bracket  |
|                    | 1   | PCIe Auxiliary card tall bracket (shipped assembled on the Auxiliary card)   |

## Channel Insertion Loss

Channel insertion loss is the signal power loss resulting from a device's insertion in a transmission line or optical fiber and is usually expressed in decibels (dB).

The following table describes the **NVIDIA® BlueField®-3** channel insertion loss budget for PCIe Gen 5.0 architecture (32 GT/s).

The total PCIe channel insertion loss approved by PCI-SIG Gen5.0 spec is 36dB @16GHz.

The total BlueField-3 DPU board insertion loss of the PCIe lanes (PCORE1) routed to the Cabline CA-II Plus is 6dB (@16GHz).

The Passive Socket Direct PCIe Auxiliary Card Loss is 1.5dB (@16Ghz).

The Cabline CA-II Plus harness loss at 16GHz:

| Harness Length | Channel Loss at Gen 5.0 |
|----------------|-------------------------|
| 15cm           | 3.8dB                   |
| 35cm           | 7.6dB                   |
| 55cm           | 11.4dB                  |

The above is measured data; it is recommended to add 0.5dB margins for your system (some loss variations are possible).

The Cabline CA-II Plus harnesses loss = 0.24dB/cm for Gen 5.0.

The above loss includes the Cabline CA-II Plus harnesses and connectors on both sides.

The PCI-SIG Gen5 SPEC also defines the total loss for AIC (bump to GF) to be 9.5dB @16Ghz.

The BlueField-3 AIC, together with a 15cm Cabline CA-II Plus harnesses and the Passive PCIe Auxiliary Card loss is: 3dB+2dB+3.8dB+1.5dB=10.3dB > 9.5dB

## Cabline CA-II Plus Harness Pinouts

### Cabline CA-II Plus Harness - Component Side

| Pin# | Signal Name     | Wire Type  | Detailed Description   | AWG# | Pin# on the other end |
|------|-----------------|------------|--|------|-----------------------|
| 1    | GND             | GND BAR    |  |      | 1                     |
| 2    | PCIE_REFCLK1_P  | Micro coax | Primary PCIe clock from the motherboard to the BlueField DPU Main card, to be used for the x16 Cabline harness PCIe interface. This clock must meet all the PCIe SIG spec requirements. It should be driven from the motherboard side. | 38   | 2                     |
| 3    | PCIE_REFCLK1_N  | Micro coax | Primary PCIe clock from the motherboard to the BlueField DPU Main card, to be used for the x16 Cabline harness PCIe interface. This clock must meet all the PCIe SIG spec requirements. It should be driven from the motherboard side. | 38   | 3                     |
| 4    | GND             | GND BAR    |  |      | 4                     |
| 5    | PCIE_CPU_CX_15N | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point   | 38   | 5                     |
| 6    | PCIE_CPU_CX_15P | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point   | 38   | 6                     |
| 7    | GND             | GND BAR    |  |      | 7                     |

| Pin# | Signal Name     | Wire Type  | Detailed Description   | AWG# | Pin# on the other end |
|------|-----------------|------------|--|------|-----------------------|
| 8    | PCIE_CPU_CX_14N | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 8                     |
| 9    | PCIE_CPU_CX_14P | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 9                     |
| 10   | GND             | GND BAR    |  |      | 10                    |
| 11   | PCIE_CPU_CX_13N | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 11                    |
| 12   | PCIE_CPU_CX_13P | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 12                    |
| 13   | GND             | GND BAR    |  |      | 13                    |
| 14   | PCIE_CPU_CX_12N | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 14                    |
| 15   | PCIE_CPU_CX_12P | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 15                    |
| 16   | GND             | GND BAR    |  |      | 16                    |
| 17   | PCIE_CPU_CX_11N | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 17                    |

| Pin# | Signal Name     | Wire Type  | Detailed Description   | AWG# | Pin# on the other end |
|------|-----------------|------------|--|------|-----------------------|
| 18   | PCIE_CPU_CX_11P | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 18                    |
| 19   | GND             | GND BAR    |  |      | 19                    |
| 20   | PCIE_CPU_CX_10N | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 20                    |
| 21   | PCIE_CPU_CX_10P | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 21                    |
| 22   | GND             | GND BAR    |  |      | 22                    |
| 23   | PCIE_CPU_CX_9N  | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 23                    |
| 24   | PCIE_CPU_CX_9P  | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 24                    |
| 25   | GND             | GND BAR    |  |      | 25                    |
| 26   | PCIE_CPU_CX_8N  | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 26                    |
| 27   | PCIE_CPU_CX_8P  | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 27                    |
| 28   | GND             | GND BAR    |  |      | 28                    |

| Pin# | Signal Name    | Wire Type  | Detailed Description   | AWG# | Pin# on the other end |
|------|----------------|------------|--|------|-----------------------|
| 29   | PCIE_CPU_CX_7N | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 29                    |
| 30   | PCIE_CPU_CX_7P | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 30                    |
| 31   | GND            | GND BAR    |  |      | 31                    |
| 32   | PCIE_CPU_CX_6N | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 32                    |
| 33   | PCIE_CPU_CX_6P | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 33                    |
| 34   | GND            | GND BAR    |  |      | 34                    |
| 35   | PCIE_CPU_CX_5N | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 35                    |
| 36   | PCIE_CPU_CX_5P | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 36                    |
| 37   | GND            | GND BAR    |  |      | 37                    |
| 38   | PCIE_CPU_CX_4N | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 38                    |



| Pin# | Signal Name    | Wire Type  | Detailed Description   | AWG# | Pin# on the other end |
|------|----------------|------------|--|------|-----------------------|
| 39   | PCIE_CPU_CX_4P | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 39                    |
| 40   | GND            | GND BAR    |  |      | 40                    |
| 41   | PCIE_CPU_CX_3N | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 41                    |
| 42   | PCIE_CPU_CX_3P | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 42                    |
| 43   | GND            | GND BAR    |  |      | 43                    |
| 44   | PCIE_CPU_CX_2N | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 44                    |
| 45   | PCIE_CPU_CX_2P | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 45                    |
| 46   | GND            | GND BAR    |  |      | 46                    |
| 47   | PCIE_CPU_CX_1N | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 47                    |
| 48   | PCIE_CPU_CX_1P | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point | 38   | 48                    |
| 49   | GND            | GND BAR    |  |      | 49                    |

| Pin# | Signal Name     | Wire Type  | Detailed Description   | AWG# | Pin# on the other end |
|------|-----------------|------------|--|------|-----------------------|
| 50   | PCIE_CPU_CX_ON  | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point   | 38   | 50                    |
| 51   | PCIE_CPU_CX_OP  | Micro coax | Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/GPU/End-Point   | 38   | 51                    |
| 52   | GND             | GND BAR    |  |      | 52                    |
| 53   | I2C_DPU_BMC_SDA | Micro coax |  | 38   | 53                    |
| 54   | I2C_DPU_BMC_SCL | Micro coax |  | 38   | 54                    |
| 55   | AUX_PGOOD       | Micro coax |  | 38   | 55                    |
| 56   | No wire         | Micro coax |  | 38   | 56                    |
| 57   | I2C_AUX_SCL     | Micro coax | The BlueField silicon serves as the I2C bus master on this bus. An I2C EEPROM at I2C address 0x57 needs to be mounted on the motherboard side to report to the Cabline CA-II Plus interface parameters to the main-card BlueField DPU silicon, like Cabline CA-II Plus cables length (contact NVIDIA for the format of this EEPROM). If additional optional I2C slave devices need to be managed by the main-card BlueField DPU silicon, they need to be included on this I2C bus as well. | 38   | 57                    |

| Pin# | Signal Name | Wire Type  | Detailed Description   | AWG# | Pin# on the other end |
|------|-------------|------------|--|------|-----------------------|
| 58   | I2C_AUX_SDA | Micro coax | The BlueField silicon serves as the I2C bus master on this bus. An I2C EEPROM at I2C address 0x57 needs to be mounted on the motherboard side to report to the Cabline CA-II Plus interface parameters to the main-card BlueField DPU silicon, like Cabline CA-II Plus cables length (contact NVIDIA for the format of this EEPROM). If additional optional I2C slave devices need to be managed by the main-card BlueField DPU silicon, they need to be included on this I2C bus as well. | 38   | 58                    |
| 59   | S_PRSNT1_L  | Micro coax | Connect this pin to GND<br>No wires are connected to these pins to ensure they do not interfere with the operation of S_PRSNT2_L for the detection when the two Cabline harnesses are installed.   | 38   | 59                    |
| 60   |             | No Wire    |  |      | 60                    |

## Cabline CA-II Plus Harness - Print Side

| Pin# | Signal Name | Wire Type  | AWG# | Detailed Description  | Pin# on the other end |
|------|-------------|------------|------|---|-----------------------|
| 1    | SER_CLK     | Micro coax | 38   | This pin is used as the serializer clock (SER_CLK) from the DPU to the device/s located on the motherboard. | 1                     |
| 2    | SER_CAPTURE | Micro coax | 38   | This pin is used as the serializer capture (SER_CAPTURE).   | 2                     |

| Pin# | Signal Name     | Wire Type  | AWG# | Detailed Description   | Pin# on the other end |
|------|-----------------|------------|------|--|-----------------------|
| 3    | SER_DO          | Micro coax | 38   | This pin is used as the serializer data out from the BlueField DPU to the device/s located on the motherboard.   | 3                     |
| 4    | S_PERST2_CONN_L | Micro coax | 38   | Optional: PCIe compliant PERST_L (active low PCI Reset) signal for the Cabline CA-II Plus PCIe interface. To be used as the PERST_L signal for the control of PCIe lane 15:8, when a bifurcation of the Cabline CA-II Plus PCIe x16 interface to two x8 interfaces is needed (and in specific main board assemblies which support such bifurcation). The direction of this optional PERST_L signal depends on the implementation:<br>When connecting a CPU root complex to the Cabline CA-II Plus PCIe interface, this signal is driven from the motherboard side (from the CPU), to the BlueField DPU;<br>When connecting a GPU or an end point to the Cabline CA-II Plus PCIe interface, this signal is driven from the BlueField DPU (which operates as a PCIe switch in this case), to the GPU or end-point on the motherboard side. | 4                     |
| 5    | SER_DI          | Micro coax | 38   | This pin is used as the serializer data in from the device/s located on the motherboard.   | 5                     |
| 6    | Reserved_06     | Micro coax | 38   |  | 6                     |
| 7    | Reserved_07     | Micro coax | 38   | Reserved for future expansion  | 7                     |

| Pin# | Signal Name    | Wire Type  | AWG# | Detailed Description  | Pin# on the other end |
|------|----------------|------------|------|---|-----------------------|
| 8    | Reserved_08    | Micro coax | 38   | Reserved for future expansion   | 8                     |
| 9    | GND            | GND BAR    |      |   | 9                     |
| 10   | PCIE_CX_CPU_0P | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 10                    |
| 11   | PCIE_CX_CPU_0N | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 11                    |
| 12   | GND            | GND BAR    |      |   | 12                    |
| 13   | PCIE_CX_CPU_1P | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 13                    |
| 14   | PCIE_CX_CPU_1N | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 14                    |
| 15   | GND            | GND BAR    |      |   | 15                    |
| 16   | PCIE_CX_CPU_2P | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 16                    |

| Pin# | Signal Name    | Wire Type  | AWG# | Detailed Description  | Pin# on the other end |
|------|----------------|------------|------|---|-----------------------|
| 17   | PCIE_CX_CPU_2N | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 17                    |
| 18   | GND            | GND BAR    |      |   | 18                    |
| 19   | PCIE_CX_CPU_3P | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 19                    |
| 20   | PCIE_CX_CPU_3N | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 20                    |
| 21   | GND            | GND BAR    |      |   | 21                    |
| 22   | PCIE_CX_CPU_4P | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 22                    |
| 23   | PCIE_CX_CPU_4N | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 23                    |
| 24   | GND            | GND BAR    |      |   | 24                    |

| Pin# | Signal Name    | Wire Type  | AWG# | Detailed Description  | Pin# on the other end |
|------|----------------|------------|------|---|-----------------------|
| 25   | PCIE_CX_CPU_5P | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 25                    |
| 26   | PCIE_CX_CPU_5N | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 26                    |
| 27   | GND            | GND BAR    |      |   | 27                    |
| 28   | PCIE_CX_CPU_6P | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 28                    |
| 29   | PCIE_CX_CPU_6N | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 29                    |
| 30   | GND            | GND BAR    |      |   | 30                    |
| 31   | PCIE_X_CPU_7P  | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 31                    |

| Pin# | Signal Name    | Wire Type  | AWG# | Detailed Description  | Pin# on the other end |
|------|----------------|------------|------|---|-----------------------|
| 32   | PCIE_CX_CPU_7N | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 32                    |
| 33   | GND            | GND BAR    |      |   | 33                    |
| 34   | PCIE_CX_CPU_8P | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 34                    |
| 35   | PCIE_CX_CPU_8N | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 35                    |
| 36   | GND            | GND BAR    |      |   | 36                    |
| 37   | PCIE_CX_CPU_9P | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 37                    |
| 38   | PCIE_CX_CPU_9N | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 38                    |
| 39   | GND            | GND BAR    |      |   | 39                    |



| Pin# | Signal Name     | Wire Type  | AWG# | Detailed Description  | Pin# on the other end |
|------|-----------------|------------|------|---|-----------------------|
| 40   | PCIE_CX_CPU_10P | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 40                    |
| 41   | PCIE_CX_CPU_10N | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 41                    |
| 42   | GND             | GND BAR    |      |   | 42                    |
| 43   | PCIE_CX_CPU_11P | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 43                    |
| 44   | PCIE_CX_CPU_11N | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 44                    |
| 45   | GND             | GND BAR    |      |   | 45                    |
| 46   | PCIE_CX_CPU_12P | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 46                    |

| Pin# | Signal Name     | Wire Type  | AWG# | Detailed Description  | Pin# on the other end |
|------|-----------------|------------|------|---|-----------------------|
| 47   | PCIE_CX_CPU_12N | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 47                    |
| 48   | GND             | GND BAR    |      |   | 48                    |
| 49   | PCIE_CX_CPU_13P | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 49                    |
| 50   | PCIE_CX_CPU_13N | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 50                    |
| 51   | GND             | GND BAR    |      |   | 51                    |
| 52   | PCIE_CX_CPU_14P | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 52                    |
| 53   | PCIE_CX_CPU_14N | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU. | 53                    |
| 54   | GND             | GND BAR    |      |   | 54                    |

| Pin# | Signal Name     | Wire Type  | AWG# | Detailed Description   | Pin# on the other end |
|------|-----------------|------------|------|--|-----------------------|
| 55   | PCIE_CX_CPU_15P | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU.  | 55                    |
| 56   | PCIE_CX_CPU_15N | Micro coax | 38   | Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the BlueField DPU.  | 56                    |
| 57   | GND             | GND BAR    |      |  | 57                    |
| 58   | S_PERST1_CONN_L | Micro coax | 38   | PCIe compliant PERST_L (active low PCI Reset) signal for the PCIe Cabline CA-II Plus Connectors. The direction of this PERST_L signal depends on the implementation: When connecting a CPU root complex to the PCIe Cabline CA-II Plus interface, this signal is driven from the motherboard side (from the CPU), to the BlueField DPU. When connecting a GPU or an end point to the PCIe Cabline CA-II Plus interface, this signal is driven from the BlueField DPU side (which operates as a PCIe switch in this case), to the GPU or end-point on the motherboard side. | 58                    |
| 59   |                 | No Wire    |      |  | 59                    |

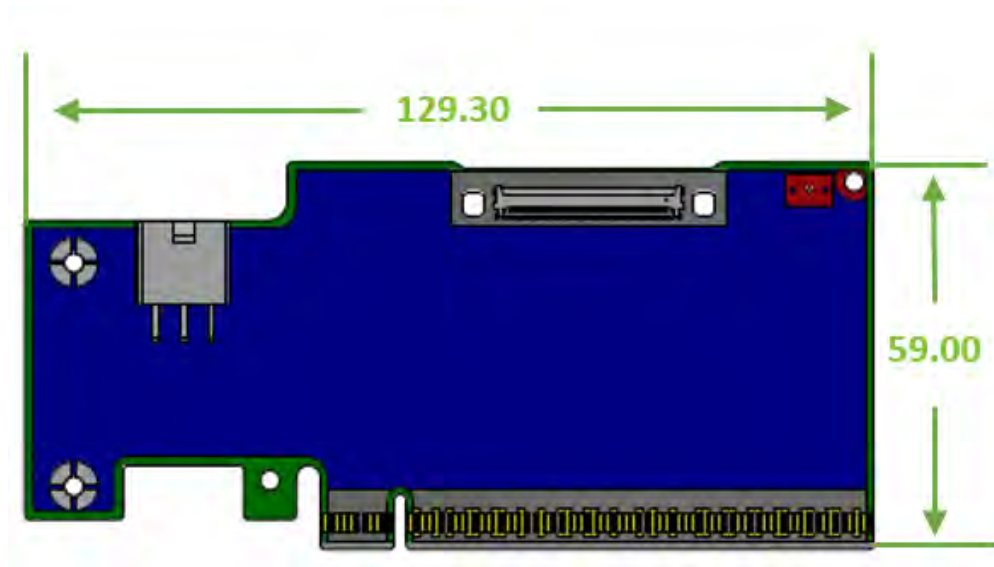
| Pin# | Signal Name | Wire Type  | AWG# | Detailed Description  | Pin# on the other end |
|------|-------------|------------|------|---|-----------------------|
| 60   | S_PRNT2_L   | Micro coax | 38   | Connect to a 4.7K pull-up resistor to 3.3V on the motherboard side, to detect if both the Cabline harnesses are connected or not. This signal is connected to S_PRNT1_L on the BlueField DPU. In the motherboard side, read logic low if both Cabline harnesses are connected. Read logic 1 (3.3V) if one or both the Cabline harnesses are not connected. No wires are connected to these pins to ensure they do not interfere with the operation of S_PRNT1_L for the detection when the two Cabline harnesses are installed. | 60                    |

## Technical Specifications

|                   |   |  |                              |
|-------------------|---|--|------------------------------|
| Physical          | PCIe Auxiliary Card Size: 5.09 in. x 2.32 in. (129.30mm x 59.00mm)<br>Two Cabline CA-II Plus harnesses (white and black) Length: 15, 25 or 35cm |  |                              |
| Power Consumption | <b>Voltage:</b> 12V, 3.3V_AUX<br><b>Maximum current:</b> 100mA for the 3.3V_AUX voltage rail  |  |                              |
| PCIe Connectivity | MTMK9100-T15  | PCI Express Gen 5.0/4.0: SERDES @ 16/32 GT/s, x16 lanes (Gen 3.0 compatible) |                              |
|                   | MTMK9100-T25 / MTKM9100-T35   | PCI Express Gen 4.0: SERDES @ 16GT/s, x16 lanes (Gen 3.0 compatible)         |                              |
| Environmental     | Temperature   | Operational  | 0°C to 55°C                  |
|                   |   | Non-operational  | -40°C to 70°C                |
|                   | Humidity  | Operational  | 10% to 85% relative humidity |
|                   |   | Non-operational  | 10% to 90% relative humidity |
|                   | Altitude (Operational)  | 3050m  |                              |
| Regulatory        | <b>Safety:</b> CB / cTUVus / CE   |  |                              |
|                   | <b>EMC:</b> CE / FCC / VCCI / ICES / RCM / KC   |  |                              |
|                   | <b>RoHS:</b> RoHS Compliant   |  |                              |

## PCIe Auxiliary Card Mechanical Drawings and Dimensions

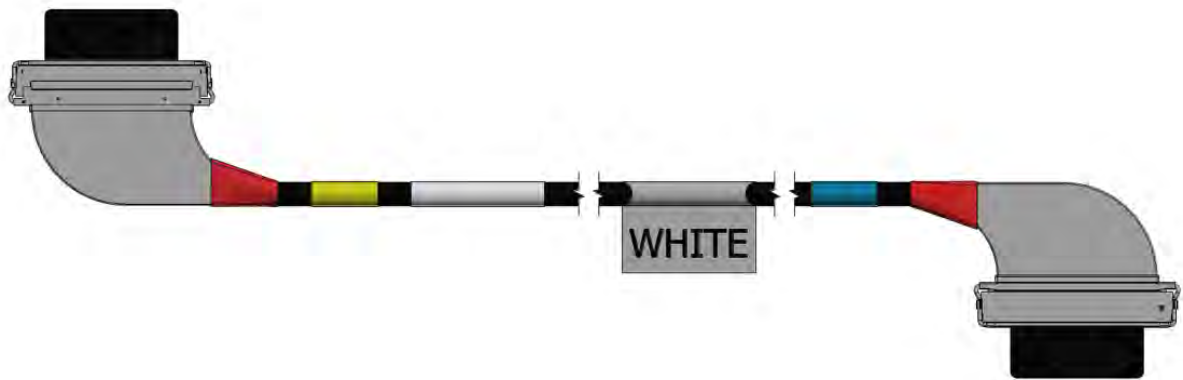
All dimensions are in millimeters. The PCB mechanical tolerance is +/- 0.13mm.



## Bracket Mechanical Drawings and Dimensions

| Auxiliary PCIe Connection Card Tall Bracket  | Auxiliary PCIe Connection Card Short Bracket  |
|--|---|
| <p>A mechanical drawing of the Auxiliary PCIe Connection Card Tall Bracket. The bracket is shown from a top-down perspective. It has a long, rectangular shape with a series of rectangular slots along its length. The overall length is dimensioned as 121.05 mm, and the overall height is dimensioned as 21.59 mm. The bracket is shown with a green outline indicating its mechanical dimensions.</p> | <p>A mechanical drawing of the Auxiliary PCIe Connection Card Short Bracket. The bracket is shown from a top-down perspective. It has a shorter, rectangular shape with a series of rectangular slots along its length. The overall length is dimensioned as 80.29 mm, and the overall height is dimensioned as 22.83 mm. The bracket is shown with a green outline indicating its mechanical dimensions.</p> |

## Cabline CA-II Plus Harnesses Mechanical Drawing



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## Supported Servers and Power Cords

To be updated in a future revision of this document.

# Document Revision History

| Date      | Description  |
|-----------|--|
| Aug 2023  | <ul style="list-style-type: none"> <li>Added step 3 to section <a href="#">Verifying DPU Connection and Setting Up Host Environment</a></li> <li>Fixed typo in <a href="#">Bracket Mechanical Drawings</a></li> </ul>  |
| Aug 2023  | <ul style="list-style-type: none"> <li>Updated the lifecycle tag of 900-9D3B6-00CV-AA0 and 900-9D3B6-00SV-AA0 to indicate "Mass Production".</li> <li>Updated <a href="#">Cabline CA-II Plus Connectors Pinouts</a>.</li> <li>Updated <a href="#">Cabline CA-II Plus Harness Pinouts</a>.</li> <li>Added a note to <a href="#">NVMe SSD Interface</a>.</li> </ul>  |
| July 2023 | Amended a note on airflow direction in <a href="#">Hardware Installation</a> .   |
| June 2023 | <ul style="list-style-type: none"> <li>Added sudo to step 2 in section <a href="#">Verifying DPU Connection and Setting Up Host Environment</a>.</li> <li>Updated list of identified devices in section <a href="#">Verifying DPU Connection and Setting Up Host Environment</a>.</li> <li>Added section <a href="#">Connecting to BlueField and Verifying Version</a>.</li> <li>Updated step 2.c. in section <a href="#">Updating BlueField BFB Image</a>.</li> <li>Added sudo to step 3.b. in section <a href="#">Updating BlueField BFB Image</a>.</li> <li>Marked 900-9D3B6-00CC-AA0 and 900-9D3B6-00SC-AA0 as EOL (End of Life) products.</li> <li>Added new DPUs to the user manual: 900-9D3B6-00CC-EA0 and 900-9D3B6-00SC-EA0.</li> <li>Updated <a href="#">Cabline CA-II Plus Harness Pinouts</a>.</li> <li>Updated SoC frequency for E-Series DPUs in <a href="#">Specifications</a></li> </ul> |
| May 2023  | <ul style="list-style-type: none"> <li>Updated <a href="#">Specifications</a> - added non-operational storage temperature specifications.</li> <li>Updated Ethernet protocols in <a href="#">Specifications</a>.</li> </ul>  |
| Apr 2023  | Added PSID and device ID information in <a href="#">NVIDIA BlueField-3 DPU User Guide</a> .  |
| Mar 2023  | Updated <a href="#">DDR5 SDRAM On-Board Memory</a> .   |
| Feb 2023  | Updated <a href="#">External PCIe Power Supply Connector</a> .   |
| Feb 2022  | <ul style="list-style-type: none"> <li>Updated list of SKUs across the document</li> <li>Added <a href="#">BlueField DPU Administrator Quick Start Guide</a></li> <li>Added <a href="#">Setting High-Speed-Port Link Type</a></li> <li>Added an important note on the <a href="#">External PCIe Power Supply Connector</a></li> </ul>  |
| Jan 2023  | Added <a href="#">PCIe Auxiliary Card Kit</a>  |
| Nov 2022  | Updated the following sections: <ul style="list-style-type: none"> <li><a href="#">NC-SI Interface Pinouts</a></li> </ul>  |
| Jul 2022  | Updated the following sections: <ul style="list-style-type: none"> <li><a href="#">Cabline CA-II Plus Connectors</a> with additional information.</li> <li>Added Cabline CA-II Connector pins in <a href="#">Pinouts Description</a>.</li> <li><a href="#">Finding the GUID/MAC on the DPU</a> with board label examples.</li> <li><a href="#">PCI Express Interface</a> pinouts to reflect changes in pins BB81 and B882.</li> <li>Added heatsink dimensions in <a href="#">Introduction</a> and <a href="#">Specifications</a>.</li> </ul>   |
| Jun 2022  | Renamed the document from "NVIDIA BleuField-3 InfiniBand/VPI DPU User Guide" to "NVIDIA BlueField-3 DPU User Guide"  |
| May 2022  | First release  |



## Notice

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