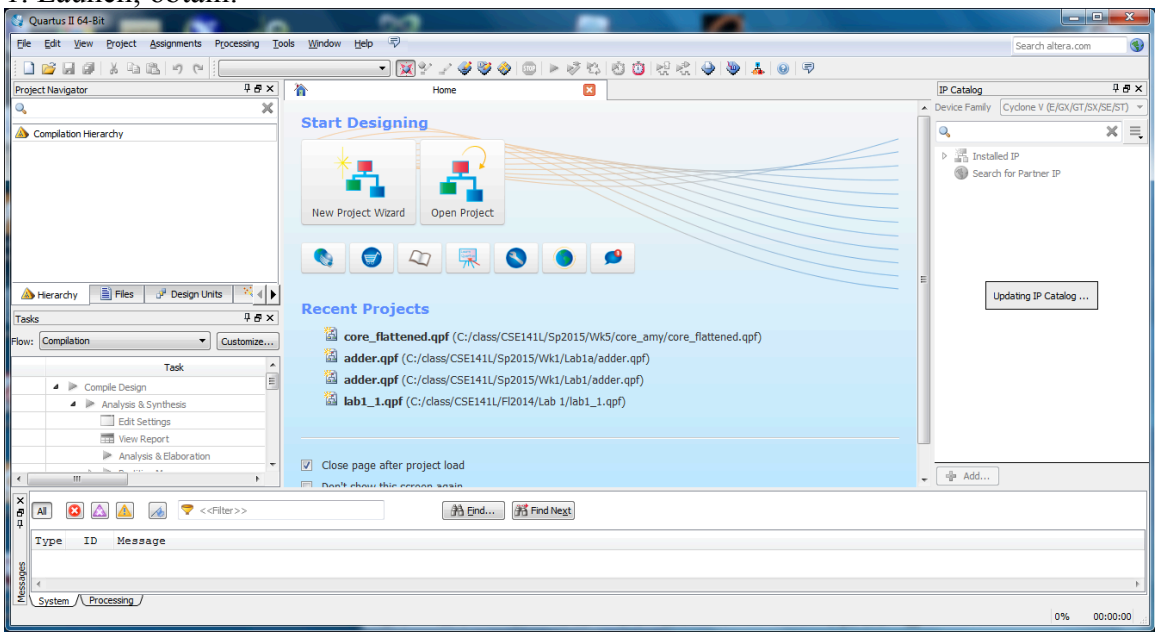
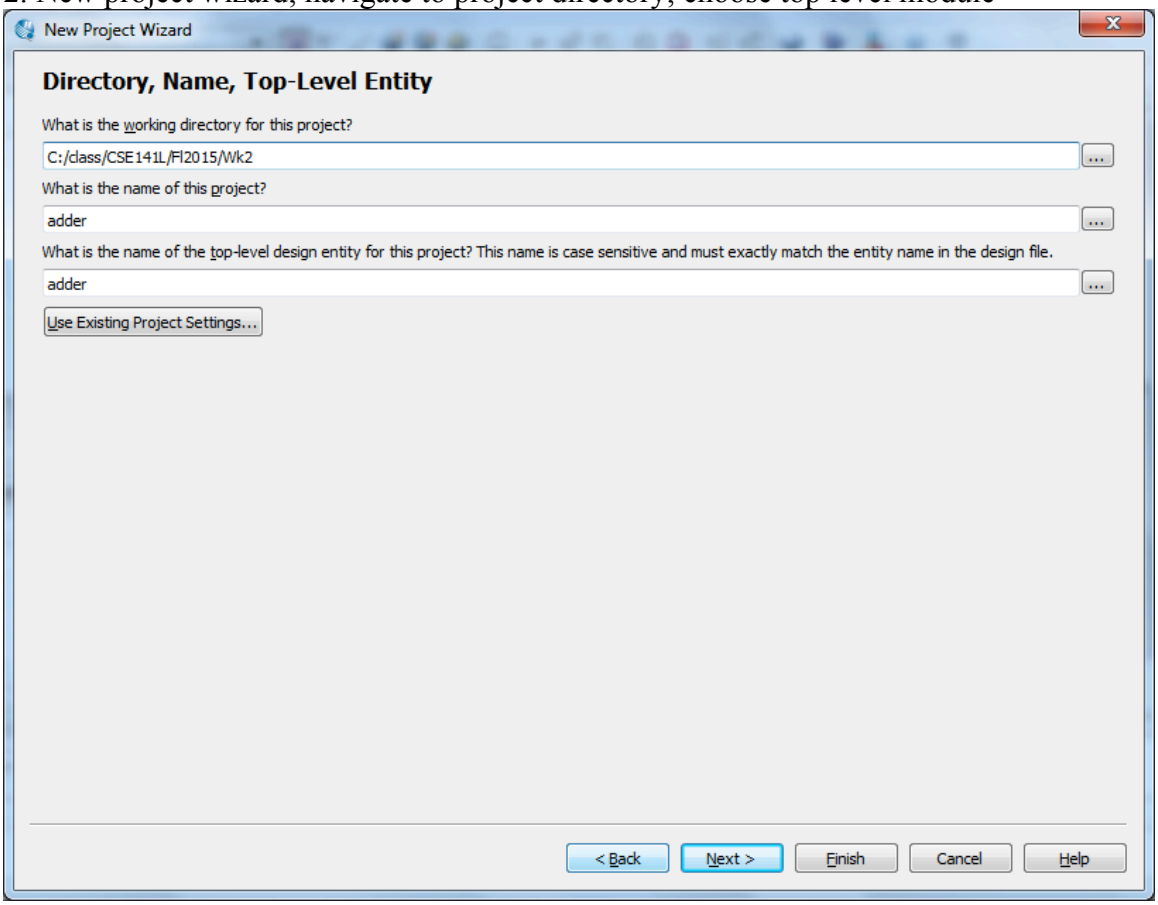
Using Quartus II

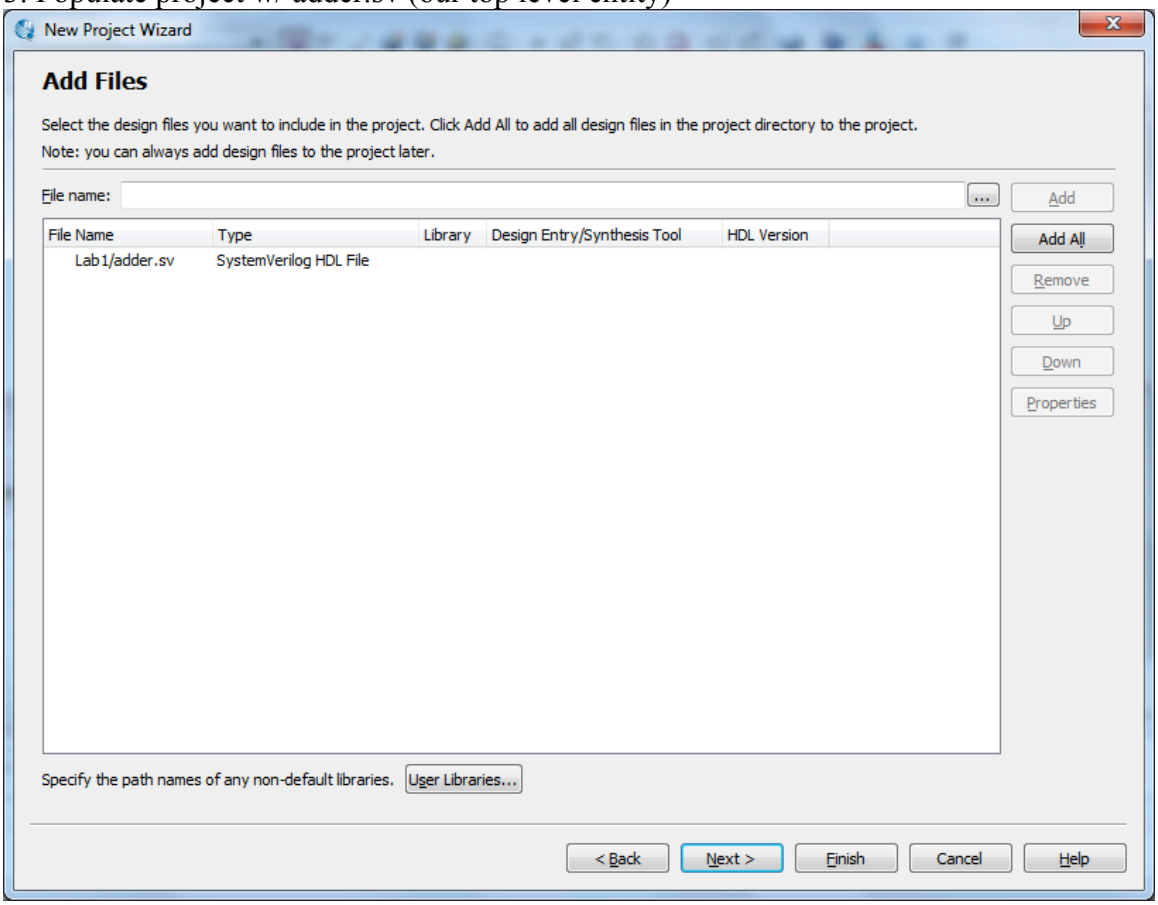
1. Launch; obtain:



2. New project wizard; navigate to project directory; choose top level module

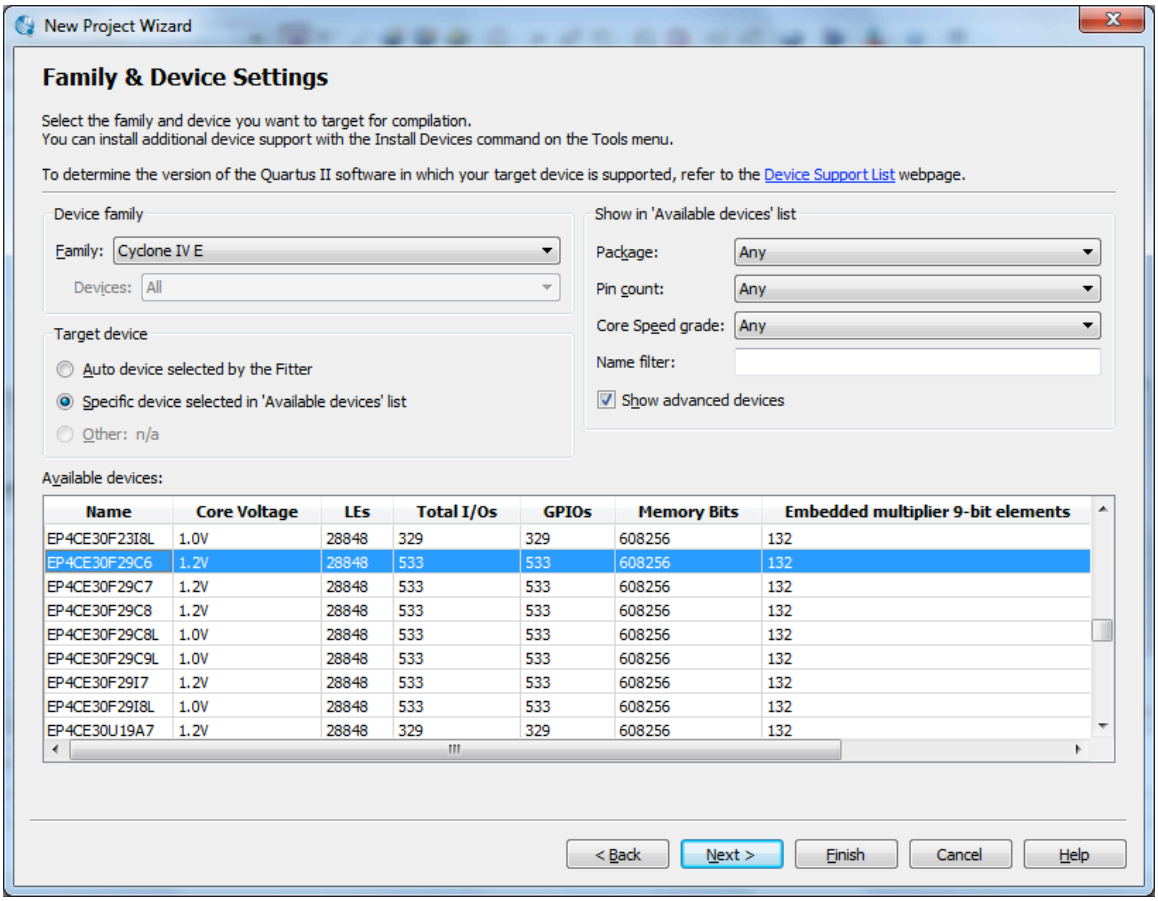


3. Populate project w/ adder.sv (our top level entity)

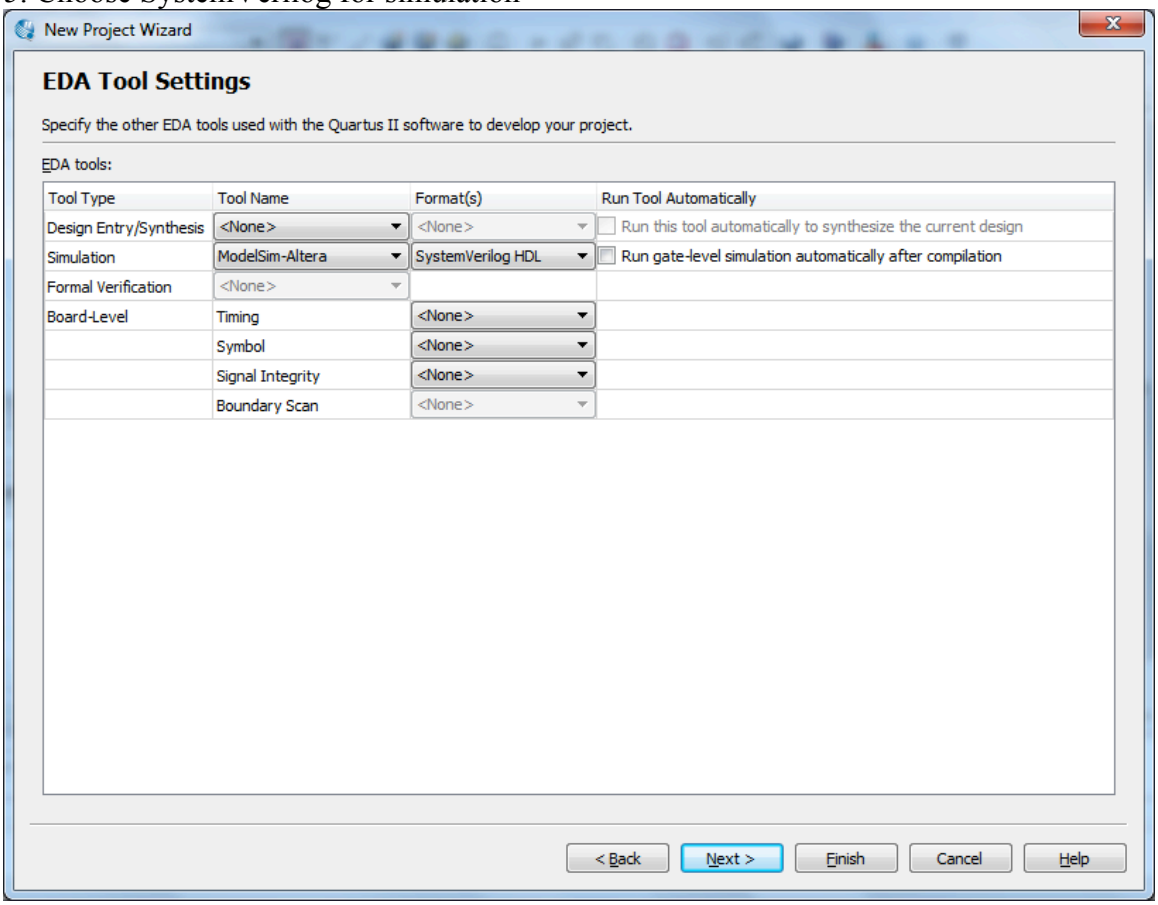


(would also include any lower level submodules -- none in this case)

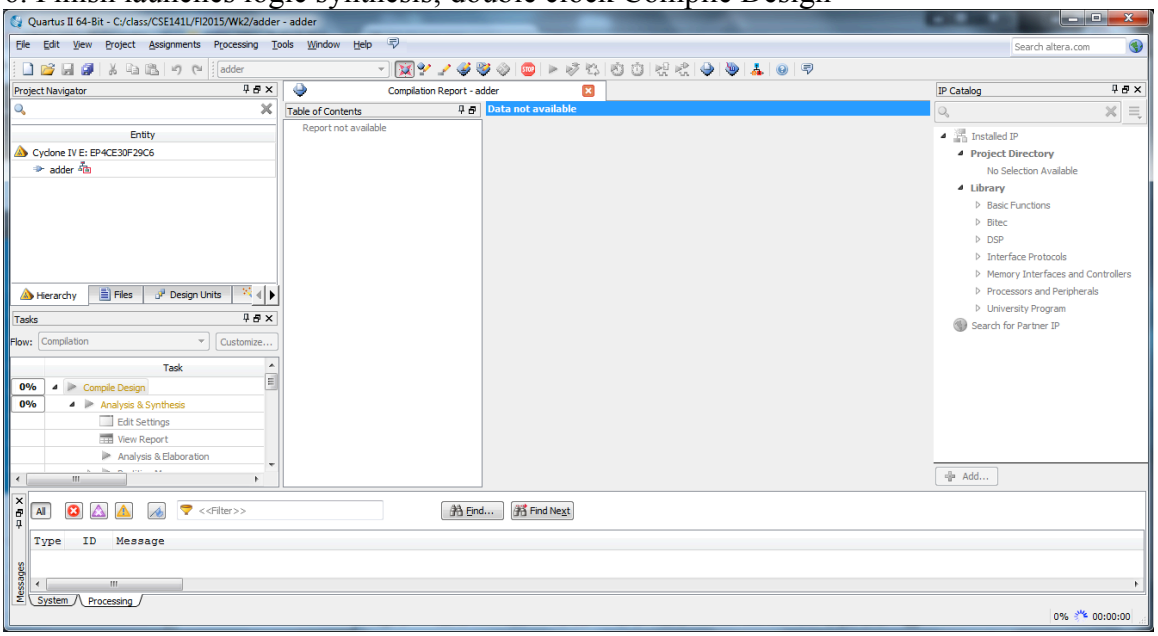
4. Choose device:



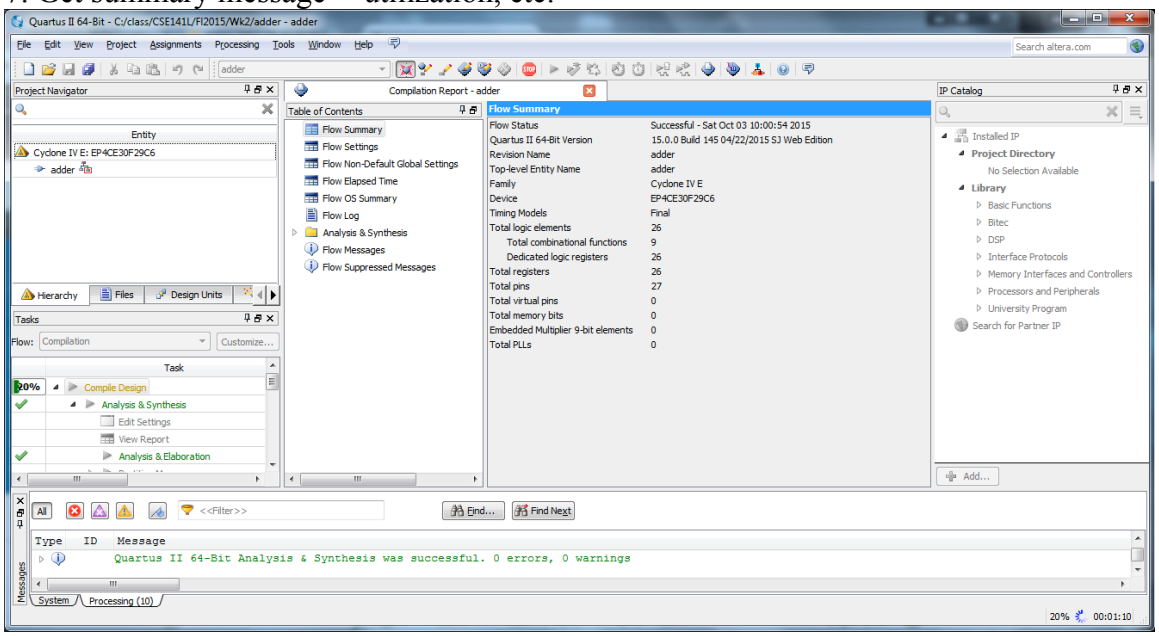
5. Choose SystemVerilog for simulation



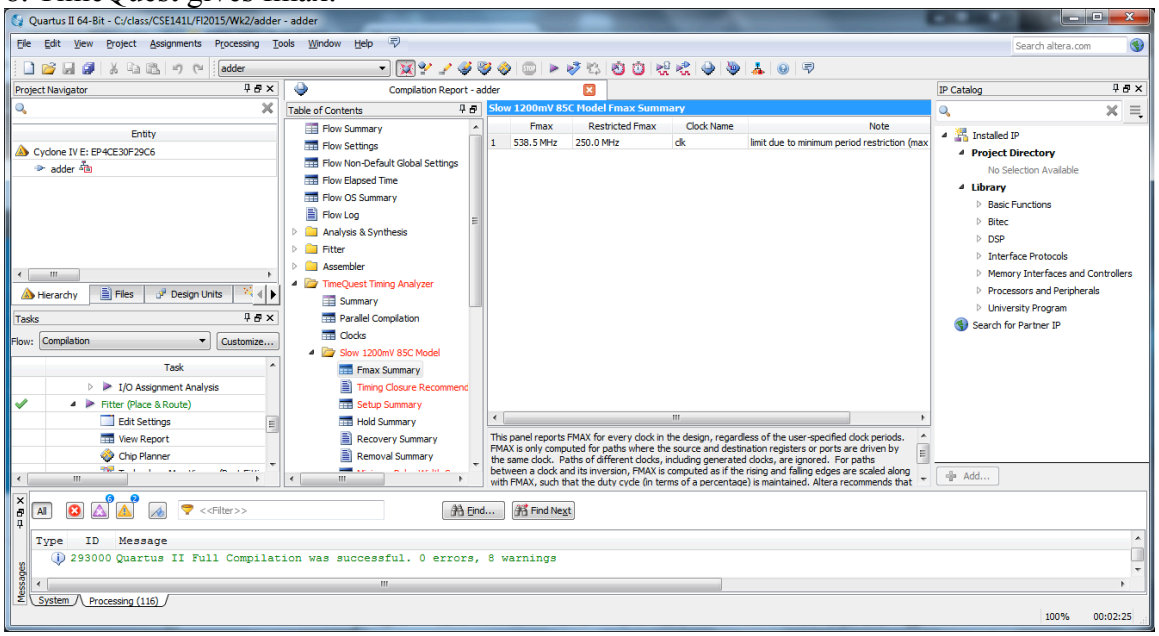
6. Finish launches logic synthesis; double clock Compile Design



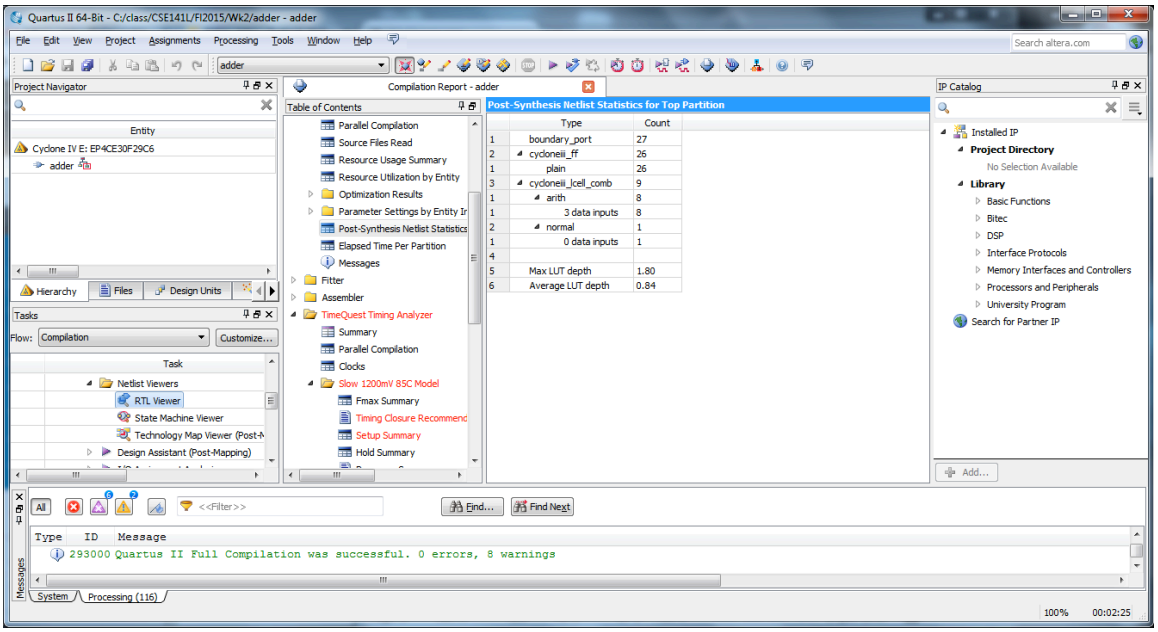
7. Get summary message -- utilization, etc.



8. TimeQuest gives fmax:



9. RTL viewer for schematic



10. Schematic -- can you read it back onto your ModelSim simulation timing diagram?