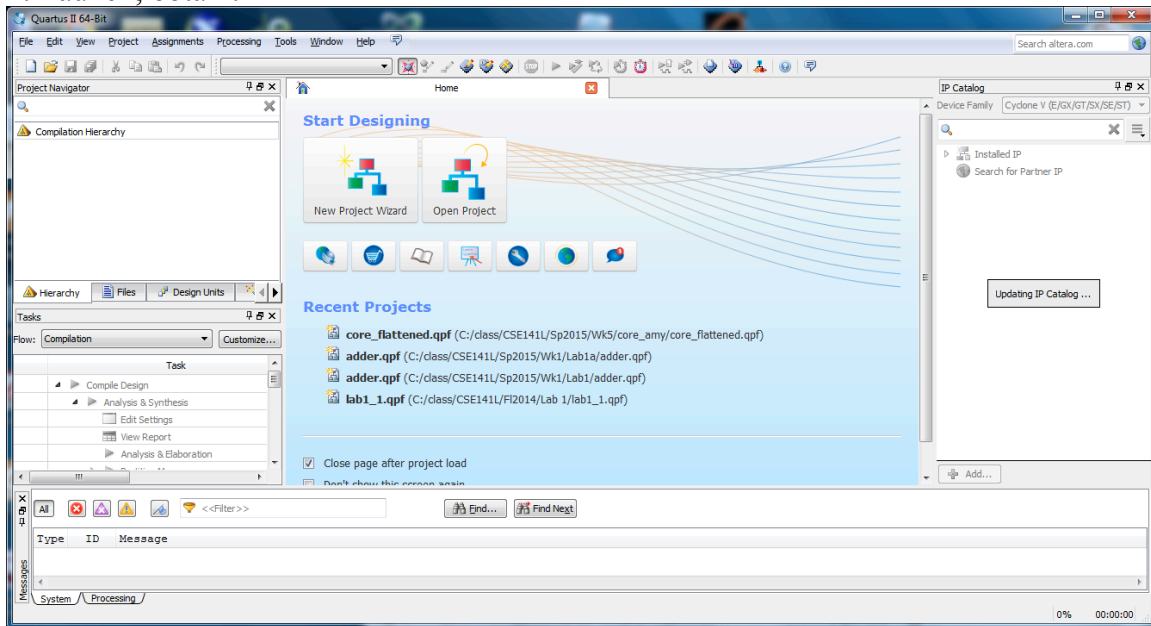
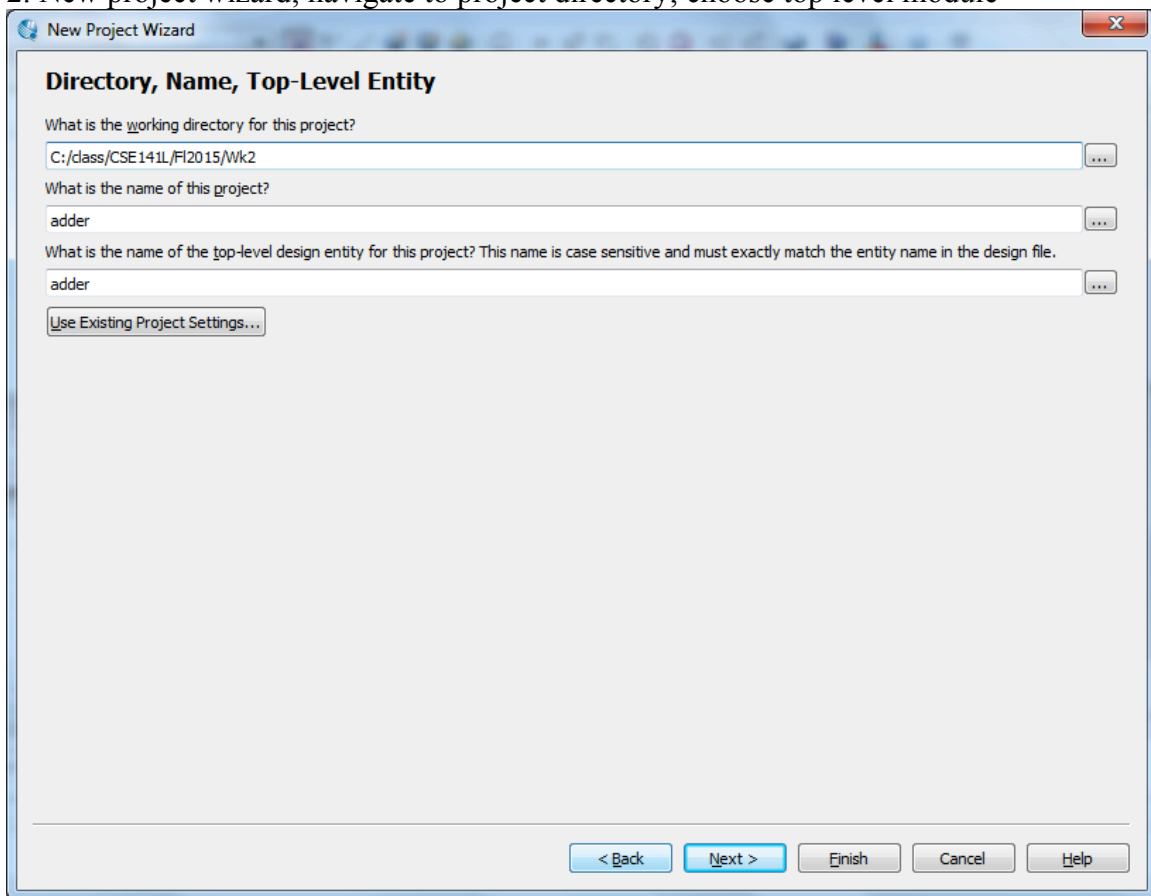


Using Quartus II

1. Launch; obtain:



2. New project wizard; navigate to project directory; choose top level module



The image shows a 'New Project Wizard' dialog box with a title bar containing a blue icon, the text 'New Project Wizard', and a red close button. The main area has a title 'Directory, Name, Top-Level Entity' in bold. It contains three text input fields, each with a browse button (three dots) to its right. The first field is labeled 'What is the working directory for this project?' and contains the path 'C:/class/CSE141L/FI2015/Wk2'. The second field is labeled 'What is the name of this project?' and contains 'adder'. The third field is labeled 'What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.' and contains 'adder'. Below these fields is a button labeled 'Use Existing Project Settings...'. At the bottom of the dialog are five buttons: '< Back' (disabled), 'Next >' (active/highlighted), 'Finish' (disabled), 'Cancel' (disabled), and 'Help' (disabled).

Directory, Name, Top-Level Entity

What is the working directory for this project?

C:/class/CSE141L/FI2015/Wk2

What is the name of this project?

adder

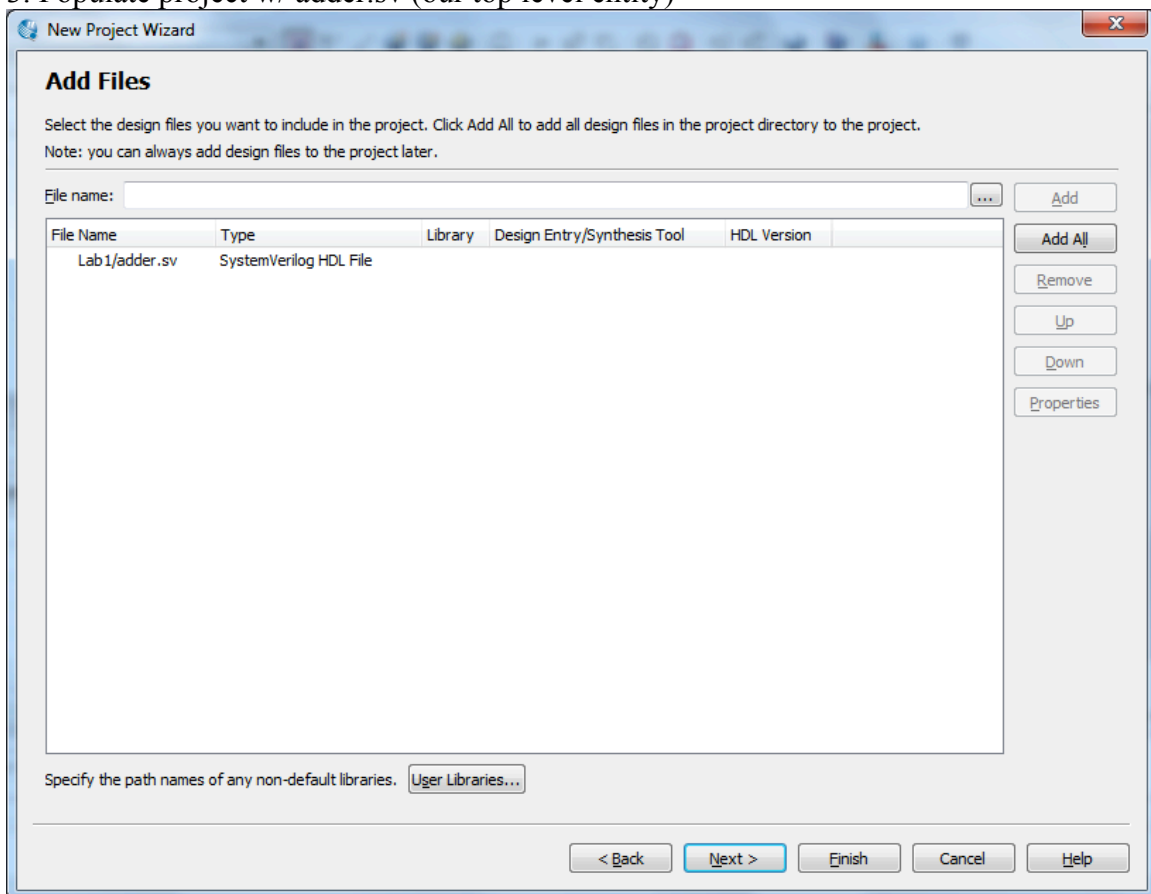
What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

adder

Use Existing Project Settings...

< Back Next > Finish Cancel Help

3. Populate project w/ adder.sv (our top level entity)



(would also include any lower level submodules -- none in this case)

4. Choose device:

New Project Wizard

Family & Device Settings

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus II software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: **Cyclone IV E**

Devices: **All**

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Show in 'Available devices' list

Package: **Any**

Pin count: **Any**

Core Speed grade: **Any**

Name filter:

☒ Show advanced devices

Available devices:

| Name | Core Voltage | LEs | Total I/Os | GPIOs | Memory Bits | Embedded multiplier 9-bit elements |
|---------------|--------------|-------|------------|-------|-------------|------------------------------------|
| EP4CE30F23I8L | 1.0V | 28848 | 329 | 329 | 608256 | 132 |
| EP4CE30F29C6 | 1.2V | 28848 | 533 | 533 | 608256 | 132 |
| EP4CE30F29C7 | 1.2V | 28848 | 533 | 533 | 608256 | 132 |
| EP4CE30F29C8 | 1.2V | 28848 | 533 | 533 | 608256 | 132 |
| EP4CE30F29C8L | 1.0V | 28848 | 533 | 533 | 608256 | 132 |
| EP4CE30F29C9L | 1.0V | 28848 | 533 | 533 | 608256 | 132 |
| EP4CE30F29I7 | 1.2V | 28848 | 533 | 533 | 608256 | 132 |
| EP4CE30F29I8L | 1.0V | 28848 | 533 | 533 | 608256 | 132 |
| EP4CE30U19A7 | 1.2V | 28848 | 329 | 329 | 608256 | 132 |

< Back Next > Finish Cancel Help

5. Choose SystemVerilog for simulation

New Project Wizard

EDA Tool Settings

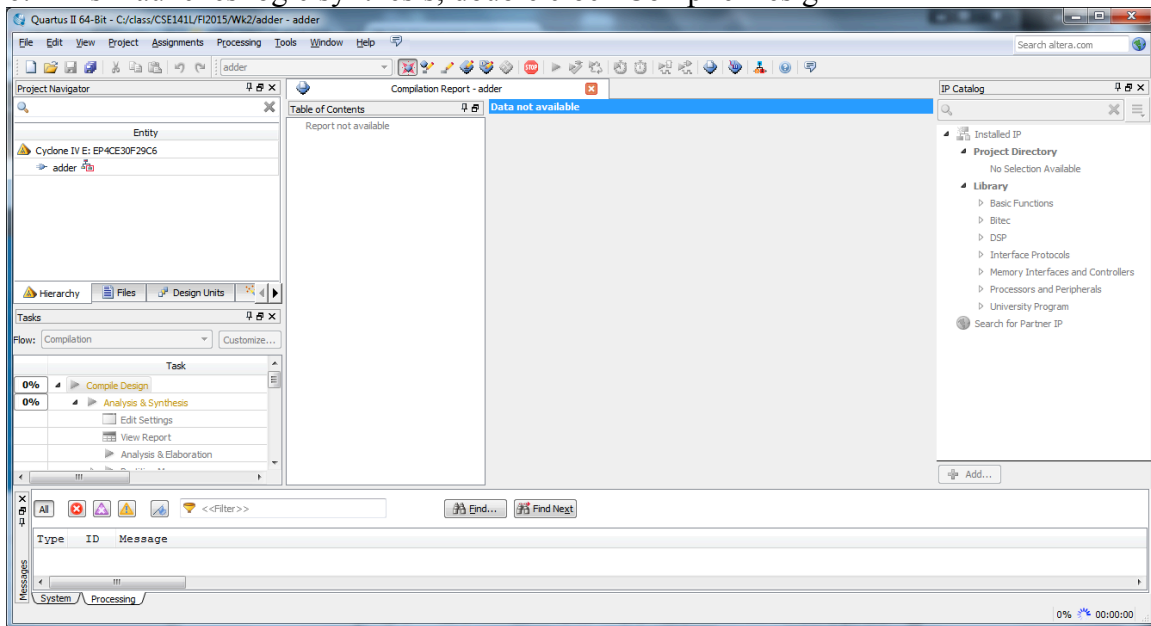
Specify the other EDA tools used with the Quartus II software to develop your project.

EDA tools:

| Tool Type | Tool Name | Format(s) | Run Tool Automatically |
|------------------------|------------------|-------------------|---|
| Design Entry/Synthesis | <None> | <None> | <input type="checkbox"/> Run this tool automatically to synthesize the current design |
| Simulation | ModelSim-Altera | SystemVerilog HDL | <input checked="" type="checkbox"/> Run gate-level simulation automatically after compilation |
| Formal Verification | <None> | | |
| Board-Level | Timing | <None> | |
| | Symbol | <None> | |
| | Signal Integrity | <None> | |
| | Boundary Scan | <None> | |

< Back Next > Finish Cancel Help

6. Finish launches logic synthesis; double click Compile Design



7. Get summary message -- utilization, etc.

The screenshot shows the Quartus II 64-Bit interface with the 'Compilation Report - adder' open. The 'Flow Summary' tab is selected, displaying the following data:

| Flow Status | Successful - Set Oct 03 10:00:54 2015 |
|------------------------------------|--|
| Quartus II 64-Bit Version | 15.0.0 Build 145 04/22/2015 SJ Web Edition |
| Revision Name | adder |
| Top-level Entity Name | adder |
| Family | Cyclone IV E |
| Device | EP4CE30F29C6 |
| Timing Mode | Final |
| Total logic elements | 26 |
| Total combinational functions | 9 |
| Dedicated logic registers | 26 |
| Total registers | 26 |
| Total pins | 27 |
| Total virtual pins | 0 |
| Total memory bits | 0 |
| Embedded Multiplier 9-bit elements | 0 |
| Total PLLs | 0 |

The 'Messages' window at the bottom shows: 'Quartus II 64-Bit Analysis & Synthesis was successful. 0 errors, 0 warnings'.

8. TimeQuest gives fmax:

The screenshot shows the Quartus II 64-Bit interface with the 'Compilation Report - adder' open. The 'TimeQuest Timing Analyzer' tab is selected, displaying the following table:

| Fmax | Restricted Fmax | Clock Name | Note |
|------|-----------------|------------|--|
| 1 | 538.5 MHz | 250.0 MHz | clk |
| | | | limit due to minimum period restriction (max |

The 'Messages' window at the bottom shows: '299000 Quartus II Full Compilation was successful. 0 errors, 8 warnings'.

9. RTL viewer for schematic

The screenshot displays the Quartus II 64-bit IDE interface for a project named 'adder'. The main window shows the 'Post-Synthesis Netlist Statistics for Top Partition' report. The report includes a table of statistics and a list of tasks in the left pane.

Table of Contents:

- Parallel Compilation
- Source Files Read
- Resource Usage Summary
- Resource Utilization by Entity
- Optimization Results
- Parameter Settings by Entity
- Post-Synthesis Netlist Statistics
- Elapsed Time Per Partition
- Messages
- Fitter
- Assembler
- TimeQuest Timing Analyzer
- Summary
- Parallel Compilation
- Clocks
- Slow 1200mV 85C Model
- Fmax Summary
- Timing Closure Recommendation
- Setup Summary
- Hold Summary

Post-Synthesis Netlist Statistics for Top Partition:

| Type | Count |
|---------------------|-------|
| boundary_port | 27 |
| cycloneii_ff | 26 |
| plain | 26 |
| cycloneii_cell_comb | 9 |
| arith | 8 |
| 3 data inputs | 8 |
| normal | 1 |
| 0 data inputs | 1 |
| Max LUT depth | 1.80 |
| Average LUT depth | 0.84 |

Tasks:

- Netlist Viewers
 - RTL Viewer
 - State Machine Viewer
 - Technology Map Viewer (Post-Mapping)
 - Design Assistant (Post-Mapping)

Messages:

293000 Quartus II Full Compilation was successful. 0 errors, 8 warnings

10. Schematic -- can you read it back onto your ModelSim simulation timing diagram?

