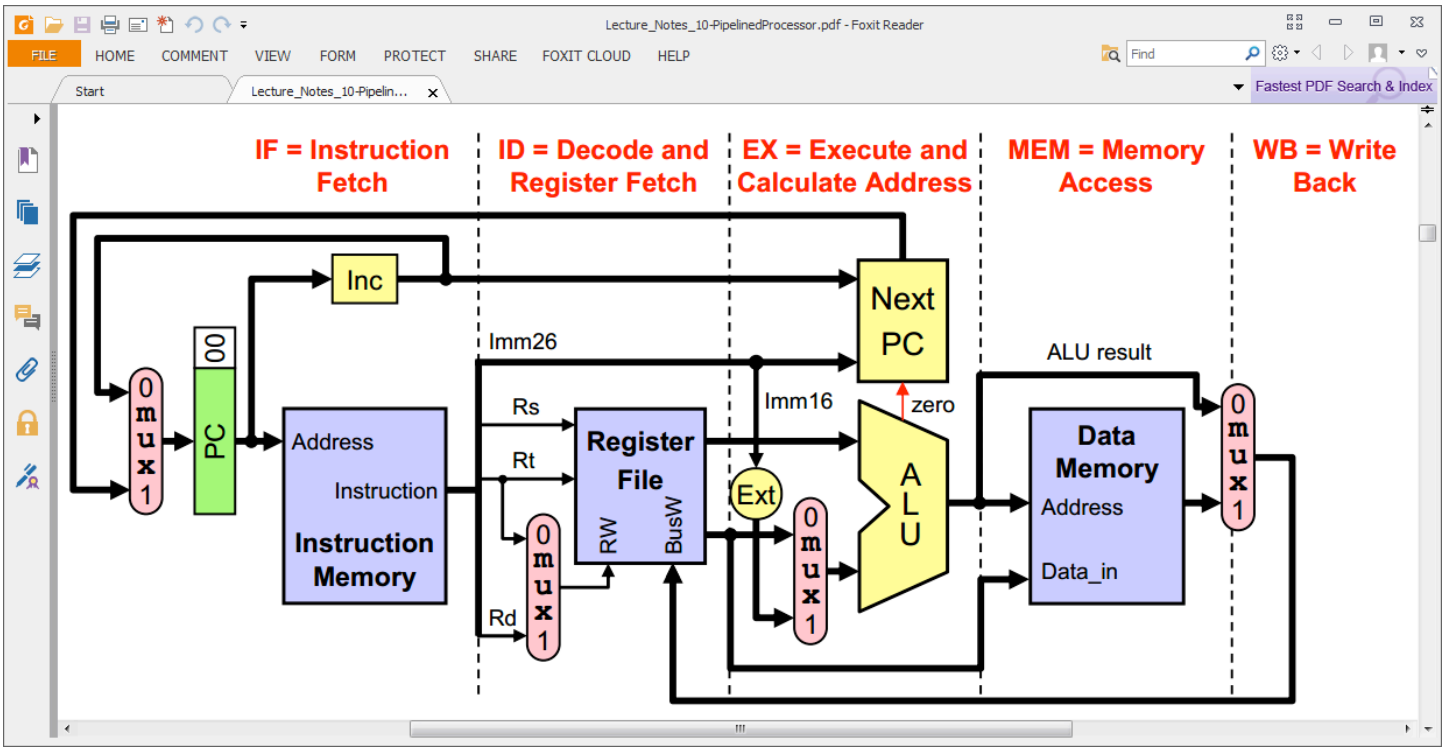
Baseline MIPS Architecture



Baseline MIPS /Architecture

Left side: PC increments or branches/jumps
Width is same as that of Instr mem Address (below)

Instr mem: Simple lookup table
Our input (Address) is as wide as you need (same as PC, above)
Depth = 2**Address -- or Width(Address) = $clog2(Depth)
Our instruction (output of Instr mem) is 9 bits wide, not 16 or 26

Reg file: Pointers Rs, Rt ($clog2(16) = 4 bits wide for us)
Data Input BusW 8 bits wide
Dual Data Outputs to ALU 8 bits wide
Ours is 8 bits wide, 16 elements deep

ALU: (a.k.a. Execute)
Two inputs, one output (you may have more inputs)
8-bit data paths
You will probably want a carry/shift out and a carry/shift in
You may have any flags: zero, equal operand, negative, etc.

Data mem: Single address port
8 bit data in
8 bit data out

Note muxes which facilitate store reg file from data mem vs. ALU
You may also wish to route data from ALU into mem directly

Baseline Architecture With One-bit Shift / Carry Link Register