

Mahmoud Abumandour

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EDUCATION

Simon Fraser University

Master of Science in Computer Science (CGPA: 4.0)

Sep 2022 - Present

BC, Canada

Mansoura University

Bachelor of Computer and Communication Engineering (CGPA: 3.96, ranked first)

Sep 2017 – Jul 2022

Mansoura, Egypt

PROFESSIONAL EXPERIENCE

Simon Fraser University

Graduate Research Assistant

BC, Canada

Sep 2022 – Present

- Investigate the impacts of different model compression schemes on the privacy and accuracy of machine learning models

Teaching Assistant

Jan 2023 – Present

- Grading assignments and exams, holding office hours, and conducting weekly lab sessions for more than 20 students (CMPT 295: Introduction to computer systems, CMPT 379: Principles of compiler design)

Google

Remote

Software Developer (Google Summer of Code, RTEMS)

May 2022 – Sep 2022

- Achieved 8x speedup over the previous release notes generator by using a multi-threaded architecture
- Automated manual Markdown and RST to PDF generation after fetching release data from RTEMS bug tracker

Software Developer (Google Summer of Code, QEMU)

May 2021 – Aug 2021

- Implemented multi-core, multi-level cache performance evaluation of user-space and full-system workloads
- Improved the system call tracing plugin by making its reports more script-friendly for post-processing

Master Micro

Cairo, Egypt

Software Engineering Intern

Sep 2022 – Present

- Designed a database format for the Design Database (DDB) file, reducing average query time by 50%
- Participated in code review and testing. Increased the testing coverage of the data querying subsystem by 10%

PROJECTS

- Fuzzing using RISC-V Emulation:** Developed a RISC-V 64-bit emulator suitable for fuzzing, increasing test generation throughput by over 20x over single-core performance
- Database Engine:** Implemented a disk-oriented database management system with partial SQL-compliance, in-memory buffer pool caching, B+ Tree indexing, and Java Database Connectivity (JDBC) driver
- AES Encryption Core:** Designed a low-power AES core for FPGA. Reduced area and power consumption by 86% over a high-throughput pipelined design
- Hyperthreaded, Software-Interlocked MIPS Processor:** A multi-threaded five-stage pipelined MIPS processor for FPGA and a custom assembler. Increased throughput by roughly 5x over single-threaded execution

SKILLS

Programming Languages: C++, C, x86 Assembly, Java, Python, Bash Scripting

Tools: CMake, Docker, git, Valgrind, Wireshark

Platforms: Linux, QEMU, FPGA, ARM Cortex M4, AVR

Hardware Design Tools: Xilinx Vivado, SystemVerilog, VHDL

OPEN-SOURCE CONTRIBUTIONS

- SerenityOS:** Defined a global OS versioning API. Increased user-space utilities POSIX compliance. Improved the SerenityOS DBMS SQL compliance by supporting INSERTs with multiple tuples and table-description statements
- QEMU:** Modernized the usage of locking and memory allocation APIs by using scope-based locks and automatically freed allocations. Deprecated TCG plugins command line syntax and implemented new one that's like modern QEMU CLI syntax