Mahmoud Abumandour

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Education

Simon Fraser University **Sep 2022 – Aug 2024**
Master of Science in Computer Science (GPA: 4.0) *BC, Canada*

Mansoura University **Sep 2017 – Jul 2022**
Bachelor of Computer and Communication Engineering (GPA: 3.96, ranked first) *Mansoura, Egypt*

Professional Experience

Simon Fraser University **BC, Canada**
Graduate Research Assistant ***Sep 2022 – Present***

- Investigate bit-flip attacks against deep learning models and the effect of model quantization on attack and defense strategies

Teaching Assistant ***Jan 2023 – Present***

- Courses: CMPT 295: Intro to computer systems & CMPT 379: Principles of compiler design

Google Summer of Code **Remote**
Real-Time Executive for Multiprocessor Systems (RTEMS) ***May 2022 – Sep 2022***

- Achieved 8x speedup over the previous release notes generator by using a multi-threaded architecture
- Automated manual Markdown and RST to PDF generation after fetching release data from RTEMS bug tracker

QEMU ***May 2021 – Aug 2021***

- Implemented multi-core, multi-level cache performance emulation of user-space and full-system workloads
- Improved the system call tracing plugin by making its reports more script-friendly for post-processing

Master Micro **Cairo, Egypt**
Software Engineering Intern ***Oct 2021 – Feb 2022***

- Designed a database format for the main design lookup table file, reducing average query time by 50%
- Participated in code review and testing. Increased the testing coverage of the data querying subsystem by 10%

Projects

- **Fuzzing using RISC-V Emulation**: Developed a RISC-V 64-bit emulator suitable for fuzzing, increasing test generation throughput by over 20x over single-core performance
- **Database Engine**: Implemented a disk-oriented database management system with partial SQL-compliance, in-memory buffer pool caching, B+ Tree indexing, and Java Database Connectivity (JDBC) driver
- **AES Encryption Core**: Designed a low-power AES core for FPGA. Reduced area and power consumption by 86% over a high-throughput pipelined design
- **Hyperthreaded, Software-Interlocked MIPS Processor**: A multi-threaded five-stage pipelined MIPS processor for FPGA and a custom assembler. Increased throughput by roughly 5x over single-threaded execution

Skills

Programming Languages: C++, C, x86 Assembly, Java, Python, Bash Scripting

Tools: CMake, Docker, git, Valgrind, Wireshark

Platforms: Linux, QEMU, FPGA, ARM Cortex M4, AVR

Hardware Design Tools: Xilinx Vivado, ModelSim, SystemVerilog, VHDL

Open-Source Contributions

- **SerenityOS**: Defined a global OS versioning API. Increased user-space utilities POSIX compliance. Improved the SerenityOS DBMS SQL compliance by supporting INSERTs with multiple tuples and table-description statements
- **QEMU**: Modernized the usage of locking and memory allocation APIs by using scope-based locks and automatically freed allocations. Redefined plugins' command line syntax adhering to modern QEMU CLI syntax