Module: Comparator (used in SAR ADC)

Designer: Qiaochu Zhang, Ming Hsieh Dept. of ECE, USC (qiaochuz@usc.edu)

Module Description: Strong arm comparator with PMOS input differential pair and reset.

Top Cell Name: comparator_p

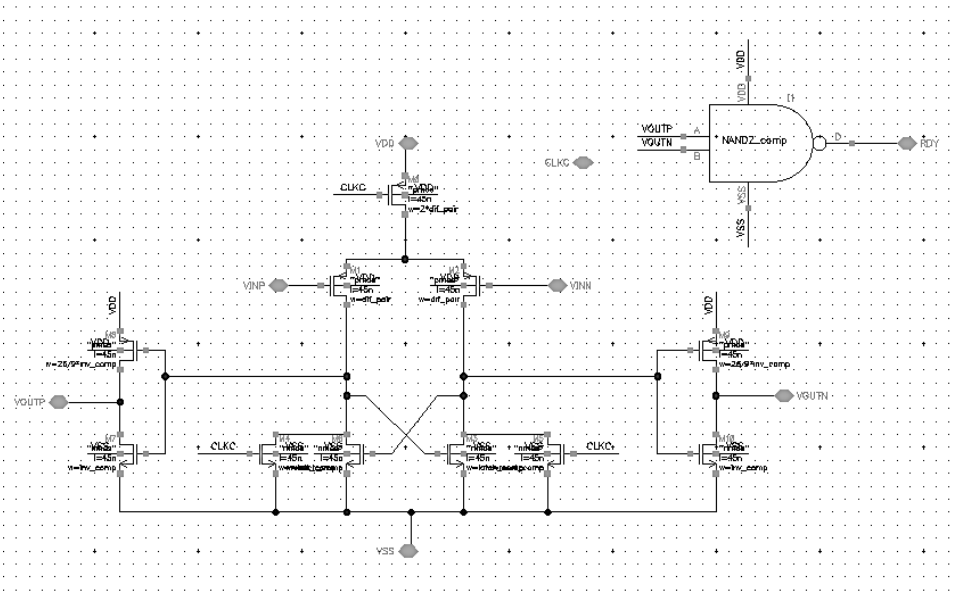
Technology: PTM 45nm CMOS

PINS:

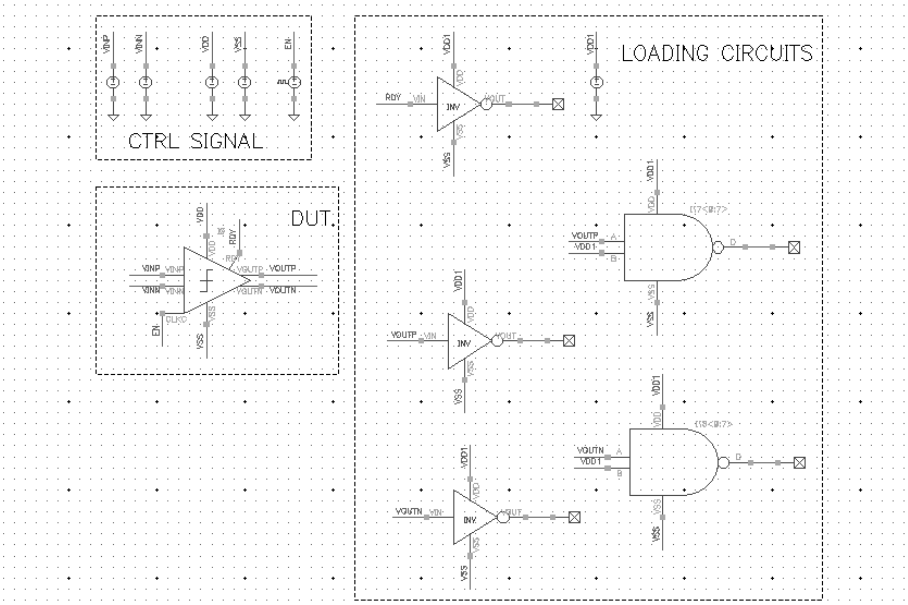
Pin Lists	
VDD	Supply Voltage
VSS	ground
CLKC	Reset signal
RDY	Ready signal
VINP, VINN	Input voltage node
VOUTP, VOUTN	Output voltage node

Schematic Netlists: comparator_p.scs

Schematic figures:



Testbenches: tb_comparator_p.scs



Parameters:

Parameters	Symbols
Input differential pair transistors width (m)	dif_pair
Latch transistor width (m)	$latch\_comp$
NAND transistor width in comparator (m)	$nand\_comp$
Inverter transistor width in comparator (m)	inv_comp
Inverter transistor width in loading circuit (m)	inv
NAND transistor width in loading circuit (m)	$nand\_w$

Metrics:

Metrics	Symbols
Regenration time (s)	Regen_time
Standard deviation of noise (V)	sigma_noise
Power consumption (W)	avg_power

Neural Network Model:

The H5 file: reg_comparator45.h5

The Json File: model_comparator45.json

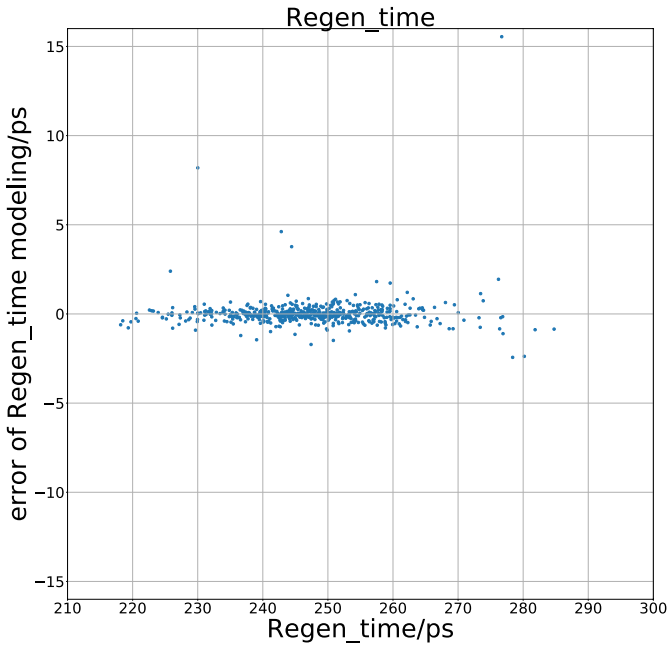
The Input Normalization File: scX_comparator45.pkl

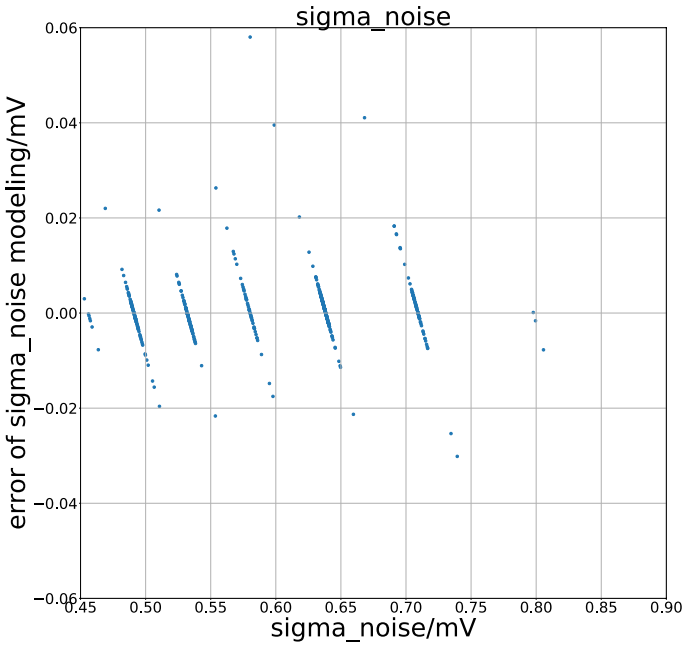
The Output Standardization File: scY_comparator45.pkl

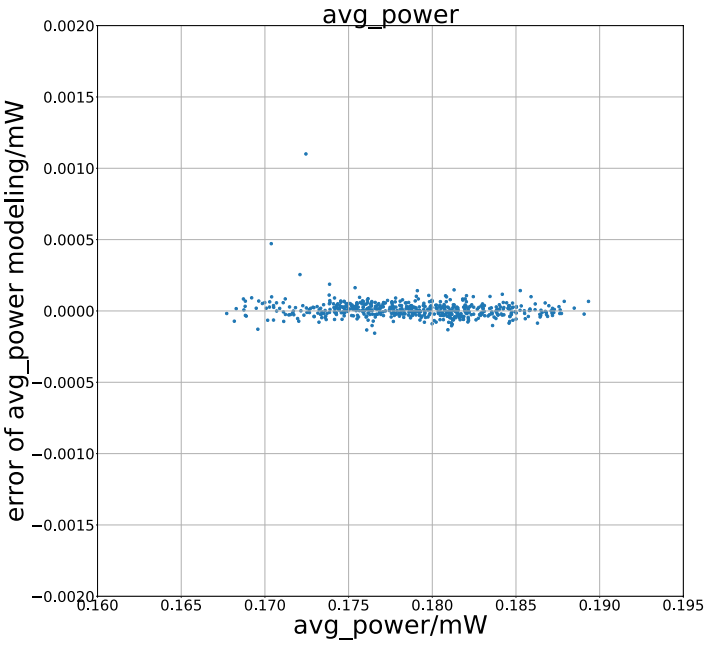
The input characterization range of the Model:

Design parameters	
Symbols	Characterization Range
dif_pair	[500nm, 540nm]
$latch\_comp$	[160nm, 200nm]
$nand\_comp$	[160nm, 200nm]
inv_comp	[160nm, 200nm]
inv	[160nm, 200nm]
$nand\_w$	[160nm, 200nm]

The error range of the Model:




sigma_noise
error of sigma_noise modeling/mV
sigma_noise/mV
0.06
0.04
0.02
0.00
−0.02
−0.04
−0.06
0.45
0.50
0.55
0.60
0.65
0.70
0.75
0.80
0.85
0.90


avg_power
error of avg_power modeling/mW
avg_power/mW
0.0020
0.0015
0.0010
0.0005
0.0000
−0.0005
−0.0010
−0.0015
−0.0020
0.160
0.165
0.170
0.175
0.180
0.185
0.190
0.195