Changes from last revision

Date	User	Edits
12/14/2019	Mostafa Ayesh	Specifications; Schematic and description of testbench; Design examples;

Subsystem or block descriptions

Design name	RF Front-End in TSMC 28nm CMOS
The Top-level cell name	RF_FrontEnd.scs
Designer	Mostafa Ayesh
Organization	University of Southern California

Overview

A Common Source Low Noise Amplifier (LNA) with an Inductive Load followed by a source follower RF buffer. The output signal from the LNA block is then forwarded to a bootstrapped sample-and-hold circuit to sample it and do the frequency conversion.

Block Specifications and Compliance

Spec Name	Min	Max	Note
Center Frequency (GHz)	25	28	\
S/H Tracking BW (GHz)	20	35	\
SFDR (dB)	40	70	\
ENOB (bit)	4	9	\
Power Consumption (mW)	11	16	\

Block diagram

The block diagram representation of the design is as follows:

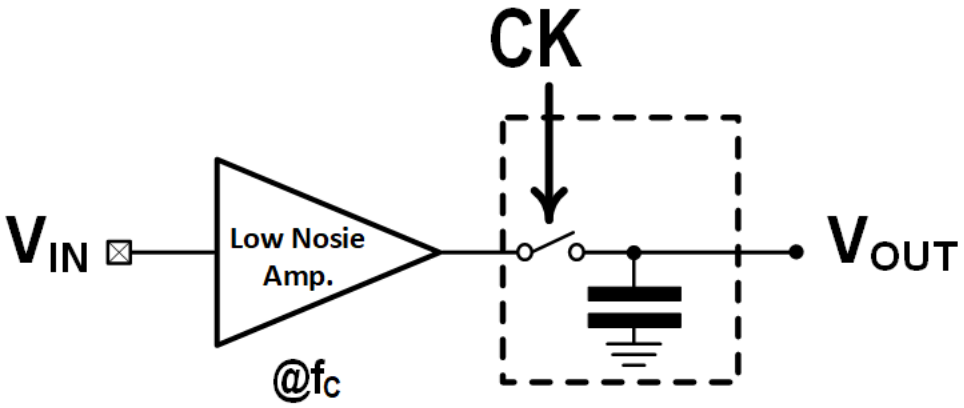


Figure 1: Architecture of the RF Front-End with AMPSE

Main analog modules	Regression models			
LNA	model_lna28.json	reg_lna28.h5	scX_lna28.pkl	scY_lna28.pkl
Track and Hold	model_sh28.json	reg_sh28.h5	scX_sh28.pkl	scY_sh28.pkl

Signal list

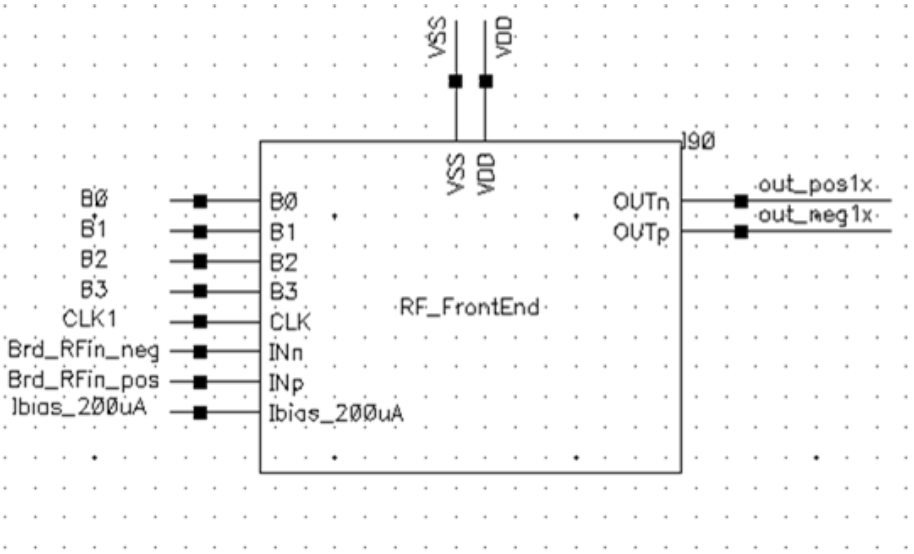


Figure 2: Symbol of the Top-Level of the RF Front-End

Signal Pins	Direction (I/O)	Type (supply, ground, analog current, analog voltage, digital voltage)	Max Voltage (core, IO or max voltage)	Specification
VDD	I	Supply	Core	Power Supply, 1.0 V
VSS	I	Ground	Core	Ground
CLK	I	Analog voltage	Core	Input Clock
INn, INp	I	Analog voltage	Core	Differential Analog Input
Ibias_200uA	I	Analog Current	Core	Input Bias Current
OUTn, OUTp	O	Analog voltage	Core	Differential Analog Output
B<0:3>	I	Digital voltage	Core	Setting Biasing Current

Design Hierarchy

The tabular description below corresponds to design hierarchy:

Category	Cell Name	Description	Figure
RF_FrontEnd_v1	LNA_28	Low Noise Amplifier	Figure. A1
	SH_28	Bootstrapped S/H	Figure. A2

Test Bench

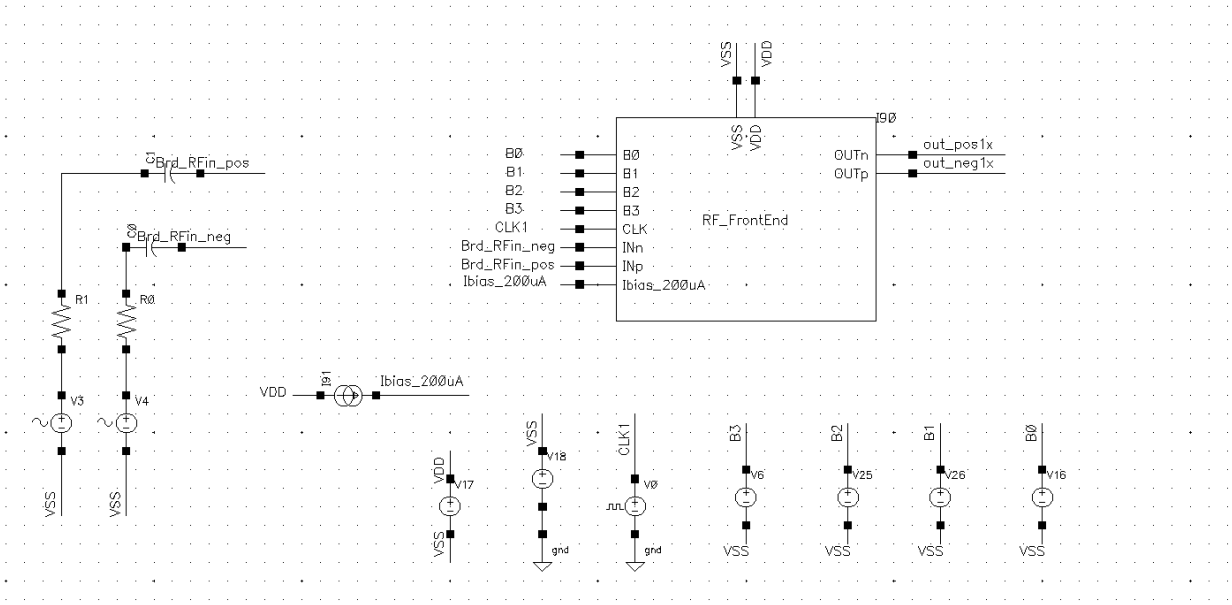


Figure 3: The Test Bench Used for the top-level RF-Front End

Cell Name	Note	
test_SH28	Transient simulation for 1. SNR 2. SFDR 3. ENOB 4. Average Power Consumption 5. Peak-to-peak Output Voltage	AC simulation for: 1. Tracking Bandwidth
test_LNA28	Transient simulation for 1. SNR 2. SFDR 3. ENOB 4. Average Power Consumption	AC simulation for: 1. Bandwidth 2. Center Frequency 3. Gain Rout

Simulations (test_ RF_FrontEnd_v1):

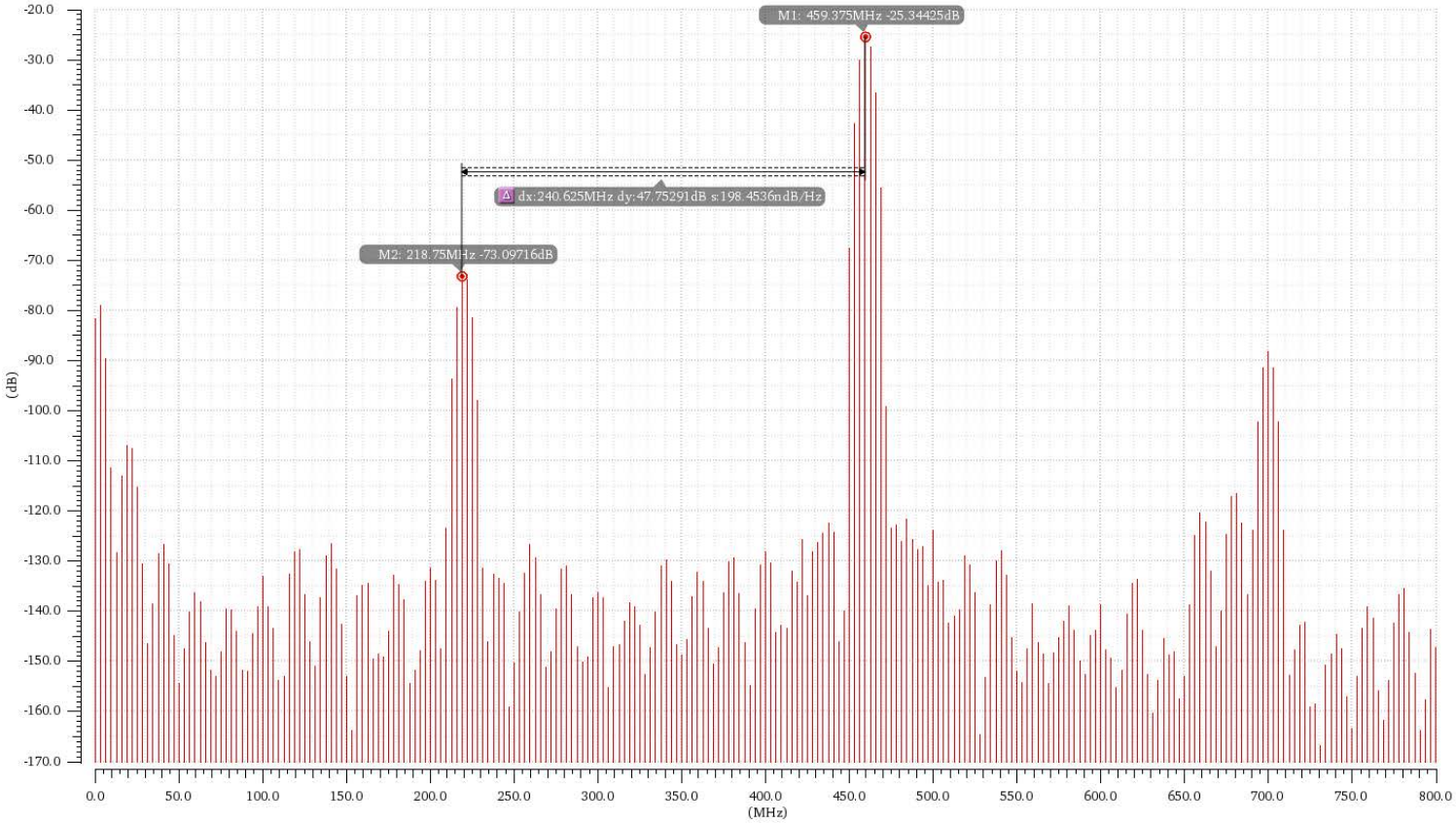
Conditions/parameters	Values	Conditions/parameters	Values	Conditions/parameters	Values
Process corner	TT	B<0:3>	1111	L_Radius(um)	15
Temperature(°C)	27	W_nMos_Follower	15	fin_gnd_1	2
VDD(V)	1	W_pmos_in	30	fin_gnd_2	10
Input amplitude(V)	400m	fin_battery_cap	80	fin_main_sw	4
Input common mode voltage	AC-coupled input.	fin_sampling_cap	4	Fin_vdd_1	2
Fin_nmos_bootstrapped_clk_1	10	Fin_pmos_bootstrapped_clk_1	6	fs (GHz)	3.2

After running the different modules regressors and building the graph of the whole block, we get the candidate values of the parameters and the list of the expected metrics per module in order to achieve the required specs and their given constraints.

Example – 1								
LNA Parameters		LNA Metrics		SH Parameters		SH Metrics		Overall Expected Specs
Wpmos_in	24.577	Center Freq. (Hz)	30.86G	fin_main_sw	8.185	SH_Power (W)	109.37u	Are shaded in green
L_Radius(m)	9.455u	Rout (Ohm)	42.14	fin_sampling_Cap	76.84f	Output PP Amplitude (V)	0.955	
Cin_OD(F)	76.84f	LNA_Power (mW)	13.92	frf(Hz)	30.86G	Tracking Bandwidth (GHz)	18.96	
Wnmos_follower	20.187	Gain (dB)	-0.8	fin_battery_cap	49.86	ENOB (bit)	7.21	
		SFDR (dB)	54	Rout_LNA (Ohm)	42.14	SNR (dB)	44.1	
		SNR (dB)	57.9			SFDR (dB)	44.77	
		ENOB (bit)	9.27					

Example – 1: Verifying Using Cadence Virtuoso®	
Overall Achieved Metrics	
Overall Power Consumption (W)	13.85m
Output PP Amplitude (V)	370m
Tracking Bandwidth (GHz)	23.5
ENOB (bit)	7.53
SNR (dB)	47.11
SFDR (dB)	48
Center Frequency (GHz)	30.55

The resulted metrics out from Cadence seems to give a quite matched result from the AMPSE. Simulations in Cadence Virtuoso were done in a moderate mode and using aps++, this might add some inaccuracy to the results.



Appendix

The schematics of the two modules used within the RF-frontend are shown below

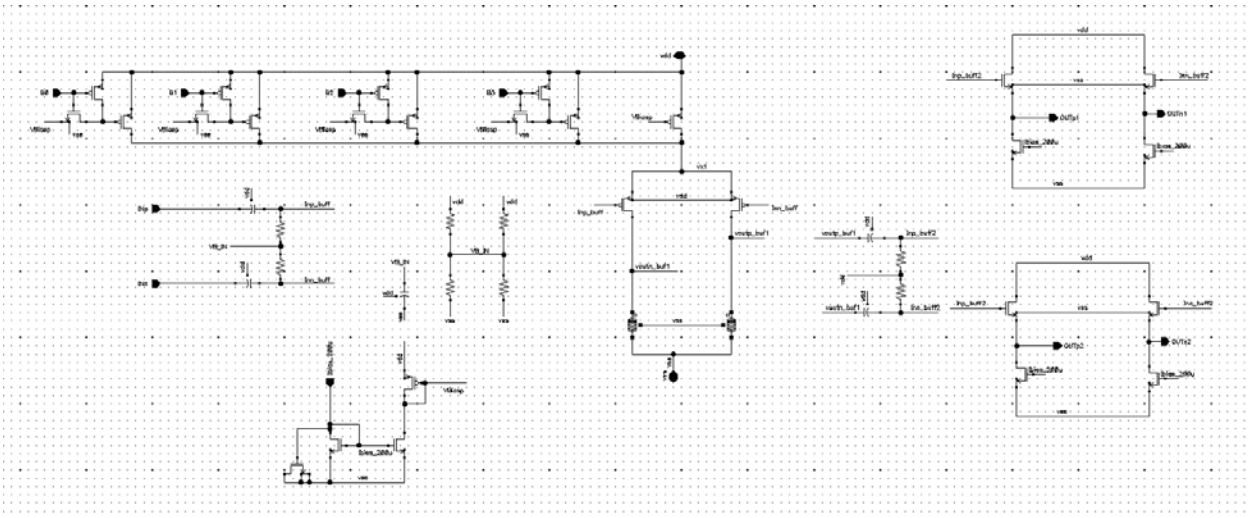


Figure A.1: The Circuit Schematic of the LNA

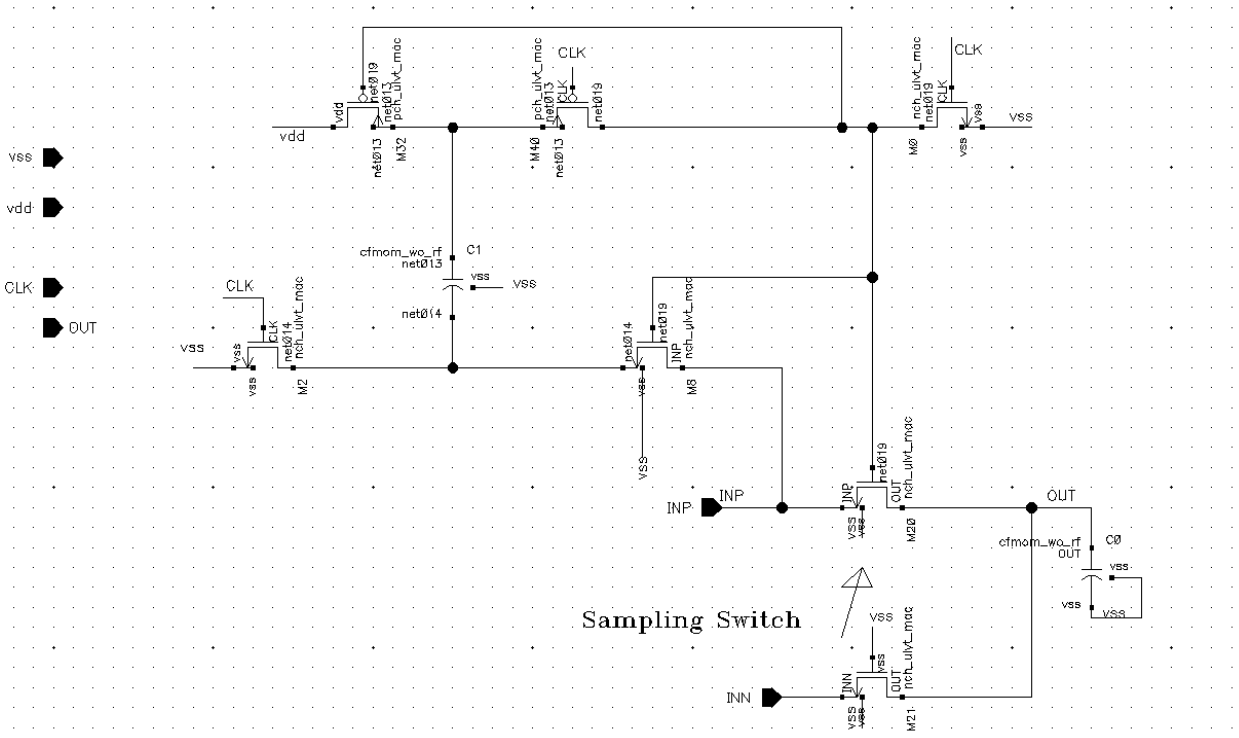


Figure A.2: The Circuit Schematic of the Bootstrapped Sample-and-Hold circuit

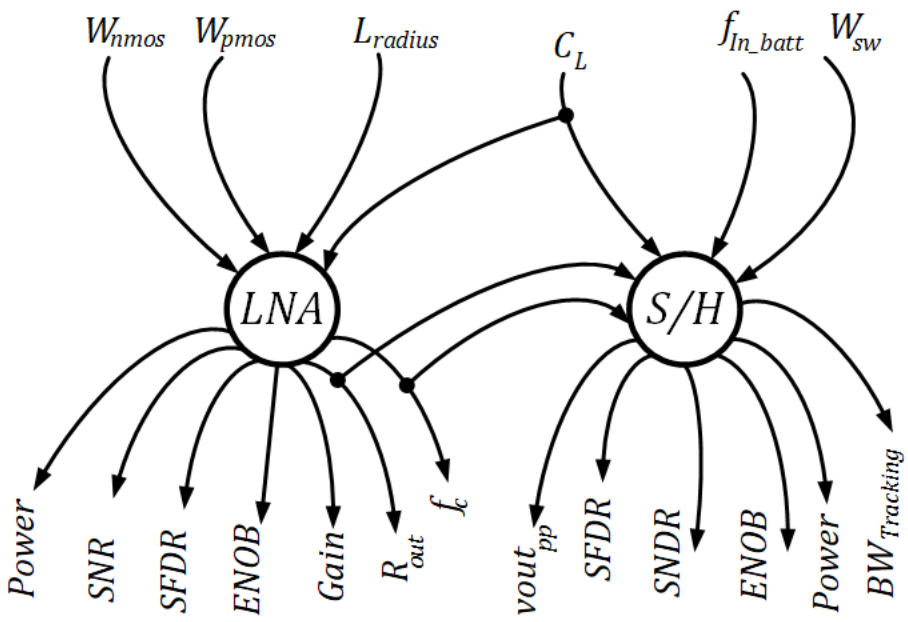
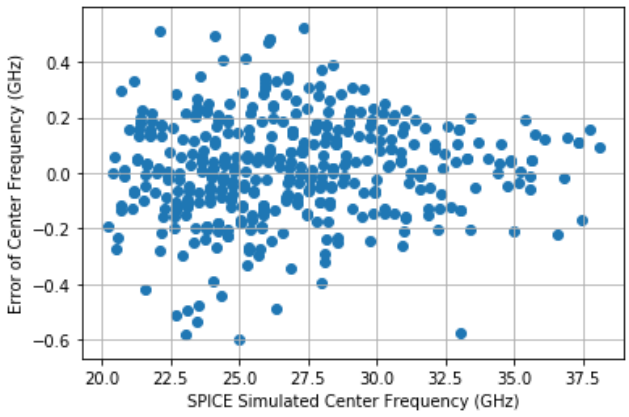
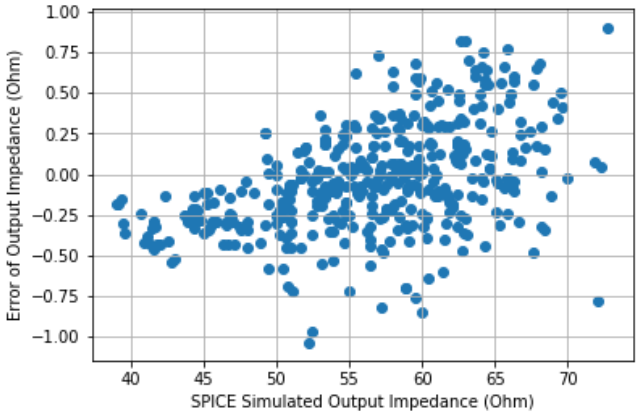


Figure A.3: The Graph Used to Model the Two Modules Together

The error range of the LNA Model:





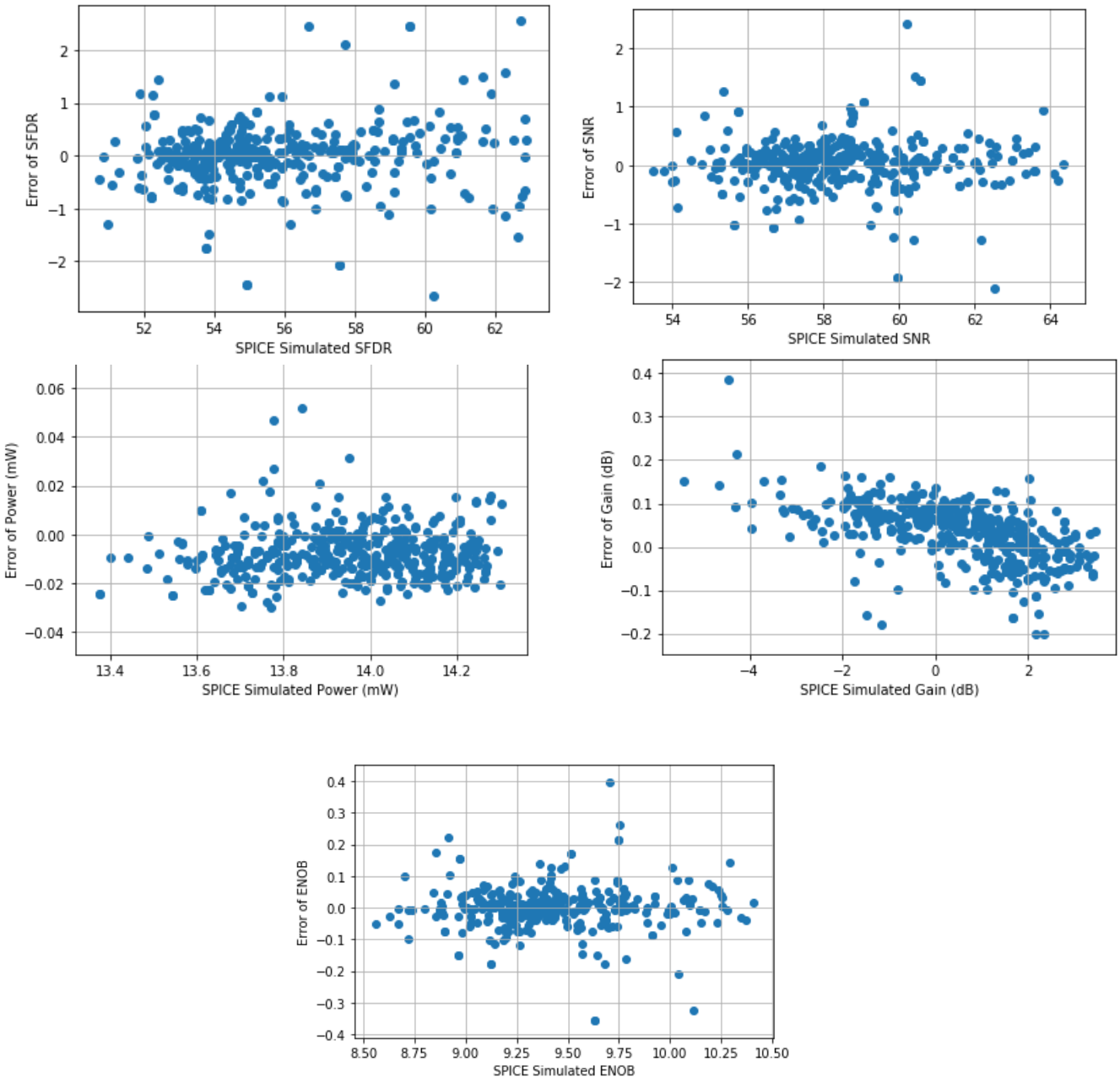


Figure A.4: The Error in Different Metrics of the LNA

The error range of the bootstrapped-SH Model:

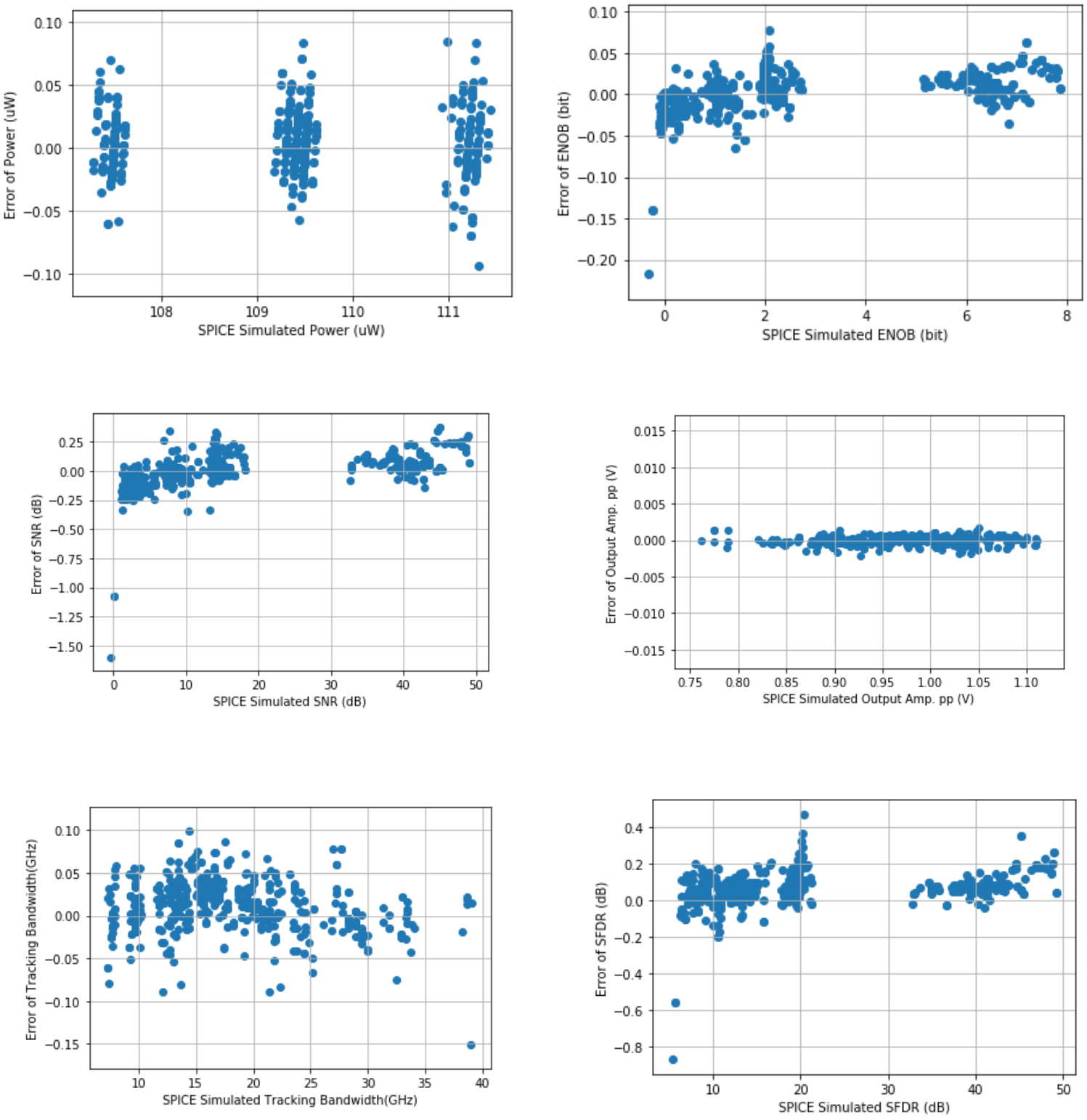


Figure A.5: The Error in Different Metrics of the Bootstrapped S/H