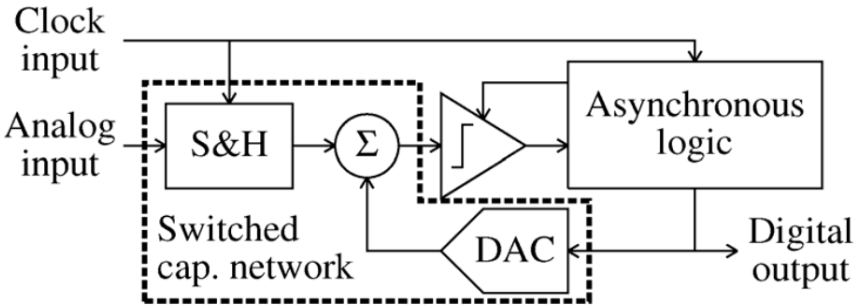
Design of Asynchronous SAR ADC in PTM 45nm CMOS using AMPSE Tool

I. Introduction

In this design an 8-bit 150MS/s SAR ADC has been implemented using the AMPSE Tool

SAR Architecture:



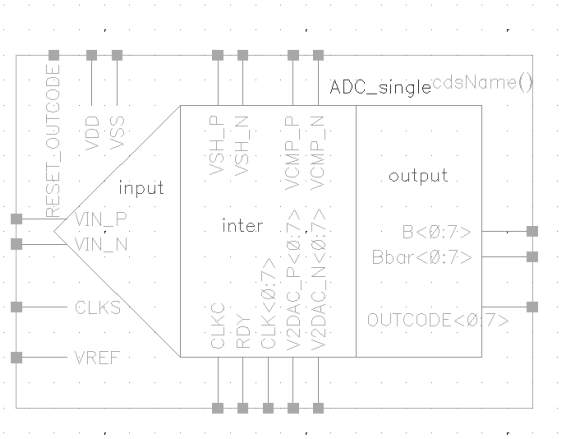
Architecture of Single SAR ADC

The major blocks in the design are:

- Bootstrap sampler and Capacitive DAC
- Comparator
- SAR logic

Description:

The Top-level cell: Chip_core – An 8-bit 150MS/s SAR ADC

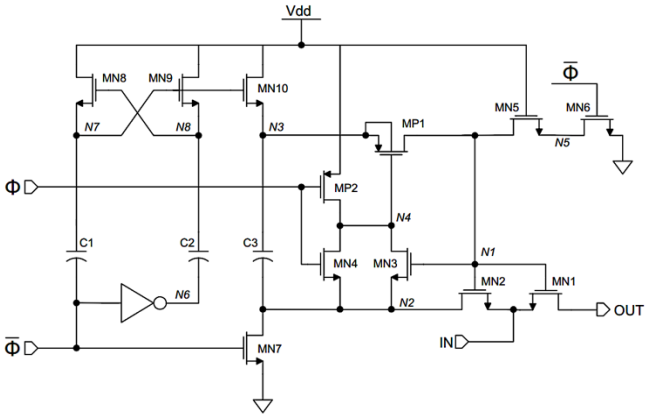


Pin Configuration:

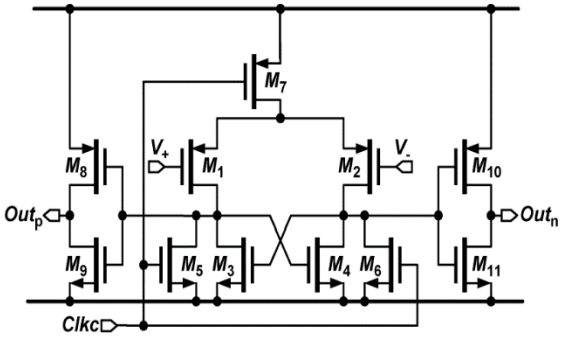
Pin Name	**Input or output**	**Specification**
VDD	Input	Power Supply, 1.1V
VSS	Input	Ground
CLK_S	Input	Input Clock 150MHz, 20% duty cycle
VREF	Input	Reference voltage, 1V
VIN_P, VIN_N	Input	Differential input signal, common mode voltage 0.55V
RESET_OUTCODE	Input	Reset output latch
OUTCODE<0:7>	output	8-bit output code

Schematic of cells

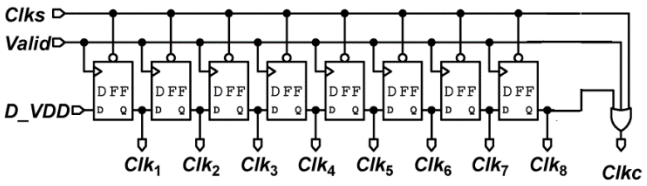
Schematic of bootstrap sampler



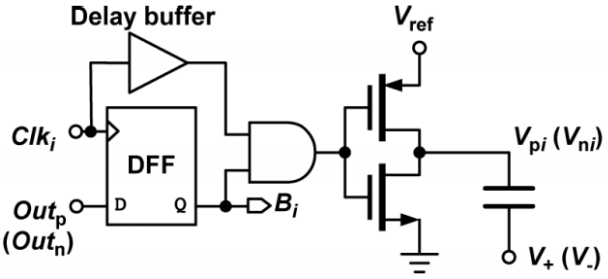
Schematic of comparator



Schematic of SAR control logic

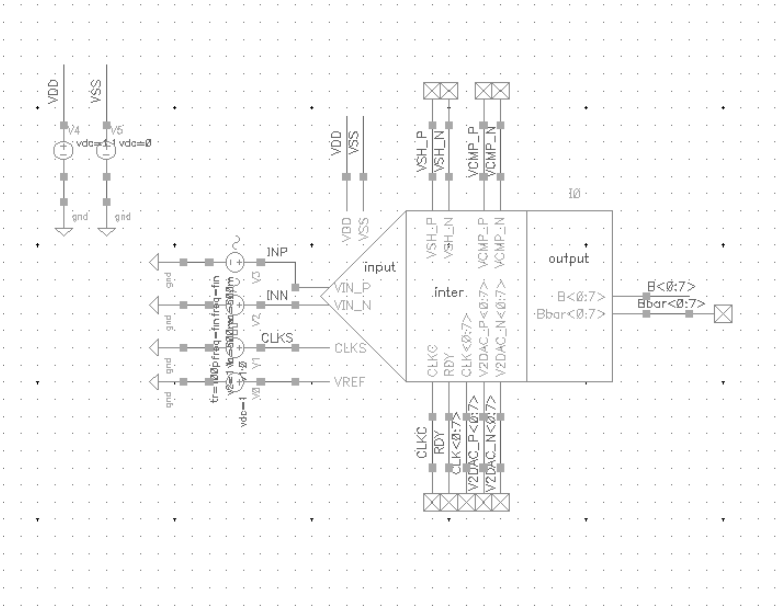


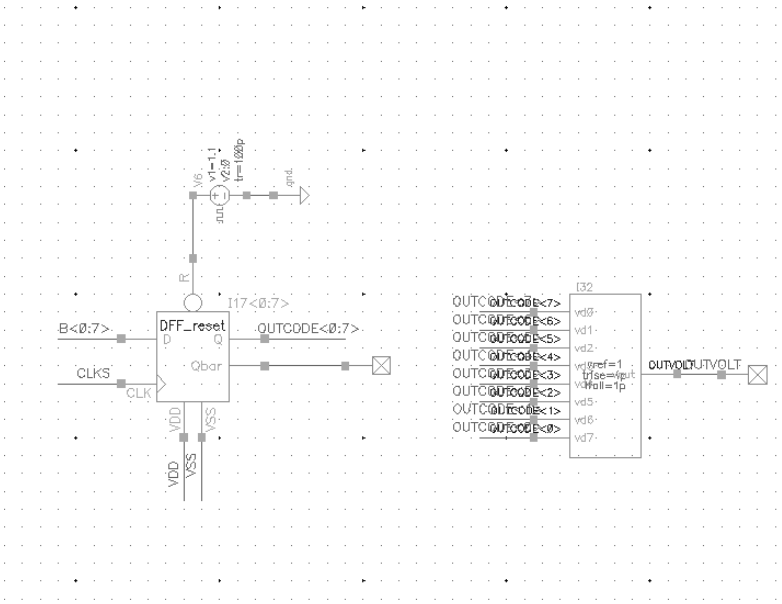
Schematic of DAC control logic



Test Bench:

1. tb_chip_core: Testbench for SAR ADC





Performance summary

Performance Metrics		
Metrics	AMPSE Design	Spice Simulation
ENOB	7.9	7.6
SFDR	70.76dB(T/H Module)	54.12dB
Power Consumption	4.43mW	6.7mW