Module: Computation DAC (used in in-memory computing)

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Module Description: Computation DAC

Top Cell Name: RR_1BIT_CELL_COMPUTE_V5_AMPSE

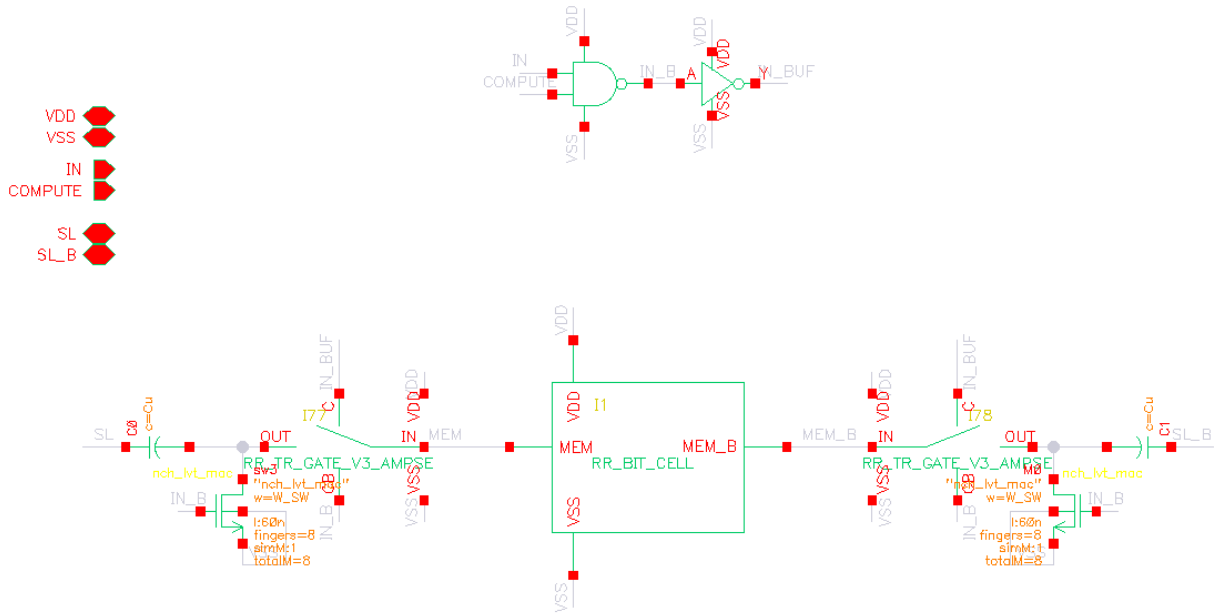
Technology: TSMC 65nm CMOS

PINS:

Pin Lists	
VDD	Supply Voltage
VSS	ground
CLK	Synchronization Clock
IN<31:0>	Input magnitude
COMPUTE	Denotes time instant when input is applied
SL, SL_B	Differential DAC output

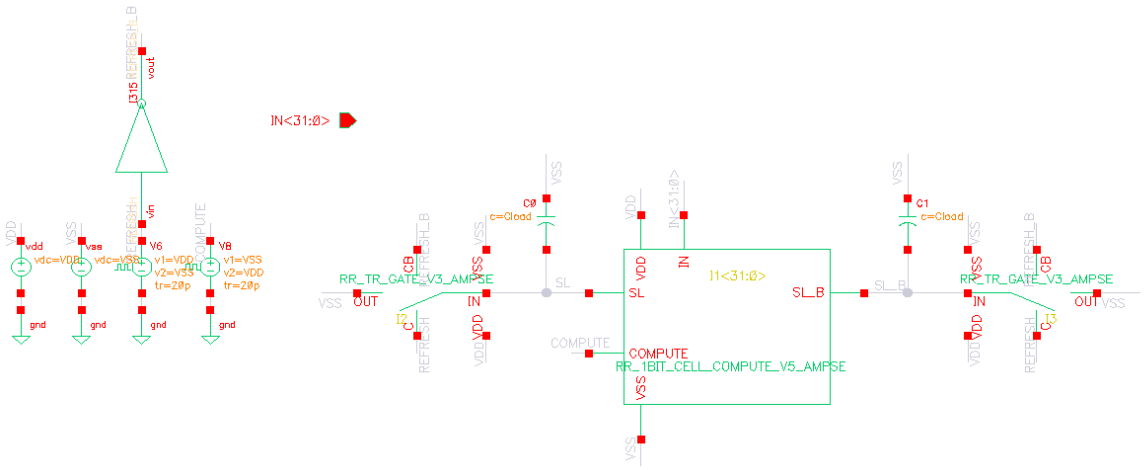
Schematic Netlists: compute_dac.scs

Schematic figures:



The bit cell consists of 1-b memory (back-to-back inverter).

Testbenches: tb_compute_dac.scs



Parameters:

Parameters	Symbols
Switch width (nm)	W_SW
Unit capacitance	Cu
Load capacitance (fF)	$Cload$
Supply voltage (V)	VDD

Metrics:

Metrics	Symbols
Power consumption	power
DAC output LSB	Delta2

Neural Network Model:

The H5 file: compute_dac.h5

The Json File: compute_dac.json

The Input Normalization File: scX_compute_dac.pkl

The Output Standardization File: scY_compute_dac.pkl

The input characterization range of the Model:

Design parameters	
Symbols	**Characterization Range**
W_SW	[200nm, 300nm]
Cu	[0.5fF, 4fF]
$Cload$	[250fF, 400fF]
VDD	[0.8V, 1.2V]

The error range of the Model: