Changes from last revision

Date	User	Edits
12/27/2019	Ce Yang	Specifications; Schematic and description of testbench; Design examples;

Subsystem or block descriptions

Design name	Delay Lock Loop (DLL) in TSMC 28nm CMOS
The Top-level cell name	Dll_schematic_28nm.scs
Designer	Ce Yang
Organization	University of Southern California

Overview

A DLL includes the voltage control delay line (VCDL), phase and frequency detector (PFD) and charge pump (CP). PFD and CP are used to provide the controlling voltage for VCDL in the circuit.

Block Specifications and Compliance

Spec Name	Min	Max	Note
Dead zone (ps)	0	1	Dead zone of the DLL after the controlling voltage becomes stable.
Fmin (GHz)	-	6.5	Maximum of the VCDL tuning range lower bound
Fmax (GHz)	7	-	Minimum of the VCDL tuning range upper bound
Power (mW)	3.5	4	Power consumption of VCDL
VDD (Volt)	0.8	1	Supply VDD

Block diagram

The block diagram representation of the design is as follows:

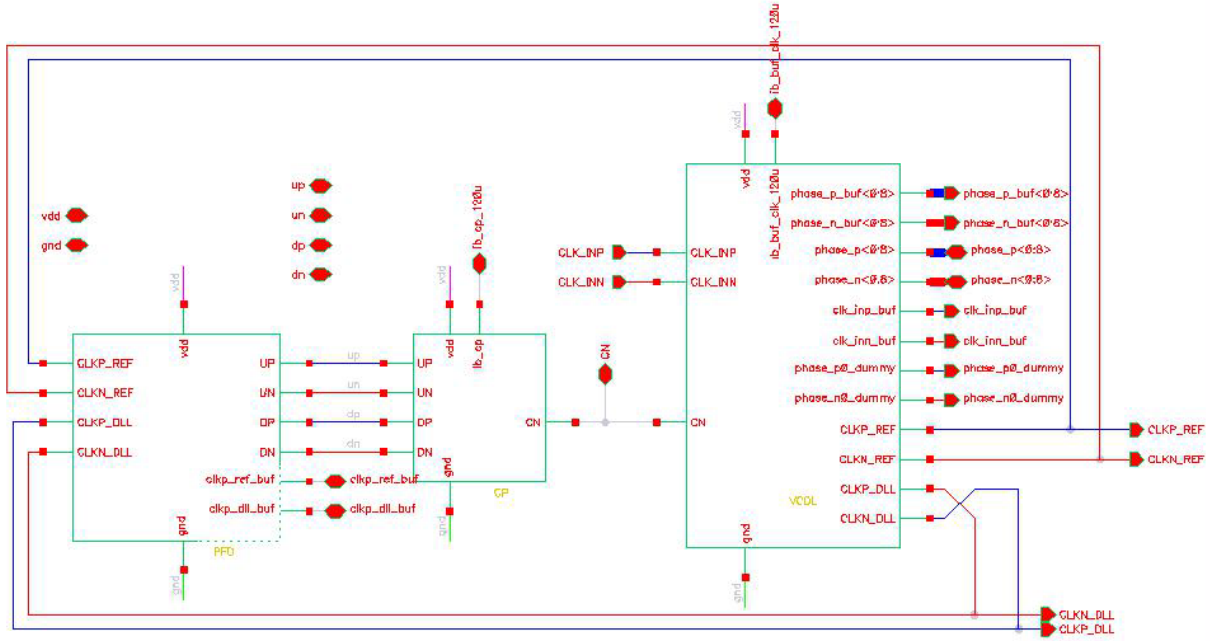

Figure 1: Architecture of DLL with AMPSE

Main analog modules	Regression models			
DLL main stage	model_dll_28.json	reg_dll_28.h5	scX_dll_28.pkl	scY_dll_28.pkl
VCDL stage	model_vcdl_28.json	reg_vcdl_28.h5	scX_vcdl_28.pkl	scY_vcdl_28.pkl

Signal list

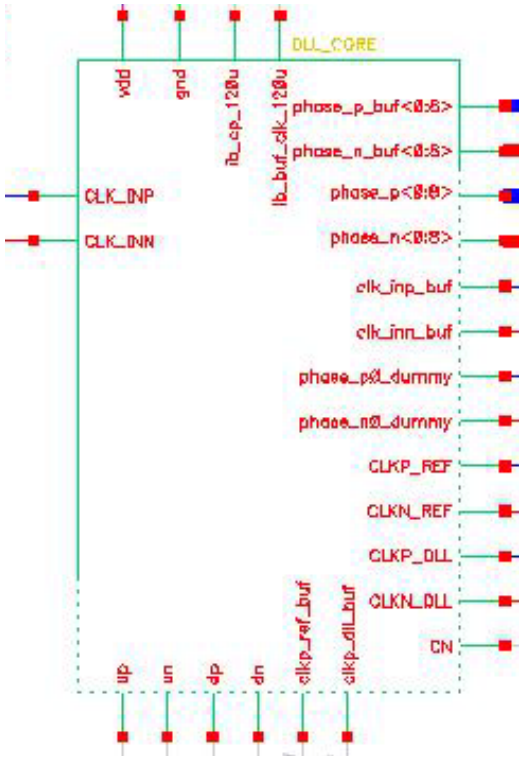

Figure 2: Symbol of the Top-Level of the DLL

Signal Pins	Direction (I/O)	Type (supply, ground, analog current, analog voltage, digital voltage)	Max Voltage (core, IO or max voltage)	Specification
vdd	I	Supply	Core	Power Supply
gnd	I	Ground	Core	Ground
CLK_INP, CLK_INN	I	Analog voltage	Core	Input clock
CLKP_REF, CLKN_REF	I/O	Analog voltage	Core	Output signal of DLL, Input signal of PFD
CLKP_DLL, CLKN_DLL	I/O	Analog voltage	Core	Output signal of DLL, Input signal of PFD
Ib_xx	I	Analog Current	Core	Bias current
phase_n,phase_p<0:8>	O	Analog voltage	Core	VCDL output
phase_n_buf,phase_p_buf<0:8>	O	Analog current	Core	DLL output

up,un,dp,dn	I/O	Analog current	Core	Input of CP
Others	I/O	Analog current	Core	Internal Nodes

Design Hierarchy

The tabular description below corresponds to design hierarchy:

Category	Cell Name	Description	Figure
DLL	VCDL	VCDL only	Figure. A1
	DLL	DLL including VCDL, PFD and CP	Figure. A2

Test Bench

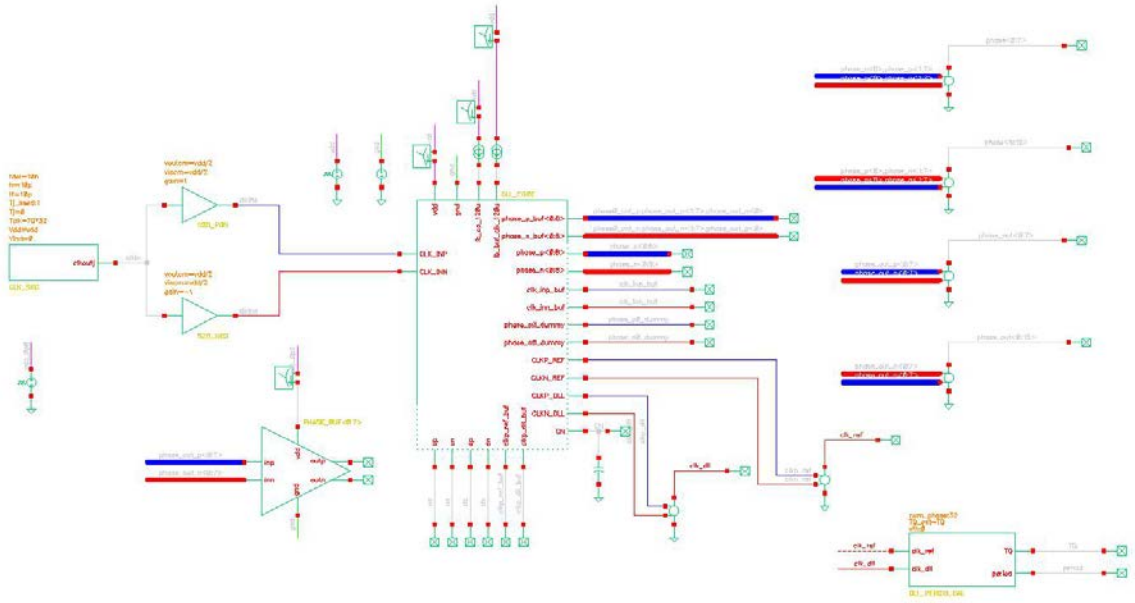

Figure 3: The Test Bench Used for the top-level DTC

Cell Name	Note	
vcdl_schematic_28nm	Transient simulation for 1. VCDL tuning range 2. VCDL power range	------

dll_schematic_ 28nm	Transient simulation for 1. DLL dead zone 2. DLL power	------

Simulations & Design Example:

Conditions/parameters	Values	Conditions/parameters	Values
Process corner	TT	Temperature(°C)	27

After running the different modules regressors and building the graph of the whole block, we get the candidate values of the parameters and the list of the expected metrics per module in order to achieve the required specs and their given constraints.

Example - VCDL					
Parameters		Metrics from AMPSE		Metrics from SPICE	
vcdl_n_width (nm)	494	fmin (GHz)	4.796	fmin (GHz)	4.27
vcdl_p_width (nm)	880	fmax (GHz)	8.358	fmax (GHz)	8.41
tc_n_width (nm)	1168	pmin (mW)	2.25	pmin (mW)	3.31
tc_p_width (nm)	1708	pmax (mW)	3.75	pmax (mW)	3.48
Vdd(V)	0.894				

Example - DLL					
Parameters		Metrics from AMPSE		Metrics from SPICE	
CP_out_width (nm)	880	Dead zone (ps)	0.488	DTC Gain (ps)	1.15
nor_n_width (nm)	256	Power (mW)	4.4	DTC Offset (ps)	4.5
nor_n_width (nm)	412				
tspc_n_width (nm)	256				
tspc_n_width (nm)	430				
Vdd(V)	0.894				

Appendix

The schematics of the two modules used within the are shown below

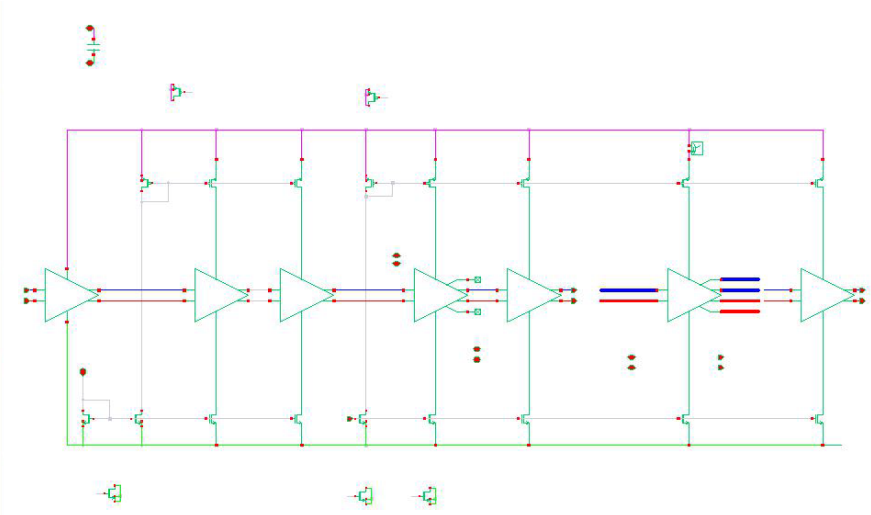

Figure A.1: The Circuit Schematic of the VCDL stage

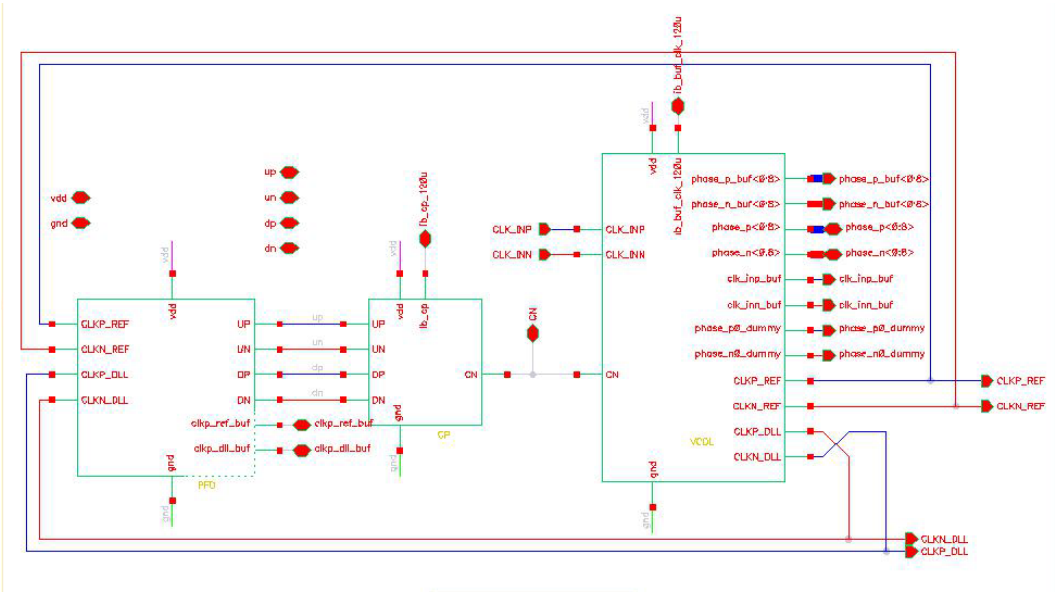

Figure A.2: The Circuit Schematic of DLL main stage

AMPSE Modules descriptions

Module Name	Class name in Netlist_Database.py	Class name in AMPSE_Graph.py

VCDL	vcdl_spice	vcdl
DLL	dll_spice	dll

All the regression files are in /regfiles

VCDL:

Parameters	min	max	step	Description
vcdl_n_width (nm)	450	550	25	Width of each finger in the inverter nmos
vcdl_p_width (nm)	720	880	40	Width of each finger in the inverter pmos
tc_n_width (nm)	1170	1430	65	Width of each finger in the tail current nmos
tc_p_width (nm)	1710	2090	95	Width of each finger in the tail current pmos
Vdd(V)	0.8	1	0.1	Supply voltage

Metrics	Description
fmin	Lower bound of tuning range
fmax	Upper bound of tuning range
pmin	Power of fmin
pmax	Power of fmax

DLL:

Parameters	min	max	step	Description

CP_out_width (nm)	720	880	80	Width of output stage of CP
nor_n_width (nm)	225	275	25	Width of each finger in the nor gate nmos
nor_n_width (nm)	360	440	40	Width of each finger in the nor gate pmos
tspc_n_width (nm)	225	275	25	Width of each finger in the tspc nmos
tspc_n_width (nm)	360	440	40	Width of each finger in the tspc pmos
Vdd(V)	0.8	1	0.1	Supply voltage

Metrics	Description
Dead zone	Dead zone of DLL
Power	Power of whole DLL

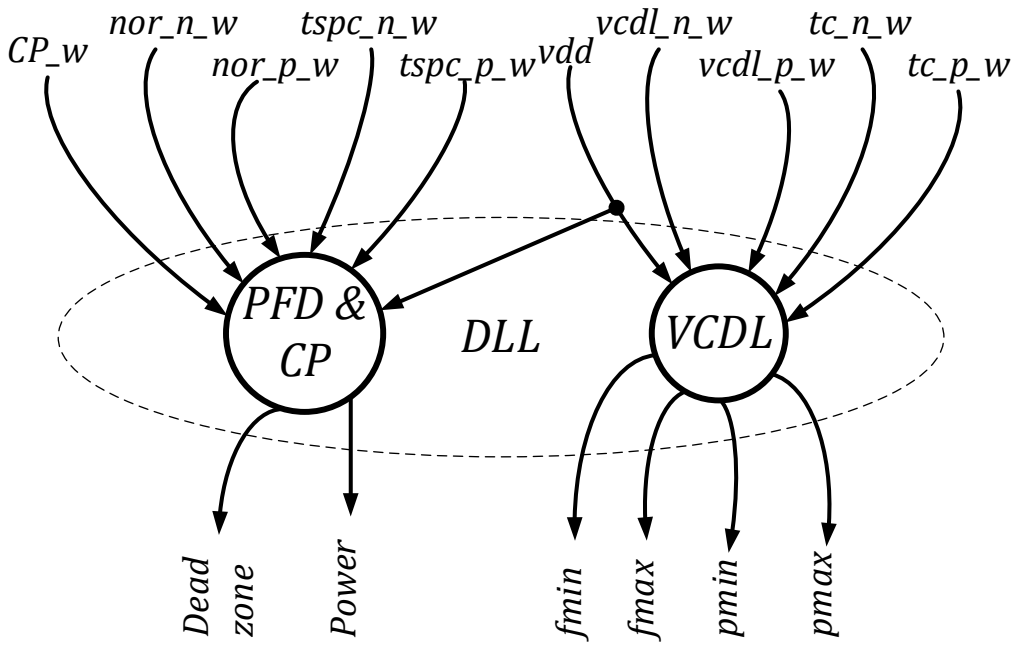

Figure A.3: The Graph Used to Model the Two Modules Together