Module: Comparator (used in SAR ADC)

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Module Description: current integration type dynamic amplifier with SR latch comparator with PMOS input differential pair and reset.

Top Cell Name: TB_comp

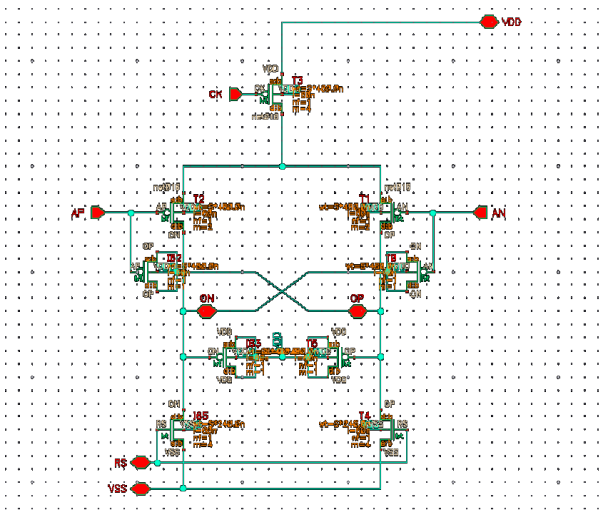
Technology: GF 65nm CMOS

PINS:

Pin Lists	
VDD	Supply Voltage
VSS	ground
LAT	Reset signal
RDY	Ready signal
INP, INN	Input voltage node
DP, DN	Digital Output voltage node

Schematic Netlists: comparator.scs

Schematic figures:



Parameters:

Parameters	Symbols
Transistor size scaling factor	S
Pre-amplifier's load cap scaling factor	CL
Supply voltage	VDD

Metrics:

Metrics	Symbols
Regenration time (s)	Regen_time
Power consumption (W)	avg_power

Neural Network Model:

The H5 file: comp.h5

The Json File: model_comp.json

The Input Normalization File: scX_comp.pkl

The Output Standardization File: scY_comp.pkl

The input characterization range of the Model:

Design parameters	
Symbols	Characterization Range
$\boldsymbol{S}$	$[4, 16] \times (240\text{nm NMOS}, 480\text{nm PMOS})$
$\boldsymbol{CL}$	$[32, 48] \times \frac{480nm}{60\text{nm}} \cdot \text{PMOS\_CAP}$
$\boldsymbol{VDD}$	$[1.0\text{V}, 1.2\text{V}]$

The error range of the Model: