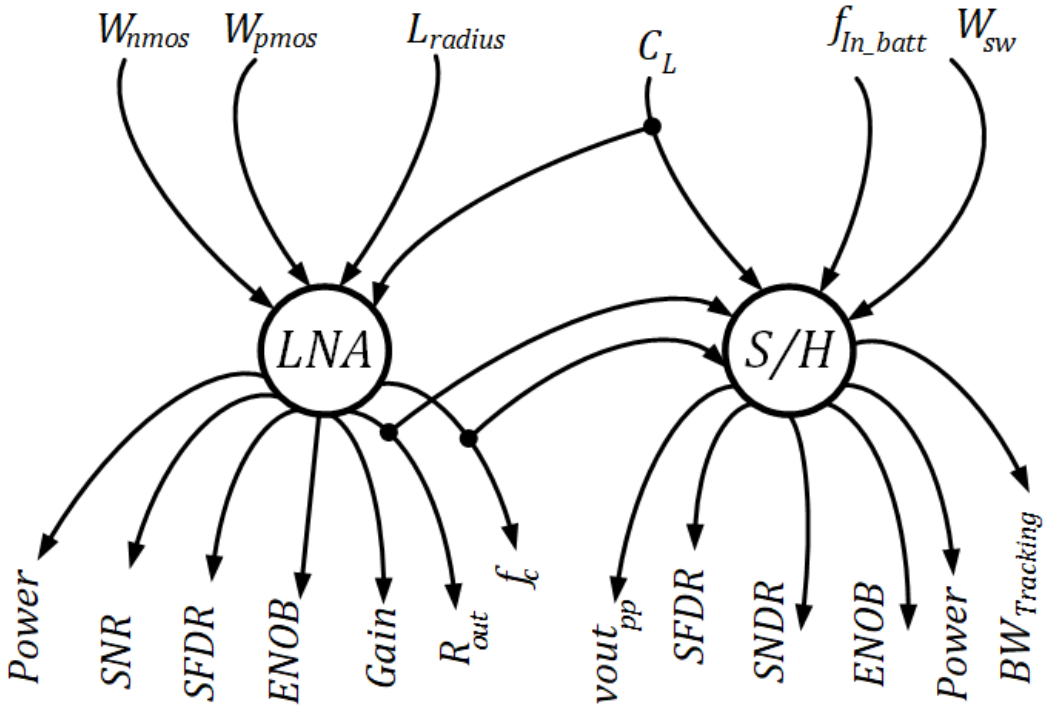
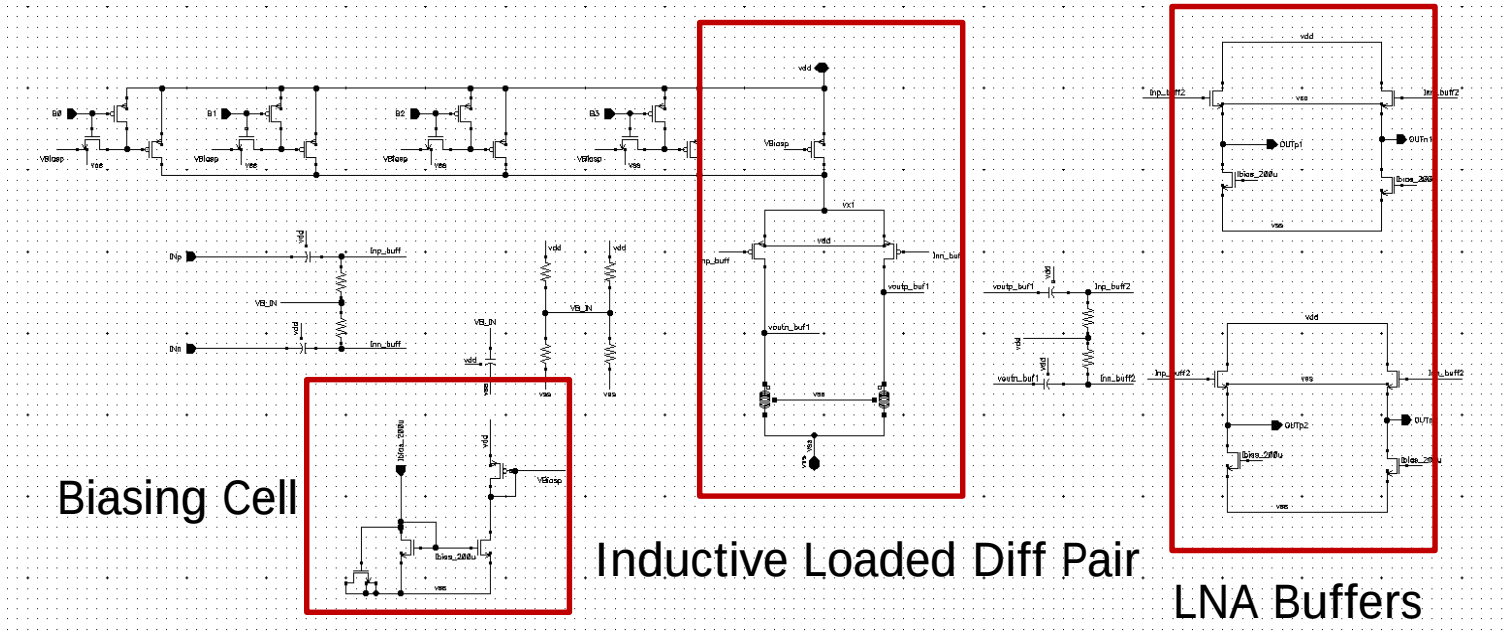
The Module Graph and The Design Parameters

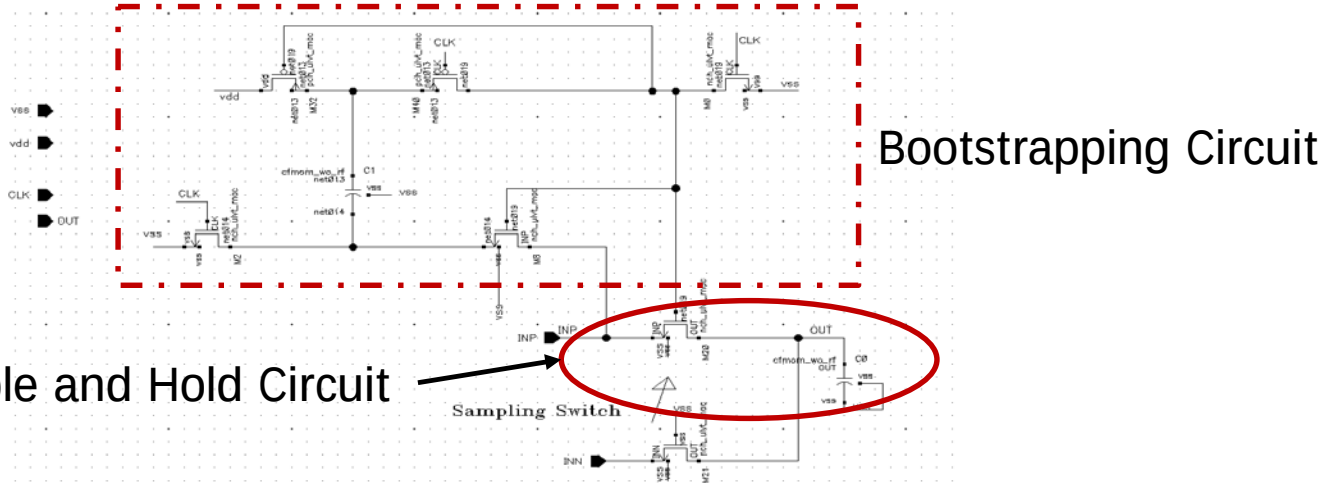
Connection of the Logic-Diagram

LNA Parameters	Description
W_{pmos}	Number of fingers for the pMOS input transistors for the LNA
$L_{radius}(m)$	The inductor radius
C_L	The LNA buffers load capacitance
W_{nmos}	Number of fingers for the nMOS transistors of the LNA buffers
SH Parameters	**Description**
W_{sw}	Number of fingers of the sampling switch
C_L	The hold capacitance value
f_c	Center Frequency
f_{In_batt}	Number of fingers of the battery capacitor inside the bootstrapping circuit
R_{Out}	Output impedance of the LNA buffers

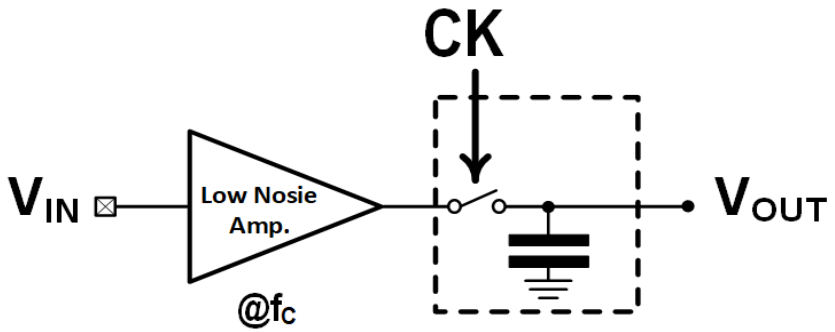


Circuit Schematics





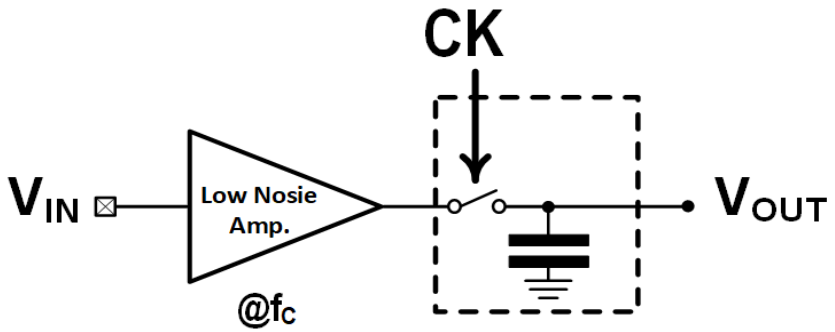
Comparison between Specs from AMPSE vs. Cadence Virtuoso



Case 1: Center Frequency for 30.86GHz

Overall Achieved Metrics	Generated using AMPSE	Rechecked using Cadence Virtuoso®
Overall Power Consumption (W)	14.02m	13.85m
Output PP Amplitude (V)	955m	370m
Tracking Bandwidth (GHz)	19	23.5
ENOB (bit)	7.21	7.53
SNR (dB)	44.1	47.11
SFDR (dB)	44.77	48
Center Frequency (GHz)	30.86G	30.55G

Comparison between Specs from AMPSE vs. Cadence Virtuoso



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Center Frequency (GHz)	30.86G	30.55G

Comparison between Specs from AMPSE vs. Cadence Virtuoso

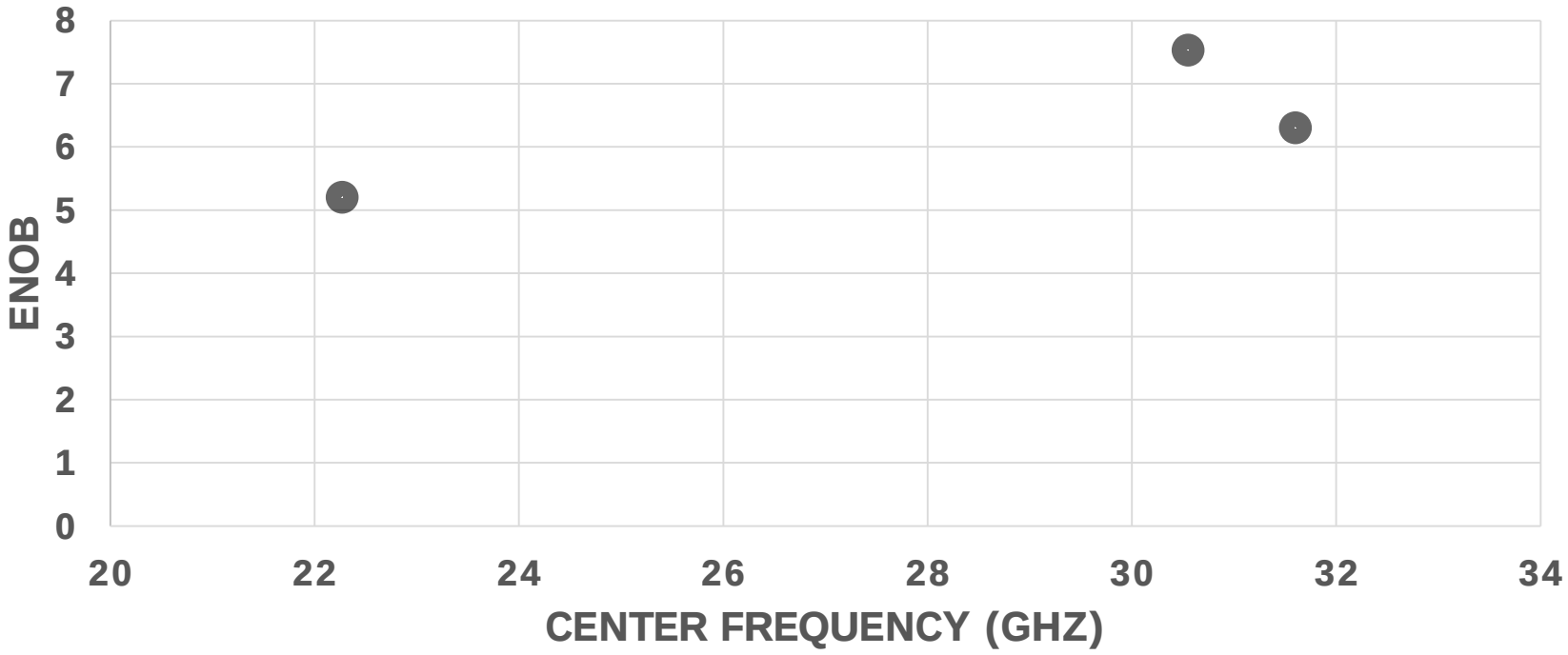
Case 2: Center Frequency for 22.4GHz

Overall Achieved Metrics	Generated using AMPSE	Rechecked using Cadence Virtuoso®
Overall Power Consumption (W)	14.17m	14.15m
Output PP Amplitude (V)	0.936	0.9
Tracking Bandwidth (Hz)	18G	18G
ENOB (bit)	6.9	5.2
SNR (dB)	43.77	35.7
SFDR (dB)	43.36	36.2
Center Frequency (Hz)	22.4G	22.27

Case 3: Center Frequency for 32GHz

Overall Achieved Metrics	Generated using AMPSE	Rechecked using Cadence Virtuoso®
Overall Power Consumption (W)	14.2m	14.35
Output PP Amplitude (V)	0.838	0.91
Tracking Bandwidth (Hz)	18.2G	21.6
ENOB (bit)	6.6	6.2
SNR (dB)	41.72	41.32
SFDR (dB)	43.3	44.8
Center Frequency (Hz)	32G	31.6G

Comparison between Specs from AMPSE vs. Cadence Virtuoso



Key point: we can design a variety of RF/mm-Wave Sub-sampling Receiver Front-Ends with the help of AMPSE.

Time-to-Design Comparison

4500 points for the LNA simulation each takes 4mins of simulation time.
8500 points for the Sample and Hold simulation each takes 10mins of simulation time.

$$Total\ simulation\ time\ =\ 4500\ *\ 4\,\mathrm{min} + 8500\ *\ 10\,min = 103{,}000\,min$$

AMPSE time was around 1.5 mins

AMPSE is more time-efficient by $\frac{103{,}000}{1.5} = 68{,}666.67$ times more that the regular sweeping-optimization approach.