Changes from last revision

Date	Designer	Edits
12/14/2019	Shiyu Su	Initial version. Specifications; Schematic and description of testbench.
12/28/2019	Shiyu Su	Design examples.
1/2/2019	Shiyu Su	Add more design examples.

Block descriptions

Design name	Current-steering DAC
The Top-level cell name	CS_DAC.scs
Designer	Shiyu Su
Organization	University of Southern California

Overview

This DAC consists of CML drivers and current-steering cells, operating up to 20GHz with an 8-bit resolution. The current-steering array is implemented in a segmented fashion with 4-bit MSBs and 4-bit LSBs. The MSBs are converted from binary to unary via a thermometer encoder while the LSBs remain binary.

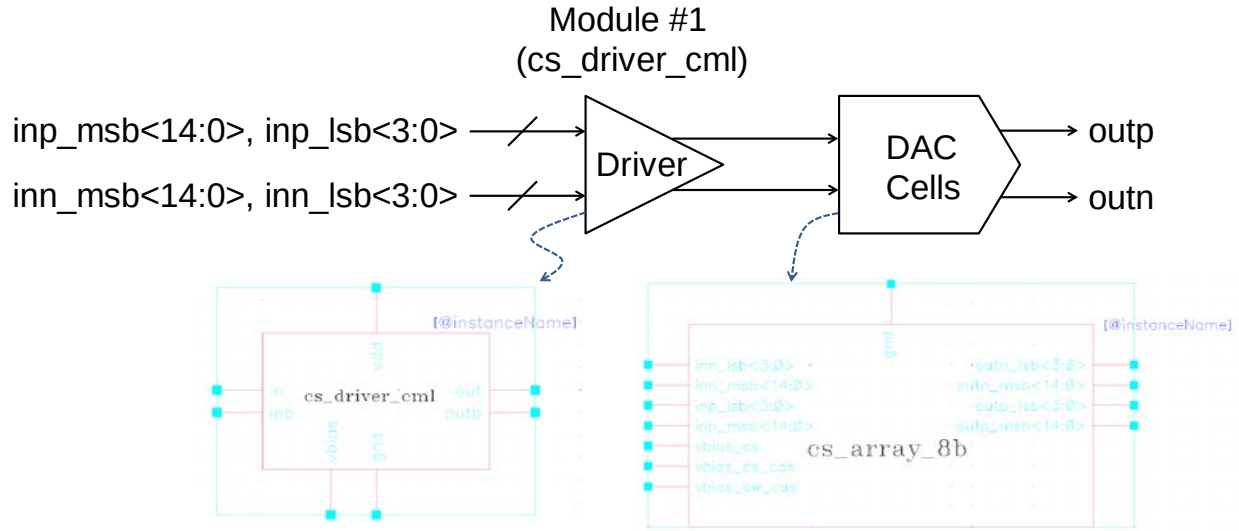
Block Specifications and Compliance

Spec Name	Min	Max	Note
Sampling rate (GS/s)	10	20	Training data is all measured with sampling rate set to 20 GS/s
SFDR (dB)	50	70	SFDR is dominated by HD3
BW (MHz)	5	10	Nyquist frequency with given sampling rate

Power Consumption (mW)	60	260	Total power consumption
VDD (Volt)	0.9	1.1	Core supply for current sources and switches
VDD IO (Volt)	2.3	2.7	IO supply for DAC output

Block diagram

Figure 1 shows the block diagram of the 8-bit segmented current-steering DAC with digital input signals and differential output current, outp and outn, which are essentially the current sums of all the current branches.



$$outp = \Sigma(outp\_msb<*>, outp\_lsb<*>)$$

$$outn = \Sigma(outn\_msb<*>, outn\_lsb<*>)$$

Figure 1. top-level block diagram of the current-steering DAC

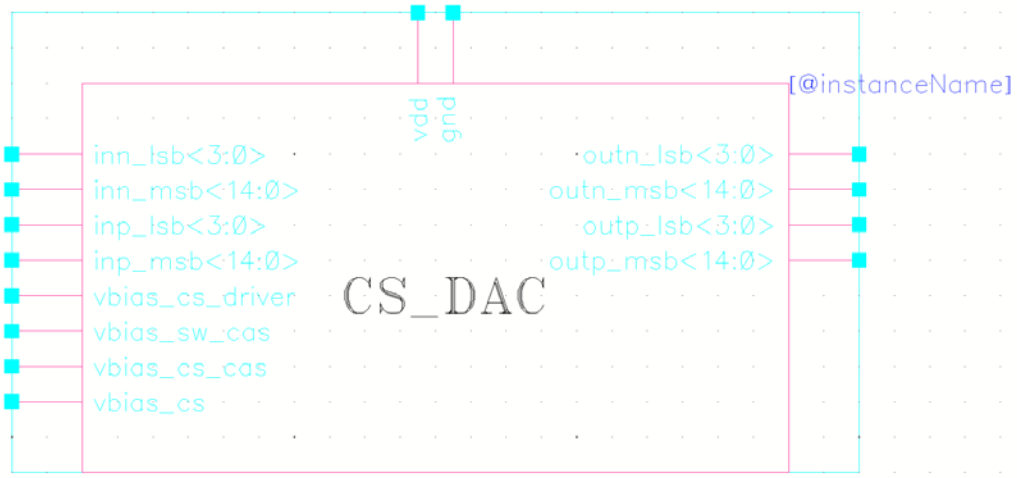


Figure 2. symbol of CS_DAC

PINS:

Signal Pins	Direction (I/O)	Type (supply, ground, analog current, analog voltage, digital voltage)	Max Voltage (core, IO or max voltage)	Specification
inp_lsb<3:0>	I	Analog voltage	core	Input digital signals of LSB branches (positive side of differential pair)
inn_lsb<3:0>	I	Analog voltage	Core	Input digital signals of LSB branches (negative side of differential pair)
inp_msb<14:0>	I	Analog voltage	Core	Input digital signals of MSB branches (positive side of differential pair)
inn_msb<14:0>	I	Analog voltage	Core	Input digital signals of MSB branches (negative side of differential pair)
outp_lsb<3:0>	O	Analog current	IO	Output current of LSB branches (positive side of differential pair)
outn_lsb<3:0>	O	Analog current	IO	Output current of LSB branches (negative side of differential pair)

outp_msb<14:0>	O	Analog current	IO	Output current of MSB branches (positive side of differential pair)
outn_msb<14:0>	O	Analog current	IO	Output current of MSB branches (negative side of differential pair)
vbias_cs	I	Analog voltage	Core	Bias voltage of the tail current source
vbias_cs_cas	I	Analog voltage	Core	Bias voltage of the cascode device of the tail current source
vbias_sw_cs	I	Analog voltage	IO	Bias voltage of the cascode device of the switching pair
vbias_cs_driver	I	Analog voltage	Core	Bias voltage of the tail current source of the DAC driver
vdd	I/O	Supply	Core	Supply
gnd	I/O	Ground	Core	Ground

Design Hierarchy

The tabular description below corresponds to design hierarchy.

Category	Cell Name			Description	Figure
Current-Steering DAC	CS_DAC	cs_array_8b	cs_16	16x unary current cell	Figure A1 & Figure A2
			cs_8	8x binary current cell	
			cs_4	4x binary current cell	
			cs_2	2x binary current cell	
			cs_1	1x binary current cell	
		cs_driver_cml		Driver for current cells	Figure A3
Ideal ADC	adc_8bit_ideal			Generator digital test signals	/
Testbench	tb_CS_DAC			Testbench for CS_DAC	Figure A4

Test Bench

Cell Name	Note
tb_cs_driver_cml.scs tb_cs_driver_cml.ocn	Testbench for cs_driver_cml. Transient simulation to measure 1. Power consumption; 2. Output swing; 3. Rise/Fall time.
tb_cs_array_8b.scs tb_cs_array_8b.ocn	Testbench for cs_array_8b. Transient simulation to measure 1. SFDR; 2. Power consumption; 3. Full-scale output current;
tb_CS_DAC.scs tb_CS_DAC.ocn	Testbench for CS_DAC. Transient simulation to measure 1. SFDR; 2. Power consumption; 3. Full-scale output current; 4. Rise/Fall time.

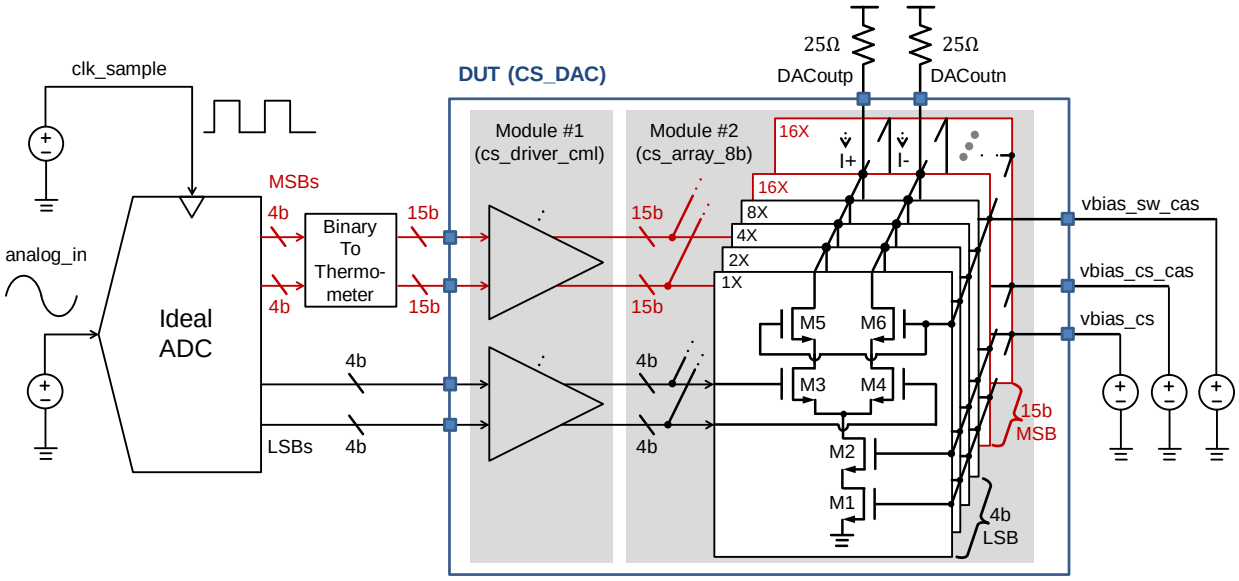


Figure 3. schematic of the CS_DAC testbench

AMPSE Modules descriptions

Module Name	Class name in Netlist_Database.py	Class name in AMPSE_Graph.py
cs_driver_cml	N/A	cs_driver_cml
cs_array_8b	N/A	cs_array_8b

All the regression files are in /regfiles

Module #1: cs_driver_cml

This is a high-speed CML driver for current cells.

Parameters:

Parameters	Characterization Range	Description
R_driver	$[40\Omega, 70\Omega]$	Load resistors
l_cs_driver	$[300nm, 500nm]$	Transistor length of tail current source
v_swing	$[300mV, 600mV]$	Swing of input digital signals
vbias_cs_driver	$[400mV, 700mV]$	Bias voltage of tail current source
w_cs_driver	$[6um, 10\mu m]$	Transistor width of tail current source
w_sw	$[400nm, 700nm]$	Transistor width of the switching pair

Metrics:

Metrics	Description
Power	Power consumption
Output swing	Output swing of the driver in voltage
Rise time	Rise time of the driver
Fall time	Fall time of the driver

Neural Network Model:

The H5 file: reg_cs_driver_cml.h5

The Json File: model_cs_driver_cml.json

The Input Normalization File: scX_cs_driver_cml.pkl

The Output Standardization File: scY_cs_driver_cml.pkl

Module #2: cs_array_8b

This is an 8-bit segmented current-steering cell array with open-drain current output.

Parameters:

Parameters	Characterization Range	Description
l_cs	$[400nm, 800nm]$	Transistor length of tail current source
v_swing	$[100mV, 500mV]$	Swing of input digital signals
vbias_sw_cas	$[1.2V, 2V]$	Bias voltage of the cascode transistors
w_cs	$[250nm, 2\mu m]$	Transistor width of tail current source
w_sw	$[400nm, 700nm]$	Transistor width of the switching pair

Metrics:

Metrics	Description
SFDR	SFDR of the DAC (dominated by HD3)
Power	Power consumption
I_fullscale	Full-scale output current of the DAC

Neural Network Model:

The H5 file: reg_cs_array_8b.h5

The Json File: model_cs_array_8b.json

The Input Normalization File: scX_cs_array_8b.pkl

The Output Standardization File: scY_cs_array_8b.pkl

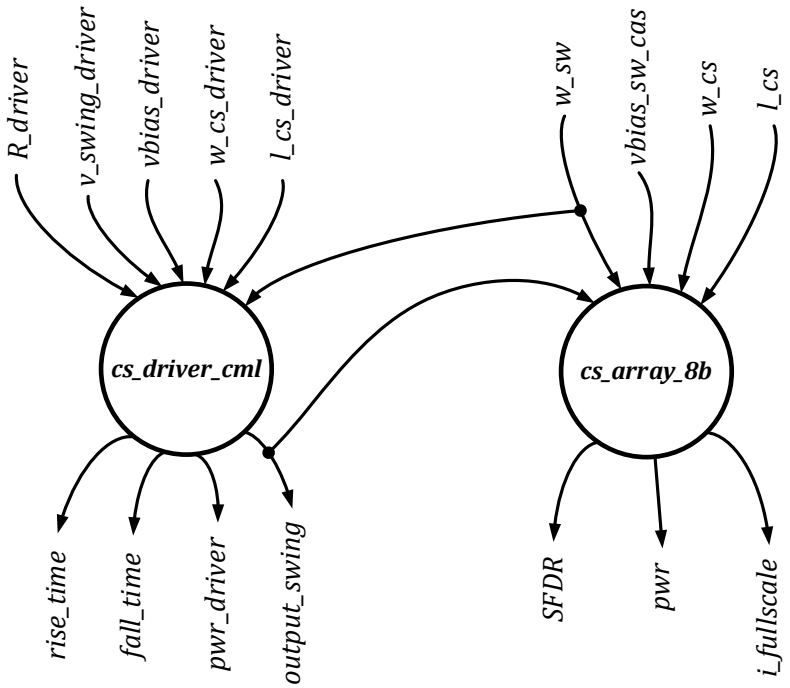


Figure 4. graph for the two modules

AMPSE Design Example 1					
AMPSE					Virtuoso
Parameters	Value	Metrics	Target	Generated	Simulated
R_driver	48.39	SFDR (dB)	70	79.52	70
I_cs_driver	458.8n	Power (mw)	200	149.6	155.73
v_swing	299.6m	I_fullscale (mA)	16	31.51	25.57
vbias_cs_driver	480.2m	Rise time (ps)	12	7.328	8.249
w_cs_driver	7.736u	Fall time (ps)	12	4.249	5.145
w_sw	397.3n				
l_cs	802n				
vbias_sw_cas	1.526				
w_cs	1.478u				

AMPSE Design Example 2					
AMPSE					Virtuoso
Parameters	Value	Metrics	Target	Generated	Simulated
R_driver	57.05	SFDR (dB)	60	74.73	70.89
I_cs_driver	434.9n	Power (mw)	150	132.4	134.12
v_swing	347.4m	I_fullscale (mA)	28	35.86	25.78
vbias_cs_driver	489.2m	Rise time (ps)	12	8.351	8.253
w_cs_driver	5.991u	Fall time (ps)	12	3.954	4.648
w_sw	678.8n				
l_cs	661.5n				
vbias_sw_cas	1.469				
w_cs	1.188u				

AMPSE Design Example 3					
AMPSE					Virtuoso
Parameters	Value	Metrics	Target	Generated	Simulated
R_driver	70.1	SFDR (dB)	50	59.48	60.64
l_cs_driver	501.1n	Power (mw)	100	86.92	88.46
v_swing	298.6m	I_fullscale (mA)	40	41.76	22.19
vbias_cs_driver	405.5m	Rise time (ps)	12	10.54	10.88
w_cs_driver	6.62u	Fall time (ps)	12	4.137	4.846
w_sw	701n				
l_cs	718.2n				
vbias_sw_cas	1.946				
w_cs	990.6n				

Appendix

Schematic for modules are listed below.

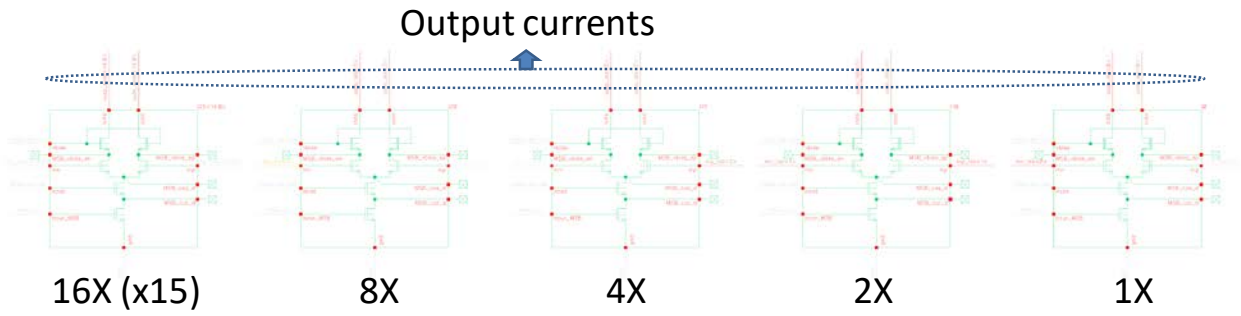


Figure A1. schematic of an 8-bit segmented current-steering cell array

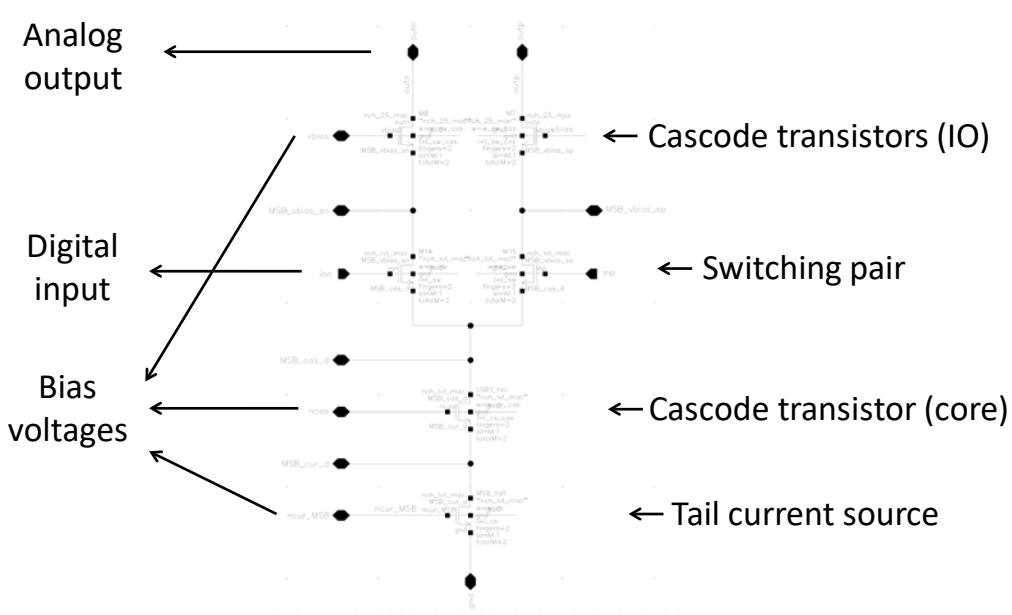


Figure A2. schematic of a current-steering cell

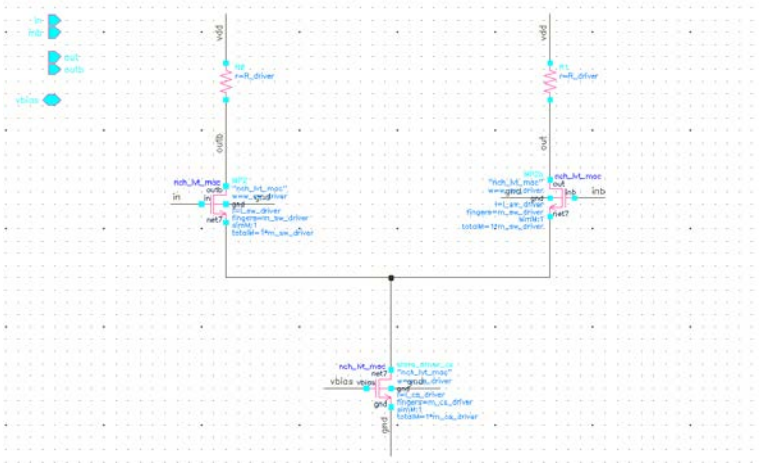


Figure A3. schematic of the driver for current-steering cells

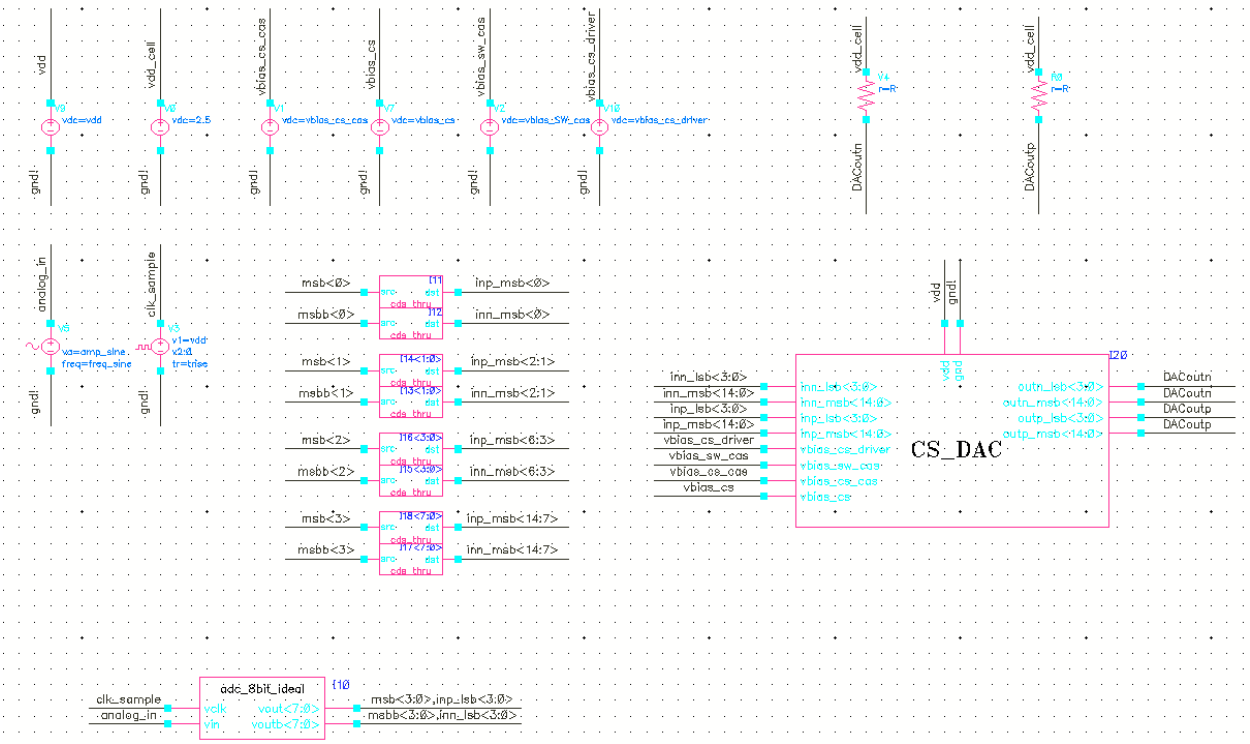


Figure A4. schematic of the testbench for CS_DAC