

**Module:** Clock Input Buffer (used in Non-Uniform Subsample Receiver)

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**Module Description:** Current Mode Logic Input Buffer & Differential to Single-Ended Buffer.

**Top Cell Name:** CML\_INPUT\_BUFFER\_v1

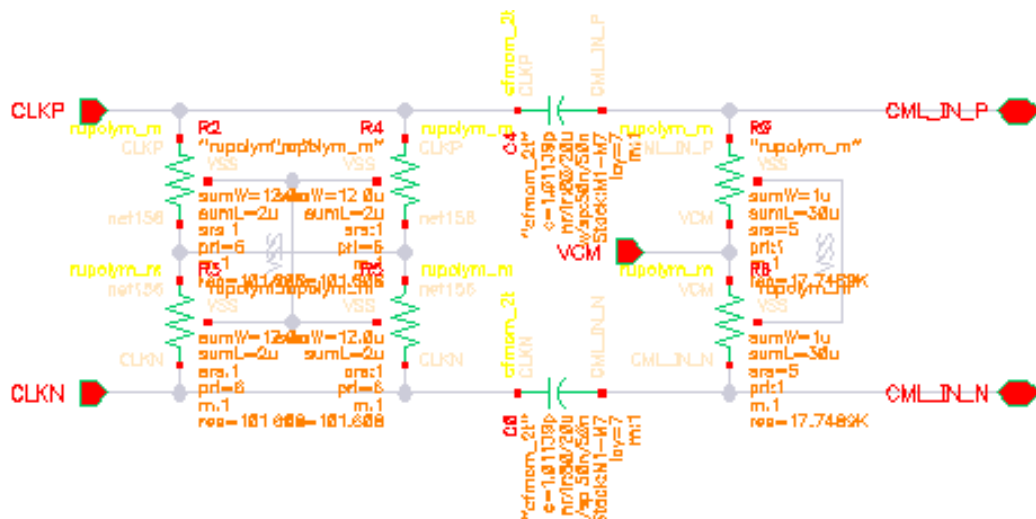
**Technology:** TSMC 28nm CMOS

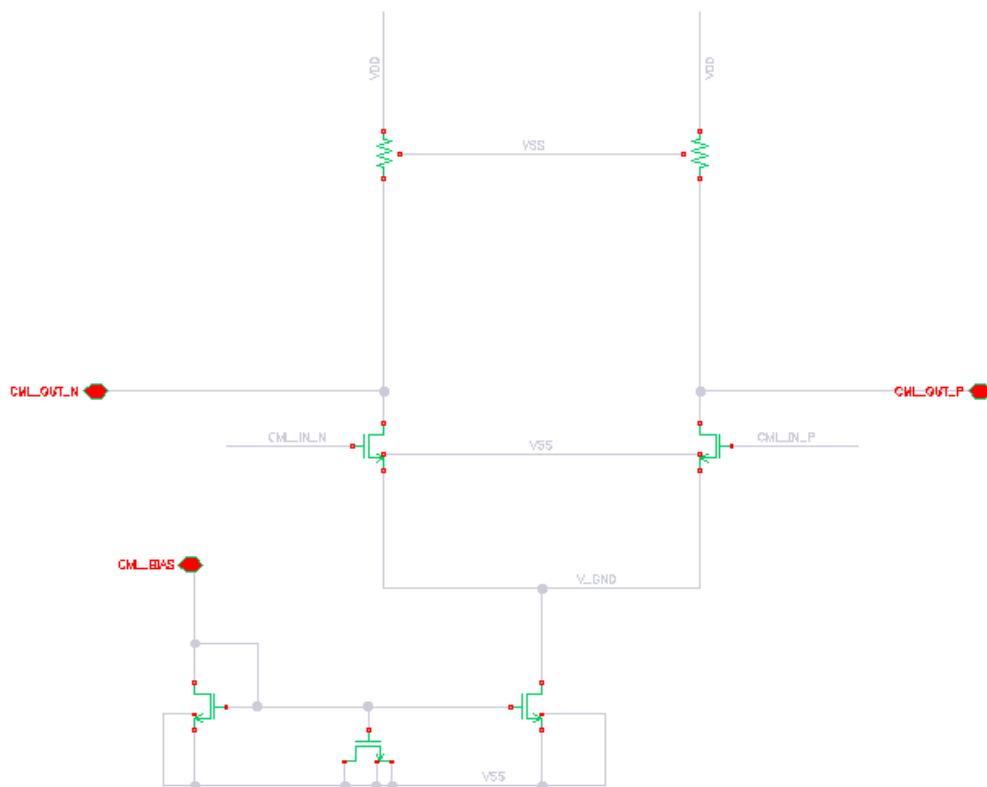
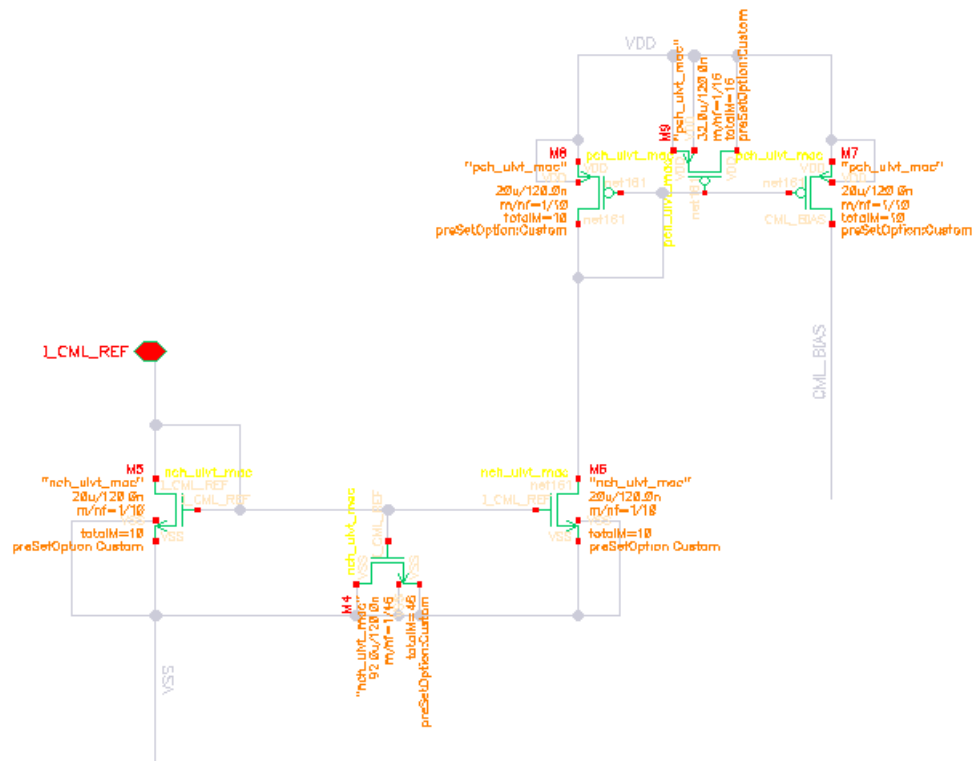
**PINS:**

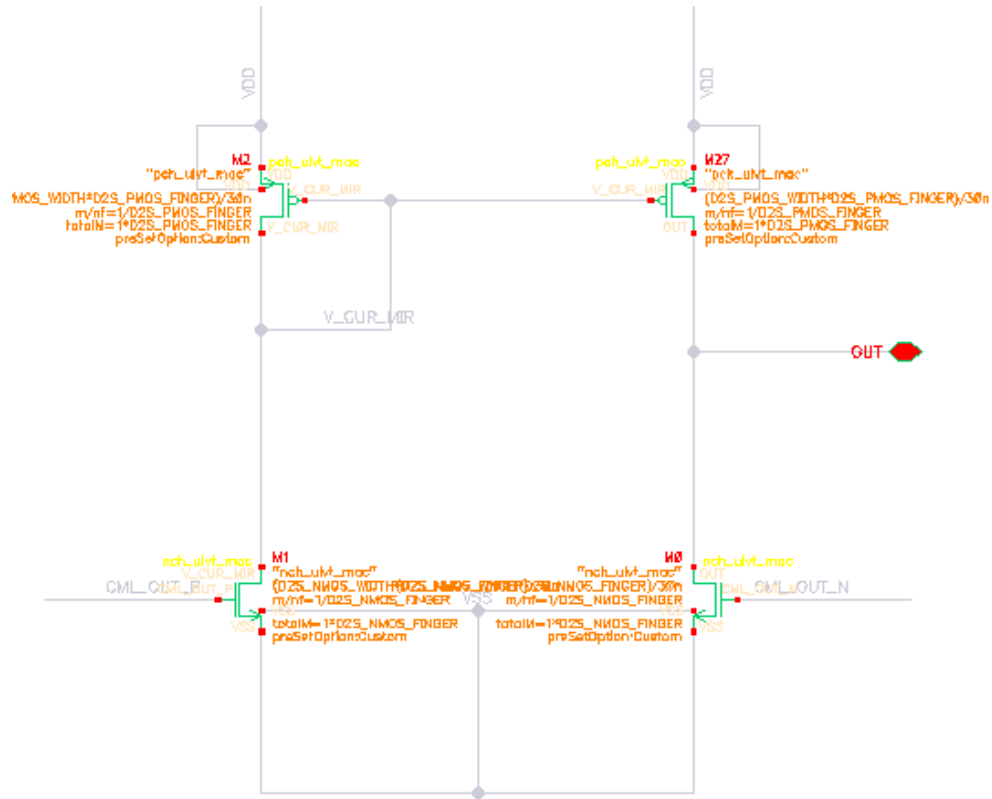
Pin Lists	
VDD	Supply Voltage
VSS	ground
CLKP, CLKN	Input clock
CML_IN_P, CML_IN_N	CML input voltage node
VCM	CML input common voltage bias
I_CML_REF	Current bias
CML_OUT_P, CML_OUT_N	CML output voltage node
OUT	D2S output voltage node

**Schematic Netlists:** CLK\_BUFFER.scs

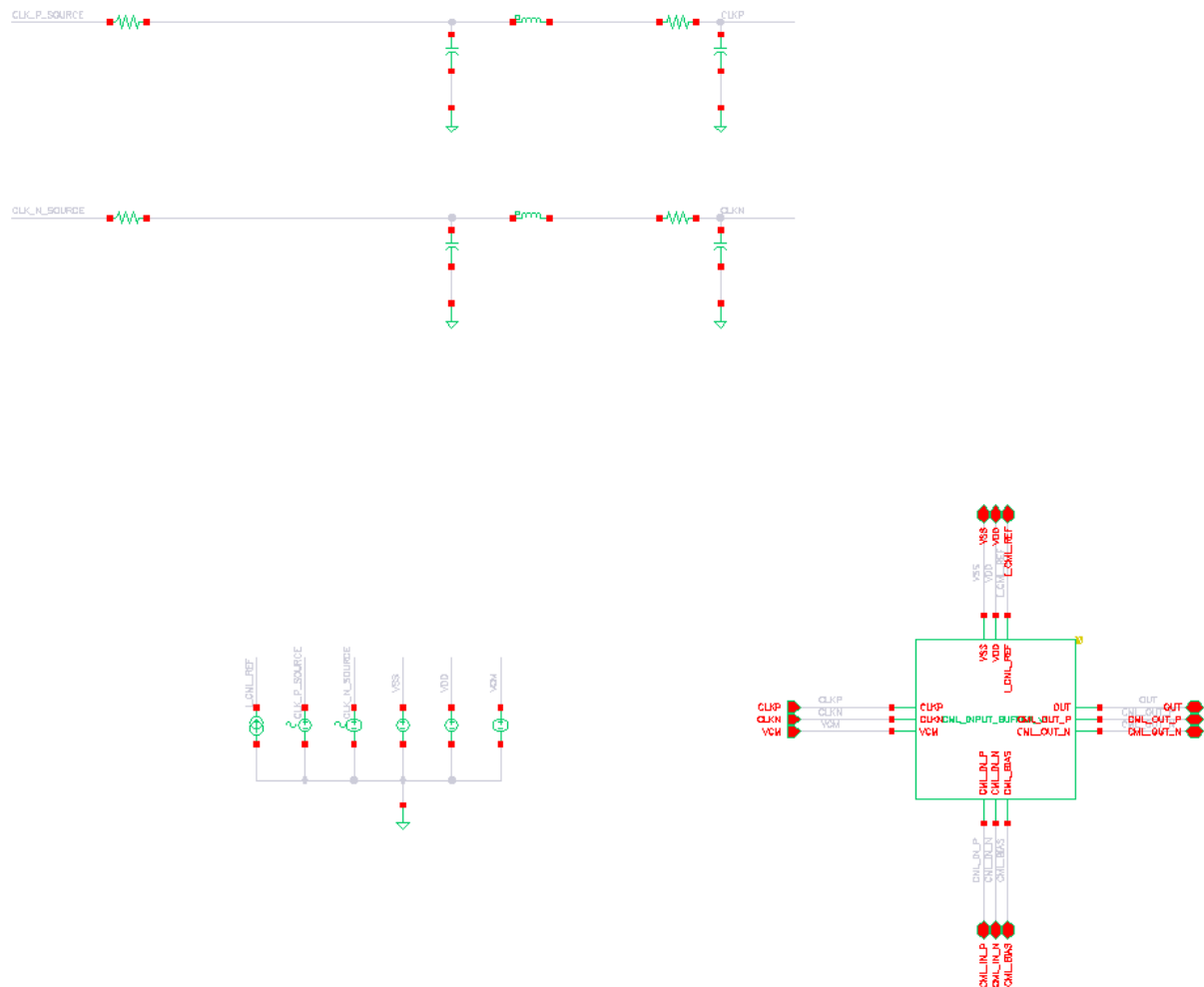
**Schematic figures:**







Testbenches: CLK\_BUFFER\_tb.scs



#### Parameters:

Parameters	Symbols
CML buffer NMOS width (m)	<i>CML_BUFFER_WIDTH</i>
CML buffer NMOS finger number	<i>CML_BUFFER_FINGER</i>
D2S buffer PMOS width (m)	<i>D2S_PMOS_WIDTH</i>
D2S buffer PMOS finger number	<i>D2S_PMOS_FINGER</i>
D2S buffer NMOS width (m)	<i>D2S_NMOS_WIDTH</i>
D2S buffer NMOS finger number	<i>D2S_NMOS_FINGER</i>

#### Metrics:

Metrics	Symbols
Power Consumption	<i>I_avg</i>
Rise/Fall time	<i>rise_time, fall_time</i>
Rise/Fall output clock jitter	<i>rise_jitter, fall_jitter</i>

### Neural Network Model:

The H5 file: cml\_test.h5

The Json File: trained\_model.json

The Input Normalization File: trained\_scX.pkl

The Output Standardization File: trained\_scY.pkl

The input characterization range of the Model:

Design parameters	
Symbols	Characterization Range
<i>CML_BUFFER_WIDTH</i>	[400nm, 1600nm]
<i>CML_BUFFER_FINGER</i>	[8, 40]
<i>D2S_P MOS_WIDTH</i>	[200nm, 800nm]
<i>D2S_P MOS_FINGER</i>	[2, 6]
<i>D2S_N MOS_WIDTH</i>	[200nm, 800nm]
<i>D2S_N MOS_FINGER</i>	[2, 6]

The error range of the Model:

