

**Module:** Common Source Amplifier (used as ADC driver)

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**Module Description:** Common source amplifier with current mirror load can be used as ADC input driver.

**Top Cell Name:** common\_source\_amp

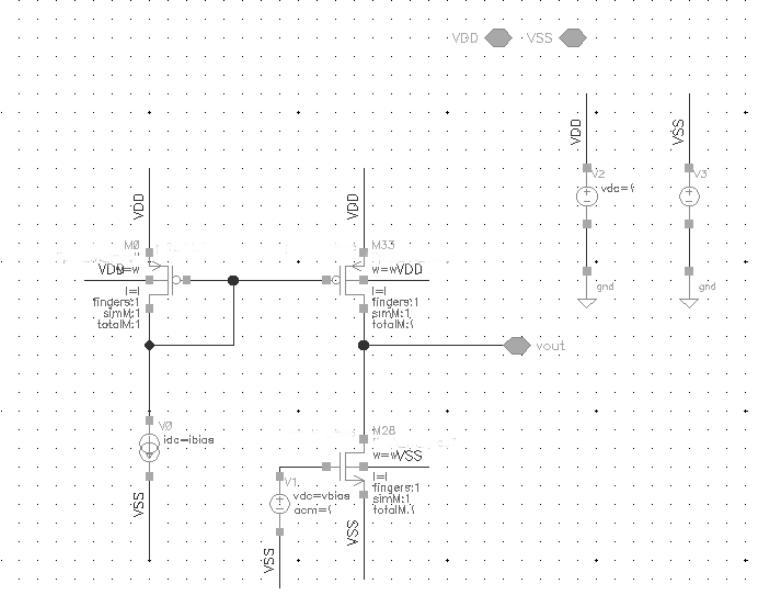
**Technology:** TSMC 65nm CMOS

**PINS:**

Pin Lists	
VDD	Supply Voltage
VSS	ground
vin	Input voltage node
vout	Output voltage node

**Schematic Netlists:** common\_source\_amp.scs

**Schematic figures:**



**Testbenches:** common\_source\_amp.scs

**Parameters:**

Parameters	Symbols
NMOS and PMOS transistors width (m)	$w$
Bias current (A)	$ibias$

#### Metrics:

Metrics	Symbols
DC Gain	gain
-3dB Bandwidth (Hz)	BW
Power consumption (W)	power

#### Neural Network Model:

**The H5 file:** cs\_reg\_complp\_gain.h5, cs\_reg\_complp\_bandwidth.h5, cs\_reg\_complp\_power.h5

**The Json File:** cs\_model\_gain.json, cs\_model\_bandwidth.json, cs\_model\_power.json

**The Input Normalization File:** cs\_scX\_complp\_gain.pkl, cs\_scX\_complp\_bandwidth.pkl, cs\_scX\_complp\_power.pkl

**The Output Standardization File:** cs\_scY\_complp\_gain.pkl, cs\_scY\_complp\_bandwidth.pkl, cs\_scY\_complp\_power.pkl

#### The input characterization range of the Model:

Design parameters	
Symbols	Characterization Range
$w$	[1μm, 2μm]
$ibias$	[100μA, 200μA]

#### The error range of the Model:

