Module: Bootstrap Sampler (used in SAR ADC)

Designer: Qiaochu Zhang, Ming Hsieh Dept. of ECE, USC (qiaochuz@usc.edu)

Module Description: Bootstrap sampler.

Top Cell Name: bootstrap_dif

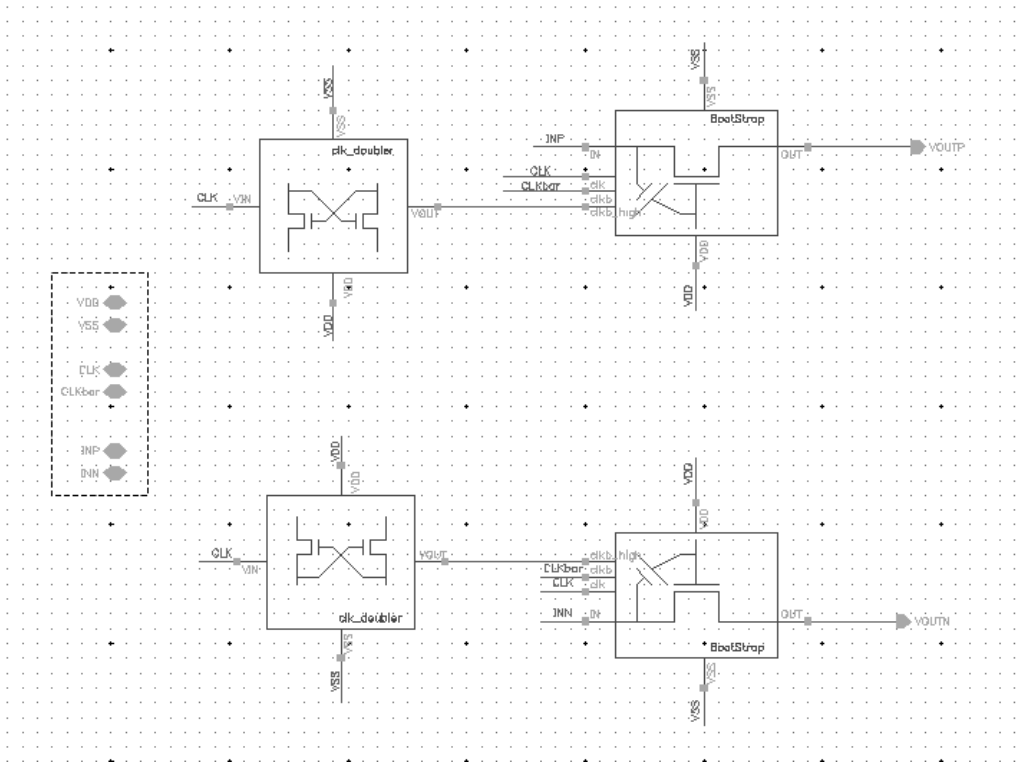
Technology: PTM 45nm CMOS

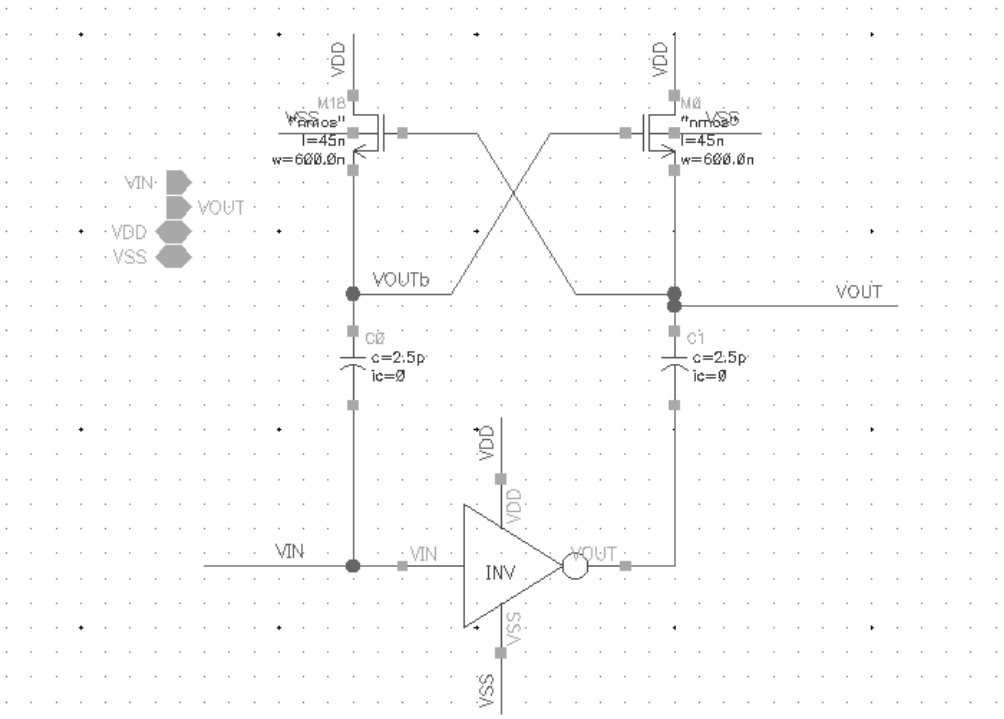
PINS:

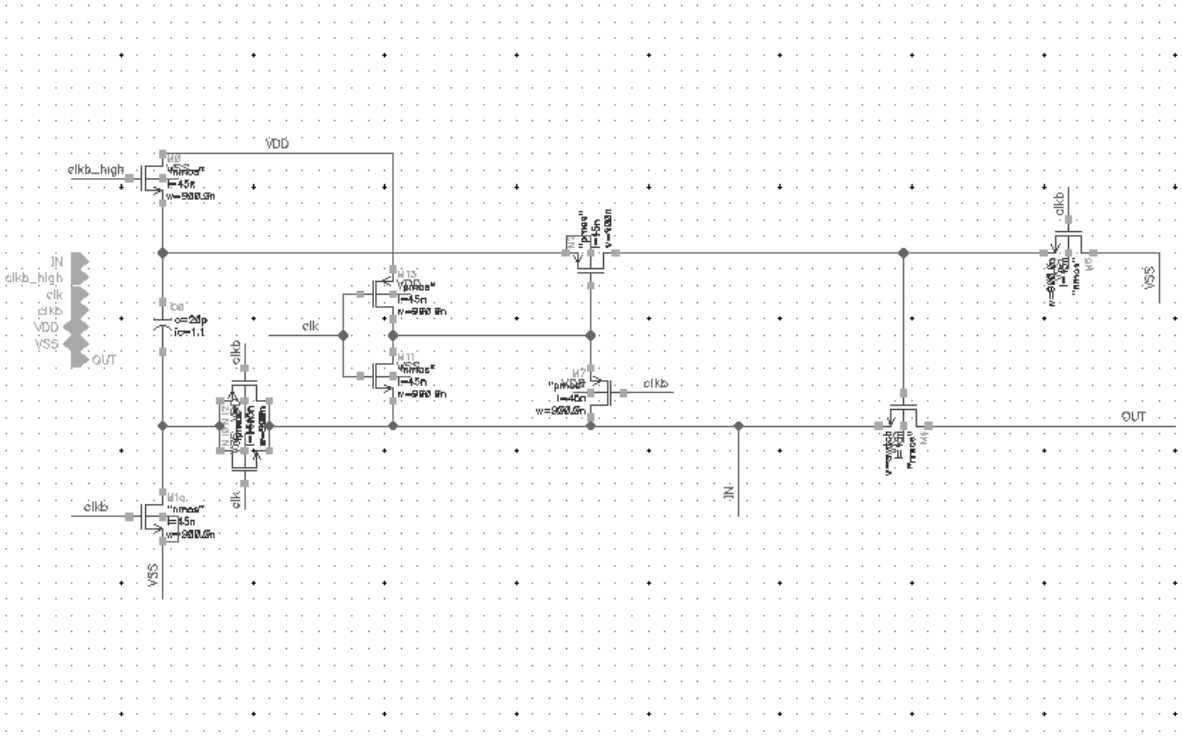
Pin Lists	
VDD	Supply Voltage
VSS	ground
CLK, CLKbar	Sampling clock
INP, INN	Input voltage node
VOUTP, VOUTN	Output voltage node

Schematic Netlists: SHBS.scs

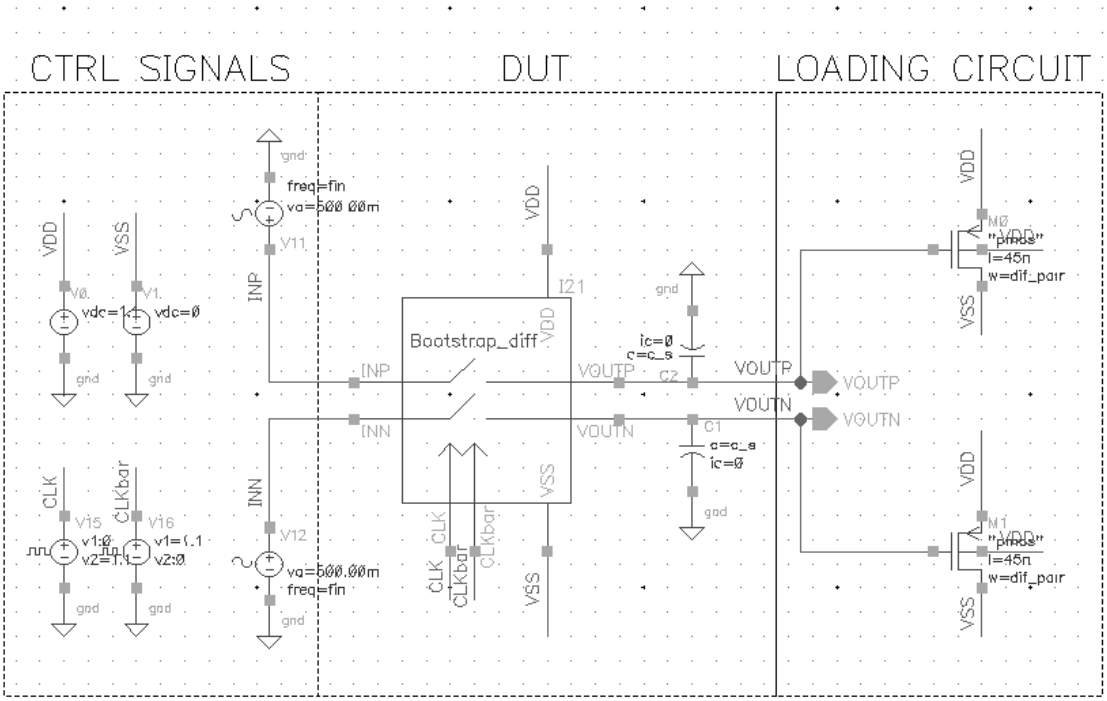
Schematic figures:







Testbenches: tb_SHBS.scs



Parameters:

Parameters	Symbols
Next stage loading (m)	dif_pair
Sampling capacitance (f)	c_s
Switch size (m)	$switch$
Sampling frequency (Hz)	fs

Metrics:

Metrics	Symbols
ENOB	ENOB
SFDR	SFDR_dB

Neural Network Model:

The H5 file: reg_SHBS45.h5

The Json File: model_SHBS45.json

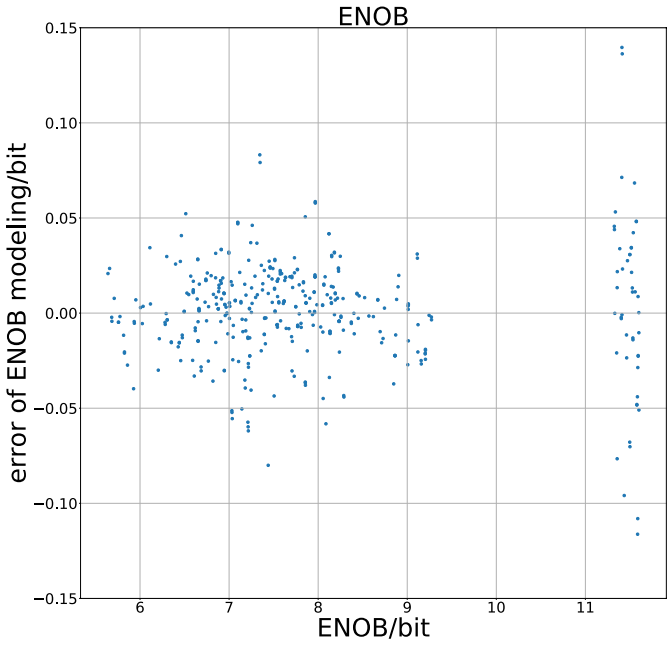
The Input Normalization File: scX_SHBS45.pkl

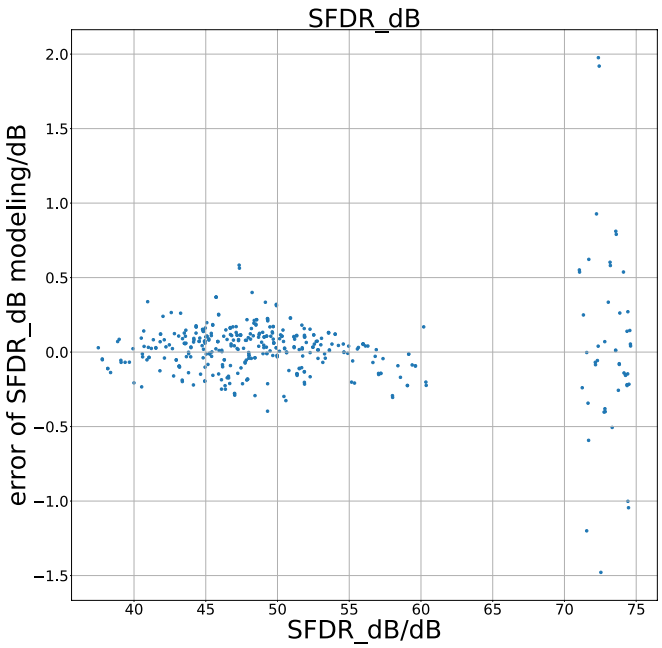
The Output Standardization File: scY_SHBS45.pkl

The input characterization range of the Model:

Design parameters	
Symbols	**Characterization Range**
dif_pair	[500nm, 540nm]
c_s	[500fF, 1.5pF]
$switch$	[800nm, 1000nm]
fs	[150MHz, 350MHz]

The error range of the Model:




SFDR_dB
error of SFDR_dB modeling/dB
SFDR_dB/dB
2.0
1.5
1.0
0.5
0.0
−0.5
−1.0
−1.5
40
45
50
55
60
65
70
75