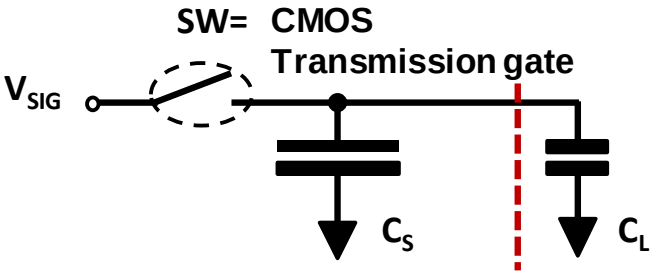
Module: Transmission gate-based Sample and Hold circuit

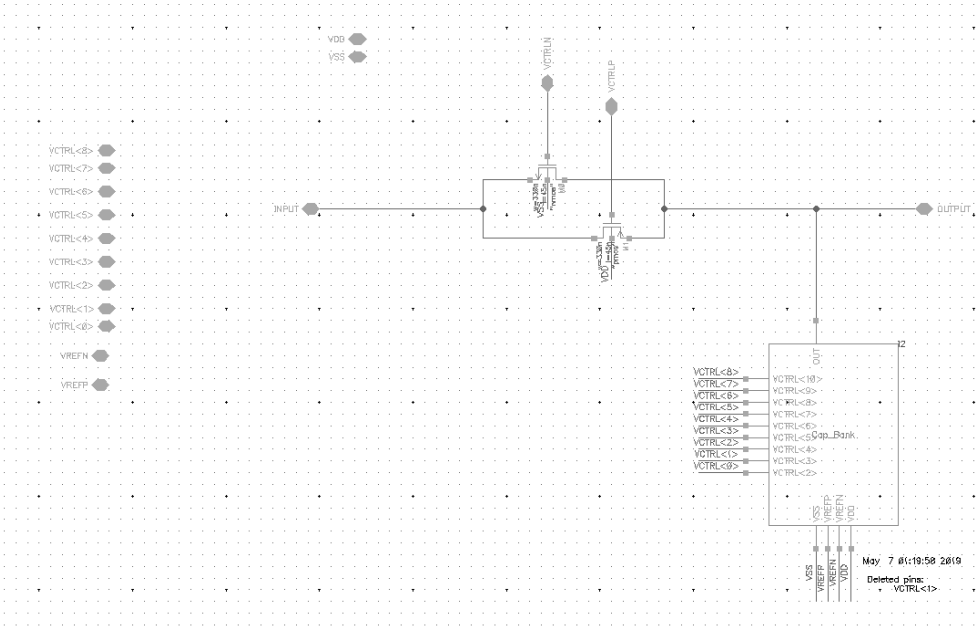
Module Description: A Sample and hold circuit based on Transmission Gate switch is implemented here. The design is a differential sample and hold switch with CDAC. This block is often used in designing SAR ADC. The simplified circuit diagram of the circuit is:



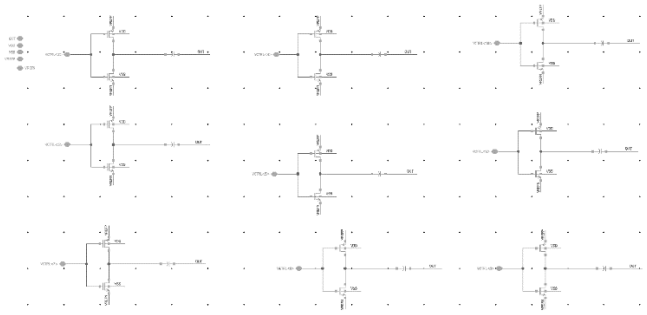
Top Cell Name: S&H_DAC

Technology: PTM 45nm CMOS

Schematic:



The Transmission Gate based Sample and Hold Circuit



Capacitor Bank (CDAC)

Schematic Netlist: sandh.scs

Testbench Netlist: sandh_parameters.scs, sandhbw.scs

Design Parameters	
Parameters	Symbols
Capacitive Load	CL
Sampling Switch Size (NMOS) (fingers)	SN
Sampling Switch Size (PMOS)(fingers)	SPP
Input signal Range	Vpp
Sampling Signal Duty Cycle	ack

Design Metrics	
Metrics	**Symbols**
SFDR of S/H	sfdr
SNDR of S/H	sndr
ENOB of S/H	enob
Power	power
Bandwidth of the S/H	bandwidth

Neural Network Model:

H5 file: sandhold.h5

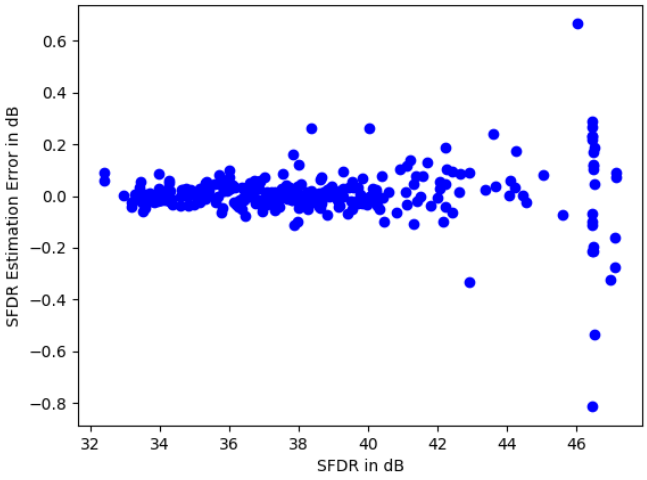
JSON file: sandhold.json

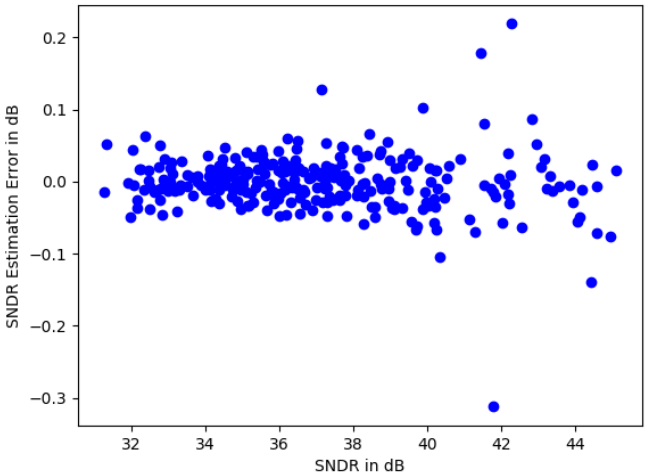
Input Normalization File: scX_sandhold.pkl

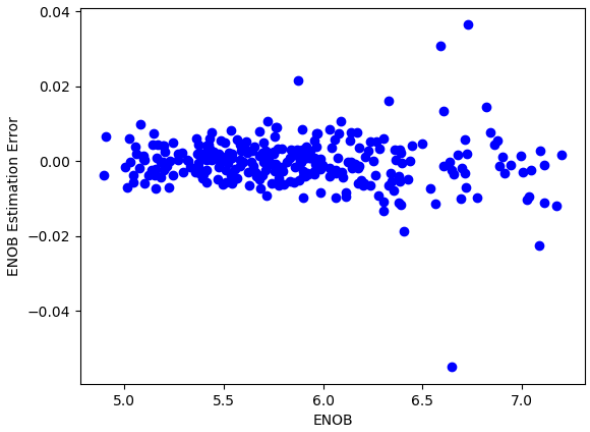
Output Standardization File: scY_sandhold.pkl

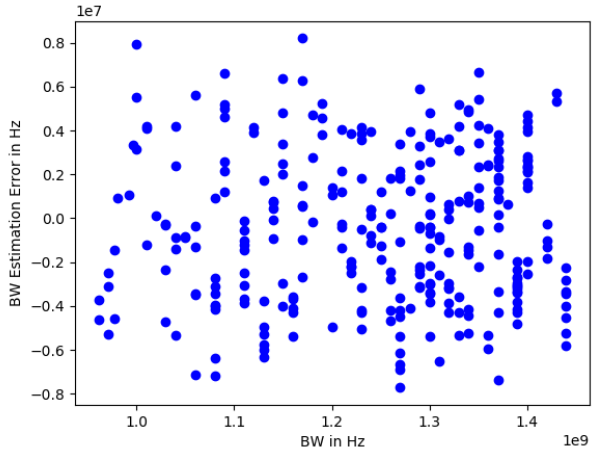
Design Parameters		
Parameters	Symbols	Search Range
Capacitive Load	CL	[10fF – 100fF]
Sampling Switch Size (NMOS)(fingers)	SN	[30-80]
Sampling Switch Size (PMOS)(fingers)	SPP	[30-80]
Input signal Range	Vpp	[350mV-900mV]
Sampling Signal Duty Cycle	ack	[250mV-450mV]

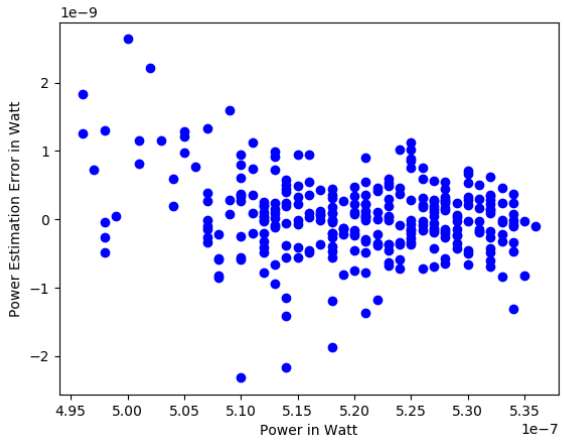
Error Range of the Model:











For further information contact: Subhajit Dutta Chowdhury (duttacho.usc.edu)