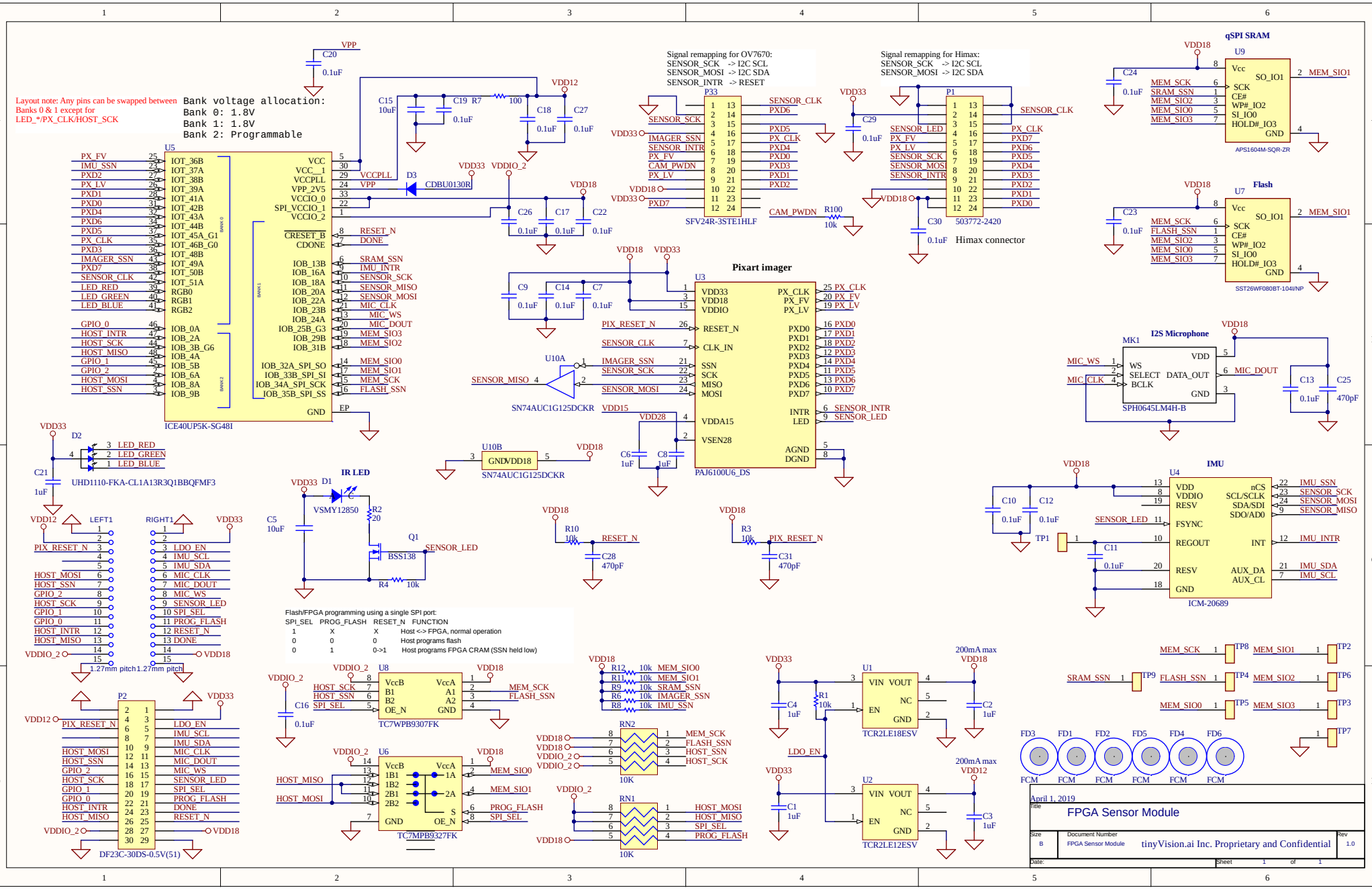
Layout note: Any pins can be swapped between Banks 0 & 1 except for LED_*/PX_CLK/HOST_SCK
Bank voltage allocation:
Bank 0: 1.8V
Bank 1: 1.8V
Bank 2: Programmable
U5
ICE40UP5K-SG48I
Signal remapping for OV7670:
SENSOR_SCK -> I2C SCL
SENSOR_MOSI -> I2C SDA
SENSOR_INTR -> RESET
P33
SFV24R-3STE1HLF
Signal remapping for Himax:
SENSOR_SCK -> I2C SCL
SENSOR_MOSI -> I2C SDA
P1
503772-2420
Himax connector
qSPI SRAM
U9
APS1604M-SQR-ZR
Flash
U7
SST26WF080BT-104I/NP
Pixart imager
U3
PAJ6100U6_DS
U10A
SN74AUC1G125DCKR
U10B
SN74AUC1G125DCKR
I2S Microphone
MK1
SPH0645LM4H-B
D2
UHD1110-FKA-CL1A13R3Q1BBQFMF3
IR LED
D1
VSMY12850
Q1
BSS138
IMU
U4
ICM-20689
P2
DF23C-30DS-0.5V(51)
U8
TC7WPB9307FK
U6
TC7MPB9327FK
RN2
RN1
U1
TCR2LE18ESV
U2
TCR2LE12ESV
200mA max
FD3
FD1
FD2
FD5
FD4
FD6
FCM
Flash/FPGA programming using a single SPI port:
SPI_SEL PROG_FLASH RESET_N FUNCTION
1 X X Host <-> FPGA, normal operation
0 0 0 Host programs flash
0 1 0->1 Host programs FPGA CRAM (SSN held low)
April 1, 2019
FPGA Sensor Module
tinyVision.ai Inc. Proprietary and Confidential
Size B
Document Number FPGA Sensor Module
Rev 1.0
Sheet 1 of 1